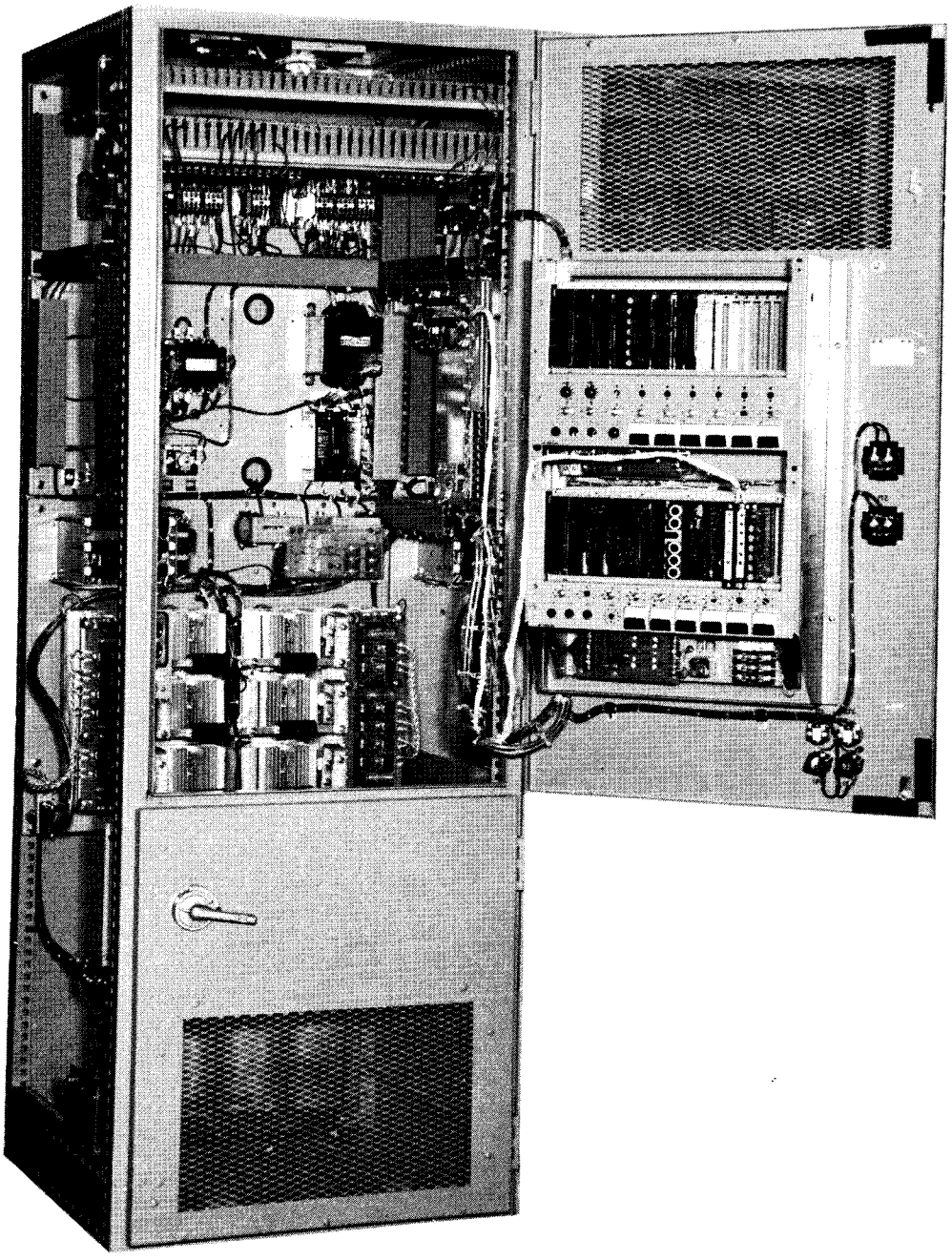


FIGURE I-1

M5B THYRISTOR POWER SYSTEM

INDEX

I. INTRODUCTION

M-5B thyristor power systems (TPS) are primarily designed to provide adjustable-voltage power for armatures of dc machines. These systems may be broken into two main parts:

(1) Thyristor power converter, consisting essentially of a thyristor power modulator (TPM), a thyristor power transformer, a basic regulator (gate control, sensor, reversing logic, ±24Vdc power supply, etc.) and of converter sequencing and protective elements.

(2) Variable regulator (process regulator), consisting of controller modules, and referencing and director logic elements.

There are two types of converters:

(a) Double converters. This type can provide output voltage and current of both polarities. This type would be used on machines which require reversing of speed (by armature control), or controlled slow down and stop capabilities as a function of regenerative capability.

(b) Single converters. Output voltage is reversible in this type, but current is restricted to one direction. It should be noted that this reverse voltage capability can be present only when forcing current toward zero. This type would be used on machines which do not require reversing by armature control, and do not require controlled slowdown by regenerative current. Many applications have sufficient load on the machine for adequate slow down and stop control without negative torque.

M-5B thyristor power converters are normally supplied by three phase lines of 460 volt - 60 hz, 550V - 60 hz, or 380V - 50 hz. They cover an output power range of approximately 30A to 660A continuous at rated voltages of 240 volts and 500 volts. The variable regulator is needed to complete a system for such functions as bus voltage regulation, current regulation, speed regulation, or combinations thereof.

A constant potential or adjustable voltage exciter can be added. They have a rating of up to 18 Amps, and are used to excite the field of the dc machine whose armature is powered by the main converter.

The entire TPS may be contained in a single, self-ventilated, NEMA I enclosure; or the TPM, regulator, and sequencing and protective elements can be mounted on an open panel with the transformer, transformer breaker, and line fuses (if used) separated from the panel lineup.

II. THYRISTOR POWER CONVERTER (TPC)

A. Phase-Controlled Converter Principles

A thyristor power converter is an apparatus which by means of phase-controlled gating of thyristors (or other controlled rectifier cells) converts as ac supply line voltage into an adjustable dc voltage; this process is known as rectifying. Inversely, dc voltage can be converted back into the ac line voltage; this mode of operation is called inverting. A converter which only can perform one of these functions is called a rectifier or an inverter, respectively.

Once a thyristor is turned on, it can only be turned off by reducing the anode current to a very small value. In the phase-controlled oonverters, the ac line voltage performs the function to end the conduction period by commutating the anode voltage.

Many converter configurations have been developed. The six-phase, double-way circuit (three-phase bridge) has evolved as the preferred arrangement for thyristor power supplies. It is simple and offers the best thyristor and transformer utilization. Figure II-1 shows the elementary schematic of such a converter for a six-phase system. The transformer is shown delta-wye connected, but the inverse may be used. It is desirable to use the delta connection for at least one winding to eliminate flux ripple of the third harmonic in the core. The main purpose of the transformer is to adjust the line voltage to the proper level, to provide isolation and to introduce inductance into the converter current path. This inductance (or added reactors) is required to control the rates of currents during commutation and faults as will be seen later. The dc output side of the converter is connected to a load circuit consisting of a counter e^{mf} e_a resistance R_d and inductancd L_D.

The significant current paths and waveforms can now be developed (Figure II-2). The uppermost traces show the secondary line voltages, measured from the first terminal letter to the second terminal letter. Initially, all thyristors are assumed to be in the blocking state.

At $\omega\tau = 15^0$ a pulse train of 120^0 duration is applied to thyristor No. 6. Since there is no other thyristor gated at this time a current path is not available to carry current. Sixty degrees later at $\omega\tau = 75^0$, a pulse train of 120^0 duration is applied to thyristor No. 1. Now with thyristors No. 6 and No. 1 receiving synchronized pulses a current path is available from U to P through the load to N and then to V. Thus the line voltage euv is applied to the load. Sixty degrees later at $\omega\tau = 135^0$ a pulse train is applied to No. 2; current is flowing in No. 6 and No. 1 at this time, however, the current in No. 6 will commutate to No. 2 because the voltage euw is greater than euv. Pulse trains are applied to successive thyristors each 60^0 and commutations will take place each 60^0 (on the negative side of the bridge when even numbered pulses are applied and on the positive side of the bridge when odd numbered thyristor gates are applied.)

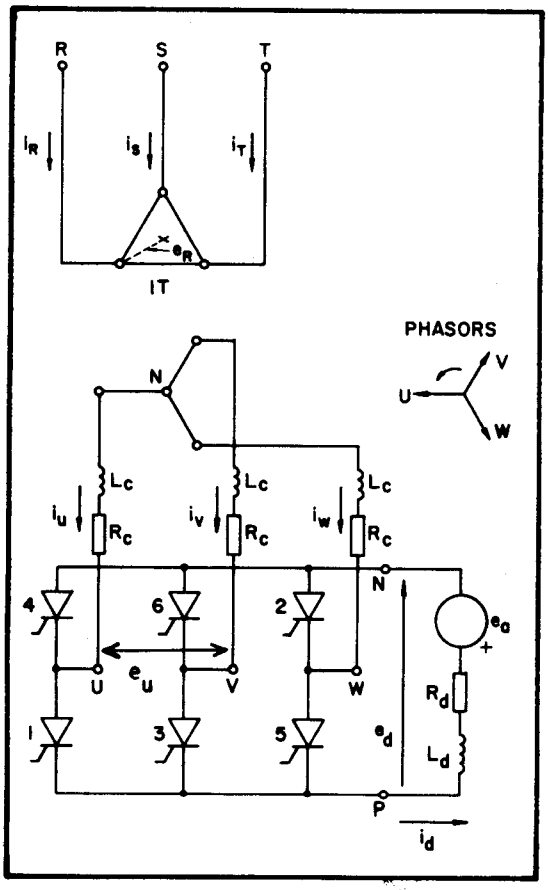


FIGURE II-1

SIX-PHASE, DOUBLE-WAY CIRCUIT

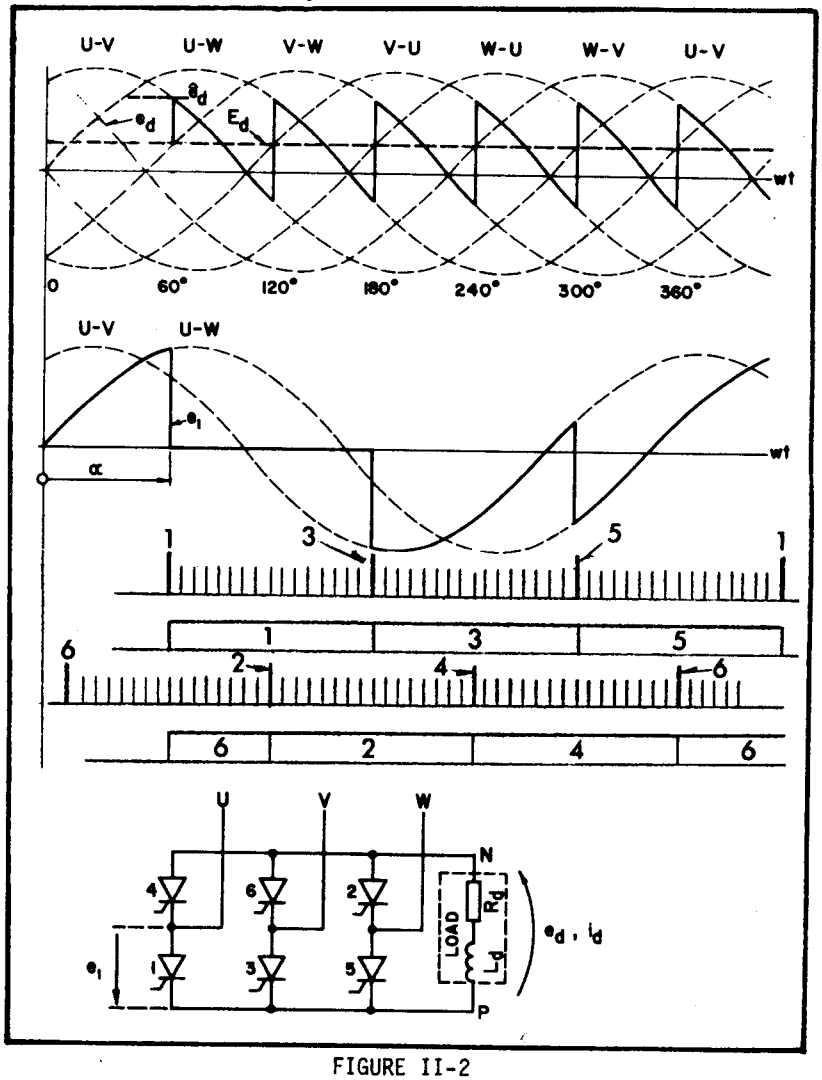


FIGURE II-2

WAVEFORMS OF THYRISTOR CONVERTER AT $\alpha = 75^0$

Assuming that the load is highly inductive, the dc current will reach a steady value after a number of cycles, and each tyy-ristor will then conduct a 120^0 wide current block each cycle. The respective waveforms of the thyristor anode-cathode voltages can now be easily developed. Figure II-2 illustrates this for a gating angle of $\alpha = 75^0$. Note that α is measured from the point where the anode-cathode voltage of the respective cell swings positive. Hence, for $\alpha = 0$, the thyristors do not have to absorb any positive voltage anymore and are then comparable to simple diodes. It is apparent from the waveshapes of the output voltage that its average value E_d is a function of the gating angle. It reaches a maximum at $\alpha = 0^0$, is zero for $\alpha = 90^0$ and assumes negative values back to $\alpha = 180^0$. This transfer curve can be obtained by integrating the waveforms. The result is:

$$E_d = E_{do} \cos \alpha$$

where the saturated output voltage is

$$E_{do} = \frac{3\sqrt{2}}{\pi} E_u$$

where E_u ··· line-to-line rms ac voltage.

Since the load current cannot reverse, the average power flow will change its sign with the voltage. Rectifier operation ($\alpha < 90^0$) renders motoring in the load circuit whereas inverter operation ($\alpha > 90^0$) requires the load to be generative.

Figure III-3 illustrates the range of operation on a time basis. In the beginning, the converter is operated in its rectifying mode with $\alpha = 0$. Then α is steadily increased into the inverter mode of operation. The lower trace shows the voltage across one of the thyristor legs.

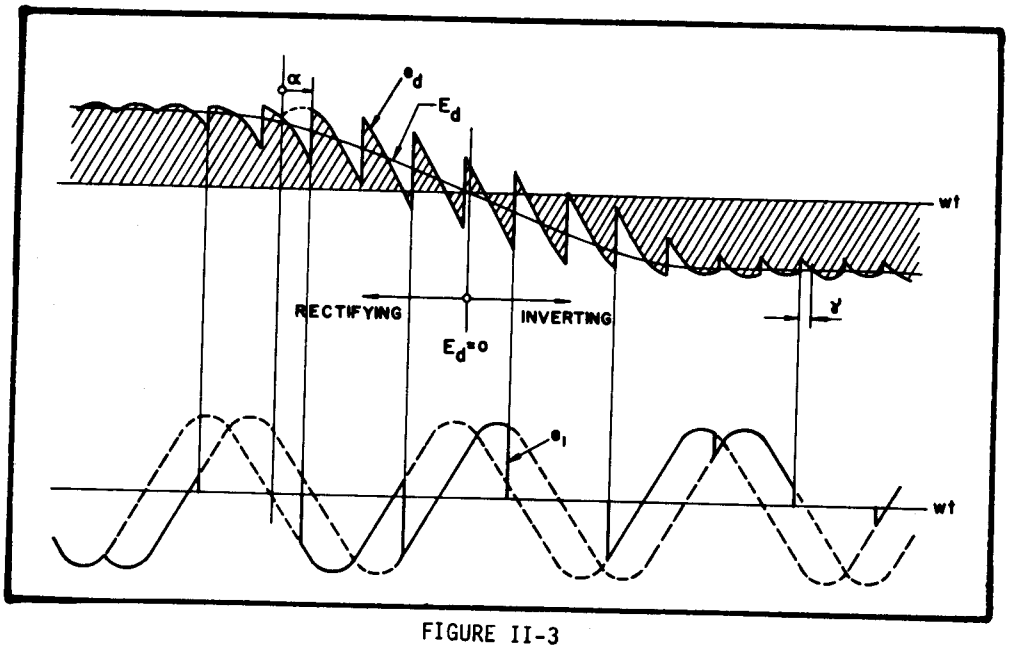


FIGURE II-3

RANGE OF OPERATION ILLUSTRATED ON A TIME BASIS
ON THE LEFT, $\alpha = 0$, RECTIFYING MODE.
α THEN INCREASES TO INVERTER MODE

Up to this point, the reactances offered by the transformer, reactors in the ac line and the power line have been neglected. This so-called commutating reactance, however, is significant. Instead of instantaneously commutaing the load current from one leg to another leg (upon gating of the latter), the current rate is limited and shaped by it. This means that both these legs conduct simultaneously for a period of time, shorting out effectively the ac source. This produces notches in the sinewave measured on points U-V-W, which, in turn, reduce the dc bus voltage.

Taking account of these commutation effects, one can derive a converter equation which includes this reactive drop:

$$E_d = E_{do} \cos \alpha - E_{do} \tfrac{1}{2} x_c I_d/I_{dn}$$

where x_c --- relative reactance of transformer, ac reactors and line (based on I_{dn})

I_d --- actual dc current

I_{dn} --- nominal (rated) dc current.

The assumption made so far was that the dc load current is continuous, and the equation applies for this condition only.

In a practical circuit such as commonly found with dc motor armatures as load, the actual operation always covers the range of discontinuous current at light load levels also. Reducing the load current, one finally reaches a level where the ripple amplitude is high enough to interrupt the current cyclicly. At this transition point, the regulation characteristic takes a sharp break and aims to a point equal to the peak converter voltage e_d at zero load current. This transition point depends on the gating angle α, the inductance and the losses in the load circuit.

Commutation from a first leg to a second must always be completed before the anode voltage of the second leg swings negative. If the latter should happen, the commutation is incomplete and the full-load current will commutate back into the first leg. This situation can only arise if the commutation was initiated at a high gating angle (in the inverter range) and if the load current is continuous.

The circuit described so far can provide voltage of both polarities. The current, however, can only flow in the conducting direction of the rectifying cells. This circuit is, therefore, classified as unidirectional or single converter.

If current reversal is required, a second converter can be added and connected to the first one in an antiparallel circuit as shown in Figure II-4. Since such a circuit can produce load current in both directions, this circuit is classified as a bi-directional or double converter.

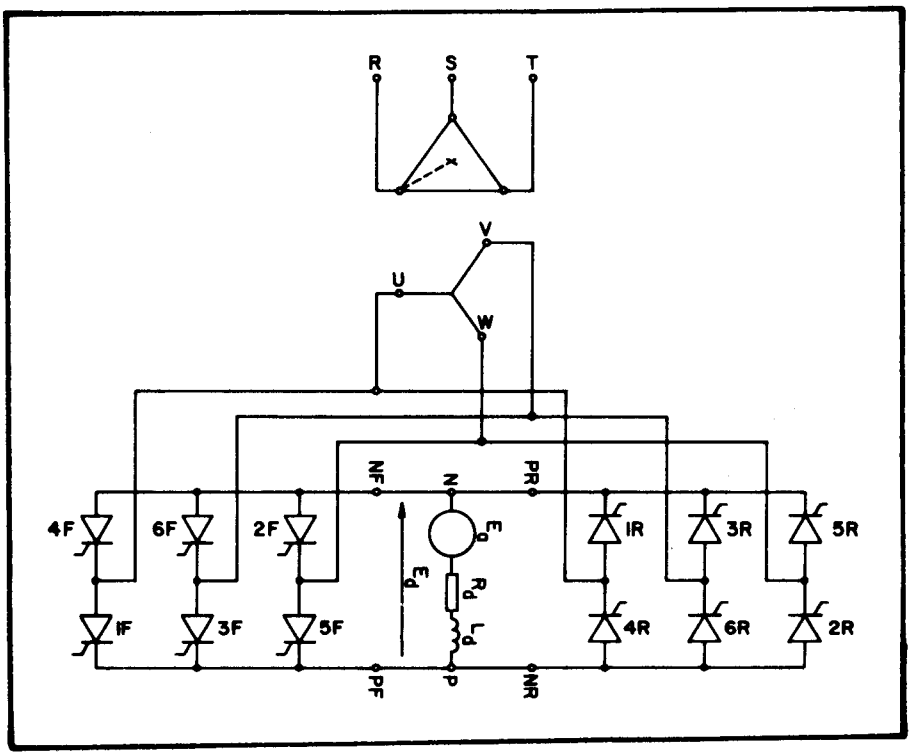


FIGURE II-4

DOUBLE CONVERTER, ANTIPARALLEL CIRCUIT

There are several ways to control such a double converter. The principle used in M-5B is to use one gate pulse generating system shared by two (forward and reverse) pulse amplifiers (Thyristor Gate Drivers); with a logic system so that only one Thyristor Gate Driver (TGD) can be operative at any time. The logic and control system determines whether the forward or reverse converter should be gated. The operation will now be explained with the help of Figure II-5 and Figure II-6. The systems diagram shows the main control elements of the double converter, with the power circuit in single line diagram form. An inner voltage loop is closed. This regulating loop helps greatly to overcome the nonlinearities of the power converter when going from continuous to discontinuous current. This loop makes it possible to consider the converter system for the outer (variable regulator) loops as a "black box" amplifier with nearly ideal (linear) characteristics.

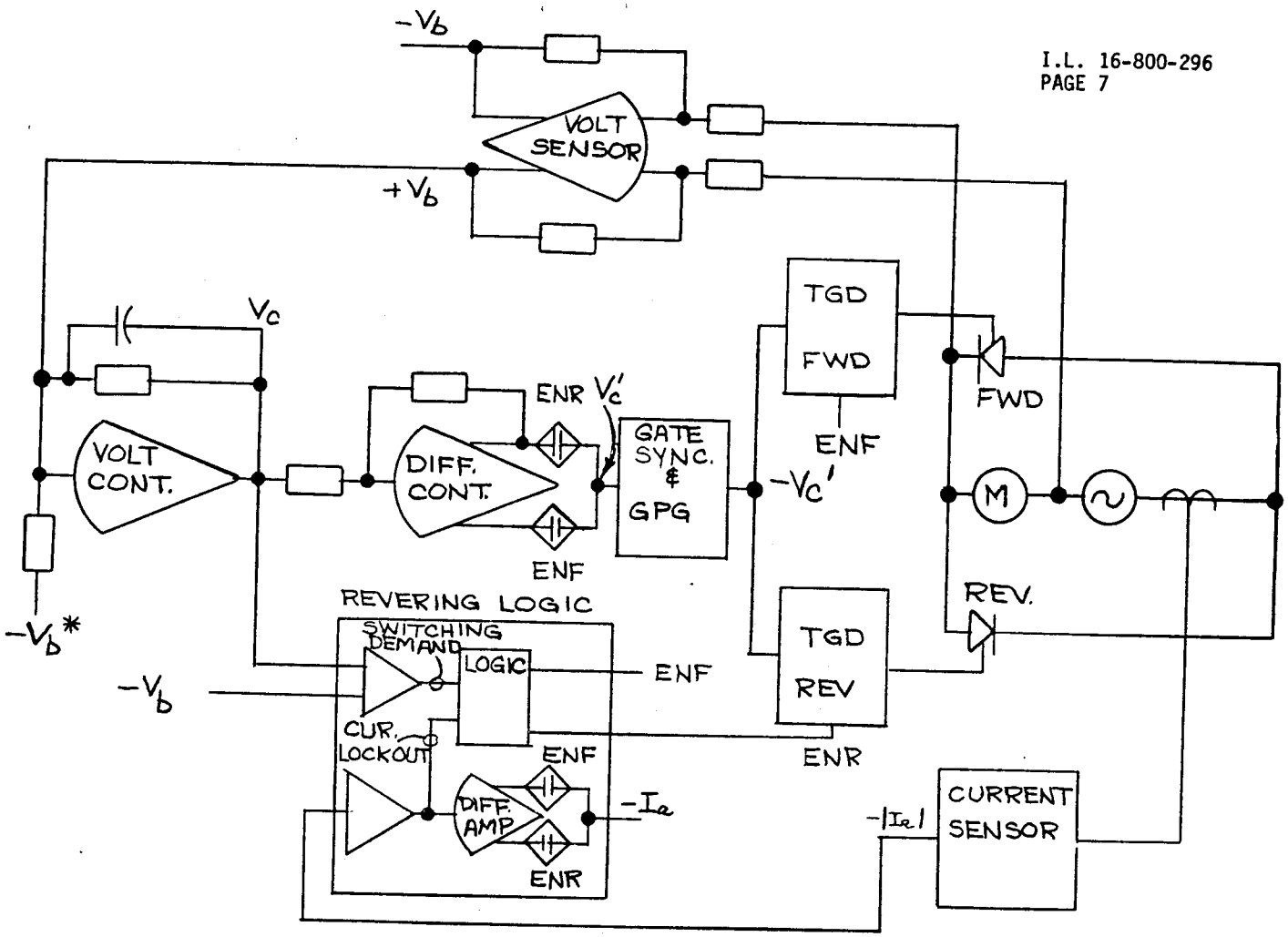


FIGURE II-5
DOUBLE CONVERTER CONTROL SYSTEM

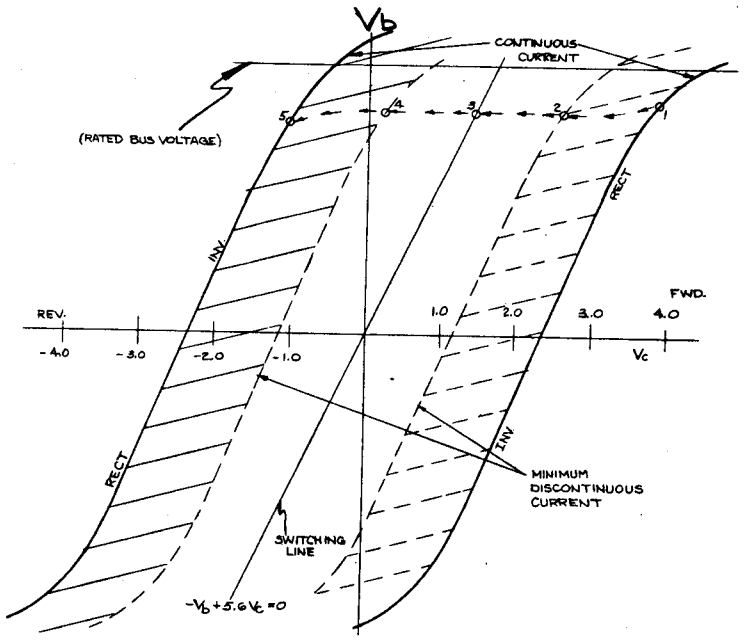


FIGURE II-6
DOUBLE CONVERTER CONTROL CHARACTERISTICS

The bus voltage is picked up by the voltage sensor (VS) and brought to one input of the voltage controller (VC) where it is compared with the reference voltage $-V_b^*$ applied at a second input. When both inputs are zero, V_c will be zero as will V_c' which corresponds to a gating angle of $\alpha = 145^0$ due to a bias in the gate synchronizer (GS).

In operation, depending on the polarity of the difference of the two input voltages to the voltage controller, control voltage V_c will swing positive or negative. By comparing this voltage V_c with bus voltage $-V_b$ the polarity of required converter conduction can be determined. For example, if bus voltage V_b is smaller than the reference $-V_b^*$, forward load current is indicated, and therefore the forward channel of the double converter should be pulsed. Under this condition V_b is positive going and compared with $-V_b$ at the input of the reversing logic will result in ENF to be a logic "1" and pulsing from the forward TGD is released. If now the reference $-V_b^*$ is reduced to demand reverse current, the opposite sequence of events will take place.

Figure II-6 shows the output of the power converter as a function of V_c for the cases of continuous and minimal discontinuous (pulsing) current. The shaded area between represents the field of various possible states of discontinuous current conduction.

It should be noted that the signal V_c' going to the GS is equal to V_c when forward gating is required; and equal but opposite to V_c when reverse gating is required. The gating system requires a negative going (legs positive) voltage to phase advance, therefore an absolute value circuit is used (represented in Figure II-5 by DIFF. CONT. and logic contacts on its outputs) to invert V_c' from V_c when the reverse TPM is being gated. This inversion is also required to establish the proper polarity (always negative feedback) for total loop gain.

The case of minimal discontinuous current is mainly of interest for armature loads. It is representing the case for a gating angle adjustment where the peaks of the converter output voltage (e_d) are just matching the counter emf of the motor (See Figure II-2). For any higher gating angle no current conduction can set in any more. This then means that no current flow can continue in the area passed the minimum discontinuous current line. Shifting into this area indicates that current of the opposite polarity is required. However, to simplify the sensing of this condition and to add some safety margin, actual switching is initiated when the indicated switching line is crossed.

As shown in Figure II-6 current will be zero when switching from forward to reverse gating under normal operating conditions. However, some fault conditions can occur (inverter fault for example) which would ask for a gating reversal with current flowing. Also in the reversing logic is a current lockout feature which prevents gating crossover until current drops to a very low value (less than 5% of rated current) so that circulating current faults will not be initiated due to other faults. Shown in the reversing logic as well in a polarity selector for current feedback. This is shown as a differential amplifier with reversing contacts on the output. Current feedback is negative for forward current. and positive for reverse current.

With the converter in the forward conduction mode, a reversal shall now be described. The counter emf e_a of the load is assumed to be as shown in Figure II-6 with the forward converter rectifying at point 1. Enable forward (EN FWD) is a logic "1" and forward gate pulses are released. Suddenly the reference $-V_b^*$ is lowered to a value below e_a demanding a current reversal. This will cause the VC output voltage V_c to advance toward negative values. At point 2, forward current will stop altogether; and at point 3, the reversing logic will be initiated. EN FWD will become a logic "0" stopping forward pulses. About 2ms later EN REV will change from a logic "0" to a logic "1" releasing reverse pulses. At point 4, the reverse converter starts to pick up current in the inverting mode. Finally at point 5, the new quiscent state of reverse conduction has been reached where V_b is again matching the reference $-V_b^*$.

The opposite sequence of events take place in case of a change from reverse to forward current. Figure II-7 shows an oscillogram of a current reversal in a double converter with current regulator.

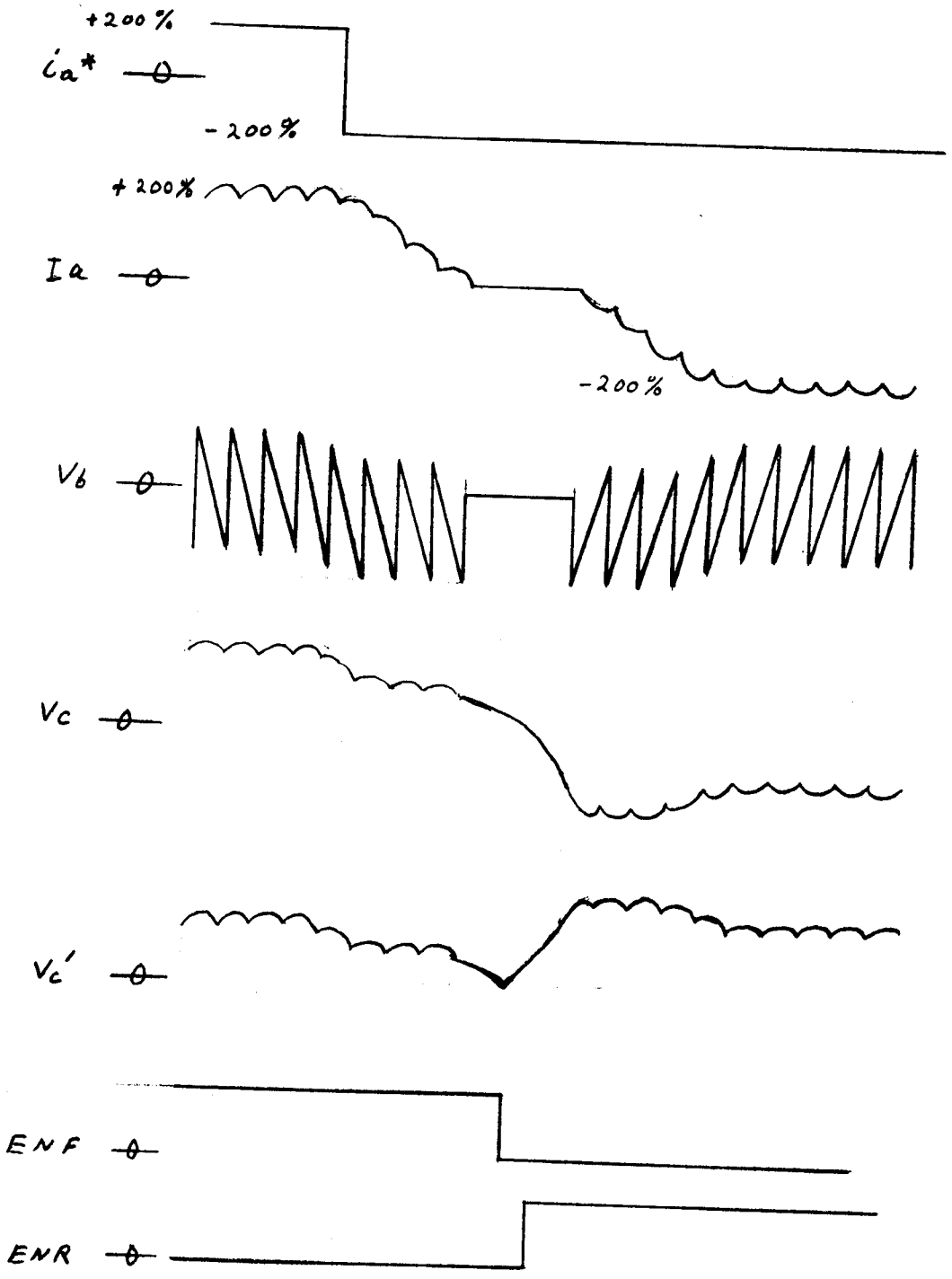
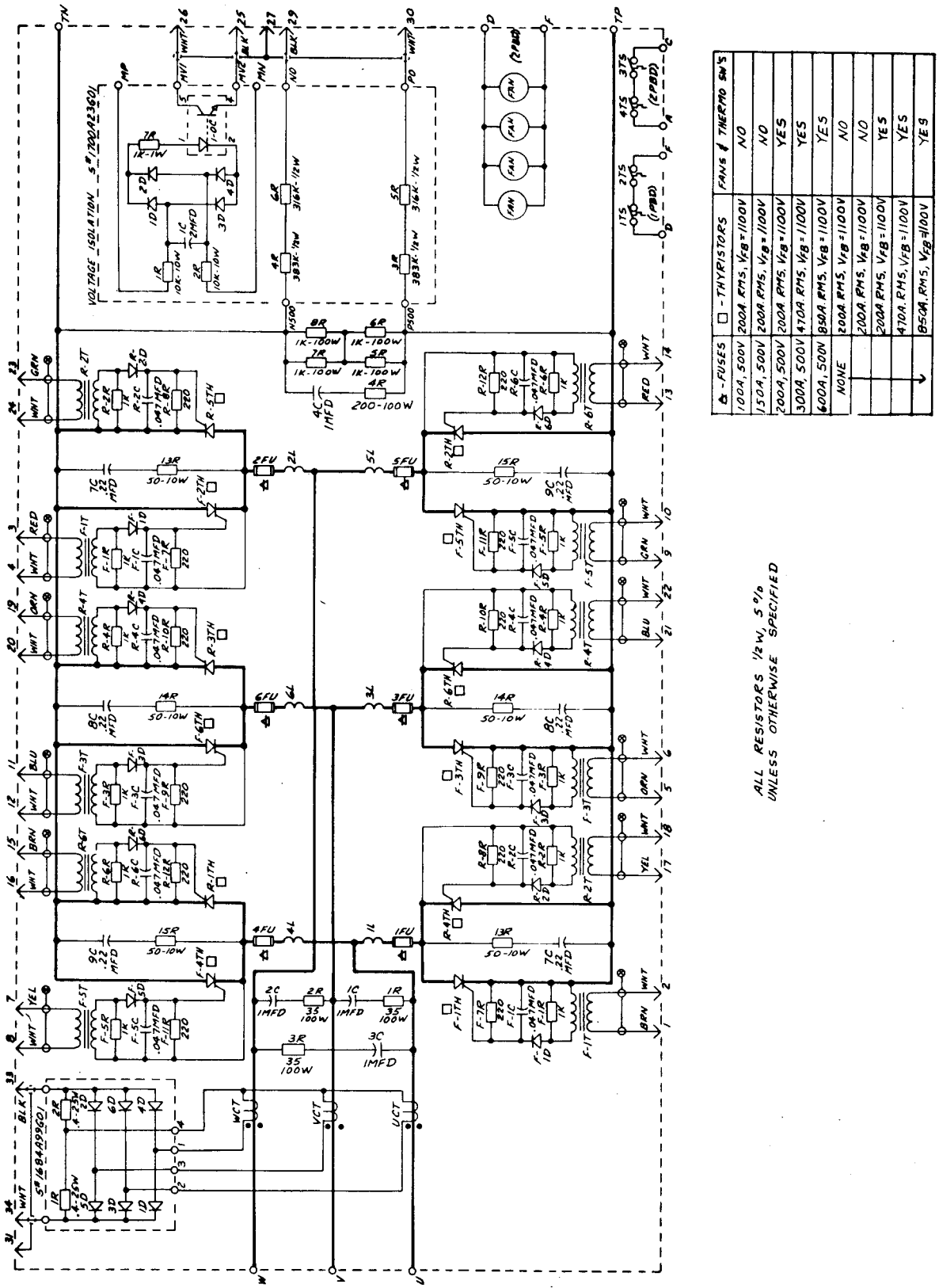


FIGURE II-7

B. Thyristor Power Modulator (TPM)

This assembly includes the thyristors mounted on heat sinks in a six-pulse, bridge circuit. Two thyristors are connected in antiparallel in the case of double converters. This TPM also contains current transformers, current sensor, thyristor R-C networks, thyristor gate pulse networks, preload resistors, AC and DC R-C networks, ferrite core assemblies, an attenuator network for voltage feedback, and a static motor voltage sensor. Fans are used on sizes greater than 150A, with thermo switches added for air loss detection. For class III protection fuses are included. A typical diagram is shown on Figure II-8.



Δ - FUSES	□ - THYRISTORS	FANS & THERMO SW'S
100A, 500V	200A RMS, V_{FB} = 1100V	NO
150A, 500V	200A RMS, V_{FB} = 1100V	NO
200A, 500V	200A RMS, V_{FB} = 1100V	YES
300A, 500V	470A RMS, V_{FB} = 1100V	YES
600A, 500V	850A RMS, V_{FB} = 1100V	YES
NONE	200A RMS, V_{FB} = 1100V	NO
	200A RMS, V_{FB} = 1100V	NO
	200A RMS, V_{FB} = 1100V	YES
	470A RMS, V_{FB} = 1100V	YES
↓	850A RMS, V_{FB} = 1100V	YES

DOUBLE CONVERTER TPM
FIGURE II-8

The TPM has current ratings of 150A, 250A, 360A, and 660A with voltage ratings of 240V and 500V. For class III protection, fuses protect thyristors from circulating current faults and inverter faults by melting and clearing the fault. For class I protection, an ac thyristor breaker and dc breaker mounted on the contactor panel, with a high impedance transformer is required to protect thyristors, and fuses are not used.

Thyristor R-C networks are used to store hole recovered charge from thyristors at turn off of current. Ferrite core assemblies attenuate excessive rates of voltage, which otherwise may lead to undesired turn on of thyristors. R-C network across the AC line and DC output damp the oscillations that would otherwise be produced by the commutation process. Gate pulse transformer networks provide isolation and shaping for the gate pulses.

Three current transformers are connected in a wye network across the current sensor bridge and to the center point of the burden resistor. This rectified signal of the ac line currents is a true reflection of the dc load current flowing during operation. The current feedback (term 33) is always negative. Three sizes of CT's are used; 200 to 5, 400 to 5, 600 to 5. Voltage at term. 33 with respect to term. 34 is:

$$-I_a = I_{dc} \times \frac{5 \times .76 \times \text{PRI TURNS}}{\text{CT (200, 400, or 600)}}$$

More than 1 primary turn is only required on the 200 to 5CT and where the rated dc current is below 120A.

The static motor voltage sensor picks up when motor voltage exceeds about 20V. This signal is used in the regulator sequencing to prevent contactor pickup should the motor have appreciable voltage on at the time of contactor initiation; providing the function previously performed by a VR relay.

The five power connections (3ac and 2dc) are bolted connections to studs. Connections of gate leads from the regulator, and feedback signals to the regulator are made with a single plug connector. Connections to the fans and thermo-switches are screw terminal connections on the pulsing boards

C. Basic Regulator

The regulator cage usually includes variable as well as basic regulator boards. The basic regulator is defined to include all functions from the input to the voltage controller to the TPM. There are two basic styles for the basic regulator:

(1) Double Converter. This basic regulator includes all components required to close an inner voltage loop, to sense bus voltage, to sense the demand and execute current reversals, and to provide gate pulses to the TPM. An internal dc power supply provides for all basic regulator circuits, and also provides for variable regulator boards housed in this same cage.

(2) Single Converters include the same components except the reverse thyristor gate driver (TGD) and the reversing logic function is not included.

Figure II-5 shows the basic regulator in a simplified form. The basic regulator may be further broken down, with the gating system being the major portion of this regulator.

1. Gate Pulse Generating System

The M5B gate control system consists of a gate control transformer (GCT) S#1295A25; the reversing logic portion of the voltage controller card (VC & RL) S#1757A01 for double converters; portions of the gate sync card (GS) S#1710A08 for 60 hz operation, S#1752A12 for 50 hz operation; two gate pulse generator cards (GPG) S#1671A17; two thyristor gate driver cards (TGD) S#1668A25 for double converters, one for single converters; some components associated with the pulsing circuits of the thyristor bridges; the inhibit (INA) and gate pulse suppression ($\overline{GPS}$) functions of the protection board; and the interconnecting wiring.

Features designed into the M5B Gating System are:

(1) Reversing Logic - Only one converter can be gated at a time.

(a) Primary Crossover Logic - Comparison of voltage feedback to voltage demand signal, which is generated internally in the VC&RL, to determine whether forward or reverse converter operation is required.

(b) Current Crossover Lockout - Crossover cannot be initiated when current is greater than 5% of rated. Current will always be zero when crossover is asked for under normal operating conditions. Under certain fault conditions (inverter faults) crossover could be asked for with high current flowing, by the voltage crossover logic, however, the current lockout feature prevents crossover faults to be generated on top of initial fault.

(c) Bias - Is preset for the regulating system used. It assures smooth initiation of current and voltage at start of gating and smooth crossover.

(2) Synchronizing Signals - Are spaced precisely 60^{o} apart.

(a) Gate Control Voltages - From GCT are directly in phase with the TPM supply voltage. In most cases the primary of GCT is taken directly off the TPM transformer secondary. In this case gating is correctly phased with no change in gate control wiring, regardless whether TPM supply transformer is delta-delta, wye-delta, or delta-wye.

(b) Sync Signal Generation - Zero crossing detection of GCT waves only, and are well filtered. Filtering virtually eliminates distortion due to commutation notches and higher frequency harmonics. Zero crossing detection eliminates any effects of line amplitude fluctuations.

(3) Phase Advance Limit - Fixed at 0^{o}. No additional margin required in TPM transformer as would be the case for a fixed at greater than 0^{o}.

(4) Picket Fence Gating - Pulses are delivered directly from firing transistor in TGD or GPA to thyristor pulse transformer to be fired. No steering diodes required as in double pulsing. Pulsing power supply is a highly filtered dc supply and is immune to large line distortion and fluctuations. Gating power is not sensitive to phasing.

(a) Hard Pulse - Gives large overdrive to thyristors for quick turn on at first pulse; when high di/dt can occur, for discharging r-c networks in conjunction with commutation of high current levels.

(b) Trailing Pulses - Are available and required to refire thyristors when operating under light load, discontinuous current operation. They are of reduced amplitude and duration to reduce loading on the gate.

(c) Tail End Chop - Shortens pulse train (to less than 120^{o}) where gating cannot be required when operating at high delay angles. This reduces reverse leakage dissipation when thyristors have reverse voltage applied.

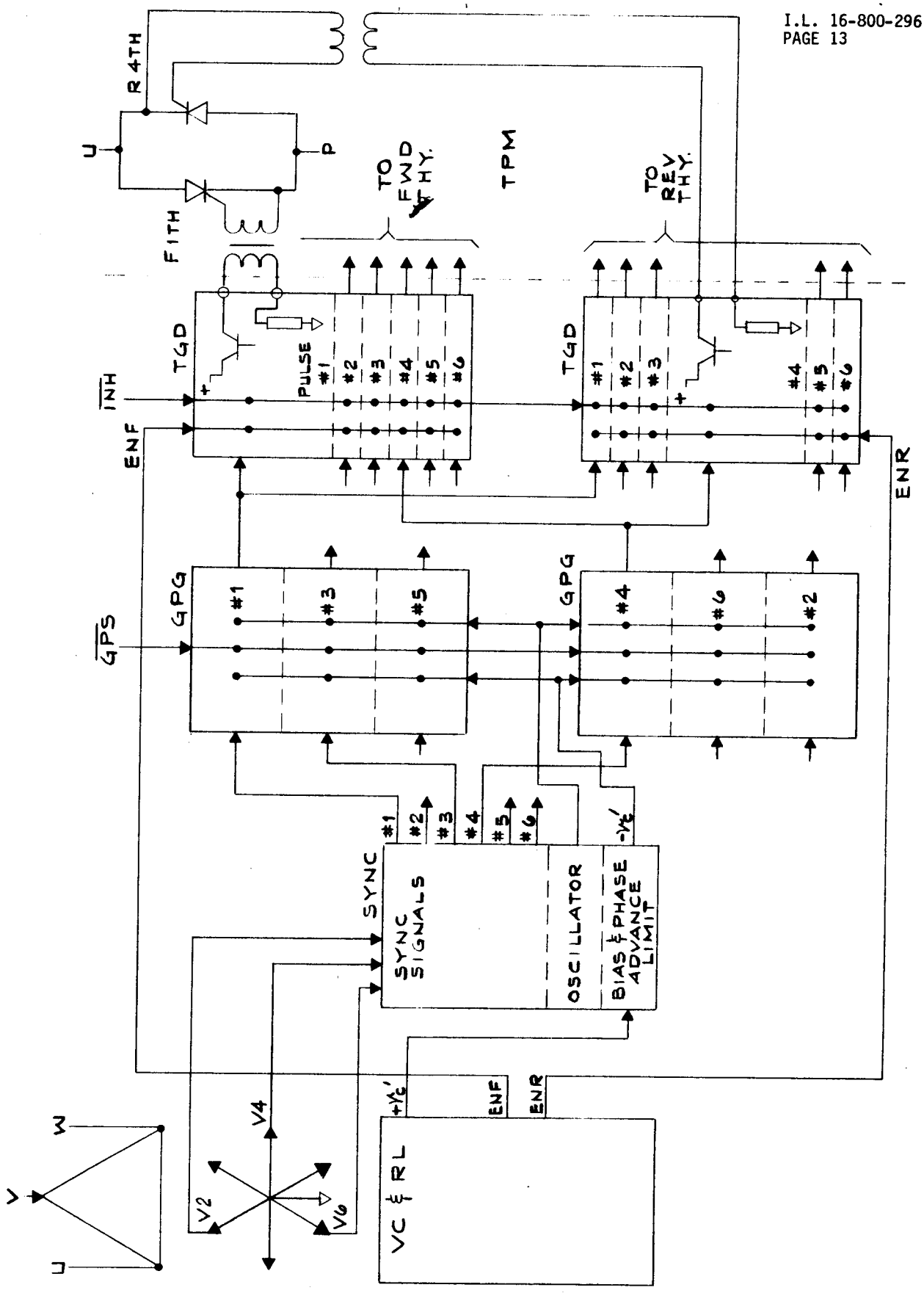
(d) Ramp Gating - Generates six pulses at 60^{o} intervals with variations of less than 1^{o} at $\alpha = 180^{o}$ which is worst tracking angle. Phase angle is directly proportional to control voltage over the range of $0 \leq \alpha \leq 180^{o}$.

(e) Ring Counter - Turns off preceeding pulse in its half of the converter (3 turns off 1, etc.) as preceeding pulses are no longer required under any operating conditions.

(5) Adjustments - None are required within the gating system.

Figure II-9 is a simplified diagram of the gating system showing important signal points required to generate pulses.

The VC & RL establishes a phase angle demand signal $+v_c$. It as well establishes which converter, forward or reverse, is to ge gated with signals ENF or ENR.



GATE PULSE GENERATOR
FIGURE II-9

The GS has three functions associated with gate control. It receives three sinusoidal waves displaced 120° which are in phase with the TPM supply voltage. It uses zero crossing points to generate 6 sync pulses displaces 60° which start, and at a later period reset, timing ramps in the GPG. A 12k hz free running oscillator is also located on this board and is used as clock pulses for all trailing pulses generated. The third circuit on the GS provides the bias and phase advance limit function which conditions the phase demand signal ($+v_c$ to $-v_c$) from the VC & RL before it goes to GPG.

The GPG(s) process the sync signals (1, 3, 5 and 4, 6, 2), phase control signal ($-v_c$), clock pulses, as well as $\overline{GPS}$ permissive signal to generate a pulse train(s) with proper starting phase angle, correct width of pulses, and correct termination of pulses. A sync signal of 240° duration starts a timing ramp at 10 prior to $\alpha = 0^o$. Signal $-v_c$ determines at what time ($0^o \leq \alpha \leq 180^o$) after start of ramp the pulse train is triggered. The width of the hard pulse (first pulse) is timed within the GPG. Clock pulses are mixed with a timing window to provide trailing pulses. The first pulse and trailing pulses are not synchronized; first pulse timing is determined only by $-v_c$, and trailing pulses are determined by clock pulse timing following a first pulse. With $0^o \leq \alpha \leq 110^o$ pulse train are of 120° duration with each GPS ring counter terminating with pulses (3 turns off 1, 5, turns off 3, etc., for 1 GPG; 4 turns off 2, etc., for 2 GPG). The ramp is reset at $\alpha = 230^o$ by the sync signal, and any trailing pulses remaining are terminated; therefore with $110^o \leq \alpha \leq 180^o$ pulse trains are shorter than 120°. Signal $\overline{GPS}$ must be a "1" to allow any pulses to occur.

The TGD amplifies pulses from the GPG. In systems where parallel thyristors are not employed (up to approximately 500 HP) the TGD shapes as well as amplifies pulses for thyristor gating, with pulses in the first 150usec of greater amplitude than remaining pulses. A logic "1" signal (ENF or ENR) is required for gating to be allowed and only one TGD in double converters can be operative at a time. Signal $\overline{INH}$ must be a "1" to allow pulsing. $\overline{INH}$ is delayed from $\overline{GPS}$ by 100 usec so that if GPS occurs during a first pulse, the first pulse and only this pulse will be allowed to proceed through the TGD to thyristors.

The M5B Gating System I.L. 16-800-289 includes description of operation for the VC & RL, GS, GPG, and TGD. It also includes functional schematics and illustrative waveforms. Please refer to that I.L. for more detail of individual gating boards.

2. Voltage Sensor (VS)

This module is used to sense the dc bus voltage and to transduce it to a regulator signal for use in the basic regulator. A transistorized differential amplifier with excellent common-mode rejection is utilized in an op-amp manner. The output voltage are essentially independent of the bus potential to ground, but reflect only the difference of the potentials at P and N. The input attenuator is adjusted to yield output voltages of ±9.6V for nominal bus voltage. For a detailed description as well as ratings and characteristics, refer to I.L. 16-800-130.

3. DC Power Supply

The power supply consists of the following essential parts:

Rectifier transformer
Bridge rectifiers
Filter capacitors
±24V, +15V series regulator module

The transformer, diodes, filter capacitors, and fuses with a sub assembly pc board are used as a pre regulator S#1725A02 and is mounted on the magnetic panel. The transformer has a 115V ac primary and three isolated secondary windings. Twelve diodes used as three single phase bridges are used with transformer secondary windings and filter capacitors to generate unregulated supplies of about 40V, 40V, and 25V. Fuses are used to protect transistors in the series regulators should there be a short circuit at their outputs.

The series regulator pc board has three identical circuits. The two 40V supplies are used with series regulators to generate ±24V; the +25V supply with its series regulator is used to generate +15V. Adjustment pots are used to factory set the voltages at +24V, -24V, +15V and should not require adjustment in the field. Light emitting diodes are used. These LEDs will go out should its fuse blow.

The unregulated +25V supply is also used for gate power. The above power supplies are only sufficient to power boards located in the regulator cage.

D. Converter Sequencing and Protection

Figure II-10 shows a single line diagram of a double converter armature supply. The ac voltage is brought from the customer feeder to an ac breaker (device 52), which depending on the short circuit capacity may be followed by current limiting ac fuses. This breaker is feeding the gate control and regulating system as well as the thyristor transformer. It may therefore be located in the customer distribution center. This common supply without interlocking of the TPM and gate control is made possible by a design feature of the sequence and protection board (S&P) which eliminates any spurious pulsing during the a-c turn on transient.

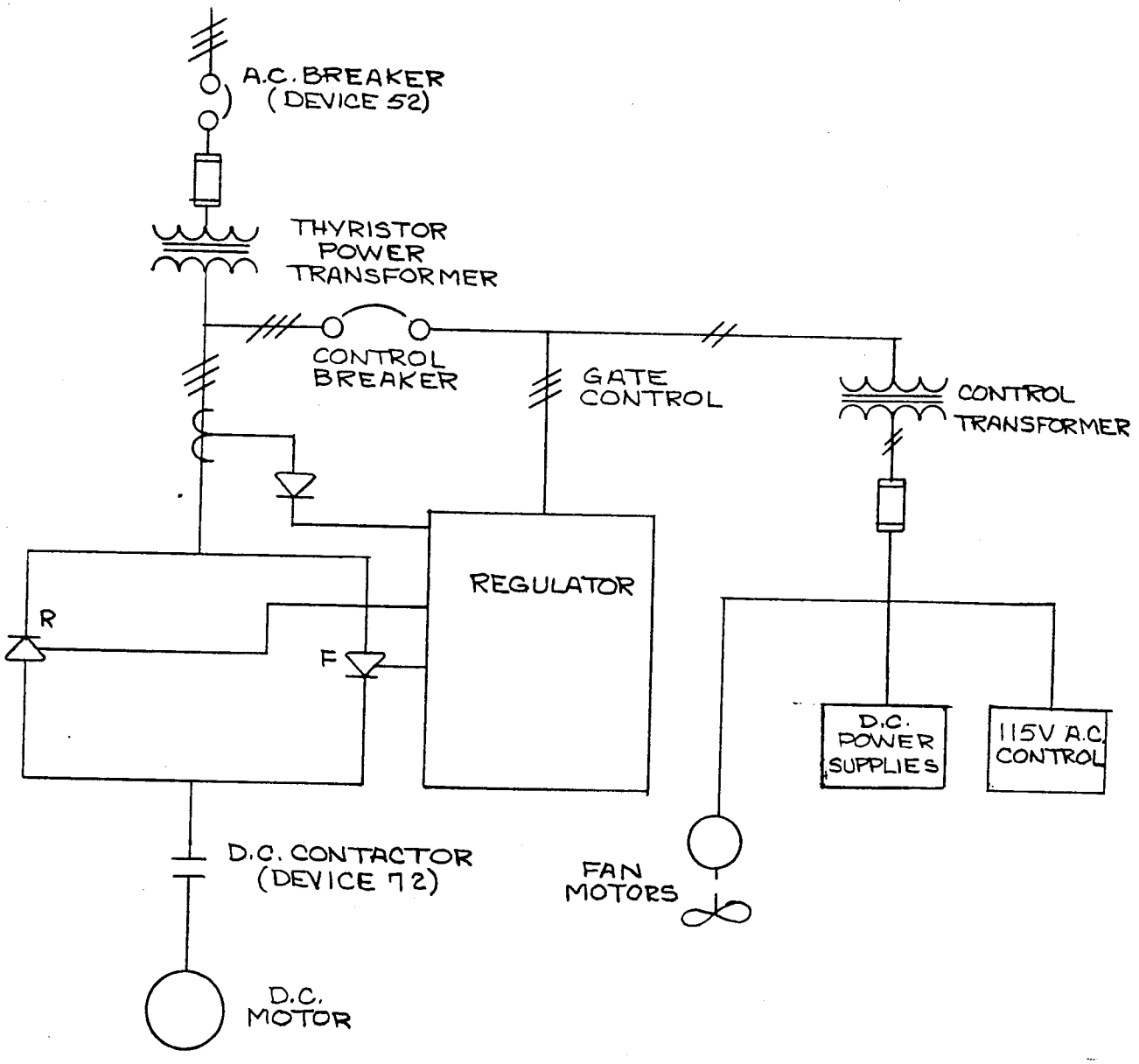


FIGURE II-10

The molded case ac breakers employed in M5B systems have magnetic trip only, set high enough that no tripping occurs due to the transformer inrush current.

The transformer secondary current is monitored with current transformers. These signals are rectified and this a-c signal is sent to the regulator for current feedback, instantaneous overcurrent, and inverse time overload functions.

The main sequencing device is the d-c contactor (device 72) between the power converter and the d-c motor armature. Its main function is to de-energize the motor positively in case of an emergency or if any work is required on the driven machinery. It is not providing electrical isolation of the armature. This is accomplished by tripping the a-c breaker.

Internal regulator sequencing is all done with static logic elements. External contacts required for sequence and protection such as main contactor auxiliary (Ma), zone A contacts (TPM thermo switch, thyristor circuit breaker auxiliary if class I protection is employed, etc.), contactor close and open push buttons, etc., are brought through an input isolation board. These contacts have 115V a-c for forcing voltage and are then coupled through optical isolators to generate logic "1" (+15V) and "0" (PSC) signals. All logic contacts and switches are designated with a diamond around the represented element. The PSR and MC switch is capable of picking up a relay as employed on M5B. The PSR relay is optional and its contact would likely be required in a line up of several drives to indicate all power supplies are ready for contactors to be closed. MC is the only relay (magnetic) required for basic sequencing and it of course is to pick up the d-c contactor.

Figure II-11 shows a typical sequencing control diagram for an armature supply. Located on the S&P board are functions overcurrent (O.C.), dc power supply monitor (PS), gate pulse suppression (GPS), and as well processes a total permissive signal from the gate synchronizer board (GS). This permissive signal on GS is a sum of functions phase sequence (Ø seq.), single phase (1Ø), line undervoltage (UV), and oscillator running (osc). Following turn on of ac power gate pulses are inhibited for about 0.5 sec to assure that all power supplies have reached an equilibrium condition. If all permissive signals in the GPS circuit are correct, then gate pulses will be released and the system will regulate for zero voltage. Assuming there has been no overload (O.L.) and all zone A permissive contacts are closed, then PSR will pick up to indicate the drive is ready for operation. Upon pressing the contactor close circuit MC will pick up providing motor voltage is low and zone B permissive contacts are closed. MC picks up the contactor and a contactor auxiliary is brought back which locks in MC and releases the 1CR and 2CR function so the current controller will regulate for current.

Upon demand to open the contactor MC will drop out removing the current reference and the current controller will start to force armature current to zero. A contactor time delay later the contactor will open however it will have to interrupt little or no current. Ma will then reset the current controller to regulate for zero voltage again.

Interlocks in zone A are of the type generally under the control of electricians, e.g., cooling fans, overloads, etc. Interlocks in zone B cover functions which are under the control of the operating personnel, e.g., lubricating pumps, limit switches, etc. This split into A and B is intended to clarify the responsibilites in case of problems. It also allows the operator to restart the drive after correcting B interlock state, without an electrician's help.

Fault currents while rectifying are normally turned off by gate pulse suppression. In case of inverting service, GPS stops only an additional ac fault current contribution. Current through the dc motor must be interrupted by clearing of TPM fuses in the case of class 3 protection or dc breaker in the case of class 1 protection.

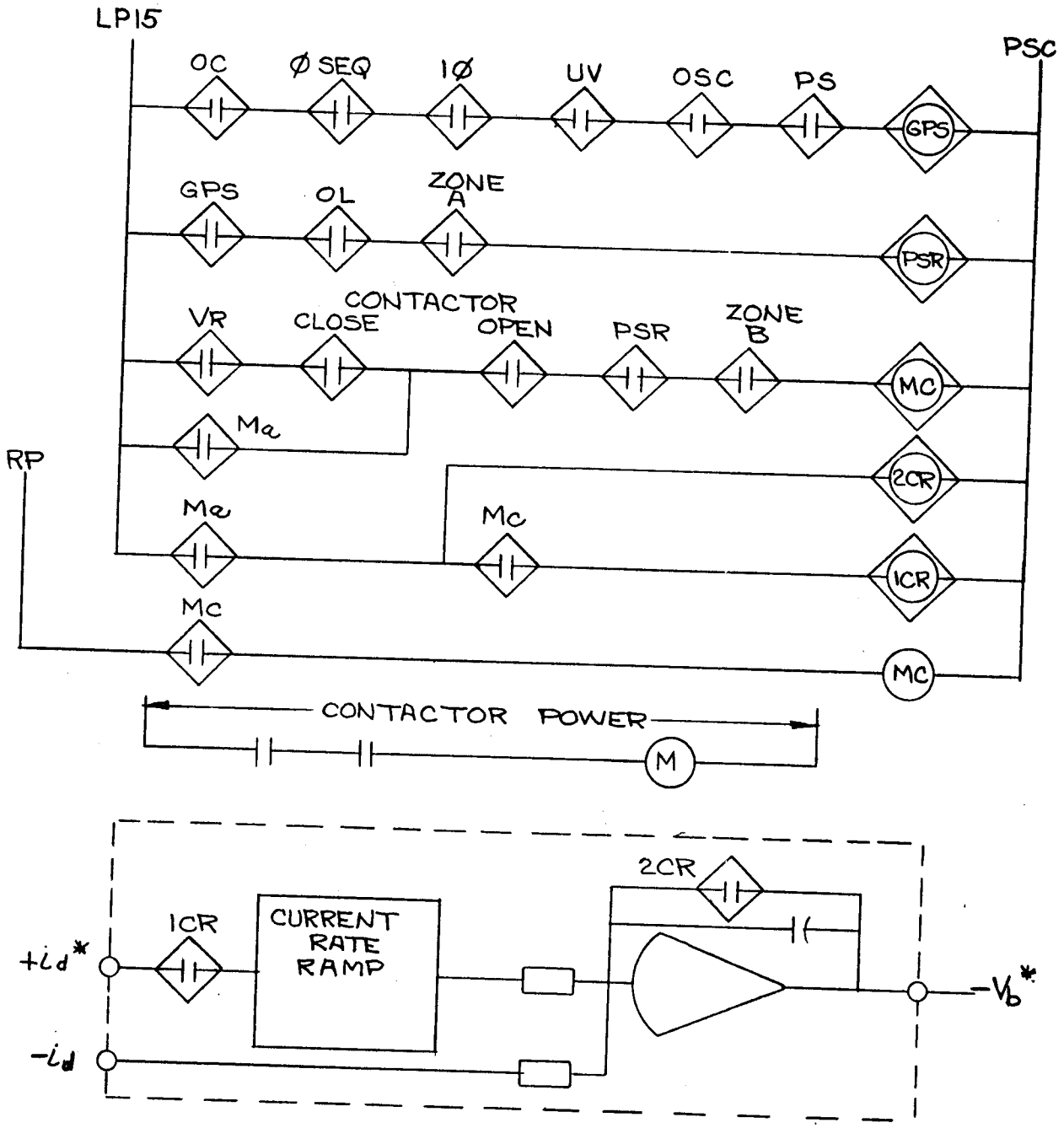


FIGURE II-11

Following is a brief description of protective functions monitoried in the regulator. As stated previously these functions are located on the sequence and protection board, or synchronizer board.

(a) o.c. - Overcurrent protection is initiated at about 125% of drive current limit value. If this current is reached a fault has occurred and gate pulses are removed. An LED indicator on S&P will come on should o.c. occur.

(b) Ø seq. - Monitor phase sequence rotation. Should wrong rotation be present at start up, gate control would be incorrect and no gate pulses are allowed. An LED on the GS board will be on when Ø seq. is correct.

(c) 1Ø - should a phase be missing on the ac feeder or TPM transformer, this circuit would detect it and remove gate pulse.

(d) U.V. - If severe line dips occur to about 80% of nominal value this circuit will operate and remove gate pulses. Any time full inverting voltage were called for with this much of aline dip an inverter fault would occur. This circuit does not eliminate all inverter faults due to severe line dips; it does however prevent some from occurring.

(e) osc. - should the internal oscillator fail gate pulses are stopped. An LED on GS will be on when the oscillator is operative. The oscillator is required of course for all pulses in the pulse trains except the first one.

(f) P.S. - regulator ±24 power supplies are monitored. Should a power supply fail gate pulses are removed since control circuits will no longer regulate. And LED on S&P board will come on should P.S., 1Ø, or u.v. operate.

(g) O.L. - current feedback is monitored on the S&P board for O.L. should O.L. occur, this opens the MC circuit and opens the main contactor. Either of two overload circuits may be used; one with a trip setting of 200% for 10 sec and 150% for 1 minute, or 300% for 10 sec and 200% for 1 minute of rated drive current.

Each input board used on M5B can process six contact functions. One or two boards may be used in the regulator cage. The first board could process contact functions of zone A, zone B, contactor close, stop, Ma, and gate pulse suppression reset. The second board could process contact functions such as jog, thread, emergency stop, etc. Each set of contact functions is monitored with an LED to indicate closed or open status; light is on for closed contacts.

III. VARIABLE REGULATORS

The variable regulator comprises the printed circuit boards and other apparatus required to regulate the process variables, such as armature or field current, bus voltage, speed and/or position of the machine. The word "variable" regulator refers to the fact that a great variety of combinations of boards is required to satisfy all of the varied industries. No attempt is made in the following to give a comprehensive descri;tion; rather the principles involved are highlighted. A description of some common regulator modules used in M5B is given in the M5B Variable Regulator I.L. 16-800-288. Startup and regulator optimization procedures are given in the respective variable regulator startup instruction leaflets.

Modern applications of regulated dirves require not only the accurate control of the primary varialbe (for instance, speed), but also the control has to fulfill one or more of the following requirements.

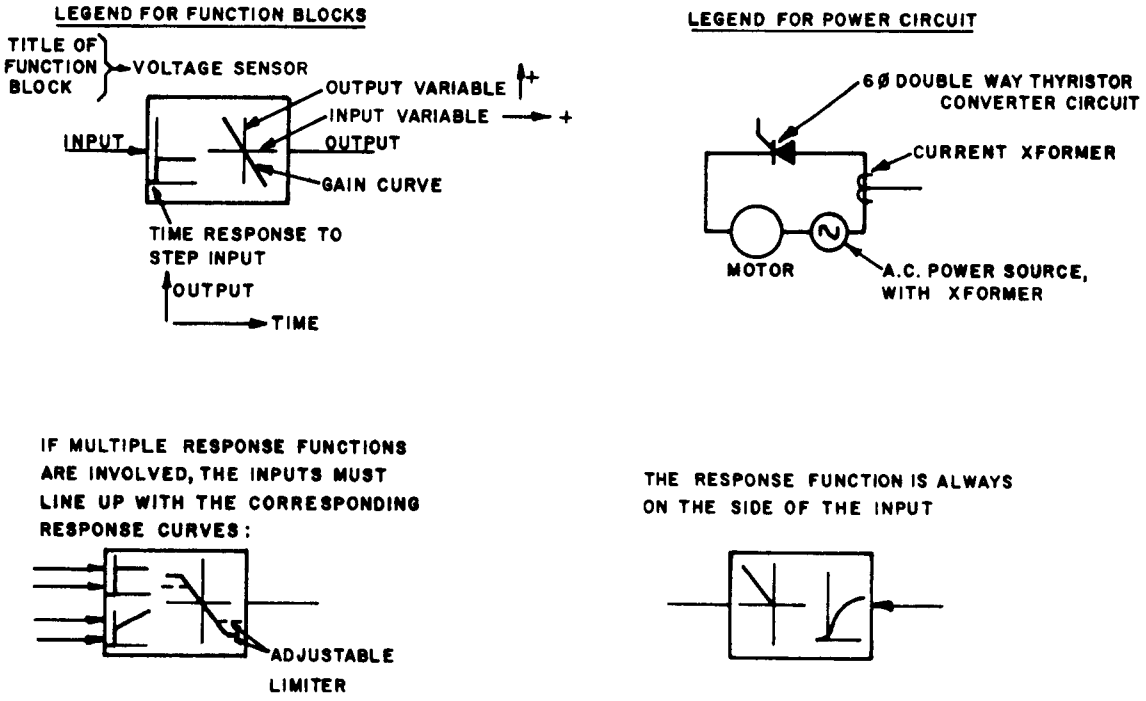
(a) Limitation of critical variables of the drive such as armature current or voltage to protect the system.

(b) Close control of variables to avoid excessive rates of change. For example, control of the rate of rise of current to assure good commutation of the machines.

(c) Smooth transfer from one mode of control to another. For example, smooth switchover from speed control with current limit to current control with speed limit.

(d) Simple and straightforward adjustment and optimization of control loop. This requirement shows its importance during startup and later when a malfunctioning controller has to be replaced.

There are three concepts available --- the spill over control, the multi-loop (cascaded) control, and the parallel control --- which allow control of the primary variable and the limitation of other secondary variables. Only the multi-loop and parallel control fulfill the requirements of modern applications. The multi-loop (or cascaded) control concept is used almost exclusively in M5B variable regulators and that concept will be described. Symbols used in regulator block diagrams are explained in Figure III-1.



LETTER SYMBOLS

Upper-case letters denote power circuit quantities:

E: emf, V: voltage, I: current, ϕ: flux

Lower-case letters denote controller signals:

e: emf, v: voltage, i: current, ψ: flux

Subscripts:

a: armature, b: bus, f: field, n: angular speed, m: motor

Superscripts:

*: reference signal

(NOTE: if additional reference signals for the same controlled variable are used, then second, third, etc. asterisks will be added.)

FIGURE III-1

REGULATOR SYMBOLS

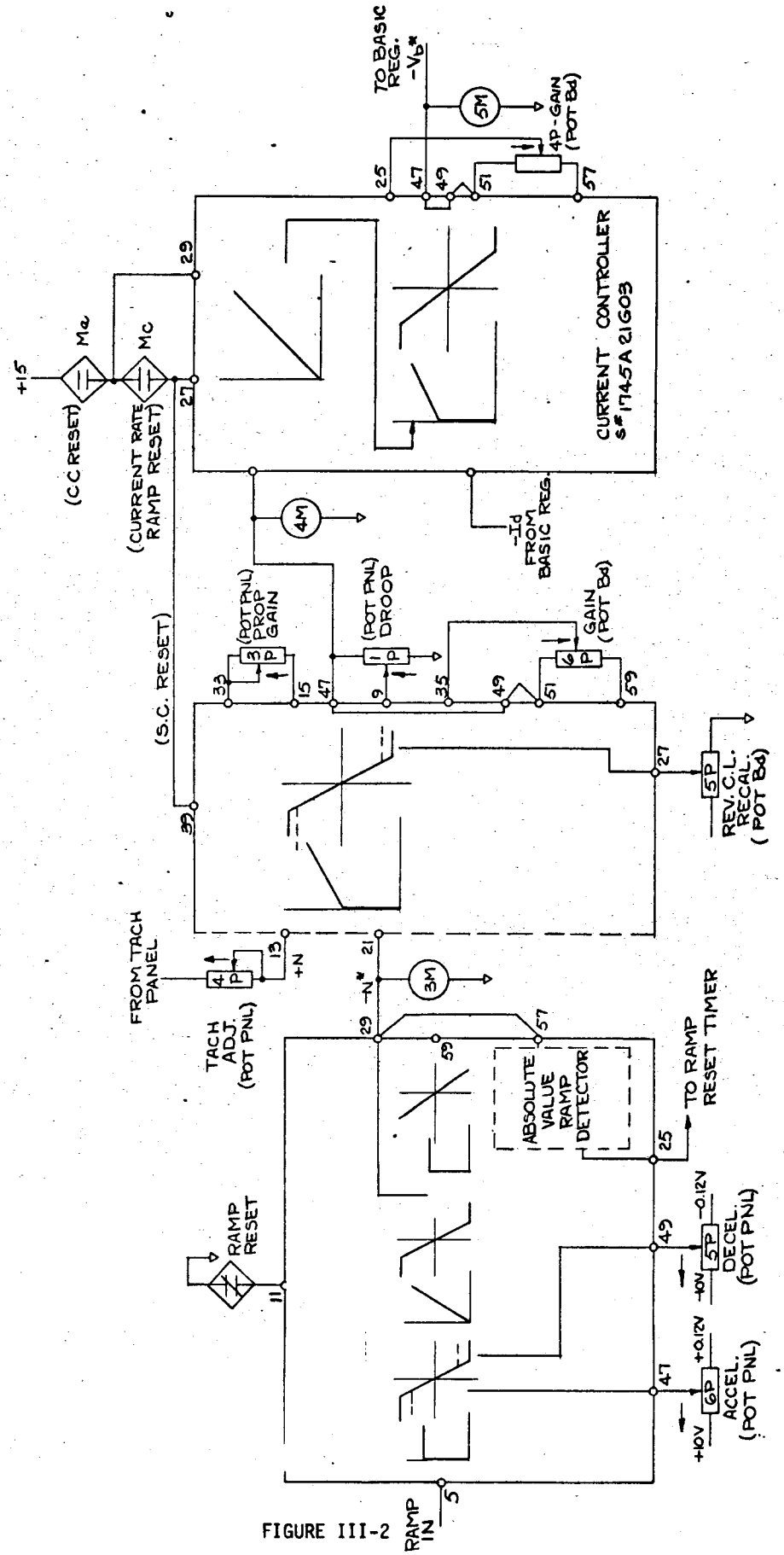


FIGURE III-2

TYPICAL M5B SPEED REGULATOR WITH RAMP

Figure III-2 shows a block diagram of a multi-loop speed regulator with ramp function generator for a double converter basic regulator. It will be used to discuss variable regulator concepts used in M5B.

The most outer loop is the RFG. It would likely be required if several drives have to track speed on acceleration. In that case ramp rates would have to be slow enough so current limit is not reached for tracking accuracy to be possible. Also an absolute value ramp detector is is available which would likely be used in stop sequencing following a ramp deceleration. The non inverted output of the RFG is used as the speed reference signal. This allows the same polarity of reference for speed wheter an RFG is used or not.

The primary variable (speed) is controlled in the next loop. Its output represents the reference for control of the secondary variable (current) in the inner loop. Therefore, it is possible by limiting the output of the outer (speed) controller to obtain any desired current limit characteristic. A constant output limit results in a verticle current limit characteristic. By limiting the output dependent on armature voltage or drive speed, a tapered current limit can be obtained. The output of the current controller, in turn represents the reference ($-V_b^*$) for the basic regulator and in limit sets the maximum bus voltage V_b produced by the converter. In practice, the output limiter in the current controller is in the range of 9.5...10.5V, and the operating range is limited to 104% of rated bus voltage by adjusting the gain in the voltage sensor.

The outer speed loop is adjusted to be only about half as fast as the inner current loop to provide a dynamic separation of the two loops. It is possible to add more loops (other than RFG) around the outer speed loop (for instance, tension loop). In this case, the above adjustment rule applies and the next outer loop is adjusted about half as fast as the loop it is generating a reference for.

It is very easy in a multi-loop system to change the mode of control and to switch, for instance from speed control to current control. In our example with no RFG, it would require reducing the setting of the speed controller output limit to the desired current reference value and applying a reference (speed limit) step into the speed controller to saturate the SC amplifier.

M5B controllers in general are designed so that only one major time delay is in each loop, which can be readily cancelled by the lead term of the respective controllers. Startup is straightforward since the steady-state and dynamic characteristic of the control are independent of each other. The most inner loop is adjusted, then each next outer loop.

There are four possible adjustments in the SC which are essentially independent. Proportional gain adjust is the lead time constant adjustment to cancel the mechanical time constant of the machine. Gain adjust is for dynamic adjustment (crossover frequency) of the SC loop. Tach adjust is to match tach feedback to maximum reference into the S.C. for speed limit. Droop adjust is available if required. It should be noted that all gain jumpers and potentiometers are external to the controllers. Should a controller board become defective, readjustment of gain and limits is usually not required.

The lead time constant of the CC is fixed to approximately cancel the armature time delay. Gain pot adjusts the dynamic response of the CC (crossover). A rate of current change ramp is used in the CC to assure good machine commutation of current. As a ramp is used, rather then a lead term in the current feedback loop, no additional lead term is required in the speed controller. As only one lead term is used in the SC, this regulator is less susceptible to tach noise and misalignment noise then would be a SC with two lead terms.

The multi-loop control concept has proved to be very effective and in M5B is used almost exclusively. A summary of the features of this control concept yields:

(a) Separate controllers are used for each controlled variable. This allows no optimum and straightforward adjustment for each loop.

(b) Steady-state and dynamic characteristics are independently adjustable.

(c) Smooth transfer from one control mode to another.