GATE SELECTOR AND DRIVER

I. INTRODUCTION

The F80 controller cards are used to provide phase control of a single phase F80 field exciter TPM in either a single converter or a dual converter configuration. The basic F80 cards include the Gate Selector and Driver S#1725A08, the Gate Controller S#1725A09 and the Bank Selector S#1725A10 (used only in the dual converter applications).

The Gate Selector and Driver, GS&D, selects an appropriate channel depending upon the polarity of the TPM AC voltage and the polarity of the reference voltage in the case of a dual converter and amplifies the controlled gate pulses to levels capable of driving two thyristor gates through an isolating pulse transformer.

Figure 1 is a picture of the GS&D. A front view locating all components by schematic identification is shown on the last page of the instruction leaflet. NOTE: Drawing 1725A08 is a multi-group assembly and some components will be missing from some style number pc boards.

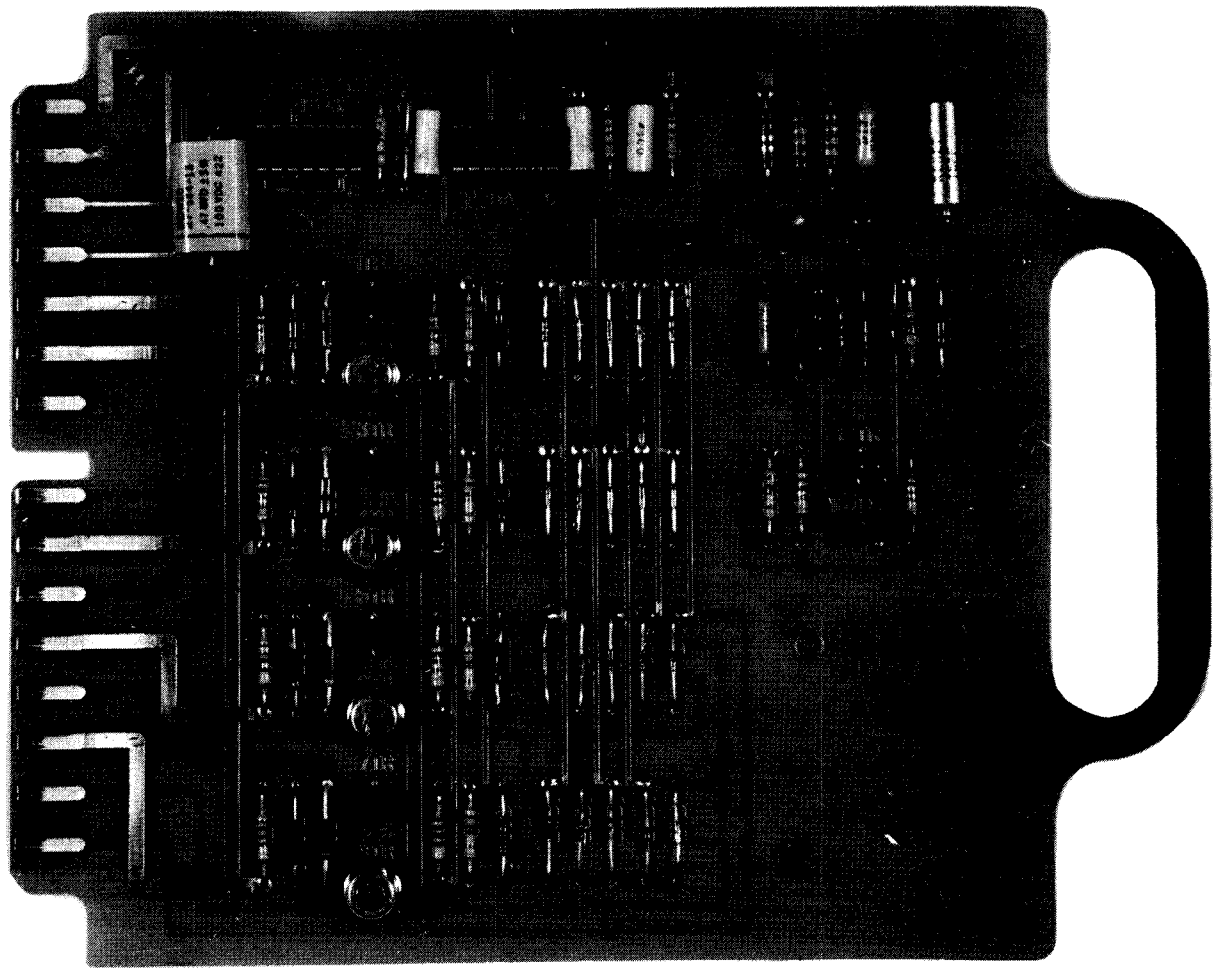
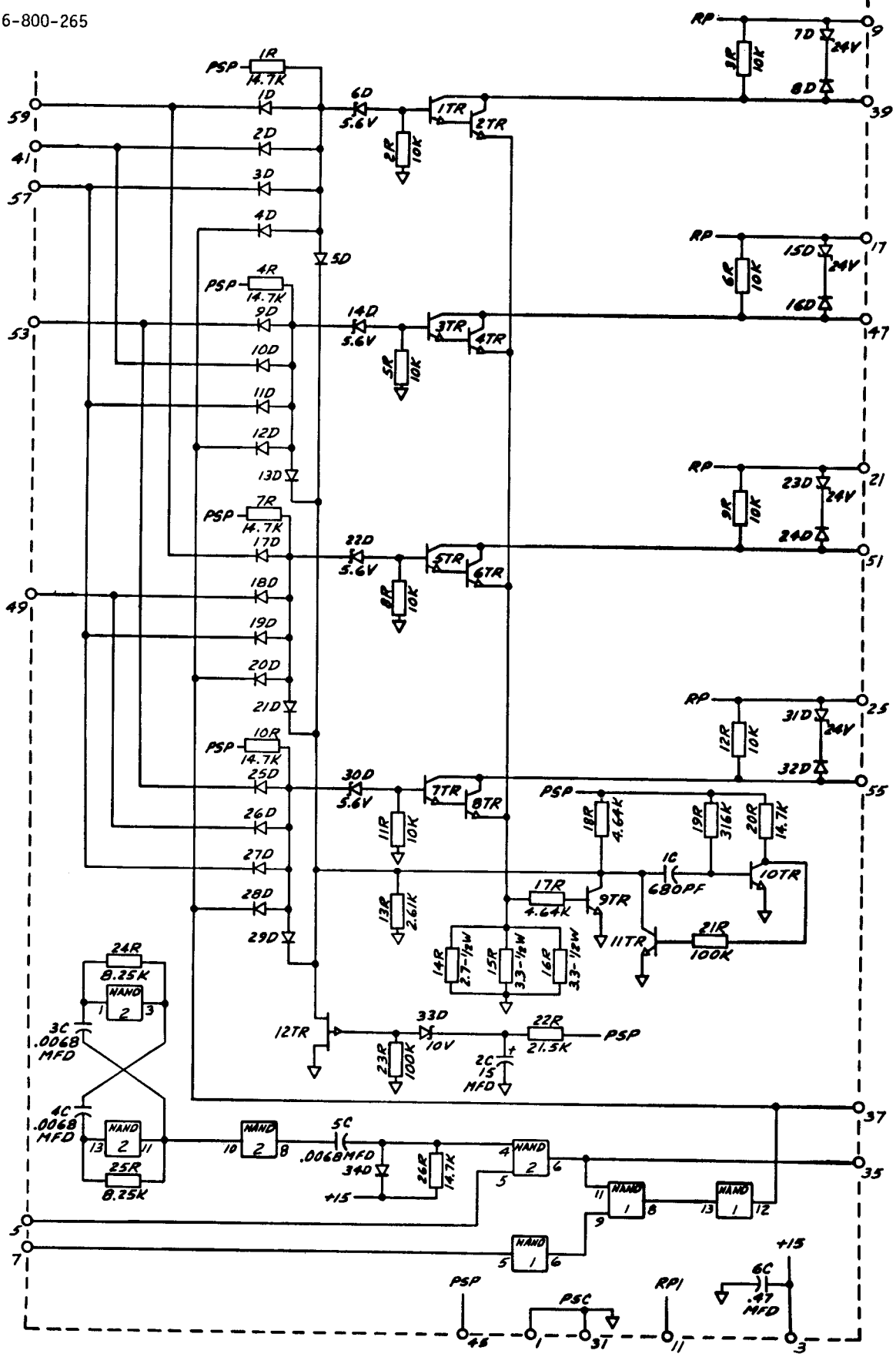


FIGURE 1



ALL RESISTORS 1/8W, 1% UNLESS OTHERWISE SPECIFIED

FIGURE 2

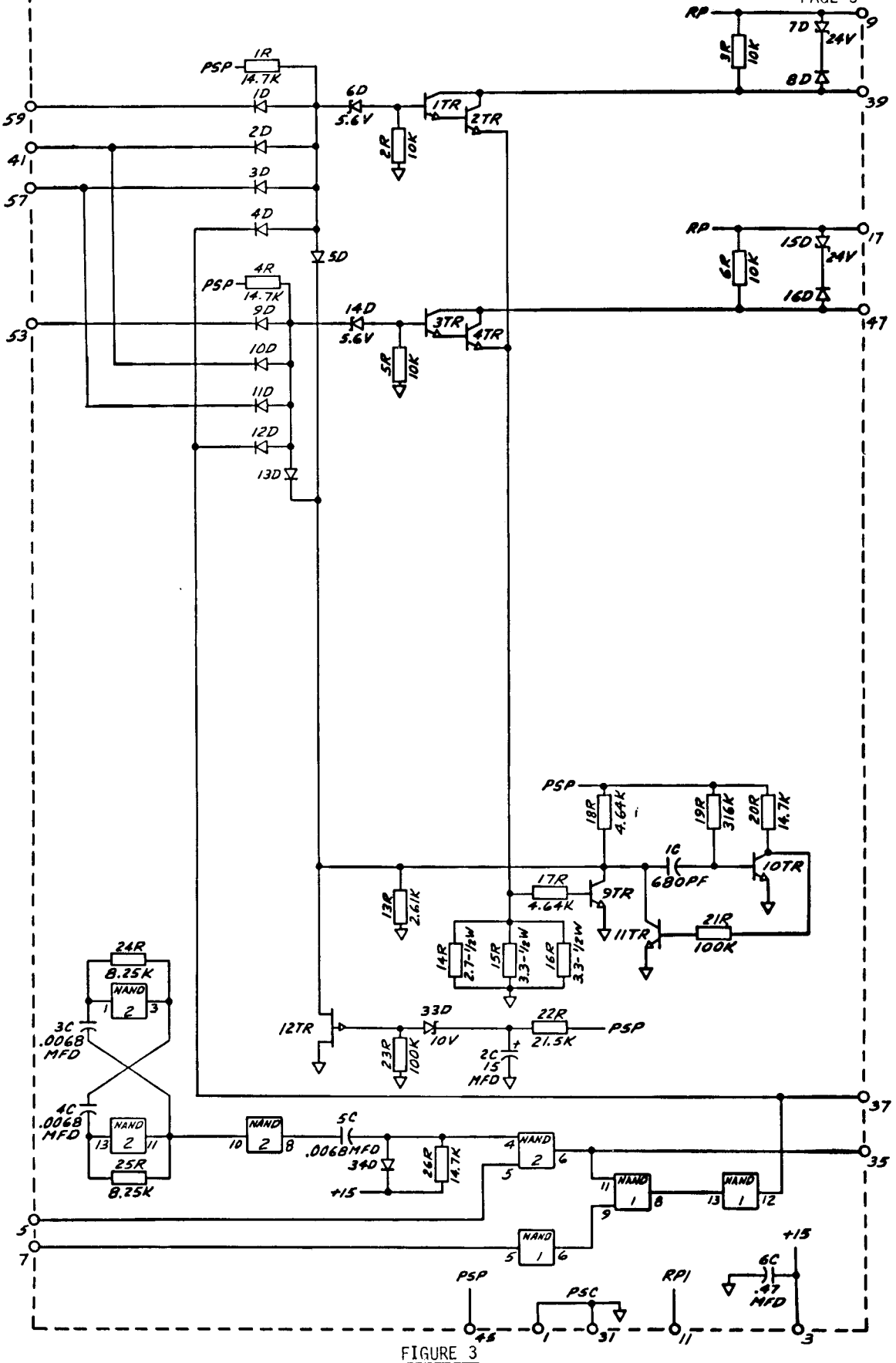

RP
7D
24V
8D
3R
10K
9
39
PSP
1R
14.7K
1D
6D
5.6V
1TR
2TR
2R
10K
59
2D
41
3D
57
4D
5D
RP
15D
24V
16D
6R
10K
17
47
4R
PSP
14.7K
9D
14D
5.6V
3TR
4TR
5R
10K
53
10D
11D
12D
13D
PSP
18R
4.64K
19R
316K
20R
14.7K
1C
680PF
10TR
17R
4.64K
9TR
11TR
21R
100K
13R
2.61K
14R
2.7-1/2W
15R
3.3-1/2W
16R
3.3-1/2W
24R
8.25K
NAND
2
3C
.006B
MFD
4C
.006B
MFD
25R
8.25K
12TR
33D
10V
22R
21.5K
PSP
23R
100K
2C
15
MFD
37
35
5C
.006BMFD
34D
+15
26R
14.7K
NAND
1
6C
.47
MFD
+15
5
7
PSP
PSC
RPI
46
1
31
11
3

FIGURE 3

II. DESCRIPTION OF OPERATION

A. Introduction

The F80 TPM provides full wave rectification of the incoming AC. This requirement necessitates control of four thyristors. Polarity reversing requirements in a dual converter application necessitates control of eight thyristors. G01 of the GS&D card contains four selection and driver circuits; G02 contains two.

B. Circuit Operation (Refer to Figures 2 and 3)

The inputs to the GS&D card are as follows:

T_{59} — A one during the positive half cycle.
A zero during the negative half cycle.

T_{41} — A one when positive TPM voltage is required.
A zero when negative TPM voltage is required.
Tie to +15V with a single converter.

T_{57} — Tie to +15V

T_{53} — A one during the negative half cycle.
A zero during the positive half cycle.

T_{49} — A one when negative TPM voltage is required.
A zero when positive TPM voltage is required.

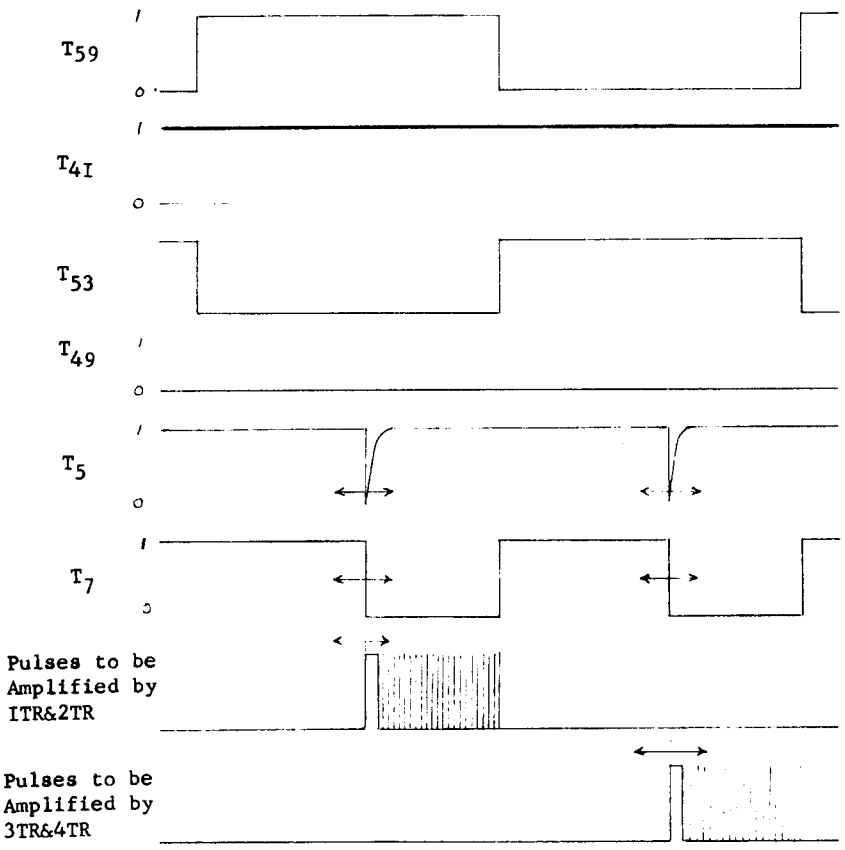
T_5 — First pulse at desired α.

T_7 — A zero from the desired α point until the AC TPM voltage changes polarity.
A zero enable allows pulse amplification in the selected driver.

When U-V is positive, this is designated as the positive half cycle. Correspondingly, the negative half cycle occurs when U-V is negative. When U-V is positive and 1THF and 3THF conduct (or 1TH and 3TH in a single converter), positive TPM voltage is generated.

For positive TPM voltage the input circuitry of transistors 1TR and 2TR is enabled during the positive half cycle and the input circuitry of transistors 3TR and 4TR is enabled during the negative half cycle. For negative TPM voltage the input circuitry of transistors 5TR and 6TR is enabled during the positive half cycle and the input circuitry of transistors 7TR and 8TR is enabled during the negative half cycle. Pulse amplification occurs when the appropriate signal is applied to terminal 7.

Figure 4 depicts the timing diagram for forward TPM voltage. The input signals to terminals 5 and 7 occur at the same time. The signal on terminal 5 is a narrow pulse which generates the first pulse in the pulse train. The signal on terminal 7 changes from a "1" to "0" and during this zero interval pulses can be amplified by the selected driver stage. The low signal on terminal 7 is inverted and applied to a NAND gate the second input of which is either the inverted signal from terminal 5 or from the oscillator. The combined pulse train is applied to the selection circuits through diodes 4D, 12D, 20D and 28D. The selected driver amplifies an appropriate pulse train as shown in Figure 4. The first pulse is approximately 50μsec in duration; the clock pulses are approximately 35μsec in duration at an 11khz rate. The starting point of the pulse train is determined by the required α position. The pulse train is stopped when the appropriate thyristors become reverse biased.



TIMING DIAGRAM FOR FORWARD TPM VOLTAGE

FIGURE 4

The outputs from this card feed the gates of the following devices:

T_9 & T_{39}	1TH, 3TH	in a single converter
	1THF, 3THF	in a dual converter
T_{17} & T_{47}	2TH, 4TH	in a single converter
	2THF, 4THF	in a dual converter
T_{21} & T_{51}	2THR, 4THR	in a dual converter
T_{25} & T_{55}	1THR, 3THR	in a dual converter

One of the driver stages should always be selected and amplifying the appropriate pulse train. The pulse amplifier stages are capable of driving a pulse transformer assembly (S#1683A96G01) which has two secondary windings for the firing of two thyristors. The amount of current on the primary side of the pulse transformer depends upon the resistance in the secondary circuits and upon the impedance of the thyristor gates.

Resistors 14R, 15R and 16R are used to monitor the current in the pulse transformer primary. The voltage developed on this resistance combination (approximately 1 ohm) is applied to the circuitry of transistors 9TR, 10TR and 11TR. If the primary current exceeds the threshold current level (0.60A) this circuitry will generate a timed inhibit signal which turns off all driver stages for 80 μsecs. (1 clock pulse interval). If a short occurs on either the primary or secondary side of the pulse transformer, this circuitry prevents the generation of excessive currents which could damage the driver stage. Transformer saturation can also cause excessive currents.

FET 12TR and the associated gate components are used to prevent gating during the power turn on transient.

Terminal 35 is an output oscillator signal which is used on the Bank Selector card. Terminal 37 is for monitoring purposes only.

III. CHARACTERISTICS AND RATINGS

A. Logic Signals: All input signals and the oscillator signal on T_{35} must be consistent with high level logic requirements.

12V	$\leq$	"1"	$\leq$	15V
2V	$\geq$	"0"	$\geq$	0V

B. Logic Loading:

T_{59}	3.2	(1.6)	T_5	1.0	(1.0)
T_{41}	3.2	(0)	T_7	1.0	(1.0)
T_{53}	3.2	(1.6)			
T_{49}	3.2	(0)			

The loading figures in ( ) are for single converters.

C. Fan Out Capability: T_{35} 9

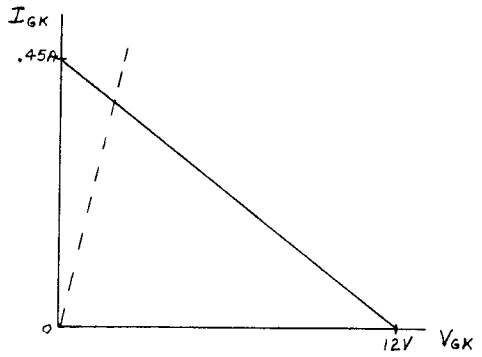
D. Power Supplies:

+15V	±1.5V	@	30ma	
PSP	+24V	±2V	@	10ma
RP	+24V	±2V	@	200ma average

On the RP line, pulse currents can have 0.5A peaks for the pulse duration.

CAUTION: PSP and RP cannot be tied to the same supply voltage to operate this card.

E. Thyristor Gate - Cathode Limits



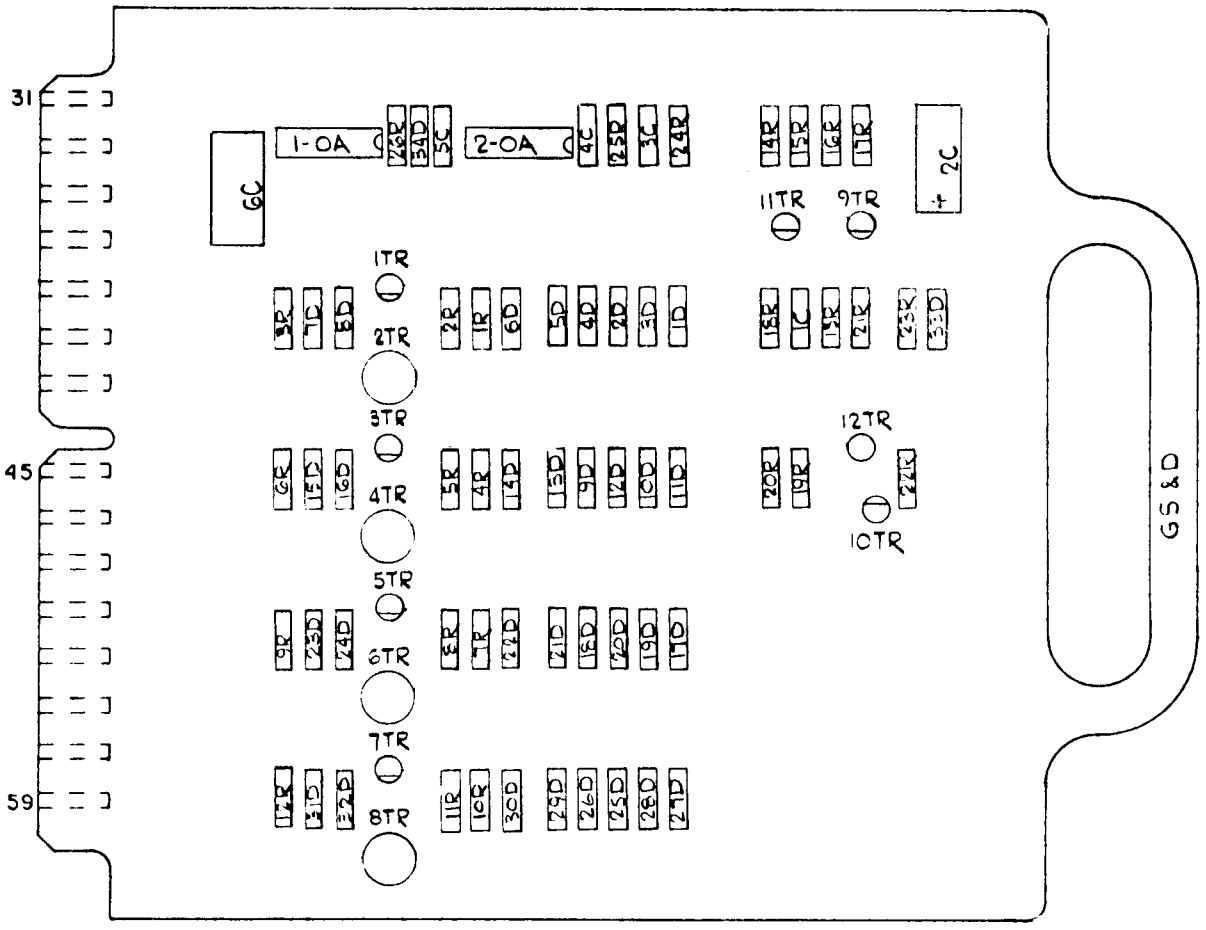

31
45
59
6C
1-0A
2-0A
4C
2C
11TR
9TR
1TR
2TR
3TR
4TR
5TR
6TR
7TR
8TR
12TR
10TR
GS&D

FIGURE 5