

SEL-351-5, -6, -7

**DIRECTIONAL OVERCURRENT RELAY
RECLOSING RELAY
FAULT LOCATOR
INTEGRATION ELEMENT STANDARD**

INSTRUCTION MANUAL

SCHWEITZER ENGINEERING LABORATORIES, INC.
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CAUTION: The relay contains devices sensitive to electrostatic discharge (ESD). When working on the relay with front or top cover removed, work surfaces and personnel must be properly grounded or equipment damage may result.



CAUTION: There is danger of explosion if the battery is incorrectly replaced. Replace only with Ray-O-Vac® no. BR2335 or equivalent recommended by manufacturer. Dispose of used batteries according to the manufacturer's instructions.



WARNING: This device is shipped with default passwords. Default passwords should be changed to private passwords at installation. Failure to change each default password to a private password may allow unauthorized access. SEL shall not be responsible for any damage resulting from unauthorized access.



DANGER: Removal of relay front panel exposes circuitry which may cause electrical shock that can result in injury or death.



DANGER: Contact with instrument terminals may cause electrical shock which can result in injury or death.



ATTENTION! Le relais contient des pièces sensibles aux décharges électrostatiques(DES). Quand on travaille sur le relais avec le panneau avant ou du dessus enlevé, les surfaces de travail et le personnel doivent être mis à la terre convenablement pour éviter les dommages à l'équipement.



ATTENTION! Il y a un danger d'explosion si la pile électrique n'est pas correctement remplacée. Utiliser exclusivement Ray-O-Vac® No. BR2335 ou un équivalent recommandé par le fabricant. Se débarrasser des piles usagées suivant les instructions du fabricant.



ATTENTION! Cet équipement est expédié avec des mots de passe par défaut. A l'installation, les mots de passe par défaut devront être changés pour des mots de passe confidentiels. Dans le cas contraire, un accès non-autorisé à l'équipement pourrait être possible. SEL décline toute responsabilité pour tout dommage résultant de cet accès non-autorisé.



DANGER: Le retrait du panneau avant expose à la circuiterie qui pourrait être la source de chocs électriques pouvant entraîner des blessures ou la mort.



DANGER: Le contact avec les bornes de l'instrument peut causer un choc électrique pouvant entraîner des blessures ou la mort.

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The English language manual is the only approved SEL manual.

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This product is covered by U.S. Patent Numbers: 5,041,737; 5,208,545; 5,317,472; 5,349,490; 5,365,396; 5,367,426; 5,479,315; 5,515,227; 5,602,707; 5,652,688; 5,694,281; 5,790,418; 5,793,750; 5,883,578 U.S. Patent(s) Pending, and Foreign Patent(s) Issued and Pending.

This product is covered by the standard SEL 10-year warranty. For warranty details, visit www.selinc.com or contact your customer service representative.

MANUAL CHANGE INFORMATION

The date code at the bottom of each page of this manual reflects the creation or revision date. Date codes are changed only on pages that have been revised and any following pages affected by the revisions (i.e., pagination). If significant revisions are made to a section, the date code on all pages of the section will be changed to reflect the revision date.

Each time revisions are made, both the main table of contents and the affected individual section table of contents are regenerated and the date code is changed to reflect the revision date.

Changes in this manual to date are summarized below (most recent revisions listed at top).

Revision Date	Summary of Revisions
	The <i>Manual Change Information</i> section has been created to begin a record of revisions to this manual. All changes will be recorded in this Summary of Revisions table.
20010307	<p>This revision includes the following changes:</p> <ul style="list-style-type: none"> – Reissued Entire Manual – Added Caution, Danger, and Warning information to the back of the cover page of the Manual. – Replaced Standard Product Warranty page with warranty statement on cover page. <p>Section 1:</p> <ul style="list-style-type: none"> – Added Tightening Torque information to <i>General Specifications</i>. – Updated Power Supply information to include medium range Power Supply Specification. – Added optoisolated input ratings for ac control signals to <i>General Specifications</i>. <p>Section 2:</p> <ul style="list-style-type: none"> – Updated <i>Optoisolated Inputs</i> subsection to include ac input selection. – Added condition of acceptability for North American Product Safety Compliance. – Added caution note to the <i>Clock Battery</i> subsection. <p>Section 3:</p> <ul style="list-style-type: none"> – Updated subsection <i>Voltage Sag, Swell, and Interruption Elements (Available in Firmware Version 7)</i>. <p>Section 5:</p> <ul style="list-style-type: none"> – Updated <i>A, B, and C Target LEDS</i> subsection. – Added <i>SELOGIC Control Equation Setting FAULT</i> subsection.

Revision Date	Summary of Revisions
	<p>Section 7:</p> <ul style="list-style-type: none"> – Added ac setting description to <i>Input Debounce Timers</i> subsection. – Updated <i>Make Latch Control Setting With Care</i> and <i>Make Active Setting Group Switching Settings With Care</i> subsections. – Added subsections <i>Displaying Metering Quantities on the Rotating Default Display</i>, <i>Displaying Metering Values Example</i>, <i>Displaying Breaker Monitor Output Information on the Rotating Default Display</i>, and <i>Displaying Breaker Monitor Outputs Example</i>. <p>Section 8:</p> <ul style="list-style-type: none"> – Updated <i>Maximum/Minimum Metering</i> subsection. – Added phase-to-phase voltages to load profile recorder. <p>Section 9:</p> <ul style="list-style-type: none"> – Updated setting ranges for VINT, VSAG, and VSWELL on Settings Sheet 13. – Added ac setting choice to optoisolated input timers on Setting Sheets 20 and 21. – Added phase-to-phase voltages to LDLIST settings choices on Settings Sheet 22. <p>Section 10:</p> <ul style="list-style-type: none"> – Changed the HIS command information. – Added MET X command description. – Updated password information. – Added warning note to the <i>PAS Command (View/Change Passwords)</i> subsection. – Updated Command Summary to include MET X, SSI R, and SSI T commands. <p>Section 12:</p> <ul style="list-style-type: none"> – Updated event report capacity, and removed Table 12.1. – Updated Make Sequential Events Recorder (SER) Settings with Care subsection. – Updated subsection <i>Sag/Swell/Interruption (SSI) Report (Available in Firmware Version 7)</i>. <p>Appendix A:</p> <ul style="list-style-type: none"> – Updated Firmware Version information. <p>Appendix B:</p> <ul style="list-style-type: none"> – Updated password information. <p>Appendix K:</p> <ul style="list-style-type: none"> – Added new <i>Appendix K: SEL-5030 ACSELERATOR™</i>.

Revision Date	Summary of Revisions
20001006	<p>This revision includes the following changes:</p> <p>Reissued entire manual.</p> <p>Section 1:</p> <ul style="list-style-type: none"> – Corrected RFI and Interference Tests. – Corrected phase angle accuracy of synchronism check elements. <p>Section 2:</p> <ul style="list-style-type: none"> – Replaced Figure 2.1. – Added cable for SEL-DTA2 to Table 2.1. – Added note to Table 2.6 (<i>Fast Operate</i>). <p>Section 3:</p> <ul style="list-style-type: none"> – Corrected setting range for 59Q in Table 3.8. – Clarified description of synchronism check element logic. – Expanded setting range for 27B81P in Table 3.10. <p>Section 4:</p> <ul style="list-style-type: none"> – Corrected loss-of-potential positive-sequence (V1) reset threshold. <p>Section 5:</p> <ul style="list-style-type: none"> – Corrected Figure 5.6. <p>Section 6:</p> <ul style="list-style-type: none"> – Corrected 79DTL factory default setting (Table 6.4). <p>Section 7:</p> <ul style="list-style-type: none"> – Added subsection <i>Details on the Remote Control Switch MOMENTARY Position</i>. – Corrected the number of local, latch, and remote bits to 16. <p>Section 8:</p> <ul style="list-style-type: none"> – Added qualifying statement about changing the LDAR setting. <p>Section 9:</p> <ul style="list-style-type: none"> – Expanded setting range for 27B81P on Settings Sheet 9. – Corrected FP_TO setting range on Global Settings Sheet. – Added description of MBT setting choice for port settings. – Added AUTO = DTA setting choice to Port Settings Sheet. <p>Section 10:</p> <ul style="list-style-type: none"> – Added notes about powering-down the relay after setting the date or time. – Added DTA2 compatibility information. – Revised SEL-351-5, -6, -7 Command Summary.

Revision Date	Summary of Revisions
	<p>Section 12: – Added Table 12.1.</p> <p>Appendix A: – Updated Firmware Version information.</p> <p>Appendix B: – Added step 16 for Breaker Wear Monitor data.</p> <p>Appendix D: – Made changes to <i>A5C0 Relay Definition Block</i>. – Updated ID Message.</p> <p>Appendix G: – Corrected Figures G.1 and G.2 for rising and falling edge operators. – Corrected Table G.3.</p> <p>Appendix H: – Corrected spelling of DECPLA, DECPLV, and DECPLM settings for DNP. – Corrected index error in <i>Relay Summary Event Data</i> subsection.</p> <p>Appendix I: – Added settings sheet for MIRRORRED BITS™ protocol.</p> <p>Appendix J: – Renamed Appendix.</p>
20000106	<p>This revision includes the following changes:</p> <p>Section 1: – Updated RFI and Interference Tests.</p> <p>Section 2: – Clarified Table 2.1.</p> <p>Section 5: – Added explanation to the Target Reset/Lamp Test Front-Panel Pushbutton subsection to indicate that the targets cannot be reset when a TRIP condition is still present.</p> <p>Section 7: – Corrected Display Point examples. – Corrected subsection “Relay Disabled Momentarily During Active Setting Group Change.”</p> <p>Section 9: – Corrected error in Relay Word bit description for 51G (Table 9.6).</p>

Revision Date	Summary of Revisions
	<p>Section 10:</p> <ul style="list-style-type: none"> – Added note to TAR R command description. – Minor change to COP command description. <p>Section 11:</p> <ul style="list-style-type: none"> – Corrected Rotating Default Display example. <p>Section 12:</p> <ul style="list-style-type: none"> – Minor corrections to Table 12.3. <p>Appendix A:</p> <ul style="list-style-type: none"> – Updated Firmware Version information. <p>Appendix G:</p> <ul style="list-style-type: none"> – Added Target Logic to Table G.3.
991123	<p>Appendix H:</p> <ul style="list-style-type: none"> – Corrected documentation errors in DNP 3.00 Device Profile, page H-5.
990827	<p>This revision includes the following changes:</p> <p>Updated MIRRORRED BITS™ format throughout to reflect new trademark.</p> <p>Section 3:</p> <ul style="list-style-type: none"> – Added explanation to the Synchronism Check Elements subsection for the new angle setting option for the SYNCNP (synchronizing phase) setting. Synchronism check can now be accomplished for synchronism check voltage input VS connected phase-to-phase or beyond a delta-wye transformer. Setting SYNCNP accounts for the constant angle difference between reference voltage VA and synchronism check voltage input VS. <p>Section 9:</p> <ul style="list-style-type: none"> – Expanded the setting range for the SYNCNP (synchronizing phase) setting to accommodate compensation angle settings for synchronism check (Settings Sheet 9 of 24). – Added the MB8A and MB8B serial port protocol settings options for MIRRORRED BITS protocol operating on communication channels requiring an eight bit data format (Settings Sheet 27 of 27). <p>Section 10:</p> <ul style="list-style-type: none"> – Added VER Command explanation at end of section. <p>Section 12:</p> <ul style="list-style-type: none"> – Added information explaining the need to make Sequential Events Recorder (SER) settings with care. <p>Appendix A:</p> <ul style="list-style-type: none"> – Updated Firmware Version information.

Revision Date	Summary of Revisions
	<p>Appendix B: – Updated Firmware Upgrade Instructions.</p> <p>Appendix H: – Updated screen capture on page H-14.</p> <p>Appendix I: – Explained the MB8A and MB8B serial port protocol settings options for Mirrored BITS protocol operating on communication channels requiring an eight data bit format.</p> <p>Appendix J: – Extensively rewritten.</p>
990721	Updated <i>Appendix A: Firmware Versions</i> .
990616	New Manual Release.

SEL-351-5, -6, -7 INSTRUCTION MANUAL

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SECTION 1: INTRODUCTION AND SPECIFICATIONS

This section includes the following overviews of the SEL-351 Relay:

- SEL-351 Relay Models
- Instruction Manual Sections
- Applications
- Hardware Connection Features
- Communications Connections
- General Specifications

SEL-351 RELAY MODELS

This instruction manual covers the following SEL-351 Relay models:

Table 1.1: SEL-351 Relay Models

Model Number	Rack Unit Height	Number of Isolated I/O Contacts	Rear-Panel Connection Type	Output Contact Type	Reference Figures
0351x0	2U	6/8	screw-terminal block	standard	1.2, 2.2, 7.1, 7.27
0351x1	3U	6/8 (main board)	screw-terminal block	standard	1.2, 2.3, 2.4, 7.1, 7.27
		8/12 (extra I/O board)	screw-terminal block	standard or high-current interrupting	1.4, 2.3, 2.4, 7.2, 7.28
0351xY	3U	same as 0351x1	plug-in connectors	same as 0351x1	1.2, 1.3, 2.3, 2.4, 2.5, 7.1, 7.2, 7.27, 7.28

The model numbers are derived from the SEL-351 Relay ordering information sheet. The model numbers in Table 1.1 are only the first part of an actual ordering number—enough to distinguish one model type from another. The “x” field indicates the firmware version (see Table 1.2). These numbers should not be used to order an SEL-351 Relay. To order an SEL-351 relay, refer to the actual ordering information sheets.

Model 0351x0 and 0351x1 differ only in that model 0351x1 has an extra I/O board (and thus increased rack unit height—see Figure 2.1). Model 0351xY is similar to model 0351x1, except that it has plug-in connectors.

A vertical SEL-351 Relay is available in the 0351x1 and 0351xY models only (see Figure 2.5). The vertical relays use the same rear panels as the horizontal 0351x1 and 0351xY models in Figure 2.4. Though Figure 2.4 shows the extra I/O board (OUT201 through IN208) for model 0351x1, the vertically-mounted version of this model can be ordered without this extra I/O board

(the space appears blank). Any SEL-351 Relay model can be ordered with sensitive Earth Fault (SEF) neutral ground overcurrent elements.

Voltage elements are detailed in **Section 3: Overcurrent, Voltage, Synchronism Check, Frequency, and Power Elements**. Neutral ground overcurrent element differences due to 0.05 A nominal channel IN (SEF) are detailed in the same section. Certain ground directional elements are nonoperational if the SEL-351 Relay is ordered with 0.05 A nominal channel IN (see **Section 4: Loss-of-Potential, Load Encroachment, and Directional Element Logic**). See Figure 1.2 and Figure 1.3 for more information on SEF options.

Throughout this instruction manual, when differences among the SEL-351 Relay models in Table 1.1 are explained, model numbers are referenced for clarity.

Differences between model 0351x0, 0351x1, and 0351xY show up in references to optoisolated inputs, output contacts, and board jumpers. Figure 2.15 through Figure 2.18 and Table 2.2 through Table 2.8 show the labeling differences between the board jumpers.

Table 1.2: SEL-351 Firmware Versions

Model Number	Firmware Version	Relay Features
03515	5	Standard features.
03516	6	Standard features plus MIRRORING BITS™ and load profiling.
<p>SEL-351 Relays with firmware version 5 can be upgraded to firmware version 6. However, SEL-351 Relays with firmware versions 5 and 6 cannot be upgraded to any higher firmware versions. This is due to hardware limitations.</p> <p>The wye-connected voltage inputs for SEL-351 Relays with firmware version 5 or 6 are rated for voltages up to 150 Vac, line-to-neutral (channel VS, too).</p>		
03517	7	Includes firmware version 6 features plus power and voltage sag/swell/interruption elements.
<p>SEL-351 Relays with firmware version 7 come with wye-connected voltage inputs only (connect any voltage up to 300 Vac, line-to-neutral).</p>		

INSTRUCTION MANUAL SECTIONS OVERVIEW

The following is an overview of the other sections in this instruction manual:

Section 2: Installation describes how to mount and wire the SEL-351 Relay. Connections for numerous applications are described. The operation of circuit board jumpers is explained. Figure 2.2 through Figure 2.5 show the SEL-351 Relay front and rear panels.

Section 3: Overcurrent, Voltage, Synchronism Check, Frequency, and Power Elements describes the operation of:

- Instantaneous/definite-time overcurrent elements (phase, neutral ground, residual ground, and negative-sequence)
- Time-overcurrent elements (phase, neutral ground, residual ground, and negative-sequence)

- Voltage elements (single-phase, phase-to-phase, etc.)
- Synchronism check elements
- Frequency elements
- Power Elements (in Firmware Version 7)
- Voltage Sag/Swell/Interruption Elements (in Firmware Version 7).

Section 4: Loss-of-Potential, Load Encroachment, and Directional Element Logic describes the operation of:

- Loss-of-potential logic and its effect on directional elements
- Load-encroachment logic and its application to phase overcurrent elements
- Voltage-polarized and current-polarized directional elements
- *Best Choice Ground Directional*[™] logic and automatic settings

Section 5: Trip and Target Logic describes the operation of:

- General trip logic
- Switch-onto-fault trip logic
- Communications-assisted trip logic
- Front-panel target LEDs

Most tripping applications (not requiring switch-onto-fault or communications-assisted tripping) require only SELOGIC[®] control equation trip setting TR and unlatch trip setting ULTR in the general trip logic (see Figure 5.1).

Section 6: Close and Reclose Logic describes the close logic operation for:

- Automatic reclosures
- Other close conditions (e.g., manual close initiation via serial port or optoisolated inputs)

Section 7: Inputs, Outputs, Timers, and Other Control Logic describes the operation of:

- Optoisolated inputs IN101 through IN106 (models 0351x0, 0351x1 and 0351xY) and IN201 through IN208 (models 0351x1 and 0351xY)
- Local control switches (local bit outputs LB1 through LB16)
- Remote control switches (remote bit outputs RB1 through RB16)
- Latch control switches (latch bit outputs LT1 through LT16)
- Multiple setting groups (six available)
- Programmable timers (timer outputs SV1T through SV16T)
- Output contacts OUT101 through OUT107 and ALARM (models 0351x0, 0351x1, and 0351xY) and OUT201 through OUT 212 (models 0351x1 and 0351xY)
- Rotating default displays

Section 8: Breaker Monitor, Metering, and Load Profile Functions describes the operation of:

- Breaker monitor
- Demand, energy, and max./min. metering
- Load Profile (in Firmware Versions 6 and 7)

Section 9: Setting the Relay explains how to enter settings and also contains the following setting reference information:

- Time-overcurrent curves (5 US and 5 IEC curves)
- Relay Word bit table and definitions (Relay Word bits are used in SELOGIC control equation settings)
- Settings Sheets for general relay, SELOGIC control equation, global, SER, text label, and serial port settings

The Settings Sheets can be photocopied and filled out to set the SEL-351 Relay. Note that these sheets correspond to the serial port SET commands listed in Table 9.1.

Section 10: Serial Port Communications and Commands describes:

- Serial port connector pinout/terminal functions
- Communications cables
- Communications protocol
- Serial port commands

See **SHO Command (Show/View Settings)** in **Section 10** for a list of the factory default settings the SEL-351 Relay ships within a standard relay shipment.

Section 11: Front-Panel Interface describes the front-panel operation of:

- Pushbuttons and correspondence to serial port commands
- Local control switches (local bit outputs LB1 through LB16)
- Rotating default displays

Section 12: Standard Event Reports, Sag/Swell/Interruption Report, and SER describes:

- Standard 15- and 30-cycle event reports
- Sequential events recorder (SER) report
- Voltage Sag/Swell/Interruption (SSI) report (in Firmware Version 7)

Section 13: Testing and Troubleshooting describes:

- General testing philosophy, methods, and tools
- Relay self-tests and troubleshooting

Section 14: Appendices contains the following appendices:

- **Appendix A: Firmware Versions**
- **Appendix B: Firmware Upgrade Instructions**
- **Appendix C: SEL Distributed Port Switch Protocol**
- **Appendix D: Configuration, Fast Meter, and Fast Operate Commands**
- **Appendix E: Compressed ASCII Commands**
- **Appendix F: Setting Negative-Sequence Overcurrent Elements**
- **Appendix G: Setting SELOGIC Control Equations**
- **Appendix H: Distributed Network Protocol (DNP) 3.00**
- **Appendix I: MIRRORED BITS (in Firmware Versions 6 and 7)**
- **Appendix J: Unsolicited SER Protocol**
- **Appendix K: SEL-5030 ACSELERATOR™**

Section 15: SEL-351 Relay Command Summary briefly describes the serial port commands that are described in detail in **Section 10: Serial Port Communications and Commands**.

APPLICATIONS

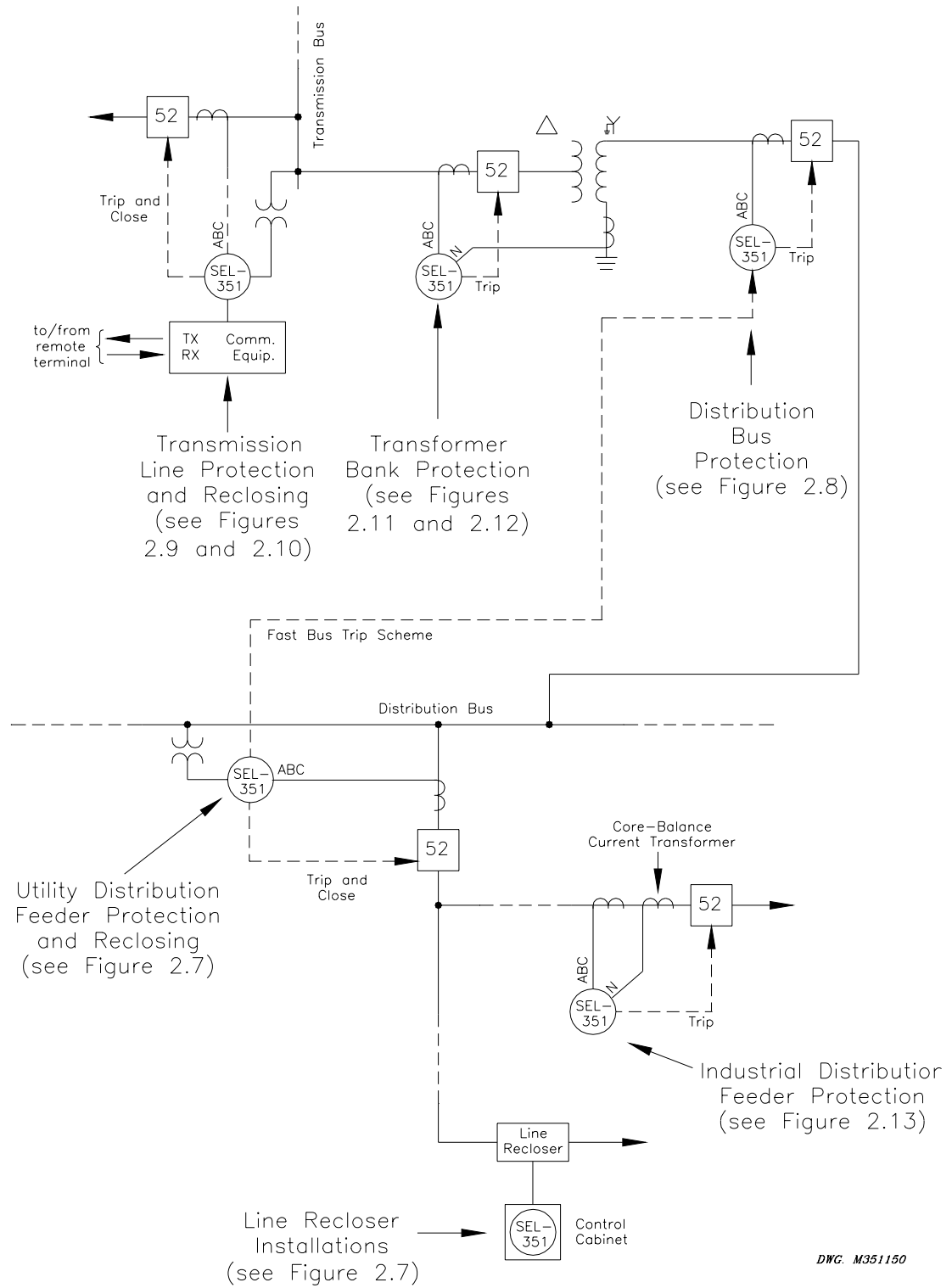


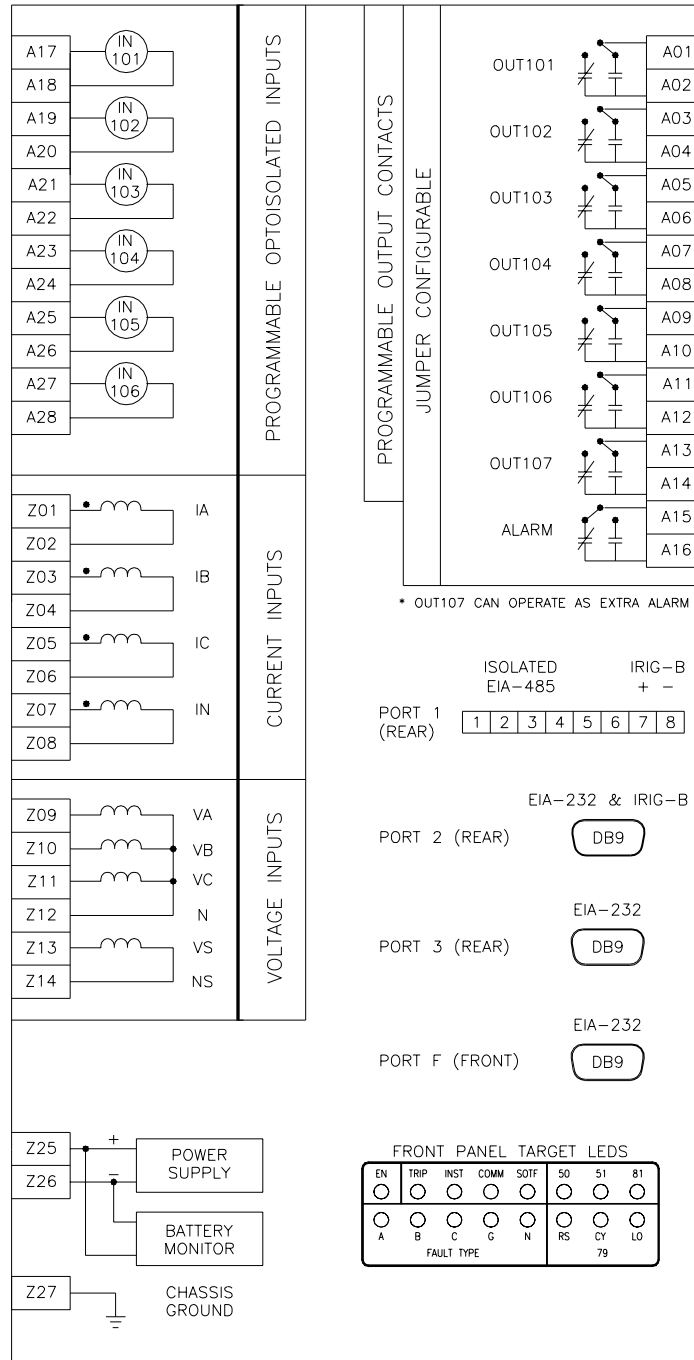
Figure 1.1: SEL-351 Relays Applied Throughout the Power System

HARDWARE CONNECTION FEATURES

See subsection *General Specifications* later in this section and *Section 2: Installation* for more information on hardware and connections.

Channel IN:

For sensitive earth fault (SEF) applications, the SEL-351 Relay should be ordered with channel IN rated at 0.05 A nominal. See item 3 at the bottom of Figures 2.11 and 2.13 for additional reference information.

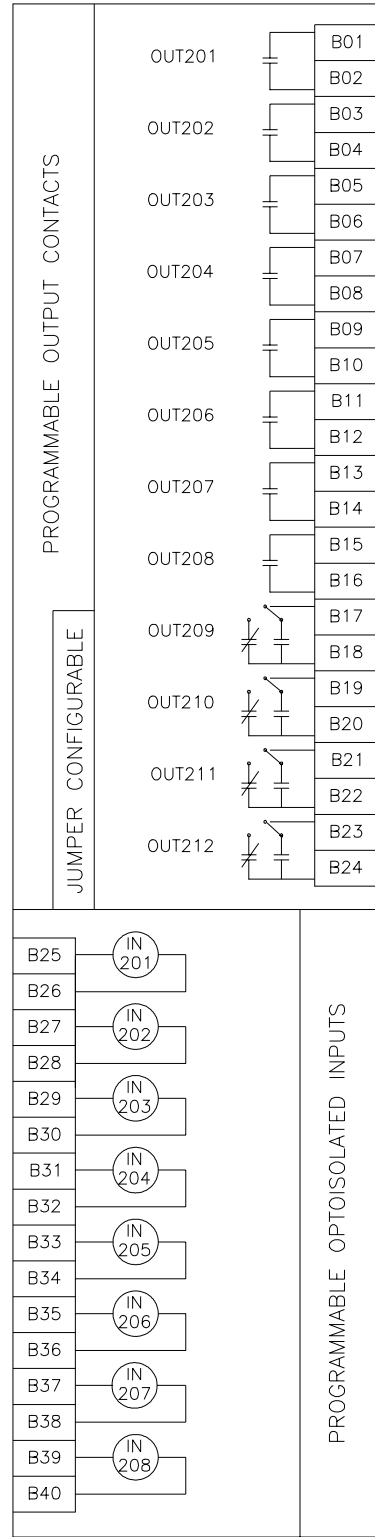


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Figure 1.2: SEL-351 Relay Inputs, Outputs, and Communications Ports (Models 0351x0, 0351x1, and 0351xY; Models 0351x1 and 0351xY Have an Extra I/O Board— See Figure 1.3 and Figure 1.4)

Output Contacts:

If the output contacts are high-current interrupting output contacts, they are polarity dependent. See Table 1.1 for information on SEL-351 Relay models with the high-current interrupting output contact option. See ***Output Contacts*** in ***Section 2: Installation*** for more information on the polarity dependence of high-current interrupting output contacts.

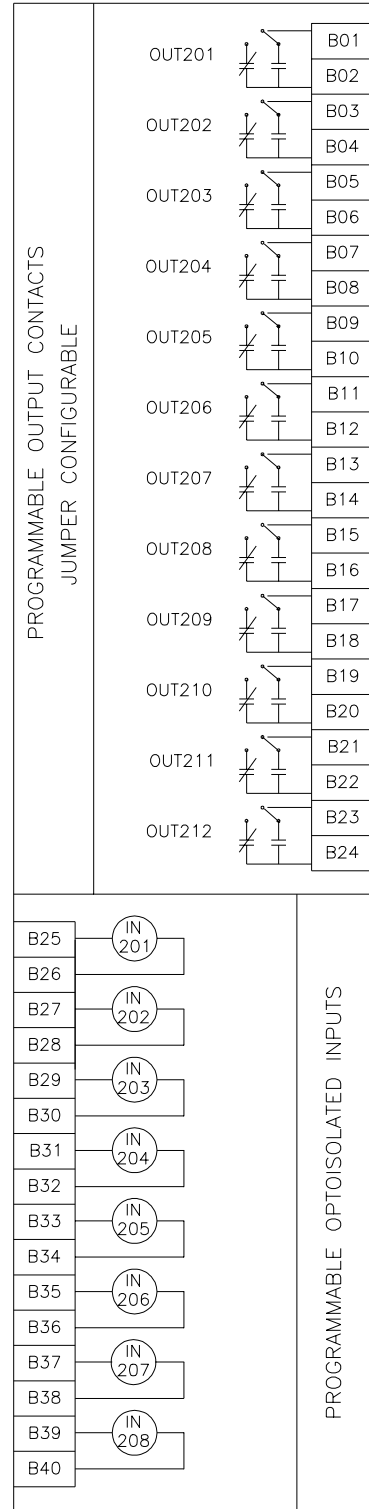


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Figure 1.3: SEL-351 Relay Extra I/O Board (Model 0351xY, Plug-In Connector Version; Main Board Shown in Figure 1.2)

Output Contacts:

If the output contacts are high-current interrupting output contacts, they are polarity dependent. See Table 1.1 for information on SEL-351 Relay models with the high-current interrupting output contact option. See *Output Contacts* in *Section 2: Installation* for more information on the polarity dependence of high-current interrupting output contacts.



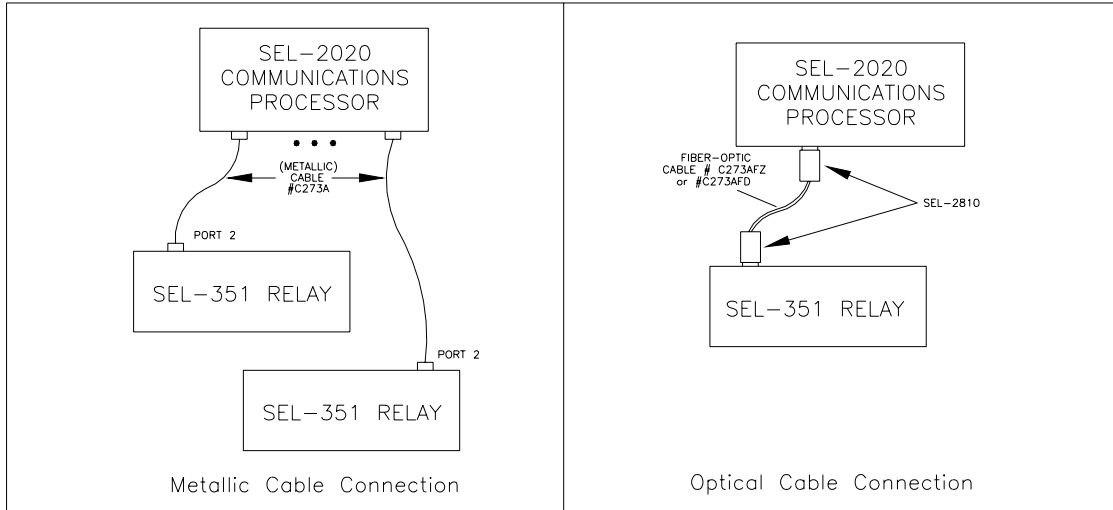
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Figure 1.4: SEL-351 Relay Extra I/O Board (Model 0351x1, Screw-Terminal Block Version; Main Board Shown in Figure 1.2)

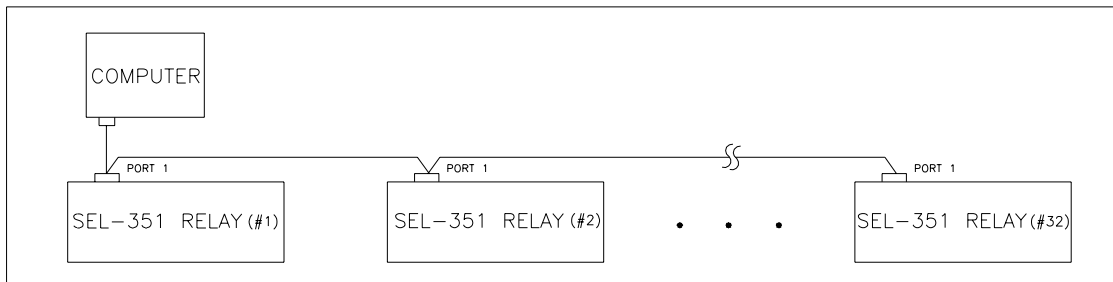
COMMUNICATIONS CONNECTIONS

See *Port Connector and Communications Cables* in **Section 10: Serial Port Communications and Commands** for more communications connections information.

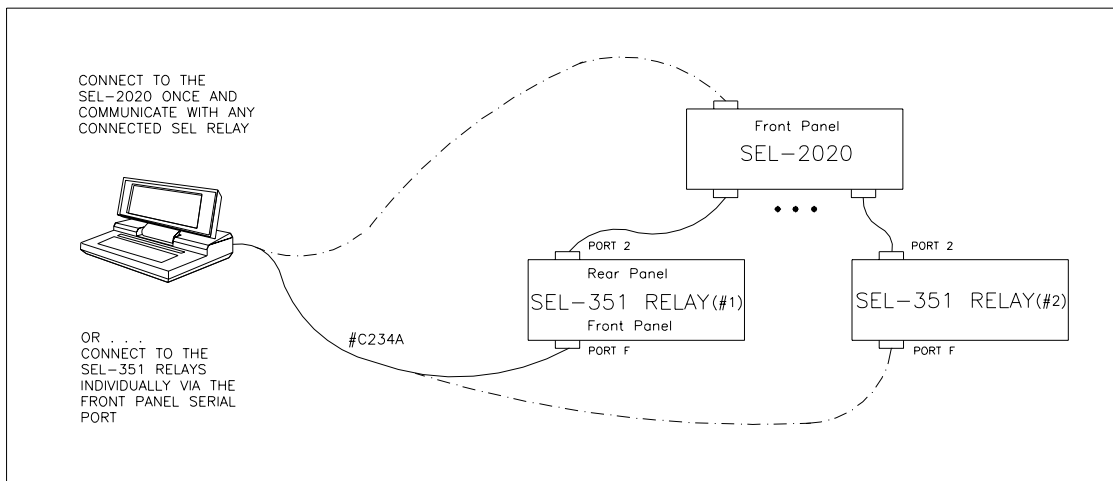
DATA AND TIME-SYNCHRONIZATION CONNECTIONS



EIA-485 CONNECTIONS



LOCAL CONNECTIONS



DWG: M351152

Figure 1.5: SEL-351 Relay Communications Connections Examples

GENERAL SPECIFICATIONS

Important: Do not use the following specification information to order an SEL-351 Relay. Refer to the actual ordering information sheets.

<u>Tightening Torque</u>	Terminal Block: Minimum: 7-in-lb (0.8 Nm) Maximum: 12-in-lb (1.4 Nm) Connectorized [®] : Minimum: 4.4-in-lb (0.5 Nm) Maximum: 8.8-in-lb (1.0 Nm)
---------------------------------	--

Terminal Connections Terminals or stranded copper wire. Ring terminals are recommended. Minimum temperature rating of 90°C.

<u>AC Voltage Inputs</u>	150 V _{L-N} , three-phase four-wire (wye) connection. 150 V continuous (connect any voltage from 0 to 150 Vac). 365 Vac for 10 seconds. Burden: 0.13 VA @ 67 V; 0.45 VA @ 120 V. 300 V _{L-N} , three-phase four-wire (wye) connection. 300 V continuous (connect any voltage from 0 to 300 Vac). 600 Vac for 10 seconds. Burden: 0.03 VA @ 67 V; 0.06 VA @ 120 V; 0.8 VA @ 300 V.
---------------------------------	--

<u>AC Current Inputs</u>	5 A nominal: 15 A continuous, 500 A for 1 second, linear to 100 A symmetrical. 1250 A for 1 cycle. Burden: 0.27 VA @ 5 A, 2.51 VA @ 15 A. 1 A nominal: 3 A continuous, 100 A for 1 second, linear to 20 A symmetrical. 250 A for 1 cycle. Burden: 0.13 VA @ 1 A, 1.31 VA @ 3 A. <u>Sensitive Earth Fault:</u> 0.05 A nominal channel IN current input: 1.5 A continuous, 20 A for 1 second, linear to 1.5 A symmetrical. 100 A for 1 cycle. Burden: 0.0004 VA @ 0.05 A, 0.36 VA @ 1.5 A.
---------------------------------	---

<u>Power Supply</u>	Rated: 125/250 Vdc or Vac Range: 85–350 Vdc or 85–264 Vac Burden: <25 W Rated: 48/125 Vdc or 125 Vac Range: 38–200 Vdc or 85–140 Vac Burden: <25 W Rated: 24/48 Vdc Range: 18–60 Vdc polarity dependent Burden: <25 W
----------------------------	---

Frequency and Rotation 60/50 Hz system frequency and ABC/ACB phase rotation are user-settable. Frequency tracking range: 40.1–65 Hz (V_A required for frequency tracking).

Output Contacts Standard:

6 A continuous carry at 70°C; 4 A continuous carry at 85°C
50 A for one second
MOV protected: 270 Vac, 360 Vdc, 40 J;
Pickup time: Less than 5 ms.
Dropout time: Less than 8 ms, typical.

Breaking Capacity (10,000 operations):

24 V	0.75 A	L/R = 40 ms
48 V	0.50 A	L/R = 40 ms
125 V	0.30 A	L/R = 40 ms
250 V	0.20 A	L/R = 40 ms

Cyclic Capacity (2.5 cycles/second):

24 V	0.75 A	L/R = 40 ms
48 V	0.50 A	L/R = 40 ms
125 V	0.30 A	L/R = 40 ms
250 V	0.20 A	L/R = 40 ms

High-Current Interruption Option for Extra I/O Board:

6 A continuous carry at 70°C; 4 A continuous carry at 85°C
50 A for one second
MOV protected: 330 Vdc, 40 J;
Pickup time: Less than 5 ms.
Dropout time: Less than 8 ms, typical.

Breaking Capacity (10,000 operations):

24 V	10 A	L/R = 40 ms
48 V	10 A	L/R = 40 ms
125 V	10 A	L/R = 40 ms
250 V	10 A	L/R = 20 ms

Cyclic Capacity (4 cycles in 1 second, followed by 2 minutes idle for thermal dissipation):

24 V	10 A	L/R = 40 ms
48 V	10 A	L/R = 40 ms
125 V	10 A	L/R = 40 ms
250 V	10 A	L/R = 20 ms

Note: Do not use high-current interrupting output contacts to switch ac control signals. These outputs are polarity dependent.

Note: Make per IEEE C37.90: 1989; Breaking and Cyclic Capacity per IEC 60255-0-20: 1974.

**Optoisolated
Input Ratings**

When used with dc control signals:

250 Vdc: on for	200–300 Vdc;	off below	150 Vdc
125 Vdc: on for	105–150 Vdc;	off below	75 Vdc
110 Vdc: on for	88–132 Vdc;	off below	66 Vdc
48 Vdc: on for	38.4–60 Vdc;	off below	28.8 Vdc
24 Vdc: on for	15–30 Vdc		

When used with ac control signals:

250 Vdc: on for	170.6–300.0 Vac;	off below	106.0 Vac
125 Vdc: on for	89.6–150.0 Vac;	off below	53.0 Vac
110 Vdc: on for	75.1–132.0 Vac;	off below	46.6 Vac
48 Vdc: on for	32.8–60.0 Vac;	off below	20.3 Vac
24 Vdc: on for	12.8–30.0 Vac		

AC mode is selectable for each input via Global settings IN101D–IN106D; IN201D–IN208D. AC input recognition delay from time of switching: 0.75 cycles maximum pickup; 1.25 cycles maximum dropout.

Note: 24, 48, 125, and 250 Vdc optoisolated inputs draw approximately 5 mA of current, 110 Vdc inputs draw approximately 8 mA of current. All current ratings are at nominal inputs voltages.

Time-Code Input

Relay accepts demodulated IRIG-B time-code input at Port 2. Relay time is synchronized to within ± 5 ms of time-source input.

**Serial
Communications**

Two rear-panels and one front-panel EIA-232 serial communications port. Rear-panel EIA-485 serial port with 2100 Vdc of isolation.

Per Port Baud Rate Selections: 300, 1200, 2400, 4800, 9600, 19200, 38400

Dimensions

See Figure 2.1.

Weight

13 lbs (5.92 kg) — 2U rack unit height relay
16 lbs (7.24 kg) — 3U rack unit height relay

**Routine
Dielectric Test**

Current inputs: 2500 Vac for 10 seconds.

Power supply, optoisolated inputs, and output contacts: 3000 Vdc for 10 seconds.

The following *IEC 60255-5 Dielectric Tests: 1977* are performed on all units with the CE mark:

2500 Vac for 10 seconds on analog inputs.

3100 Vdc for 10 seconds on power supply, optoisolated inputs, and output contacts.

Operating Temp.

-40° to 185°F (-40° to +85°C) (type test).

(LCD contrast impaired for temperatures below -20°C.)

IEC 60068-2-1: 1990 Basic environmental testing procedures, Part 2: Tests - Test Ad: Cold (type test).

IEC 60068-2-2: 1974 Basic environmental testing procedures, Part 2: Tests - Test Bd: Dry Heat (type test).

Environment

IEC 60068-2-30: 1980 Basic environmental testing procedures, Part 2: Tests, Test Db and guidance: Damp heat, cyclic (12 + 12-hour cycle), (six-day type test).

IEC 60529: 1989-11 Degrees of Protection Provided by Enclosures - IP30, IP54 from the front panel using the SEL-9103 Front Cover Dust and Splash Protection (type test).

RFI and Interference Tests

IEEE C37.90.1 - 1989 IEEE SWC Tests for Protective Relays and Relay Systems (3 kV oscillatory, 5 kV fast transient) (type test).

IEEE C37.90.2 - IEEE Trial-Use Standard, Withstand Capability of Relay Systems to Radiated Electromagnetic Interference from Transceivers, 10 V/m (type test).

Exceptions:

- 5.5.2(2) Performed with 200 frequency steps per octave.
- 5.5.3 Digital Equipment Modulation Test not performed.
- 5.5.4 Test signal turned off between frequency steps to simulate keying.

IEC 60801-4: 1988 Electromagnetic compatibility for industrial-process measurement and control equipment, Part 4: Electrical fast transient/burst requirements, Severity Level 4 (4 kV on power supply, 2 kV on inputs and outputs) (type test).

IEC 60255-22-1: 1988 Electrical disturbance tests for measuring relays and protection equipment, Part 1: 1 MHz burst disturbance tests. Severity Level 3 (2.5 kV common mode, 1.0 kV differential) (type test).

IEC 60255-22-3: 1989 Electrical relays, Section 3: Radiated electromagnetic field disturbance tests, Severity Level 3 (10 V/m) (type test).

IEC 60255-22-4: 1992 Electrical disturbance tests for measuring relays and protection equipment, Section 4 - Fast transient disturbance test (type test).

Impulse Tests

IEC 60255-5: 1977 Electrical relays, Part 5: Insulation tests for electrical relays, Section 6: Dielectric Tests, Series C (2500 Vac on analog inputs; 3000 Vdc on power supply, contact inputs, and contact outputs). Section 8: Impulse Voltage Tests, 0.5 Joule 5 kV (type test).

Vibration and Shock Test

IEC 60255-21-1: 1988 Electrical relays, Part 21: Vibration, shock, bump, and seismic tests on measuring relays and protection equipment, Section One - Vibration tests (sinusoidal), Class 1 (type test).

IEC 60255-21-2: 1988 Electrical relays, Part 21: Vibration, shock, bump, and seismic tests on measuring relays and protection equipment, Section Two - Shock and bump tests, Class 1 (type test).

IEC 60255-21-3: 1993 Electrical relays, Part 21: Vibration, shock, bump, and seismic tests on measuring relays and protection equipment, Section Three - Seismic tests, Class 2 (type test).

ESD Test *IEC 60255-22-2: 1996 Electrical disturbance tests for measuring relays and protective equipment, Section 2: Electrostatic discharge tests, Severity Level 4 (8 kV contact discharge all points except serial ports, 15 kV air discharge to all other points) (type test).*

Processing Specifications

AC Voltage and Current Inputs 16 samples per power system cycle, 3 dB low-pass filter cut-off frequency of 560 Hz.

Digital Filtering One cycle cosine after low-pass analog filtering.
Net filtering (analog plus digital) rejects dc and all harmonics greater than the fundamental.

Protection and Control Processing 4 times per power system cycle

Relay Element Pickup Ranges and Accuracies

Instantaneous/Definite-Time Overcurrent Elements

Pickup Range:	0.25–100.00 A, 0.01 A steps (5 A nominal) 1.00–170.00 A, 0.01 A steps (5 A nominal—for phase-to-phase elements) 0.05–20.00 A, 0.01 A steps (1 A nominal) 0.20–34.00 A, 0.01 A steps (1 A nominal—for phase-to-phase elements) 0.005–1.500 A, 0.001 A steps (0.05 A nominal channel IN current input)
Steady-State Pickup Accuracy:	±0.05 A and ±3% of setting (5 A nominal) ±0.01 A and ±3% of setting (1 A nominal) ±1 mA and ±5% of setting (0.05 A nominal channel IN current input)
Transient Overreach:	±5% of pickup
Time Delay:	0.00–16,000.00 cycles, 0.25-cycle steps
Timer Accuracy:	±0.25 cycle and ±0.1% of setting
Undervoltage Frequency Element Block Range:	12.50–150.00 V (150 V wye) 25.00–300.00 V (300 V wye)

See pickup and reset time curves in Figure 3.5 and Figure 3.6

Time-Overcurrent Elements

Pickup Range:	0.50–16.00 A, 0.01 A steps (5 A nominal) 0.10–3.20 A, 0.01 A steps (1 A nominal) 0.005–0.160 A, 0.001 A steps (0.05 A nominal channel IN current input)
Steady-State Pickup Accuracy:	± 0.05 A and $\pm 3\%$ of setting (5 A nominal) ± 0.01 A and $\pm 3\%$ of setting (1 A nominal) ± 1 mA and $\pm 5\%$ of setting (0.05 A nominal channel IN current input)
Time Dial Range:	0.50–15.00, 0.01 steps (US) 0.05–1.00, 0.01 steps (IEC)
Curve Timing Accuracy:	± 1.50 cycles and $\pm 4\%$ of curve time for current between 2 and 30 multiples of pickup

Under- and Overvoltage Elements

Pickup Ranges:	0.00–150.00 V, 0.01 V steps (various elements) {150 V voltage inputs} 0.00–300.00 V, 0.01 V steps (various elements) {300V voltage inputs} 0.00–260.00 V, 0.01 V steps (phase-to-phase elements) {150 V voltage inputs} 0.00–520.00 V, 0.01 V steps (phase-to-phase elements) {300 V voltage inputs}
Steady-State Pickup Accuracy:	± 1 V and $\pm 5\%$ of setting {150 V voltage inputs} ± 2 V and $\pm 5\%$ of setting {300 V voltage inputs}
Transient Overreach:	$\pm 5\%$ of pickup

Synchronism-Check Elements

Slip Frequency Pickup Range:	0.005–0.500 Hz, 0.001 Hz steps
Slip Frequency Pickup Accuracy:	± 0.003 Hz
Phase Angle Range:	0–80°, 1° steps
Phase Angle Accuracy:	$\pm 4^\circ$

Under- and Overfrequency Elements

Pickup Range:	40.10–65.00 Hz, 0.01 Hz steps
Steady-State <i>plus</i> Transient Overshoot:	± 0.01 Hz
Time Delay:	2.00–16,000.00 cycles, 0.25-cycle steps
Timer Accuracy:	± 0.25 cycle and $\pm 0.1\%$ of setting

Timers

Pickup Ranges:	0.00–999,999.00 cycles, 0.25-cycle steps (reclosing relay and some programmable timers)
	0.00–16,000.00 cycles, 0.25-cycle steps (some programmable and other various timers)
Pickup and dropout accuracy for all timers:	±0.25 cycle and ±0.1% of setting

Substation Battery Voltage Monitor

Pickup Range:	20–300 Vdc, 1 Vdc steps
Pickup Accuracy:	±2% of setting

Metering Accuracy

Accuracies are specified at 20°C and at nominal system frequency unless noted otherwise.

Voltages $V_A, V_B, V_C, V_S, 3V_0, V_1, V_2$	±0.1% (33.5–150 V; wye-connected) {150 V voltage inputs} ±0.2% (67.0–300 V; wye-connected) {300 V voltage inputs}
Currents I_A, I_B, I_C	±1 mA and ±0.1% (0.5–10 A) (5 A nominal) ±0.2 mA and ±0.1% (0.1–2 A) (1 A nominal) Temperature coefficient: $[(0.0002\%)/(^{\circ}\text{C})^2] * (\text{ }^{\circ}\text{C} - 20^{\circ}\text{C})^2$ (see example below)
Currents $I_N, I_1, 3I_0, 3I_2$	±0.05 A and ±3% (0.5–100 A) (5 A nominal) ±0.01 A and ±3% (0.1–20 A) (1 A nominal) ±1 mA and ±5% (0.01–1.5 A) (0.05 A nominal channel IN current input)
Phase Angle Accuracy	±0.5°

MW / MVAR
(A, B, C, and 3-phase; 5 A nominal;
wye-connected voltages)

Accuracy (MW / MVAR)	at load angle
for 0.5 A ≤ phase current < 1.0 A s:	
0.70% / -	0° or 180° (unity power factor)
0.75% / 6.50%	±8° or ±172°
1.00% / 2.00%	±30° or ±150°
1.50% / 1.50%	±45° or ±135°
2.00% / 1.00%	±60° or ±120°
6.50% / 0.75%	±82° or ±98°
- / 0.70%	±90° (power factor = 0)
for phase current ≥ 1.0 A s:	
0.35% / -	0° or 180° (unity power factor)
0.40% / 6.00%	±8 or ±172°
0.75% / 1.50%	±30° or ±150°
1.00% / 1.00%	±45° or ±135°
1.50% / 0.75%	±60° or ±120°
6.00% / 0.40%	±82° or ±98°
- / 0.35%	±90° (power factor = 0)

Metering accuracy calculation example for currents I_A, I_B, and I_C due to preceding stated temperature coefficient:

For temperature of 40°C, the additional error for currents I_A, I_B, and I_C is:

$$[(0.0002\%)/(\text{°C})^2] \cdot (40\text{°C} - 20\text{°C})^2 = 0.08\%$$

Power Element Accuracy

Pickup: ±0.005 A • (voltage secondary) and ±5% of setting at unity power factor {1 A nom}
±0.025 A • (voltage secondary) and ±5% of setting at unity power factor {5 A nom}

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SECTION 2: INSTALLATION

RELAY MOUNTING

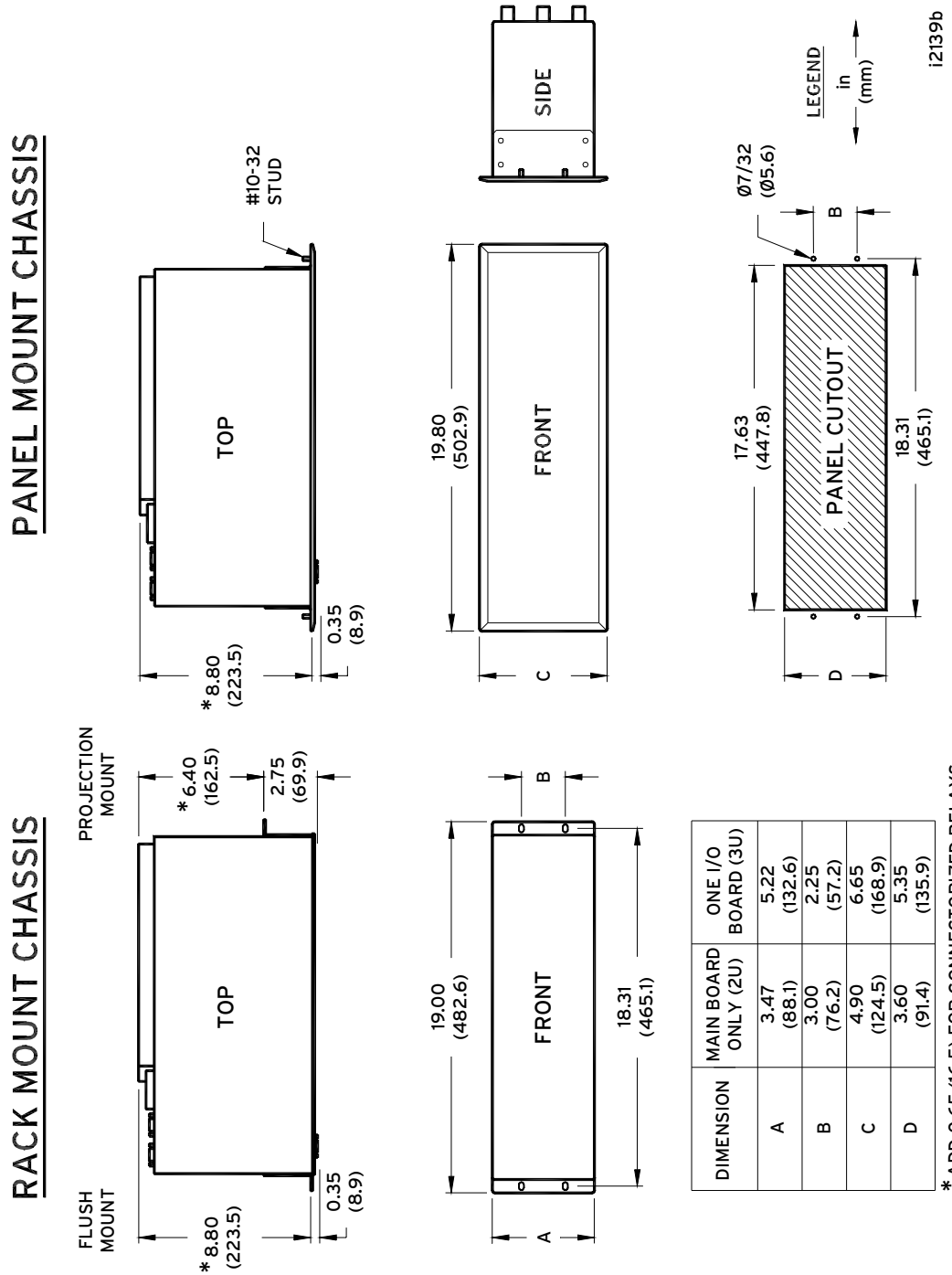


Figure 2.1: SEL-351 Relay Dimensions for Rack-Mount and Panel-Mount Models

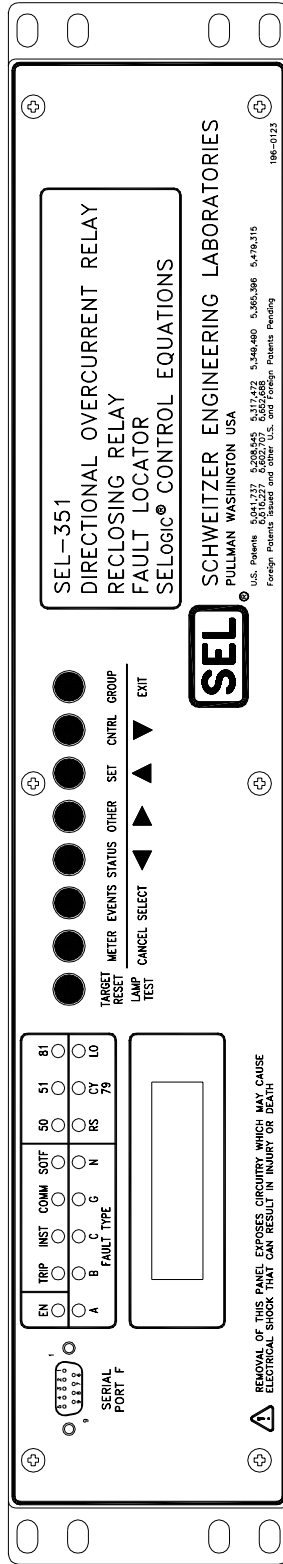
Figure 2.1 gives the SEL-351 Relay dimensions for rack-mount and panel-mount models.

For panel-mount models, the 7/32" (5.6 mm) drill holes shown in the Figure 2.1 panel cutout are to accommodate the four integral #10-32 studs that project out the back of the front panel of the panel-mount relays. These studs are used to fasten the panel-mount relays to the greater panel surface, which has been drilled and cut according to Figure 2.1 specifications. The panel-mount relays slide in from the front and are fastened (via the integral studs) on the back.

The rack-mount and panel-mount dimensions are identical except the front panel dimensions on the panel-mount version are larger to hide any panel cuts.

REAR-PANEL CONNECTION DIAGRAMS

Figure 2.2 through Figure 2.4 represent examples of different relay configurations. All 3U-rack-height units can be ordered with terminal block, plug-in connectors, or extra I/O. All 2-U rack height units are equipped with terminal blocks only. For model options, view the SEL-351 Model Options Table on our web site, or contact your local SEL sales representative.



DWG. 11130

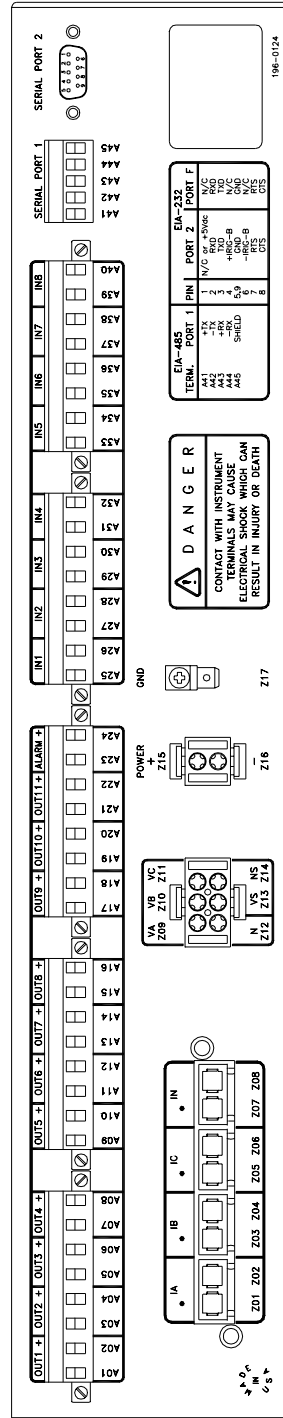
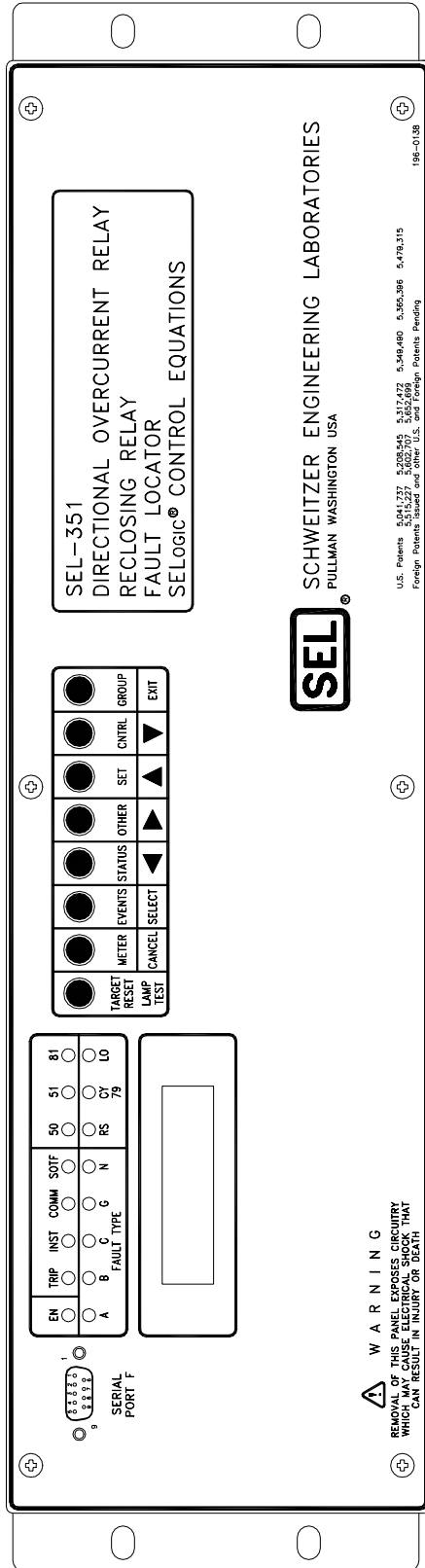
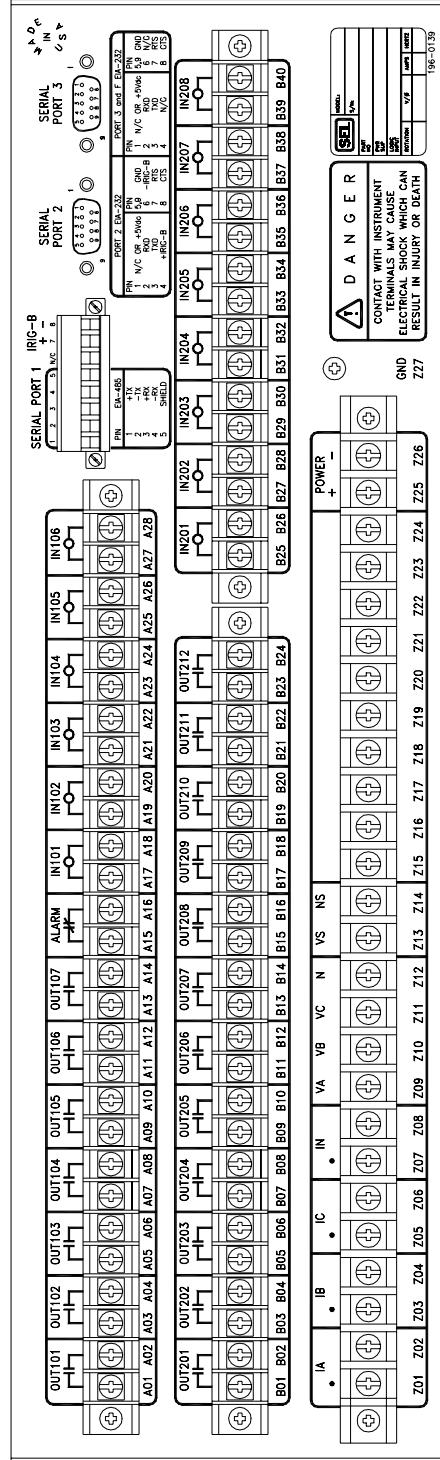


Figure 2.2: SEL-351 Relay Front- and Rear-Panel Drawings (Model 0351x0)



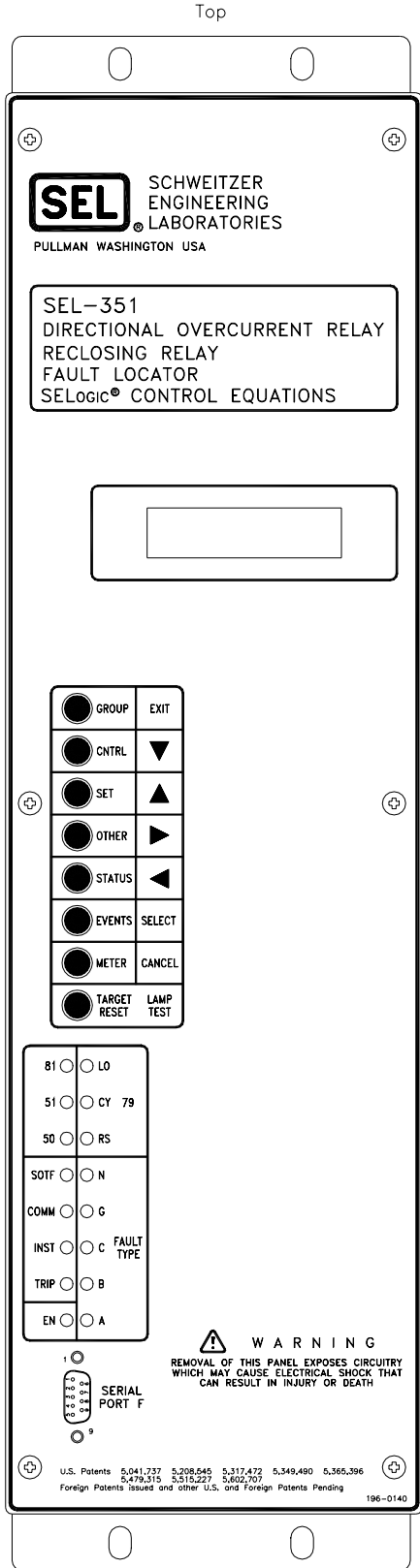
DWG: 11192



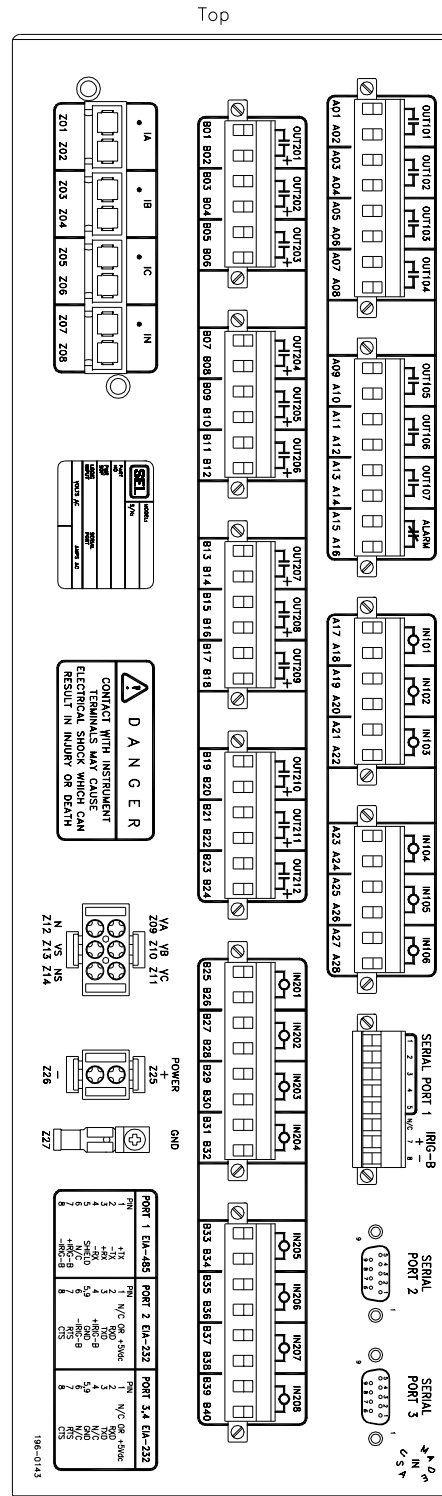
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Figure 2.3: SEL-351 Relay Front- and Rear-Panel Drawings—Model 0351x1 Rear and Models 0351x1 and 0351xY Front (Horizontal)

DWG: M351137



DWG: i1316



DWG: i1357

Figure 2.4: SEL-351 Relay Front- and Rear-Panel Drawings—Model 0351xY Rear and Models 0351x1 and 0351xY Front (Vertical)

MAKING REAR-PANEL CONNECTIONS

Refer to Figure 2.6 through Figure 2.13 for wiring examples of typical applications.

Refer to Table 1.1 and Figure 2.2 through Figure 2.4. Notice the two types of rear-panel hardware connections. Reference is made to the model numbers in discussing rear-panel connection differences in the following text.

Improvements in Connectorized® SEL-351 Relays (Plug-In Connectors) Result in Part Number Changes

The current transformer shorting connector (for current channel inputs IA, IB, IC, and IN) has been made more robust. This improvement makes the new connector design incompatible with the old design. Thus, presently constructed Connectorized SEL-351 Relays with this improved connector have a new part number (partial part numbers shown; see also Table 1.1 in *Section 1: Introduction and Specifications*):

<u>old</u>		<u>new</u>
0351xJ	→	0351xY

The respective wiring harness part numbers for these old and new Connectorized SEL-351 Relays are (partial part numbers shown):

<u>old</u>		<u>new</u>
WA0351xJ	→	WA0351xY

The other connectors on the Connectorized SEL-351 Relay rear panel (power input, voltage inputs, output contacts, etc.) are the same for the old or new models. Only the current transformer shorting connector has changed.

Figure 2.4 shows the rear panel for new model 0351xY. This figure can also be used as a reference for old model 0351xJ. All terminal labeling/numbering remains the same.

Required Equipment and General Connection Information

Models 0351xY (Plug-In Connectors)

Tools: small slotted-tip screwdriver, wire strippers

Parts: SEL-WA0351xY Wiring Harness

Wiring Harness

The SEL-WA0351xY Wiring Harness includes all connectors necessary for relay installation. All connectors requiring special termination come prewired from the factory. Refer to the SEL-WA0351xY Model Option Tables, which are available from the factory.

The SEL-WA0351xY Wiring Harness includes the following connectors (not prewired):

- (2) 8-position female plug-in connectors for output contacts OUT101 through ALARM.
- (2) 6-position female plug-in connectors for optoisolated inputs IN101 through IN106.
- (1) 8-position female plug-in connectors for EIA-485/IRIG-B Serial Port 1.

- (4) 6-position female plug-in connectors for output contacts OUT201 through OUT212.
- (2) 8-position female plug-in connectors for optoisolated inputs IN201 through IN208.

These connectors accept wire size AWG 24 to 12. Strip the wires 0.31 inches (8 mm) and install with a small slotted-tip screwdriver. Secure each 8-position connector to the relay chassis with the screws located on either end of the connector. The 8-position connectors are coded at the factory to prevent swapping connectors during installation. Refer to Figure 2.5 for the standard input/output connector coding.

The wiring harness includes the following prewired connectors:

- (1) ct shorting connector for current inputs IA, IB, IC, and IN.
- (1) connector for voltage inputs VA, VB, VC, and VS.
- (1) connector for POWER inputs (+ and -).
- (1) spade connector for GROUND connection (chassis ground).

These prewired connectors (and the serial port connector) are unique and may only be installed in one orientation.

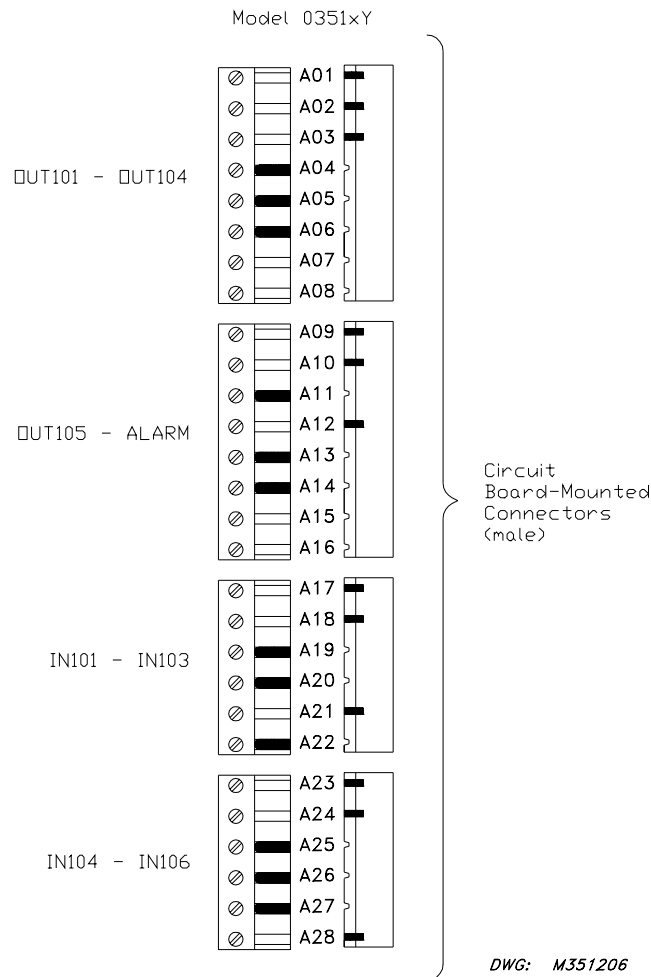


Figure 2.5: SEL-351 Relay Plug-In Connector Coding (Top View; Model 0351xY)

Models 0351x0 and 0351x1 (Screw-Terminal Blocks)

Tools: Phillips or slotted-tip screwdriver

Parts: All screws are size #6-32. Locking screws can be requested from the factory.

Chassis Ground

Model 0351xY

Ground the relay chassis at terminal Z27 with the spade connector provided in the previously discussed wiring harness (tab size 0.250 inches x 0.032 inches). If the tab on the chassis is removed, the chassis ground connection can be made with the size #6-32 screw.

Models 0351x0 and 0351x1

Ground the relay chassis at terminal Z27.

Power Supply

Model 0351xY

The power supply wiring harness includes a two-position connector and factory-installed wire. Note the polarity indicators on terminals Z25(+) and Z26(-). Control power passes through these terminals to a fuse and to the switching power supply. The control power circuitry is isolated from the relay chassis ground.

Plug the power supply connector into terminals Z25 and Z26. The connector locks in place upon insertion.

Refer to *Section 1: Introduction and Specifications* for power supply ratings. The relay power supply rating is listed on the serial number sticker on the relay rear panel.

Models 0351x0 and 0351x1

Connect control voltage to the POWER terminals. Note the polarity indicators on terminals Z25(+) and Z26(-). Control power passes through these terminals to a fuse and to the switching power supply. The control power circuitry is isolated from the relay chassis ground.

Refer to *Section 1: Introduction and Specifications* for power supply ratings. The relay power supply rating is listed on the serial number sticker on the relay rear panel.

Output Contacts

Model 0351x0

Model 0351x0 can be ordered with standard output contacts only. Refer to *General Specifications* in *Section 1: Introduction and Specifications* for output contact ratings.

Standard output contacts are not polarity dependent.

Models 0351x1 and 0351xY

Models 0351x1 and 0351xY have output contacts on the:

main board	OUT101 through ALARM (ordered as standard output contacts only)
extra I/O board	OUT201 through OUT212 [ordered as standard or high-current interrupting output contacts (all of one type or the other)]

Refer to *General Specifications* in *Section 1: Introduction and Specifications* for output contact ratings. To determine the type of output contacts on the extra I/O board of your Model 0351x1 relay, refer to the part number on the serial number sticker on the relay rear panel.

Standard Output Contacts

Models 0351x1 and 0351xY part numbers with a numeral “2” in the field underlined below (sample part numbers) indicate standard output contacts on the extra I/O board (OUT201 through OUT212):

0351x1H42542X1 0351xYH42542X1

Standard output contacts are not polarity dependent.

High-Current Interrupting Output Contacts

Models 0351x1 and 0351xY part numbers with a numeral “6” in the field underlined below (sample part numbers) indicate high-current interrupting output contacts on the extra I/O board (OUT201 through OUT212):

0351x1H42546X1 0351xYH42546X1

High-current interrupting output contacts are polarity dependent. Note the “+” polarity markings above even-numbered terminals B02, B04, B06, ..., B24 in Figure 2.4. The extra I/O board of the Model 0351x1 relay in Figure 2.3 does not show these “+” polarity markings (because it is the rear panel for an extra I/O board with standard output contacts).

As an example, consider the connection of terminals B01 and B02 (high-current interrupting output contact OUT201) in a circuit:

Terminal B02 (+) has to be at a higher voltage potential than terminal B01 in the circuit.

The same holds true for output contacts OUT202 through OUT212 (if they are also high-current interrupting output contacts).

Note: Do not use the high-current interrupting output contacts to switch ac control signals.

Optoisolated Inputs

The optoisolated inputs in any of the SEL-351 Relay models (e.g., IN102, IN207) are not polarity dependent. With nominal control voltage applied, each optoisolated input draws approximately 4 mA of current. Refer to *General Specifications* in *Section 1: Introduction and Specifications* for optoisolated input ratings.

Inputs can be configured to respond to ac or dc control signals via Global settings IN101D–IN106D and IN201D–IN208D.

Refer to the serial number sticker on the relay rear panel for the optoisolated input voltage rating (listed under label: LOGIC INPUT).

Current Transformer Inputs

Model 0351xY

The wiring harness includes a prewired eight-position ct shorting connector. Note the polarity dots above terminals Z01, Z03, Z05, and Z07. Refer to Figure 2.6 through Figure 2.13 for typical ct wiring examples.

Plug the ct shorting connector into terminals Z01 through Z08. Secure the connector to the relay chassis with the two screws located on either end of the connector. When removing the ct shorting connector, pull it straight out away from the rear panel. With the ct shorting connector removed from the rear panel, internal mechanisms in the connector separately short out each individual power system current transformer.

The connector accepts wire size AWG 16 to 10. A special tool is used at the factory to attach the wire to the connector.

Refer to the serial number sticker on the relay rear panel for the nominal current ratings (5 A or 1 A) for the phase (IA, IB, IC) and neutral (IN) current inputs (listed under label: AMPS AC). The neutral (IN) current input also has a 0.05 A nominal current option.

Models 0351x0 and 0351x1

Note the polarity dots above terminals Z01, Z03, Z05, and Z07. Refer to Figure 2.6 through Figure 2.13 for typical ct wiring examples.

Refer to the serial number sticker on the relay rear panel for the nominal current ratings (5 A or 1 A) for the phase (IA, IB, IC) and neutral (IN) current inputs (listed under label: AMPS AC). The neutral (IN) current input also has a 0.05 A nominal current option.

Potential Transformer Inputs

Model 0351xY

The pt wiring harness includes a prewired six-position connector. Plug the connector into terminals Z09 through Z14. The connector is keyed uniquely and locks in place upon insertion.

Note the signal labels (VA, VB, VC, N, VS, NS) on terminals Z09 through Z14. Figure 1.2 shows the internal connection for terminals VA, VB, VC, and N. Note also that VS/NS is a separate single-phase voltage input.

Wye-Connected Voltages

Any of the single-phase voltage inputs (i.e., VA-N, VB-N, VC-N, or VS-NS) can be connected to voltages up to 150 V (or 300 V; see Table 1.2) continuous. Figure 2.6 through Figure 2.11 show examples of wye-connected voltages. Frequency is determined from the voltages connected to terminals VA-N and VS-NS (see subsections *Synchronism Check Elements* and *Frequency*

Elements in Section 3: Overcurrent, Voltage, Synchronism Check, Frequency, and Power Elements).

Model 0351xY part numbers with a numeral “2” or “5” in the field underlined below (sample part numbers) indicate wye-connected voltage inputs:

0351xYH42542X1
0351xYH45542X1

Models 0351x0 and 0351x1

Note the signal labels (VA, VB, VC, N, VS, NS) on terminals Z09 through Z14. Figure 1.2 shows the internal connection for terminals VA, VB, VC, and N. Note also that VS/NS is a separate single-phase voltage input.

Wye-Connected Voltages

Any of the single-phase voltage inputs (i.e., VA-N, VB-N, VC-N, or VS-NS) can be connected to voltages up to 150 V (or 300 V; see Table 1.2) continuous. Figure 2.6 through Figure 2.11 show examples of wye-connected voltages. Frequency is determined from the voltages connected to terminals VA-N and VS-NS (see subsections *Synchronism Check Elements* and *Frequency Elements in Section 3: Overcurrent, Voltage, Synchronism Check, Frequency, and Power Elements*). Model 0351x0 or 0351x1 part numbers with a numeral “2” or “5” in the field underlined below (model 0351x0 sample part number shown) indicate wye-connected voltage inputs:

0351x0H42542X1
0351x0H45542X1

Serial Ports

Refer to Table 10.1 for information on the serial ports available on the different SEL-351 Relay models. All ports are independent—you can communicate to any combination simultaneously.

Serial Port 1 on all the SEL-351 Relay models is an EIA-485 port (4-wire). The Serial Port 1 plug-in connector accepts wire size AWG 24 to 12. Strip the wires 0.31 inches (8 mm) and install with a small slotted-tip screwdriver. For models 0351x0, 0351x1, and 0351xY, the Serial Port 1 connector has extra positions for IRIG-B time-code signal input (see Table 10.3; see following discussion on IRIG-B time code input).

All EIA-232 ports accept 9-pin D-subminiature male connectors. Port 2 on all the SEL-351 Relay models includes the IRIG-B time-code signal input (see Table 10.2; see following discussion on IRIG-B time code input).

The pin definitions for all the ports are given on the relay rear panel and detailed in Table 10.2 through Table 10.4 in *Section 10: Serial Port Communications and Commands*.

Refer to Table 2.1 for a list of cables available from SEL for various communication applications. Refer to *Section 10: Serial Port Communications and Commands* for detailed cable diagrams for selected cables (cable diagrams precede Table 10.4).

Note: Listing of devices not manufactured by SEL in Table 2.1 is for the convenience of our customers. SEL does not specifically endorse or recommend such products, nor does

SEL guarantee proper operation of those products, or the correctness of connections, over which SEL has no control.

For example, to connect any EIA-232 port to the 9-pin male connector on a laptop computer, order cable number C234A and specify the length needed (standard length is eight feet). To connect the SEL-351 Relay Port 2 to the SEL-2020 Communications Processor that supplies the communication link and the IRIG-B time synchronization signal, order cable number C273A. For connecting devices at distances over 100 feet, SEL offers fiber-optic transceivers. The SEL-2800 family of transceivers provides fiber-optic links between devices for electrical isolation and long distance signal transmission. Contact SEL for further information on these products.

Table 2.1: Communication Cables to Connect the SEL-351 Relay to Other Devices

SEL-351 EIA-232 Serial Ports	Connect to Device (gender refers to the device)	SEL Cable No.
All EIA-232 ports	PC, 25-Pin Male (DTE)	C227A
All EIA-232 ports	Laptop PC, 9-Pin Male (DTE)	C234A
All EIA-232 ports	SEL-2020/2030/2100 without IRIG-B	C272A
2	SEL-2020/2030/2100 with IRIG-B	C273A
All EIA-232 ports	SEL-PRTU	C231
All EIA-232 ports	SEL-DTA2	C272A
2* 3* (models 0351x0, 0351x1, and 0351xY only)	Telenetics Modem, 5 Vdc Powered	C220*
All EIA-232 ports	Standard Modem, 25-Pin Female (DCE)	C222
All EIA-232 ports	RFL-9660	C245A

* A corresponding main board jumper must be installed to power the Telenetics Modem with +5 Vdc (0.5 A limit) from the SEL-351 Relay. See Figure 2.14 and Table 2.7.

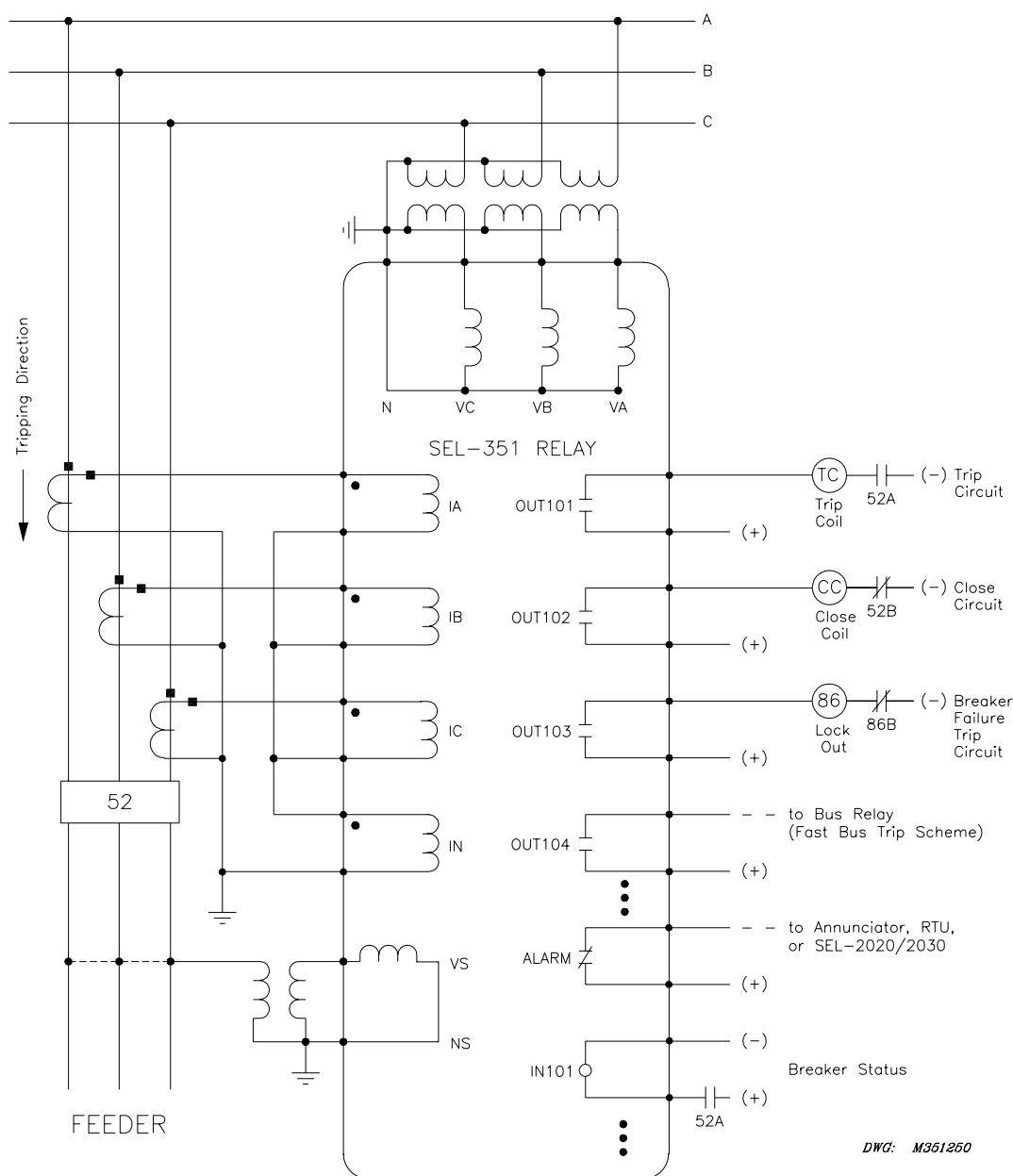
IRIG-B Time-Code Input

The SEL-351 Relay accepts a demodulated IRIG-B time signal to synchronize the relay internal clock with some external source. The demodulated IRIG-B time signal can come via the SEL-2020 or SEL-2030 Communications Processor or the SEL-2100 Protection Logic Processor listed in Table 2.1.

A demodulated IRIG-B time code can be input into Serial Port 2 on any of the SEL-351 Relay models (see Table 10.2). This is handled adeptly by connecting Serial Port 2 of the SEL-351 Relay to an SEL-2020, SEL-2030, or SEL-2100 with Cable C273A.

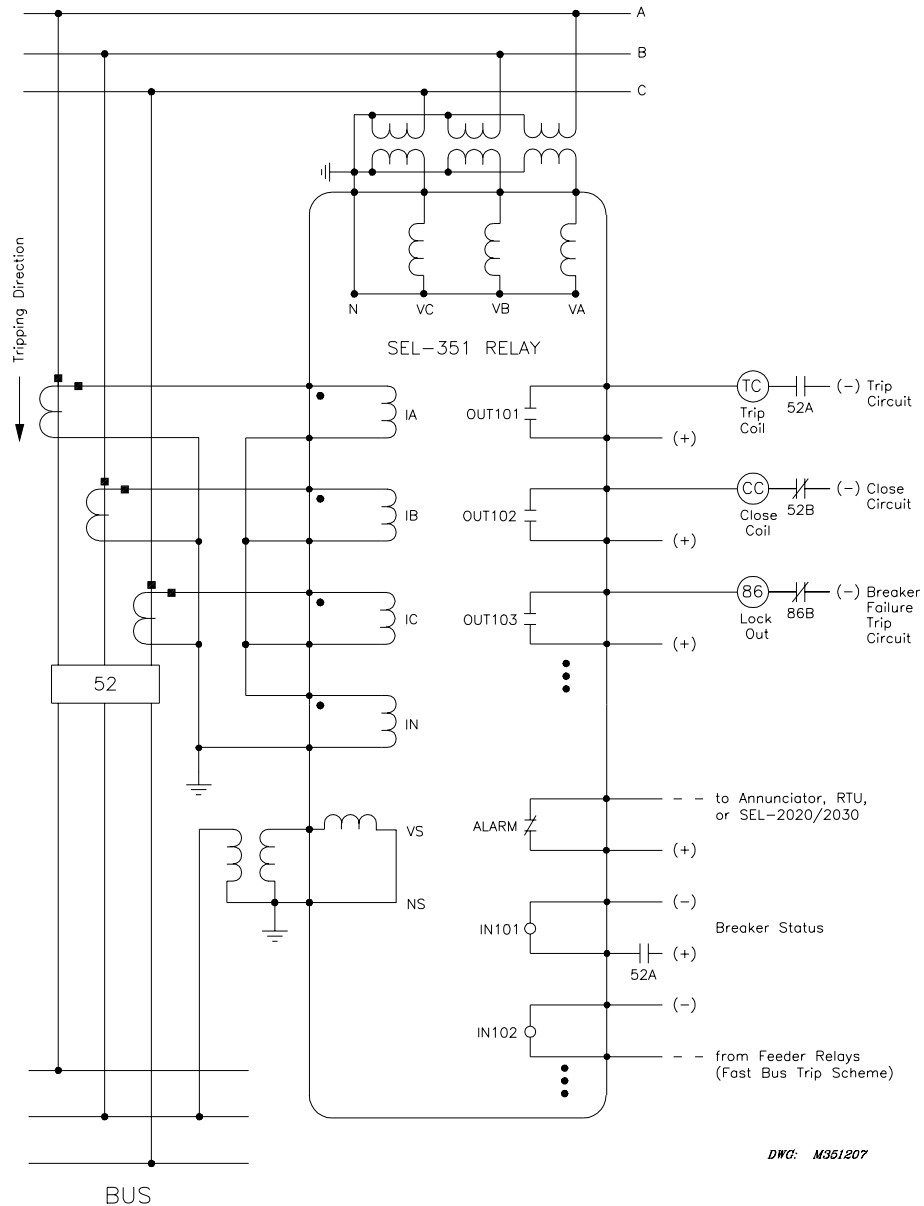
A demodulated IRIG-B time code can be input into the connector for Serial Port 1 on models 0351x0, 0351x1, and 0351xY (see Table 10.3). If demodulated IRIG-B time code is input into this connector, it should not be input into Serial Port 2 and vice versa.

SEL-351 RELAY AC/DC CONNECTION DIAGRAMS FOR VARIOUS APPLICATIONS



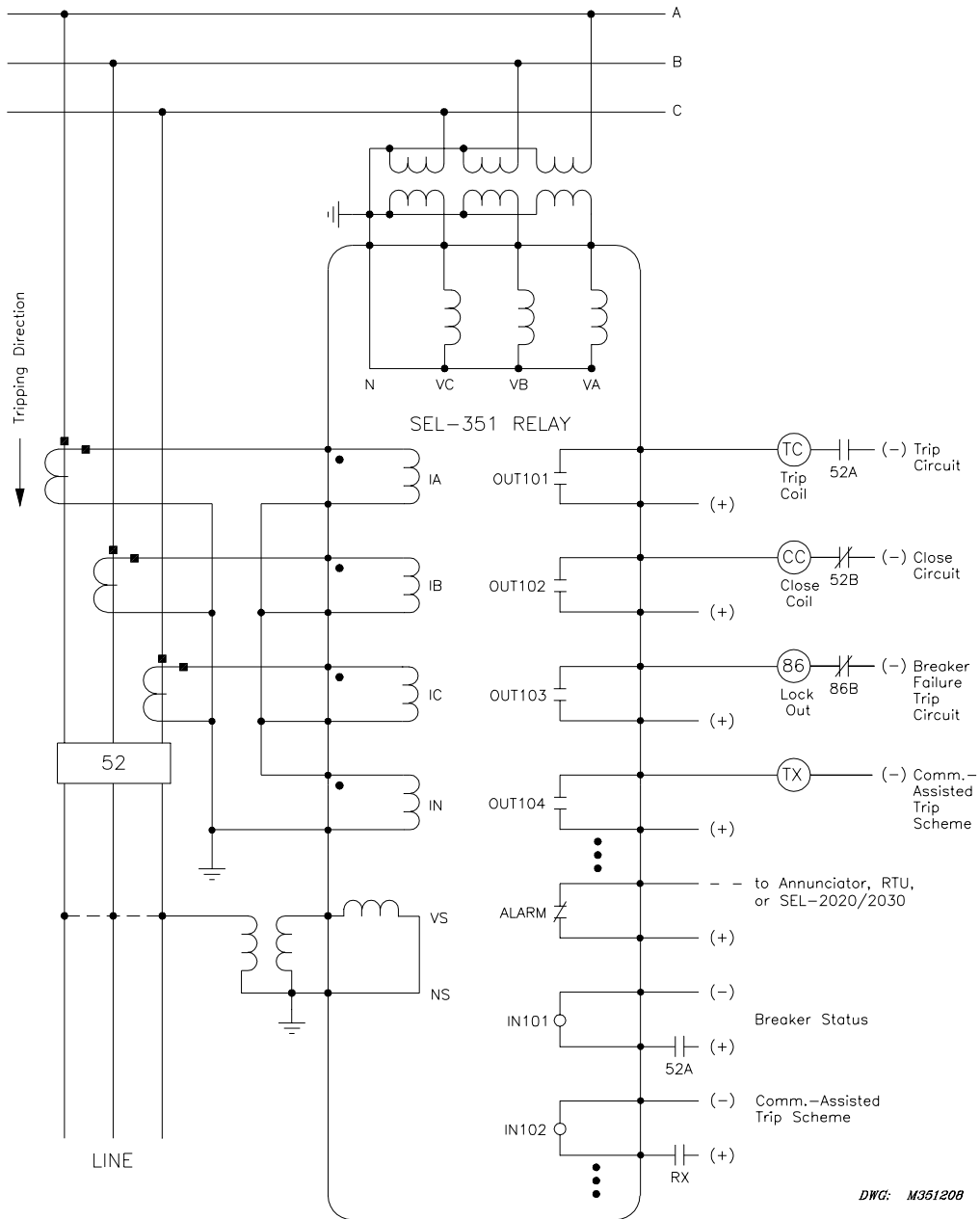
1. For line recloser control installations (see bottom of Figure 1.1), an SEL-351 Relay is connected much like this example.
2. The voltage inputs do not need to be connected. Voltage is needed for voltage elements, synchronism check elements, frequency elements, voltage-polarized directional elements, fault location, metering (i.e., voltage, MW, MVAR), and frequency tracking. Voltage Channel VS is used only in voltage and synchronism check elements and voltage metering.
3. Current Channel IN does not need to be connected. Channel IN provides current I_N for the neutral ground overcurrent elements. Separate from Channel IN, the residual ground overcurrent elements operate from the internally derived residual current I_G ($I_G = 3I_0 = I_A + I_B + I_C$). But in this residual connection example, the neutral ground and residual ground overcurrent elements operate the same because $I_N = I_G$.

Figure 2.6: SEL-351 Relay Provides Overcurrent Protection and Reclosing for a Utility Distribution Feeder (Includes Fast Bus Trip Scheme)



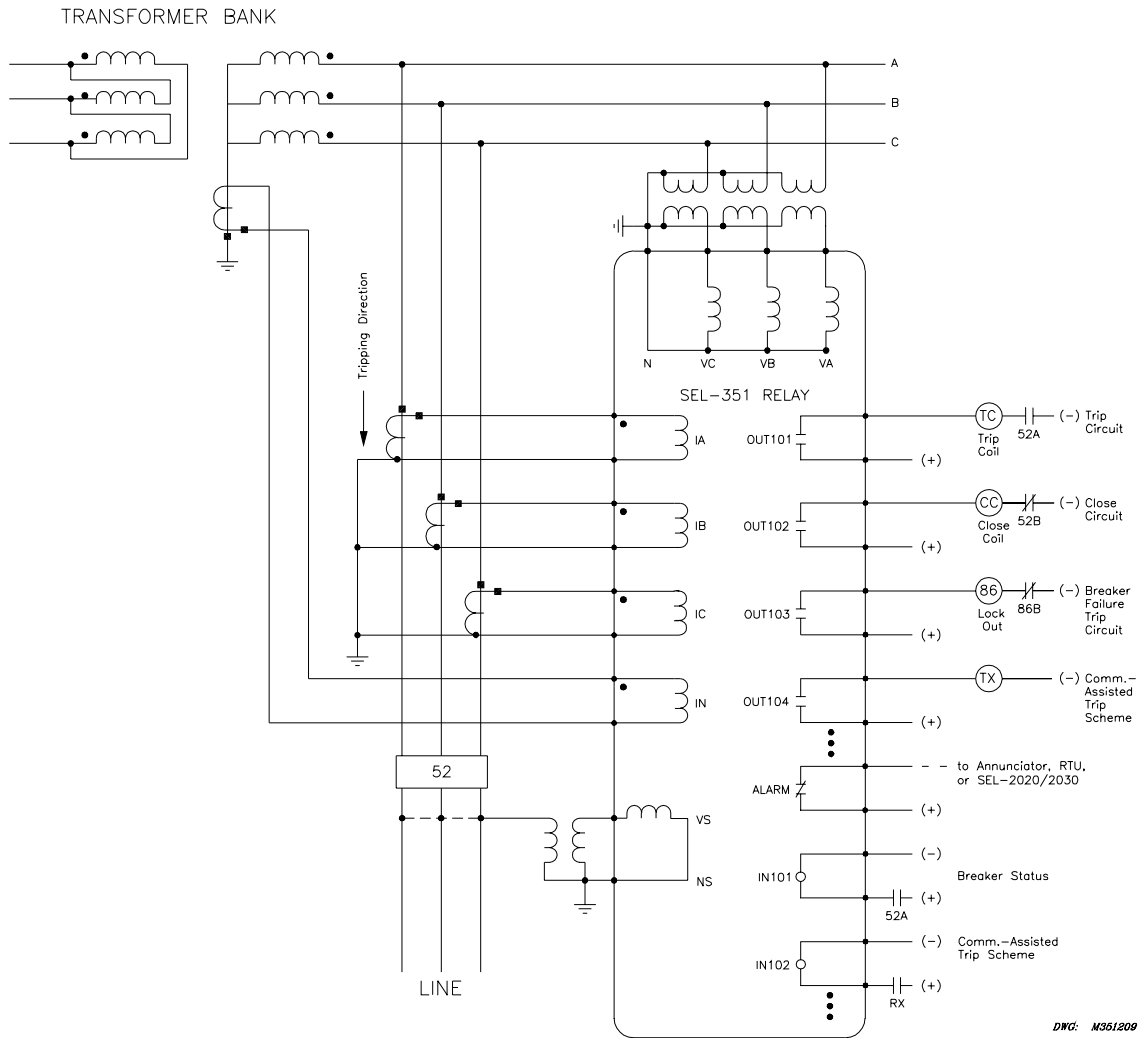
1. The fast bus trip scheme is often referred to as a reverse-interlocking or zone-interlocking scheme.
2. The voltage inputs do not need to be connected. Voltage is needed for voltage elements, synchronism check elements, frequency elements, voltage-polarized directional elements, fault location, metering (i.e., voltage, MW, MVAR), and frequency tracking. Voltage Channel VS is used only in voltage and synchronism check elements and voltage metering. In this example, the voltage across terminals VB-VC is synchronism-checked with the voltage across terminals VS-NS.
3. Current Channel IN does not need to be connected. Channel IN provides current I_N for the neutral ground overcurrent elements. Separate from Channel IN, the residual ground overcurrent elements operate from the internally derived residual current I_G ($I_G = 3I_0 = I_A + I_B + I_C$). But in this residual connection example, the neutral ground and residual ground overcurrent elements operate the same because $I_N = I_G$.
4. Although automatic reclosing is probably not needed in this example, output contact OUT102 can close the circuit breaker via initiation from various means (serial port communications, optoisolated input assertion, etc.), with desired supervision (e.g., synchronism check).

Figure 2.7: SEL-351 Relay Provides Overcurrent Protection for a Distribution Bus (Includes Fast Bus Trip Scheme)



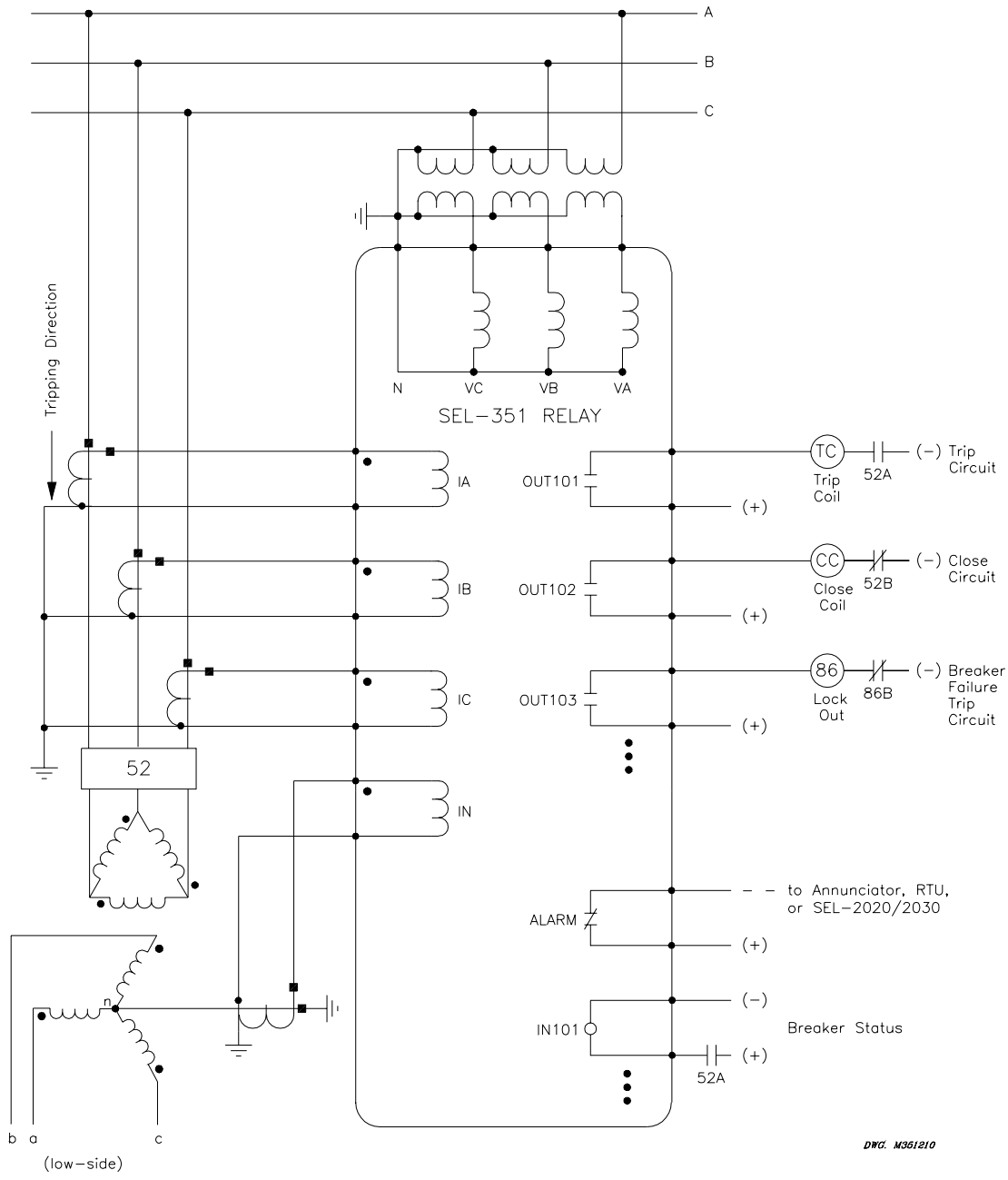
1. Voltage Channel VS does not need to be connected. It is used only in voltage and synchronism check elements and voltage metering.
2. Current Channel IN does not need to be connected. Channel IN provides current I_N for the neutral ground overcurrent elements. Separate from Channel IN, the residual ground overcurrent elements operate from the internally derived residual current I_G ($I_G = 3I_0 = I_A + I_B + I_C$). But in this residual connection example, the neutral ground and residual ground overcurrent elements operate the same because $I_N = I_G$.

Figure 2.8: SEL-351 Relay Provides Directional Overcurrent Protection and Reclosing for a Transmission Line



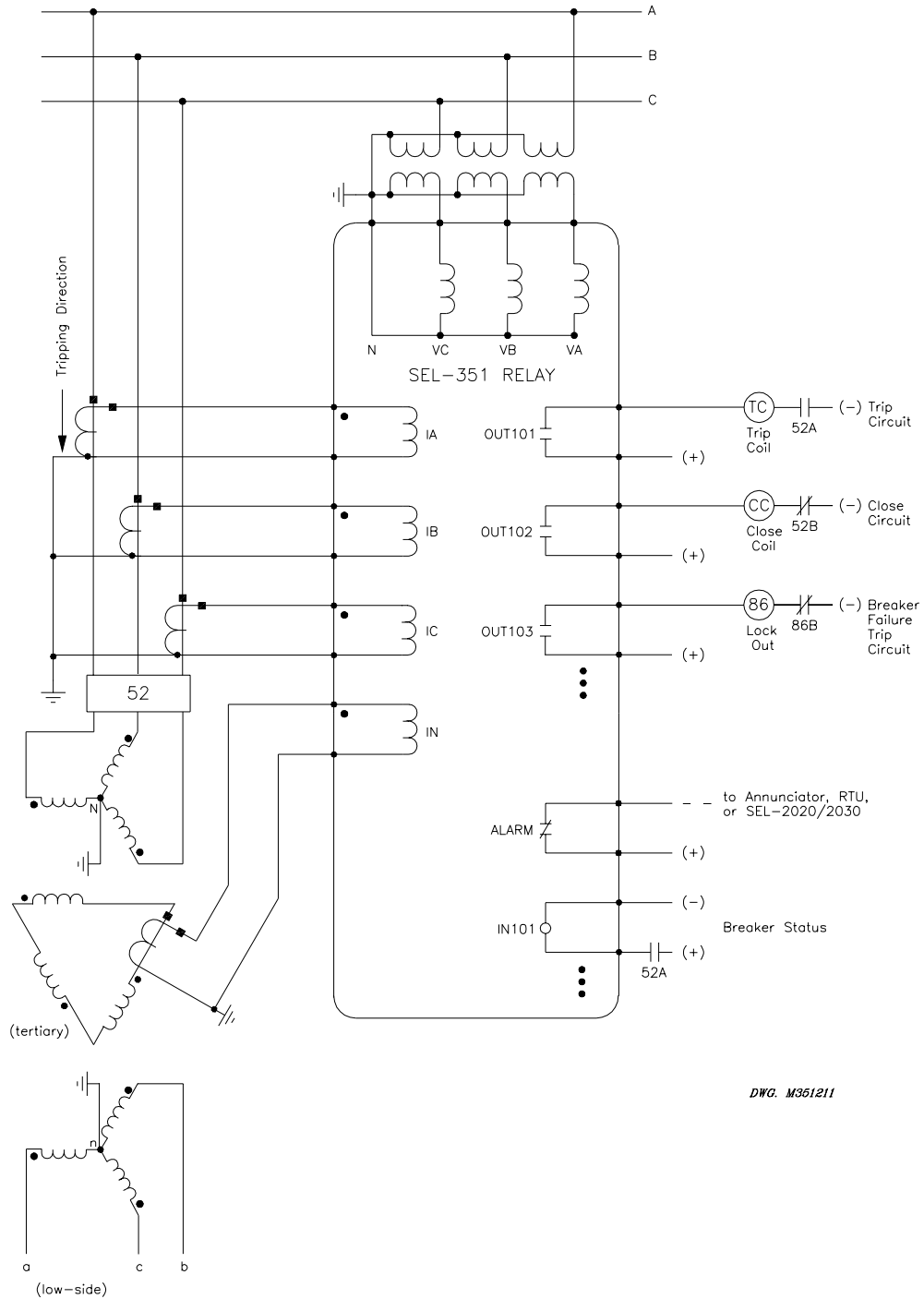
1. Voltage Channel VS does not need to be connected. It is used only in voltage and synchronism check elements and voltage metering.
2. In this example, current Channel IN provides current polarization for a directional element used to control ground overcurrent elements. Separate from Channel IN, the residual ground overcurrent elements operate from the internally derived residual current I_G ($I_G = 3I_0 = I_A + I_B + I_C$).

Figure 2.9: SEL-351 Relay Provides Directional Overcurrent Protection and Reclosing for a Transmission Line (Current-Polarization Source Connected to Channel IN)



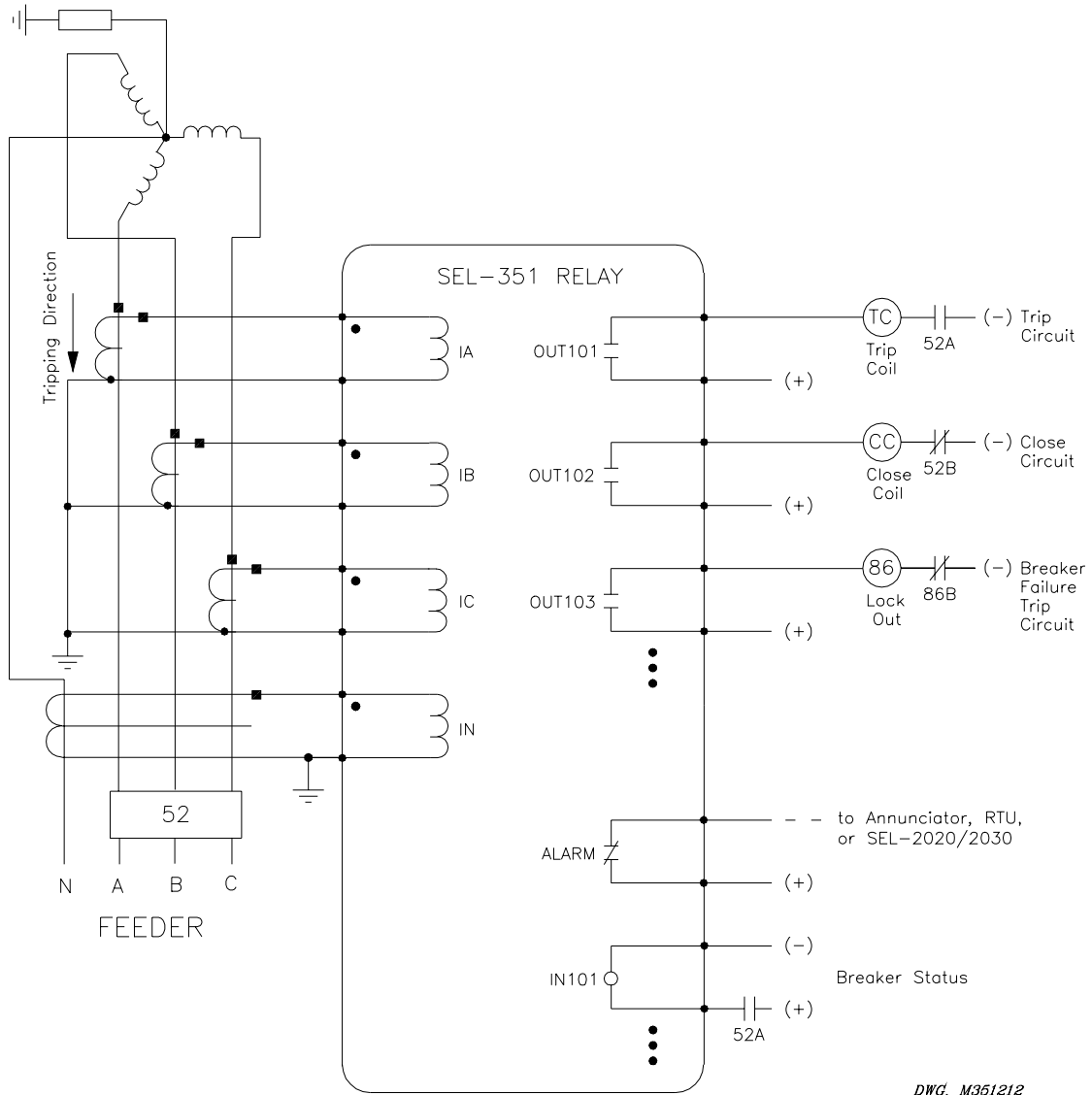
1. The voltage inputs do not need to be connected. Voltage is needed for voltage elements, synchronism check elements, frequency elements, voltage-polarized directional elements, fault location, metering (i.e., voltage, MW, MVAR), and frequency tracking.
2. Although automatic reclosing is probably not needed in this example, output contact OUT102 can close the circuit breaker via initiation from various means (serial port communications, optoisolated input assertion, etc.), with desired supervision (e.g., hot bus check).
3. For sensitive earth fault (SEF) applications, the SEL-351 Relay should be ordered with channel IN rated at 0.05 A nominal. See current input specifications in the *General Specifications* subsection in *Section 1: Introduction and Specifications*. See neutral ground overcurrent element pickup specifications in *Section 3: Overcurrent, Voltage, Synchronism Check, Frequency, and Power Elements*.

Figure 2.10: SEL-351 Relay Provides Overcurrent Protection for a Delta-Wye Transformer Bank



1. The voltage inputs do not need to be connected. Voltage is needed for voltage elements, synchronism check elements, frequency elements, voltage-polarized directional elements, fault location, metering (i.e., voltage, MW, MVAR), and frequency tracking.
2. Although automatic reclosing is probably not needed in this example, output contact OUT102 can close the circuit breaker via initiation from various means (serial port communications, optoisolated input assertion, etc.), with desired supervision (e.g., hot bus check).

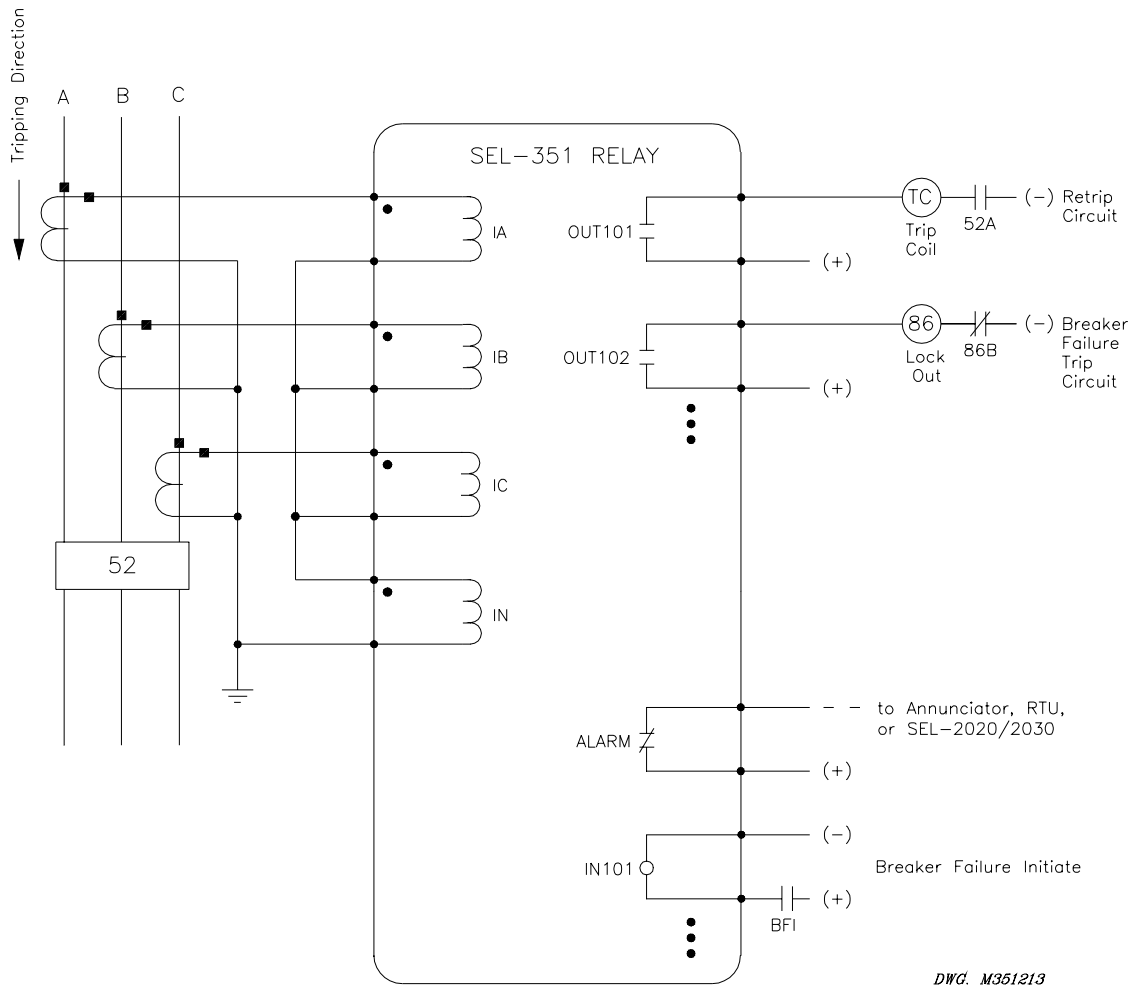
Figure 2.11: SEL-351 Relay Provides Overcurrent Protection for a Transformer Bank With a Tertiary Winding



DWG. M351212

1. A core-balance current transformer is often referred to as a zero-sequence, ground fault, or window current transformer.
2. Although automatic reclosing is probably not needed in this example, output contact OUT102 can close the circuit breaker via initiation from various means (serial port communications, optoisolated input assertion, etc.), with desired supervision.
3. For sensitive earth fault (SEF) applications, the SEL-351 Relay should be ordered with channel IN rated at 0.05 A nominal. See current input specifications in the *General Specifications* subsection in *Section 1: Introduction and Specifications*. See neutral ground overcurrent element pickup specifications in *Section 3: Overcurrent, Voltage, Synchronism Check, Frequency, and Power Elements*.

Figure 2.12: SEL-351 Relay Provides Overcurrent Protection for an Industrial Distribution Feeder (Core-Balance Current Transformer Connected TO Channel IN)



DWG. M351213

Current Channel IN does not need to be connected. Channel IN provides current I_N for the neutral ground overcurrent elements. Separate from Channel IN, the residual ground overcurrent elements operate from the internally derived residual current I_G ($I_G = 3I_0 = I_A + I_B + I_C$). But in this residual connection example, the neutral ground and residual ground overcurrent elements operate the same because $I_N = I_G$.

Figure 2.13: SEL-351 Relay Provides Dedicated Breaker Failure Protection

CIRCUIT BOARD CONNECTIONS

Accessing the Relay Circuit Boards

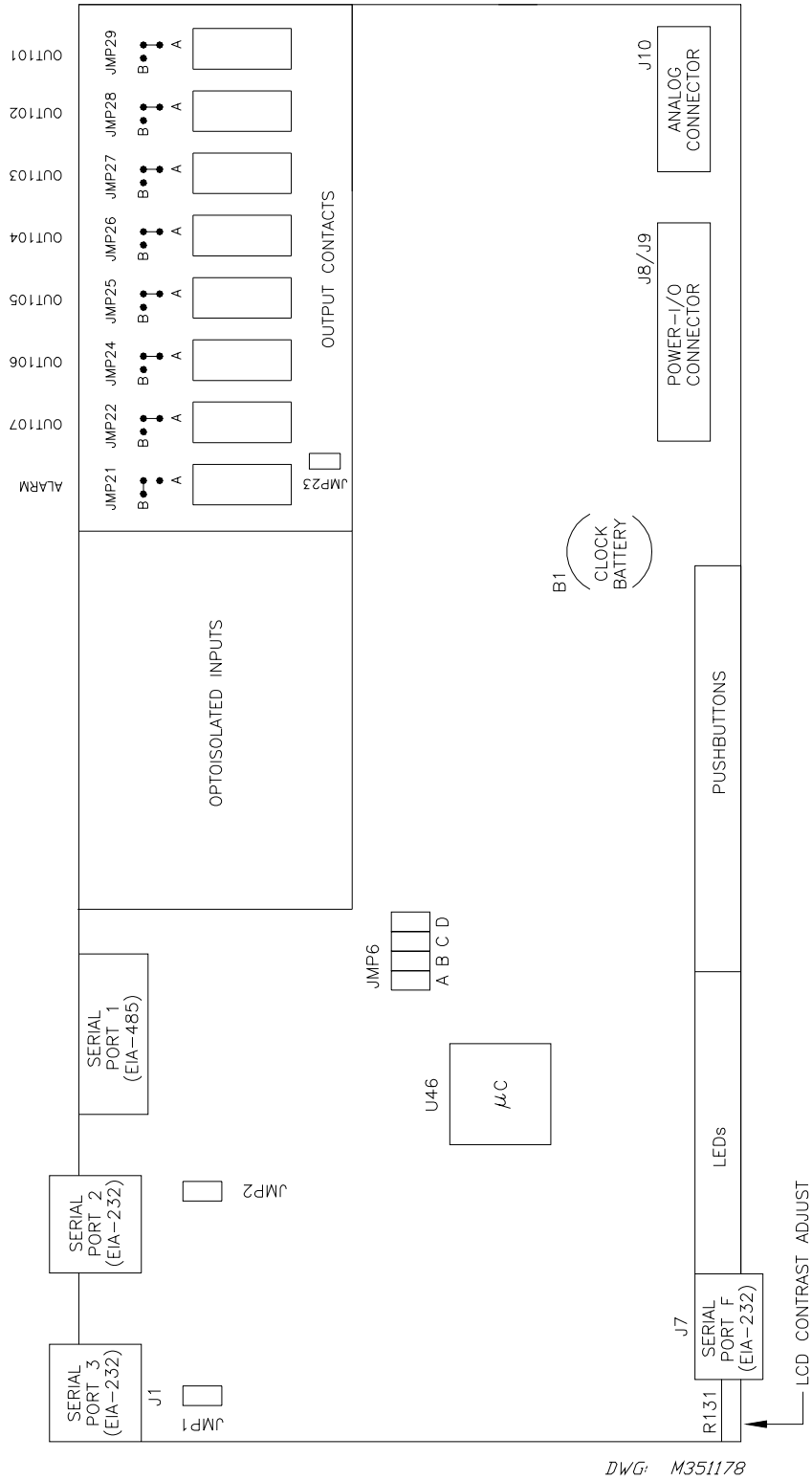
To change circuit board jumpers or replace the clock battery on the relay main board, refer to Figure 2.14 through Figure 2.16 and take the following steps:

1. Deenergize the relay. On Connectorized versions this can be easily accomplished by removing the connector at rear-panel terminals Z25 and Z26
2. Remove any cables connected to serial ports on the front and rear panels.
3. Loosen the six front-panel screws (they remain attached to the front panel), and remove the relay front panel.



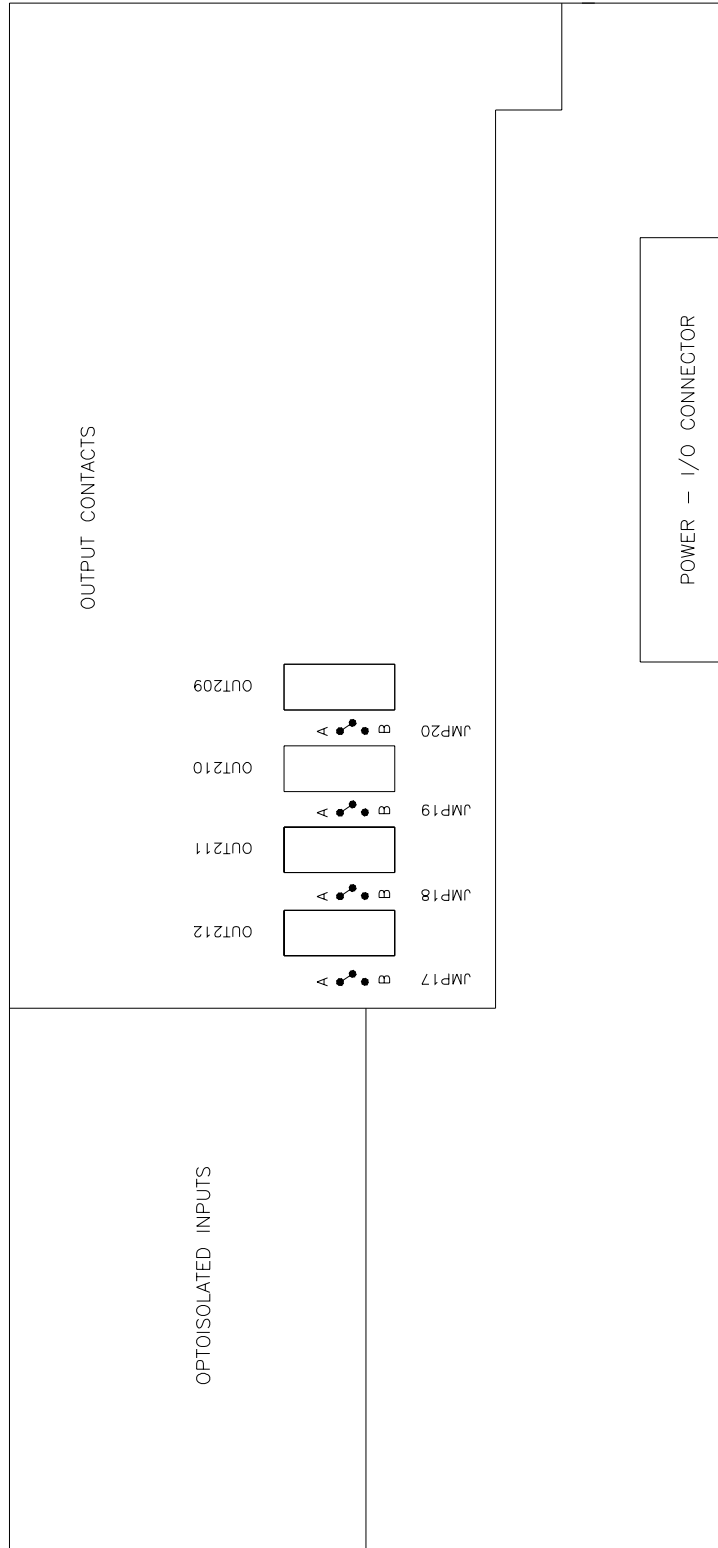
The relay contains devices sensitive to Electrostatic Discharge (ESD). When working on the relay with front or top cover removed, work surfaces and personnel must be properly grounded or equipment damage may result.

4. Each circuit board corresponds to a row of rear-panel terminal blocks or connectors and is affixed to a drawout tray. Identify which drawout tray needs to be removed. SEL-351 Relay model 0351x0 has only a main board. Models 0351x1 and 0351xY have an extra I/O board below the main board.
5. On Connectorized versions, remove the rear-panel connectors that correspond to the circuit board you wish to remove by loosening the screws on either end of each connector. Removal of the extra I/O board also requires removal of the main board (because the LCD on the main board is in the way).
6. Disconnect circuit board cables as necessary to allow the desired board and drawout tray to be removed. Removal of the extra I/O board requires removal of the main board first. Ribbon cables can be removed by pushing the extraction ears away from the connector. The 6-conductor power cable can be removed by grasping the power connector wires and pulling away from the circuit board.
7. Grasp the drawout assembly of the board and pull the assembly from the relay chassis.
8. Locate the jumper(s) or battery to be changed (refer to Figure 2.14 through Figure 2.16). Make the desired changes. Note that the output contact jumpers are soldered in place.
9. When finished, slide the drawout assembly into the relay chassis. Reconnect the cables removed in step 6. Replace the relay front-panel cover.
10. Replace any cables previously connected to serial ports.
11. Replace any rear-panel connectors removed in step 5.
12. Reenergize the relay. On Connectorized versions, replace the power connector at rear-panel terminals Z25 and Z26.



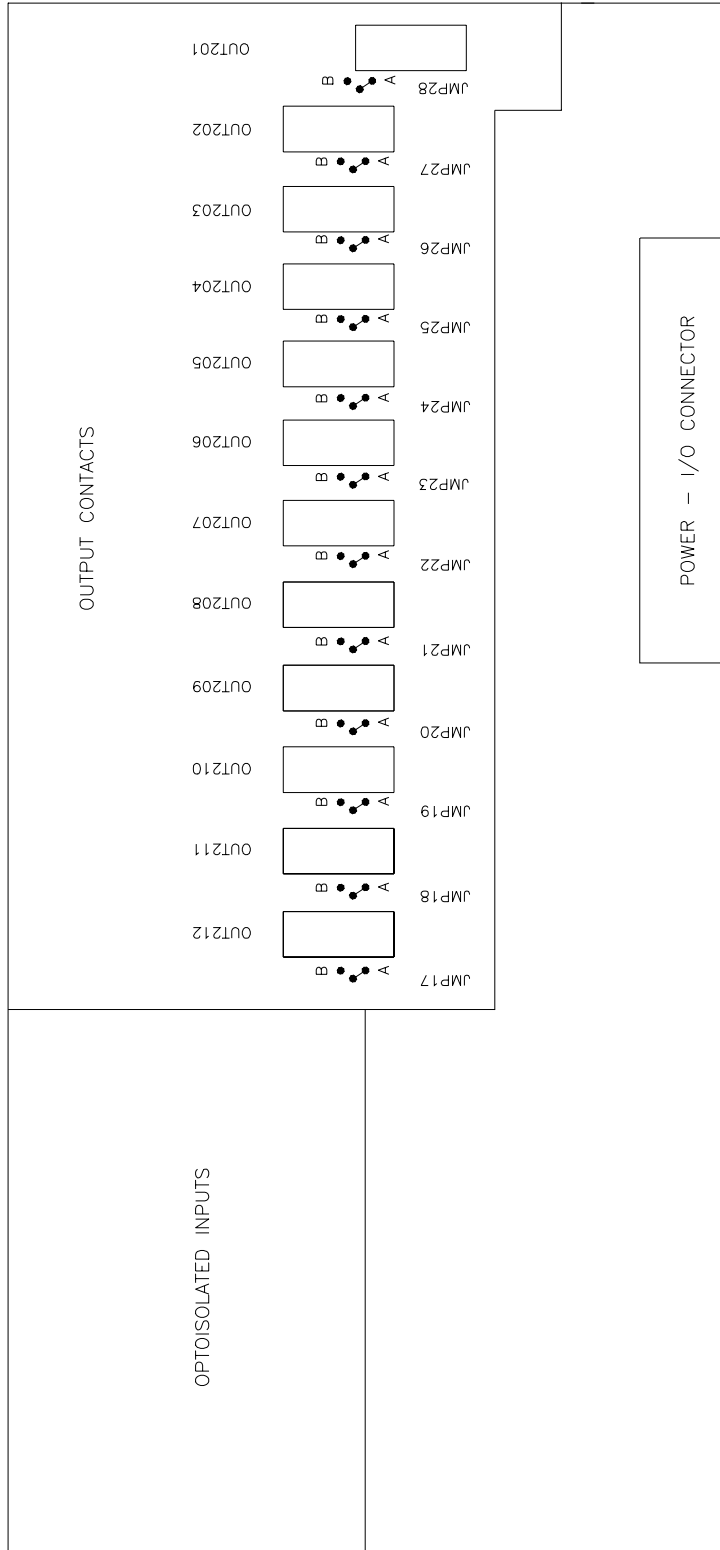
DWG: M351178

Figure 2.14: Jumper, Connector, and Major Component Locations on the SEL-351 Relay Main Board (Models 0351x0, 0351x1, and 0351xY)



DWG: M351181A

Figure 2.15: Jumper, Connector, and Major Component Locations on the SEL-351 Relay Extra I/O Board (Models 0351xY, Plug-In Connector Version)



DWG: M351181

Figure 2.16: Jumper, Connector, and Major Component Locations on the SEL-351 Relay Extra I/O Board (Model 0351x1, Screw-Terminal Block Version)

Output Contact Jumpers

Table 2.2 shows the correspondence between output contact jumpers and the output contacts they control. The referenced figures show the exact location and correspondence. With a jumper in the A position, the corresponding output contact is an “a” type output contact. An “a” type output contact is open when the output contact coil is deenergized and closed when the output contact coil is energized. With a jumper in the B position, the corresponding output contact is a “b” type output contact. A “b” type output contact is closed when the output contact coil is deenergized and open when the output contact coil is energized. These jumpers are soldered in place.

In the figures referenced in Table 2.2, note that the ALARM output contacts are “b” type output contacts and the other output contacts are all “a” type output contacts. This is how these jumpers are configured in a standard relay shipment. Refer to corresponding Figure 7.27 through Figure 7.30 for examples of output contact operation for different output contact types.

Table 2.2: Output Contact Jumpers and Corresponding Output Contacts

SEL-351 Relay Model Number	Output Contact Jumpers	Corresponding Output Contacts	Reference Figures
0351x0, 0351x1, and 0351xY	JMP21–JMP29 (but not JMP23)	ALARM–OUT101	Figure 2.14
0351xY	JMP17–JMP20	OUT212–OUT209	Figure 2.15
0351x1	JMP17–JMP28	OUT212–OUT201	Figure 2.16

“Extra Alarm” Output Contact Control Jumper

All the SEL-351 Relay models have dedicated alarm output contacts (labeled ALARM—see Figure 2.2 through Figure 2.4). Often more than one alarm output contact is needed for such applications as local or remote annunciation, backup schemes, etc. An extra alarm output contact can be had for all the SEL-351 Relay models without the addition of any external hardware.

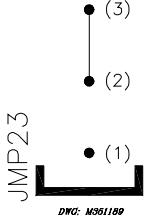
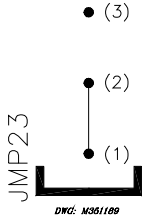
The output contact next to the dedicated ALARM output contact can be converted to operate as an “extra alarm” output contact by moving a jumper on the main board (see Table 2.3).

Table 2.3: “Extra Alarm” Output Contacts and Corresponding Controlling Jumpers

SEL-351 Relay Model Number	“Extra Alarm” Output Contact	Controlling Jumper	Reference Figures
0351x0, 0351x1, and 0351xY	OUT107	JMP23	2.14, 7.27

The position of the jumper controls the operation of the output contact next to the dedicated ALARM output contact. With the jumper in one position, the output contact operates regularly. With the jumper in the other position, the output contact is driven by the same signal that operates the dedicated ALARM output contact (see Table 2.4).

Table 2.4: Required Position of Jumper JMP23 for Desired Output Contact OUT107 Operation (Models 0351x0, 0351x1, and 0351xY)

Position	Output Contact OUT107 Operation
	<p>Regular output contact OUT107 (operated by Relay Word bit OUT107). Jumper JMP23 comes in this position in a <u>standard relay shipment</u> (see Figure 7.27).</p>
	<p>“Extra Alarm” output contact (operated by alarm logic/circuitry). Relay Word bit OUT107 does not have any effect on output contact OUT107 when jumper JMP23 is in this position (see Figure 7.27).</p>

If an output contact is operating as an “extra alarm” (driven by the same signal that operates the dedicated ALARM output contact), it will be in the opposite state of the dedicated ALARM output contact in a standard relay shipment. In a standard relay shipment, the dedicated ALARM output contact comes as a “b” type output contact and all the other output contacts (including the “extra alarm”) come as “a” type output contacts.

The output contact type for any output contact can be changed (see preceding subsection *Output Contact Jumpers*). Thus, the dedicated ALARM output contact and the “extra alarm” output contact can be configured as the same output contact type if desired (e.g., both can be configured as “b” type output contacts).

Password and Breaker Jumpers

Table 2.5: Password and Breaker Jumper Positions for Standard Relay Shipments

SEL-351 Relay Model Number	Password Jumper/Position (for standard relay shipments)	Breaker Jumper/Position (for standard relay shipments)	Reference Figures
0351x0 0351x1 0351xY	JMP6-A = OFF	JMP6-B = ON	2.14

Table 2.6: Password and Breaker Jumper Operation

Jumper Type	Jumper Position	Function
Password	ON (in place)	disable password protection ¹ for serial ports and front panel
	OFF (removed/not in place)	enable password protection ¹ for serial ports and front panel
Breaker	ON (in place)	enable serial port commands OPEN ² , CLOSE ² , and PULSE ³
	OFF (removed/not in place)	disable serial port commands OPEN ² , CLOSE ² , and PULSE ³

¹ View or set the passwords with the PASSWORD command (see *Section 10: Serial Port Communications and Commands*).

² Also controls *Fast Operate*, Breaker Control, and Open/Close commands (see *Appendix D*).

³ The OPEN, CLOSE, and PULSE commands are used primarily to assert output contacts for circuit breaker control or testing purposes (see *Section 10: Serial Port Communications and Commands*).

Note that JMP6 in Figure 2.14 has multiple jumpers A through D. Jumpers A and B are used (see Table 2.5 and Table 2.6). Since jumpers C and D are not used, the positions (ON or OFF) of jumpers C and D are of no consequence.

EIA-232 Serial Port Voltage Jumpers

The jumpers listed in Table 2.7 connect or disconnect +5 Vdc to Pin 1 on the corresponding EIA-232 serial ports. The +5 Vdc is rated at 0.5 A maximum for each port. See Table 10.2 in *Section 10: Serial Port Communications and Commands* for EIA-232 serial port pin functions.

In a standard relay shipment, the jumpers are “OFF” (removed/not in place) so that the +5 Vdc is not connected to Pin 1 on the corresponding EIA-232 serial ports. Put the jumpers “ON” (in place) so that the +5 Vdc is connected to Pin 1 on the corresponding EIA-232 serial ports.

Table 2.7: EIA-232 Serial Port Voltage Jumper Positions for Standard Relay Shipments

SEL-351 Relay Model Number	EIA-232 Serial Port 2 (rear panel)	EIA-232 Serial Port 3 (rear panel)	Reference Figures
0351x0 0351x1 0351xY	JMP2 = OFF	JMP1 = OFF	2.14

Condition of Acceptability for North American Product Safety Compliance

To meet product safety compliance for end-use applications in North American, use an external fuse rated 3 A or less in-line with the +5 Vdc source on pin 1. SEL Fiber-optic transceivers include a fuse that meets this requirement.

Clock Battery

Refer to Figure 2.14 for clock battery location (front of main board). A lithium battery powers the relay clock (date and time) if the external dc source is lost or removed. The battery is a 3 V lithium coin cell. At room temperature (25°C), the battery will nominally operate for 10 years at rated load.

If the dc source is lost or disconnected, the battery powers the clock. When the relay is powered from an external source, the battery only experiences a low self-discharge rate. Thus, battery life can extend well beyond the nominal 10 years because the battery rarely has to discharge after the relay is installed. The battery cannot be recharged.

If the relay does not maintain the date and time after power loss, replace the battery. Follow the instructions in the previous subsection *Accessing the Relay Circuit Boards* to remove the relay main board.



There is danger of explosion if the batter is incorrectly replaced. Replace only with Ray-O-Vac[®] no. BR2335 or equivalent recommended by manufacturer. Dispose of used batteries according to the manufacturer's instructions.

Remove the battery from beneath the clip and install a new one. The positive side (+) of the battery faces up. Reassemble the relay as described in *Accessing the Relay Circuit Boards*. Set the relay date and time via serial communications port or front panel (see *Section 10: Serial Port Communications and Commands* or *Section 11: Front-Panel Interface*, respectively).

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SECTION 3: OVERCURRENT, VOLTAGE, SYNCHRONISM CHECK, FREQUENCY, AND POWER ELEMENTS

INSTANTANEOUS/DEFINITE-TIME OVERCURRENT ELEMENTS

Phase Instantaneous/Definite-Time Overcurrent Elements

Four levels of phase instantaneous/definite-time overcurrent elements are available. Two additional levels of phase instantaneous overcurrent elements (Levels 5 and 6) are also available. The different levels are enabled with the E50P enable setting, as shown in Figure 3.1, Figure 3.2, and Figure 3.3.

Level 2 element 67P2S in Figure 3.3 is used in directional comparison blocking schemes (see *Directional Comparison Blocking (DCB) Logic* in *Section 5: Trip and Target Logic*). All the other phase instantaneous/definite-time overcurrent elements are available for use in any tripping or control scheme.

Settings Ranges

Setting range for pickup settings 50P1P through 50P6P:

0.25–100.00 A secondary	(5 A nominal phase current inputs, IA, IB, IC)
0.05–20.00 A secondary	(1 A nominal phase current inputs, IA, IB, IC)

Setting range for definite-time settings 67P1D through 67P4D:

0.00–16000.00 cycles, in 0.25-cycle steps

Setting range for definite-time setting 67P2SD (used in the DCB logic):

0.00–60.00 cycles, in 0.25-cycle steps

Accuracy

Pickup: ± 0.05 A secondary and $\pm 3\%$ of setting (5 A nominal phase current inputs, IA, IB, IC)
 ± 0.01 A secondary and $\pm 3\%$ of setting (1 A nominal phase current inputs, IA, IB, IC)

Timer: ± 0.25 cycles and $\pm 0.1\%$ of setting

Transient Overreach: $\pm 5\%$ of setting

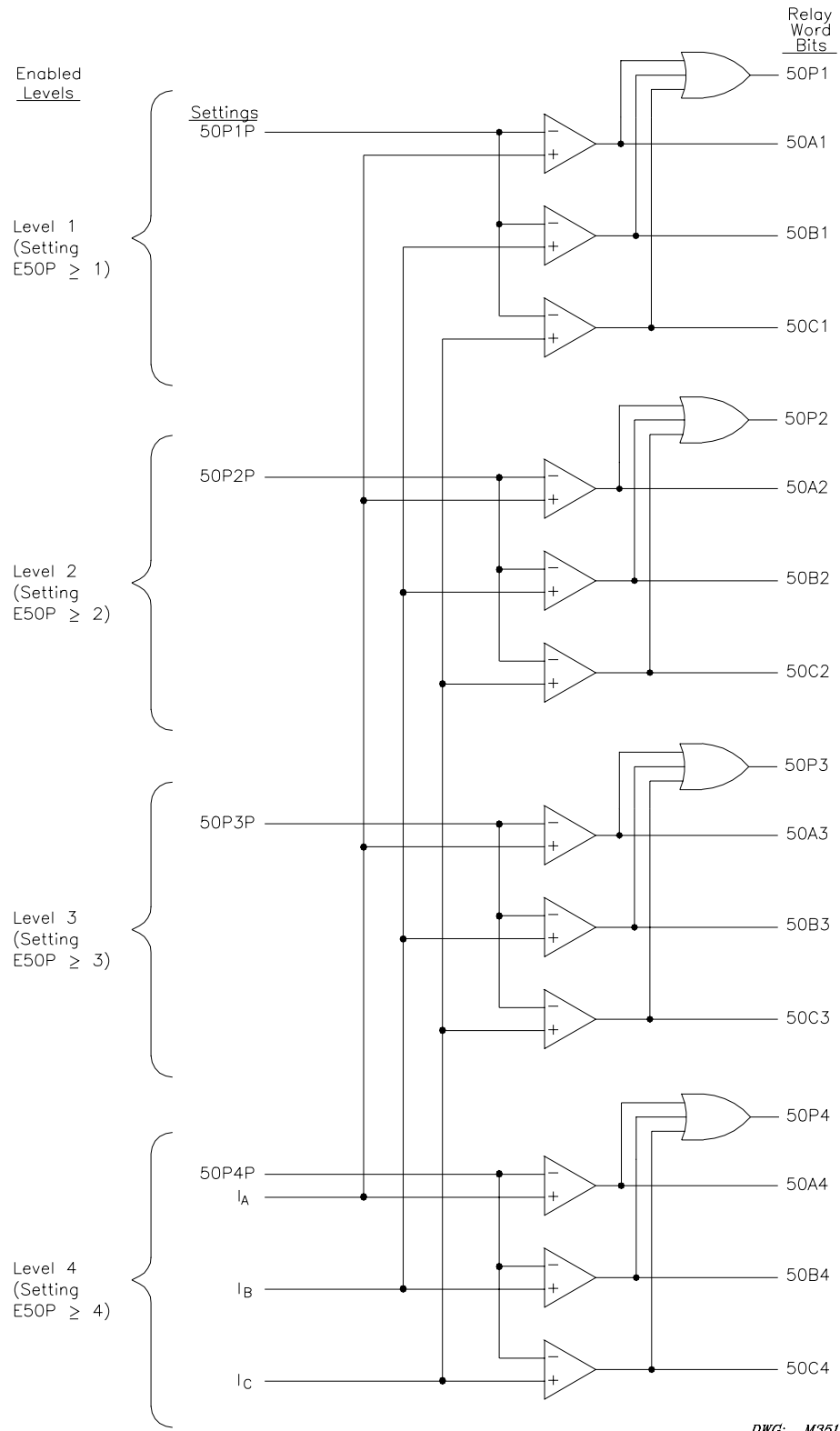


Figure 3.1: Levels 1 through 4 Phase Instantaneous Overcurrent Elements

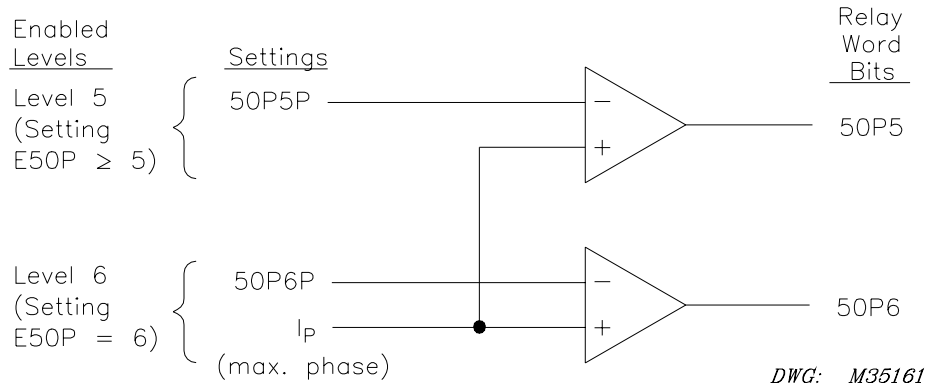


Figure 3.2: Levels 5 through 6 Phase Instantaneous Overcurrent Elements

Pickup Operation

The phase instantaneous/definite-time overcurrent element logic begins with Figure 3.1 and Figure 3.2. The pickup settings for each level (50P1P through 50P6P) are compared to the magnitudes of the individual phase currents I_A , I_B , and I_C . The logic outputs in Figure 3.1 and Figure 3.2 are Relay Word bits and operate as follows (Level 1 example shown):

- 50A1 = 1 (logical 1), if $I_A >$ pickup setting 50P1P
= 0 (logical 0), if $I_A \leq$ pickup setting 50P1P
- 50B1 = 1 (logical 1), if $I_B >$ pickup setting 50P1P
= 0 (logical 0), if $I_B \leq$ pickup setting 50P1P
- 50C1 = 1 (logical 1), if $I_C >$ pickup setting 50P1P
= 0 (logical 0), if $I_C \leq$ pickup setting 50P1P
- 50P1 = 1 (logical 1), if at least one of the Relay Word bits 50A1, 50B1, or 50C1 is asserted (e.g., 50B1 = 1)
= 0 (logical 0), if all three Relay Word bits 50A1, 50B1, and 50C1 are deasserted (50A1 = 0, 50B1 = 0, and 50C1 = 0)

Note that single-phase overcurrent elements are not available in Levels 5 and 6 (see Figure 3.2).

Ideally, set $50P1P > 50P2P > 50P3P > 50P4P$ so that instantaneous overcurrent elements 67P1 through 67P4 will display in an organized fashion in event reports (see Figure 3.3 and Table 12.3).

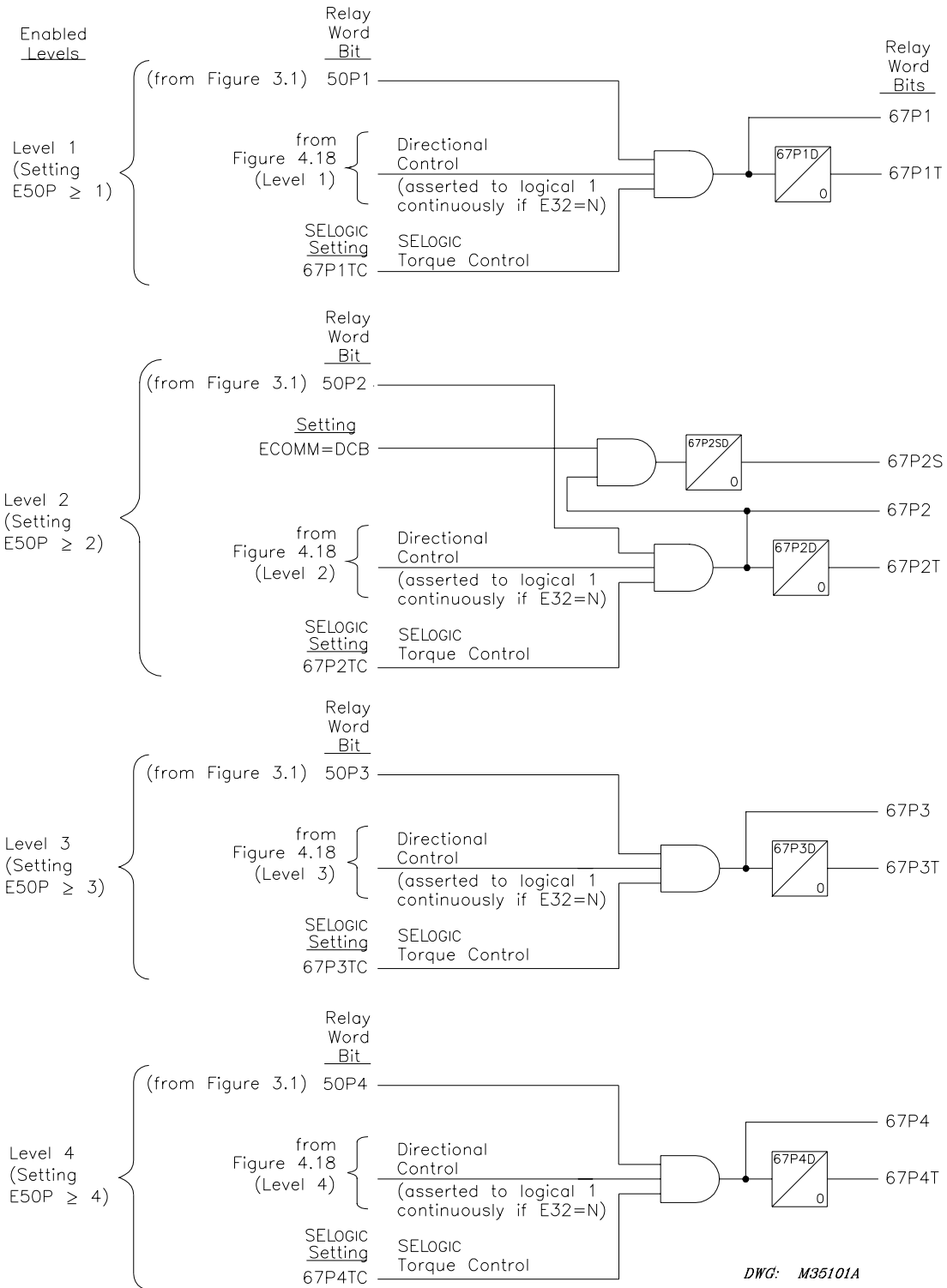


Figure 3.3: Levels 1 through 4 Phase Instantaneous/Definite-Time Overcurrent Elements (With Directional Control Option)

DIRECTIONAL CONTROL OPTION

The phase instantaneous overcurrent element Relay Word bit outputs in Figure 3.1 (50P1, 50P2, 50P3, and 50P4) are inputs into the phase instantaneous/definite-time overcurrent element logic in Figure 3.3.

Levels 1 through 4 in Figure 3.3 have corresponding directional control options. See Figure 4.18 in *Section 4: Loss-of-Potential, Load Encroachment, and Directional Element Logic* for more information on this optional directional control. If the directional control enable setting E32 is set:

$$E32 = N$$

then directional control is defeated, and the directional control inputs into all four phase instantaneous/definite-time overcurrent element levels in Figure 3.3 are asserted to logical 1 continuously. Then only the corresponding SELOGIC[®] control equation torque control settings have to be considered in the control of the phase instantaneous/definite-time overcurrent elements.

For example, consider the Level 1 phase instantaneous/definite-time overcurrent elements 67P1/67P1T in Figure 3.3. If the directional control enable setting E32 is set:

$$E32 = N$$

then the directional control input from Figure 4.18 (Level 1) is asserted to logical 1 continuously. Then only the corresponding SELOGIC control equation torque control setting 61P1TC has to be considered in the control of the phase instantaneous/definite-time overcurrent elements 67P1/67P1T.

SELOGIC control equation torque control settings are discussed next.

Torque Control

Levels 1 through 4 in Figure 3.3 have corresponding SELOGIC control equation torque control settings 67P1TC through 67P4TC. SELOGIC control equation torque control settings cannot be set directly to logical 0. The following are torque control setting examples for Level 1 phase instantaneous/definite-time overcurrent elements 67P1/67P1T.

67P1TC = 1 Setting 67P1TC set directly to logical 1:

Then only the corresponding directional control input from Figure 4.18 has to be considered in the control of phase instantaneous/definite-time overcurrent elements 67P1/67P1T.

If directional control enable setting E32 =N, then phase instantaneous/definite-time overcurrent elements 67P1/67P1T are enabled and nondirectional.

Note: All overcurrent element SELOGIC control equation torque control settings are set directly to logical 1 (e.g., 67P1TC = 1) for the factory default settings. See *SHO Command (Show/View Settings)* in *Section 10: Serial Port Communications and Commands* for a list of the factory default settings.

67P1TC = IN105 Input IN105 deasserted (67P1TC = IN105 = logical 0):

Then phase instantaneous/definite-time overcurrent elements 67P1/67P1T are defeated and nonoperational, regardless of any other setting.

Input IN105 asserted (67P1TC = IN105 = logical 1):

Then only the corresponding directional control input from Figure 4.18 has to be considered in the control of phase instantaneous/definite-time overcurrent elements 67P1/67P1T.

If directional control enable setting E32 = N, then phase instantaneous/definite-time overcurrent elements 67P1/67P1T are enabled and nondirectional.

Sometimes SELOGIC control equation torque control settings are set to provide directional control. See *Directional Control Provided by Torque Control Settings* at the end of *Section 4: Loss-of-Potential, Load Encroachment, and Directional Element Logic*.

Combined Single-Phase Instantaneous Overcurrent Elements

The single-phase instantaneous overcurrent element Relay Word bit outputs in Figure 3.1 are combined together in Figure 3.4 on a per phase basis, producing Relay Word bit outputs 50A, 50B, and 50C.

Relay Word bits 50A, 50B, and 50C can be used to indicate the presence or absence of current in a particular phase.

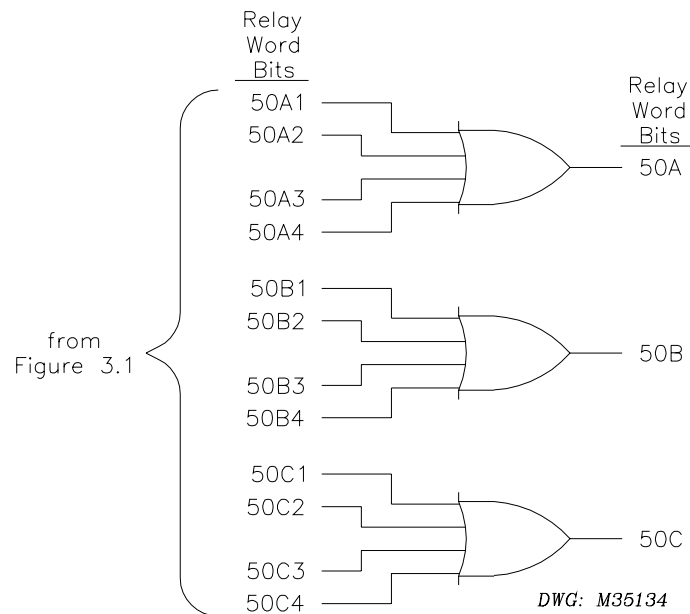


Figure 3.4: Combined Single-Phase Instantaneous Overcurrent Elements

Pickup and Reset Time Curves

Figure 3.5 and Figure 3.6 show pickup and reset time curves applicable to all nondirectional instantaneous overcurrent elements in the SEL-351 Relay (60 Hz or 50 Hz relays). These times do not include output contact operating time and, thus, are accurate for determining element operation time for use in internal SELOGIC control equations. Output contact pickup/dropout time is 4 ms (0.25 cycle for a 60 Hz relay; 0.20 cycle for a 50 Hz relay).

If instantaneous overcurrent elements are made directional, the pickup time curve in Figure 3.5 is adjusted as follows:

multiples of pickup setting ≤ 4 : add 0.25 cycle

multiples of pickup setting > 4 : add 0.50 cycle

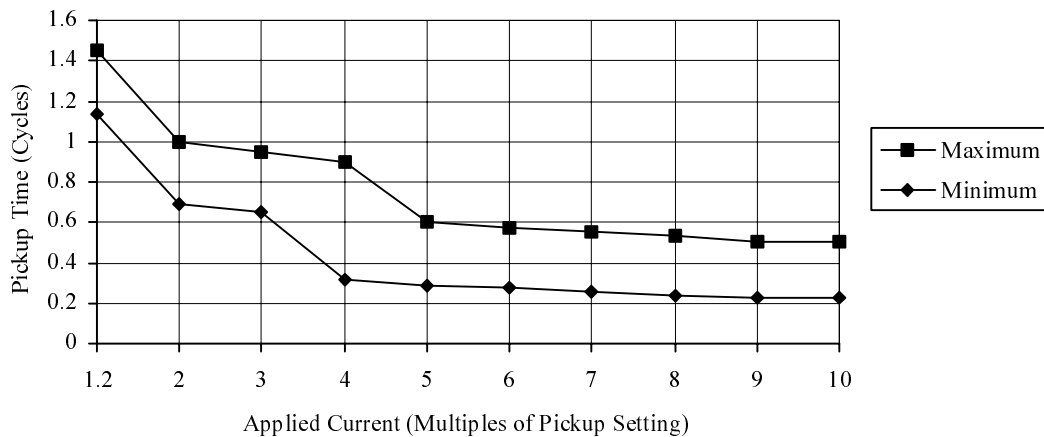


Figure 3.5: SEL-351 Relay Nondirectional Instantaneous Overcurrent Element Pickup Time Curve

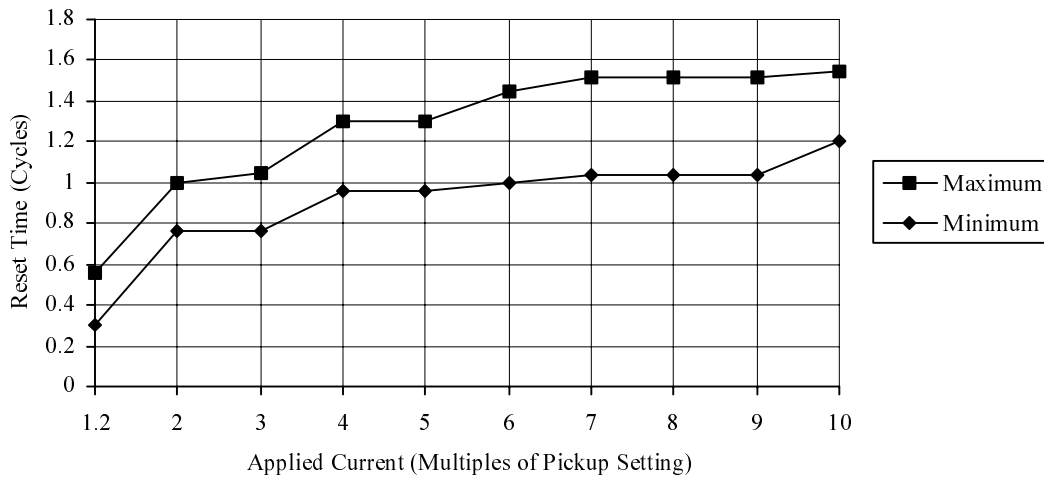


Figure 3.6: SEL-351 Relay Nondirectional Instantaneous Overcurrent Element Reset Time Curve

Phase-to-Phase Instantaneous Overcurrent Elements

Four levels of phase-to-phase instantaneous overcurrent elements are available. The different levels are enabled with the E50P enable setting, as shown in Figure 3.7.

Setting Range

Setting range for pickup settings 50PP1P through 50PP4P:

1.00–170.00 A secondary	(5 A nominal phase current inputs, IA, IB, IC)
0.20–34.00 A secondary	(1 A nominal phase current inputs, IA, IB, IC)

Accuracy

Pickup: ± 0.05 A secondary and $\pm 3\%$ of setting (5 A nominal phase current inputs, IA, IB, IC)
 ± 0.01 A secondary and $\pm 3\%$ of setting (1 A nominal phase current inputs, IA, IB, IC)

Pickup Operation

The pickup settings for each level (50PP1P through 50PP4P) are compared to the magnitudes of the individual phase-to-phase difference currents I_{AB} , I_{BC} , and I_{CA} . The logic outputs in Figure 3.7 are the following Relay Word bits (Level 1 example shown):

$$\begin{aligned} 50AB1 &= 1 \text{ (logical 1), if } I_{AB} > \text{ pickup setting 50PP1P} \\ &= 0 \text{ (logical 0), if } I_{AB} \leq \text{ pickup setting 50PP1P} \\ 50BC1 &= 1 \text{ (logical 1), if } I_{BC} > \text{ pickup setting 50PP1P} \\ &= 0 \text{ (logical 0), if } I_{BC} \leq \text{ pickup setting 50PP1P} \\ 50CA1 &= 1 \text{ (logical 1), if } I_{CA} > \text{ pickup setting 50PP1P} \\ &= 0 \text{ (logical 0), if } I_{CA} \leq \text{ pickup setting 50PP1P} \end{aligned}$$

Pickup and Reset Time Curves

See Figure 3.5 and Figure 3.6.

Neutral Ground Instantaneous/Definite-Time Overcurrent Elements

Four levels of neutral ground instantaneous/definite-time overcurrent elements are available. Two additional levels of neutral ground instantaneous overcurrent elements (Levels 5 and 6) are also available. The different levels are enabled with the E50N enable setting, as shown in Figure 3.8 and Figure 3.9.

Level 2 element 67N2S in Figure 3.8 is used in directional comparison blocking schemes (see *Directional Comparison Blocking (DCB) Logic* in *Section 5: Trip and Target Logic*). All the other neutral ground instantaneous/definite-time overcurrent elements are available for use in any tripping or control scheme.

To understand the operation of Figure 3.8 and Figure 3.9, follow the explanation given for Figure 3.1, Figure 3.2, and Figure 3.3 in the preceding *Phase Instantaneous/Definite-Time Overcurrent Elements* subsection, substituting current I_N (channel IN current) for phase currents and substituting like settings and Relay Word bits.

For sensitive earth fault (SEF) applications, the SEL-351 Relay should be ordered with channel IN rated at 0.05 A nominal. For this channel IN rating, the increased pickup sensitivity of the neutral ground overcurrent elements is noted in the following setting ranges.

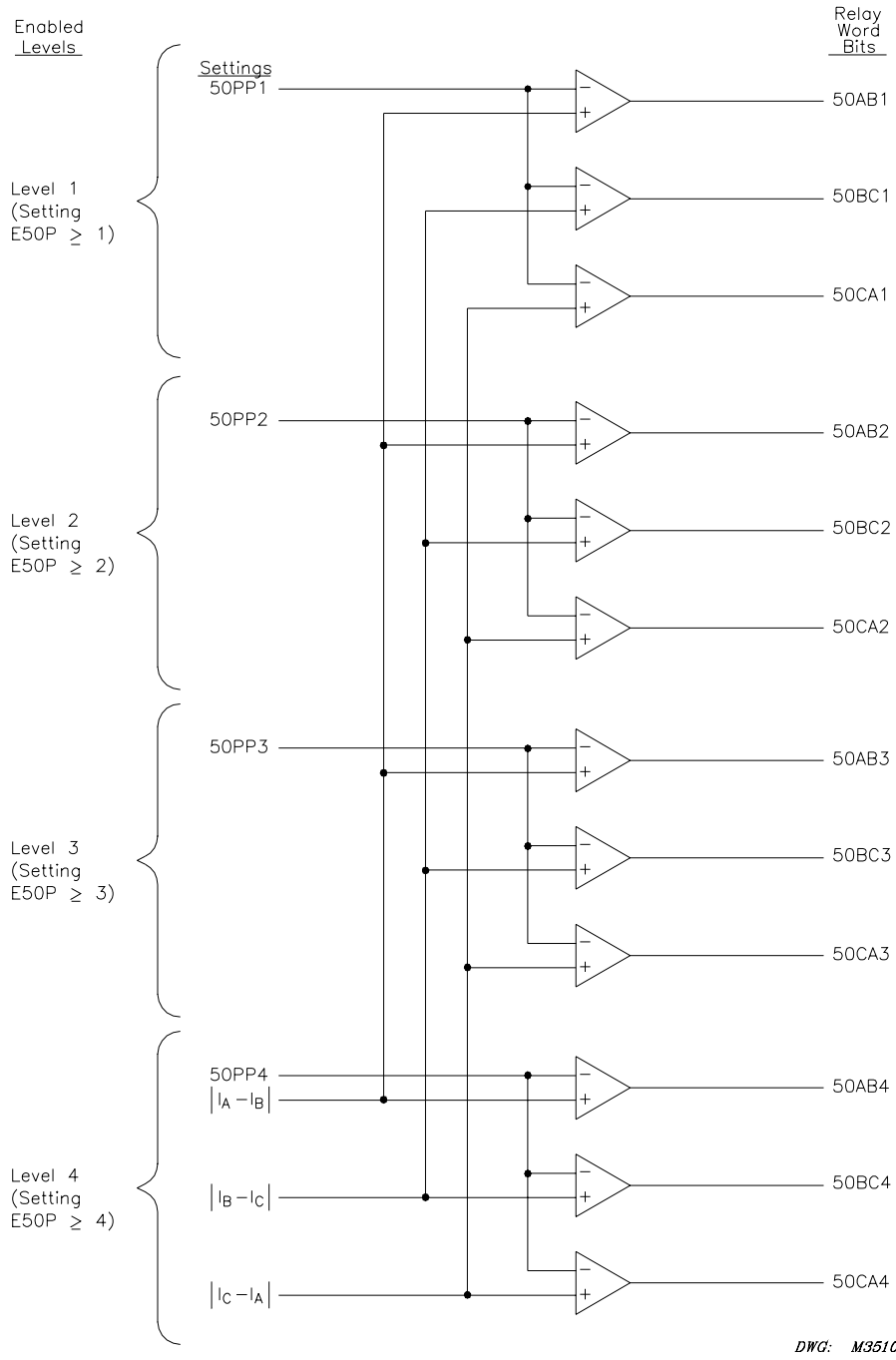


Figure 3.7: Levels 1 Through 4 Phase-to-Phase Instantaneous Overcurrent Elements

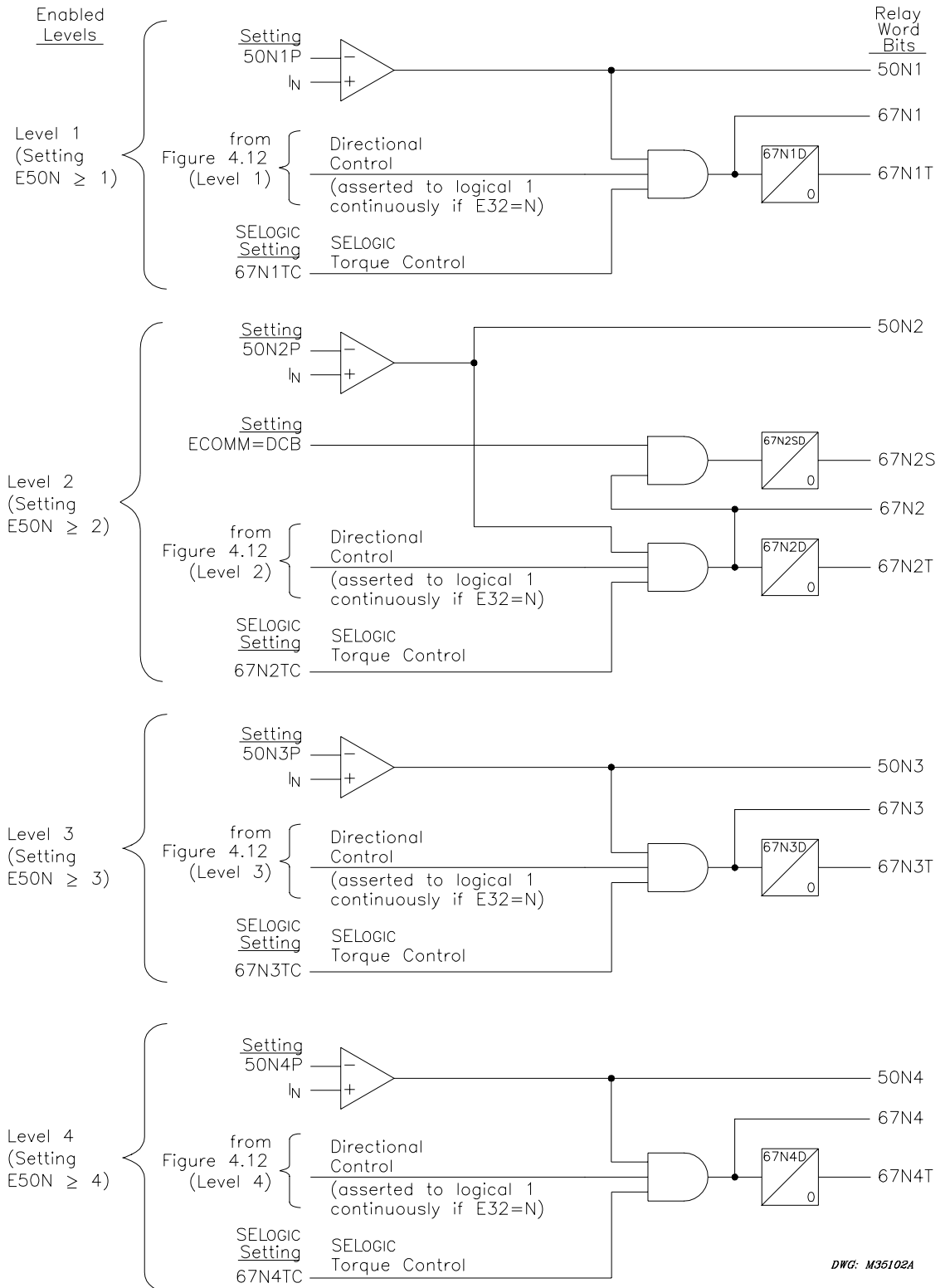


Figure 3.8: Levels 1 Through 4 Neutral Ground Instantaneous/Definite-Time Overcurrent Elements (With Directional Control Option)

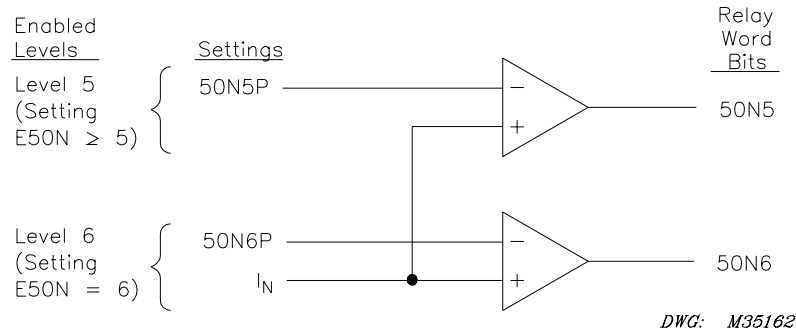


Figure 3.9: Levels 5 Through 6 Neutral Ground Instantaneous Overcurrent Elements

Settings Ranges

Setting range for pickup settings 50N1P through 50N6P:

0.250–100.000 A secondary	(5 A nominal channel IN current input)
0.050–20.000 A secondary	(1 A nominal channel IN current input)
0.005–1.500 A secondary	(0.05 A nominal channel IN current input)

Setting range for definite-time settings 67N1D through 67N4D:

0.00–16000.00 cycles, in 0.25-cycle steps

Setting range for definite-time setting 67N2SD (used in DCB logic):

0.00–60.00 cycles, in 0.25-cycle steps

Note: If channel IN is rated 0.05 A nominal, then there is an additional 2-cycle time delay on all the neutral ground instantaneous (50N1–50N6, 67N1–67N6) and definite-time (67N1T–67N4T) elements. Any time delay provided by the definite-time settings (67N1D–67N4D) is in addition to this 2-cycle time delay.

Accuracy

Pickup:	±0.05 A secondary and ±3% of setting (5 A nominal channel IN current input)
	±0.01 A secondary and ±3% of setting (1 A nominal channel IN current input)
	±1 mA secondary and ±5% of setting (0.05 A nominal channel IN current input)
Timer:	±0.25 cycles and ±0.1% of setting
Transient Overreach:	±5% of setting

Pickup and Reset Time Curves

See Figure 3.5 and Figure 3.6.

Residual Ground Instantaneous/Definite-Time Overcurrent Elements

Four levels of residual ground instantaneous/definite-time overcurrent elements are available. Two additional levels of residual ground instantaneous overcurrent elements (Levels 5 and 6) are also available. The different levels are enabled with the E50G enable setting, as shown in Figure 3.10 and Figure 3.11.

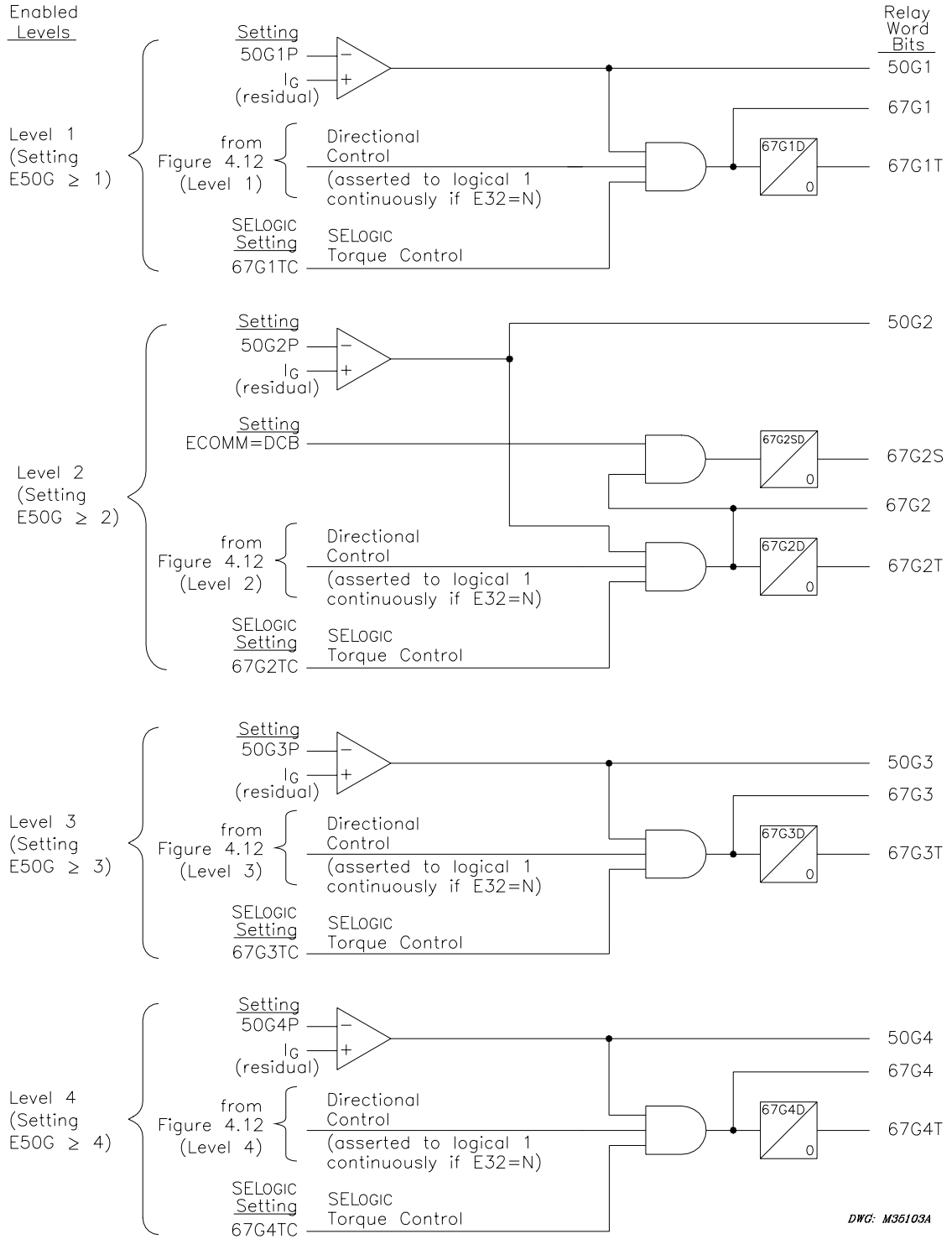


Figure 3.10: Levels 1 Through 4 Residual Ground Instantaneous/Definite-Time Overcurrent Elements (With Directional Control Option)

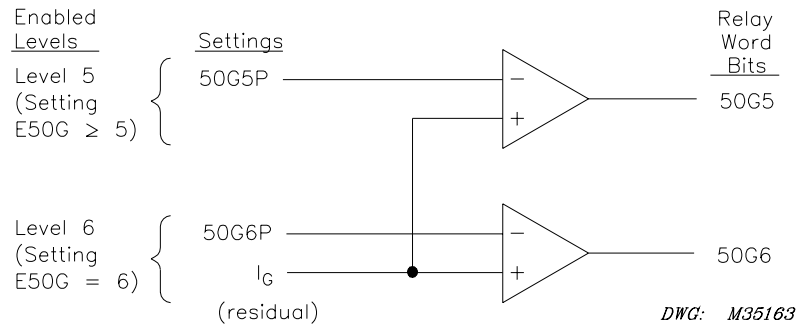


Figure 3.11: Levels 5 Through 6 Residual Ground Instantaneous Overcurrent Elements

Level 2 element 67G2S in Figure 3.10 is used in directional comparison blocking schemes (see **Directional Comparison Blocking (DCB) Logic** in **Section 5: Trip and Target Logic**). All the other residual ground instantaneous/definite-time overcurrent elements are available for use in any tripping or control scheme.

To understand the operation of Figure 3.10 and Figure 3.11, follow the explanation given for Figure 3.1, Figure 3.2, and Figure 3.3 in the preceding **Phase Instantaneous/Definite-Time Overcurrent Elements** subsection, substituting residual ground current I_G ($I_G = 3I_0 = I_A + I_B + I_C$) for phase currents and substituting like settings and Relay Word bits.

Settings Ranges

Setting range for pickup settings 50G1P through 50G6P:

0.25–100.00 A secondary	(5 A nominal phase current inputs, IA, IB, IC)
0.05–20.00 A secondary	(1 A nominal phase current inputs, IA, IB, IC)

Setting range for definite-time settings 67G1D through 67G4D:

0.00–16000.00 cycles, in 0.25-cycle steps

Setting range for definite-time setting 67G2SD (used in DCB logic):

0.00–60.00 cycles, in 0.25-cycle steps

Accuracy

Pickup: ± 0.05 A secondary and $\pm 3\%$ of setting (5 A nominal phase current inputs, IA, IB, IC)
 ± 0.01 A secondary and $\pm 3\%$ of setting (1 A nominal phase current inputs, IA, IB, IC)

Timer: ± 0.25 cycles and $\pm 0.1\%$ of setting

Transient Overreach: $\pm 5\%$ of setting

Pickup and Reset Time Curves

See Figure 3.5 and Figure 3.6.

Negative-Sequence Instantaneous/Definite-Time Overcurrent Elements

IMPORTANT: See *Appendix F* for information on setting negative-sequence overcurrent elements.

Four levels of negative-sequence instantaneous/definite-time overcurrent elements are available. Two additional levels of negative-sequence instantaneous overcurrent elements (Levels 5 and 6) are also available. The different levels are enabled with the E50Q enable setting, as shown in Figure 3.12 and Figure 3.13.

Level 2 element 67Q2S in Figure 3.12 is used in directional comparison blocking schemes (see *Directional Comparison Blocking (DCB) Logic* in *Section 5: Trip and Target Logic*). All the other negative-sequence instantaneous/definite-time overcurrent elements are available for use in any tripping or control scheme.

To understand the operation of Figure 3.12 and Figure 3.13, follow the explanation given for Figure 3.1, Figure 3.2, and Figure 3.3 in the preceding *Phase Instantaneous/Definite-Time Overcurrent Elements* subsection, substituting negative-sequence current $3I_2$ [$3I_2 = I_A + a^2 \cdot I_B + a \cdot I_C$ (ABC rotation), $3I_2 = I_A + a^2 \cdot I_C + a \cdot I_B$ (ACB rotation), where $a = 1 \angle 120^\circ$ and $a^2 = 1 \angle -120^\circ$] for phase currents and substituting like settings and Relay Word bits.

Settings Ranges

Setting range for pickup settings 50Q1P through 50Q6P:

0.25–100.00 A secondary	(5 A nominal phase current inputs, IA, IB, IC)
0.05–20.00 A secondary	(1 A nominal phase current inputs, IA, IB, IC)

Setting range for definite-time settings 67Q1D through 67Q4D:

0.00–16000.00 cycles, in 0.25-cycle steps

Setting range for definite-time setting 67Q2SD (used in DCB logic):

0.00–60.00 cycles, in 0.25-cycle steps

Accuracy

Pickup: ± 0.05 A secondary and $\pm 3\%$ of setting (5 A nominal phase current inputs, IA, IB, IC)
 ± 0.01 A secondary and $\pm 3\%$ of setting (1 A nominal phase current inputs, IA, IB, IC)

Timer: ± 0.25 cycles and $\pm 0.1\%$ of setting

Transient Overreach: $\pm 5\%$ of setting

Pickup and Reset Time Curves

See Figure 3.5 and Figure 3.6.

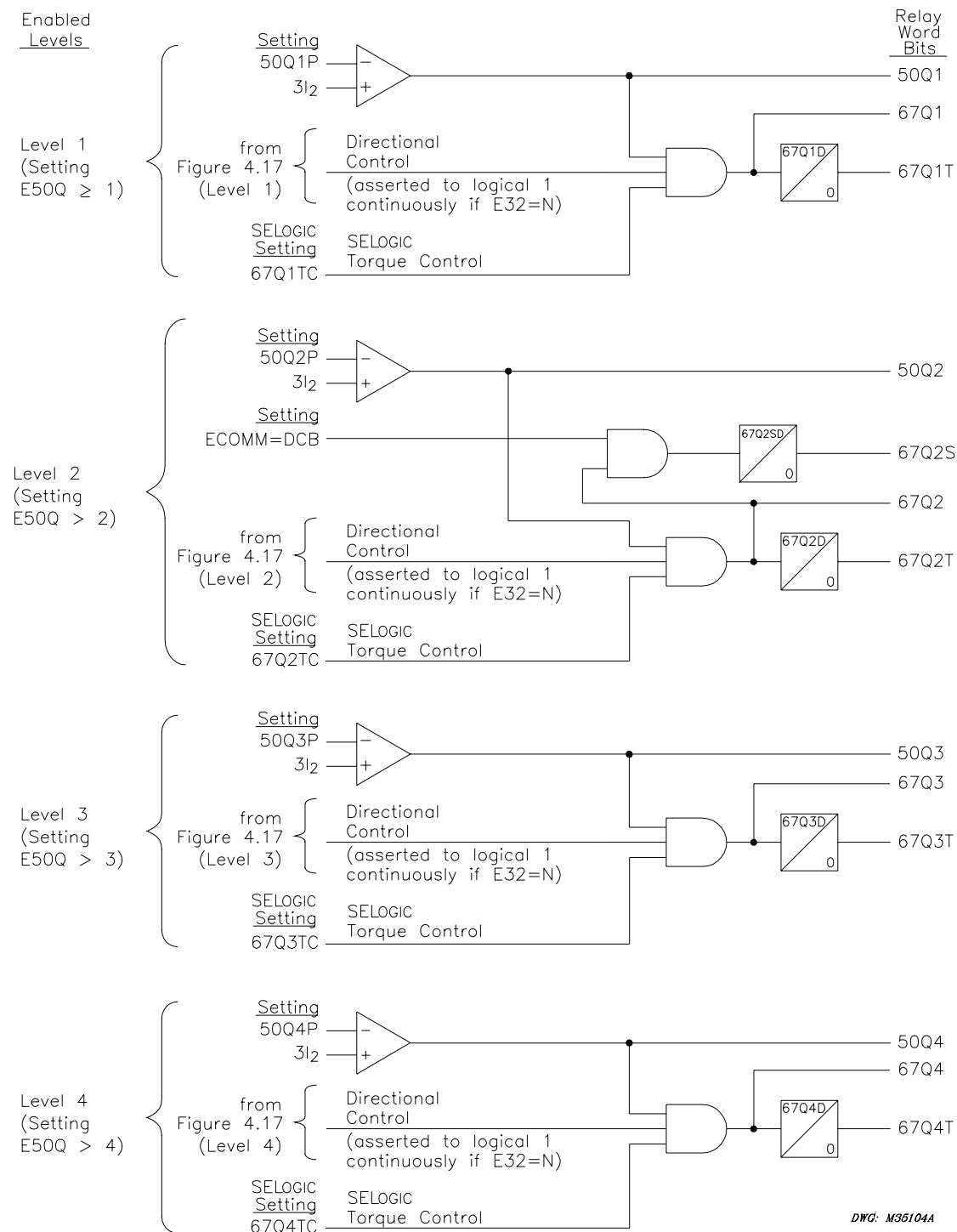


Figure 3.12: Levels 1 Through 4 Negative-Sequence Instantaneous/Definite-Time Overcurrent Elements (With Directional Control Option)

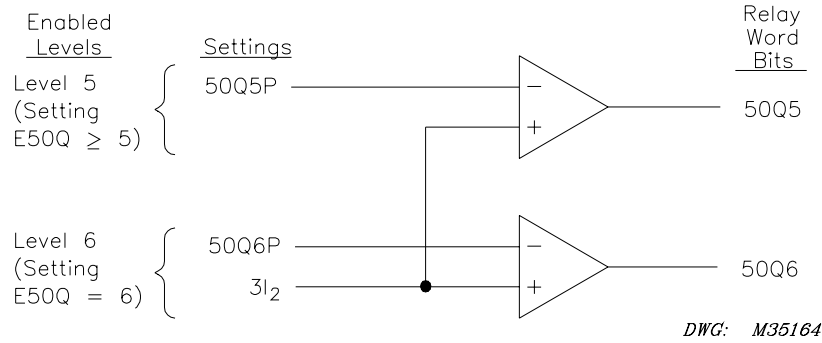


Figure 3.13: Levels 5 Through 6 Negative-Sequence Instantaneous Overcurrent Elements

TIME-OVERCURRENT ELEMENTS

Phase Time-Overcurrent Elements

Four phase time-overcurrent elements are available. The elements are enabled with the E51P enable setting as follows:

Table 3.1: Available Phase Time-Overcurrent Elements

Time-Overcurrent Element	Enabled with Setting	Operating Current	See Figure
51PT	E51P = 1 or 2	I_p , maximum of A-, B-, and C-phase currents	Figure 3.14
51AT	E51P = 2	I_A , A-phase current	Figure 3.15
51BT	E51P = 2	I_B , B-phase current	Figure 3.16
51CT	E51P = 2	I_C , C-phase current	Figure 3.17

The following is an example of 51PT element operation. The other phase time-overcurrent elements operate similarly (note the similarity among the logic in Figure 3.14, Figure 3.15, Figure 3.16, and Figure 3.17).

Settings Ranges (51PT Element Example)

Besides the settings involved with the Torque Control Switch operation in Figure 3.14, the 51PT phase time-overcurrent element has the following settings:

Table 3.2: Phase Time-Overcurrent Element (Maximum Phase) Settings

Setting	Definition	Range
51PP	pickup	0.50–16.00 A secondary (5 A nominal phase current inputs, IA, IB, IC) 0.10–3.20 A secondary (1 A nominal phase current inputs, IA, IB, IC)
51PC	curve type	U1–U5 (US curves) see Figure 9.1–Figure 9.10 C1–C5 (IEC curves)
51PTD	time dial	0.50–15.00 (US curves) see Figure 9.1–Figure 9.10 0.05–1.00 (IEC curves)
51PRS	electromechanical reset timing	Y, N
51PTC	SELOGIC control equation torque control setting	Relay Word bits referenced in Table 9.3 or set directly to logical 1 (=1)—see note below

Note: SELOGIC control equation torque control settings (e.g., 51PTC) cannot be set directly to logical 0.

See **Section 9: Setting the Relay** for additional time-overcurrent element setting information.

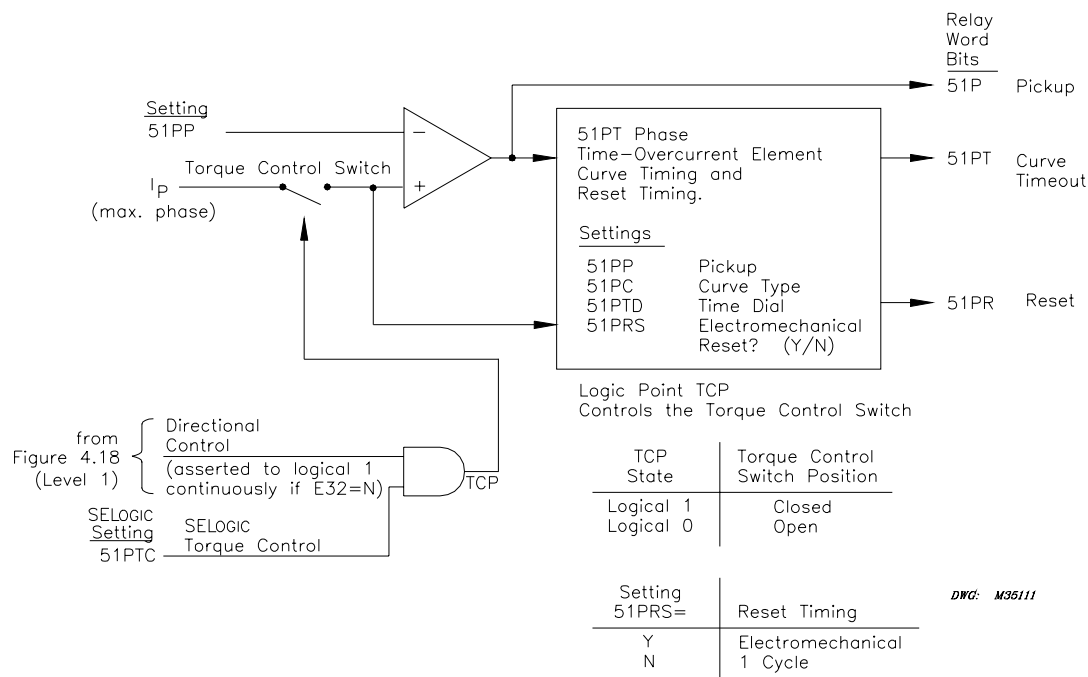


Figure 3.14: Phase Time-Overcurrent Element 51PT (With Directional Control Option)

Accuracy

Pickup: ± 0.05 A secondary and $\pm 3\%$ of setting (5 A nominal phase current inputs, IA, IB, IC)
 ± 0.01 A secondary and $\pm 3\%$ of setting (1 A nominal phase current inputs, IA, IB, IC)
 Curve Timing: ± 1.50 cycles and $\pm 4\%$ of curve time for currents between (and including)
 2 and 30 multiples of pickup

Logic Outputs (51PT Element Example)

The resultant logic outputs in Figure 3.14 are the following Relay Word bits:

Table 3.3: Phase Time-Overcurrent Element (Maximum Phase) Logic Outputs

Relay Word Bit	Definition/ Indication	Application
51P	Maximum phase current, I_p , is greater than phase time-overcurrent element pickup setting 51PP.	Element pickup testing or other control applications. See <i>Trip Logic</i> in <i>Section 5: Trip and Target Logic</i> .
51PT	Phase time-overcurrent element is timed out on its curve.	Tripping and other control applications. See <i>Trip Logic</i> in <i>Section 5: Trip and Target Logic</i> .
51PR	Phase time-overcurrent element is fully reset.	Element reset testing or other control applications.

Torque Control Switch Operation (51PT Element Example)

Torque Control Switch Closed

The pickup comparator in Figure 3.14 compares the pickup setting (51PP) to the maximum phase current, I_p , if the Torque Control Switch is closed. I_p is also routed to the curve timing/reset timing functions. The Relay Word Bits logic outputs operate as follows with the Torque Control Switch closed:

- 51P = 1 (logical 1), if $I_p >$ pickup setting 51PP and the phase time-overcurrent element is timing or is timed out on its curve
 = 0 (logical 0), if $I_p \leq$ pickup setting 51PP
- 51PT = 1 (logical 1), if $I_p >$ pickup setting 51PP and the phase time-overcurrent element is timed out on its curve
 = 0 (logical 0), if $I_p >$ pickup setting 51PP and the phase time-overcurrent element is timing, but not yet timed out on its curve
 = 0 (logical 0), if $I_p \leq$ pickup setting 51PP
- 51PR = 1 (logical 1), if $I_p \leq$ pickup setting 51PP and the phase time-overcurrent element is fully reset
 = 0 (logical 0), if $I_p \leq$ pickup setting 51PP and the phase time-overcurrent element is timing to reset (not yet fully reset)
 = 0 (logical 0), if $I_p >$ pickup setting 51PP and the phase time-overcurrent element is timing or is timed out on its curve

Torque Control Switch Open

If the Torque Control Switch in Figure 3.14 is open, maximum phase current, I_p , cannot get through to the pickup comparator (setting 51PP) and the curve timing/reset timing functions. For example, suppose that the Torque Control Switch is closed, I_p is:

$$I_p > \text{pickup setting 51PP}$$

and the phase time-overcurrent element is timing or is timed out on its curve. If the Torque Control Switch is then opened, I_p effectively appears as a magnitude of zero (0) to the pickup comparator:

$$I_p = 0 \text{ A (effective)} < \text{pickup setting 51PP}$$

resulting in Relay Word bit 51P deasserting to logical 0. I_p also effectively appears as a magnitude of zero (0) to the curve timing/reset timing functions, resulting in Relay Word bit 51PT also deasserting to logical 0. The phase time-overcurrent element then starts to time to reset. Relay Word bit 51PR asserts to logical 1 when the phase time-overcurrent element is fully reset.

Control of Logic Point TCP

Refer to Figure 3.14.

The Torque Control Switch is controlled by logic point TCP. Logic point TCP is controlled by directional control (optional) and SELOGIC control equation torque control setting 51PTC.

If logic point TCP = logical 1, the Torque Control Switch is closed and maximum phase current, I_p , is routed to the pickup comparator (setting 51PP) and the curve timing/reset timing functions.

If logic point TCP = logical 0, the Torque Control Switch is open and maximum phase current, I_p , cannot get through to the pickup comparator and the curve timing/reset timing functions. The maximum phase current, I_p , effectively appears as a magnitude of zero (0) to the pickup comparator and the curve timing/reset timing function.

Directional Control Option

Refer to Figure 3.14.

See Figure 4.18 in **Section 4: Loss-of-Potential, Load Encroachment, and Directional Element Logic** for more information on the optional directional control. If the directional control enable setting E32 is set:

$$E32 = N$$

then directional control is defeated, and the directional control input into logic point TCP in Figure 3.14 is asserted to logical 1 continuously. Then, only the corresponding SELOGIC control equation torque control setting 51PTC has to be considered in the control of logic point TCP (and, thus, in the control of the Torque Control Switch and phase time-overcurrent element 51PT).

Torque Control

Refer to Figure 3.14.

SELOGIC control equation torque control settings (e.g., 51PTC) cannot be set directly to logical 0. The following are setting examples of SELOGIC control equation torque control setting 51PTC for phase time-overcurrent element 51PT.

51PTC = 1 Setting 51PTC set directly to logical 1:

Then only the corresponding directional control input from Figure 4.18 has to be considered in the control of logic point TCP (and, thus, in the control of the Torque Control Switch and phase time-overcurrent element 51PT).

If directional control enable setting E32 = N, then logic point TCP = logical 1 and, thus, the Torque Control Switch closes and phase time-overcurrent element 51PT is enabled and nondirectional.

Note: All overcurrent element SELOGIC control equation torque control settings are set directly to logical 1 (e.g., 51PTC = 1) for the factory default settings. See *SHO Command (Show/View Settings)* in **Section 10: Serial Port Communications and Commands** for a list of the factory default settings.

51PTC = IN105 Input IN105 deasserted (51PTC = IN105 = logical 0):

Then logic point TCP = logical 0 and, thus, the Torque Control Switch opens and phase time-overcurrent element 51PT is defeated and nonoperational, regardless of any other setting.

Input IN105 asserted (51PTC = IN105 = logical 1):

Then only the corresponding directional control input from Figure 4.18 has to be considered in the control of logic point TCP (and, thus, in the control of the Torque Control Switch and phase time-overcurrent element 51PT).

If directional control enable setting E32 = N, then logic point TCP = logical 1 and, thus, the Torque Control Switch closes and phase time-overcurrent element 51PT is enabled and nondirectional.

Sometimes SELOGIC control equation torque control settings are set to provide directional control. See *Directional Control Provided by Torque Control Settings* at the end of **Section 4: Loss-of-Potential, Load Encroachment, and Directional Element Logic**.

Reset Timing Details (51PT Element Example)

Refer to Figure 3.14.

Any time current I_p goes above pickup setting 51PP and the phase time-overcurrent element starts timing, Relay Word bit 51PR (reset indication) = logical 0. If the phase time-overcurrent element times out on its curve, Relay Word bit 51PT (curve time-out indication) = logical 1.

Setting 51PRS = Y

If electromechanical reset timing setting 51PRS = Y, the phase time-overcurrent element reset timing emulates electromechanical reset timing. If maximum phase current, I_p , goes above pickup setting 51PP (element is timing or already timed out) and then current I_p goes below 51PP, the element starts to time to reset, emulating electromechanical reset timing. Relay Word bit 51PR (resetting indication) = logical 1 when the element is fully reset.

Setting 51PRS = N

If reset timing setting 51PRS = N, element 51PT reset timing is a 1-cycle dropout. If current I_p goes above pickup setting 51PP (element is timing or already timed out) and then current I_p goes below pickup setting 51PP, there is a 1-cycle delay before the element fully resets. Relay Word bit 51PR (reset indication) = logical 1 when the element is fully reset.

Operation of Single-Phase Time-Overcurrent Elements (51AT, 51BT, 51CT)

To understand the operation of Figure 3.15, Figure 3.16, and Figure 3.17 follow the explanation given for Figure 3.14 in the preceding part of this *Phase Time-Overcurrent Elements* subsection, substituting phase current I_A (or I_B or I_C) for maximum phase current I_p and substituting like settings and Relay Word bits. The settings ranges and accuracies for the single-phase time-overcurrent elements settings are the same as the corresponding settings in Table 3.2.

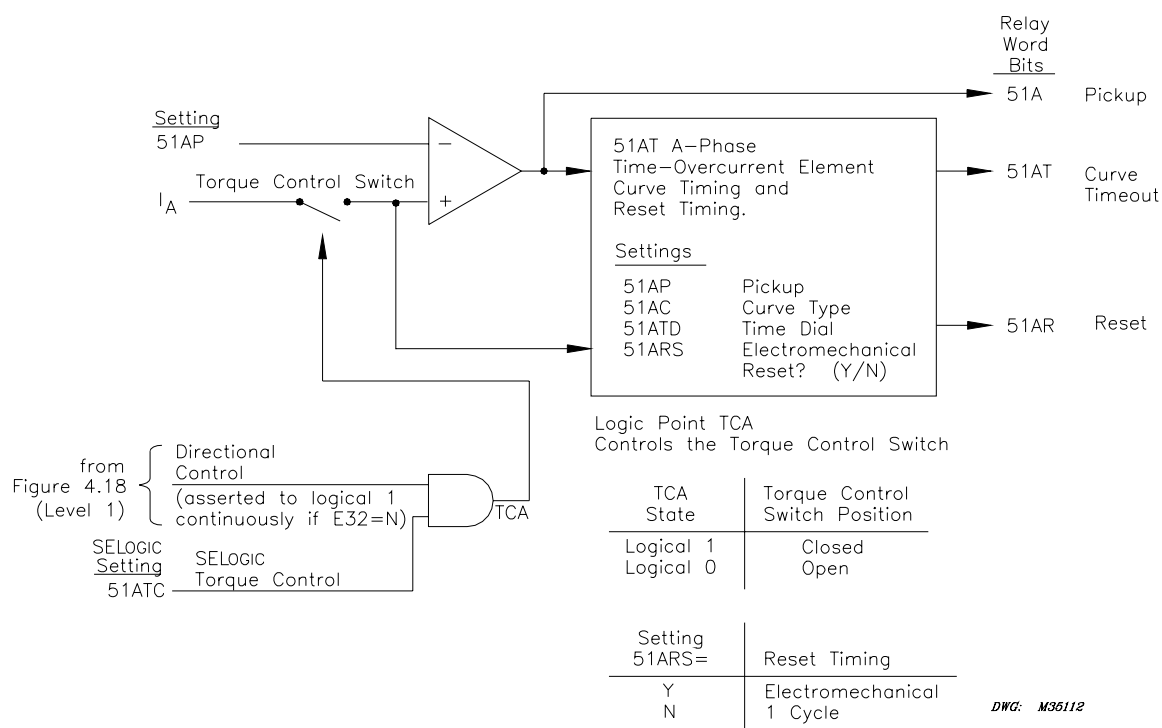


Figure 3.15: A-Phase Time-Overcurrent Element 51AT (With Directional Control Option)

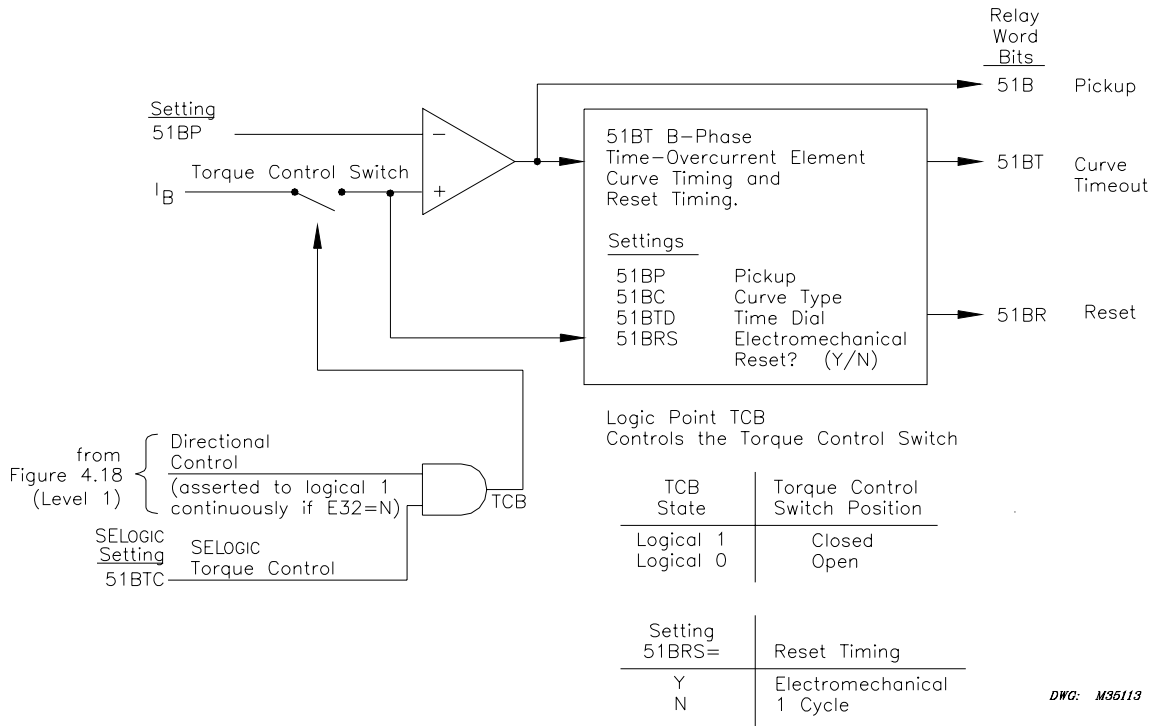


Figure 3.16: B-Phase Time-Overcurrent Element 51BT (With Directional Control Option)

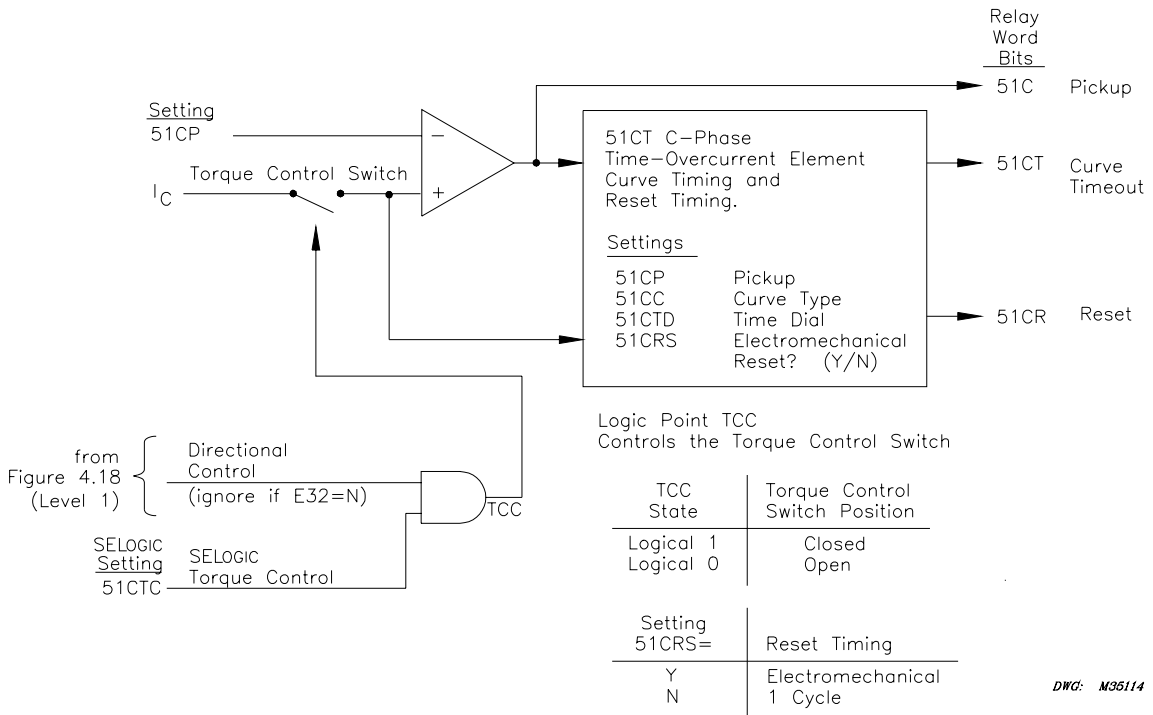


Figure 3.17: C-Phase Time-Overcurrent Element 51CT (With Directional Control Option)

Neutral Ground Time-Overcurrent Element

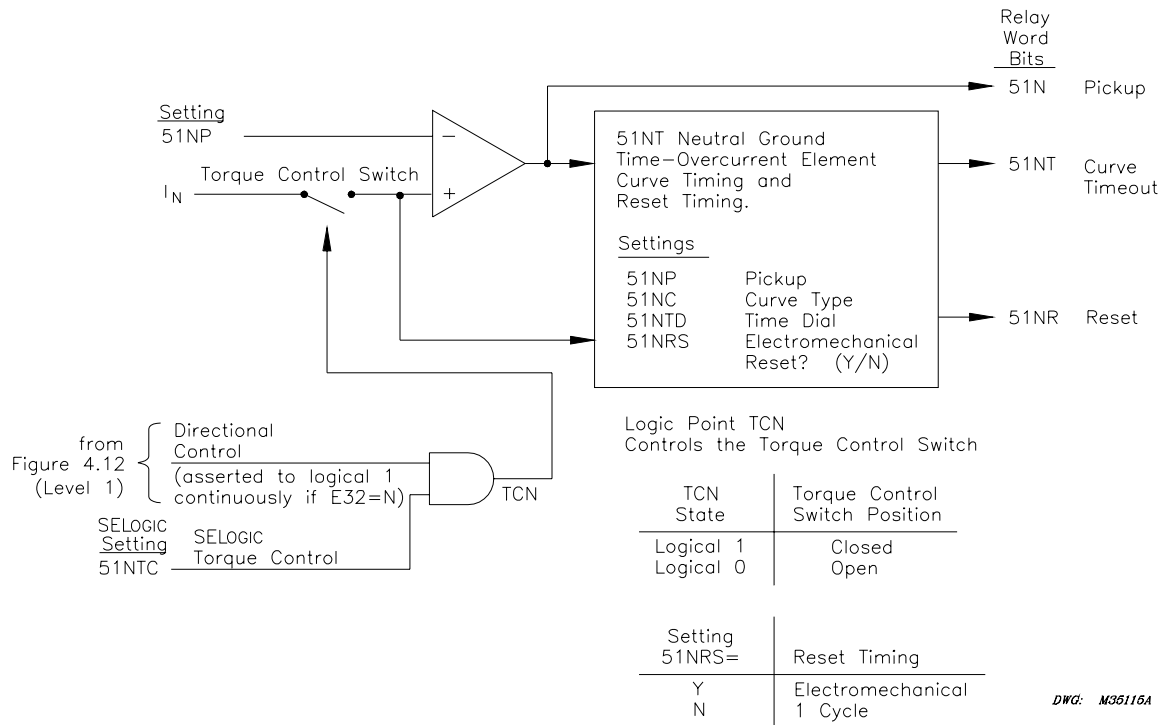


Figure 3.18: Neutral Ground Time-Overcurrent Element 51NT (With Directional Control Option)

To understand the operation of Figure 3.18, follow the explanation given for Figure 3.14 in the preceding *Phase Time-Overcurrent Elements* subsection, substituting current I_N (channel IN current) for maximum phase current I_p and substituting like settings and Relay Word bits.

For sensitive earth fault (SEF) applications, the SEL-351 Relay should be ordered with channel IN rated at 0.05 A nominal. For this channel IN rating, the increased pickup sensitivity of the neutral ground time-overcurrent element is noted in Table 3.4.

Settings Ranges

Table 3.4: Neutral Ground Time-Overcurrent Element Settings

Setting	Definition	Range
51NP	pickup	0.500–16.000 A secondary (5 A nominal channel IN current input) 0.100–3.200 A secondary (1 A nominal channel IN current input) 0.005–0.160 A secondary (0.05 A nominal channel IN current input)
51NC	curve type	U1–U5 (US curves) see Figure 9.1–Figure 9.10 C1–C5 (IEC curves)
51NTD	time dial	0.50–15.00 (US curves) see Figure 9.1–Figure 9.10 0.05–1.00 (IEC curves)
51NRS	electromechanical reset timing	Y, N
51NTC	SELOGIC control equation torque control setting	Relay Word bits referenced in Table 9.3 or set directly to logical 1 (= 1)—see note below

Note: SELOGIC control equation torque control setting (e.g., 51NTC) cannot be set directly to logical 0.

See *Section 9: Setting the Relay* for additional time-overcurrent element setting information.

Accuracy

Pickup: ± 0.05 A secondary and $\pm 3\%$ of setting (5 A nominal channel IN current input)
 ± 0.01 A secondary and $\pm 3\%$ of setting (1 A nominal channel IN current input)
 ± 1 mA secondary and $\pm 5\%$ of setting (0.05 A nominal channel IN current input)

Curve Timing: ± 1.50 cycles and $\pm 4\%$ of curve time for currents between (and including) 2 and 30 multiples of pickup

Residual Ground Time-Overcurrent Element

To understand the operation of Figure 3.19, follow the explanation given for Figure 3.14 in the preceding *Phase Time-Overcurrent Elements* subsection, substituting residual ground current I_G ($I_G = 3I_0 = I_A + I_B + I_C$) for maximum phase current I_p and substituting like settings and Relay Word bits.

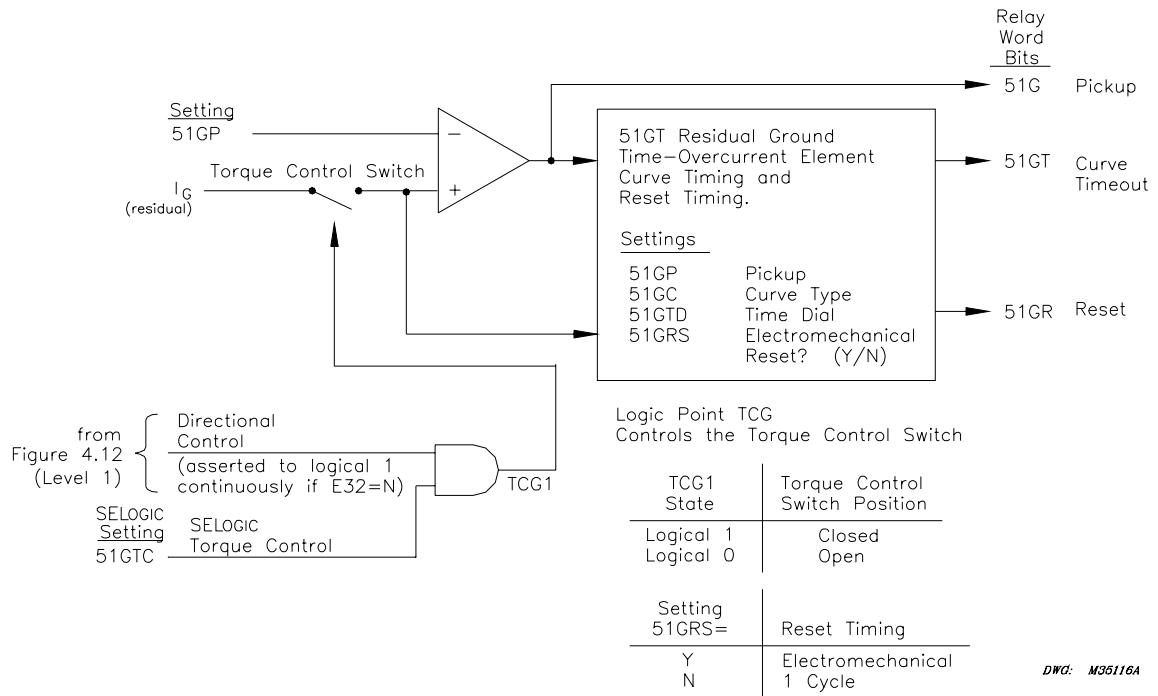


Figure 3.19: Residual Ground Time-Overcurrent Element 51GT (With Directional Control Option)

Settings Ranges

Table 3.5: Residual Ground Time-Overcurrent Element Settings

Setting	Definition	Range
51GP	pickup	0.50–16.00 A secondary (5 A nominal phase current inputs, IA, IB, IC) 0.10–3.20 A secondary (1 A nominal phase current inputs, IA, IB, IC)
51GC	curve type	U1–U5 (US curves) see Figure 9.1–Figure 9.10 C1–C5 (IEC curves)
51GTD	time dial	0.50–15.00 (US curves) see Figure 9.1–Figure 9.10 0.05–1.00 (IEC curves)
51GRS	electromechanical reset timing	Y, N
51GTC	SELOGIC control equation torque control setting	Relay Word bits referenced in Table 9.3 or set directly to logical 1 (= 1)—see note below

Note: SELOGIC control equation torque control setting (e.g., 51GTC) cannot be set directly to logical 0.

See **Section 9: Setting the Relay** for additional time-overcurrent element setting information.

Accuracy

- Pickup: ± 0.05 A secondary and $\pm 3\%$ of setting (5 A nominal phase current inputs, IA, IB, IC)
 ± 0.01 A secondary and $\pm 3\%$ of setting (1 A nominal phase current inputs, IA, IB, IC)
- Curve Timing: ± 1.50 cycles and $\pm 4\%$ of curve time for currents between (and including) 2 and 30 multiples of pickup

Negative-Sequence Time-Overcurrent Element

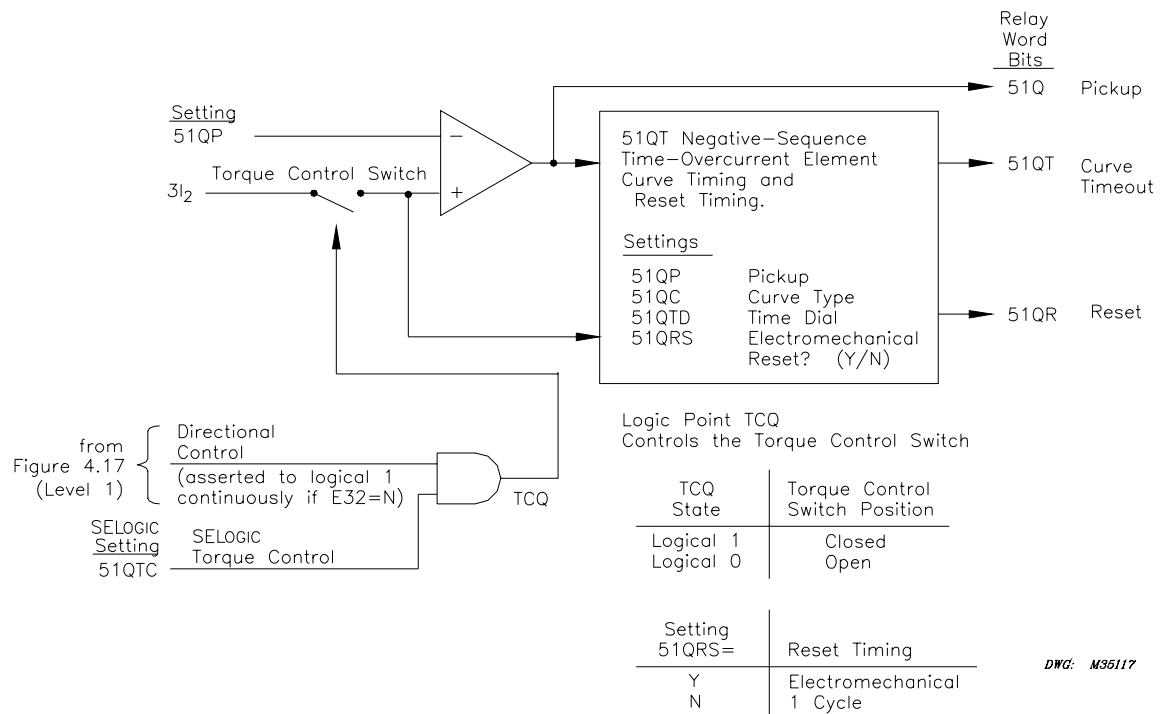


Figure 3.20: Negative-Sequence Time-Overcurrent Element 51QT (With Directional Control Option)

IMPORTANT: See *Appendix F* for information on setting negative-sequence overcurrent elements.

To understand the operation of Figure 3.20, follow the explanation given for Figure 3.14 in the preceding *Phase Time-Overcurrent Elements* subsection, substituting negative-sequence current $3I_2$ [$3I_2 = I_A + a^2 \cdot I_B + a \cdot I_C$ (ABC rotation), $3I_2 = I_A + a^2 \cdot I_C + a \cdot I_B$ (ACB rotation), where $a = 1 \angle 120^\circ$ and $a^2 = 1 \angle -120^\circ$] for maximum phase current I_P and like settings and Relay Word bits.

Settings Ranges

Table 3.6: Negative-Sequence Time-Overcurrent Element Settings

Setting	Definition	Range
51QP	pickup	0.50–16.00 A secondary (5 A nominal phase current inputs, IA, IB, IC) 0.10–3.20 A secondary (1 A nominal phase current inputs, IA, IB, IC)
51QC	curve type	U1–U5 (US curves) see Figure 9.1–Figure 9.10 C1–C5 (IEC curves)
51QTD	time dial	0.50–15.00 (US curves) see Figure 9.1–Figure 9.10 0.05–1.00 (IEC curves)
51QRS	electromechanical reset timing	Y, N
51QTC	SELOGIC control equation torque control setting	Relay Word bits referenced in Table 9.3 or set directly to logical 1 (= 1)—see note below

Note: SELOGIC control equation torque control setting (e.g., 51QTC) cannot be set directly to logical 0.

See *Section 9: Setting the Relay* for additional time-overcurrent element setting information.

Accuracy

Pickup: ± 0.05 A secondary and $\pm 3\%$ of setting (5 A nominal phase current inputs, IA, IB, IC)
 ± 0.01 A secondary and $\pm 3\%$ of setting (1 A nominal phase current inputs, IA, IB, IC)

Curve Timing: ± 1.50 cycles and $\pm 4\%$ of curve time for currents between (and including) 2 and 30 multiples of pickup

VOLTAGE ELEMENTS

Enable numerous voltage elements by making the enable setting:

$$\text{EVOLT} = \text{Y}$$

Voltage Values

The voltage elements operate off of various voltage values shown in Table 3.7.

Table 3.7: Voltage Values Used by Voltage Elements

Voltage	Description
V_A	A-phase voltage, from SEL-351 Relay rear-panel voltage input VA
V_B	B-phase voltage, from SEL-351 Relay rear-panel voltage input VB
V_C	C-phase voltage, from SEL-351 Relay rear-panel voltage input VC
V_{AB}	Phase-to-phase voltage
V_{BC}	Phase-to-phase voltage
V_{CA}	Phase-to-phase voltage
$3V_0$	Zero-sequence voltage
V_2	Negative-sequence voltage
V_1	Positive-sequence voltage
V_S	Synchronism check voltage, from SEL-351 Relay rear-panel voltage input VS (see Note 1)

Note 1: Voltage V_S is used in the synchronism check elements described in the following subsection *Synchronism Check Elements*. Voltage V_S is also used in the three voltage elements described at the end of Table 3.8 and in Figure 3.23. These voltage elements are independent of the synchronism check elements, even though voltage V_S is used in both.

Voltage Element Settings

Table 3.8 list available voltage elements and the corresponding voltage inputs and settings ranges for SEL-351 Relays (also refer to Figure 1.2).

Note: Voltage element pickup settings should not be set near zero, because they can assert or deassert due to noise when no signal is applied. SEL recommends a minimum setting of 2.00 V.

Table 3.8: Voltage Elements Settings and Settings Ranges

Voltage Element (Relay Word bits)	Operating Voltage	Pickup Setting/Range	See Figure
27A1	V_A	27P1P	Figure 3.21
27B1	V_B	0.00–150.00 V secondary {150 V voltage inputs}	
27C1	V_C	0.00–300.00 V secondary {300 V voltage inputs}	
3P27 = 27A1 * 27B1 * 27C1			
27A2	V_A	27P2P	
27B2	V_B	0.00–150.00 V secondary {150 V voltage inputs}	
27C2	V_C	0.00–300.00 V secondary {300 V voltage inputs}	
59A1	V_A	59P1P	
59B1	V_B	0.00–150.00 V secondary {150 V voltage inputs}	
59C1	V_C	0.00–300.00 V secondary {300 V voltage inputs}	
3P59 = 59A1 * 59B1 * 59C1			
59A2	V_A	59P2P	
59B2	V_B	0.00–150.00 V secondary {150 V voltage inputs}	
59C2	V_C	0.00–300.00 V secondary {300 V voltage inputs}	
27AB	V_{AB}	27PP	Figure 3.22
27BC	V_{BC}	0.00–260.00 V secondary {150 V voltage inputs}	
27CA	V_{CA}	0.00–520.00 V secondary {300 V voltage inputs}	
59AB	V_{AB}	59PP	
59BC	V_{BC}	0.00–260.00 V secondary {150 V voltage inputs}	
59CA	V_{CA}	0.00–520.00 V secondary {300 V voltage inputs}	
59N1	$3V_0$	59N1P 0.00–150.00 V secondary {150 V voltage inputs} 0.00–300.00 V secondary {300 V voltage inputs}	
59N2	$3V_0$	59N2P 0.00–150.00 V secondary {150 V voltage inputs} 0.00–300.00 V secondary {300 V voltage inputs}	
59Q	V_2	59QP 0.00–100.00 V secondary {150 V voltage inputs} 0.00–200.00 V secondary {300 V voltage inputs}	
59V1	V_1	59V1P 0.00–150.00 V secondary {150 V voltage inputs} 0.00–300.00 V secondary {300 V voltage inputs}	
27S	V_S	27SP 0.00–150.00 V secondary {150 V voltage inputs} 0.00–300.00 V secondary {300 V voltage inputs}	

Voltage Element (Relay Word bits)	Operating Voltage	Pickup Setting/Range	See Figure
59S1	V_s	59S1P 0.00–150.00 V secondary {150 V voltage inputs} 0.00–300.00 V secondary {300 V voltage inputs}	
59S2	V_s	59S2P 0.00–150.00 V secondary {150 V voltage inputs} 0.00–300.00 V secondary {300 V voltage inputs}	

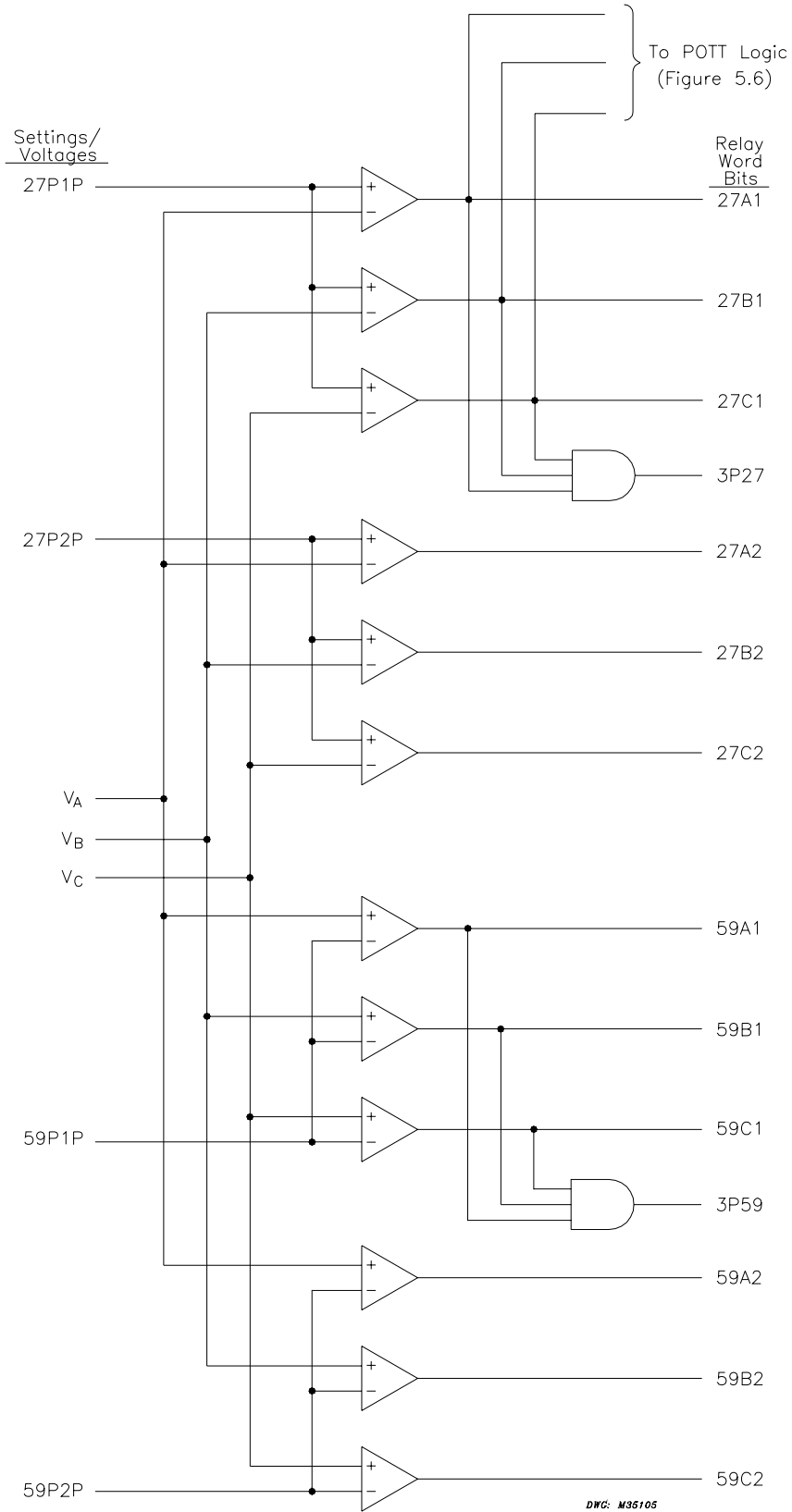


Figure 3.21: Single-Phase and Three-Phase Voltage Elements

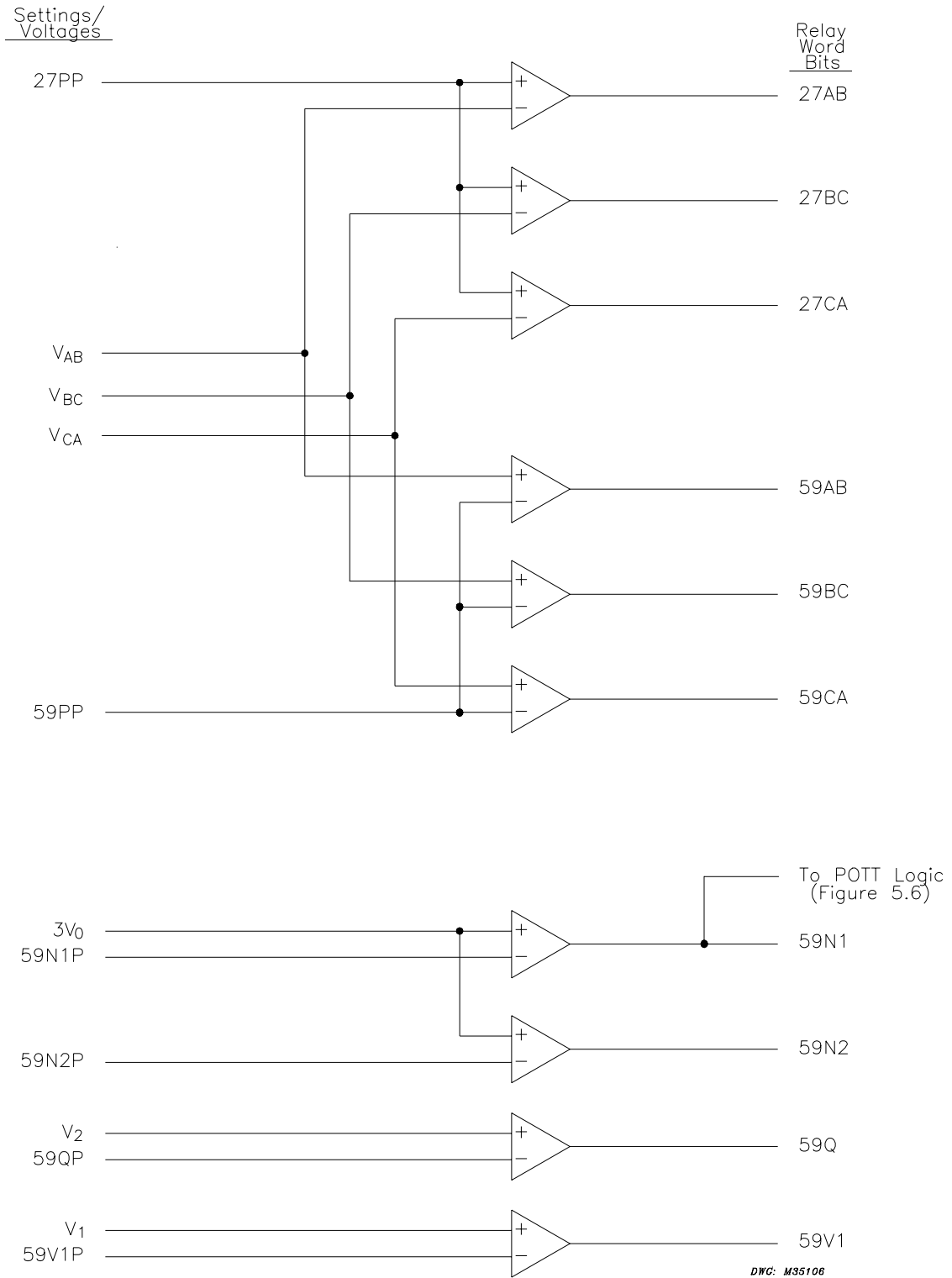
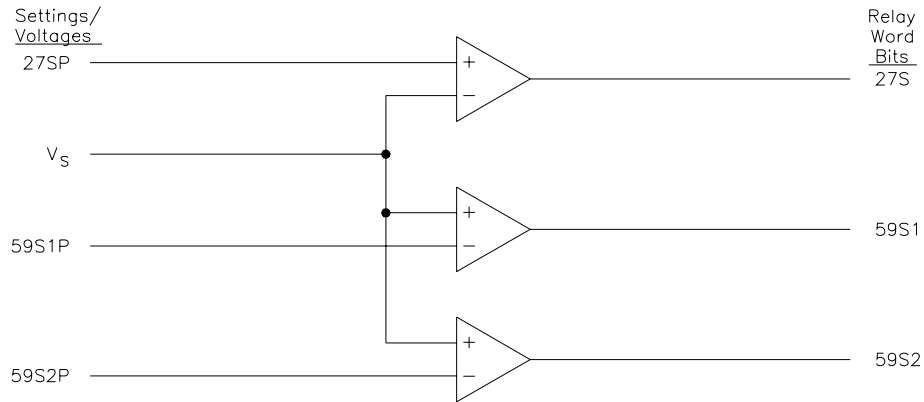


Figure 3.22: Phase-to-Phase and Sequence Voltage Elements



DWG: M35110

Figure 3.23: Channel VS Voltage Elements

Accuracy

Pickup: ± 1 V and $\pm 5\%$ of setting {150 V voltage inputs}
 ± 2 V and $\pm 5\%$ of setting {300 V voltage inputs}
 Transient Overreach: $\pm 5\%$ of setting

Voltage Element Operation

Note that the voltage elements in Table 3.8 and Figure 3.21 through Figure 3.23 are a combination of “undervoltage” (Device 27) and “overvoltage” (Device 59) type elements. Undervoltage elements (Device 27) assert when the operating voltage goes below the corresponding pickup setting. Overvoltage elements (Device 59) assert when the operating voltage goes above the corresponding pickup setting.

Undervoltage Element Operation Example

Refer to Figure 3.21 (top of the figure).

Pickup setting 27P1P is compared to the magnitudes of the individual phase voltages V_A , V_B , and V_C . The logic outputs in Figure 3.21 are the following Relay Word bits:

- 27A1 = 1 (logical 1), if $V_A <$ pickup setting 27P1P
 = 0 (logical 0), if $V_A \geq$ pickup setting 27P1P
- 27B1 = 1 (logical 1), if $V_B <$ pickup setting 27P1P
 = 0 (logical 0), if $V_B \geq$ pickup setting 27P1P
- 27C1 = 1 (logical 1), if $V_C <$ pickup setting 27P1P
 = 0 (logical 0), if $V_C \geq$ pickup setting 27P1P
- 3P27 = 1 (logical 1), if all three Relay Word bits 27A1, 27B1, and 27C1 are asserted (27A1 = 1, 27B1 = 1, and 27C1 = 1)
 = 0 (logical 0), if at least one of the Relay Word bits 27A1, 27B1, or 27C1 is deasserted (e.g., 27A1 = 0)

Overvoltage Element Operation Example

Refer to Figure 3.21 (bottom of the figure).

Pickup setting 59P1P is compared to the magnitudes of the individual phase voltages V_A , V_B , and V_C . The logic outputs in Figure 3.21 are the following Relay Word bits:

59A1 = 1 (logical 1), if $V_A >$ pickup setting 59P1P
= 0 (logical 0), if $V_A \leq$ pickup setting 59P1P

59B1 = 1 (logical 1), if $V_B >$ pickup setting 59P1P
= 0 (logical 0), if $V_B \leq$ pickup setting 59P1P

59C1 = 1 (logical 1), if $V_C >$ pickup setting 59P1P
= 0 (logical 0), if $V_C \leq$ pickup setting 59P1P

3P59 = 1 (logical 1), if all three Relay Word bits 59A1, 59B1, and 59C1 are asserted
(59A1 = 1, 59B1 = 1, and 59C1 = 1)
= 0 (logical 0), if at least one of the Relay Word bits 59A1, 59B1, or 59C1 is deasserted (e.g., 59A1 = 0)

Voltage Elements Used in POTT Logic

Refer to Figure 3.21 and Figure 3.22 for wye-connected voltage inputs. Note that voltage elements 27A1, 27B1, 27C1, and 59N1 are also used in the weak-infeed portion of the POTT logic, if the weak-infeed logic is enabled (see Figure 5.6).

If the weak-infeed portion of the POTT logic is enabled (setting EWFC = Y) and these voltage elements are used in the logic, they can still be used in other applications (if the settings are applicable). If the weak-infeed portion of the POTT logic is not enabled, these voltage elements can be used in any desired application.

SYNCHRONISM CHECK ELEMENTS

Enable the two single-phase synchronism check elements by making the enable setting:

E25 = Y

Figure 2.6 through Figure 2.9 in **Section 2: Installation** show examples where synchronism check can be applied. Synchronism check voltage input VS is connected to one side of the circuit breaker, on any desired phase. The other synchronizing phase (V_A , V_B , or V_C voltage inputs) on the other side of the circuit breaker is setting-selected.

The two synchronism check elements use the same voltage window (to assure healthy voltage) and slip frequency settings (see Figure 3.24). They have separate angle settings (see Figure 3.25).

If the voltages are static (voltages not slipping with respect to one another) or setting TCLOSD = 0.00, the two synchronism check elements operate as shown in the top of Figure 3.25. The angle settings are checked for synchronism check closing.

If the voltages are not static (voltages slipping with respect to one another), the two synchronism check elements operate as shown in the bottom of Figure 3.25. The angle difference is compen-

sated by breaker close time, and the breaker is ideally closed at a zero degree phase angle difference, to minimize system shock.

These synchronism check elements are explained in detail in the following text.

Voltage Input VS Connected Phase-to-Phase or Beyond Delta-Wye Transformer

Sometimes synchronism check voltage V_S cannot be in phase with voltage V_A , V_B , or V_C . This happens in applications where voltage input V_S is connected phase-to-phase or beyond a delta-wye transformer. For such applications requiring V_S to be at a constant phase angle difference from any of the possible synchronizing voltages (V_A , V_B , or V_C), an angle setting is made with the SYNCP setting (see Table 3.9 and the SYNCP setting discussion that follows).

Synchronism Check Elements Settings

Table 3.9: Synchronism Check Elements Settings and Settings Ranges

Setting	Definition	Range
25VLO	low voltage threshold for “healthy voltage” window	0.00–150.00 V secondary (150 V voltage inputs) 0.00–300.00 V secondary (300 V voltage inputs)
25VHI	high voltage threshold for “healthy voltage” window	0.00–150.00 V secondary (150 V voltage inputs) 0.00–300.00 V secondary (300 V voltage inputs)
25SF	maximum slip frequency	0.005–0.500 Hz
25ANG1	synchronism check element 25A1 maximum angle	0°–80°
25ANG2	synchronism check element 25A2 maximum angle	0°–80°
SYNCP	synchronizing phase or the number of degrees that synchronism check voltage V_S constantly lags voltage V_A	V_A , V_B , or V_C 0°–330°, in 30-degree steps
TCLOSD	breaker close time for angle compensation	0.00–60.00 cycles
BSYNCH	SELOGIC control equation block synchronism check setting	Relay Word bits referenced in Table 9.4

Setting SYNCP

The angle setting choices (0, 30, ..., 300, or 330 degrees) for setting SYNCP are referenced to V_A . They indicate how many degrees V_S constantly lags V_A . In any synchronism check application, voltage input V_A -N always has to be connected to determine system frequency on one side of the circuit breaker (to determine the slip between V_S and V_A). V_A always has to meet

the “healthy voltage” criteria (settings 25VHI and 25VLO—see Figure 3.24). Thus, for situations where V_S cannot be in phase with V_A , V_B , or V_C , it is most straightforward to have the angle setting choices (0, 30, ..., 300, or 330 degrees) referenced to V_A . See Application Guide entitled *Compensate for Constant Phase Angle Difference in Synchronism Check with the SEL-351 Relay Family* for more information on setting SYNCP with an angle setting.

Note on setting SYNCP = 0:

Settings SYNCP = 0 and SYNCP = VA are effectively the same (voltage V_S is directly synchronism checked with voltage V_A ; V_S does not lag V_A). The relay will display the setting entered (SYNCP = VA or SYNCP = 0).

Accuracy

Voltage Pickup:	± 1 V and $\pm 5\%$ of setting {150 V voltage inputs}
	± 2 V and $\pm 5\%$ of setting {300 V voltage inputs}
Voltage Transient Overreach:	$\pm 5\%$ of setting
Slip Pickup:	0.003 Hz
Angle Pickup:	$\pm 4^\circ$

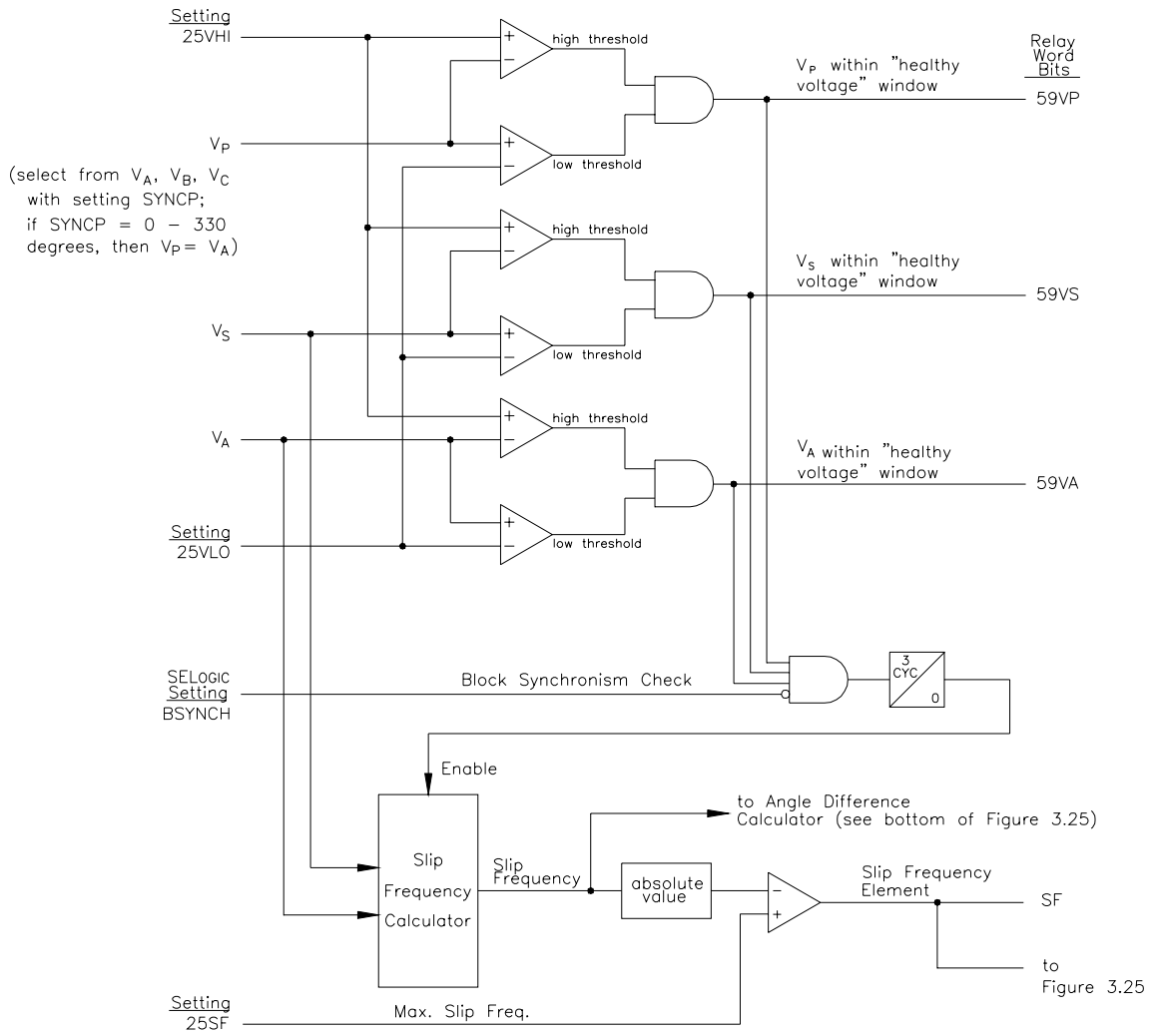
Synchronism Check Elements Voltage Inputs

The two synchronism check elements are single-phase elements, with single-phase voltage inputs V_P and V_S used for both elements:

V_P Phase input voltage (V_A , V_B , or V_C for wye-connected voltages), designated by setting SYNCP (e.g., if SYNCP = VB, then $V_P = V_B$)

V_S Synchronism check voltage, from SEL-351 Relay rear-panel voltage input VS

For example, if V_P is designated as phase input voltage V_B (setting SYNCP = VB), then rear-panel voltage input VS is connected to B-phase on the other side of the circuit breaker. The voltage across terminals VB-N is synchronism checked with the voltage across terminals VS-NS (see Figure 1.2 and Figure 2.6 through Figure 2.9).



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Figure 3.24: Synchronism Check Voltage Window and Slip Frequency Elements

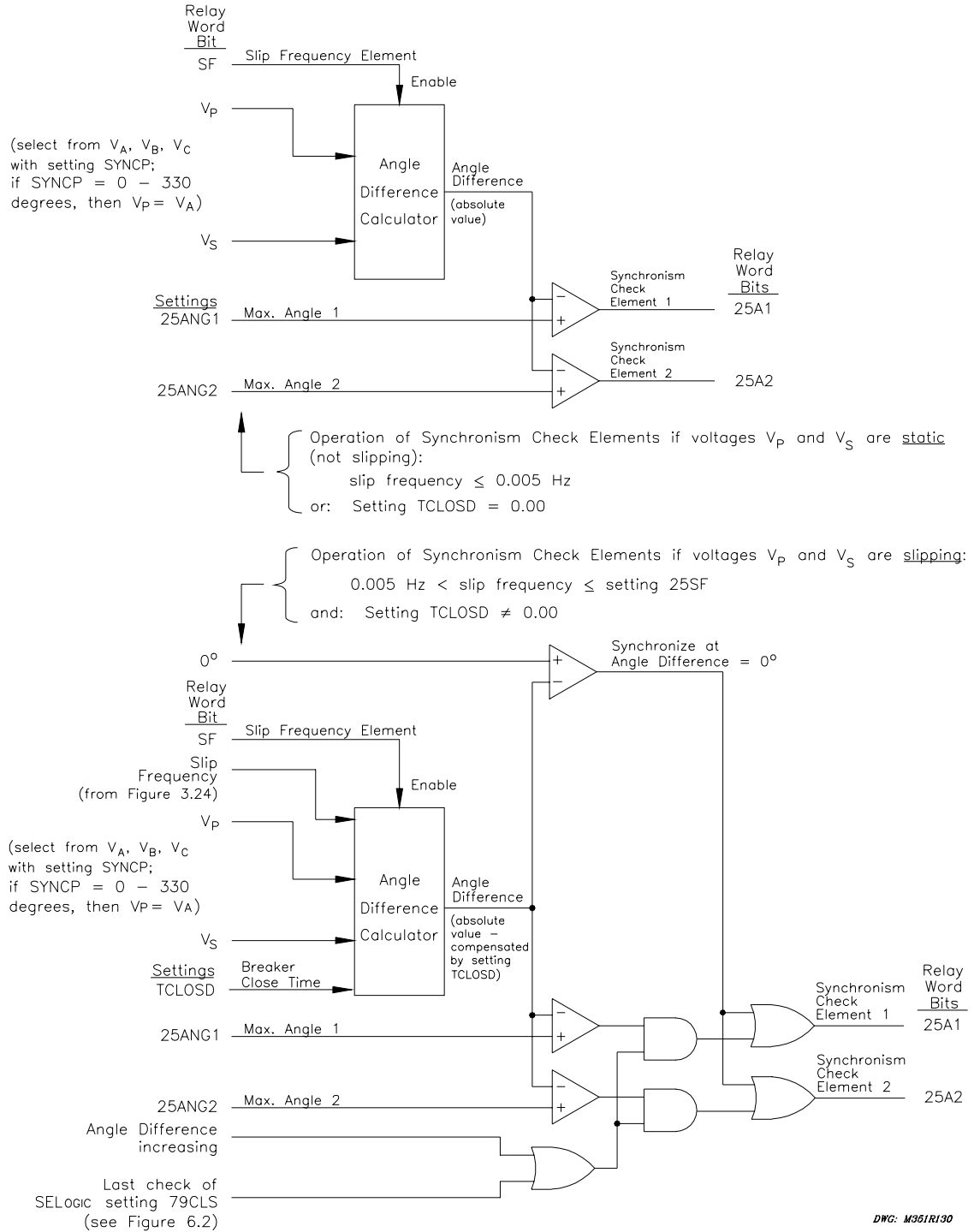


Figure 3.25: Synchronism Check Elements

System Frequencies Determined from Voltages V_A and V_S

To determine slip frequency, the system frequencies on both sides of the circuit breaker need to be determined. Voltage V_S determines the frequency on one side. Voltage V_A (for wye-connected voltage inputs) determines the frequency on the other side. Thus, voltage terminals VA-N have to be connected, even if another voltage (e.g., voltage V_B) is to be synchronized with voltage V_S .

In most applications, all three voltage inputs VA, VB, and VC are connected to the three-phase power system and no additional connection concerns are needed for voltage connection VA-N. The presumption is that the frequency determined for A-phase is also valid for B- and C-phase in a three-phase power system.

However, for example, if voltage V_B is to be synchronized with voltage V_S and plans were to connect only voltage terminals VB-N and VS-NS then voltage terminals VA-N will also have to be connected for frequency determination. If desired, voltage terminals VA-N can be connected in parallel with voltage terminals VB-N. In such a nonstandard parallel connection, remember that voltage terminals VA-N are monitoring Phase B. This understanding helps prevent confusion when observing metering and event report information or voltage element operation.

Another possible solution to this example (synchronism check voltage input VS connected to Phase B) is to make setting SYNCP = 120 (the number of degrees that synchronism check voltage V_S constantly lags voltage V_A) and connect voltage input VA to Phase A. Voltage input VB doesn't have to be connected.

System Rotation Can Affect Setting SYNCP

The solution in the preceding paragraph:

- Voltage input VA connected to Phase A
- Voltage input VS connected to Phase B
- Setting SYNCP = 120 degrees (V_S constantly lags V_A by 120°)

presumes ABC system rotation. If voltage input connections are the same, but system rotation is ACB, then setting SYNCP = 240 degrees (V_S constantly lags V_A by 240°). For more information on setting SYNCP with an angle setting, see Application Guide titled *Compensate for Constant Phase Angle Difference in Synchronism Check with the SEL-351 Relay Family*.

Synchronism Check Elements Operation

Refer to Figure 3.24 and Figure 3.25.

Voltage Window

Refer to Figure 3.24.

Single-phase voltage inputs V_P and V_S are compared to a voltage window, to verify that the voltages are “healthy” and lie within settable voltage limits 25VLO and 25VHI. If both voltages are within the voltage window, the following Relay Word bits assert:

- 59VP indicates that voltage V_P is within voltage window setting limits 25VLO and 25VHI
- 59VS indicates that voltage V_S is within voltage window setting limits 25VLO and 25VHI

As discussed previously, voltage V_A (for wye-connected voltage inputs) determines the frequency on the voltage V_P side of the circuit breaker. Voltage V_A is also run through voltage limits 25VLO and 25VHI to assure “healthy voltage” for frequency determination, with corresponding Relay Word bit output 59VA.

Other Uses for Voltage Window Elements

If voltage limits 25VLO and 25VHI are applicable to other control schemes, Relay Word bits 59VP, 59VS, and 59VA can be used in other logic at the same time they are used in the synchronism check logic.

If synchronism check is not being used, Relay Word bits 59VP, 59VS, and 59VA can still be used in other logic, with voltage limit settings 25VLO and 25VHI set as desired. Enable the synchronism check logic (setting E25 = Y) and make settings 25VLO and 25VHI. Apply Relay Word bits 59VP, 59VS, and 59VA in desired logic scheme, using SELOGIC control equations. Even though synchronism check logic is enabled, the synchronism check logic outputs (Relay Word bits SF, 25A1, and 25A2) do not need to be used.

Block Synchronism Check Conditions

Refer to Figure 3.24.

The synchronism check element slip frequency calculator runs if both voltages V_P and V_S are healthy (59VP and 59VS asserted to logical 1) and the SELOGIC control equation setting BSYNCH (Block Synchronism Check) is deasserted (= logical 0). Setting BSYNCH is most commonly set to block synchronism check operation when the circuit breaker is closed (synchronism check is only needed when the circuit breaker is open):

$$\text{BSYNCH} = 52A \quad (\text{see Figure 6.1 and Figure 7.3})$$

In addition, synchronism check operation can be blocked when the relay is tripping:

$$\text{BSYNCH} = \dots + \text{TRIP}$$

Slip Frequency Calculator

Refer to Figure 3.24.

The synchronism check element Slip Frequency Calculator in Figure 3.24 runs if voltages V_P , V_S , and V_A are healthy (59VP, 59VS, and 59VA asserted to logical 1) and the SELOGIC control equation setting BSYNCH (Block Synchronism Check) is deasserted (= logical 0). The Slip Frequency Calculator output is:

$$\begin{aligned} \text{Slip Frequency} &= f_p - f_s && (\text{in units of Hz} = \text{slip cycles/second}) \\ f_p &= \text{frequency of voltage } V_P && (\text{in units of Hz} = \text{cycles/second}) \text{ [determined from } V_A] \\ f_s &= \text{frequency of voltage } V_S && (\text{in units of Hz} = \text{cycles/second}) \end{aligned}$$

A complete slip cycle is one single 360-degree revolution of one voltage (e.g., V_S) by another voltage (e.g., V_P). Both voltages are thought of as revolving phasor-wise, so the “slipping” of V_S past V_P is the relative revolving of V_S past V_P .

For example, in Figure 3.24, if voltage V_P has a frequency of 59.95 Hz and voltage V_S has a frequency of 60.05 Hz, the difference between them is the slip frequency:

$$\text{Slip Frequency} = 59.95 \text{ Hz} - 60.05 \text{ Hz} = -0.10 \text{ Hz} = -0.10 \text{ slip cycles/second}$$

The slip frequency in this example is negative, indicating that voltage V_S is not “slipping” behind voltage V_P , but in fact “slipping” ahead of voltage V_P . In a time period of one second, the angular distance between voltage V_P and voltage V_S changes by 0.10 slip cycles, which translates into:

$$0.10 \text{ slip cycles/second} \times (360^\circ/\text{slip cycle}) \times 1 \text{ second} = 36^\circ$$

Thus, in a time period of one second, the angular distance between voltage V_P and voltage V_S changes by 36 degrees.

The absolute value of the Slip Frequency output is run through a comparator and if the slip frequency is less than the maximum slip frequency setting, 25SF, Relay Word bit SF asserts to logical 1.

Angle Difference Calculator

The synchronism check element Angle Difference Calculator in Figure 3.25 runs if the slip frequency is less than the maximum slip frequency setting 25SF (Relay Word bit SF is asserted).

Voltages V_P and V_S are “Static”

Refer to top of Figure 3.25.

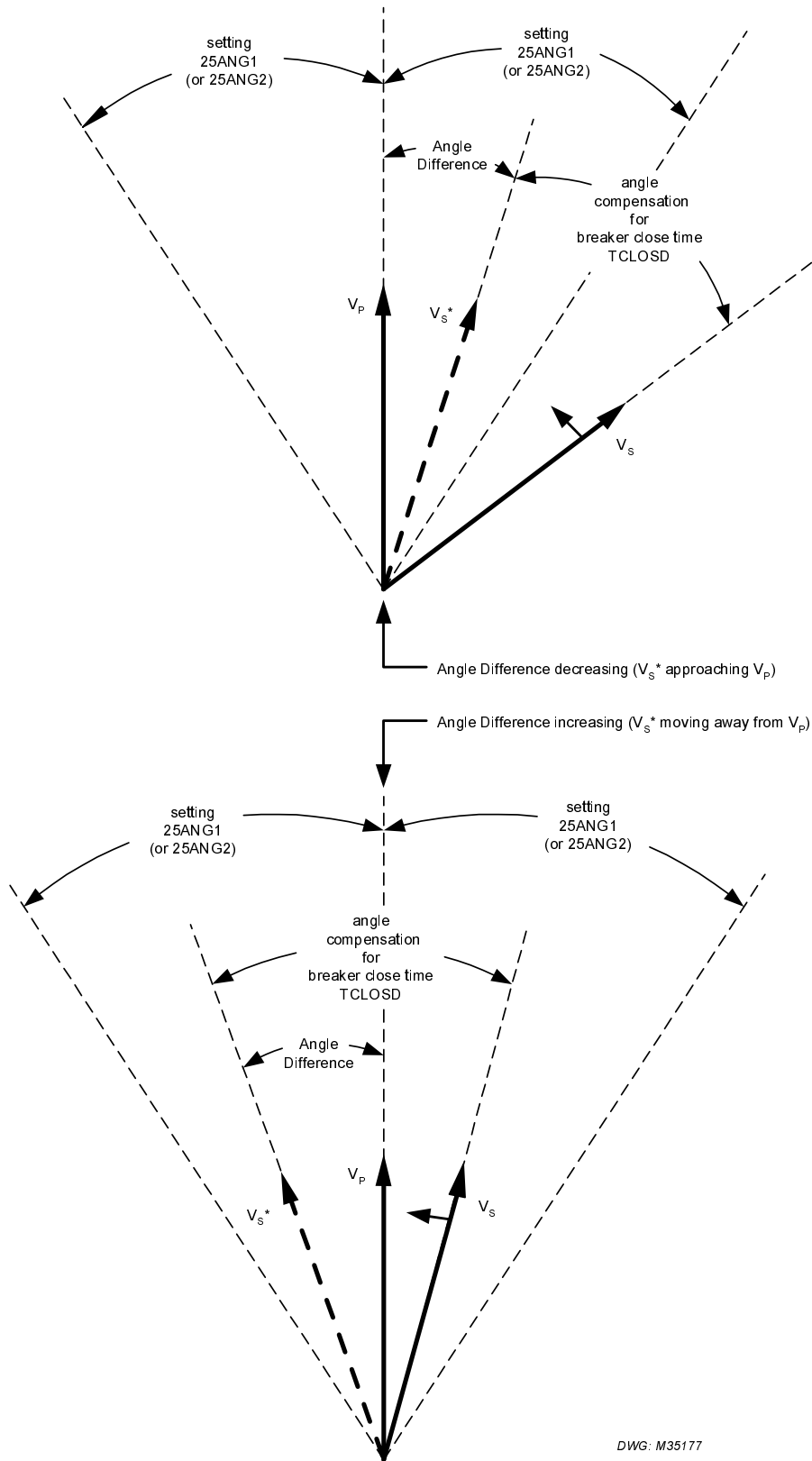
If the slip frequency is less than or equal to 0.005 Hz, the Angle Difference Calculator does not take into account breaker close time—it presumes voltages V_P and V_S are “static” (not “slipping” with respect to one another). This would usually be the case for an open breaker with voltages V_P and V_S that are paralleled via some other electric path in the power system. The Angle Difference Calculator calculates the angle difference between voltages V_P and V_S :

$$\text{Angle Difference} = |(\angle V_P - \angle V_S)|$$

For example, if $\text{SYNCP} = 90$ (indicating V_S constantly lags $V_P = V_A$ by 90 degrees), but V_S actually lags V_A by 100 angular degrees on the power system at a given instant, the Angle Difference Calculator automatically accounts for the 90 degrees and:

$$\text{Angle Difference} = |(\angle V_P - \angle V_S)| = 10^\circ$$

Also, if breaker close time setting $\text{TCLOSD} = 0.00$, the Angle Difference Calculator does not take into account breaker close time, even if the voltages V_P and V_S are “slipping” with respect to one another. Thus, synchronism check elements 25A1 or 25A2 assert to logical 1 if the Angle Difference is less than corresponding maximum angle setting 25ANG1 or 25ANG2.



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Figure 3.26: Angle Difference Between V_P and V_S Compensated by Breaker Close Time ($f_P < f_S$ and V_P Shown as Reference in This Example)

Voltages V_p and V_s are “Slipping”

Refer to bottom of Figure 3.25.

If the slip frequency is greater than 0.005 Hz and breaker close time setting TCLOSD \neq 0.00, the Angle Difference Calculator takes the breaker close time into account with breaker close time setting TCLOSD (set in cycles; see Figure 3.26). The Angle Difference Calculator calculates the Angle Difference between voltages V_p and V_s , compensated with the breaker close time:

$$\text{Angle Difference} = \left| (\angle V_p - \angle V_s) + [(f_p - f_s) \times \text{TCLOSD} \times (1 \text{ second}/60 \text{ cycles}) \times (360^\circ/\text{slip cycle})] \right|$$

Angle Difference Example (Voltages V_p and V_s are “Slipping”)

Refer to bottom of Figure 3.25.

For example, if the breaker close time is 10 cycles, set TCLOSD = 10. Presume the slip frequency is the example slip frequency calculated previously. The Angle Difference Calculator calculates the angle difference between voltages V_p and V_s , compensated with the breaker close time:

$$\text{Angle Difference} = \left| (\angle V_p - \angle V_s) + [(f_p - f_s) \times \text{TCLOSD} \times (1 \text{ second}/60 \text{ cycles}) \times (360^\circ/\text{slip cycle})] \right|$$

Intermediate calculations:

$$(f_p - f_s) = (59.95 \text{ Hz} - 60.05 \text{ Hz}) = -0.10 \text{ Hz} = -0.10 \text{ slip cycles/second}$$

$$\text{TCLOSD} \times (1 \text{ second}/60 \text{ cycles}) = 10 \text{ cycles} \times (1 \text{ second}/60 \text{ cycles}) = 0.167 \text{ second}$$

Resulting in:

$$\begin{aligned} \text{Angle Difference} &= \left| (\angle V_p - \angle V_s) + [(f_p - f_s) \times \text{TCLOSD} \times (1 \text{ second}/60 \text{ cycles}) \times (360^\circ/\text{slip cycle})] \right| \\ &= \left| (\angle V_p - \angle V_s) + [-0.10 \times 0.167 \times 360^\circ] \right| \\ &= \left| (\angle V_p - \angle V_s) - 6^\circ \right| \end{aligned}$$

During the breaker close time (TCLOSD), the voltage angle difference between voltages V_p and V_s changes by 6 degrees. This 6 degree angle compensation is applied to voltage V_s , resulting in derived voltage V_s^* , as shown in Figure 3.26.

Note: The angle compensation in Figure 3.26 appears much greater than 6 degrees. Figure 3.26 is for general illustrative purposes only.

The top of Figure 3.26 shows the Angle Difference decreasing— V_s^* is approaching V_p . Ideally, circuit breaker closing is initiated when V_s^* is in phase with V_p (Angle Difference = 0 degrees). Then when the circuit breaker main contacts finally close, V_s is in phase with V_p , minimizing system shock.

The bottom of Figure 3.26 shows the Angle Difference increasing— V_s^* is moving away from V_p . Ideally, circuit breaker closing is initiated when V_s^* is in phase with V_p (Angle Difference = 0 degrees). Then when the circuit breaker main contacts finally close, V_s is in phase with V_p . But in this case, V_s^* has already moved past V_p . In order to initiate circuit breaker closing when V_s^* is in phase with V_p (Angle Difference = 0 degrees), V_s^* has to slip around another revolution, relative to V_p .

Synchronism Check Element Outputs

Synchronism check element outputs (Relay Word bits 25A1 and 25A2 in Figure 3.25) assert to logical 1 for the conditions explained in the following text.

Voltages V_p and V_s are “Static” or Setting TCLOSD = 0.00

Refer to top of Figure 3.25.

If V_p and V_s are “static” (not “slipping” with respect to one another), the Angle Difference between them remains constant—it is not possible to close the circuit breaker at an ideal zero degree phase angle difference. Thus, synchronism check elements 25A1 or 25A2 assert to logical 1 if the Angle Difference is less than corresponding maximum angle setting 25ANG1 or 25ANG2.

Also, if breaker close time setting TCLOSD = 0.00, the Angle Difference Calculator does not take into account breaker close time, even if the voltages V_p and V_s are “slipping” with respect to one another. Thus, synchronism check elements 25A1 or 25A2 assert to logical 1 if the Angle Difference is less than corresponding maximum angle setting 25ANG1 or 25ANG2.

Voltages V_p and V_s are “Slipping” and Settling TCLOSD \neq 0.00

Refer to bottom of Figure 3.25. If V_p and V_s are “slipping” with respect to one another and breaker close time setting TCLOSD \neq 0.00, the Angle Difference (compensated by breaker close time TCLOSD) changes through time. Synchronism check element 25A1 or 25A2 asserts to logical 1 for any one of the following three scenarios.

1. The top of Figure 3.26 shows the Angle Difference decreasing— V_s^* is approaching V_p . When V_s^* is in phase with V_p (Angle Difference = 0 degrees), synchronism check elements 25A1 and 25A2 assert to logical 1.
2. The bottom of Figure 3.26 shows the Angle Difference increasing— V_s^* is moving away from V_p . V_s^* was in phase with V_p (Angle Difference = 0 degrees), but has now moved past V_p . If the Angle Difference is increasing, but the Angle Difference is still less than maximum angle settings 25ANG1 or 25ANG2, then corresponding synchronism check elements 25A1 or 25A2 assert to logical 1.

In this scenario of the Angle Difference increasing, but still being less than maximum angle settings 25ANG1 or 25ANG2, the operation of corresponding synchronism check elements 25A1 and 25A2 becomes less restrictive. Synchronism check breaker closing does not have to wait for voltage V_s^* to slip around again in phase with V_p (Angle Difference = 0 degrees). There might not be enough time to wait for this to happen. Thus, the “Angle Difference = 0 degrees” restriction is eased for this scenario.

3. Refer to ***Reclose Supervision Logic*** in ***Section 6: Close and Reclose Logic***.

Refer to the bottom of Figure 6.2 in ***Section 6: Close and Reclose Logic***. If timer 79CLSD is set greater than zero (e.g., 79CLSD = 60.00 cycles) and it times out without SELOGIC control equation setting 79CLS (Reclose Supervision) asserting to logical 1, the relay goes to the Lockout State (see top of Figure 6.3).

Refer to the top of Figure 6.2 in ***Section 6: Close and Reclose Logic***. If timer 79CLSD is set to zero (79CLSD = 0.00), SELOGIC control equation setting 79CLS (Reclose Supervision) is

checked only once to see if it is asserted to logical 1. If it is not asserted to logical 1, the relay goes to the Lockout State.

Refer to the top of Figure 3.26. Ideally, circuit breaker closing is initiated when V_S^* is in phase with V_P (Angle Difference = 0 degrees). Then when the circuit breaker main contacts finally close, V_S is in-phase with V_P , minimizing system shock. But with time limitations imposed by timer 79CLSD, this may not be possible. To try to avoid going to the Lockout State, the following logic is employed:

If 79CLS has not asserted to logical 1 while timer 79CLSD is timing (or timer 79CLSD is set to zero and only one check of 79CLS is made), the synchronism check logic at the bottom of Figure 3.25 becomes less restrictive at the “instant” timer 79CLSD is going to time out (or make the single check). It drops the requirement of waiting until the decreasing Angle Difference (V_S^* approaching V_P) brings V_S^* in phase with V_P (Angle Difference = 0 degrees). Instead, it just checks to see that the Angle Difference is less than angle settings 25ANG1 or 25ANG2.

If the Angle Difference is less than angle setting 25ANG1 or 25ANG2, then the corresponding Relay Word bit, 25A1 or 25A2, asserts to logical 1 for that “instant” (asserts for 1/4 cycle).

For example, if SELOGIC control equation setting 79CLS (Reclose Supervision) is set as follows:

$$79CLS = 25A1 + \dots$$

and the angle difference is less than angle setting 25ANG1 at that “instant,” setting 79CLS asserts to logical 1 for 1/4 cycle, allowing the sealed-in open interval time-out to propagate on to the close logic in Figure 6.1 in **Section 6: Close and Reclose Logic**. Element 25A2 operates similarly.

Synchronism Check Applications for Automatic Reclosing and Manual Closing

Refer to **Close Logic** and **Reclose Supervision Logic** in **Section 6: Close and Reclose Logic**.

For example, set 25ANG1 = 15 degrees and use the resultant synchronism check element in the reclosing relay logic to supervise automatic reclosing:

$$\text{e.g., } 79CLS = 25A1 + \dots \quad (\text{see Figure 6.2})$$

Set 25ANG2 = 25° and use the resultant synchronism check element in manual close logic to supervise manual closing (for example, assert IN106 to initiate manual close):

$$\text{e.g., } CL = IN106 * (25A2 + \dots) \quad (\text{see Figure 6.1})$$

In this example, the angular difference across the circuit breaker can be greater for a manual close (25 degrees) than for an automatic reclose (15 degrees).

A single output contact (e.g., OUT102 = CLOSE) can provide the close function for both automatic reclosing and manual closing (see Figure 6.1 logic output).

FREQUENCY ELEMENTS

Six frequency elements are available. The desired number of frequency elements are enabled with the E81 enable setting:

E81 = N (none), 1 through 6

as shown in Figure 3.28. Frequency is determined from the voltage connected to voltage terminals VA-N.

Frequency Element Settings

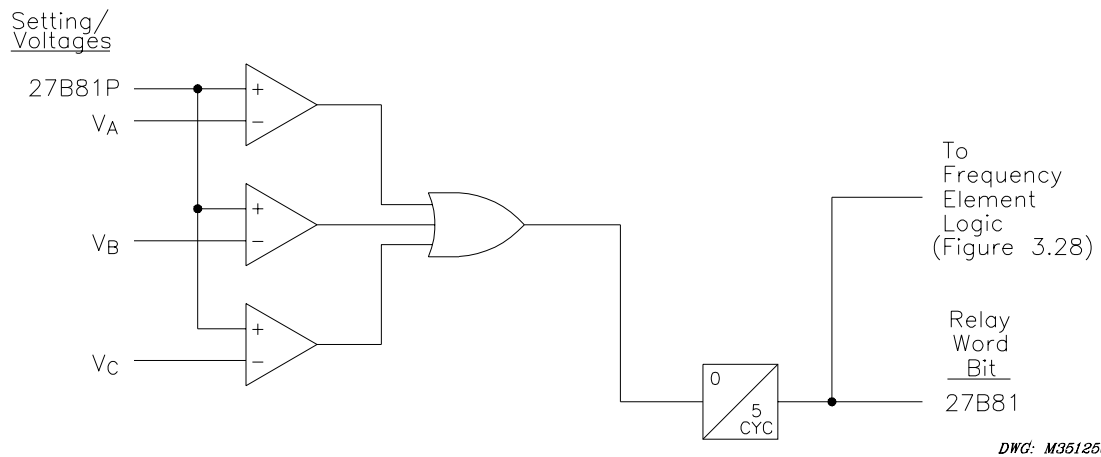


Figure 3.27: Undervoltage Block for Frequency Elements

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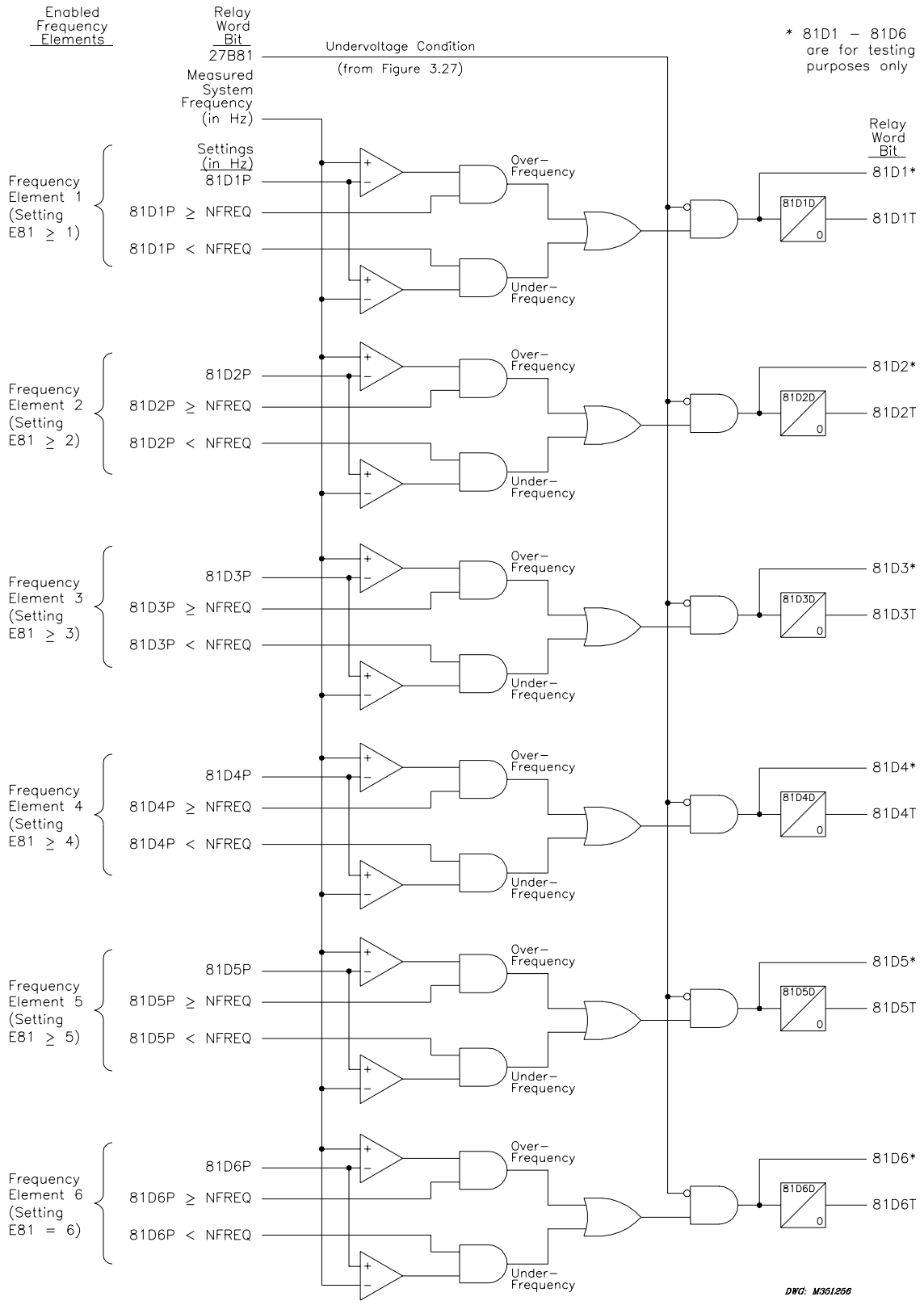


Figure 3.28: Levels 1 Through 6 Frequency Elements

Table 3.10: Frequency Elements Settings and Settings Ranges

Setting	Definition	Range
27B81P	undervoltage frequency element block	12.50–150.00 V secondary (wye-connected voltages, {150 V voltage inputs}) 25.00–300.00 V secondary (wye-connected voltages, {300 V voltage inputs})
81D1P	frequency element 1 pickup	40.10–65.00 Hz
81D1D	frequency element 1 time delay	2.00–16000.00 cycles, in 0.25-cycle steps
81D2P	frequency element 2 pickup	40.10–65.00 Hz
81D2D	frequency element 2 time delay	2.00–16000.00 cycles, in 0.25-cycle steps
81D3P	frequency element 3 pickup	40.10–65.00 Hz
81D3D	frequency element 3 time delay	2.00–16000.00 cycles, in 0.25-cycle steps
81D4P	frequency element 4 pickup	40.10–65.00 Hz
81D4D	frequency element 4 time delay	2.00–16000.00 cycles, in 0.25-cycle steps
81D5P	frequency element 5 pickup	40.10–65.00 Hz
81D5D	frequency element 5 time delay	2.00–16000.00 cycles, in 0.25-cycle steps
81D6P	frequency element 6 pickup	40.10–65.00 Hz
81D6D	frequency element 6 time delay	2.00–16000.00 cycles, in 0.25-cycle steps

Accuracy

Pickup: ±0.01 Hz
 Timer: ±0.25 cycles and ±0.1% of setting

Create Over- and Underfrequency Elements

Refer to Figure 3.28.

Note that pickup settings 81D1P through 81D6P are compared to setting NFREQ. NFREQ is the nominal frequency setting (a global setting), set to 50 or 60 Hz.

Overfrequency Element

For example, make settings:

NFREQ = 60 Hz (nominal system frequency is 60 Hz)
E81 \geq 1 (enable frequency element 1)
81D1P = 61.25 Hz. (frequency element 1 pickup)

With these settings: 81D1P \geq NFREQ

the overfrequency part of frequency element 1 logic is enabled. 81D1 and 81D1T operate as overfrequency elements. 81D1 is used in testing only.

Underfrequency Element

For example, make settings:

NFREQ = 60 Hz (nominal system frequency is 60 Hz)
E81 \geq 2 (enable frequency element 2)
81D2P = 59.65 Hz (frequency element 2 pickup)

With these settings: 81D2P < NFREQ

the underfrequency part of frequency element 2 logic is enabled. 81D2 and 81D2T operate as underfrequency elements. 81D2 is used in testing only.

Frequency Element Operation

Refer to Figure 3.28.

Overfrequency Element Operation

With the previous overfrequency element example settings, if system frequency is less than or equal to 61.25 Hz (81D1P = 61.25 Hz), frequency element 1 outputs:

81D1 = logical 0 (instantaneous element)
81D1T = logical 0 (time delayed element)

If system frequency is greater than 61.25 Hz (81D1P = 61.25 Hz), frequency element 1 outputs:

81D1 = logical 1 (instantaneous element)
81D1T = logical 1 (time delayed element)

Relay Word bit 81D1T asserts to logical 1 only after time delay 81D1D.

Underfrequency Element Operation

With the previous underfrequency element example settings, if system frequency is less than or equal to 59.65 Hz (81D2P = 59.65 Hz), frequency element 2 outputs:

81D2 = logical 1 (instantaneous element)
81D2T = logical 1 (time delayed element)

Relay Word bit 81D2T asserts to logical 1 only after time delay 81D2D.

If system frequency is greater than 59.65 Hz (81D2P = 59.65 Hz), frequency element 2 outputs:

81D2 = logical 0 (instantaneous element)
81D2T = logical 0 (time delayed element)

Frequency Element Voltage Control

Refer to Figure 3.27 and Figure 3.28.

Note that all six frequency elements are controlled by the same undervoltage element (Relay Word bit 27B81). Relay Word bit 27B81 asserts to logical 1 and blocks the frequency element operation if any voltage (V_A , V_B , or V_C) goes below voltage pickup 27B81P. This control prevents erroneous frequency element operation following fault inception.

Other Uses for Undervoltage Element 27B81

If voltage pickup setting 27B81P is applicable to other control schemes, Relay Word bit 27B81 can be used in other logic at the same time it is used in the frequency element logic.

If frequency elements are not being used, Relay Word bit 27B81 can still be used in other logic, with voltage setting 27B81P set as desired. Enable the frequency elements (setting E81 \geq 1) and make setting 27B81P. Apply Relay Word bit 27B81 in desired logic scheme, using SELOGIC control equations. Even though frequency elements are enabled, the frequency element outputs (Relay Word bits 81D1T through 81D6T) do not have to be used.

Frequency Element Uses

The instantaneous frequency elements (81D1 through 81D6) are used in testing only.

The time-delayed frequency elements (81D1T through 81D6T) are used for underfrequency load shedding, frequency restoration, and other schemes.

VOLTAGE SAG, SWELL, AND INTERRUPTION ELEMENTS (AVAILABLE IN FIRMWARE VERSION 7)

The SEL-351-7 Relay has three types of elements to detect voltage disturbances. These elements detect voltage sags, swells, and interruptions (abbreviated as “VSSI” or “SSI”). These elements are enabled by group setting ESSI = Y and controlled by the VINT, VSWELL, and VSAG settings.

Enter the VSSI element threshold settings VSAG, VSWELL, and VINT in percentage units, which relate to the Positive-Sequence Reference Voltage: V_{base} . The use of percentage settings

instead of absolute voltage limits allows the SSI elements to perform better in systems that have a range of nominal voltages, with no need to adjust settings for seasonal loading or to set them far apart to accommodate the action of a tap-changing transformer. The SSI elements respond to phase-neutral voltage quantities.

The Positive-Sequence Reference Voltage is discussed in its own subsection.

The Voltage Sag, Swell, Interruption Recorder automatically uses the SSI elements. These elements are also available as Relay Word bits, so they can be used in any SELOGIC control equation. See *Sag/Swell/Interruption (SSI) Report (Available in Firmware Version 7)* in *Section 12: Standard Event Reports, Sag/Swell/Interruption Report, and SER*.

Voltage Sag Elements

As shown in Figure 3.29, if the magnitude of a phase voltage drops below the voltage sag pickup threshold for one cycle, the corresponding SAG Relay Word bit for that phase asserts (SAGA, SAGB, or SAGC). If all three SAGA, SAGB, and SAGC elements assert, an additional Relay Word bit asserts—SAG3P. The SAG elements remain asserted until the magnitude of the corresponding phase voltage rises and remains above the sag dropout threshold for one cycle.

The sag pickup and dropout thresholds depend on Vbase and the VSAG setting.

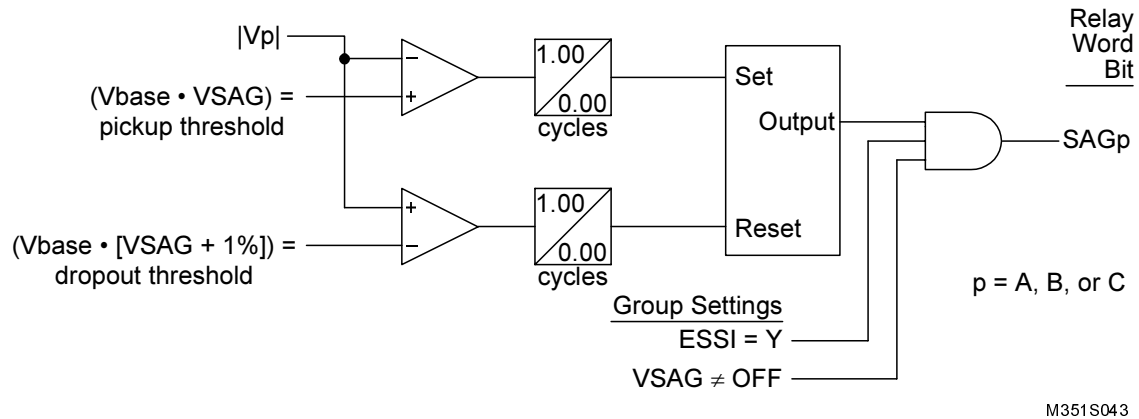
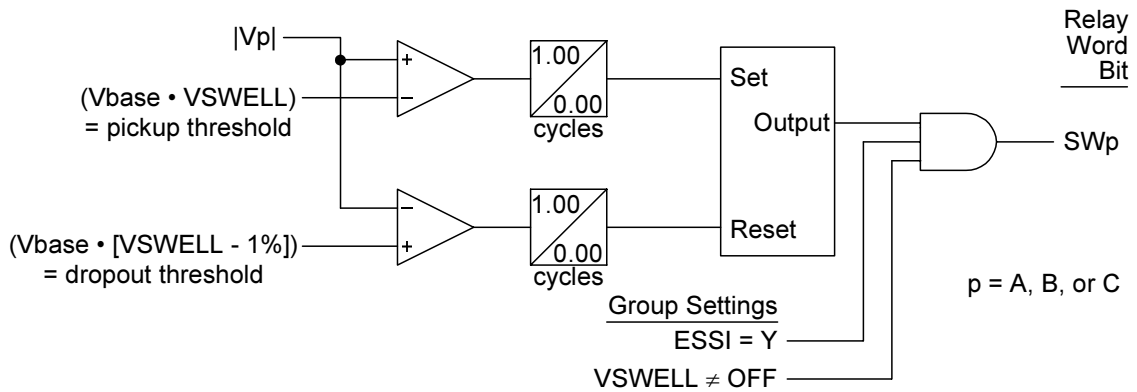


Figure 3.29: Voltage Sag Elements

Voltage Swell Elements

As shown in Figure 3.30, if the magnitude of a phase voltage rises above the voltage swell pickup threshold for one cycle, the corresponding SW Relay Word bit for that phase asserts (SWA, SWB, or SWC). If all three SWA, SWB, and SWC elements assert, an additional Relay Word bit asserts—SW3P. The SW elements remain asserted until the magnitude of the corresponding phase voltage drops and remains below the swell dropout threshold for one cycle.

The swell pickup and dropout thresholds depend on Vbase and the VSWELL setting.



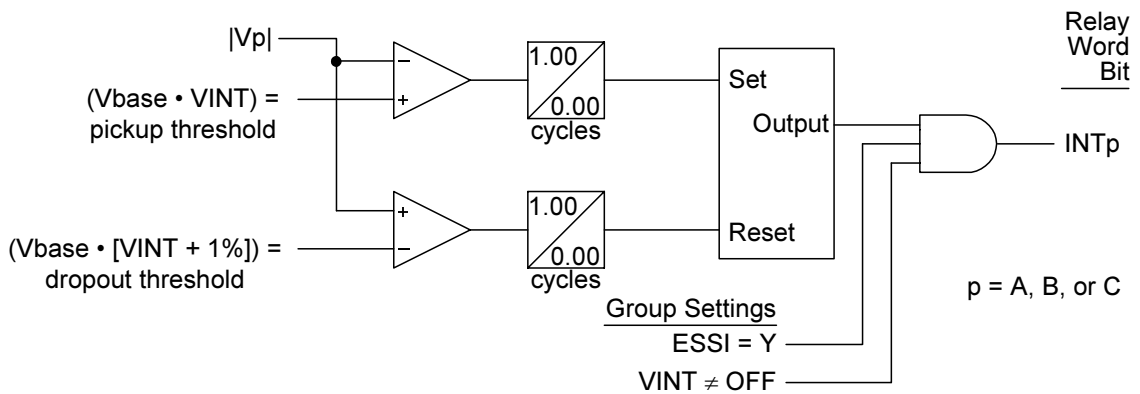
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Figure 3.30: Voltage Swell Elements

Voltage Interruption Elements

As shown in Figure 3.31, if the magnitude of a phase voltage drops below the voltage interruption pickup threshold for one cycle, the corresponding INT Relay Word bit for that phase asserts (INTA, INTB, or INTC). If all three INTA, INTB, and INTC elements assert, an additional Relay Word bit asserts—INT3P. The INT elements remain asserted until the magnitude of the corresponding phase voltage rises and remains above the interruption dropout threshold for one cycle.

The interruption pickup and dropout thresholds depend on Vbase and the VINT setting.



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Figure 3.31: Voltage Interruption Elements

Voltage Sag, Swell, and Interruption Elements Settings

The settings ranges for the SSI thresholds are shown in Table 3.11.

The factory default settings match the Interruption, Sag, and Swell definitions in IEEE Standard 1159-1995 “Classifications of RMS Variations.”

Table 3.11: Sag/Swell/Interruption Elements Settings (must first set ESSI = Y)

Settings	Definition	Range	Default
VINT*	Percentage of memory voltage compared to phase-neutral voltage to assert INT elements	OFF, 5 to 95 percent of positive-sequence reference voltage, Vbase	10.00%
VSAG	Percentage of memory voltage compared to phase-neutral voltage to assert SAG elements	OFF, 10 to 95 percent of positive-sequence reference voltage, Vbase	90.00%
VSWELL	Percentage of memory voltage compared to phase-neutral voltage to assert SW elements	OFF, 105 to 180 percent of positive-sequence reference voltage, Vbase (300 V secondary maximum upper limit)	110.00%

* VINT cannot be set higher than VSAG.

Positive-Sequence Reference Voltage, Vbase

The relay converts the positive-sequence voltage quantity, $|V1|$, to a reference voltage, Vbase, that has a thermal demand characteristic with a time constant of 100 seconds. This allows the Vbase quantity to slowly track normal system voltage variations (tap changer operations and load effects), but not follow fast system voltage changes (unless the change is held for several seconds).

In a balanced three-phase system, $|V1|$ is the average of the three phase voltages.

The present value of Vbase can be viewed by issuing the MET X command. See *MET Command (Metering Data)* in *Section 10: Serial Port Communications and Commands*.

Vbase Thermal Element Block

To prevent the Vbase quantity from tracking during transient voltage conditions, the calculation of the Vbase thermal element is blocked during the assertion of any of the SAGp, SWp, INTp, or FAULT Relay Word bits. When blocked, the Vbase quantity will not change. This allows the SAG, SWELL, and INT elements voltage comparisons to be made with the reference Vbase locked at a “healthy” system voltage level. Once the disturbance is over and all of the SAGp, SWp, INTp, and FAULT Relay Word bits deassert, the thermal element for Vbase is unblocked.

Figure 3.32 shows an example of how Vbase tracking is suspended during a voltage disturbance. The example voltage disturbance is the result of an overload condition (three-phase sag), followed by a source-side breaker operation (three-phase interruption). To illustrate the dynamic nature of the VSSI thresholds, the Interrupt, Sag, and Swell pickup levels are also plotted, using the factory default settings for VINT, VSAG, and VSWELL. For a three-phase disturbance, V1 has the same magnitude as Va, Vb, and Vc (as shown). Single-phase disturbances are handled in a similar fashion, except that the phases and V1 will have different voltage magnitudes.

The use of a VSAG setting higher than 90 percent, at the same time as a VSWELL setting lower than 110 percent, should be carefully considered. Moving these thresholds too close together increases the probability that an end of disturbance condition is missed. This could create a false

sag or swell condition that may not clear itself until the next disturbance, thus causing the Vbase thermal element to remain blocked.

Vbase thermal element blocking by the FAULT Relay Word bit is programmable via SELOGIC setting FAULT. SELOGIC control equation setting FAULT also controls other relay functions, see subsection *SELOGIC Control Equation Setting FAULT* in *Section 5: Trip and Target Logic*.

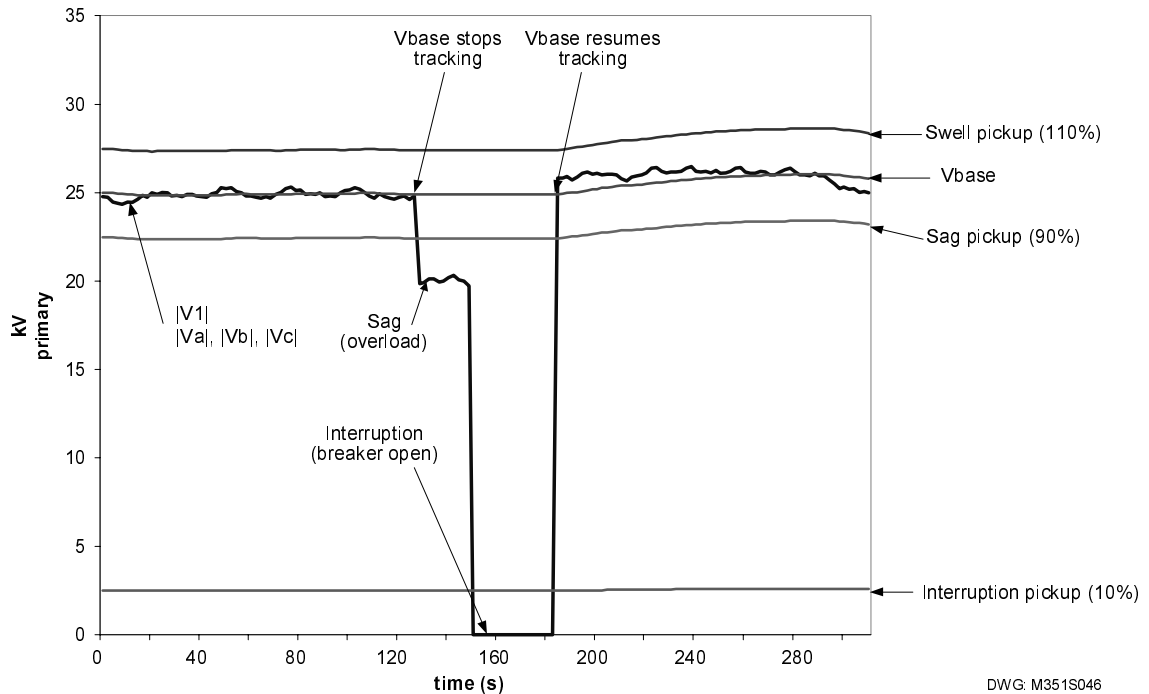


Figure 3.32: Vbase Tracking Example (Three-Phase Disturbance)

Vbase Initialization

The Vbase thermal element is automatically initialized when the relay is powered up, and also after a settings change or group change that results in a new $ESSI = Y$ condition.

Vbase can also be forced to initialize by issuing the **SSI R** command (Access Level 1).

During initialization, the SSI elements are deasserted and the SSI Recorder is disabled until all of the following conditions are met:

- $|V1| > |3V2|$ (correct phase rotation check)
- $|V1| > |3V0|$ (correct phase connection check)
- V_a , V_b , and V_c are all greater than 25 V secondary
- FAULT is deasserted
- $|V1|$ is within three percent of the calculated Vbase value
- At least twelve seconds have elapsed

As soon as the above Vbase initialization conditions are satisfied, the SSI Relay Word bits will be allowed to change state according to their settings and the present voltage conditions, and the SSI Recorder will be enabled.

Vbase Tracking Range

The Vbase quantity will track the positive-sequence voltage over a large range of system voltages. The tracking limits are explained below. In normal relay use, these limits are not likely to be reached, because one of the Sag, Swell, or Interruption Relay Word bits would most likely assert for a large voltage deviation, thus blocking the Vbase thermal element from tracking to one of the range limits.

The minimum value that Vbase can achieve is equivalent to 25 volts secondary, so the minimum Vbase in primary kV is $\frac{25V \cdot PTR}{1000}$.

The maximum value that Vbase can achieve is equivalent to 300 volts secondary divided by VSWELL, so the maximum Vbase in primary kV is $\frac{300V \cdot PTR \cdot 100}{VSWELL \cdot 1000} = \frac{30V \cdot PTR}{VSWELL}$.

SSI Reset command

After commissioning tests or other maintenance activities that have applied test voltages to the SEL-351 Relay, the Vbase element may have locked onto a test voltage. Use the **SSI R** (reset) command once normal system voltages are restored on the voltage terminals. Powering up the relay automatically performs this reset.

See *Reset the SSI Recorder Logic* in *Section 12: Standard Event Reports, Sag/Swell/- Interruption Report, and SER* for more details.

POWER ELEMENTS (AVAILABLE IN FIRMWARE VERSION 7)

Four independent power elements are available. The desired number of power elements is enabled with the EPWR (enable power elements) setting:

EPWR = N (none), 1 through 4.

Each enabled power element operates on a per-phase basis. These per-phase power elements can be set to detect real power or reactive power. With SELOGIC control equations, the power elements provide a wide variety of protection and control applications. Typical applications are:

- Overpower and/or underpower protection/control
- Reverse power protection/control
- VAR control for capacitor banks

Power Elements Settings

Table 3.12: Power Elements Settings and Settings Ranges

Settings	Definition	Range
PWR1P,PWR2P, PWR3P,PWR4P	Power element pickup	OFF, 2.0–13000 VA secondary, single-phase (5A nominal phase current inputs, IA, IB, IC) OFF, 0.4–2600 VA secondary, single-phase (1A nominal phase current inputs, IA, IB, IC)
PWR1T,PWR2T, PWR3T,PWR4T	Power element type	+WATTS, -WATTS, +VARS, -VARS
PWR1D,PWR2D, PWR3D,PWR4D	power element time delay	0.00–16000 cycles, in 0.25-cycle steps

The power element type settings are made in reference to the load convention:

- +WATTS: positive or forward real power
- WATTS: negative or reverse real power
- +VARS: positive or forward reactive power (lagging)
- VARS: negative or reverse reactive power (leading)

Accuracy

Pickup: $\pm 0.025 \text{ A} \cdot (\text{voltage secondary})$ and $\pm 5\%$ of setting at unity power factor (for PWRnT = +WATTS or -WATTS) or power factor = 0 (for PWRnT = +VARS or -VARS)(5A nominal phase current inputs, IA, IB, IC)

$\pm 0.005 \text{ A} \cdot (\text{voltage secondary})$ and $\pm 5\%$ of setting at unity power (for PWRnT = +WATTS or -WATTS) or power factor = 0 (for PWRnT = +VARS or -VARS)(1A nominal phase current inputs, IA, IB, IC)

Timer: ± 0.25 cycles and $\pm 0.1\%$ of setting

Power Elements Logic Operation

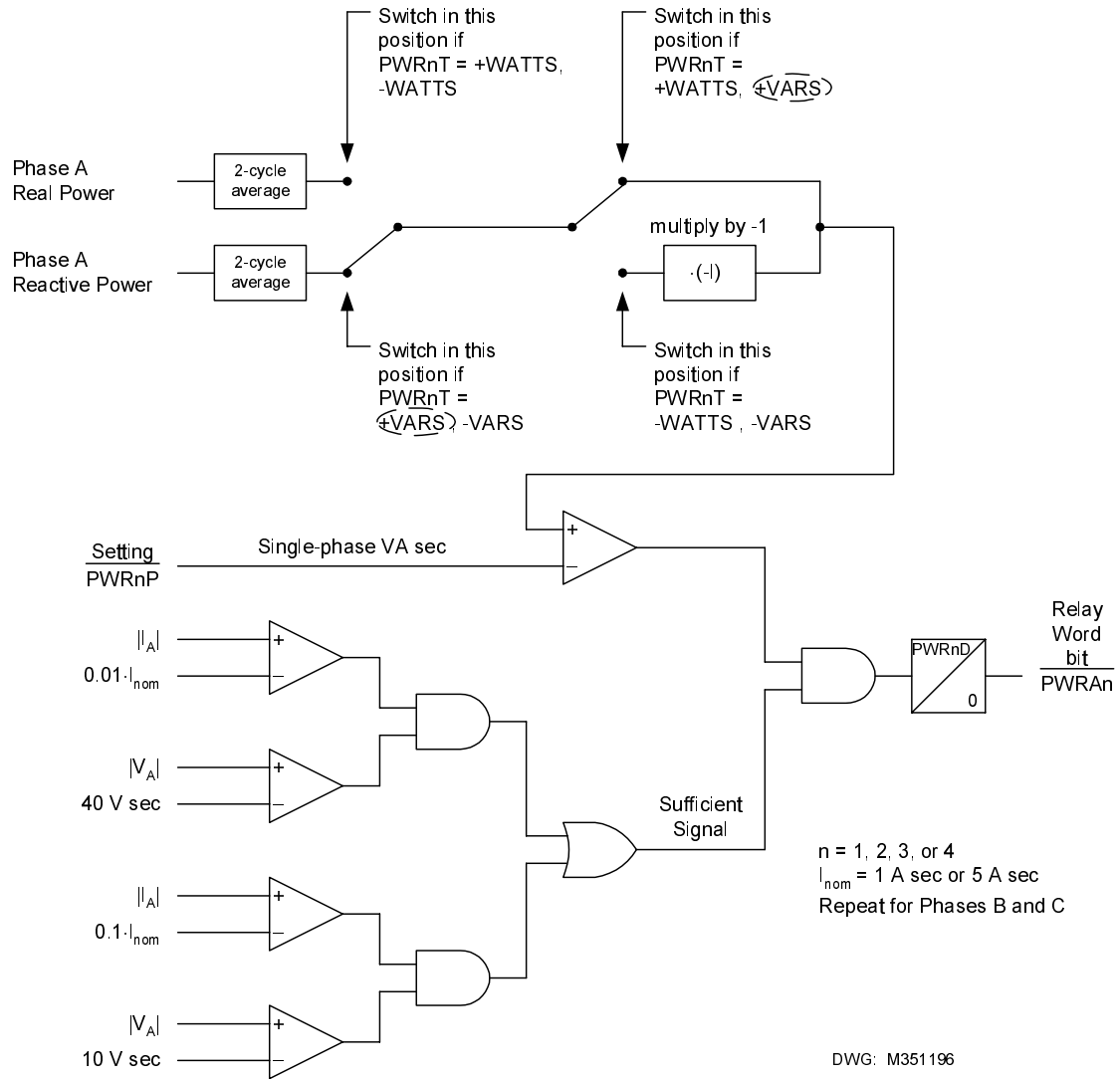
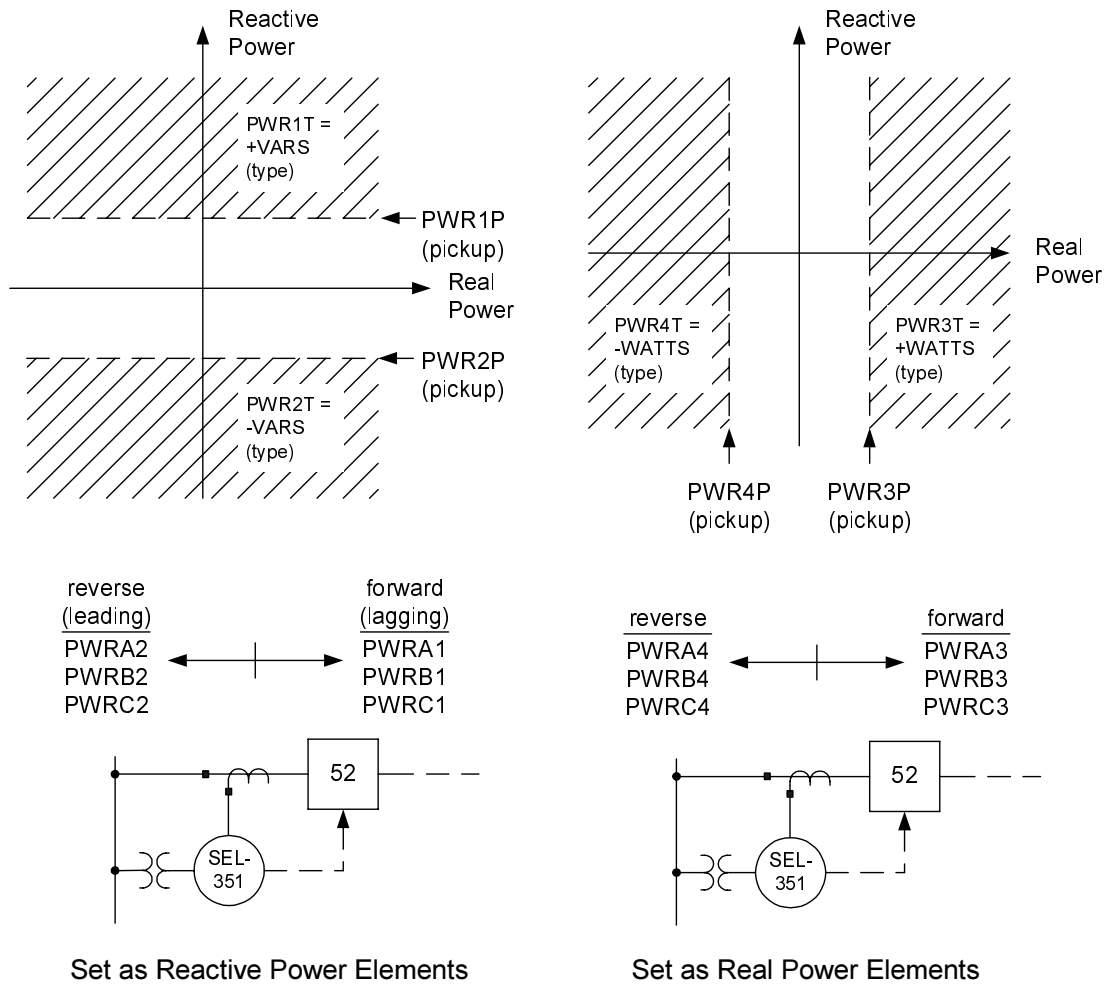


Figure 3.33: Power Elements Logic (+VARS Example Shown)



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Figure 3.34: Power Elements Operation in the Real/Reactive Power Plane

In Figure 3.33, an example is shown with setting $PWRnT = +VARS$. This corresponds to the settings PWR1P (pickup) and PWR1T (type) in Figure 3.2.

In Figure 3.34, if the Phase A reactive power level is above pickup setting PWRnP, Relay Word bit PWRAn asserts ($PWRAn = \text{logical } 1$) after time delay setting PWRnD ($n = 1$ through 4), subject to the “sufficient signal” conditions.

The “sufficient signal” conditions in Figure 3.34 require at least 1 percent nominal current if the corresponding phase voltage is greater than 40 V secondary. If the voltage is between 10 and 40 V secondary, at least 10 percent nominal current is required.

Pickup setting PWRnP is always a positive number value (see Table 3.1). Thus, if -WATTS or -VARS are chosen with setting PWRnT, the corresponding real or reactive power values have to be multiplied by -1 so that element PWRAn asserts for negative real or reactive power.

Power Elements Application—VAR Control for a Capacitor Bank

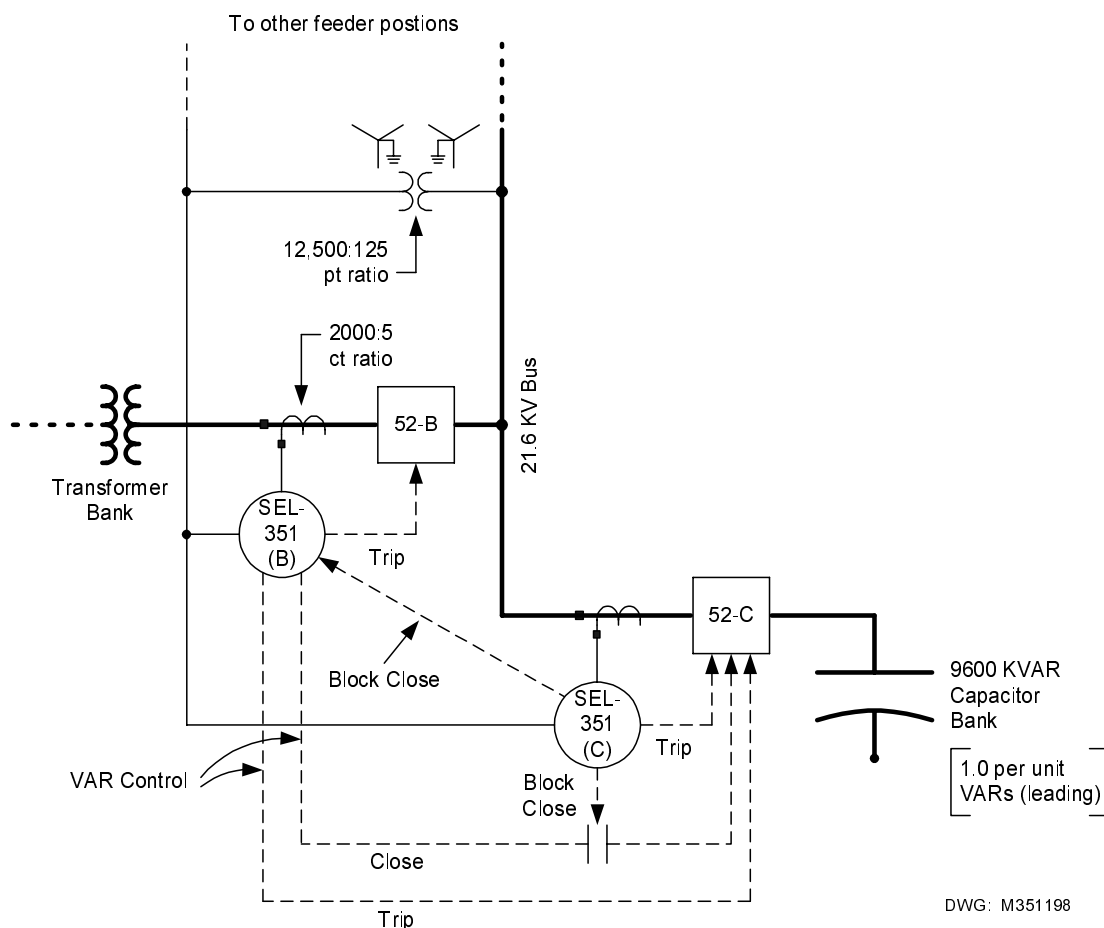


Figure 3.35: SEL-351(B) Relay Provides VAR Control for 9600 kVAR Capacitor Bank

The 9600 kVAR capacitor bank in Figure 3.35 is put on-line and taken off-line according to the VAR loading on the transformer bank feeding the 21.6 kV bus. The VAR loading is measured with the SEL-351(B) Relay located at bus circuit breaker 52-B.

Two SEL-351 Relays control the capacitor bank—both relays are connected to capacitor bank circuit breaker 52-C. The SEL-351(C) Relay provides capacitor overcurrent protection and trips circuit breaker 52-C for a fault in the capacitor bank. The SEL-351(B) Relay provides VAR control and automatically puts the capacitor bank on-line (closes circuit breaker 52-C) or takes it off-line (trips circuit breaker 52-C) according to the measured VAR level. The SEL-351(B) Relay also provides bus overcurrent protection and trips circuit breaker 52-B for a fault on the 21.6 kV bus.

In Figure 3.35, if the SEL-351(C) Relay trips circuit breaker 52-C for a fault in the capacitor bank, then a block close signal is sent from the SEL-351(C) Relay to the SEL-351(B) Relay. This prevents the SEL-351(B) Relay from issuing an automatic close to circuit breaker 52-C.

For additional security, the close circuit from the SEL-351(B) Relay to circuit breaker 52-C is supervised by a block close output contact from the SEL-351(C) Relay. This block close output contact opens if the SEL-351(C) Relay trips circuit breaker 52-C for a fault in the capacitor bank—no automatic closing can then take place.

These block close signals seal in when the SEL-351(C) Relay trips circuit breaker 52-C for a fault in the capacitor bank. Automatic closing of circuit breaker 52-C with the SEL-351(B) Relay can then take place only after the block close signals are reset. The exact implementation of this block close logic requires an application note beyond the scope of this discussion.

The rest of this discussion focuses on the determination of VAR levels (and corresponding power element settings) for automatic tripping and closing of circuit breaker 52-C with the SEL-351(B) Relay.

Convert three-phase 9600 kVAR (kVA) to single-phase VA (voltamperes) secondary:

$$9600 \text{ kVA} / (21.6 \text{ kV} \cdot \sqrt{3}) = 256.6 \text{ A primary}$$

$$256.6 \text{ A primary} \cdot (5/2000) = 0.64 \text{ A secondary}$$

$$0.64 \text{ A secondary} \cdot 125 \text{ V secondary} = 80.0 \text{ VA secondary (single-phase)}$$

The three-phase 9600 kVAR capacitor is corresponded to 1.0 per unit VARs (leading) for demonstration convenience in Figure 3.35. Figure 3.36 shows the per unit VAR levels for putting on-line (closing circuit breaker 52-C) or taking off-line (tripping circuit breaker 52-C) the capacitor bank.

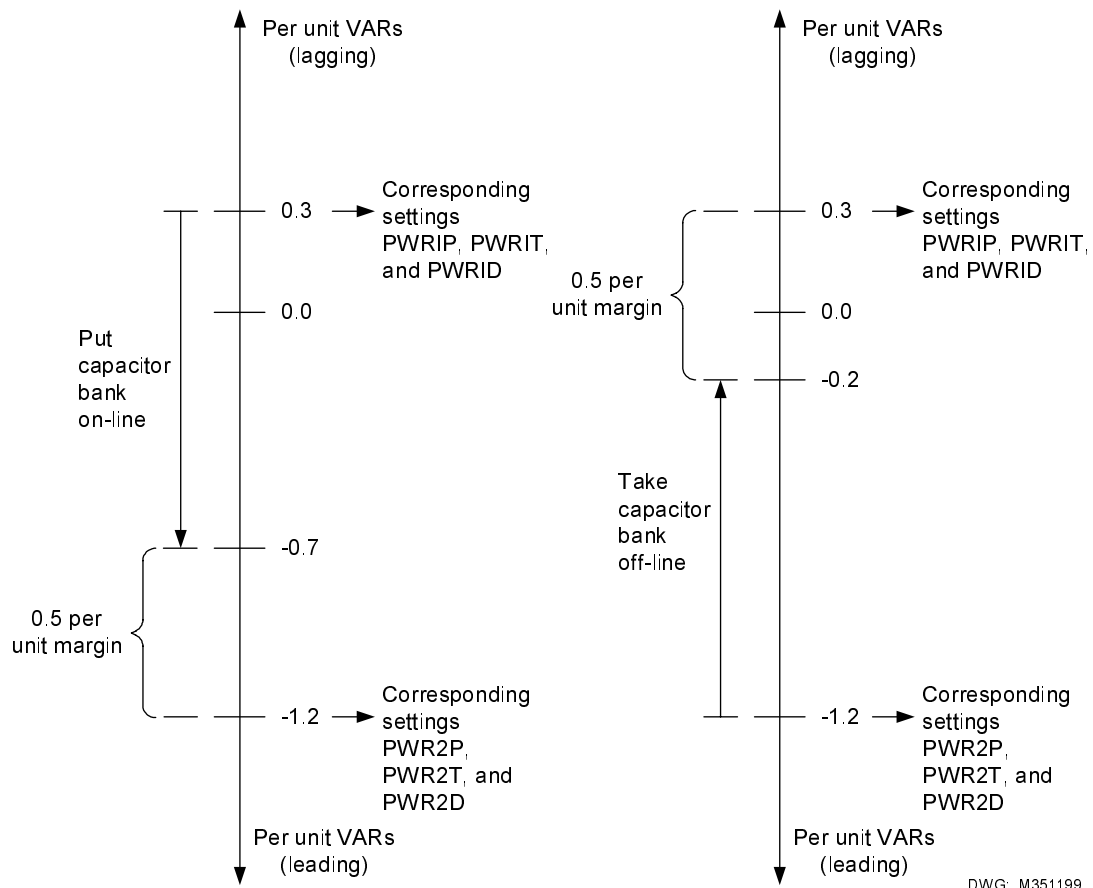


Figure 3.36: Per Unit Setting Limits for Switching 9600 kVAR Capacitor Bank On- and Off-Line

The capacitor bank is put on-line at the 0.3 per unit VAR level (lagging) on the bus. The per unit VAR level immediately changes to the -0.7 per unit VAR level (leading) when the capacitor bank is put on-line ($0.3 - 1.0 = -0.7$). There is a margin of 0.5 per unit VARs until the capacitor bank is then taken off-line ($-0.7 - 0.5 = -1.2$).

The capacitor bank is taken off-line at the -1.2 per unit VAR level (leading) on the bus. The per unit VAR level immediately changes to -0.2 per unit VAR level (leading) when the capacitor bank is taken off-line ($-1.2 + 1.0 = -0.2$). There is a margin of 0.5 per unit VARs until the capacitor bank is put on-line again ($-0.2 + 0.5 = 0.3$).

From preceding calculations and figures:

$$9600 \text{ kVAR} \approx 1.0 \text{ per unit VARs} \approx 80.0 \text{ VA secondary (single-phase)}$$

Convert the per unit VAR levels 0.3 and -1.2 to single-phase VA (voltamperes) secondary:

$$0.3 \cdot 80.0 \text{ VA secondary (single-phase)} = 24.0 \text{ VA secondary (single-phase)}$$

$$-1.2 \cdot 80.0 \text{ VA secondary (single-phase)} = -96.0 \text{ VA secondary (single-phase)}$$

Make the following power element settings for the SEL-351(B) Relay:

EPWR	= 2	(enable two power elements)
PWR1P	= 24.0	(power element pickup; VA secondary [single-phase])
PWR1T	= +VARs	(power element type; lagging VARs)
PWR1D	= _____	(power element time delay; cycles)
PWR2P	= 96.0	(power element pickup; VA secondary [single-phase])
PWR2T	= -VARs	(power element type; leading VARs)
PWR2D	= _____	(power element time delay; cycles)

To override transient reactive power conditions, set the above power element time delay settings equivalent to several seconds (or perhaps minutes).

Resulting single-phase power elements PWRA1, PWRB1, and PWRC1 assert when the lagging VAR level exceeds the 0.3 per unit VAR level (lagging) for each respective phase (see Figure 3.36 and left-hand side of Figure 3.34). These elements are used in close logic in the SEL-351(B) Relay to automatically put the 9600 kVAR capacitor bank on-line.

Resulting single-phase power elements PWRA2, PWRB2, and PWRC2 assert when the leading VAR level exceeds the -1.2 per unit VAR level (leading) for each respective phase (see Figure 3.36 and left-hand side of Figure 3.34). These elements are used in trip logic in the SEL-351(B) Relay to automatically take the 9600 kVAR capacitor bank off-line.

The exact implementation of this capacitor close and trip logic in SELOGIC control equations in the SEL-351(B) Relay requires an application note beyond the scope of this discussion.

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SECTION 4: LOSS-OF-POTENTIAL, LOAD ENCROACHMENT, AND DIRECTIONAL ELEMENT LOGIC

LOSS-OF-POTENTIAL LOGIC

The loss-of-potential (LOP) logic operates as shown in Figure 4.1.

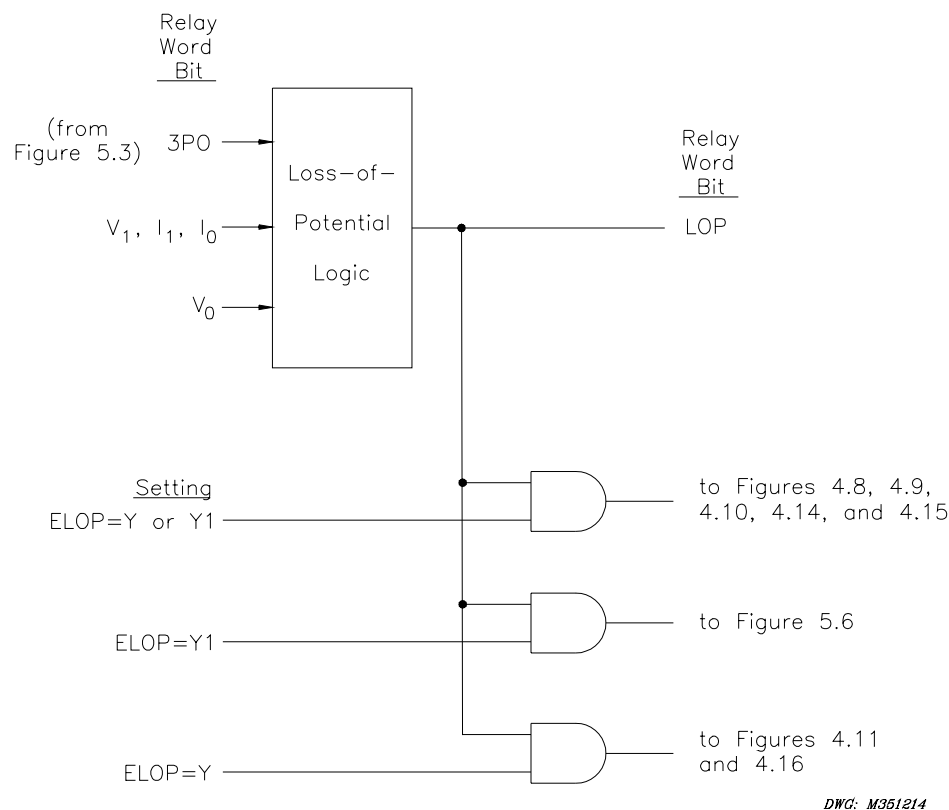


Figure 4.1: Loss-of-Potential Logic

Inputs into the LOP logic are:

- 3PO three-pole open condition (indicates circuit breaker open condition see Figure 5.3)
- V_1 positive-sequence voltage (V secondary)
- I_1 positive-sequence current (A secondary)
- V_0 zero-sequence voltage (V secondary)
- I_0 zero-sequence current (A secondary)
- V_2 negative-sequence voltage (V secondary)

The circuit breaker has to be closed (Relay Word bit 3PO = logical 0) for the LOP logic to operate.

Loss-of-potential is declared (Relay Word bit LOP = logical 1) when a 10% drop in V_1 is detected, with no corresponding change in I_1 or I_0 . If the LOP condition persists for 60 cycles, it latches in. LOP resets (Relay Word bit LOP = logical 0) when V_1 returns above 50 V secondary and

- V_0 is less than 5 V secondary (150 V voltage inputs).
 V_0 is less than 10 V secondary (300 V voltage inputs).

The loss-of-potential enable setting, ELOP, does not enable or disable the LOP logic. It just routes the LOP Relay Word bit to different logic, as shown in Figure 4.1 and explained in the remainder of this subsection.

Setting ELOP = Y or Y1

If setting ELOP = Y or Y1 and a loss-of-potential condition occurs (Relay Word bit LOP asserts to logical 1), negative-sequence voltage-polarized, zero-sequence voltage-polarized, and positive-sequence voltage-polarized directional elements are disabled (see Figure 4.8, Figure 4.9, Figure 4.14, and Figure 4.15). The loss-of-potential condition makes these voltage-polarized directional elements unreliable. Thus, they are disabled. The overcurrent elements controlled by these voltage-polarized directional elements are disabled also (unless overridden by conditions explained in the following Setting ELOP = Y discussion).

In Figure 4.10, the assertion of LOP is an additional enable for the channel IN current-polarized directional element. This directional element is not voltage polarized.

In Figure 5.6, if setting ELOP = Y1 and LOP asserts, keying and echo keying in the permissive overreaching transfer trip (POTT) logic are blocked.

Setting ELOP = Y

Additionally, if setting ELOP = Y and a loss-of-potential condition occurs (Relay Word bit LOP asserts to logical 1), overcurrent elements set direction forward are enabled (see Figure 4.11 and Figure 4.16). These direction forward overcurrent elements effectively become nondirectional and provide overcurrent protection during a loss-of-potential condition.

As detailed previously, voltage-based directional elements are disabled during a loss-of-potential condition. Thus, the overcurrent elements controlled by these voltage-based directional elements are also disabled. But this disable condition is overridden for the overcurrent elements set direction forward if setting ELOP = Y.

Setting ELOP = N

If setting ELOP = N, the loss-of-potential logic still operates (Relay Word bit LOP asserts to logical 1 for a loss-of-potential condition) but does not disable any voltage-based directional elements (as occurs with ELOP = Y or Y1) or enable overcurrent elements set direction forward (as occurs with ELOP = Y).

LOAD-ENCROACHMENT LOGIC

The load-encroachment logic (see Figure 4.2) and settings are enabled/disabled with setting ELOAD (= Y or N).

The load-encroachment feature allows phase overcurrent elements to be set independent of load levels. This is especially helpful in bus overcurrent applications. A bus relay sees the cumulative currents of all the feeders but still has to provide overcurrent backup protection for all these feeders. If the phase elements in the bus relay are set to provide adequate backup, they often are set close to maximum bus load current levels. This runs the risk of tripping on bus load current. The load-encroachment feature prevents this from happening as shown in the example that follows in this subsection.

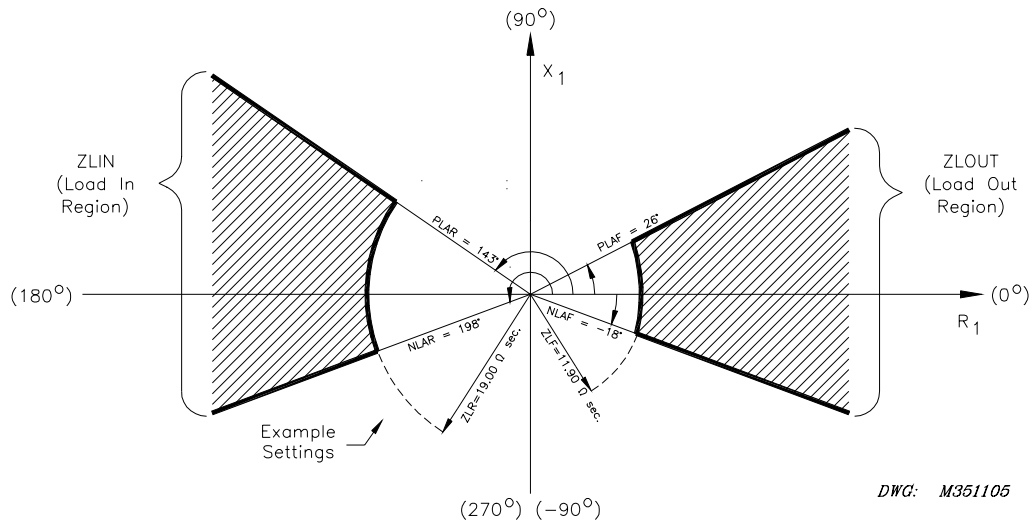
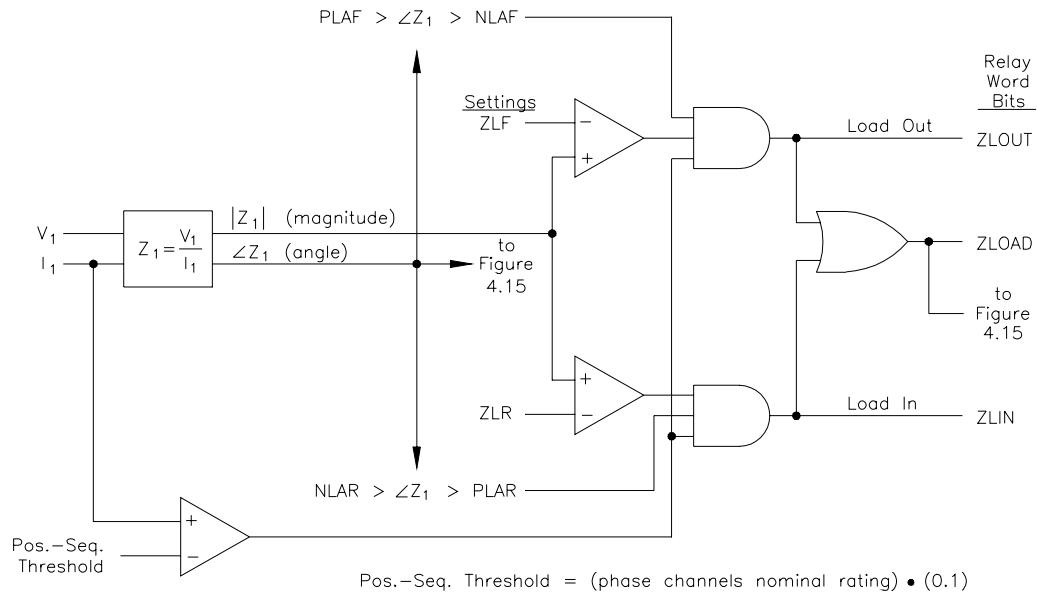


Figure 4.2: Load-Encroachment Logic

Note that a positive-sequence impedance calculation (Z_1) is made in the load-encroachment logic in Figure 4.2. Load is largely a balanced condition, so apparent positive-sequence impedance is a good load measure. The load-encroachment logic only operates if the positive-sequence current (I_1) is greater than the Positive-Sequence Threshold defined in Figure 4.2. For a balanced load condition, $I_1 =$ phase current magnitude.

Forward load (load flowing out) lies within the hatched region labeled ZLOUT. Relay Word bit ZLOUT asserts to logical 1 when the load lies within this hatched region.

Reverse load (load flowing in) lies within the hatched region labeled ZLIN. Relay Word bit ZLIN asserts to logical 1 when the load lies within this hatched region.

Relay Word bit ZLOAD is the OR-combination of ZLOUT and ZLIN:

$$ZLOAD = ZLOUT + ZLIN$$

Settings Ranges

Refer to Figure 4.2.

Setting Description and Range

ZLF	Forward Minimum Load Impedance—corresponding to maximum load flowing out
ZLR	Reverse Minimum Load Impedance—corresponding to maximum load flowing in
	0.05–64.00 Ω secondary (5 A nominal phase current inputs, IA, IB, IC) {150 V voltage inputs}
	0.10–128.00 Ω secondary (5 A nominal phase current inputs, IA, IB, IC) {300 V voltage inputs}
	0.25–320.00 Ω secondary (1 A nominal phase current inputs, IA, IB, IC) {150 V voltage inputs}
	0.50–640.00 Ω secondary (1 A nominal phase current inputs, IA, IB, IC) {300 V voltage inputs}
PLAF	Maximum Positive Load Angle Forward (-90° to +90°)
NLAF	Maximum Negative Load Angle Forward (-90° to +90°)
PLAR	Maximum Positive Load Angle Reverse (+90° to +270°)
NLAR	Maximum Negative Load Angle Reverse (+90° to +270°)

Load-Encroachment Setting Example

Example system conditions:

Nominal Line-Line Voltage:	230 kV
Maximum Forward Load:	800 MVA
Maximum Reverse Load:	500 MVA
Power Factor (Forward Load):	0.90 lag to 0.95 lead
Power Factor (Reverse Load):	0.80 lag to 0.95 lead
CT ratio:	2000/5 = 400
PT ratio:	134000/67 = 2000

The PTs are connected line-to-neutral.

Convert Maximum Loads to Equivalent Secondary Impedances

Start with maximum forward load:

$$800 \text{ MVA} \cdot (1/3) = 267 \text{ MVA per phase}$$

$$230 \text{ kV} \cdot (1/\sqrt{3}) = 132.8 \text{ kV line-to-neutral}$$

$$267 \text{ MVA} \cdot (1/132.8 \text{ kV}) \cdot (1000\text{kV/MV}) = 2010 \text{ A primary}$$

$$2010 \text{ A primary} \cdot (1/\text{CT ratio}) = 2010 \text{ A primary} \cdot (1 \text{ A secondary}/400 \text{ A primary}) \\ = 5.03 \text{ A secondary}$$

$$132.8 \text{ kV} \cdot (1000 \text{ V/kV}) = 132800 \text{ V primary}$$

$$132800 \text{ V primary} \cdot (1/\text{PT ratio}) = 132800 \text{ V primary} \cdot (1 \text{ V secondary}/2000 \text{ V primary}) \\ = 66.4 \text{ V secondary}$$

Now, calculate the equivalent secondary impedance:

$$66.4 \text{ V secondary}/5.03 \text{ A secondary} = 13.2 \Omega \text{ secondary}$$

This Ω secondary value can be calculated more expediently with the following equation:

$$[(\text{line-line voltage in kV})^2 \cdot (\text{CT ratio})]/[(3\text{-phase load in MVA}) \cdot (\text{PT ratio})]$$

Again, for the maximum forward load:

$$[(230)^2 \cdot (400)]/[(800) \cdot (2000)] = 13.2 \Omega \text{ secondary}$$

To provide a margin for setting ZLF, multiply by a factor of 0.9:

$$\text{ZLF} = 13.2 \Omega \text{ secondary} \cdot 0.9 = 11.90 \Omega \text{ secondary}$$

For the maximum reverse load:

$$[(230)^2 \cdot (400)]/[(500) \cdot (2000)] = 21.1 \Omega \text{ secondary}$$

Again, to provide a margin for setting ZLR:

$$\text{ZLR} = 21.1 \Omega \text{ secondary} \cdot 0.9 = 19.00 \Omega \text{ secondary}$$

Convert Power Factors to Equivalent Load Angles

The power factor (forward load) can vary from 0.90 lag to 0.95 lead.

$$\text{Setting PLAF} = \cos^{-1}(0.90) = 26^\circ$$

$$\text{Setting NLAF} = \cos^{-1}(0.95) = -18^\circ$$

The power factor (reverse load) can vary from 0.80 lag to 0.95 lead.

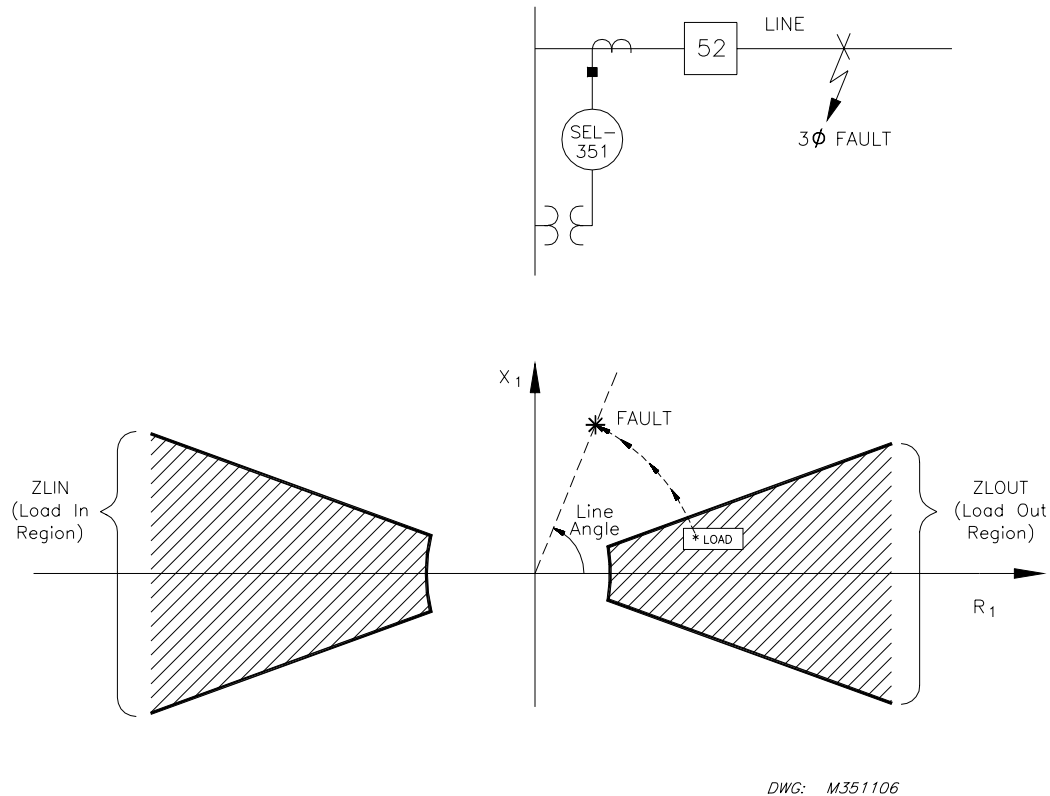
$$\text{Setting PLAR} = 180^\circ - \cos^{-1}(0.80) = 180^\circ - 37^\circ = 143^\circ$$

$$\text{Setting NLAR} = 180^\circ + \cos^{-1}(0.95) = 180^\circ + 18^\circ = 198^\circ$$

Apply Load-Encroachment Logic to a Phase Time-Overcurrent

Again, from Figure 4.2:

$$Z_{LOAD} = Z_{LOUT} + Z_{LIN}$$



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Figure 4.3: Migration of Apparent Positive-Sequence Impedance for a Fault Condition

Refer to Figure 4.3. In a load condition, the apparent positive-sequence impedance is within the ZLOUT area, resulting in:

$$Z_{LOAD} = Z_{LOUT} + Z_{LIN} = \text{logical 1} + Z_{LIN} = \text{logical 1}$$

If a fault occurs, the apparent positive-sequence impedance moves outside the ZLOUT area (and stays outside the ZLIN area, too), resulting in:

$$Z_{LOAD} = Z_{LOUT} + Z_{LIN} = \text{logical 0} + \text{logical 0} = \text{logical 0}$$

Refer to Figure 3.14 in *Section 3: Overcurrent, Voltage, Synchronism Check, Frequency, and Power Elements*. To prevent phase time-overcurrent element 51PT from operating for high load conditions, make the following SELOGIC[®] control equation torque control setting:

$$51PTC = !Z_{LOAD} * !LOP + 50P6 \quad (= \text{NOT}[Z_{LOAD}] * \text{NOT}[LOP] + 50P6)$$

As shown in Figure 4.2, load-encroachment logic is a positive-sequence calculation. During LOP conditions (loss-of-potential; see Figure 4.1), positive-sequence voltage (V_1) can be substantially depressed in magnitude or changed in angle. This change in V_1 can possibly cause ZLOAD to deassert (= logical 0), erroneously indicating that a “fault condition” exists. Thus, !ZLOAD should be supervised by !LOP in a torque control setting. This also effectively happens in the directional element in Figure 4.15, where ZLOAD and LOP are part of the logic.

In the above setting example, phase instantaneous overcurrent element 50P6 is set above any maximum load current level—if 50P6 picks up, there is assuredly a fault. For faults below the pickup level of 50P6, but above the pickup of phase time-overcurrent element 51PT, the !ZLOAD*!LOP logic discriminates between high load and fault current. If an LOP condition occurs (LOP = logical 1), the pickup level of 50P6 becomes the effective pickup of phase time-overcurrent element 51PT (51PT loses its sensitivity when an LOP condition occurs):

$$\begin{aligned} 51PTC &= !ZLOAD*!LOP + 50P6 = !ZLOAD*NOT[LOP] + 50P6 \\ &= !ZLOAD*NOT[logical 1] + 50P6 = 50P6 \end{aligned}$$

Use SEL-321 Relay Application Guide for the SEL-351 Relay

The load-encroachment logic and settings in the SEL-351 Relay are the same as those in the SEL-321 Relay. Refer to *Application Guide 93-10 (SEL-321 Relay Load-Encroachment Function Setting Guidelines)* for applying the load-encroachment logic in the SEL-351 Relay. Note that *Application Guide AG93-10* discusses applying the load-encroachment feature to phase distance elements in the SEL-321 Relay. The SEL-351 Relay doesn't have phase distance elements, but the principles and settings example are still applicable to the SEL-351 Relay.

DIRECTIONAL CONTROL FOR NEUTRAL GROUND AND RESIDUAL GROUND OVERCURRENT ELEMENTS

The directional control for overcurrent elements is enabled by making directional control enable setting E32. Setting E32 and other directional control settings are described in the following subsection *Directional Control Settings*.

Three directional elements are available to control the neutral ground and residual ground overcurrent elements. These three directional elements are:

- Negative-sequence voltage-polarized directional element
- Zero-sequence voltage-polarized directional element
- Channel IN current-polarized directional element

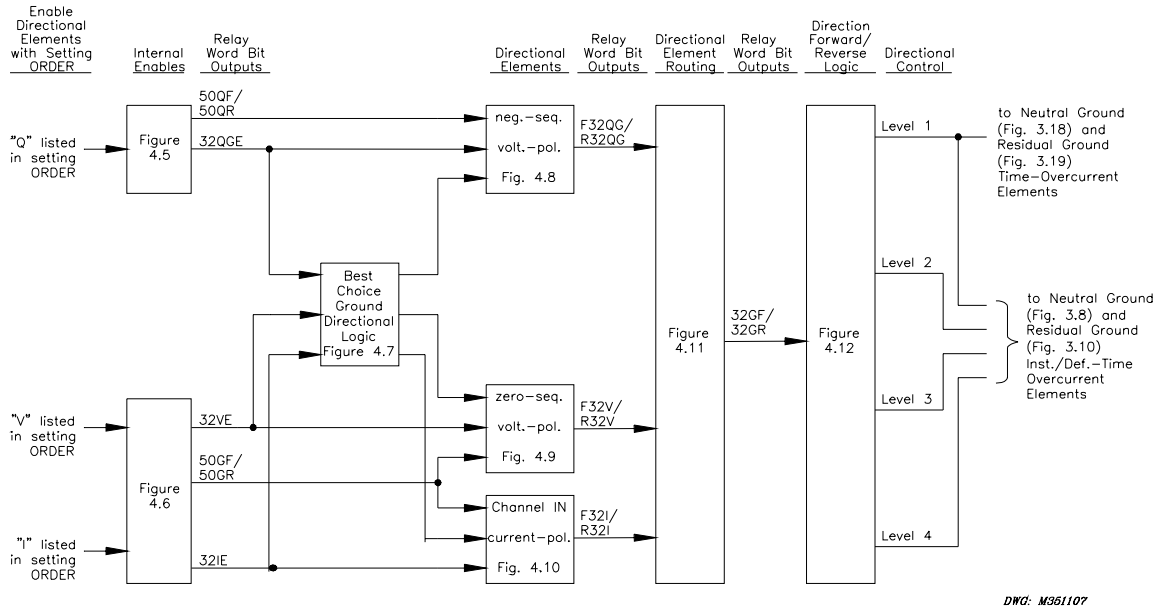


Figure 4.4: General Logic Flow of Directional Control for Neutral Ground and Residual Ground Overcurrent Elements

Figure 4.4 gives an overview of how these directional elements are enabled and routed to control the neutral ground and residual ground overcurrent elements.

Note in Figure 4.4 that setting ORDER enables the directional elements. Setting ORDER can be set with any combination of Q, V, and I. They have the following correspondence to the directional elements:

- Q Negative-sequence voltage-polarized directional element
- V Zero-sequence voltage-polarized directional element
- I Channel IN current-polarized directional element

The order in which these directional elements are listed in setting ORDER determines the priority in which they operate to provide *Best Choice Ground Directional*TM logic control. See discussion on setting ORDER in the following subsection *Directional Control Settings*.

Note 1: If channel IN is rated 0.05 A nominal, then setting option “I” is not available for setting ORDER. This results in internal enable 32IE defaulting to logical 0 at the bottom of Figure 4.6. The channel IN current-polarized directional element that follows in Figure 4.10 is defeated and nonoperational when internal enable 32IE = logical 0.

Thus, the channel IN current-polarized directional element in Figure 4.10 is defeated, nonoperational, and unavailable when channel IN is rated 0.05 A nominal.

Internal Enables

Refer to Figure 4.4, Figure 4.5, and Figure 4.6.

The internal enables 32QGE, 32VE, and 32IE have the following correspondence to the directional elements:

32QGE	Negative-sequence voltage-polarized directional element
32VE	Zero-sequence voltage-polarized directional element
32IE	Channel IN current-polarized directional element

Note that Figure 4.5 has extra internal enable 32QE, which is used in the directional element logic that controls negative-sequence and phase overcurrent elements (see Figure 4.13).

The settings involved with internal enables 32QGE, 32VE, and 32IE in Figure 4.5 and Figure 4.6 (e.g., settings a2, k2, a0) are explained in the following subsection *Directional Control Settings*.

Best Choice Ground Directional Logic

Refer to Figure 4.4 and Figure 4.7.

The internal enables 32QGE, 32VE, and 32IE and setting ORDER are used in the *Best Choice Ground Directional* logic in Figure 4.7. The *Best Choice Ground Directional* logic determines which directional element should be enabled to operate. The neutral ground and residual ground overcurrent elements set for directional control are then controlled by this enabled directional element.

Directional Elements

Refer to Figure 4.4, Figure 4.8, Figure 4.9, and Figure 4.10.

The enable output of *Best Choice Ground Directional* logic in Figure 4.7 determines which directional element will run.

Additionally, note if enable setting ELOP = Y or Y1 and a loss-of-potential condition occurs (Relay Word bit LOP asserts), the negative-sequence voltage-polarized and zero-sequence voltage-polarized directional elements are disabled (see Figure 4.8 and Figure 4.9).

The channel IN current-polarized directional element does not use voltage in making direction decisions, thus a loss-of-potential condition does not disable the element, but rather aids in enabling it. When the internal enable 32IE is asserted, the channel IN current-polarized directional element (Figure 4.10) is enabled if enable setting ELOP = Y or Y1 and a loss-of-potential condition occurs (Relay Word bit LOP asserts).

Refer to Figure 4.1 and accompanying text for more information on loss-of-potential.

Directional Element Routing

Refer to Figure 4.4 and Figure 4.11.

The directional element outputs are routed to the forward (Relay Word bit 32GF) and reverse (Relay Word bit 32GR) logic points and then on to the direction forward/reverse logic in Figure 4.12.

Loss-of-Potential

Note if all the following are true:

- Enable setting ELOP = Y,
- A loss-of-potential condition occurs (Relay Word bit LOP asserts),
- And internal enable 32IE (for channel IN current-polarized directional element) is not asserted

then the forward logic point (Relay Word bit 32GF) asserts to logical 1, thus, enabling the neutral ground and residual ground overcurrent elements that are set direction forward (with settings DIR1 = F, DIR2 = F, etc.). These direction forward overcurrent elements effectively become nondirectional and provide overcurrent protection during a loss-of-potential condition.

As detailed previously (in Figure 4.8 and Figure 4.9), voltage-based directional elements are disabled during a loss-of-potential condition. Thus, the overcurrent elements controlled by these voltage-based directional elements are disabled also. But this disable condition is overridden for the overcurrent elements set direction forward if setting ELOP = Y.

Refer to Figure 4.1 and accompanying text for more information on loss-of-potential.

Direction Forward/Reverse Logic

Refer to Figure 4.4 and Figure 4.12.

The forward (Relay Word bit 32GF) and reverse (Relay Word bit 32GR) logic points are routed to the different levels of overcurrent protection by the level direction settings DIR1 through DIR4.

Table 4.1 shows the overcurrent elements that are controlled by each level direction setting. Note in Table 4.1 that all the time-overcurrent elements (51_T elements) are controlled by the DIR1 level direction setting.

In most communications-assisted trip schemes, the levels are set as follows (see Figure 5.4):

- Level 1 overcurrent elements set direction forward (DIR1 = F)
- Level 2 overcurrent elements set direction forward (DIR2 = F)
- Level 3 overcurrent elements set direction reverse (DIR3 = R)

If a level direction setting (e.g., DIR1) is set:

DIR1 = N (nondirectional)

then the corresponding Level 1 directional control output in Figure 4.12 asserts to logical 1. The referenced Level 1 overcurrent elements in Figure 4.12 are then not controlled by the directional control logic.

See the beginning of following subsection *Directional Control Settings* for discussion of the operation of level direction settings DIR1 through DIR4 when the directional control enable setting E32 is set to E32 = N.

In some applications, level direction settings DIR1 through DIR4 are not flexible enough in assigning the desired direction for certain overcurrent elements. Subsection *Directional Control*

Provided by Torque Control Settings at the end of this section describes how to avoid this limitation for special cases.

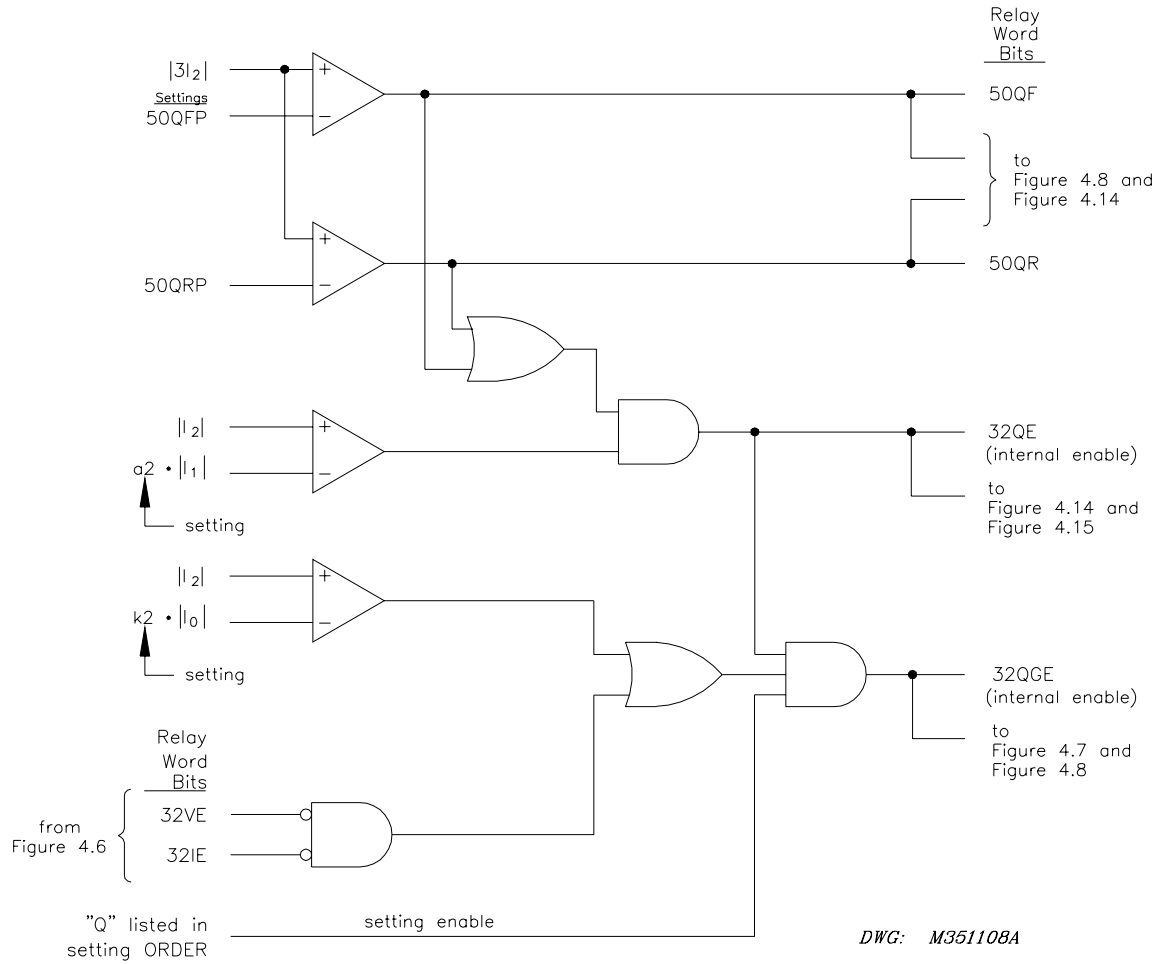


Figure 4.5: Internal Enables (32QE and 32QGE) Logic for Negative-Sequence Voltage-Polarized Directional Elements

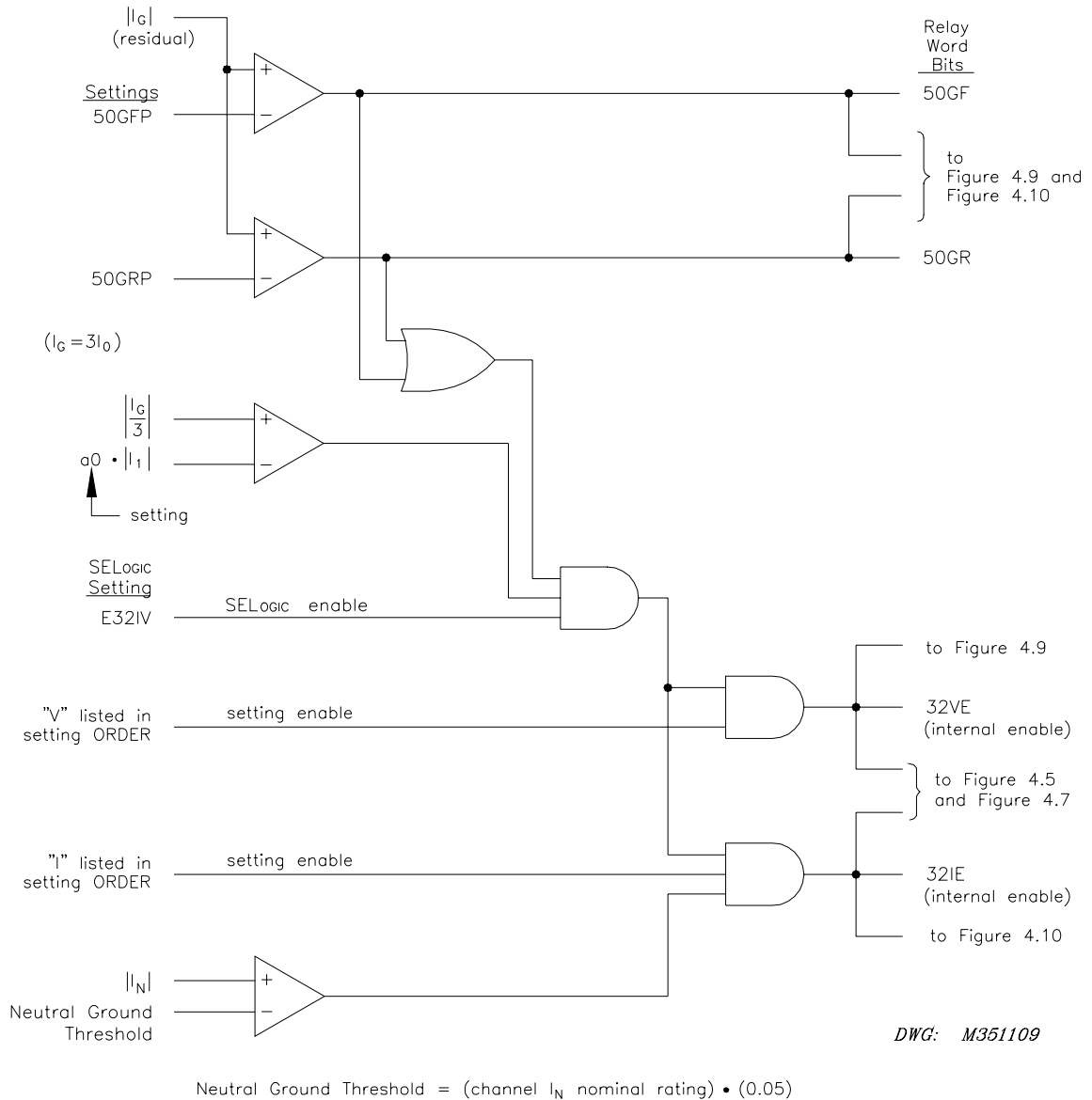
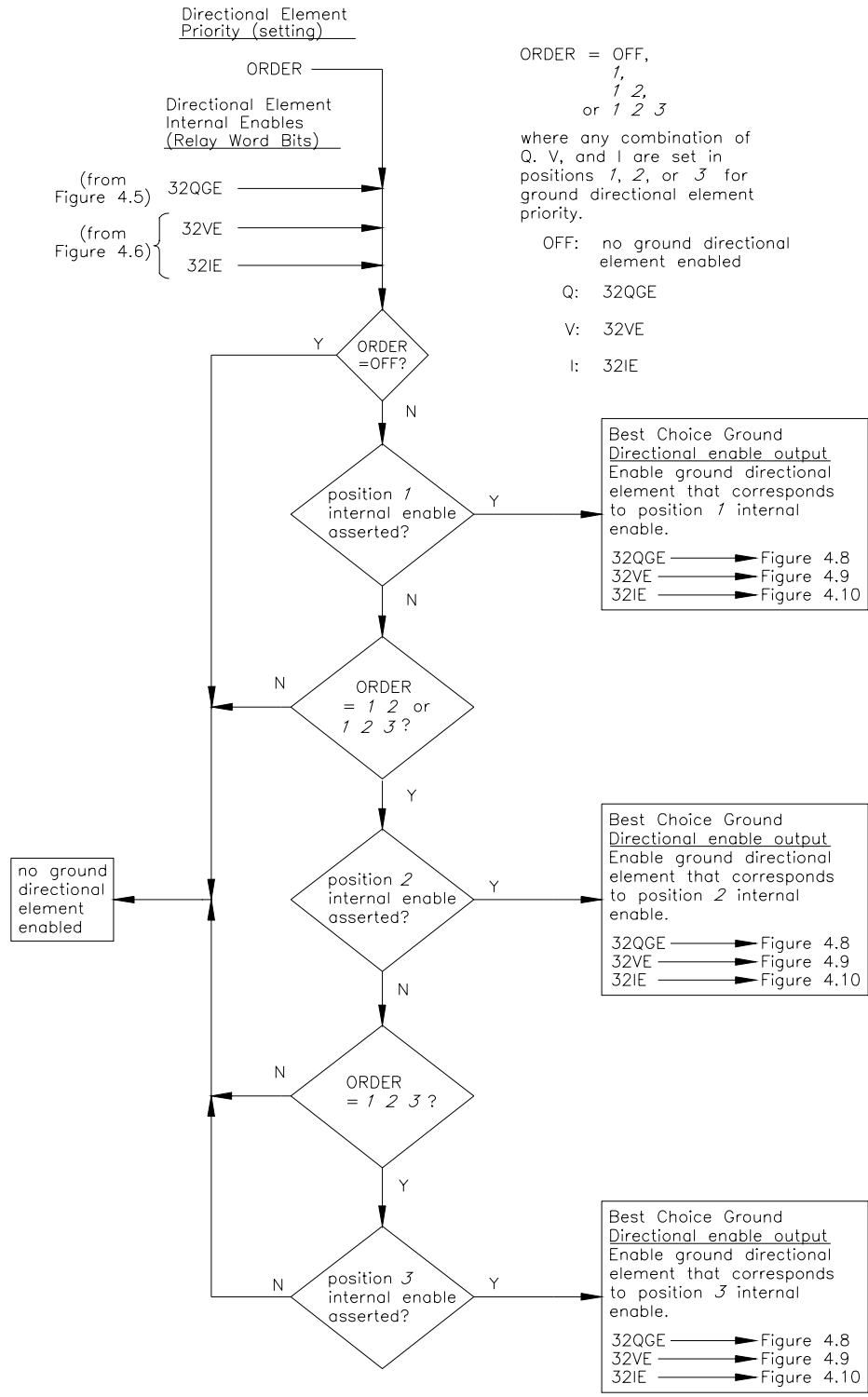


Figure 4.6: Internal Enables (32VE and 32IE) Logic for Zero-Sequence Voltage-Polarized and Channel IN Current-Polarized Directional Elements

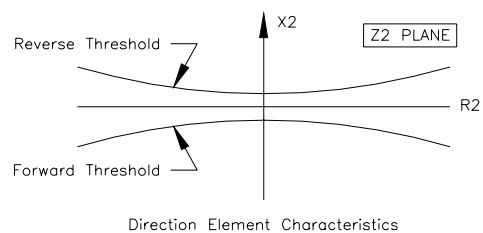
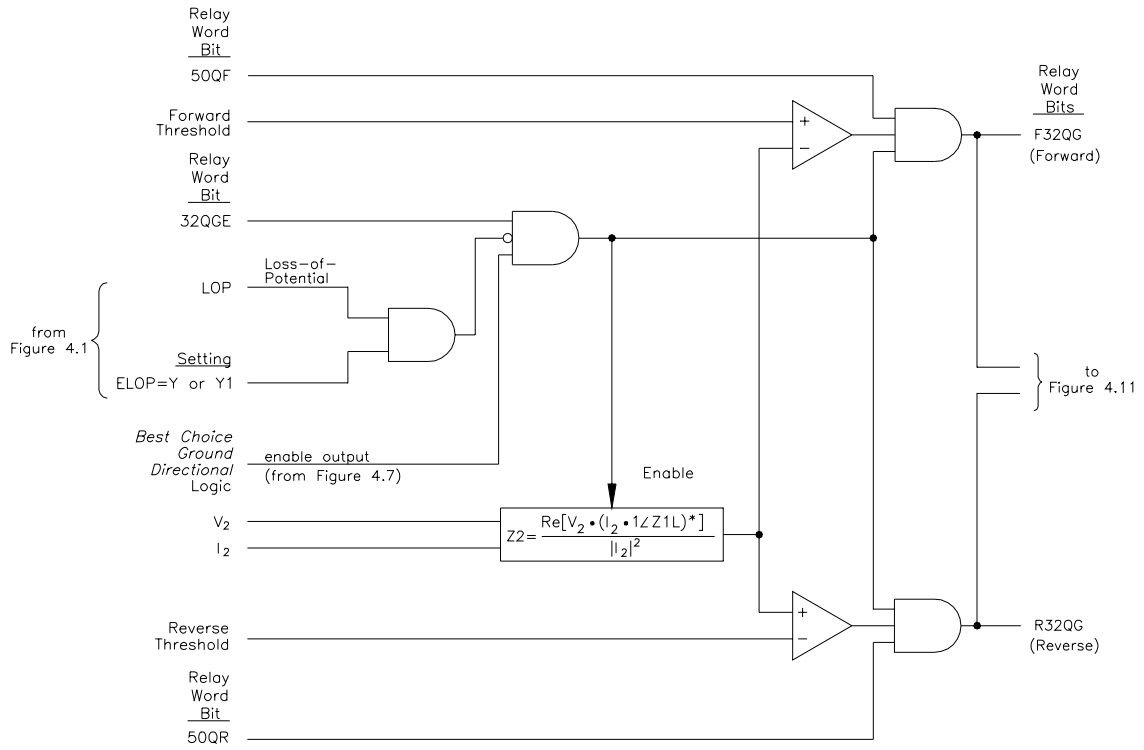
Note: If channel IN is rated 0.05 A nominal, then setting option “I” is not available for setting ORDER. This results in internal enable 32IE defaulting to logical 0 at the bottom of Figure 4.6. The channel IN current-polarized directional element that follows in Figure 4.10 is defeated and nonoperational when internal enable 32IE = logical 0.

Thus, the channel IN current-polarized directional element in Figure 4.10 is defeated, nonoperational, and unavailable when channel IN is rated 0.05 A nominal.



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Figure 4.7: Best Choice Ground Directional Logic



Forward Threshold:

If $Z2F \text{ Setting} \leq 0$, Forward Threshold = $0.75 \cdot Z2F - 0.25 \cdot \left| \frac{V_2}{I_2} \right|$

If $Z2F \text{ Setting} > 0$, Forward Threshold = $1.25 \cdot Z2F - 0.25 \cdot \left| \frac{V_2}{I_2} \right|$

Reverse Threshold:

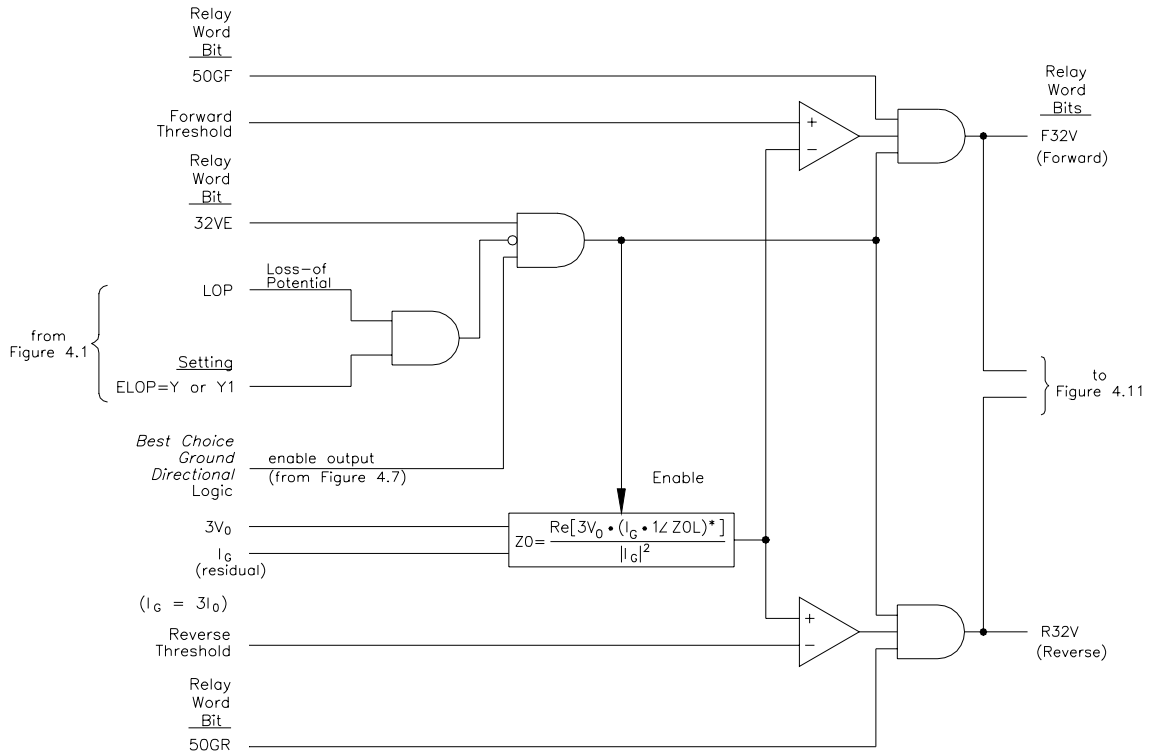
If $Z2R \text{ Setting} \geq 0$, Reverse Threshold = $0.75 \cdot Z2R + 0.25 \cdot \left| \frac{V_2}{I_2} \right|$

If $Z2R \text{ Setting} < 0$, Reverse Threshold = $1.25 \cdot Z2R + 0.25 \cdot \left| \frac{V_2}{I_2} \right|$

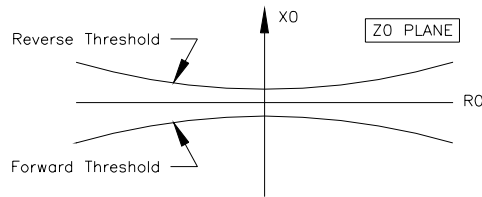
Note: $1Z Z1L$ = One OHM At The Positive-Sequence Line Angle

DWG: M351111A

Figure 4.8: Negative-Sequence Voltage-Polarized Directional Element for Neutral Ground and Residual Ground Overcurrent Elements



DWG: M351112A



Direction Element Characteristics

Forward Threshold:

$$\text{If } Z0F \text{ Setting} \leq 0, \text{ Forward Threshold} = 0.75 \cdot Z0F - 0.25 \cdot \left| \frac{V_0}{I_0} \right|$$

$$\text{If } Z0F \text{ Setting} > 0, \text{ Forward Threshold} = 1.25 \cdot Z0F - 0.25 \cdot \left| \frac{V_0}{I_0} \right|$$

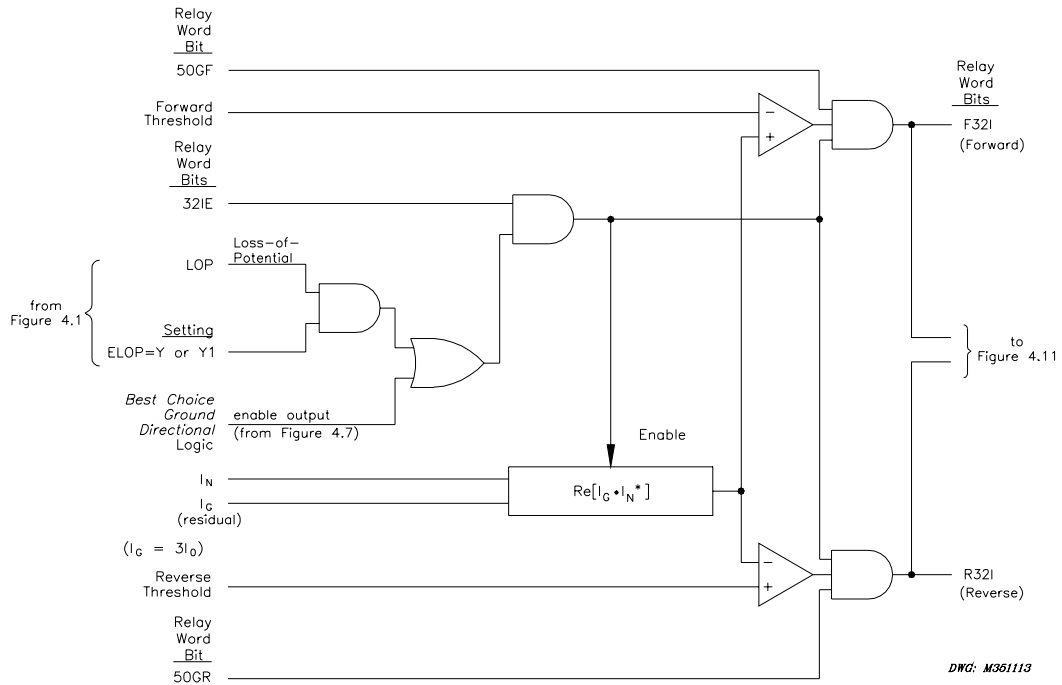
Reverse Threshold:

$$\text{If } Z0R \text{ Setting} \geq 0, \text{ Reverse Threshold} = 0.75 \cdot Z0R + 0.25 \cdot \left| \frac{V_0}{I_0} \right|$$

$$\text{If } Z0R \text{ Setting} < 0, \text{ Reverse Threshold} = 1.25 \cdot Z0R + 0.25 \cdot \left| \frac{V_0}{I_0} \right|$$

Note: 1Z Z0L = One OHM At The Zero-Sequence Line Angle

Figure 4.9: Zero-Sequence Voltage-Polarized Directional Element for Neutral Ground and Residual Ground Overcurrent Elements



Forward Threshold

$$\text{Forward Threshold} = (\text{channel } I_N \text{ nominal rating}) \cdot (\text{phase channels nominal rating}) \cdot (0.05)^2$$

Reverse Threshold

$$\text{Reverse Threshold} = -(\text{channel } I_N \text{ nominal rating}) \cdot (\text{phase channels nominal rating}) \cdot (0.05)^2$$

Figure 4.10: Channel IN Current-Polarized Directional Element for Neutral Ground and Residual Ground Overcurrent Elements (see Note 1 Following Figure 4.6)

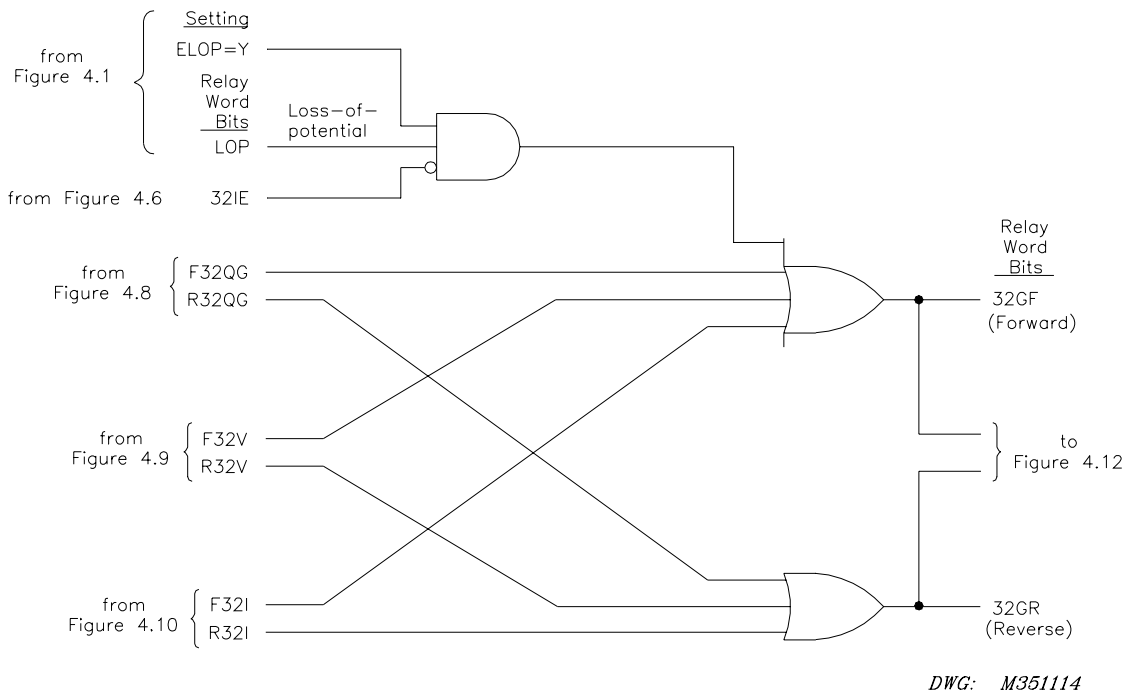


Figure 4.11: Routing of Directional Elements to Neutral Ground and Residual Ground Overcurrent Elements

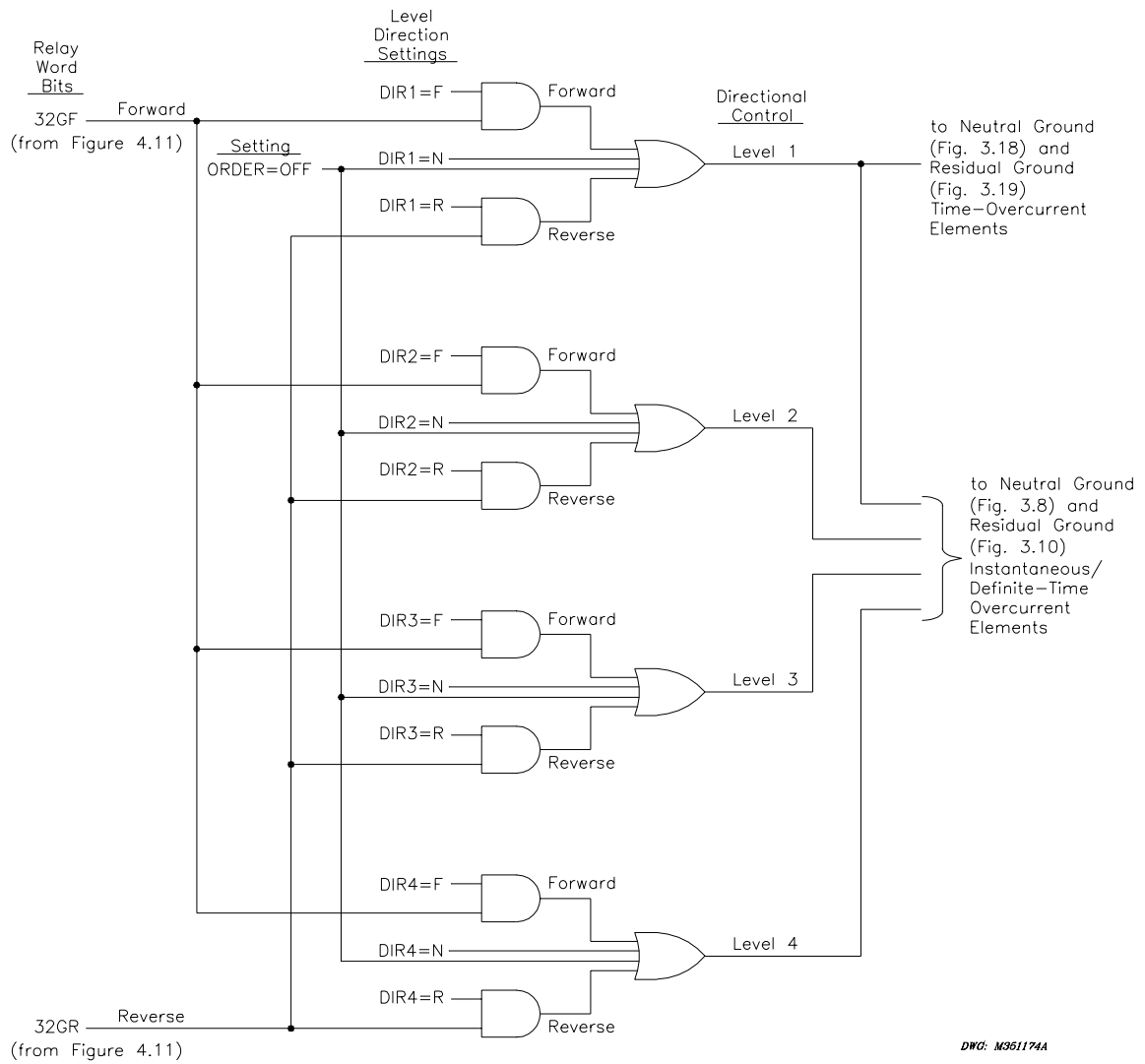


Figure 4.12: Direction Forward/Reverse Logic for Neutral Ground and Residual Ground Overcurrent Elements

DIRECTIONAL CONTROL FOR NEGATIVE-SEQUENCE AND PHASE OVERCURRENT ELEMENTS

The directional control for overcurrent elements is enabled by making directional control enable setting E32. Setting E32 and other directional control settings are described in the following subsection *Directional Control Settings*.

The negative-sequence voltage-polarized directional element controls the negative-sequence overcurrent elements. Negative-sequence voltage-polarized and positive-sequence voltage-polarized directional elements control the phase overcurrent elements. Figure 4.13 gives an overview of how the negative-sequence voltage-polarized and positive-sequence voltage-polarized directional elements are enabled and routed to control the negative-sequence and phase overcurrent elements.

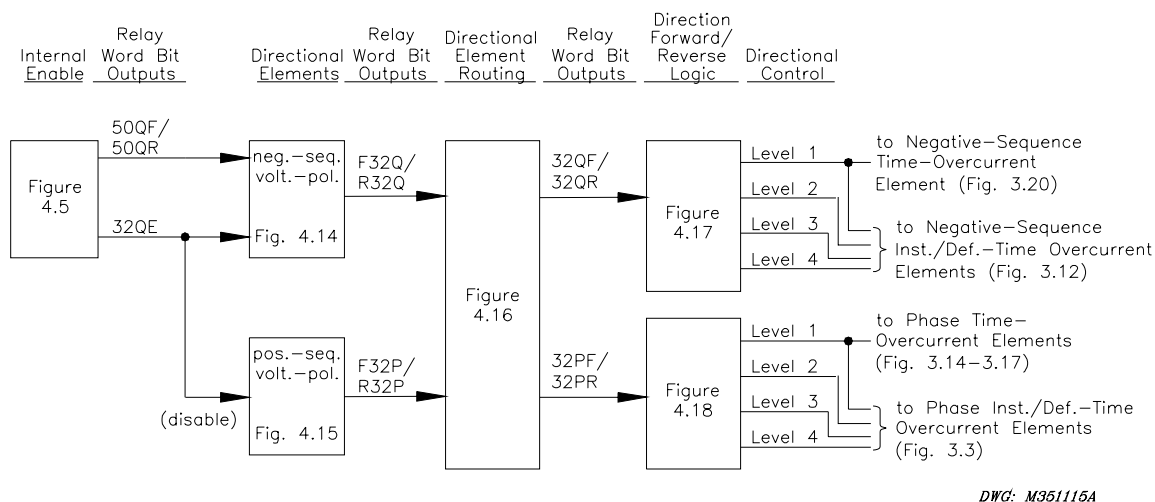


Figure 4.13: General Logic Flow of Directional Control for Negative-Sequence and Phase Overcurrent Elements

The negative-sequence voltage-polarized directional element has priority over the positive-sequence voltage-polarized directional elements in controlling the phase overcurrent elements. The negative-sequence voltage-polarized directional element operates for unbalanced faults, while the positive-sequence voltage-polarized directional element operates for three-phase faults.

Internal Enables

Refer to Figure 4.5 and Figure 4.13.

The internal enable 32QE corresponds to the negative-sequence voltage-polarized directional element.

Note that Figure 4.5 has extra internal enable 32QGE, which is used in the directional element logic that controls the neutral ground and residual ground overcurrent elements (see Figure 4.4).

The settings involved with internal enable 32QE in Figure 4.5 (e.g., settings a2, k2) are explained in a following subsection *Directional Control Settings*.

Directional Elements

Refer to Figure 4.13, Figure 4.14, and Figure 4.15.

If enable setting ELOP = Y or Y1 and a loss-of-potential condition occurs (Relay Word bit LOP asserts), the negative-sequence voltage-polarized and positive-sequence voltage-polarized directional elements are disabled (see Figure 4.14 and Figure 4.15).

Refer to Figure 4.1 and accompanying text for more information on loss-of-potential.

Note in Figure 4.13 and Figure 4.15, that the assertion of internal enable 32QE (for the negative-sequence voltage-polarized directional element) disables the positive-sequence voltage-polarized directional element. The negative-sequence voltage-polarized directional element has priority over the positive-sequence voltage-polarized directional elements in controlling the phase overcurrent elements. The negative-sequence voltage-polarized directional element operates for unbalanced faults while the positive-sequence voltage-polarized directional element operates for three-phase faults.

Note also in Figure 4.15 that the assertion of ZLOAD disables the positive-sequence voltage-polarized directional element. ZLOAD asserts when the relay is operating in a user-defined load region (see Figure 4.2).

Directional Element Routing

Refer to Figure 4.13 and Figure 4.16.

The directional element outputs are routed to the forward (Relay Word bits 32QF and 32PF) and reverse (Relay Word bits 32QR and 32PR) logic points and then on to the direction forward/reverse logic in Figure 4.17 and Figure 4.18.

Loss-of-Potential

Note if both the following are true:

- Enable setting ELOP = Y,
- A loss-of-potential condition occurs (Relay Word bit LOP asserts),

then the forward logic points (Relay Word bits 32QF and 32PF) assert to logical 1, thus, enabling the negative-sequence and phase overcurrent elements that are set direction forward (with settings DIR1 = F, DIR2 = F, etc.). These direction forward overcurrent elements effectively become nondirectional and provide overcurrent protection during a loss-of-potential condition.

As detailed previously (in Figure 4.14 and Figure 4.15), voltage-based directional elements are disabled during a loss-of-potential condition. Thus, the overcurrent elements controlled by these voltage-based directional elements are also disabled. But this disable condition is overridden for the overcurrent elements set direction forward if setting ELOP = Y.

Refer to Figure 4.1 and accompanying text for more information on loss-of-potential.

Direction Forward/Reverse Logic

Refer to Figure 4.13, Figure 4.17, and Figure 4.18.

The forward (Relay Word bits 32QF and 32PF) and reverse (Relay Word bits 32QR and 32PR) logic points are routed to the different levels of overcurrent protection by the level direction settings DIR1 through DIR4.

Table 4.1 shows the overcurrent elements that are controlled by each level direction setting. Note in Table 4.1 that all the time-overcurrent elements (51_T elements) are controlled by the DIR1 level direction setting.

In most communications-assisted trip schemes, the levels are set as follows (see Figure 5.4):

Level 1 overcurrent elements set direction forward (DIR1 = F)

Level 2 overcurrent elements set direction forward (DIR2 = F)

Level 3 overcurrent elements set direction reverse (DIR3 = R)

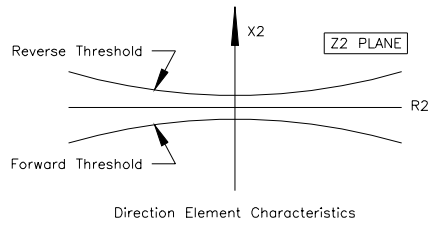
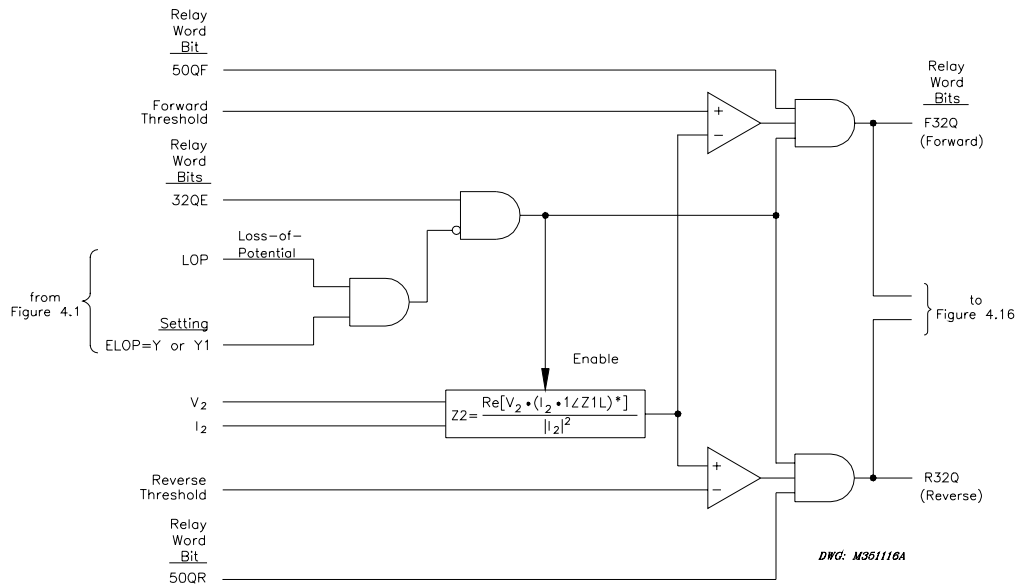
If a level direction setting (e.g., DIR1) is set:

DIR1 = N (nondirectional)

then the corresponding Level 1 directional control outputs in Figure 4.17 and Figure 4.18 assert to logical 1. The referenced Level 1 overcurrent elements in Figure 4.17 and Figure 4.18 are then not controlled by the directional control logic.

See the beginning of following subsection ***Directional Control Settings*** for discussion of the operation of level direction settings DIR1 through DIR4 when the directional control enable setting E32 is set to E32 = N.

In some applications, level direction settings DIR1 through DIR4 are not flexible enough in assigning the desired direction for certain overcurrent elements. Subsection ***Directional Control Provided by Torque Control Settings*** at the end of this section describes how to avoid this limitation for special cases.



Forward Threshold:

$$\text{If } Z2F \text{ Setting} \leq 0, \text{ Forward Threshold} = 0.75 \cdot Z2F - 0.25 \cdot \left| \frac{V_2}{I_2} \right|$$

$$\text{If } Z2F \text{ Setting} > 0, \text{ Forward Threshold} = 1.25 \cdot Z2F - 0.25 \cdot \left| \frac{V_2}{I_2} \right|$$

Reverse Threshold:

$$\text{If } Z2R \text{ Setting} \geq 0, \text{ Reverse Threshold} = 0.75 \cdot Z2R + 0.25 \cdot \left| \frac{V_2}{I_2} \right|$$

$$\text{If } Z2R \text{ Setting} < 0, \text{ Reverse Threshold} = 1.25 \cdot Z2R + 0.25 \cdot \left| \frac{V_2}{I_2} \right|$$

Figure 4.14: Negative-Sequence Voltage-Polarized Directional Element for Negative-Sequence and Phase Overcurrent Elements

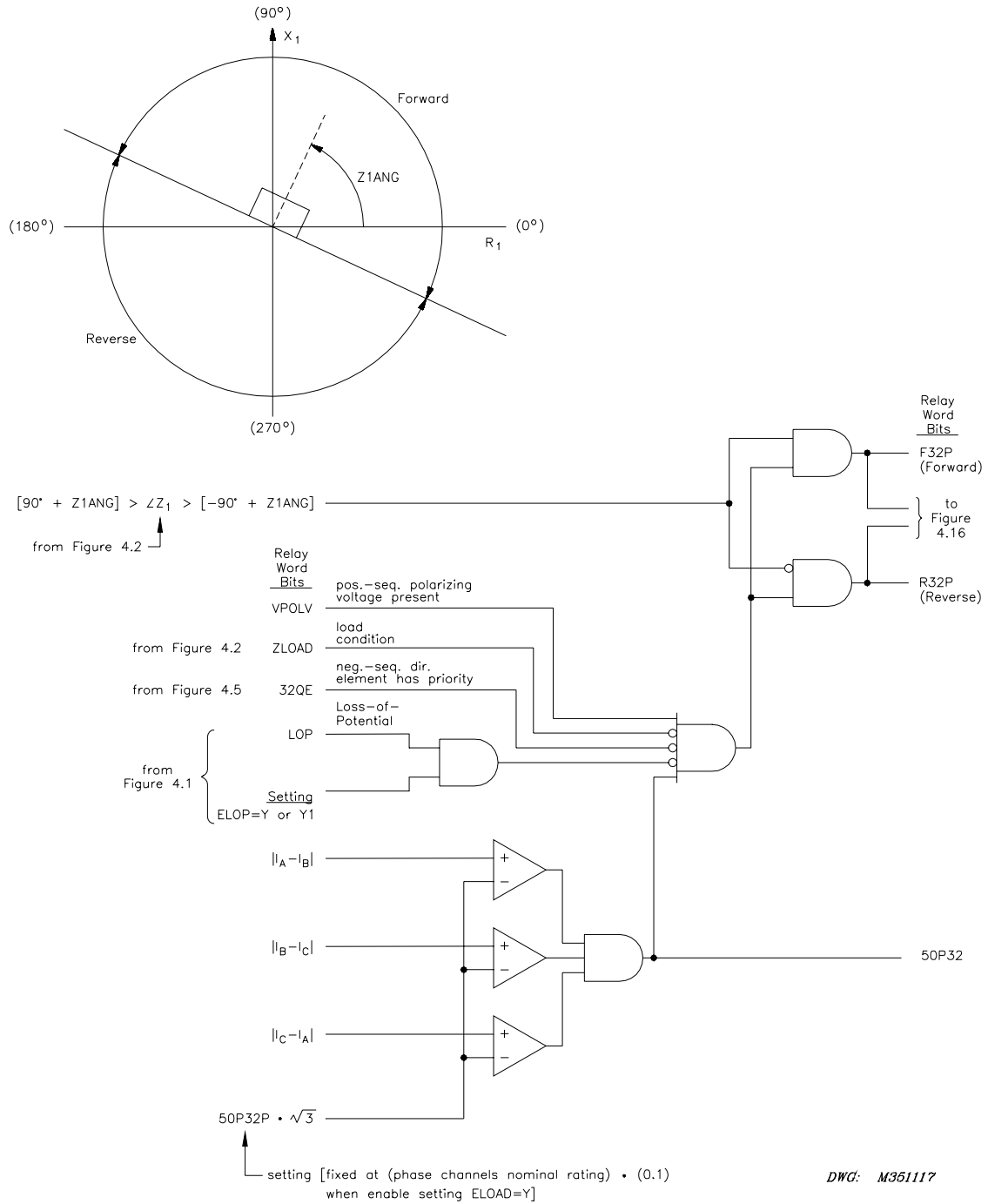
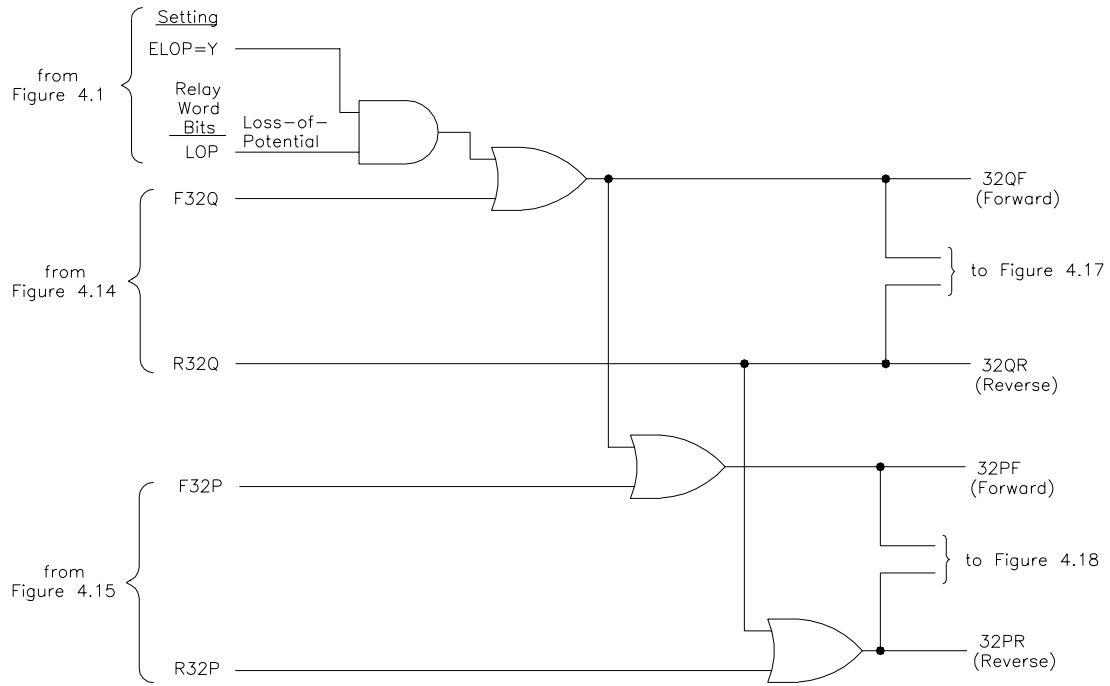


Figure 4.15: Positive-Sequence Voltage-Polarized Directional Element for Phase Overcurrent Elements



DWG: M351118A

Figure 4.16: Routing of Directional Elements to Negative-Sequence and Phase Overcurrent Elements

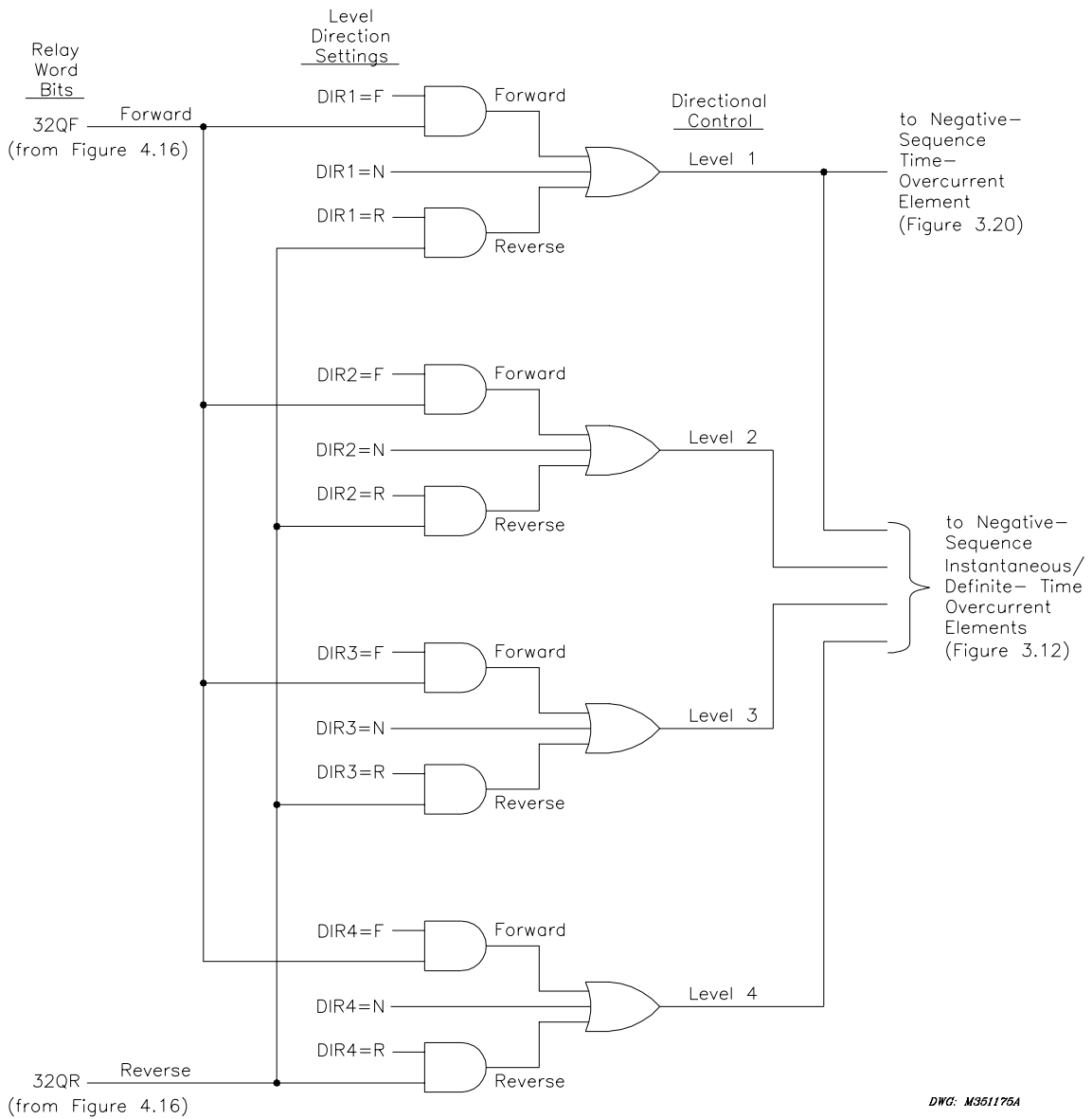


Figure 4.17: Direction Forward/Reverse Logic for Negative-Sequence Overcurrent Elements

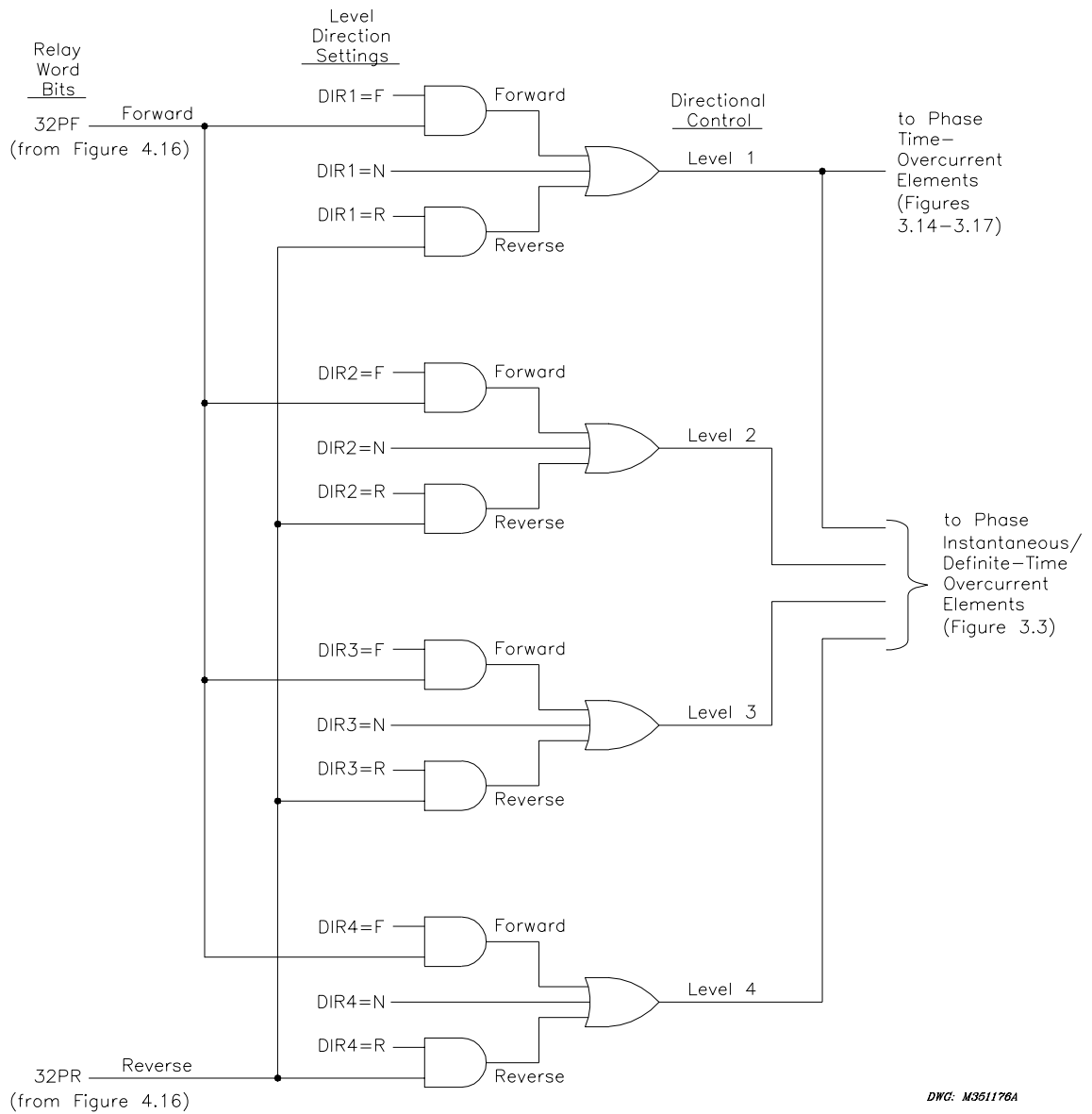


Figure 4.18: Direction Forward/Reverse Logic for Phase Overcurrent Elements

DIRECTIONAL CONTROL SETTINGS

The directional control for overcurrent elements is enabled by making directional control enable setting E32. Setting E32 has setting choices:

- Y enable directional control
- N disable directional control
- AUTO enable directional control and set a number of the directional element settings automatically

Note: If directional control enable setting E32 = N, directional control is disabled and no directional control settings are made. All level direction settings are set internally as:

- DIR1 = N (no directional control for Level 1 overcurrent elements)
- DIR2 = N (no directional control for Level 2 overcurrent elements)
- DIR3 = N (no directional control for Level 3 overcurrent elements)
- DIR4 = N (no directional control for Level 4 overcurrent elements)

With the above settings, the directional control outputs in Figure 4.12, Figure 4.17, and Figure 4.18 assert to logical 1. The referenced overcurrent elements in Figure 4.12, Figure 4.17, and Figure 4.18 are then not controlled by the directional control logic.

Settings Made Automatically

If the directional control enable setting E32 is set:

E32 = AUTO

then the following directional control settings are calculated and set automatically:

Z2F, Z2R, 50QFP, 50QRP, a2, k2, 50GFP, 50GRP, a0, Z0F, and Z0R

Once these settings are calculated automatically, they can only be modified if the user goes back and changes the directional control enable setting to E32 = Y.

The remaining directional control settings are not set automatically if setting E32 = AUTO. They have to be set by the user, whether setting E32 = AUTO or Y. These settings are:

DIR1, DIR2, DIR3, DIR4, ORDER, 50P32P, and E32IV

All these settings are explained in detail in the remainder of this subsection.

Settings

DIR1–Level 1 Overcurrent Element Direction Setting

DIR2–Level 2 Overcurrent Element Direction Setting

DIR3–Level 3 Overcurrent Element Direction Setting

DIR4–Level 4 Overcurrent Element Direction Setting

Setting Range:

F = Direction Forward

R = Direction Reverse

N = Nondirectional

Table 4.1 shows the overcurrent elements that are controlled by each level direction setting. Note in Table 4.1 that all the time-overcurrent elements (51_T elements) are controlled by the DIR1 level direction setting. Figure 4.12, Figure 4.17, and Figure 4.18 show the logic implementation of the control listed in Table 4.1.

Table 4.1: Overcurrent Elements Controlled by Level Direction Settings DIR1 Through DIR4 (Corresponding Overcurrent Element Figure Numbers in Parentheses)

Level Direction Settings	Phase	Neutral Ground	Residual Ground	Negative-Sequence
DIR1	67P1 (3.3)	67N1 (3.8)	67G1 (3.10)	67Q1 (3.12)
	67P1T (3.3)	67N1T (3.8)	67G1T (3.10)	67Q1T (3.12)
	51PT (3.14)	51NT (3.18)	51GT (3.19)	51QT (3.20)
	51AT (3.15)			
	51BT (3.16)			
	51CT (3.17)			
DIR2	67P2 (3.3)	67N2 (3.8)	67G2 (3.10)	67Q2 (3.12)
	67P2T (3.3)	67N2T (3.8)	67G2T (3.10)	67Q2T (3.12)
	67P2S (3.3)	67N2S (3.8)	67G2S (3.10)	67Q2S (3.12)
DIR3	67P3 (3.3)	67N3 (3.8)	67G3 (3.10)	67Q3 (3.12)
	67P3T (3.3)	67N3T (3.8)	67G3T (3.10)	67Q3T (3.12)
DIR4	67P4 (3.3)	67N4 (3.8)	67G4 (3.10)	67Q4 (3.12)
	67P4T (3.3)	67N4T (3.8)	67G4T (3.10)	67Q4T (3.12)

In most communications-assisted trip schemes, the levels are set as follows (see Figure 5.4):

Level 1 overcurrent elements set direction forward (DIR1 = F)

Level 2 overcurrent elements set direction forward (DIR2 = F)

Level 3 overcurrent elements set direction reverse (DIR3 = R)

In some applications, level direction settings DIR1 through DIR4 are not flexible enough in assigning the desired direction for certain overcurrent elements. Subsection *Directional Control Provided by Torque Control Settings* at the end of this section describes how to avoid this limitation for special cases.

ORDER–Ground Directional Element Priority Setting

Setting Range:

Q	Negative-sequence voltage-polarized directional element
V	Zero-sequence voltage-polarized directional element
I	Channel IN current-polarized directional element
OFF	No ground directional control

Setting ORDER can be set with any combination of Q, V, and I. The order in which these directional elements are listed in setting ORDER determines the priority in which they operate to provide *Best Choice Ground Directional* logic control. See Figure 4.7.

Note : If channel IN is rated 0.05 A nominal, then setting option “I” is not available for setting ORDER. This results in internal enable 32IE defaulting to logical 0 at the bottom of Figure 4.6. The channel IN current-polarized directional element that follows in Figure 4.10 is defeated and nonoperational when internal enable 32IE = logical 0.

Thus, the channel IN current-polarized directional element in Figure 4.10 is defeated, nonoperational, and unavailable when channel IN is rated 0.05 A nominal.

For example, if setting:

ORDER = QV

then the first listed directional element (Q = negative-sequence voltage-polarized directional element; see Figure 4.8) is the first priority directional element to provide directional control for the neutral ground and residual ground overcurrent elements.

If the negative-sequence voltage-polarized directional element is not operable (i.e., it does not have sufficient operating quantity as indicated by its internal enable, 32QGE, not being asserted), then the second listed directional element (V = zero-sequence voltage-polarized directional element; see Figure 4.9) provides directional control for the neutral ground and residual ground overcurrent elements.

Another example, if setting:

ORDER = V

then the zero-sequence voltage-polarized directional element (V = zero-sequence voltage-polarized directional element; see Figure 4.9) provides directional control for the neutral ground and residual ground overcurrent elements all the time.

Setting ORDER can be set with any element combination (e.g., ORDER = IQV, ORDER = QVI, ORDER = IV, ORDER = VQ, ORDER = I, ORDER = Q).

If setting:

ORDER = OFF

then the three directional elements (Q, V, and I) are inoperable. Note in Figure 4.12 that setting ORDER = OFF effectively makes the neutral ground and residual ground overcurrent elements nondirectional (the directional control outputs of Figure 4.12 are continuously asserted to logical 1).

50P32P–Phase Directional Element Three-Phase Current Pickup

Setting Range:

0.50–10.00 A secondary (5 A nominal phase current inputs, IA, IB, IC)

0.1–2.00 A secondary (1 A nominal phase current inputs, IA, IB, IC)

The 50P32P setting is set to pick up for all three-phase faults that need to be covered by the phase overcurrent elements. It supervises the positive-sequence voltage-polarized directional elements F32P and R32P (see Figure 4.15).

If the load-encroachment logic is enabled (enable setting ELOAD = Y), then setting 50P32P is not made or displayed, but is fixed internally at:

0.5 A secondary (5 A nominal phase current inputs, IA, IB, IC)

0.1 A secondary (1 A nominal phase current inputs, IA, IB, IC)

Z2F–Forward Directional Z2 Threshold

Z2R–Reverse Directional Z2 Threshold

Setting Range:

-64.00 to 64.00 Ω secondary (150 V voltage inputs, VA, VB, VC; 5 A nominal phase current inputs, IA, IB, IC)

-320.00 to 320.00 Ω secondary (150 V voltage inputs, VA, VB, VC; 1 A nominal phase current inputs, IA, IB, IC)

-128.00 to 128.00 Ω secondary (300 V voltage inputs, VA, VB, VC; 5 A nominal phase current inputs, IA, IB, IC)

-640.00 to 640.00 Ω secondary (300 V voltage inputs, VA, VB, VC; 1 A nominal phase current inputs, IA, IB, IC)

Z2F and Z2R are used to calculate the Forward and Reverse Thresholds, respectively, for the negative-sequence voltage-polarized directional elements (see Figure 4.8 and Figure 4.14).

Z2F and Z2R Set Automatically

If enable setting E32 = AUTO, settings Z2F and Z2R (negative-sequence impedance values) are calculated automatically, using the positive-sequence line impedance magnitude setting Z1MAG as follows:

$$Z2F = Z1MAG/2 \quad (\Omega \text{ secondary})$$

$$Z2R = Z1MAG/2 + z \quad (\Omega \text{ secondary; "z" listed in table below})$$

If enable setting E32 = Y, settings Z2F and Z2R (negative-sequence impedance values) are calculated by the user and entered by the user, but setting Z2R must be greater in value than setting Z2F by value "z":

Relay Configuration	z (Ω secondary)
5 A nominal current, 150 V voltage inputs	0.1
5 A nominal current, 300 V voltage inputs	0.2
1 A nominal current, 150 V voltage inputs	0.5
1 A nominal current, 300 V voltage inputs	1.0

50QFP—Forward Directional Negative-Sequence Current Pickup

50QRP—Reverse Directional Negative-Sequence Current Pickup

Setting Range:

0.25–5.00 A secondary (5 A nominal phase current inputs, IA, IB, IC)

0.05–1.00 A secondary (1 A nominal phase current inputs, IA, IB, IC)

The 50QFP setting ($3I_2$ current value) is the pickup for the forward fault detector 50QF of the negative-sequence voltage-polarized directional elements (see Figure 4.5). Ideally, the setting is above normal load unbalance and below the lowest expected negative-sequence current magnitude for unbalanced forward faults.

The 50QRP setting ($3I_2$ current value) is the pickup for the reverse fault detector 50QR of the negative-sequence voltage-polarized directional elements (see Figure 4.5). Ideally, the setting is above normal load unbalance and below the lowest expected negative-sequence current magnitude for unbalanced reverse faults.

50QFP and 50QRP Set Automatically

If enable setting E32 = AUTO, settings 50QFP and 50QRP are set automatically at:

50QFP = 0.50 A secondary (5 A nominal phase current inputs, IA, IB, IC)

50QRP = 0.25 A secondary (5 A nominal phase current inputs, IA, IB, IC)

50QFP = 0.10 A secondary (1 A nominal phase current inputs, IA, IB, IC)

50QRP = 0.05 A secondary (1 A nominal phase current inputs, IA, IB, IC)

a2–Positive-Sequence Current Restraint Factor, I_2/I_1

Setting Range:

0.02–0.50 (unitless)

Refer to Figure 4.5.

The a2 factor increases the security of the negative-sequence voltage-polarized directional elements. It keeps the elements from operating for negative-sequence current (system unbalance), which circulates due to line asymmetries, CT saturation during three-phase faults, etc.

a2 Set Automatically

If enable setting E32 = AUTO, setting a2 is set automatically at:

$$a2 = 0.1$$

For setting a2 = 0.1, the negative-sequence current (I_2) magnitude has to be greater than 1/10 of the positive-sequence current (I_1) magnitude in order for the negative-sequence voltage-polarized directional elements to be enabled ($|I_2| > 0.1 \cdot |I_1|$).

k2–Zero-Sequence Current Restraint Factor, I_2/I_0

Setting Range:

0.10–1.20 (unitless)

Note the internal enable logic outputs in Figure 4.5:

32QE internal enable for the negative-sequence voltage-polarized directional element that controls the negative-sequence and phase overcurrent elements

32QGE internal enable for the negative-sequence voltage-polarized directional element that controls the neutral ground and residual ground overcurrent elements

The k2 factor is applied to internal enable 32QGE. The negative-sequence current (I_2) magnitude has to be greater than the zero-sequence current (I_0) magnitude multiplied by k2 in order for the 32QGE internal enable (and following negative-sequence voltage-polarized directional element in Figure 4.8) to be enabled:

$$|I_2| > k2 \cdot |I_0|$$

This check assures that the relay uses the most robust analog quantities in making directional decisions for the neutral ground and residual ground overcurrent elements.

If both of the internal enables:

32VE internal enable for the zero-sequence voltage-polarized directional element that controls the neutral ground and residual ground overcurrent elements

32IE internal enable for the channel IN current-polarized directional element that controls the neutral ground and residual ground overcurrent elements

are deasserted, then factor k2 is ignored as a logic enable for the 32QGE internal enable. If neither the zero-sequence voltage-polarized nor the channel IN current-polarized directional elements are operable, less restrictions (i.e., factor k2) are put on the operation of the negative-sequence voltage-polarized directional element.

k2 Set Automatically

If enable setting E32 = AUTO, setting k2 is set automatically at:

$$k2 = 0.2$$

For setting k2 = 0.2, the negative-sequence current (I_2) magnitude has to be greater than 1/5 of the zero-sequence current (I_0) magnitude in order for the negative-sequence voltage-polarized directional elements to be enabled ($|I_2| > 0.2 \cdot |I_0|$). Again, this presumes at least one of the internal enables 32VE or 32IE is asserted.

50GFP—Forward Directional Residual Ground Current Pickup

50GRP—Reverse Directional Residual Ground Current Pickup

Setting Range:

0.25–5.00 A secondary (5 A nominal phase current inputs, IA, IB, IC)

0.05–1.00 A secondary (1 A nominal phase current inputs, IA, IB, IC)

If preceding setting ORDER does not contain V or I (no zero-sequence voltage-polarized or channel IN current-polarized directional elements are enabled), then settings 50GFP and 50GRP are not made or displayed.

The 50GFP setting ($3I_0$ current value) is the pickup for the forward fault detector 50GF of the zero-sequence voltage-polarized and channel IN current-polarized directional elements (see Figure 4.6). Ideally, the setting is above normal load unbalance and below the lowest expected zero-sequence current magnitude for unbalanced forward faults.

The 50GRP setting ($3I_0$ current value) is the pickup for the reverse fault detector 50GR of the zero-sequence voltage-polarized and channel IN current-polarized directional elements (see Figure 4.6). Ideally, the setting is above normal load unbalance and below the lowest expected zero-sequence current magnitude for unbalanced reverse faults.

50GFP and 50GRP Set Automatically

If enable setting E32 = AUTO, settings 50GFP and 50GRP are set automatically at:

50GFP = 0.50 A secondary (5 A nominal phase current inputs, IA, IB, IC)

50GRP = 0.25 A secondary (5 A nominal phase current inputs, IA, IB, IC)

50GFP = 0.10 A secondary (1 A nominal phase current inputs, IA, IB, IC)

50GRP = 0.05 A secondary (1 A nominal phase current inputs, IA, IB, IC)

a0–Positive-Sequence Current Restraint Factor, I_0/I_1

Setting Range:

0.02–0.50 (unitless)

If preceding setting ORDER does not contain V or I (no zero-sequence voltage-polarized or channel IN current-polarized directional elements are enabled), then setting a0 is not made or displayed.

Refer to Figure 4.6.

The a0 factor increases the security of the zero-sequence voltage-polarized and channel IN current-polarized directional elements. It keeps the elements from operating for zero-sequence current (system unbalance), which circulates due to line asymmetries, CT saturation during three-phase faults, etc.

a0 Set Automatically

If enable setting E32 = AUTO, setting a0 is set automatically at:

$$a0 = 0.1$$

For setting a0 = 0.1, the zero-sequence current (I_0) magnitude has to be greater than 1/10 of the positive-sequence current (I_1) magnitude in order for the zero-sequence voltage-polarized and channel IN current-polarized directional elements to be enabled ($|I_0| > 0.1 \cdot |I_1|$).

Z0F–Forward Directional Z0 Threshold

Z0R–Reverse Directional Z0 Threshold

Setting Range:

-64.00 to 64.00 Ω secondary (150 V voltage inputs, VA, VB, VC; 5 A nominal phase current inputs, IA, IB, IC)

-320.00 to 320.00 Ω secondary (150 V voltage inputs, VA, VB, VC; 1 A nominal phase current inputs, IA, IB, IC)

-128.00 to 128.00 Ω secondary (300 V voltage inputs, VA, VB, VC; 5 A nominal phase current inputs, IA, IB, IC)

-640.00 to 640.00 Ω secondary (300 V voltage inputs, VA, VB, VC; 1 A nominal phase current inputs, IA, IB, IC)

If preceding setting ORDER does not contain V (no zero-sequence voltage-polarized directional element is enabled), then settings Z0F and Z0R are not made or displayed.

Z0F and Z0R are used to calculate the Forward and Reverse Thresholds, respectively, for the zero-sequence voltage-polarized directional elements (see Figure 4.9).

Z0F and Z0R Set Automatically

If enable setting E32 = AUTO, settings Z0F and Z0R (zero-sequence impedance values) are calculated automatically, using the zero-sequence line impedance magnitude setting Z0MAG as follows:

$$Z0F = Z0MAG/2 \quad (\Omega \text{ secondary})$$

$$Z0R = Z0MAG/2 + z \quad (\Omega \text{ secondary; "z" listed in table below})$$

If enable setting E32 = Y, settings Z0F and Z0R (zero-sequence impedance values) are calculated by the user and entered by the user, but setting Z0R must be greater in value than setting Z0F by value "z":

Relay Configuration	z (Ω secondary)
5 A nominal current, 150 V voltage inputs	0.1
5 A nominal current, 300 V voltage inputs	0.2
1 A nominal current, 150 V voltage inputs	0.5
1 A nominal current, 300 V voltage inputs	1.0

E32IV–SELOGIC Control Equation Enable

Refer to Figure 4.6.

SELOGIC control equation setting E32IV must be asserted to logical 1 to enable the zero-sequence voltage-polarized and channel IN current-polarized directional elements for directional control of neutral ground and residual ground overcurrent elements.

Most often, this setting is set directly to logical 1:

$$E32IV = 1 \quad (\text{numeral 1})$$

For situations where zero-sequence source isolation can occur (e.g., by the opening of a circuit breaker) and result in possible mutual coupling problems for the zero-sequence voltage-polarized and channel IN current-polarized directional elements, SELOGIC control equation setting E32IV should be deasserted to logical 0. In this example, this is accomplished by connecting a circuit breaker auxiliary contact from the identified circuit breaker to the SEL-351 Relay:

$$E32IV = IN106 \quad (52a \text{ connected to optoisolated input IN106})$$

Almost any desired control can be set in SELOGIC control equation setting E32IV.

DIRECTIONAL CONTROL PROVIDED BY TORQUE CONTROL SETTINGS

For most applications, the level direction settings DIR1 through DIR4 are used to set overcurrent elements direction forward, reverse, or nondirectional. Table 4.1 shows the overcurrent elements that are controlled by each level direction setting. Note in Table 4.1 that all the time-overcurrent elements (51_T elements) are controlled by the DIR1 level direction setting. See Figure 4.12, Figure 4.17, and Figure 4.18.

In most communications-assisted trip schemes, the levels are set as follows (see Figure 5.4):

Level 1 overcurrent elements set direction forward (DIR1 = F)

Level 2 overcurrent elements set direction forward (DIR2 = F)

Level 3 overcurrent elements set direction reverse (DIR3 = R)

Suppose that the Level 1 overcurrent elements should be set as follows:

67P1 direction forward

67G1 direction forward

51PT direction forward

51AT direction reverse

51BT direction reverse

51CT direction reverse

51NT nondirectional

51GT direction forward

To accomplish this, the DIR1 setting is “turned off,” and the corresponding SELOGIC control equation torque control settings for the above overcurrent elements are used to make the elements directional (forward or reverse) or nondirectional. The required settings are:

DIR1 = N (“turned off”; see Figure 4.12, Figure 4.17, and Figure 4.18)

67P1TC = 32PF (direction forward; see Figure 3.3)

67G1TC = 32GF (direction forward; see Figure 3.10)

51PTC = 32PF (direction forward; see Figure 3.14)

51ATC = 32PR (direction reverse; see Figure 3.15)

51BTC = 32PR (direction reverse; see Figure 3.16)

51CTC = 32PR (direction reverse; see Figure 3.17)

51NTC = 1 (nondirectional; see Figure 3.18)

51GTC = 32GF (direction forward; see Figure 3.19)

This is just one example of using SELOGIC control equation torque control settings to make overcurrent elements directional (forward or reverse) or nondirectional. This example discussed only Level 1 overcurrent elements (controlled by level direction setting DIR1). The same setting principles can apply to the other levels as well. Many variations are possible.

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SECTION 5: TRIP AND TARGET LOGIC

TRIP LOGIC

The trip logic in Figure 5.1 provides flexible tripping with SELOGIC[®] control equation settings:

TRCOMM	Communications-Assisted Trip Conditions. Setting TRCOMM is supervised by communications-assisted trip logic. See <i>Communications-Assisted Trip Logic—General Overview</i> later in this section for more information on communications-assisted tripping.
DTT	Direct Transfer Trip Conditions. Note in Figure 5.1 that setting DTT is unsupervised. Any element that asserts in setting DTT will cause Relay Word bit TRIP to assert to logical 1. Although setting TR is also unsupervised, setting DTT is provided separate from setting TR for target LED purposes. (COMM target LED on the front panel illuminates when DTT asserts to logical 1; see COMM target LED discussion in the <i>Front-Panel Target LEDs</i> subsection at the end of this section). A typical setting for DTT is: $\text{DTT} = \text{IN106}$ where input IN106 is connected to the output of direct transfer trip communications equipment. Setting DTT is also used for Direct Underreaching Transfer Trip (DUTT) schemes.
TRSOTF	Switch-Onto-Fault Trip Conditions. Setting TRSOTF is supervised by the switch-onto-fault condition SOTFE. See <i>Switch-Onto-Fault (SOTF) Trip Logic</i> on page 5-7 for more information on switch-onto-fault logic.
TR	Other Trip Conditions. Setting TR is the SELogic control equation trip setting most often used if tripping does not involve communications-assisted (settings TRCOMM and DTT) or switch-onto-fault (setting TRSOTF) trip logic. Note in Figure 5.1 that setting TR is unsupervised. Any element that asserts in setting TR will cause Relay Word bit TRIP to assert to logical 1.
ULTR	Unlatch Trip Conditions.
TDURD	Minimum Trip Duration Time. This timer establishes the minimum time duration for which the TRIP Relay Word bit asserts. This is rising edge initiated timer. The settable range for this timer is 4–16,000 cycles. See Figure 5.2.

More than one trip setting (or all four trip settings TRCOMM, DTT, TRSOTF, and TR) can be set. For example, in a communications-assisted trip scheme, TRCOMM is set with direction forward overreaching Level 2 overcurrent elements, TR is set with direction forward underreaching Level 1 overcurrent elements and other time delayed elements (e.g., Level 2 definite-time overcurrent elements), and TRSOTF is set with nondirectional overcurrent elements.

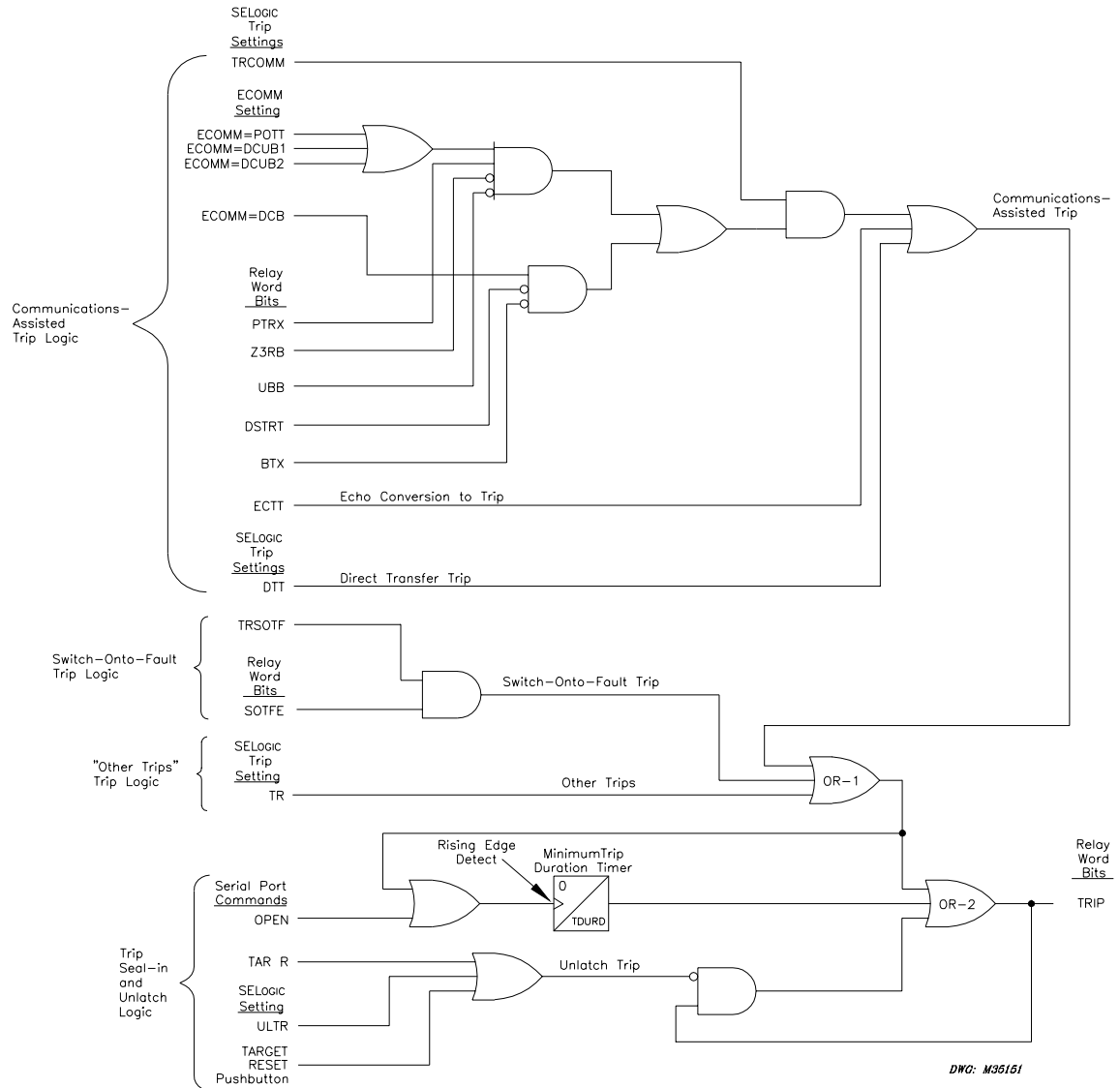


Figure 5.1: Trip Logic

Set Trip

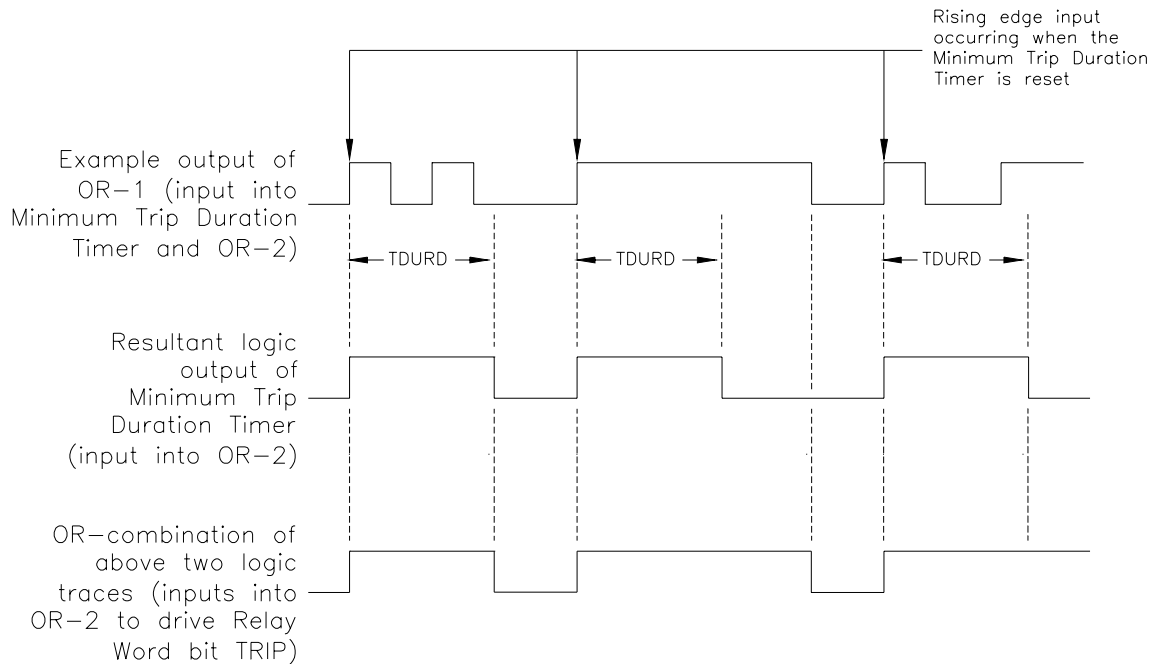
Refer to Figure 5.1. All trip conditions:

- Communications-Assisted Trip
- Direct Transfer Trip
- Switch-Onto-Fault Trip
- Other Trips

are combined into OR-1 gate. The output of OR-1 gate asserts Relay Word bit TRIP to logical 1, regardless of other trip logic conditions. It also is routed into the Minimum Trip Duration Timer (setting TDURD).

As shown in the time line example in Figure 5.2, the Minimum Trip Duration Timer (with setting TDURD) outputs a logical 1 for a time duration of “TDURD” cycles any time it sees a rising edge on its input (logical 0 to logical 1 transition), if it is not already timing (timer is reset). The TDURD timer assures that the TRIP Relay Word bit remains asserted at logical 1 for a minimum of “TDURD” cycles. If the output of OR-1 gate is logical 1 beyond the TDURD time, Relay Word bit TRIP remains asserted at logical 1 for as long as the output of OR-1 gate remains at logical 1, regardless of other trip logic conditions.

The Minimum Trip Duration Timer can be set no less than 4 cycles.



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Figure 5.2: Minimum Trip Duration Timer Operation (See Bottom of Figure 5.1)

Note: The OPEN Command is no longer embedded in Trip Logic.

In previous firmware versions of the SEL-351 Relay, the OPEN command was embedded in the trip logic in Figure 5.1. The OPEN command was routed directly into the Minimum Trip Duration Timer, along with the output of logic gate OR-1.

The OPEN command is no longer directly embedded in the trip logic. This change was made so that users can supervise the OPEN command if desired via setting TR.

The OPEN command is now included in the trip logic in the factory settings:

$$\text{TR} = \dots + \text{OC}$$

Relay Word bit OC asserts for execution of the OPEN Command. See *OPE Command (Open Breaker)* in *Section 10: Serial Port Communications and Commands* for more information on the OPEN Command. More discussion follows later on the factory settings for setting TR.

If previous firmware versions of the SEL-351 Relay with the OPEN command imbedded in the trip logic also have setting TR set as:

$$\text{TR} = \dots + \text{OC}$$

this would appear as a redundancy in inputting the OPEN command into the trip logic. But, this is not a problem—just a redundancy in logic. Thus, SEL-351 Relays with various firmware versions can be set the same with respect to setting $\text{TR} = \dots + \text{OC}$.

If a user wants to supervise the OPEN command with optoisolated input IN105, the following setting is made:

$$\text{TR} = \dots + \text{OC} * \text{IN105}$$

With this setting, the OPEN command can provide a trip only if optoisolated input IN105 is asserted. This is just one OPEN command supervision example—many variations are possible.

To prevent the execution of the OPEN command from initiating reclosing, Relay Word bit OC is entered in the SELOGIC control equation setting 79DTL (Drive-to-Lockout) in the factory settings. See the Note in the Lockout State discussion, following Table 6.1.

A COMM target LED option for the OPEN command is discussed in the *Front-Panel Target LEDs* subsection at the end of this section.

Unlatch Trip

Once Relay Word bit TRIP is asserted to logical 1, it remains asserted at logical 1 until all the following conditions come true:

- Minimum Trip Duration Timer stops timing (logic output of the TDURD timer goes to logical 0)
- Output of OR-1 gate deasserts to logical 0
- One of the following occurs:
 - SELOGIC control equation setting ULTR asserts to logical 1,
 - The front-panel TARGET RESET button is pressed,
 - Or the TAR R (Target Reset) command is executed via the serial port.

The front-panel TARGET RESET button or the TAR R (Target Reset) serial port command are primarily used during testing. Use these to force the TRIP Relay Word bit to logical 0 if test

conditions are such that setting ULTR does not assert to logical 1 to automatically deassert the TRIP Relay Word bit instead.

Other Applications for the Target Reset Function

Refer to the bottom of Figure 5.1. Note that the combination of the TARGET RESET Pushbutton and the TAR R (Target Reset) serial port command is also available as Relay Word bit TRGTR. See Figure 5.17 and accompanying text for applications for Relay Word bit TRGTR.

Factory Settings Example (Using Setting TR)

If the “communications-assisted” and “switch-onto-fault” trip logic at the top of Figure 5.1 can effectively be ignored, the figure becomes a lot smaller. Then SELOGIC control equation trip setting TR is the only input into OR-1 gate and follows into the “seal-in and unlatch” logic for Relay Word bit TRIP.

The factory settings for the trip logic SELOGIC control equation settings are:

$$\begin{aligned} \text{TR} &= 51\text{PT} + 51\text{GT} + 81\text{D1T} + \text{LB3} + 50\text{P1} * \text{SH0} + \text{OC} && \text{(trip conditions)} \\ \text{ULTR} &= !(51\text{P} + 51\text{G}) && \text{(unlatch trip conditions)} \end{aligned}$$

The factory setting for the Minimum Trip Duration Timer setting is:

$$\text{TDURD} = 9.000 \text{ cycles}$$

See the settings sheets in *Section 9: Setting the Relay* for setting ranges.

Set Trip

In SELOGIC control equation setting $\text{TR} = 51\text{PT} + 51\text{GT} + 81\text{D1T} + \text{LB3} + 50\text{P1} * \text{SH0} + \text{OC}$:

- Time-overcurrent elements 51PT and 51GT trip directly. Time-overcurrent and definite-time overcurrent elements can be torque controlled (e.g., elements 51PT and 51GT are torque controlled by SELOGIC control equation settings 51PTC and 51GTC, respectively). Check torque control settings to see if any control is applied to time-overcurrent and definite-time overcurrent elements. Such control is not apparent by mere inspection of trip setting TR or any other SELOGIC control equation trip setting.
- Frequency element 81D1T trips directly.
- Local bit LB3 trips directly (operates as a manual trip switch via the front panel). See *Local Control Switches* in *Section 7: Inputs, Outputs, Timers, and Other Control Logic* for more information on local bits.
- Phase instantaneous overcurrent element 50P1 is supervised by Relay Word bit SH0 in an ANDed condition $50\text{P1} * \text{SH0}$. Elements 50P1 can only generate a trip when $\text{SH0} = \text{logical } 1$ (reclosing relay is at shot = 0). After the first trip in a reclose cycle, the shot counter increments from 0 to 1, $\text{SH0} = \text{logical } 0$, and element 50P1 cannot generate a trip. See *Section 6: Close and Reclose Logic* for more information on reclosing relay operation.
- Relay Word bit OC asserts for execution of the OPEN Command. See *OPE Command (Open Breaker)* in *Section 10: Serial Port Communications and Commands* for more information on the OPEN Command.

With setting TDURD = 9.000 cycles, once the TRIP Relay Word bit asserts via SELOGIC control equation setting TR, it remains asserted at logical 1 for a minimum of 9 cycles.

Unlatch Trip

In SELOGIC control equation setting ULTR = $!(51P + 51G)$:

Both time-overcurrent element pickups 51P and 51G must be deasserted before the trip logic unlatches and the TRIP Relay Word bit deasserts to logical 0.

$$ULTR = !(51P + 51G) = \text{NOT}(51P + 51G) = \text{NOT}(51P) * \text{NOT}(51G)$$

Additional Settings Examples

The factory setting for SELOGIC control equation setting ULTR is a current-based trip unlatch condition. A circuit breaker status unlatch trip condition can be programmed as shown in the following examples.

Unlatch Trip with 52a Circuit Breaker Auxiliary Contact

A 52a circuit breaker auxiliary contact is wired to optoisolated input IN101.

$$52A = \text{IN101} \quad (\text{SELOGIC control equation circuit breaker status setting—see } \mathit{Optoisolated\ Inputs} \text{ in } \mathit{Section\ 7: Inputs, Outputs, Timers, and Other Control Logic})$$

$$ULTR = \text{!IN101}$$

Input IN101 has to be deenergized (52a circuit breaker auxiliary contact has to be open) before the trip logic unlatches and the TRIP Relay Word bit deasserts to logical 0.

$$ULTR = \text{!IN101} = \text{NOT}(\text{IN101})$$

Unlatch Trip With 52b Circuit Breaker Auxiliary Contact

A 52b circuit breaker auxiliary contact is wired to optoisolated input IN101.

$$52A = \text{!IN101} \quad (\text{SELOGIC control equation circuit breaker status setting—see } \mathit{Optoisolated\ Inputs} \text{ in } \mathit{Section\ 7: Inputs, Outputs, Timers, and Other Control Logic})$$

$$ULTR = \text{IN101}$$

Input IN101 must be energized (52b circuit breaker auxiliary contact has to be closed) before the trip logic unlatches and the TRIP Relay Word bit deasserts to logical 0.

Program an Output Contact for Tripping

In the factory settings, the resultant of the trip logic in Figure 5.1 is routed to output contact OUT101 with the following SELOGIC control equation setting:

$$\text{OUT101} = \text{TRIP}$$

If more than one TRIP output contact is needed, program other output contacts with the TRIP Relay Word bit. Examples of uses for additional TRIP output contacts:

- Tripping more than one breaker
- Keying an external breaker failure relay
- Keying communication equipment in a Direct Transfer Trip scheme

See *Output Contacts* in *Section 7: Inputs, Outputs, Timers, and Other Control Logic* for more information on programming output contacts.

SWITCH-ONTO-FAULT (SOTF) TRIP LOGIC

Switch-Onto-Fault (SOTF) trip logic provides a programmable time window for selected elements to trip right after the circuit breaker closes. “Switch-onto-fault” implies that a circuit breaker is closed into an existing fault condition. For example, suppose safety grounds are accidentally left attached to a line after a clearance. If the circuit breaker is closed into such a condition, the resulting fault needs to be cleared right away and reclosing blocked. An instantaneous overcurrent element is usually set to trip in the three-pole open (3PO) logic and the SOTF trip logic.

Refer to the switch-onto-fault trip logic in Figure 5.1 (middle of figure). The SOTF trip logic permits tripping if both the following occur:

- An element asserts in SELOGIC control equation trip setting TRSOTF
- Relay Word bit SOTFE is asserted to logical 1

Relay Word bit SOTFE (the output of the SOTF logic) provides the effective time window for an element in trip setting TRSOTF (e.g., TRSOTF = 50P2) to trip after the circuit breaker closes. Figure 5.3 and the following discussion describe the three-pole open (3PO) logic and the SOTF logic.

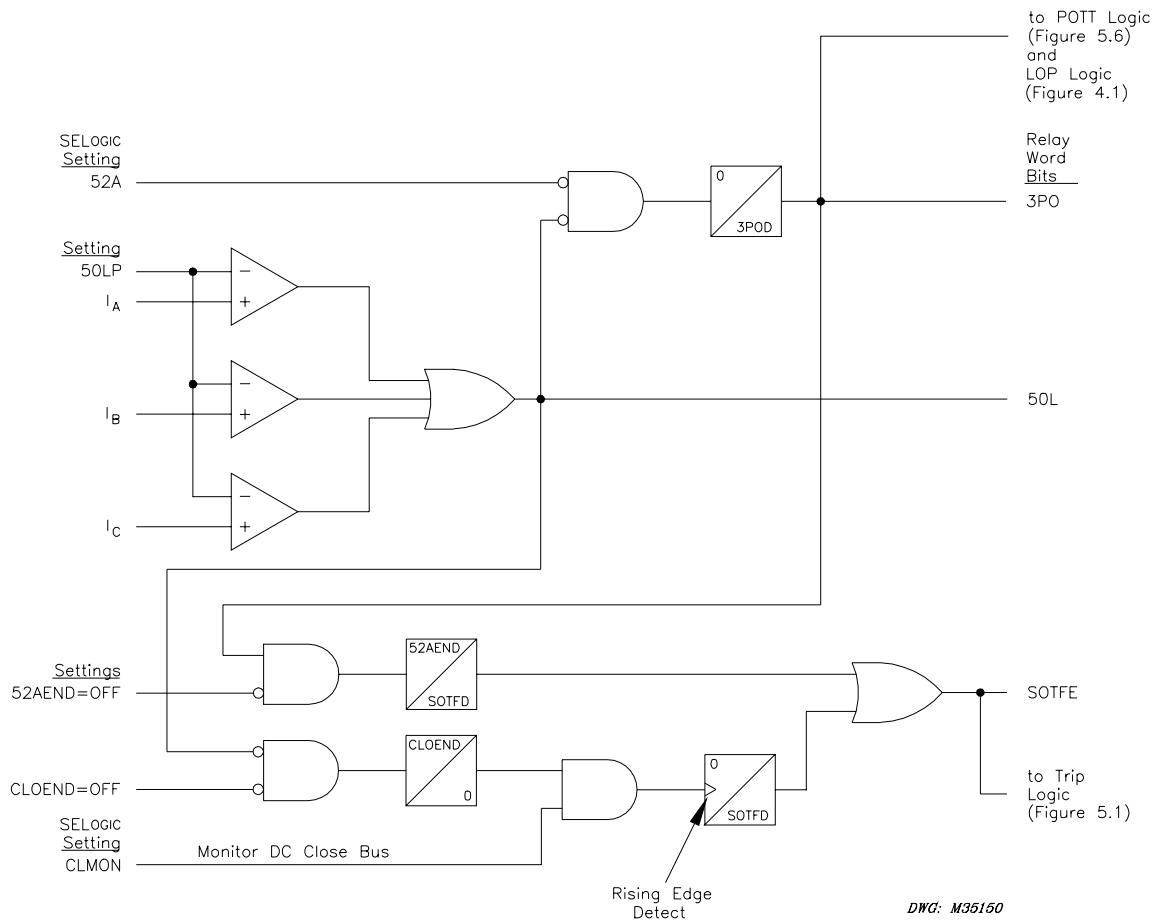


Figure 5.3: Three-Pole Open Logic (Top) and Switch-Onto-Fault Logic (Bottom)

Three-Pole Open Logic

Three-pole open (3PO) logic is the top half of Figure 5.3. It is not affected by enable setting ESOTF (see Settings Sheet 2 of 27 in *Section 9: Setting the Relay*).

The open circuit breaker condition is determined from the combination of:

- Circuit breaker status (52A)
- Load current condition (50L)

If the circuit breaker is open (52A = logical 0) and current is below phase pickup 50LP (50L = logical 0), then the three-pole open (3PO) condition is true:

3PO = logical 1 (circuit breaker open)

The 3POD dropout time qualifies circuit breaker closure, whether detected by circuit breaker status (52A) or load current level (50L). When the circuit breaker is closed:

3PO = logical 0 (circuit breaker closed)

Determining Three-Pole Open Condition Without Circuit Breaker Auxiliary Contact

If a circuit breaker auxiliary contact is not connected to the SEL-351 Relay, SELOGIC control equation setting 52A is set:

$$52A = 0 \quad (\text{numeral } 0)$$

With SELOGIC control equation setting 52A continually at logical 0, 3PO logic is controlled solely by load detection element 50L. Phase pickup 50LP is set below load current levels.

When the circuit breaker is open, Relay Word bit 50L drops out (= logical 0) and the 3PO condition asserts:

$$3PO = \text{logical } 1 \quad (\text{circuit breaker open})$$

When the circuit breaker is closed, Relay Word bit 50L picks up (= logical 0; current above phase pickup 50LP) and the 3PO condition deasserts after the 3POD dropout time:

$$3PO = \text{logical } 0 \quad (\text{circuit breaker closed})$$

Note that the 3PO condition is also routed to the permissive overreaching transfer trip (POTT) logic (see Figure 5.6) and the loss-of-potential (LOP) logic (see Figure 4.1).

Circuit Breaker Operated Switch-Onto-Fault Logic

Circuit breaker operated switch-onto-fault logic is enabled by making time setting 52AEND (52AEND \neq OFF). Time setting 52AEND qualifies the three-pole open (3PO) condition and then asserts Relay Word bit SOTFE:

$$SOTFE = \text{logical } 1$$

Note that SOTFE is asserted when the circuit breaker is open. This allows elements set in the SELOGIC control equation trip setting TRSOTF to operate if a fault occurs when the circuit breaker is open (see Figure 5.1). In such a scenario (e.g., flashover inside the circuit breaker tank), the tripping via setting TRSOTF cannot help in tripping the circuit breaker (the circuit breaker is already open), but can initiate breaker failure protection, if a breaker failure scheme is implemented in the SEL-351 Relay (see output contact OUT103 example in *Output Contacts* in **Section 7: Inputs, Outputs, Timers, and Other Control Logic**) or externally.

When the circuit breaker is closed, the 3PO condition deasserts (3PO = logical 0) after the 3POD dropout time (setting 3POD is usually set for no more than a cycle). The SOTF logic output, SOTFE, continues to remain asserted at logical 1 for dropout time SOTFD time.

Close Bus Operated Switch-Onto-Fault Logic

Close bus operated switch-onto-fault logic is enabled by making time setting CLOEND (CLOEND \neq OFF). Time setting CLOEND qualifies the deassertion of the load detection element 50L (indicating that the circuit breaker is open).

Circuit breaker closure is detected by monitoring the dc close bus. This is accomplished by wiring an optoisolated input on the SEL-351 Relay (e.g., IN105) to the dc close bus. When a manual close or automatic reclosure occurs, optoisolated input IN105 is energized. SELOGIC control equation setting CLMON (close bus monitor) monitors the optoisolated input IN105:

CLMON = IN105

When optoisolated input IN105 is energized, CLMON asserts to logical 1. At the instant that optoisolated input IN105 is energized (close bus is energized), the circuit breaker is still open so the output of the CLOEND timer continues to be asserted to logical 1. Thus, the ANDed combination of these conditions latches in the SOTFD timer. The SOTFD timer outputs a logical 1 for a time duration of “SOTFD” cycles any time it sees a rising edge on its input (logical 0 to logical 1 transition), if it is not already timing. The SOTF logic output, SOTFE, asserts to logical 1 for SOTFD time.

Switch-Onto-Fault Logic Output (SOTFE)

Relay Word bit SOTFE is the output of the circuit breaker operated SOTF logic or the close bus operated SOTF logic described previously. Time setting SOTFD in each of these logic paths provides the effective time window for the overcurrent elements in SELOGIC control equation trip setting TRSOTF to trip after the circuit breaker closes (see Figure 5.1—middle of figure). Time setting SOTFD is usually set around 30 cycles.

A SOTF trip illuminates the SOTF front-panel LED.

Switch-Onto-Fault Trip Logic Trip Setting (TRSOTF)

An instantaneous overcurrent element is usually set to trip in the SELOGIC control equation trip setting TRSOTF (e.g., TRSOTF = 50P2).

If the voltage potential for the relay is from the line-side of the circuit breaker, the instantaneous overcurrent element in the SELOGIC control equation trip setting TRSOTF should be nondirectional. When the circuit breaker is open and the line is deenergized, the relay sees zero voltage. If a close-in three-phase fault condition exists on the line (e.g., safety grounds accidentally left attached to the line after a clearance) and then the circuit breaker is closed, the relay continues to see zero voltage. The directional elements have no voltage for reference and cannot operate. In this case, the instantaneous overcurrent element in the SOTF trip logic should be nondirectional.

COMMUNICATIONS-ASSISTED TRIP LOGIC –GENERAL OVERVIEW

The SEL-351 Relay includes communications-assisted tripping schemes that provide unit-protection for transmission lines with the help of communications. No external coordination devices are required.

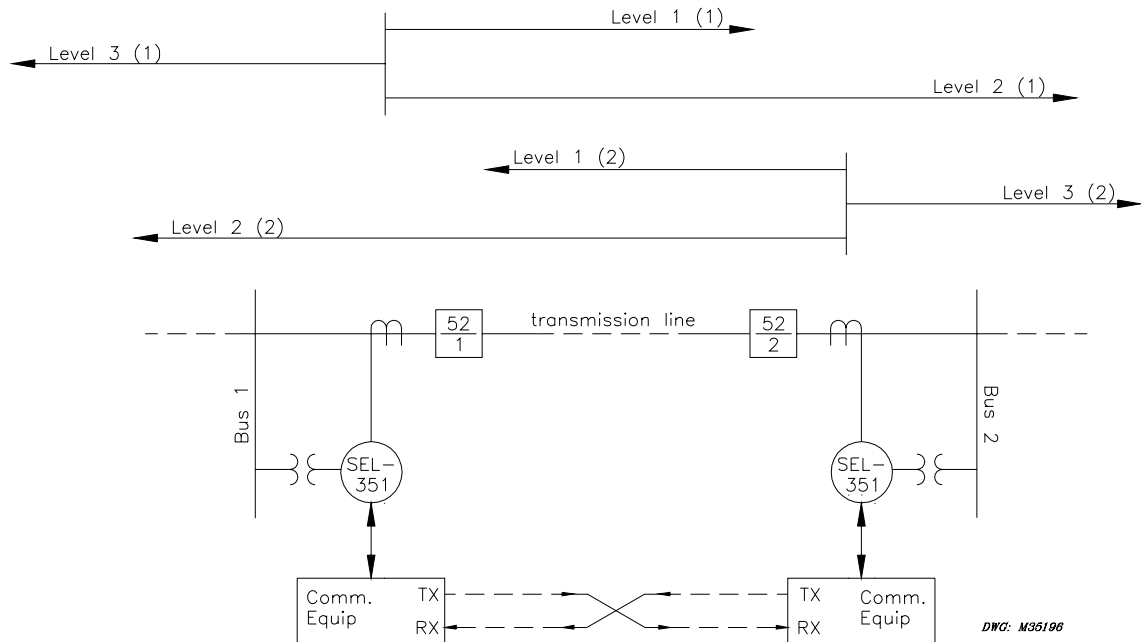


Figure 5.4: Communications-Assisted Tripping Scheme

Refer to Figure 5.4 and the top half of Figure 5.1.

The six available tripping schemes are:

- Direct Transfer Trip (DTT)
- Direct Underreaching Transfer Trip (DUTT)
- Permissive Overreaching Transfer Trip (POTT)
- Permissive Underreaching Transfer Trip (PUTT)
- Directional Comparison Unblocking (DCUB)
- Directional Comparison Blocking (DCB)

Enable Setting ECOMM

The POTT, PUTT, DCUB, and DCB tripping schemes are enabled with enable setting ECOMM. Setting choices are:

ECOMM = N	[no communications-assisted trip scheme enabled]
ECOMM = POTT	[POTT or PUTT scheme]
ECOMM = DCUB1	[DCUB scheme for two-terminal line (communications from <u>one</u> remote terminal)]

ECOMM = DCUB2 [DCUB scheme for three-terminal line (communications from
two remote terminals)]
ECOMM = DCB [DCB scheme]

These tripping schemes can all work in two-terminal or three-terminal line applications. The DCUB scheme requires separate settings choices for these applications (ECOMM = DCUB1 or DCUB2) because of unique DCUB logic considerations.

In most cases, these tripping schemes require (see Figure 5.4):

- Level 1 underreaching overcurrent elements set direction forward (setting DIR1 = F)
- Level 2 overreaching overcurrent elements set direction forward (setting DIR2 = F)
- Level 3 overcurrent elements set direction reverse (setting DIR3 = R)

See *Directional Control Settings*, in *Section 4: Loss-of-Potential, Load Encroachment, and Directional Element Logic* for more information on level direction settings DIR1 through DIR4.

POTT, PUTT, DCUB, and DCB communications-assisted tripping schemes are explained in subsections that follow.

Trip Setting TRCOMM

The POTT, PUTT, DCUB, and DCB tripping schemes use SELOGIC control equation trip setting TRCOMM for those tripping elements that are supervised by the communications-assisted trip logic (see top half of Figure 5.1). Setting TRCOMM is typically set with Level 2 overreaching overcurrent elements (set direction forward):

- 67P2 Level 2 directional phase instantaneous overcurrent element
- 67N2 Level 2 directional neutral ground instantaneous overcurrent element
- 67G2 Level 2 directional residual ground instantaneous overcurrent element
- 67Q2 Level 2 directional negative-sequence instantaneous overcurrent element

The exception is a DCB scheme, where Level 2 overreaching overcurrent elements (set direction forward) with a short delay are used instead:

- 67P2S Level 2 directional phase instantaneous overcurrent element (with delay 67P2SD)
- 67N2S Level 2 directional neutral ground instantaneous overcurrent element (with delay 67N2SD)
- 67G2S Level 2 directional residual ground instantaneous overcurrent element (with delay 67G2SD)
- 67Q2S Level 2 directional negative-sequence instantaneous overcurrent element (with delay 67Q2SD)

The short delays provide necessary carrier coordination delays (waiting for the block trip signal).

Trip Settings TRSOTF and TR

In a communications-assisted trip scheme, the SELOGIC control equation trip settings TRSOTF and TR can also be used, in addition to setting TRCOMM.

Setting TRSOTF can be set as described in preceding subsection *Switch-Onto-Fault (SOTF) Trip Logic*.

Setting TR is typically set with unsupervised Level 1 underreaching overcurrent elements (set direction forward):

- 67P1 Level 1 directional phase instantaneous overcurrent element
- 67N1 Level 1 directional neutral ground instantaneous overcurrent element
- 67G1 Level 1 directional residual ground instantaneous overcurrent element
- 67Q1 Level 1 directional negative-sequence instantaneous overcurrent element

and other time delayed elements (e.g., Level 2 definite-time overcurrent elements).

Trip Setting DTT

The DTT and DUTT tripping schemes are realized with SELOGIC control equation trip setting DTT, discussed at the beginning of this section.

Use Existing SEL-321 Relay Application Guides for the SEL-351 Relay

The communications-assisted tripping schemes settings in the SEL-351 Relay are very similar to those in the SEL-321 Relay. Existing SEL-321 Relay application guides can also be used in setting up these schemes in the SEL-351 Relay. The following application guides are available from SEL:

- AG93-06** *Applying the SEL-321 Relay to Directional Comparison Blocking (DCB) Schemes*
- AG95-29** *Applying the SEL-321 Relay to Permissive Overreaching Transfer Trip (POTT) Schemes*
- AG96-19** *Applying the SEL-321 Relay to Directional Comparison Unblocking (DCUB) Schemes*

The major differences are how the optoisolated input settings and the trip settings are made. The following explanations describe these differences.

Optoisolated Input Settings Differences Between the SEL-321 and SEL-351 Relays

The SEL-351 Relay does not have optoisolated input settings like the SEL-321 Relay. Rather, the optoisolated inputs of the SEL-351 Relay are available because Relay Word bits are used in SELOGIC control equations. The following optoisolated input setting example is for a Permissive Overreaching Transfer Trip (POTT) scheme.

<u>SEL-321 Relay</u>	<u>SEL-351 Relay</u>	
IN102 = PT	PT1 = IN102	(received permissive trip)

In the above SEL-351 Relay setting example, Relay Word bit IN102 is set in the PT1 SELOGIC control equation. Optoisolated input IN102 is wired to a communications equipment receiver output contact. Relay Word bit IN102 can also be used in other SELOGIC control equation in the SEL-351 Relay. See *Optoisolated Inputs* in *Section 7: Inputs, Outputs, Timers, and Other Control Logic* for more information on optoisolated inputs.

Trip Settings Differences Between the SEL-321 and SEL-351 Relays

Some of the SELOGIC control equation trip settings of the SEL-321 and SEL-351 Relays are not operationally different, just labeled differently. The correspondence is:

<u>SEL-321 Relay</u>	<u>SEL-351 Relay</u>	
MTCS	TRCOMM	(Communications-Assisted Trip Conditions)
MTO	TRSOTF	(Switch-Onto-Fault Trip Conditions)
MTU	TR	(Unconditional or Other Trip Conditions)

The SEL-321 Relay handles trip unlatching with setting TULO. The SEL-351 Relay handles trip unlatching with SELOGIC control equation setting ULTR.

The SEL-321 Relay has single-pole trip logic. The SEL-351 Relay does not have single-pole trip logic.

PERMISSIVE OVERREACHING TRANSFER TRIP (POTT) LOGIC

Enable the POTT logic by setting ECOMM = POTT. The POTT logic in Figure 5.6 is also enabled for directional comparison unblocking schemes (ECOMM = DCUB1 or ECOMM = DCUB2). The POTT logic performs the following tasks:

- Keys communication equipment to send permissive trip when any element included in the SELOGIC control equation communications-assisted trip equation TRCOMM asserts and the current reversal logic is not asserted.
- Prevents keying and tripping by the POTT logic following a current reversal.
- Echoes the received permissive signal to the remote terminal.
- Prevents channel lockup during echo and test.
- Provides a secure means of tripping for weak- and/or zero-infeed line terminals.

Use Existing SEL-321 Relay POTT Application Guide for the SEL-351 Relay

Use the existing SEL-321 Relay POTT application guide (AG95-29) to help set up the SEL-351 Relay in a POTT scheme (see preceding subsection *Communications-Assisted Trip Logic—General Overview* for more setting comparison information on the SEL-321/SEL-351 Relays).

External Inputs

See *Optoisolated Inputs* in *Section 7: Inputs, Outputs, Timers, and Other Control Logic* for more information on optoisolated inputs.

PT1–Received Permissive Trip Signal(s)

In two-terminal line POTT applications, a permissive trip signal is received from one remote terminal. One optoisolated input on the SEL-351 Relay (e.g., input IN104) is driven by a communications equipment receiver output (see Figure 5.8). Make SELOGIC control equation setting PT1:

$$PT1 = IN104 \quad (\text{two-terminal line application})$$

In three-terminal line POTT applications, permissive trip signals are received from two remote terminals. Two optoisolated inputs on the SEL-351 Relay (e.g., input IN104 and IN106) are driven by communications equipment receiver outputs (see Figure 5.9). Make SELOGIC control equation setting PT1 as follows:

$$PT1 = IN104 * IN106 \quad (\text{three-terminal line application})$$

SELOGIC control equation setting PT1 in Figure 5.5 is routed to control Relay Word bit PT if enable setting ECOMM = POTT. Relay Word bit PT is then an input into the POTT logic in Figure 5.6 (for echo keying).

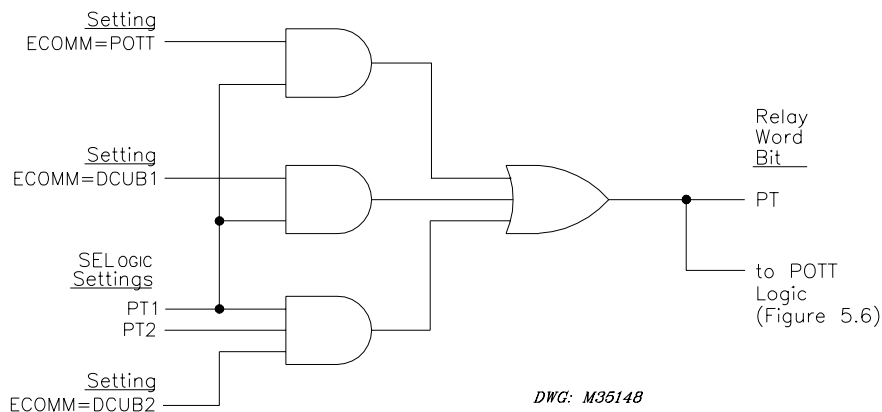


Figure 5.5: Permissive Input Logic Routing to POTT Logic

Also note that SELOGIC control equation setting PT1 in Figure 5.7 is routed to control Relay Word bit PTRX if enable setting ECOMM = POTT. Relay Word bit PTRX is the permissive trip receive input into the trip logic in Figure 5.1.

Timer Settings

See *Section 9: Setting the Relay* for setting ranges.

Z3RBD–Zone (Level) 3 Reverse Block Delay

Current-reversal guard timer—typically set at 5 cycles.

EBLKD–Echo Block Delay

Prevents echoing of received PT for settable delay after dropout of local permissive elements in trip setting TRCOMM—typically set at 10 cycles. Set to OFF to defeat EBLKD.

ETDPU –Echo Time Delay Pickup

Sets minimum time requirement for received PT, before echo begins—typically set at 2 cycles.
Set to OFF for no echo.

EDURD –Echo Duration

Limits echo duration, to prevent channel lockup—typically set at 3.5 cycles.

Logic Outputs

The following logic outputs can be tested by assigning them to output contacts. See *Output Contacts* in *Section 7: Inputs, Outputs, Timers, and Other Control Logic* for more information on output contacts.

Z3RB –Zone (Level) 3 Reverse Block

Current-reversal guard asserted (operates as an input into the trip logic in Figure 5.1 and the DCUB logic in Figure 5.10).

ECTT –Echo Conversion to Trip

PT received, converted to a trip condition for a Weak-Infeed Condition (operates as an input into the trip logic in Figure 5.1).

KEY –Key Permissive Trip

Signals communications equipment to transmit permissive trip. For example, SELOGIC control equation setting OUT105 is set:

$$\text{OUT105} = \text{KEY}$$

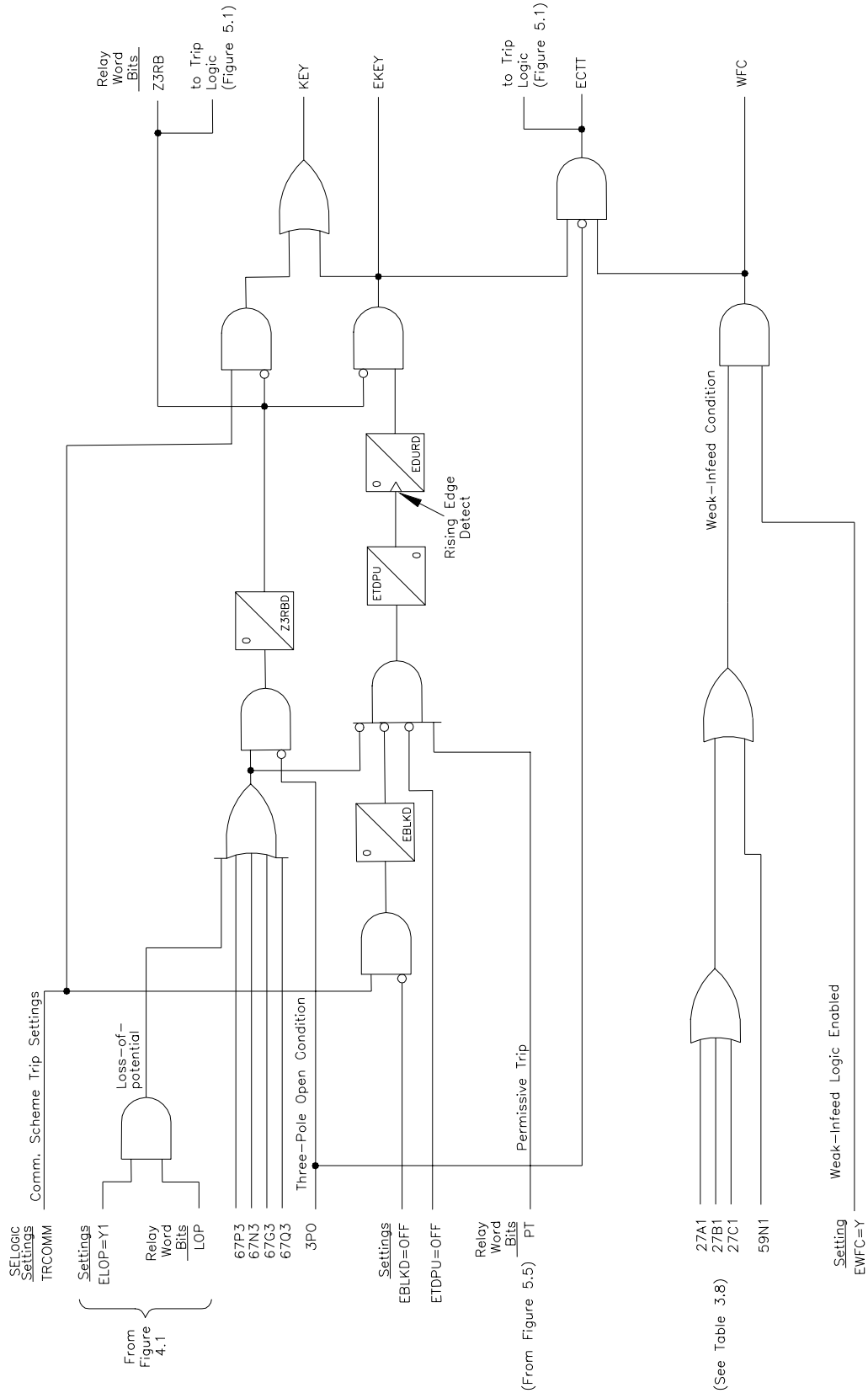
Output contact OUT105 drives a communications equipment transmitter input in a two-terminal line application (see Figure 5.8).

In a three-terminal line scheme, output contact OUT107 is set the same as OUT105 (see Figure 5.9):

$$\text{OUT107} = \text{KEY}$$

EKEY –Echo Key Permissive Trip

Permissive trip signal keyed by Echo logic (used in testing).



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Figure 5.6: POTT Logic

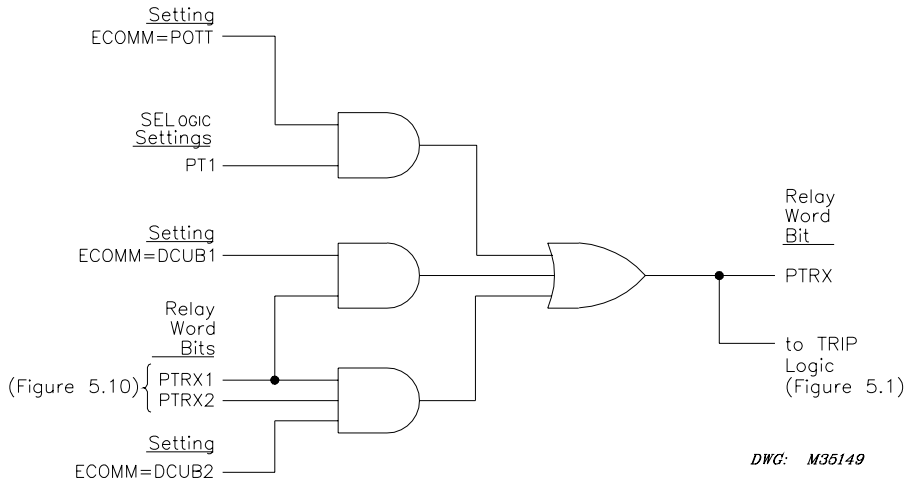


Figure 5.7: Permissive Input Logic Routing to Trip Logic

Variations for Permissive Underreaching Transfer Trip (PUTT) Scheme

Refer to Figure 5.4 and Figure 5.6. In a PUTT scheme, keying is provided by Level 1 underreaching overcurrent elements (set direction forward), instead of with Relay Word bit KEY. This is accomplished by setting output contact OUT105 with these elements:

- 67P1 Level 1 directional phase instantaneous overcurrent element
- 67N1 Level 1 directional neutral ground instantaneous overcurrent element
- 67G1 Level 1 directional residual ground instantaneous overcurrent element
- 67Q1 Level 1 directional negative-sequence instantaneous overcurrent element

instead of with element KEY (see Figure 5.8):

$$\text{OUT105} = 67\text{P1} + 67\text{N1} + 67\text{G1} + 67\text{Q1} \quad (\text{Note: only use enabled elements})$$

If echo keying is desired, add the echo key permissive trip logic output, as follows:

$$\text{OUT105} = 67\text{P1} + 67\text{N1} + 67\text{G1} + 67\text{Q1} + \text{EKEY}$$

In a three-terminal line scheme, output contact OUT107 is set the same as OUT105 (see Figure 5.9).

Installation Variations

Figure 5.9 shows output contacts OUT105 and OUT107 connected to separate communication equipment, for the two remote terminals. Both output contacts are programmed the same (OUT105 = KEY and OUT107 = KEY).

Depending on the installation, perhaps one output contact (e.g., OUT105 = KEY) could be connected in parallel to both transmitter inputs (TX) on the communication equipment in Figure 5.9. Then output contact OUT107 can be used for another function.

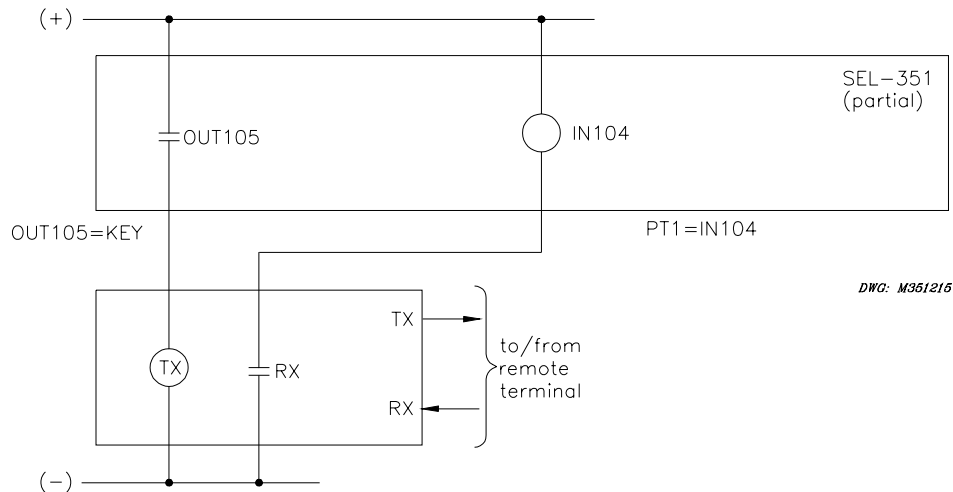


Figure 5.8: SEL-351 Relay Connections to Communications Equipment for a Two-Terminal Line POTT Scheme

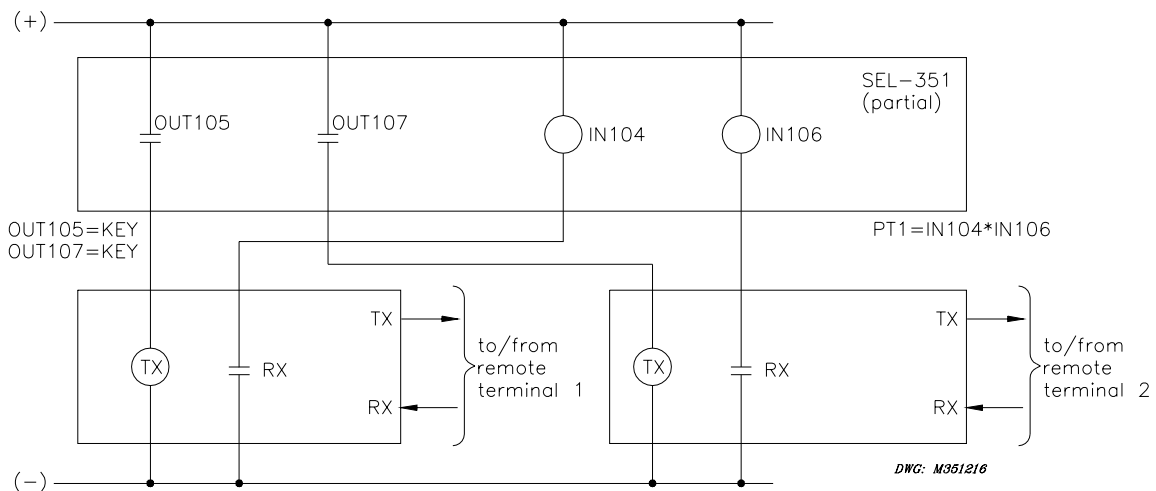


Figure 5.9: SEL-351 Relay Connections to Communications Equipment for a Three-Terminal Line POTT Scheme

DIRECTIONAL COMPARISON UNBLOCKING (DCUB) LOGIC

Enable the DCUB logic by setting $E\text{COMM} = \text{DCUB1}$ or $E\text{COMM} = \text{DCUB2}$. The DCUB logic in Figure 5.10 is an extension of the POTT logic in Figure 5.6. Thus, the relay requires all the POTT settings and logic, plus exclusive DCUB settings and logic. The difference between setting choices DCUB1 and DCUB2 is:

- DCUB1 directional comparison unblocking scheme for two-terminal line (communications from one remote terminal)
- DCUB2 directional comparison unblocking scheme for three-terminal line (communications from two remote terminals)

The DCUB logic in Figure 5.10 takes in the loss-of-guard and permissive trip outputs from the communication receivers (see Figure 5.12 and Figure 5.13) and makes permissive (PTRX1/PTRX2) and unblocking block (UBB1/UBB2) logic output decisions.

DCUB schemes are typically implemented with FSK (frequency shift carrier) or analog microwave as the communications medium.

Use Existing SEL-321 Relay DCUB Application Guide for the SEL-351 Relay

Use the existing SEL-321 Relay DCUB application guide (AG96-19) to help set up the SEL-351 Relay in a DCUB scheme (see preceding subsection *Communications-Assisted Trip Logic—General Overview* for more setting comparison information on the SEL-321/SEL-351 Relays).

External Inputs

See *Optoisolated Inputs* in *Section 7: Inputs, Outputs, Timers, and Other Control Logic* for more information on optoisolated inputs.

PT1, PT2—Received Permissive Trip Signal(s)

In two-terminal line DCUB applications (setting ECOMM = DCUB1), a permissive trip signal is received from one remote terminal. One optoisolated input on the SEL-351 Relay (e.g., input IN104) is driven by a communications equipment receiver output (see Figure 5.12). Make SELOGIC control equation setting PT1:

$$PT1 = IN104 \quad \text{(two-terminal line application)}$$

In three-terminal line DCUB applications (setting ECOMM = DCUB2), permissive trip signals are received from two remote terminals. Two optoisolated inputs on the SEL-351 Relay (e.g., inputs IN104 and IN106) are driven by communications equipment receiver outputs (see Figure 5.13). Make SELOGIC control equation settings PT1 and PT2 as follows:

$$PT1 = IN104 \quad \text{(three-terminal line application)}$$
$$PT2 = IN106$$

SELOGIC control equation settings PT1 and PT2 are routed into the DCUB logic in Figure 5.10 for “unblocking block” and “permissive trip receive” logic decisions.

As explained in the preceding POTT subsection, the SELOGIC control equation settings PT1 and PT2 in Figure 5.5 are routed in various combinations to control Relay Word bit PT, depending on enable setting ECOMM = DCUB1 or DCUB2. Relay Word bit PT is then an input into the POTT logic in Figure 5.6 (for echo keying).

LOG1, LOG2 –Loss-of-Guard Signal(s)

In two-terminal line DCUB applications (setting ECOMM = DCUB1), a loss-of-guard signal is received from one remote terminal. One optoisolated input on the SEL-351 Relay (e.g., input IN105) is driven by a communications equipment receiver output (see Figure 5.12). Make SELOGIC control equation setting LOG1:

LOG1 = IN105 (two-terminal line application)

In three-terminal line DCUB applications (setting ECOMM = DCUB2), loss-of-guard signals are received from two remote terminals. Two optoisolated inputs on the SEL-351 Relay (e.g., input IN105 and IN207) are driven by communications equipment receiver outputs (see Figure 5.13). Make SELOGIC control equation settings LOG1 and LOG2 as follows:

LOG1 = IN105 (three-terminal line application)
LOG2 = IN207

SELOGIC control equation settings LOG1 and LOG2 are routed into the DCUB logic in Figure 5.10 for “unblocking block” and “permissive trip receive” logic decisions.

Timer Settings

See *Section 9: Setting the Relay* for setting ranges.

GARD1D –Guard-Present Delay

Sets minimum time requirement for reinstating permissive tripping following a loss-of-channel condition—typically set at 10 cycles. Channel 1 and 2 logic use separate timers but have this same delay setting.

UBDURD –DCUB Disable Delay

Prevents tripping by POTT logic after a settable time following a loss-of-channel condition—typically set at 9 cycles (150 ms). Channel 1 and 2 logic use separate timers but have this same delay setting.

UBEND –DCUB Duration Delay

Sets minimum time required to declare a loss-of-channel condition—typically set at 0.5 cycles. Channel 1 and 2 logic use separate timers but have this same delay setting.

Logic Outputs

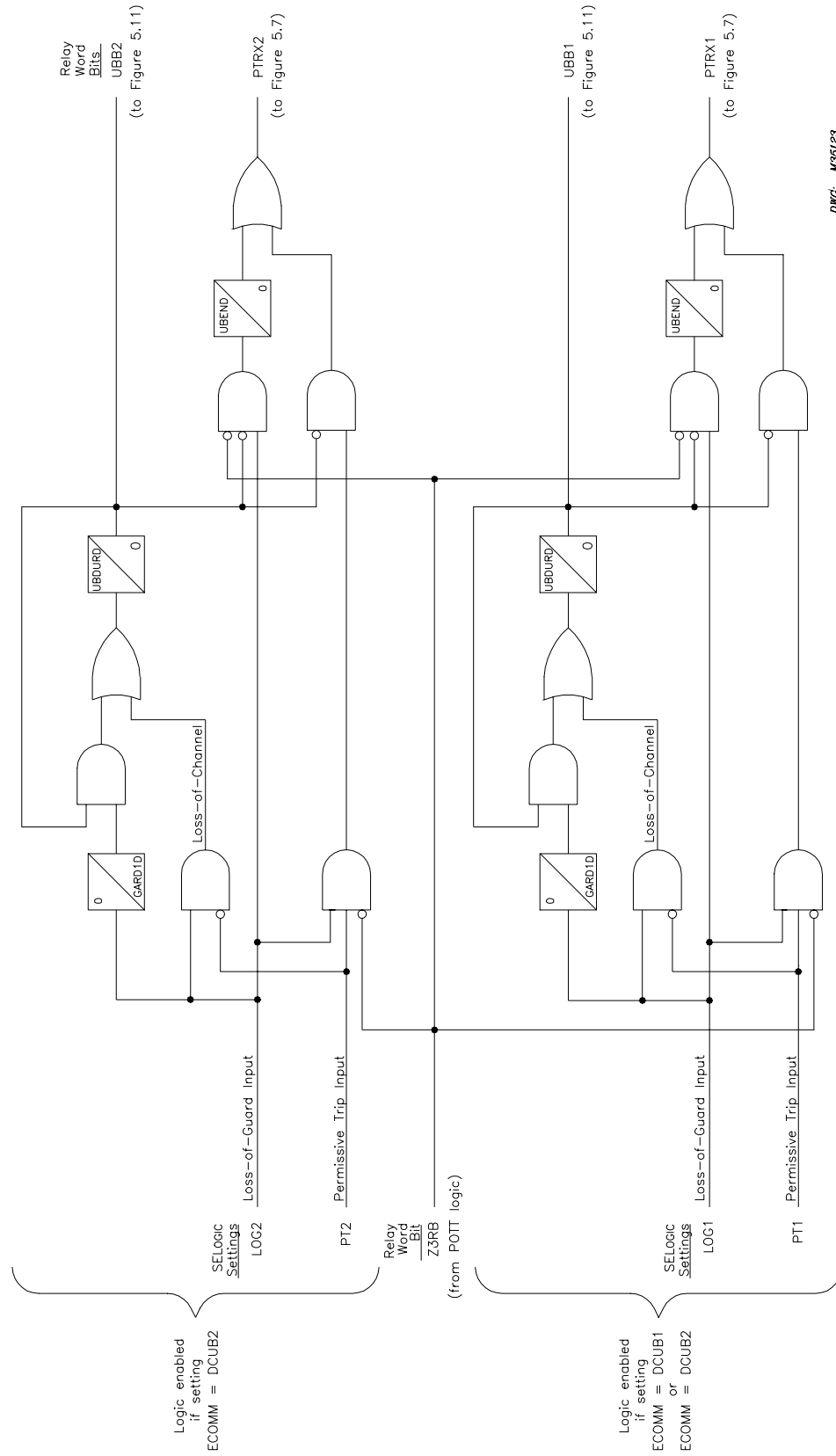
The following logic outputs can be tested by assigning them to output contacts. See *Output Contacts* in *Section 7: Inputs, Outputs, Timers, and Other Control Logic* for more information on output contacts.

UBB1, UBB2 –Unblocking Block Output(s)

In two-terminal line DCUB applications (setting ECOMM = DCUB1), UBB1 disables tripping if the loss-of-channel condition continues for longer than time UBDURD.

In three-terminal line DCUB applications (setting ECOMM = DCUB2), UBB1 or UBB2 disable tripping if the loss-of-channel condition (for the respective Channel 1 or 2) continues for longer than time UBDURD.

The UBB1 and UBB2 are routed in various combinations in Figure 5.11 to control Relay Word bit UBB, depending on enable setting ECOMM = DCUB1 or DCUB2. Relay Word bit UBB is the unblock block input into the trip logic in Figure 5.1. When UBB asserts to logical 1, tripping is blocked.



DWG: M35123

Figure 5.10: DCUB Logic

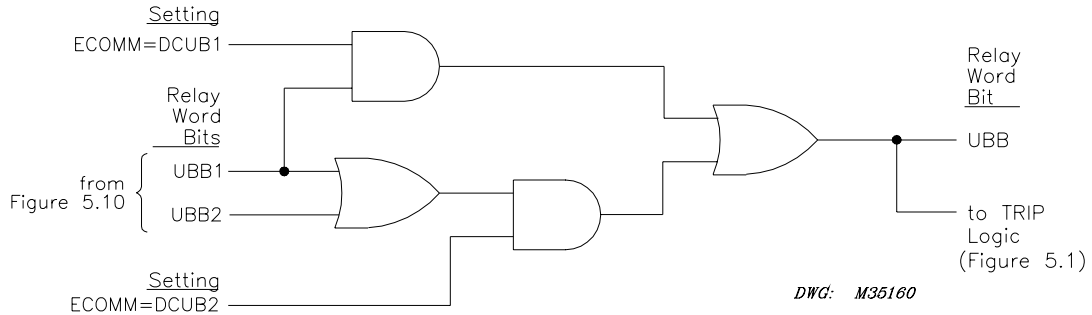


Figure 5.11: Unblocking Block Logic Routing to Trip Logic

PTRX1, PTRX2—Permissive Trip Receive Outputs

In two-terminal line DCUB applications (setting ECOMM = DCUB1), PTRX1 asserts for loss-of-channel or an actual received permissive trip.

In three-terminal line DCUB applications (setting ECOMM = DCUB2), PTRX1 or PTRX2 assert for loss-of-channel or an actual received permissive trip (for the respective Channel 1 or 2).

The PTRX1/PTRX2 Relay Word bits are then routed in various combinations in Figure 5.7 to control Relay Word bit PTRX, depending on enable setting ECOMM = DCUB1 or DCUB2. Relay Word bit PTRX is the permissive trip receive input into the trip logic in Figure 5.1.

Installation Variations

Figure 5.13 shows output contacts OUT105 and OUT107 connected to separate communication equipment, for the two remote terminals. Both output contacts are programmed the same (OUT105 = KEY and OUT107 = KEY).

Depending on the installation, perhaps one output contact (e.g., OUT105 = KEY) could be connected in parallel to both transmitter inputs (TX) on the communication equipment in Figure 5.13. Then output contact OUT107 can be used for another function.

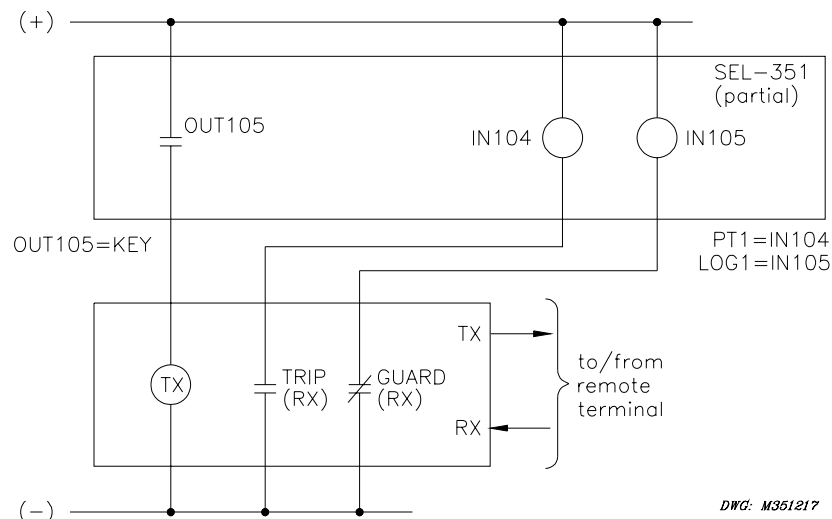


Figure 5.12: SEL-351 Relay Connections to Communications Equipment for a Two-Terminal Line DCUB Scheme (Setting ECOMM = DCUB1)

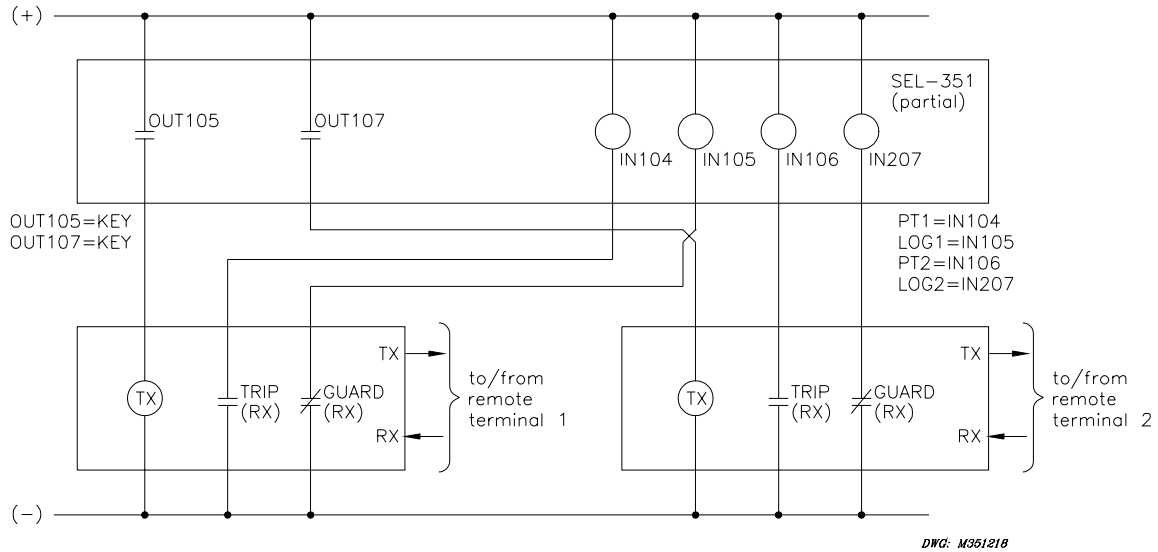


Figure 5.13: SEL-351 Relay Connections to Communications Equipment for a Three-Terminal Line DCUB Scheme (Setting ECOMM = DCUB2)

DIRECTIONAL COMPARISON BLOCKING (DCB) LOGIC

Enable the DCB logic by setting ECOMM = DCB. The DCB logic in Figure 5.14 performs the following tasks:

- Provides the individual carrier coordination timers for the Level 2 directional overcurrent elements 67P2S, 67N2S, 67G2S, and 67Q2S. These delays allow time for the block trip signal to arrive from the remote terminal.
- Instantaneously keys the communications equipment to transmit block trip for reverse faults and extends this signal for a settable time following the dropout of all Level 3 directional overcurrent elements 67P3, 67N3, 67G3, and 67Q3.
- Latches the block trip send condition by the directional overcurrent following a close-in zero-voltage three-phase fault where the polarizing memory expires. Latch is removed when the polarizing memory voltage returns or current is removed.
- Extends the received block signal by a settable time.

Use Existing SEL-321 Relay DCB Application Guide for the SEL-351 Relay

Use the existing SEL-321 Relay DCB application guide (AG93-06) to help set up the SEL-351 Relay in a DCB scheme (see preceding subsection *Communications-Assisted Trip Logic—General Overview* for more setting comparison information on the SEL-321/SEL-351 Relays).

External Inputs

See *Optoisolated Inputs* in *Section 7: Inputs, Outputs, Timers, and Other Control Logic* for more information on optoisolated inputs.

BT—Received Block Trip Signal(s)

In two-terminal line DCB applications, a block trip signal is received from one remote terminal. One optoisolated input on the SEL-351 Relay (e.g., input IN104) is driven by a communications equipment receiver output (see Figure 5.15). Make SELOGIC control equation setting BT:

$$BT = IN104 \quad \text{(two-terminal line application)}$$

In three-terminal line DCB applications, block trip signals are received from two remote terminals. Two optoisolated inputs on the SEL-351 Relay (e.g., input IN104 and IN106) are driven by communications equipment receiver outputs (see Figure 5.16). Make SELOGIC control equation setting BT as follows:

$$BT = IN104 + IN106 \quad \text{(three-terminal line application)}$$

SELOGIC control equation setting BT is routed through a dropout timer (BTXD) in the DCB logic in Figure 5.14. The timer output, Relay Word bit BTX, is routed to the trip logic in Figure 5.1.

Timer Settings

See *Section 9: Setting the Relay* for setting ranges.

Z3XPU—Zone (Level) 3 Reverse Pickup Time Delay

Current-reversal guard pickup timer—typically set at 1 cycle.

Z3XD—Zone (Level) 3 Reverse Dropout Extension

Current-reversal guard dropout timer—typically set at 5 cycles.

BTXD—Block Trip Receive Extension

Sets reset time of block trip received condition (BTX) after the reset of block trip input BT.

67P2SD, 67N2SD, 67G2SD, 67Q2SD—Level 2 Short Delay

Carrier coordination delays for the output of Level 2 overreaching overcurrent elements 67P2S, 67N2S, 67G2S, and 67Q2S, respectively—typically set at 1 cycle.

Logic Outputs

The following logic outputs can be tested by assigning them to output contacts. See *Output Contacts* in *Section 7: Inputs, Outputs, Timers, and Other Control Logic* for more information on output contacts.

DSTRT –Directional Carrier Start

Program an output contact for directional carrier start. For example, SELOGIC control equation setting OUT105 is set:

$$\text{OUT105} = \text{DSTRT}$$

Output contact OUT105 drives a communications equipment transmitter input in a two-terminal line application (see Figure 5.15).

In a three-terminal line scheme, output contact OUT107 is set the same as OUT105 (see Figure 5.16):

$$\text{OUT107} = \text{DSTRT}$$

DSTART includes current reversal guard logic.

NSTRT –Nondirectional Carrier Start

Program an output contact to include nondirectional carrier start, in addition to directional start. For example, SELOGIC control equation setting OUT105 is set:

$$\text{OUT105} = \text{DSTRT} + \text{NSTRT}$$

Output contact OUT105 drives a communications equipment transmitter input in a two-terminal line application (see Figure 5.15).

In a three-terminal line scheme, output contact OUT107 is set the same as OUT105 (see Figure 5.16):

$$\text{OUT107} = \text{DSTRT} + \text{NSTRT}$$

STOP –Stop Carrier

Program to an output contact to stop carrier. For example, SELOGIC control equation setting OUT106 is set:

$$\text{OUT106} = \text{STOP}$$

Output contact OUT106 drives a communications equipment transmitter input in a two-terminal line application (see Figure 5.15).

In a three-terminal line scheme, output contact OUT208 is set the same as OUT106 (see Figure 5.16):

$$\text{OUT208} = \text{STOP}$$

BTX –Block Trip Extension

The received block trip input (e.g., BT = IN104) is routed through a dropout timer (BTXD) in the DCB logic in Figure 5.14. The timer output (BTX) is routed to the trip logic in Figure 5.1.

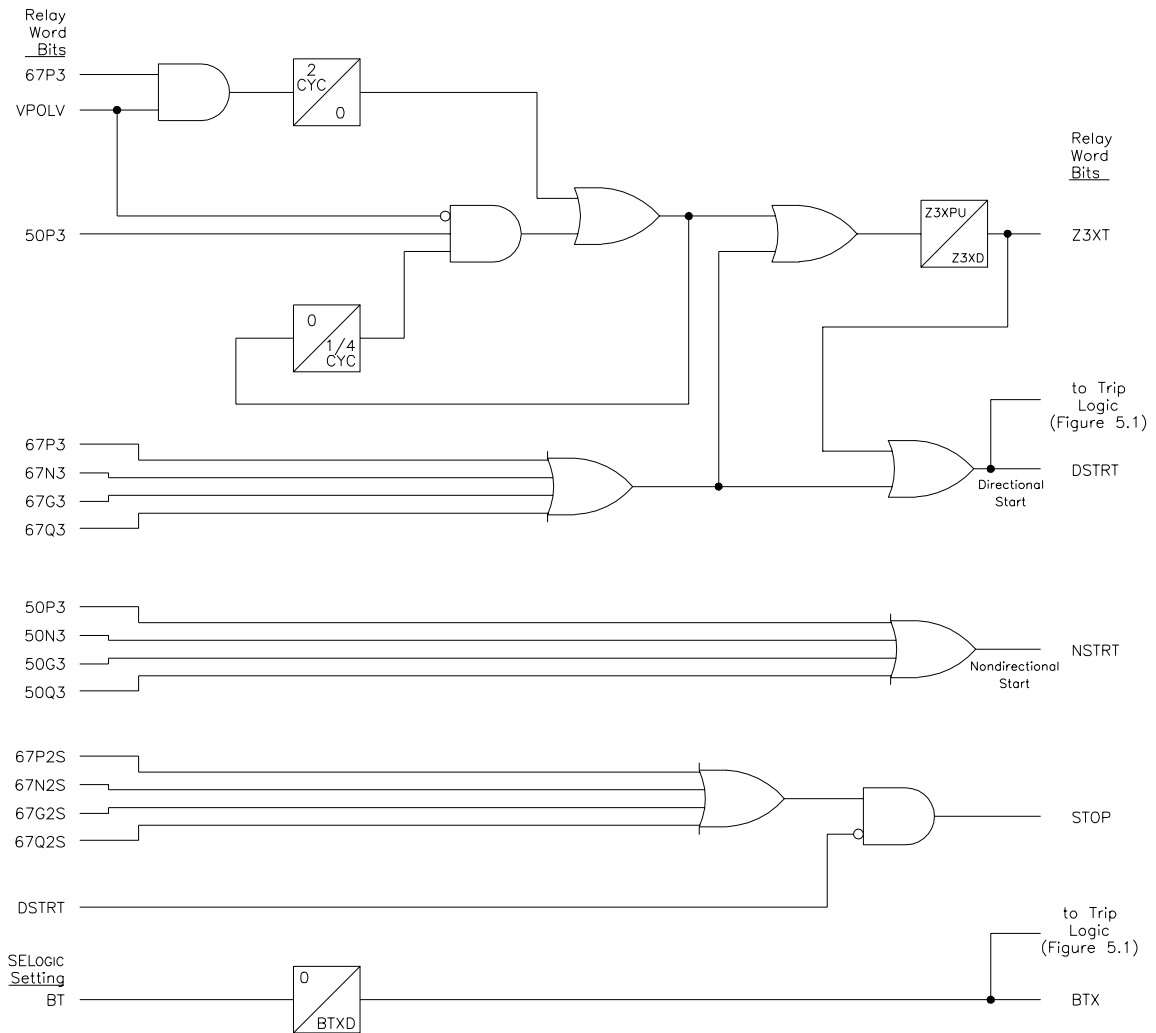


Figure 5.14: DCB Logic

Installation Variations

Figure 5.16 shows output contacts OUT105, OUT106, OUT107, and OUT208 connected to separate communication equipment, for the two remote terminals. Both output contact pairs are programmed the same (OUT105 = DSTRT + NSTRT and OUT107 = DSTRT + NSTRT; OUT106 = STOP and OUT208 = STOP).

Depending on the installation, perhaps one output contact (e.g., OUT105 = DSTRT + NSTRT) can be connected in parallel to both START inputs on the communication equipment in Figure 5.16. Then output contact OUT107 can be used for another function.

Depending on the installation, perhaps one output contact (e.g., OUT106 = STOP) can be connected in parallel to both STOP inputs on the communication equipment in Figure 5.16. Then output contact OUT208 can be used for another function.

Figure 5.16 also shows communication equipment RX (receive) output contacts from each remote terminal connected to separate inputs IN104 and IN106 on the SEL-351 Relay. The inputs

operate as block trip receive inputs for the two remote terminals and are used in the SELOGIC control equation setting:

$$BT = IN104 + IN106$$

Depending on the installation, perhaps one input (e.g., IN104) can be connected in parallel to both communication equipment RX (receive) output contacts in Figure 5.16. Then setting BT would be programmed as:

$$BT = IN104$$

and input IN106 can be used for another function.

In Figure 5.15 and Figure 5.16, the carrier scheme cutout switch contact (85CO) should be closed when the communications equipment is taken out of service so that the BT input of the relay remains asserted. An alternative to asserting the BT input is to change to a setting group where the DCB logic is not enabled.

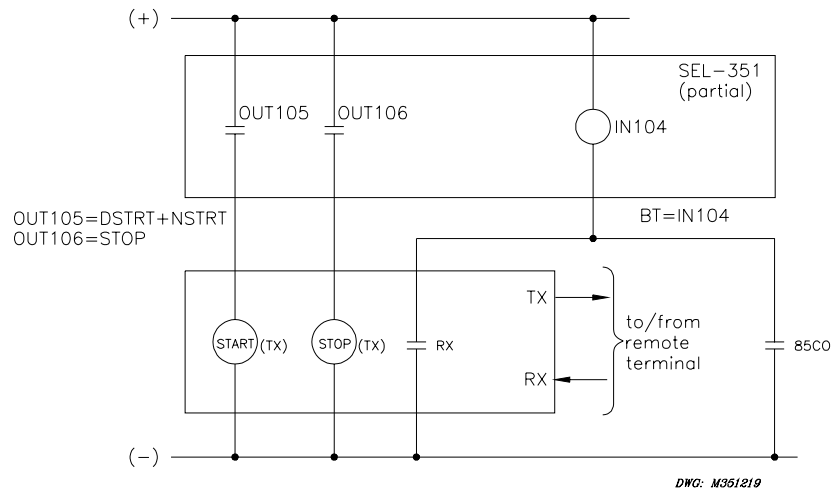


Figure 5.15: SEL-351 Relay Connections to Communications Equipment for a Two-Terminal Line DCB Scheme

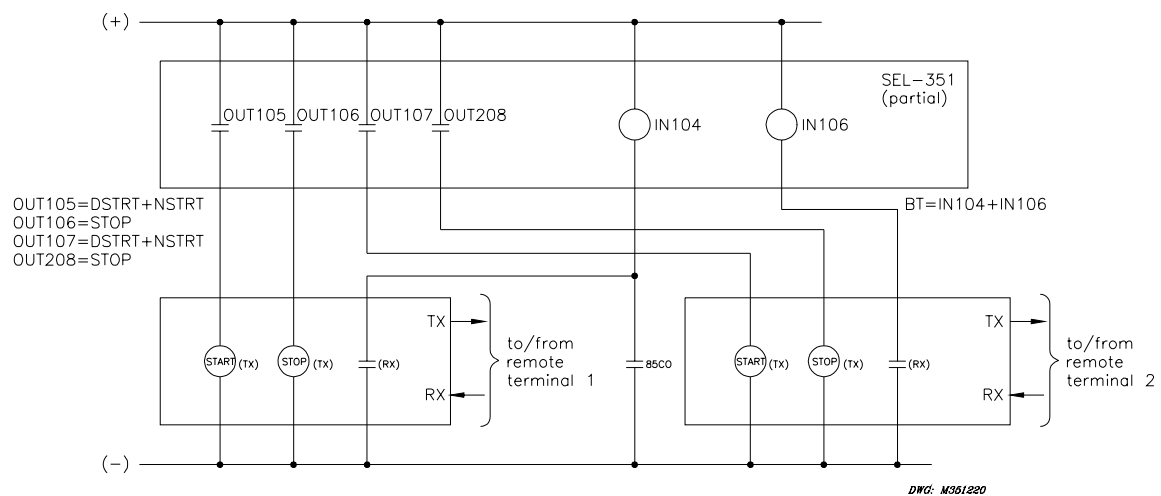


Figure 5.16: SEL-351 Relay Connections to Communications Equipment for a Three-Terminal Line DCB Scheme

FRONT-PANEL TARGET LEDs

Table 5.1: SEL-351 Relay Front-Panel Target LED Definitions

LED Number	LED Label	Definition
1	EN	Relay Enabled—see subsection <i>Relay Self-Tests</i> in <i>Section 13: Testing and Troubleshooting</i>
2	TRIP	Indication that a trip occurred, by overcurrent element, frequency element, or otherwise
3	INST	Instantaneous trip
4	COMM	Communications-assisted trip
5	SOTF	Switch-onto-fault trip
6	50	Instantaneous/definite time overcurrent element generated trip
7	51	Time-overcurrent element generated trip
8	81	Frequency element generated trip
9	A	Phase A involved in the fault
10	B	Phase B involved in the fault
11	C	Phase C involved in the fault
12	G	Residual ground overcurrent element trips for the fault
13	N	Neutral ground overcurrent element trips for the fault
14	RS	Reclosing relay is in the Reset State (follows Relay Word bit 79RS)
15	CY	Reclosing relay is in the Cycle State (follows Relay Word bit 79CY)
16	LO	Reclosing relay is in the Lockout State (follows Relay Word bit 79LO)

Target LEDs numbered 2 through 13 in Table 5.1 are updated and then latched for every new assertion (rising edge) of the TRIP Relay Word bit. The TRIP Relay Word bit is the output of the trip logic (see Figure 5.1).

Further target LED information follows. Refer also to Figure 2.2 through Figure 2.5 in *Section 2: Installation* for the placement of the target LEDs on the front panel.

Additional Target LED Information

TRIP Target LED

The TRIP target LED illuminates at the rising edge of trip (the new assertion of the TRIP Relay Word bit).

The TRIP target LED is especially helpful in providing front-panel indication for tripping that does not involve overcurrent or frequency elements. If the trip is not an overcurrent or frequency element generated trip, none of the target LEDs numbered 3 through 13 in Table 5.1 illuminate, but the TRIP target LED still illuminates. Thus, tripping via the front-panel local control (local bits), serial port (remote bits or OPEN command), or voltage elements is indicated only by the illumination of the TRIP target LED.

INST Target LED

The INST target LED illuminates at the rising edge of trip if SELOGIC control equation setting FAULT has been asserted for less than 3 cycles. FAULT is usually set with time-overcurrent element pickups (e.g., FAULT = 51P + 51G) to detect fault inception. If tripping occurs within 3 cycles of fault inception, the INST target illuminates.

SELOGIC control equation setting FAULT also controls other relay functions. See *SELOGIC Control Equation Setting FAULT* in this section.

COMM Target LED

The COMM target LED illuminates at the rising edge of trip if the trip is the result of SELOGIC control equation setting TRCOMM and associated communications-assisted trip logic, Relay Word bit ECTT, or SELOGIC control equation setting DTT (see Figure 5.1, top half of figure).

Another Application for the COMM Target LED

If none of the traditional communications-assisted trip logic is used (i.e., SELOGIC control equation setting TRCOMM is not used; see Figure 5.4 and accompanying text), consideration can be given to using the COMM target LED to **indicate tripping via remote communications channels** (e.g., via serial port commands or SCADA asserting optoisolated inputs). Use SELOGIC control equation setting DTT (Direct Transfer Trip) to accomplish this (see Figure 5.1).

For example, if the OPEN command or remote bit RB1 (see CON command in *Section 10: Serial Port Communications and Commands*) are used to trip via the serial port and they should illuminate the COMM target LED, set them in SELOGIC control equation setting DTT:

$$DTT = \dots + OC + RB1$$

Additionally, if SCADA asserts optoisolated input IN104 to trip and it should illuminate the COMM target LED, set it in SELOGIC control equation setting DTT also:

$$DTT = \dots + IN104 + \dots$$

Relay Word bits set in SELOGIC control equation setting DTT do not have to be set in SELOGIC control equation setting TR—both settings directly assert the TRIP Relay Word bit. The only

difference between settings DTT and TR is that setting DTT causes the COMM target LED to illuminate.

Many other variations of the above DTT settings examples are possible.

SOTF Target LED

The SOTF target LED illuminates at the rising edge of the TRIP Relay Word bit if the trip is the result of the SELOGIC control equation setting TRSOTF and associated switch-onto-fault trip logic (see Figure 5.3).

50 Target LED

The 50 target LED illuminates at the rising edge of trip if an instantaneous or definite-time overcurrent element causes the trip.

51 Target LED

The 51 target LED illuminates at the rising edge of trip if a time-overcurrent element (51PT, 51AT, 51BT, 51CT, 51NT, 51GT, or 51QT) causes the trip.

81 Target LED

The 81 target LED illuminates at the rising edge of trip if a frequency element (81D1T through 81D6T) causes the trip.

FAULT TYPE Target LEDs

A, B, and C Target LEDs

“A” (Phase A) target LED is illuminated at the rising edge of trip if an overcurrent element causes the trip and Phase A is involved in the fault [likewise for “B” (Phase B) and “C” (Phase C) target LEDs]. SELOGIC control equation FAULT has to be picked up for three-phase fault indication.

LEDs A, B, and C always latch in on trip, if the corresponding phase is involved with the fault. LEDs A, B, and C reset (unlatch) similar to the other target LEDs. SELOGIC control equation FAULT has to be picked up for three-phase fault indication (FAULT = 51P + 51G in the factory default settings—set with the pickup indicators of the time-overcurrent elements). Additionally, the fault must be present for at least one cycle after the relay trips for reliable targeting. This is most noticeable in relay testing when breaker opening times are not included in the test setup.

SELOGIC control equation setting FAULT also controls other relay functions. See *SELOGIC Control Equation Setting FAULT* in this section.

G Target LED

G target LED is illuminated at the rising edge of trip if a residual ground overcurrent element causes the trip or was picked up and timing to trip.

N Target LED

N target LED is illuminated at the rising edge of trip if a neutral ground overcurrent element causes the trip.

79 Target LEDs

If the reclosing relay is turned off (enable setting E79 = N or 79OI1 = 0), all the Device 79 (reclosing relay) target LEDs are extinguished.

Target Reset/Lamp Test Front-Panel Pushbutton

When the Target Reset/Lamp Test front-panel pushbutton is pressed:

- All front-panel LEDs illuminate for one (1) second.
- All latched target LEDs (target LEDs numbered 2 through 13 in Table 5.1) are extinguished (unlatched), unless a trip condition is present in which case the latched target LEDs reappear in their previous state.

Other Applications for the Target Reset Function

Refer to the bottom of Figure 5.1. The combination of the TARGET RESET Pushbutton and the TAR R (Target Reset) serial port command is available as Relay Word bit TRGTR. Relay Word bit TRGTR pulses to logical 1 for one processing interval when either the TARGET RESET Pushbutton is pushed or the TAR R (Target Reset) serial port command is executed.

Relay Word bit TRGTR can be used to unlatch logic. For example, refer to the breaker failure logic in Figure 7.27 in *Section 7: Inputs, Outputs, Timers, and Other Control Logic*. If a breaker failure trip occurs (SV7T asserts), the occurrence can be displayed on the front panel with seal-in logic and a rotating default display (see *Rotating Default Display* in *Sections 7 and 11*, also):

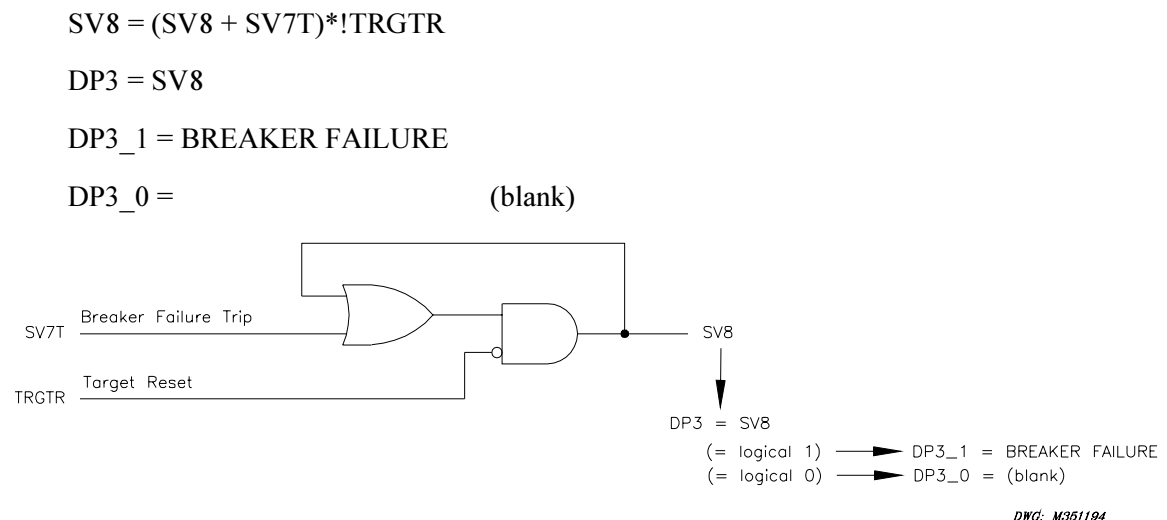


Figure 5.17: Seal-in of Breaker Failure Occurrence for Message Display

If a breaker failure trip has occurred, the momentary assertion of SV7T (breaker failure trip) will cause SV8 in Figure 5.17 to seal-in. Asserted SV8 in turn asserts DP3, causing the message:

BREAKER FAILURE

to display in the rotating default display.

This message can be removed from the display rotation by pushing the TARGET RESET Pushbutton (Relay Word bit TRGTR pulses to logical 1, unlatching SV8 and in turn deasserting DP3). Thus, front-panel rotating default displays can be easily reset along with the front-panel targets by pushing the TARGET RESET Pushbutton.

SELogic Control Equation Setting FAULT

SELOGIC control equation setting FAULT has control over or is used in the following:

- Front-panel target LEDs INST, A, B, and C. See earlier subsection *Front-Panel Target LEDs*.
- Demand Metering – FAULT is used to suspend demand metering updating and peak recording. See subsection *Demand Metering* in *Section 8: Breaker Monitor, Metering, and Load Profile Functions*.
- Maximum/Minimum Metering – FAULT is used to block Maximum/Minimum metering updating. See subsection *Maximum/Minimum Metering* in *Section 8: Breaker Monitor, Metering, and Load Profile Functions*.
- Voltage Sag, Swell Interruption elements – FAULT is used to suspend the calculation of Vbase. See subsection *Voltage Sag, Swell, and Interruption Elements* in *Section 3: Overcurrent, Voltage Synchronism Check, Frequency, and Power Elements*.

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SECTION 6: CLOSE AND RECLOSE LOGIC

This section is made up of three subsections:

Close Logic

This subsection describes the final logic that controls the close output contact (e.g., OUT102 = CLOSE). This output contact closes the circuit breaker for automatic reclosures and other close conditions (e.g., manual close initiation via serial port or optoisolated inputs).

If automatic reclosing is not needed, but the SEL-351 Relay is to close the circuit breaker for other close conditions (e.g., manual close initiation via serial port or optoisolated inputs), then this subsection is the only subsection that needs to be read in this section (particularly the description of SELOGIC[®] control equation setting CL).

Reclose Supervision Logic

This subsection describes the logic that supervises automatic reclosing when an open interval time times out—a final condition check right before the close logic asserts the close output contact.

Reclose Logic

This subsection describes all the reclosing relay settings and logic needed for automatic reclosing (besides the final close logic and reclose supervision logic described in the previous subsections).

The reclose enable setting, E79, has setting choices N, 1, 2, 3, and 4. Setting E79 = N defeats the reclosing relay. Setting choices 1 through 4 are the number of desired automatic reclosures.

Note: Setting E79 = N defeats the reclosing relay, but does not defeat the ability of the close logic described in the first subsection (Figure 6.1) to close the circuit breaker for other close conditions via SELOGIC control equation setting CL (e.g., manual close initiation via serial port or optoisolated inputs).

CLOSE LOGIC

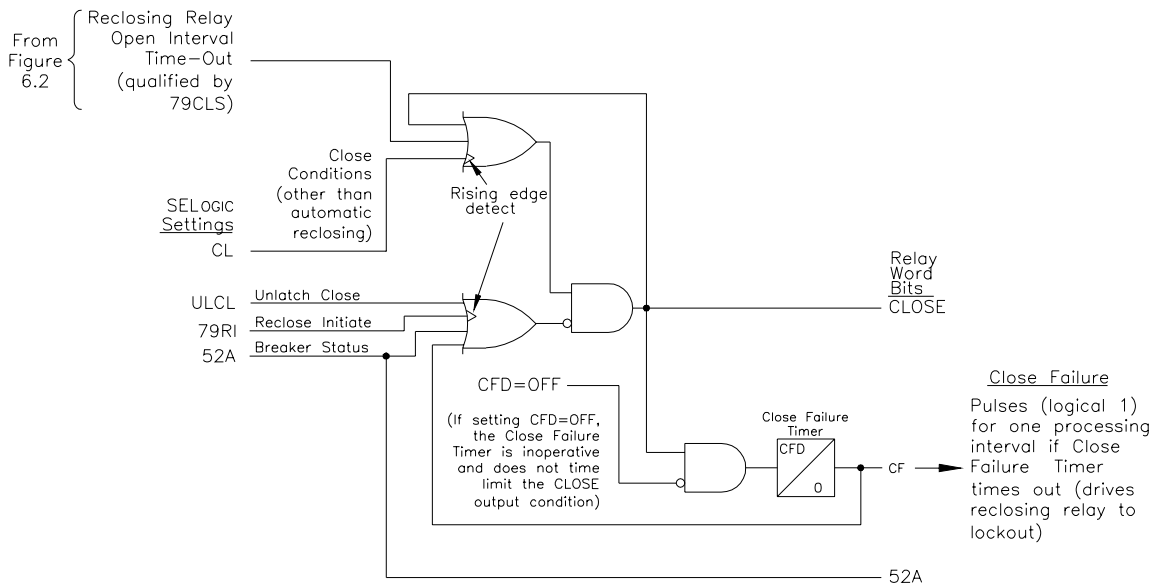
The close logic in Figure 6.1 provides flexible circuit breaker closing/automatic reclosing with SELOGIC control equation settings:

52A	(breaker status)
CL	(close conditions, other than automatic reclosing)
ULCL	(unlatch close conditions, other than circuit breaker status, close failure, or reclose initiation)

and setting:

CFD	(Close Failure Time)
-----	----------------------

See the settings sheet in *Section 9: Setting the Relay* for setting ranges.



DWG: M3511Bb

Figure 6.1: Close Logic

Set Close

If all the following are true:

- The unlatch close condition is not asserted (ULCL = logical 0).
- The circuit breaker is open (52A = logical 0).
- The reclose initiation condition (79RI) is not making a rising edge (logical 0 to logical 1) transition.
- And a close failure condition does not exist (Relay Word bit CF = 0).

Then the CLOSURE Relay Word bit can be asserted to logical 1 if either of the following occurs:

- A reclosing relay open interval times out (qualified by SELOGIC control equation setting 79CLS—see Figure 6.2).
- Or SELOGIC control equation setting CL goes from logical 0 to logical 1 (rising edge transition).

Note: CLOSURE Command no longer embedded in Close Logic

In previous firmware versions of the SEL-351 Relay, the CLOSURE command was embedded in the close logic in Figure 6.1. The CLOSURE command was routed directly into the same OR logic gate as Reclosing Relay Open Interval Time-out and SELOGIC control equation setting CL.

The CLOSURE command is no longer directly embedded in the close logic. This change was made so that users can supervise the CLOSURE command if desired via setting CL.

The CLOSURE command is included in the close logic in the factory settings:

$$CL = \dots + CC$$

Relay Word bit CC asserts for execution of the CLOSE Command. See *CLO Command (Close Breaker)* in *Section 10: Serial Port Communications and Commands* for more information on the CLOSE Command. More discussion follows later on the factory settings for setting CL.

If previous firmware versions of the SEL-351 Relay with the CLOSE command imbedded in the close logic also have setting CL set as:

$$CL = \dots + CC$$

this would appear as a redundancy in inputting the CLOSE command into the close logic. But, this is no problem—just a redundancy in logic. Thus, SEL-351 Relays with various firmware versions can be set the same with respect to setting $CL = \dots + CC$.

If a user wants to supervise the CLOSE command with optoisolated input IN106, the following setting is made:

$$CL = \dots + CC * IN106$$

With this setting, the CLOSE command can provide a close only if optoisolated input IN106 is asserted. This is just one CLOSE command supervision example—many variations are possible.

Unlatch Close

If the CLOSE Relay Word bit is asserted at logical 1, it stays asserted at logical 1 until one of the following occurs:

- The unlatch close condition asserts (ULCL = logical 1).
- The circuit breaker closes (52A = logical 1).
- The reclose initiation condition (79RI) makes a rising edge (logical 0 to logical 1) transition.
- Or the Close Failure Timer times out (Relay Word bit CF = 1).

The Close Failure Timer is inoperative if setting CFD = OFF.

Factory Settings Example

The factory settings for the close logic SELOGIC control equation settings are:

$$\begin{aligned} 52A &= IN101 \\ CL &= LB4 + CC \\ ULCL &= TRIP \end{aligned}$$

The factory setting for the Close Failure Timer setting is:

$$CFD = 60.00 \text{ cycles}$$

See the settings sheets at the end of *Section 9: Setting the Relay* for setting ranges.

Set Close

If the Reclosing Relay Open Interval Time-Out logic input at the top of Figure 6.1 is ignored (reclosing is discussed in detail in a following subsection), then SELOGIC control equation setting CL is the only logic input that can set the CLOSE Relay Word bit.

In SELOGIC control equation setting $CL = LB4 + CC$

- Local bit LB4 operates as a manual close switch via the front panel. See *Local Control Switches* in *Section 7: Inputs, Outputs, Timers, and Other Control Logic* and *Local Control* in *Section 11: Front-Panel Interface* for more information on local control.
- Relay Word bit CC asserts for execution of the CLOSE Command. See *CLO Command (Close Breaker)* in *Section 10: Serial Port Communications and Commands* for more information on the CLOSE Command.

Unlatch Close

SELOGIC control equation setting ULCL is set with the TRIP Relay Word bit. This prevents the CLOSE Relay Word bit from being asserted any time the TRIP Relay Word bit is asserted (TRIP takes priority). See *Trip Logic* in *Section 5: Trip and Target Logic*.

SELOGIC control equation setting 52A is set with optoisolated input IN101. Input IN101 is connected to a 52a circuit breaker auxiliary contact. When a closed circuit breaker condition is detected, the CLOSE Relay Word bit is deasserted to logical 0. Setting 52A can handle a 52a or 52b circuit breaker auxiliary contact connected to an optoisolated input (see *Optoisolated Inputs* in *Section 7: Inputs, Outputs, Timers, and Other Control Logic* for more 52A setting examples).

With setting $CFD = 60.00$ cycles, once the CLOSE Relay Word bit asserts, it remains asserted at logical 1 no longer than a maximum of 60 cycles. If the Close Failure Timer times out, Relay Word bit CF asserts to logical 1, forcing the CLOSE Relay Word bit to logical 0.

Defeat the Close Logic

If SELOGIC control equation circuit breaker auxiliary setting 52A is set with numeral 0 ($52A = 0$), then the close logic is inoperable. Also, the reclosing relay is defeated (see *Reclosing Relay* later in this section).

Circuit Breaker Status

Refer to the bottom of Figure 6.1. Note that SELOGIC control equation setting 52A (circuit breaker status) is available as Relay Word bit 52A. This makes for convenience in setting other SELOGIC control equations. For example, if the following setting is made:

$52A = IN101$ (52a auxiliary contact wired to input IN101)

or

$52A = !IN101$ (52b auxiliary contact wired to input IN101)

then if breaker status is used in other SELOGIC control equations, it can be entered as 52A—the user doesn't have to enter IN101 (for a 52a) or !IN101 (for a 52b). For example, refer to

Rotating Default Display in ***Section 7: Inputs, Outputs, Timers, and Other Control Logic***. In the factory settings, circuit breaker status indication is controlled by display point setting DP2:

DP2 = IN101

This can be entered instead as:

DP2 = 52A

(presuming SELOGIC control equation setting 52A = IN101 is made).

Program an Output Contact for Closing

In the factory settings, the resultant of the close logic in Figure 6.1 is routed to output contact OUT102 with the following SELOGIC control equation:

OUT102 = CLOSE

See ***Output Contacts*** in ***Section 7: Inputs, Outputs, Timers, and Other Control Logic*** for more information on programming output contacts.

RECLOSE SUPERVISION LOGIC

Note that one of the inputs into the close logic in Figure 6.1 is:

Reclosing Relay Open Interval Time-Out (qualified by 79CLS)

This input into the close logic in Figure 6.1 is the indication that a reclosing relay open interval has timed out (see Figure 6.6), a qualifying condition (SELOGIC control equation setting 79CLS) has been met, and thus automatic reclosing of the circuit breaker should proceed by asserting the CLOSE Relay Word bit to logical 1. This input into the close logic in Figure 6.1 is an output of the reclose supervision logic in the following Figure 6.2.

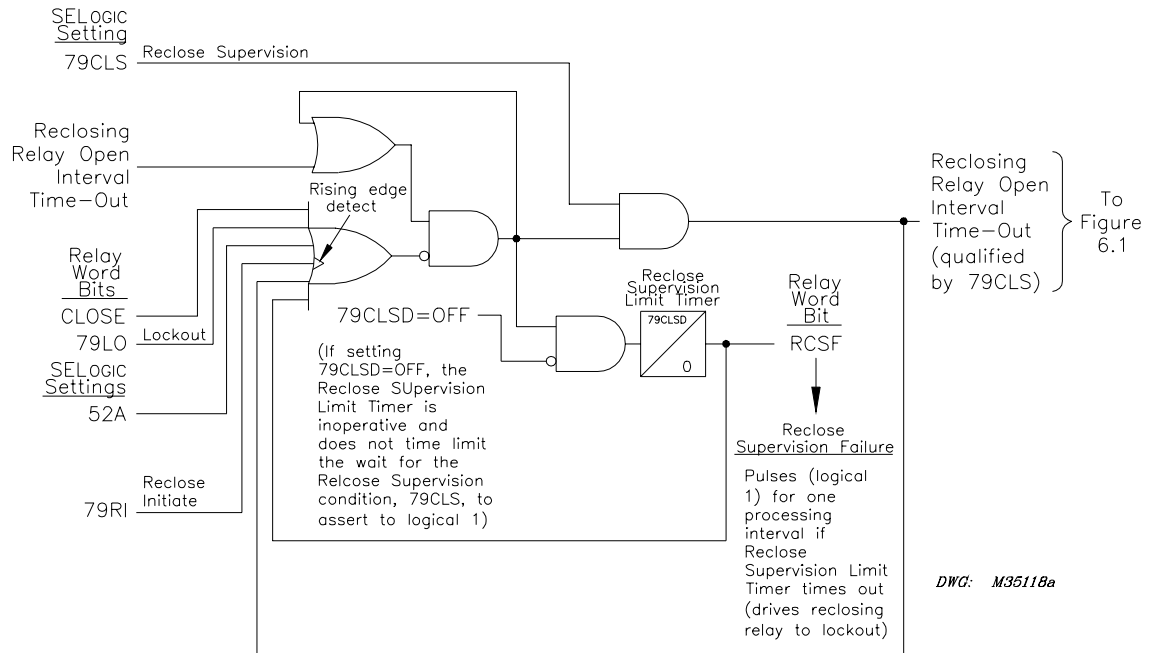
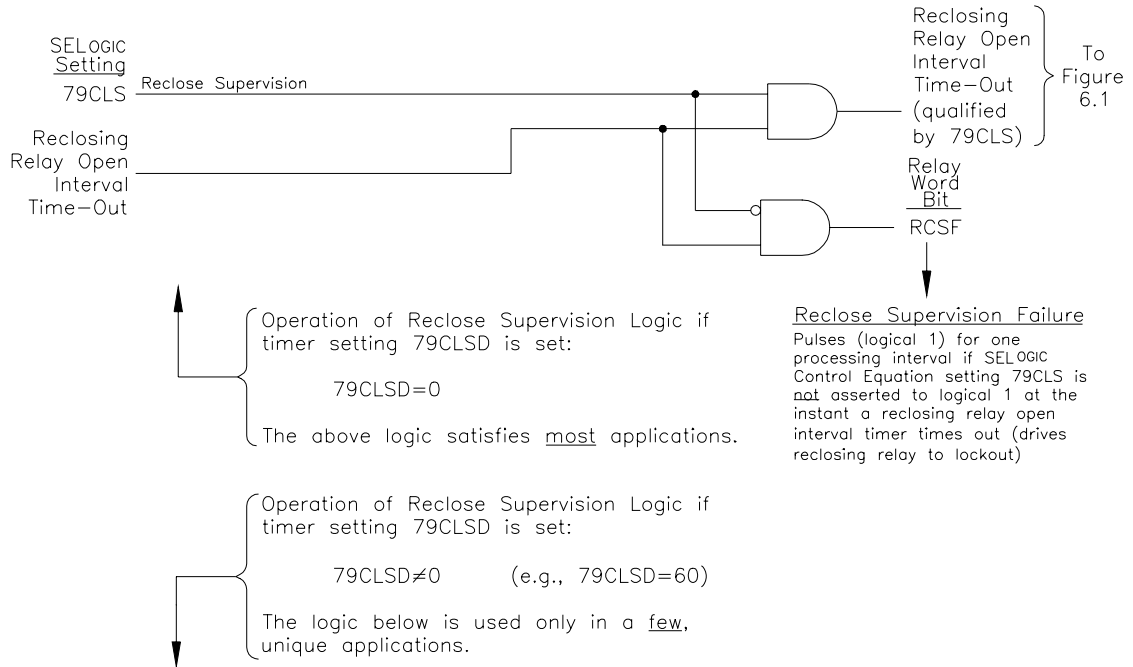


Figure 6.2: Reclose Supervision Logic (Following Open Interval Time-Out)

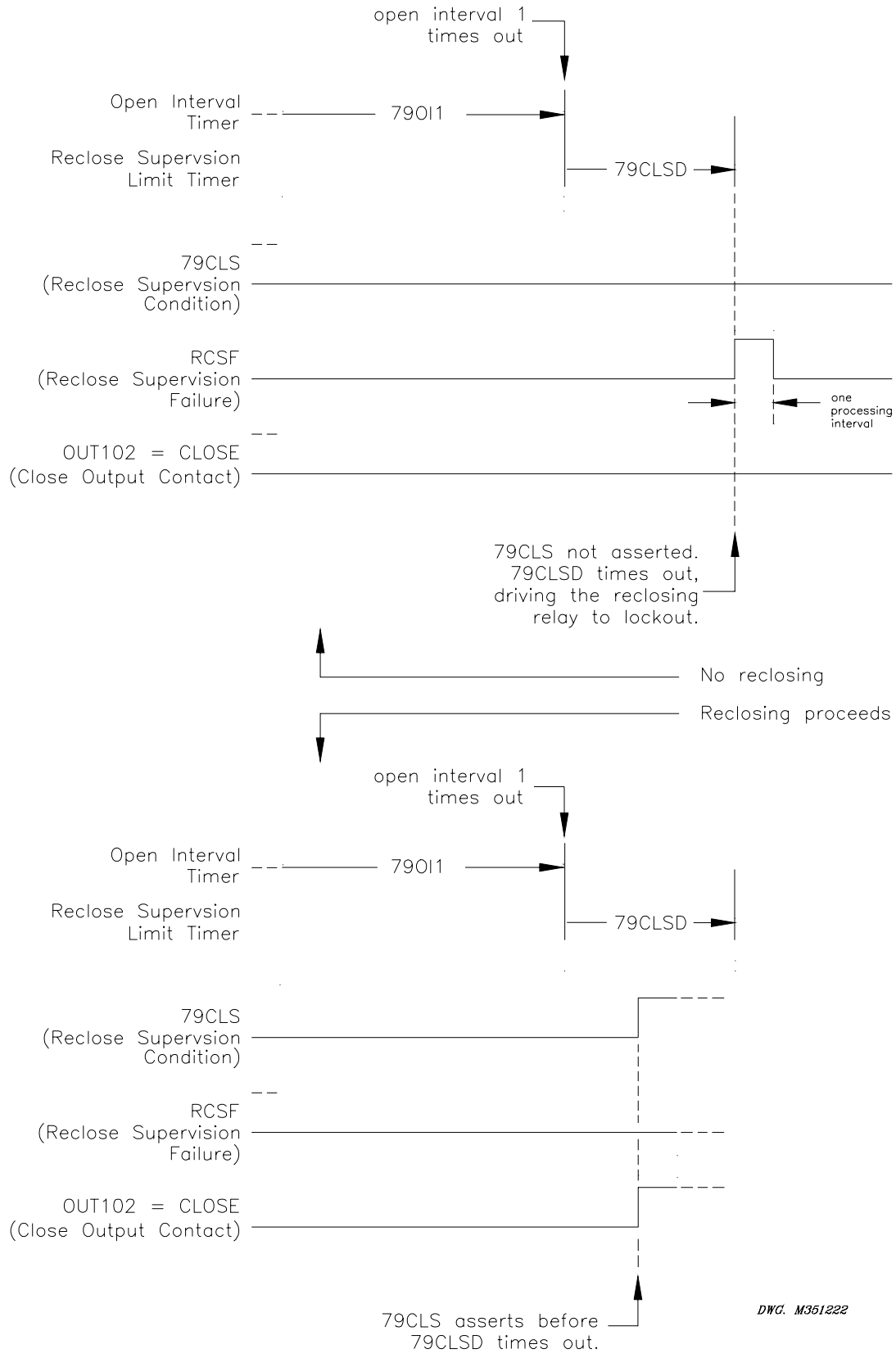


Figure 6.3: Reclose Supervision Limit Timer Operation (Refer to Bottom of Figure 6.2)

Settings and General Operation

Figure 6.2 contains the following SELOGIC control equation setting:

79CLS (reclose supervision conditions—checked after reclosing relay open interval time-out)

and setting:

79CLSD (Reclose Supervision Limit Time)

See the settings sheets at the end of *Section 9: Setting the Relay* for setting ranges.

For Most Applications (Top of Figure 6.2)

For most applications, the Reclose Supervision Limit Time setting should be set to zero cycles:

$79CLSD = 0.00$

With this setting, the logic in the top of Figure 6.2 is operative. When an open interval times out, the SELOGIC control equation reclose supervision setting 79CLS is checked just once.

If 79CLS is asserted to logical 1 at the instant of an open interval time-out, then the now-qualified open interval time-out will propagate onto the final close logic in Figure 6.1 to automatically reclose the circuit breaker.

If 79CLS is deasserted to logical 0 at the instant of an open interval time-out, the following occurs:

- No automatic reclosing takes place.
- Relay Word bit RCSF (Reclose Supervision Failure indication) asserts to logical 1 for one processing interval.
- The reclosing relay is driven to the Lockout State.

See *Factory Settings Example* and *Additional Settings Example 1* that follow in this subsection.

For A Few, Unique Applications (Bottom of Figure 6.2 and Figure 6.3)

For a few unique applications, the Reclose Supervision Limit Time setting is not set equal to zero cycles:

e.g., $79CLSD = 60.00$

With this setting, the logic in the bottom of Figure 6.2 is operative. When an open interval times out, the SELOGIC control equation reclose supervision setting 79CLS is then checked for a time window equal to setting 79CLSD.

If 79CLS asserts to logical 1 at any time during this 79CLSD time window, then the now-qualified open interval time-out will propagate onto the final close logic in Figure 6.1 to automatically reclose the circuit breaker.

If 79CLS remains deasserted to logical 0 during this entire 79CLSD time window, when the time window times out, the following occurs:

- No automatic reclosing takes place.
- Relay Word bit RCSF (Reclose Supervision Failure indication) asserts to logical 1 for one processing interval.
- The reclosing relay is driven to the Lockout State.

The logic in the bottom of Figure 6.2 is explained in more detail in the following text.

Set Reclose Supervision Logic (Bottom of Figure 6.2)

Refer to the bottom of Figure 6.2. If all the following are true:

- The close logic output CLOSE (also see Figure 6.1) is not asserted (Relay Word bit CLOSE = logical 0).
- The reclosing relay is not in the Lockout State (Relay Word bit 79LO = logical 0).
- The circuit breaker is open (52A = logical 0).
- The reclose initiation condition (79RI) is not making a rising edge (logical 0 to logical 1) transition.
- The Reclose Supervision Limit Timer is not timed out (Relay Word bit RCSF = logical 0).

then a reclosing relay open interval time-out seals in Figure 6.2. Then, when 79CLS asserts to logical 1, the sealed-in reclosing relay open interval time-out condition will propagate through Figure 6.2 and on to the close logic in Figure 6.1.

Unlatch Reclose Supervision Logic (Bottom of Figure 6.2)

Refer to the bottom of Figure 6.2. If the reclosing relay open interval time-out condition is sealed-in, it stays sealed-in until one of the following occurs:

- The close logic output CLOSE (also see Figure 6.1) asserts (Relay Word bit CLOSE = logical 1).
- The reclosing relay goes to the Lockout State (Relay Word bit 79LO = logical 1).
- The circuit breaker closes (52A = logical 1).
- The reclose initiation condition (79RI) makes a rising edge (logical 0 to logical 1) transition.
- SELOGIC control equation setting 79CLS asserts (79CLS = logical 1).
- Or the Reclose Supervision Limit Timer times out (Relay Word bit RCSF = logical 1 for one processing interval).

The Reclose Supervision Limit Timer is inoperative if setting 79CLSD = OFF. With 79CLSD = OFF, reclose supervision condition 79CLS is not time limited. When an open interval times out, reclose supervision condition 79CLS is checked indefinitely until one of the other above unlatch conditions comes true.

The unlatching of the sealed-in reclosing relay open interval time-out condition by the assertion of SELOGIC control equation setting 79CLS indicates successful propagation of a reclosing relay open interval time-out condition on to the close logic in Figure 6.1.

See *Additional Settings Example 2* that follows in this subsection.

Factory Settings Example

Refer to the top of Figure 6.2.

The factory setting for the SELOGIC control equation reclose supervision setting is:

$$79CLS = 1 \quad (\text{numeral } 1)$$

The factory setting for the Reclose Supervision Limit Timer setting is:

$$79CLSD = 0.00 \text{ cycles}$$

Any time a reclosing relay open interval times out, it propagates immediately through Figure 6.2 and then on to Figure 6.1, because SELOGIC control equation setting 79CLS is always asserted to logical 1. Effectively, there is no special reclose supervision.

Additional Settings Example 1

Refer to the top of Figure 6.2 and Figure 6.4.

SEL-351 Relays are installed at both ends of a transmission line in a high-speed reclose scheme. After both circuit breakers open for a transmission line fault, the SEL-351(1) Relay recloses circuit breaker 52/1 first, followed by the SEL-351(2) Relay reclosing circuit breaker 52/2, after a synchronism check across circuit breaker 52/2.

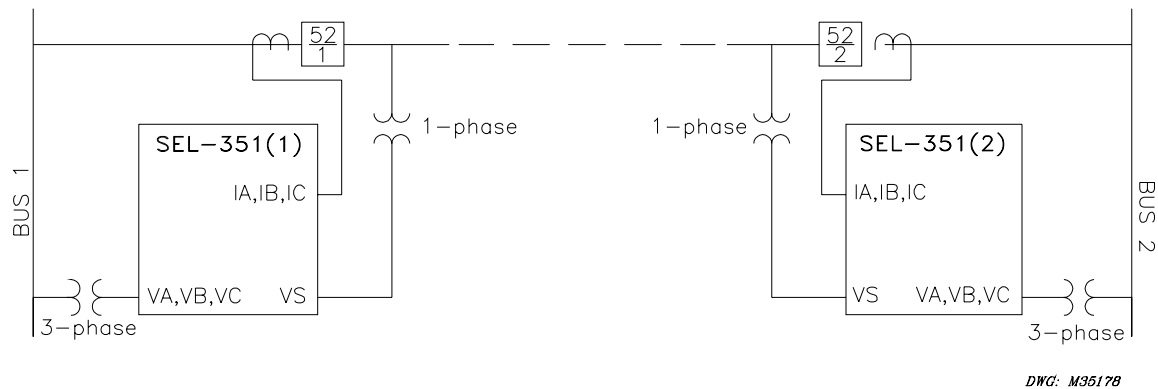


Figure 6.4: SEL-351 Relays Installed at Both Ends of a Transmission Line in a High-Speed Reclose Scheme

SEL-351(1) Relay

Before allowing circuit breaker 52/1 to be reclosed after an open interval time-out, the SEL-351(1) Relay checks that Bus 1 voltage is hot and the transmission line voltage is dead. This requires reclose supervision settings:

$$\begin{aligned} 79CLSD &= 0.00 \text{ cycles} && \text{(only one check)} \\ 79CLS &= 3P59 * 27S \end{aligned}$$

where:

$$\begin{aligned} 3P59 &= \text{all three Bus 1 phase voltages (VA, VB, and VC) are hot} \\ 27S &= \text{monitored single-phase transmission line voltage (channel VS) is dead} \end{aligned}$$

SEL-351(2) Relay

The SEL-351(2) Relay checks that Bus 2 voltage is hot, the transmission line voltage is hot, and in synchronism after the reclosing relay open interval times out, before allowing circuit breaker 52/2 to be reclosed. This requires reclose supervision settings:

$$\begin{aligned} 79CLSD &= 0.00 \text{ cycles} && \text{(only one check)} \\ 79CLS &= 25A1 \end{aligned}$$

where:

$$25A1 = \text{selected Bus 2 phase voltage (VA, VB, or VC) is in synchronism with monitored single-phase transmission line voltage (channel VS) and both are hot}$$

Other Setting Considerations for SEL-351(1) and SEL-351(2) Relays

Refer to *Skip Shot and Stall Open Interval Timing Settings (79SKP and 79STL, Respectively)* in the following *Reclosing Relay* subsection.

SELOGIC control equation setting 79STL stalls open interval timing if it asserts to logical 1. If setting 79STL is deasserted to logical 0, open interval timing can continue.

The SEL-351(1) Relay has no intentional open interval timing stall condition (circuit breaker 52/1 closes first after a transmission line fault):

$$79STL = 0 \quad \text{(numeral 0)}$$

The SEL-351(2) Relay starts open interval timing after circuit breaker 52/1 at the remote end has reenergized the line. The SEL-351(2) Relay has to see Bus 2 hot, transmission line hot, and in synchronism across open circuit breaker 52/2 for open interval timing to begin. Thus, SEL-351(2) Relay open interval timing is stalled when the transmission line voltage and Bus 2 voltage are not in synchronism across open circuit breaker 52/2:

$$79STL = !25A1 \quad [=NOT(25A1)]$$

Note: A transient synchronism check condition across open circuit breaker 52/2 could possibly occur if circuit breaker 52/1 recloses into a fault on one phase of the transmission line. The other two unfaulted phases would be briefly energized until circuit breaker 52/1 is tripped again. If channel VS of the SEL-351(2) Relay is connected to one of these briefly

energized phases, synchronism check element 25A1 could momentarily assert to logical 1.

So that this possible momentary assertion of synchronism check element 25A1 does not cause any inadvertent reclose of circuit breaker 52/2, make sure the open interval timers in the SEL-351(2) Relay are set with some appreciable time greater than the momentary energization time of the faulted transmission line. Or, run the synchronism check element 25A1 through a programmable timer before using it in the preceding 79CLS and 79STL settings for the SEL-351(2) Relay (see Figure 7.25 and Figure 7.26). Note the built-in 3-cycle qualification of the synchronism check voltages shown in Figure 3.24.

Additional Settings Example 2

Refer to subsection *Synchronism Check Elements* in *Section 3: Overcurrent, Voltage, Synchronism Check, Frequency, and Power Elements*. Also refer to Figures 6.3 and 6.4.

If the synchronizing voltages across open circuit breaker 52/2 are “slipping” with respect to one another, the Reclose Supervision Limit Timer setting 79CLSD should be set greater than zero so there is time for the slipping voltages to come into synchronism. For example:

$$\begin{aligned}79CLSD &= 60.00 \text{ cycles} \\79CLS &= 25A1\end{aligned}$$

The status of synchronism check element 25A1 is checked continuously during the 60-cycle window. If the slipping voltages come into synchronism while timer 79CLSD is timing, synchronism check element 25A1 asserts to logical 1 and reclosing proceeds.

In the above referenced subsection *Synchronism Check Elements*, note item 3 under *Synchronism Check Element Outputs*, Voltages V_p and V_s are “Slipping.” Item 3 describes a last attempt for a synchronism check reclose before timer 79CLSD times out (or setting 79CLSD = 0.00 and only one check is made).

RECLOSING RELAY

Note that input:

Reclosing Relay Open Interval Time-Out

in Figure 6.2 is the logic input that is qualified by SELOGIC control equation setting 79CLS, and then propagated on to the close logic in Figure 6.1 to automatically reclose a circuit breaker. The explanation that follows in this reclosing relay subsection describes all the reclosing relay settings and logic that eventually result in this open interval time-out logic input into Figure 6.2. Other aspects of the reclosing relay are also explained. Up to four (4) automatic reclosures (shots) are available.

The reclose enable setting, E79, has setting choices N, 1, 2, 3, and 4. Setting E79 = N defeats the reclosing relay. Setting choices 1 through 4 are the number of desired automatic reclosures (see *Open Interval Timers* that follows in this subsection).

Reclosing Relay States and General Operation

Figure 6.5 explains in general the different states of the reclosing relay and its operation.

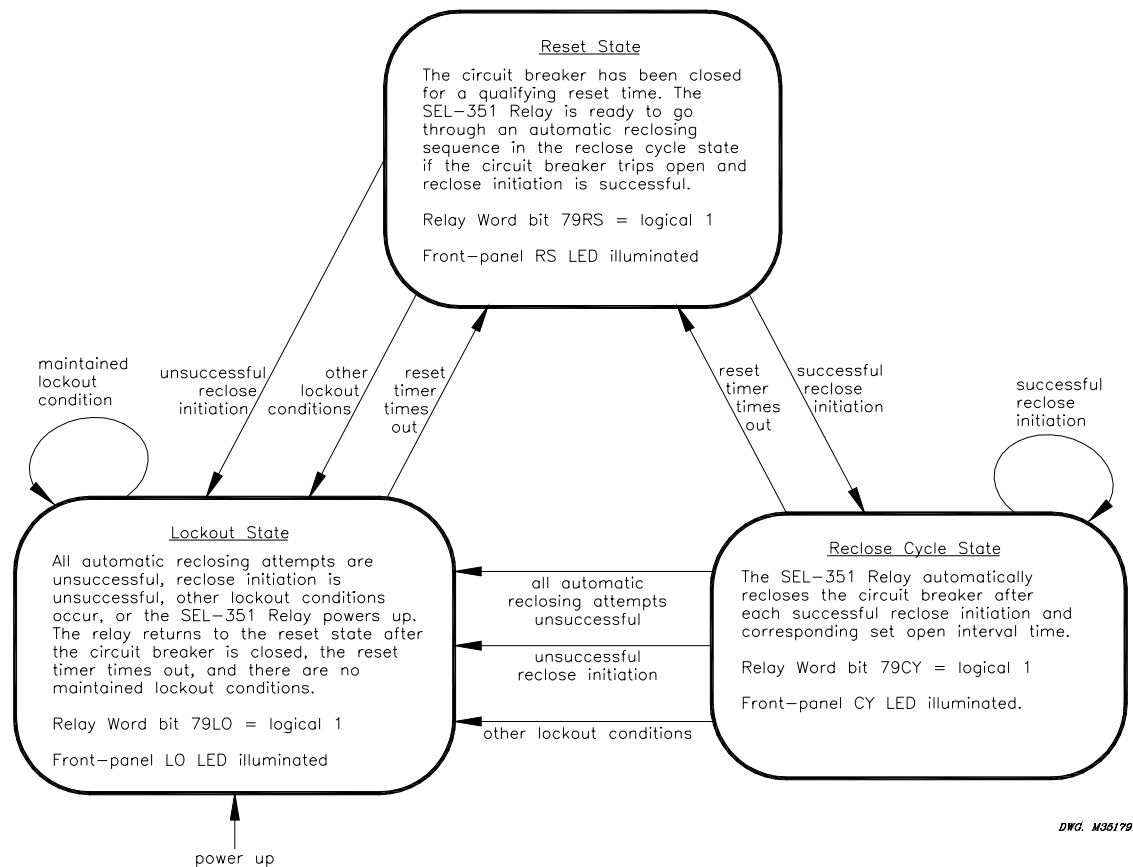


Figure 6.5: Reclosing Relay States and General Operation

Table 6.1: Relay Word Bit and Front-Panel Correspondence to Reclosing Relay States

Reclosing Relay State	Corresponding Relay Word Bit	Corresponding Front-Panel LED
Reset	79RS	RS
Reclose Cycle	79CY	CY
Lockout	79LO	LO

The reclosing relay is in one (and only one) of these states (listed in Table 6.1) at any time. When in a given state, the corresponding Relay Word bit asserts to logical 1, and the LED illuminates. Automatic reclosing only takes place when the relay is in the Reclose Cycle State.

Lockout State

The reclosing relay goes to the Lockout State if any one of the following occurs:

- The shot counter is equal to or greater than the last shot at time of reclose initiation (e.g., all automatic reclosing attempts are unsuccessful—see Figure 6.6).
- Reclose initiation is unsuccessful because of SELOGIC control equation setting 79RIS [see *Reclose Initiate and Reclose Initiate Supervision Settings (79RI and 79RIS, Respectively)* later in this subsection].
- The circuit breaker opens without reclose initiation (e.g., an external trip).
- The shot counter is equal to or greater than last shot, and the circuit breaker is open [e.g., the shot counter is driven to last shot with SELOGIC control equation setting 79DLS while open interval timing is in progress. See *Drive-to-Lockout and Drive-to-Last Shot Settings (79DTL and 79DLS, respectively)* later in this subsection].
- The close failure timer (setting CFD) times out (see Figure 6.1).
- SELOGIC control equation setting 79DTL = logical 1 [see *Drive-to-Lockout and Drive-to-Last Shot Settings (79DTL and 79DLS, respectively)* later in this subsection].
- The Reclose Supervision Limit Timer (setting 79CLSD) times out (see Figure 6.2 and top of Figure 6.3).

Note: OPEN Command no longer embedded in Drive-to-Lockout Logic

In previous firmware versions of the SEL-351 Relay (except the original release), the OPEN command was embedded to drive the reclosing relay to lockout (see *Appendix A*). The OPEN command is no longer directly embedded in the reclosing relay logic. It is also no longer directly embedded in the trip logic (see the Note following Figure 5.2).

This change was made so that users can supervise the OPEN command if desired (see the example in the Note following Figure 5.2).

The OPEN command is now included in the reclosing relay logic via the factory SELOGIC control equation settings:

$$79DTL = \dots + OC \quad (\text{drive-to-lockout})$$

Relay Word bit OC asserts for execution of the OPEN Command. See OPE Command (Open Breaker) in *Section 10: Serial Port Communications and Commands* for more information on the OPEN Command. Also, see *Drive-to-Lockout and Drive-to-Last Shot Settings (79DTL and 79DLS, respectively)* later in this subsection.

If the OPEN command is set to trip ($TR = \dots + OC$; see Note following Figure 5.2), then the following reclosing relay SELOGIC control equation settings should also be made (presuming that an OPEN command trip should not initiate reclosing):

$$\begin{aligned} 79RI &= TRIP && (\text{reclose initiate}) \\ 79DTL &= \dots + OC && (\text{drive-to-lockout}) \end{aligned}$$

This is how the SEL-351 Relay is set at the factory.

These reclosing relay SELOGIC control equation factory settings can be used in any firmware version. It is logically redundant in firmware versions with the OPEN command imbedded to drive the reclosing relay to lockout, but this is no problem.

Reclosing Relay States and Settings/Setting Group Changes

If individual settings are changed for the active setting group or the active setting group is changed, all of the following occur:

- The reclosing relay remains in the state it was in before the settings change.
- The shot counter is driven to last shot (last shot corresponding to the new settings; see discussion on last shot that follows).
- The reset timer is loaded with reset time setting 79RSLD (see discussion on reset timing later in this section).

If the relay happened to be in the Reclose Cycle State and was timing on an open interval before the settings change, the relay would be in the Reclose Cycle State after the settings change, but the relay would immediately go to the Lockout State. This is because the breaker is open, and the relay is at last shot after the settings change, and thus no more automatic reclosures are available.

If the circuit breaker remains closed through the settings change, the reset timer times out on reset time setting 79RSLD after the settings change and goes to the Reset State (if it is not already in the Reset State), and the shot counter returns to shot = 0. If the relay happens to trip during this reset timing, the relay will immediately go to the Lockout State, because shot = last shot.

Defeat the Reclosing Relay

If any one of the following reclosing relay settings are made:

- Reclose enable setting E79 = N.
- Open Interval 1 time setting 79OI1 = 0.00.

then the reclosing relay is defeated, and no automatic reclosing can occur. These settings are explained later in this section. See also the settings sheets at the end of *Section 9: Setting the Relay*.

If the reclosing relay is defeated, the following also occur:

- All three reclosing relay state Relay Word bits (79RS, 79CY, and 79LO) are forced to logical 0 (see Table 6.1).
- All shot counter Relay Word bits (SH0, SH1, SH2, SH3, and SH4) are forced to logical 0 (the shot counter is explained later in this section).
- The front-panel LEDs RS, CY, and LO are all extinguished—a ready indication that the recloser is defeated.

Close Logic Can Still Operate When the Reclosing Relay is Defeated

If the reclosing relay is defeated, the close logic (see Figure 6.1) can still operate if SELOGIC control equation circuit breaker status setting 52A is set to something other than numeral 0. Making the setting 52A = 0 defeats the close logic and also defeats the reclosing relay.

For example, if 52A = IN101, a 52a circuit breaker auxiliary contact is connected to input IN101. If the reclosing relay does not exist, the close logic still operates, allowing closing to take place via SELOGIC control equation setting CL (close conditions, other than automatic reclosing). See *Close Logic* earlier in this section for more discussion on SELOGIC control equation settings 52A and CL. Also see *Optoisolated Inputs* in *Section 7: Inputs, Outputs, Timers, and Other Control Logic* for more discussion on SELOGIC control equation setting 52A.

Reclosing Relay Timer Settings

The open interval and reset timer factory settings are shown in Table 6.2:

Table 6.2: Reclosing Relay Timer Settings and Setting Ranges

Timer Setting (range)	Factory Setting (in cycles)	Definition
79OI1 (0.00–999999 cyc)	30.00	open interval 1 time
79OI2 (0.00–999999 cyc)	600.00	open interval 2 time
79OI3 (0.00–999999 cyc)	0.00	open interval 3 time
79OI4 (0.00–999999 cyc)	0.00	open interval 4 time
79RSD (0.00–999999 cyc)	1800.00	reset time from reclose cycle state
79RSLD (0.00–999999 cyc)	300.00	reset time from lockout state

The operation of these timers is affected by SELOGIC control equation settings discussed later in this section. Also see the settings sheets at the end of *Section 9: Setting the Relay*.

Open Interval Timers

The reclose enable setting, E79, determines the number of open interval time settings that can be set. For example, if setting E79 = 3, the first three open interval time settings in Table 6.2, are made available for setting.

If an open interval time is set to zero, then that open interval time is not operable, and neither are the open interval times that follow it.

In the factory settings in Table 6.2, the open interval 3 time setting 79OI3 is the first open interval time setting set equal to zero:

$$79OI3 = 0.00 \text{ cycles}$$

Thus, open interval times 79OI3 and 79OI4 are not operable. In the factory settings, both open interval times 79OI3 and 79OI4 are set to zero. But if the settings were:

$$\begin{aligned} 79OI3 &= 0.00 \text{ cycles} \\ 79OI4 &= 900.00 \text{ cycles (set to some value other than zero)} \end{aligned}$$

open interval time 79OI4 would still be inoperative, because a preceding open interval time is set to zero (i.e., 79OI3 = 0.00).

If open interval 1 time setting, 79OI1, is set to zero (79OI1 = 0.00 cycles), no open interval timing takes place, and the reclosing relay is defeated.

The open interval timers time consecutively; they do not have the same beginning time reference point. In the above factory settings, open interval 1 time setting, 79OI1, times first. If the subsequent first reclosure is not successful, then open interval 2 time setting, 79OI2, starts timing. If the subsequent second reclosure is not successful, the relay goes to the Lockout State. See the example time line in Figure 6.6.

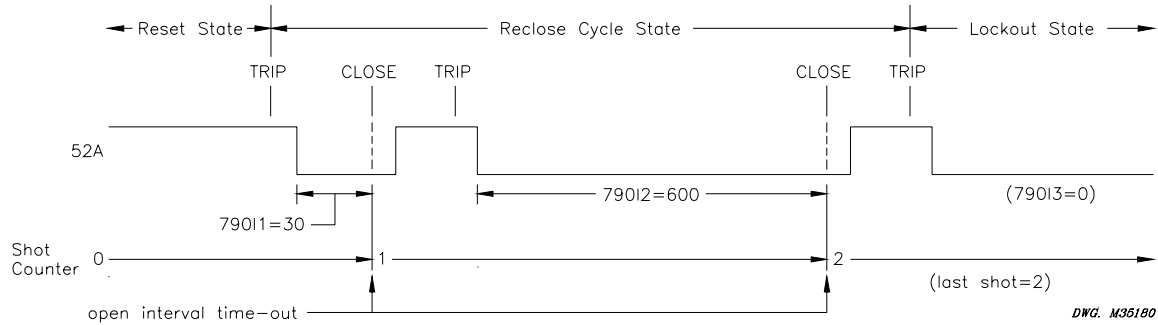


Figure 6.6: Reclosing Sequence From Reset to Lockout With Factory Settings

SELOGIC control equation setting 79STL (stall open interval timing) can be set to control open interval timing [see *Skip Shot and Stall Open Interval Timing Settings (79SKP and 79STL, respectively)* later in this subsection].

Determination of Number of Reclosures (Last Shot)

The number of reclosures is equal to the number of open interval time settings that precede the first open interval time setting set equal to zero. The “last shot” value is also equal to the number of reclosures.

In the above factory settings, two set open interval times precede open interval 3 time, which is set to zero (79OI3 = 0.00):

$$\begin{aligned} 79OI1 &= 30.00 \\ 79OI2 &= 600.00 \\ 79OI3 &= 0.00 \end{aligned}$$

For this example:

$$\text{Number of reclosures (last shot)} = 2 = \text{the number of set open interval times that precede the first open interval set to zero.}$$

Observe Shot Counter Operation

Observe the reclosing relay shot counter operation, especially during testing, with the front-panel shot counter screen (accessed via the OTHER pushbutton). See *Functions Unique to the Front-Panel Interface* in *Section 11: Front-Panel Interface*.

Reset Timer

The reset timer qualifies circuit breaker closure before taking the relay to the Reset State from the Reclose Cycle State or the Lockout State. Circuit breaker status is determined by the SELOGIC control equation setting 52A. (See *Close Logic* earlier in this section for more discussion on SELOGIC control equation setting 52A. Also see *Optoisolated Inputs* in *Section 7: Inputs, Outputs, Timers, and Other Control Logic* for more discussion on SELOGIC control equation setting 52A.)

Setting 79RSD:

Qualifies closures when the relay is in the Reclose Cycle State. These closures are usually automatic reclosures resulting from open interval time-out.

It is also the reset time used in sequence coordination schemes [see *Sequence Coordination (79SEQ)* discussed later in this subsection].

Setting 79RSLD:

Qualifies closures when the relay is in the Lockout State. These closures are usually manual closures. These manual closures can originate external to the relay, via the CLOSE command, or via the SELOGIC control equation setting CL (see Figure 6.1).

Setting 79RSLD is also the reset timer used when the relay powers up, has individual settings changed for the active setting group, or the active setting group is changed (see *Reclosing Relay States and Settings/Setting Group Changes* earlier in this subsection).

Typically, setting 79RSLD is set less than setting 79RSD. Setting 79RSLD emulates reclosing relays with motor-driven timers that have a relatively short reset time from the lockout position to the reset position.

The 79RSD and 79RSLD settings are set independently (setting 79RSLD can even be set greater than setting 79RSD, if desired). SELOGIC control equation setting 79BRS (block reset timing) can be set to control reset timing [see *Block Reset Timing Setting (79BRS)* later in this subsection].

Monitoring Open Interval and Reset Timing

Open interval and reset timing can be monitored with the following Relay Word bits:

<u>Relay Word Bits</u>	<u>Definition</u>
OPTMN	Indicates that the open interval timer is <u>actively</u> timing
RSTMN	Indicates that the reset timer is <u>actively</u> timing

If the open interval timer is actively timing, OPTMN asserts to logical 1. When the relay is not timing on an open interval (e.g., it is in the Reset State or in the Lockout State), OPTMN deasserts to logical 0. The relay can only time on an open interval when it is in the Reclose Cycle State, but just because the relay is in the Reclose Cycle State does not necessarily mean the relay is timing on an open interval. The relay only times on an open interval after successful reclose

initiation and no stall conditions are present [see *Skip Shot and Stall Open Interval Timing Settings (79SKP and 79STL, Respectively)* later in this subsection].

If the reset timer is actively timing, RSTMN asserts to logical 1. If the reset timer is not timing, RSTMN deasserts to logical 0. See *Block Reset Timing Setting (79BRS)* later in this subsection.

Reclosing Relay Shot Counter

Refer to Figure 6.6.

The shot counter increments for each reclose operation. For example, when the relay is timing on open interval 1, 79OI1, it is at shot = 0. When the open interval times out, the shot counter increments to shot = 1 and so forth for the set open intervals that follow. The shot counter cannot increment beyond the last shot for automatic reclosing [see *Determination of Number of Reclosures (Last Shot)* earlier in this subsection]. The shot counter resets back to shot = 0 when the reclosing relay returns to the Reset State.

Table 6.3: Shot Counter Correspondence to Relay Word Bits and Open Interval Times

Shot	Corresponding Relay Word Bit	Corresponding Open Interval
0	SH0	79OI1
1	SH1	79OI2
2	SH2	79OI3
3	SH3	79OI4
4	SH4	

When the shot counter is at a particular shot value (e.g., shot = 2), the corresponding Relay Word bit asserts to logical 1 (e.g., SH2 = logical 1).

The shot counter also increments for sequence coordination operation. The shot counter can increment beyond the last shot for sequence coordination [see *Sequence Coordination Setting (79SEQ)* later in this subsection].

Reclosing Relay SELogic Control Equation Settings Overview

Table 6.4: Reclosing Relay SELOGIC Control Equation Settings

SELOGIC Control Equation Setting	Factory Setting	Definition
79RI	TRIP	Reclose Initiate
79RIS	52A + 79CY	Reclose Initiate Supervision
79DTL	OC + !IN102 + LB3	Drive-to-Lockout
79DLS	79LO	Drive-to-Last Shot
79SKP	0	Skip Shot
79STL	TRIP	Stall Open Interval Timing
79BRS	0	Block Reset Timing
79SEQ	0	Sequence Coordination
79CLS	1	Reclose Supervision

These settings are discussed in detail in the remainder of this subsection.

Reclose Initiate and Reclose Initiate Supervision Settings (79RI and 79RIS, Respectively)

The reclose initiate setting 79RI is a rising-edge detect setting. The reclose initiate supervision setting 79RIS supervises setting 79RI. When setting 79RI senses a rising edge (logical 0 to logical 1 transition), setting 79RIS has to be at logical 1 (79RIS = logical 1) in order for open interval timing to be initiated.

If 79RIS = logical 0 when setting 79RI senses a rising edge (logical 0 to logical 1 transition), the relay goes to the Lockout State.

Factory Settings Example

With factory settings:

$$\begin{aligned}79RI &= \text{TRIP} \\79RIS &= 52A + 79CY\end{aligned}$$

the transition of the TRIP Relay Word bit from logical 0 to logical 1 initiates open interval timing only if the 52A + 79CY Relay Word bit is at logical 1 (52A = logical 1, or 79CY = logical 1). Input IN101 is assigned as the breaker status input in the factory settings (52A = IN101).

The circuit breaker has to be closed (circuit breaker status 52A = logical 1) at the instant of the first trip of the auto-reclose cycle in order for the SEL-351 to successfully initiate reclosing and start timing on the first open interval. The SEL-351 is not yet in the reclose cycle state (79CY = logical 0) at the instant of the first trip.

Then for any subsequent trip operations in the auto-reclose cycle, the SEL-351 is in the reclose cycle state (79CY = logical 1) and the SEL-351 successfully initiates reclosing for each trip.

Because of factory setting $79RIS = 52A + 79CY$, successful reclose initiation in the reclose cycle state ($79CY = \text{logical } 1$) is not dependent on the circuit breaker status ($52A$). This allows successful reclose initiation for the case of an instantaneous trip, but the circuit breaker status indication is slow—the instantaneous trip (reclose initiation) occurs before the SEL-351 sees the circuit breaker close.

If a flashover occurs in a circuit breaker tank during an open interval (circuit breaker open and the SEL-351 calls for a trip), the SEL-351 goes immediately to lockout.

Additional Settings Example

The preceding settings example initiates open interval timing on rising edge of the TRIP Relay Word bit. The following is an example of reclose initiation on the opening of the circuit breaker.

Presume input IN101 is connected to a 52a circuit breaker auxiliary contact ($52A = \text{IN101}$).

With setting:

$$79RI = !52A$$

the transition of the 52A Relay Word bit from logical 1 to logical 0 (breaker opening) initiates open interval timing. Setting 79RI looks for a logical 0 to logical 1 transition, thus Relay Word bit 52A is inverted in the 79RI setting [$!52A = \text{NOT}(52A)$].

The reclose initiate supervision setting 79RIS supervises setting 79RI. With settings:

$$\begin{aligned} 79RI &= !52A \\ 79RIS &= \text{TRIP} \end{aligned}$$

the transition of the 52A Relay Word bit from logical 1 to logical 0 initiates open interval timing only if the TRIP Relay Word bit is at logical 1 ($\text{TRIP} = \text{logical } 1$). Thus, the TRIP Relay Word bit has to be asserted when the circuit breaker opens in order to initiate open interval timing. With a long enough setting of the Minimum Trip Duration Timer (TDURD), the TRIP Relay Word bit will still be asserted to logical 1 when the circuit breaker opens (see Figure 5.1 and Figure 5.2 in *Section 5: Trip and Target Logic*).

If the TRIP Relay Word bit is at logical 0 ($\text{TRIP} = \text{logical } 0$) when the circuit breaker opens (logical 1 to logical 0 transition), the relay goes to the Lockout State. This helps prevent reclose initiation for circuit breaker openings caused by trips external to the relay.

If circuit breaker status indication ($52A$) is slow, additional setting change $\text{ULCL} = 0$ (unlatch close; refer to Figure 6.1 and accompanying explanation) may need to be made when $79RI = !52A$. $\text{ULCL} = 0$ avoids going to lockout prematurely for an instantaneous trip after an auto-reclose by not turning CLOSE off until the circuit breaker status indication tells the relay that the breaker is closed. The circuit breaker anti-pump circuitry should take care of the TRIP and CLOSE being on together for a short period of time.

Other Settings Considerations

1. In the preceding additional setting example, the reclose initiate setting (79RI) includes input IN101, that is connected to a 52a breaker auxiliary contact (52A = IN101).

$$79RI = !52A$$

If a 52b breaker auxiliary contact is connected to input IN101 (52A = !IN101), the reclose initiate setting (79RI) remains the same.

2. If no reclose initiate supervision is desired, make the following setting:

$$79RIS = 1 \quad \text{(numeral 1)}$$

Setting 79RIS = logical 1 at all times. Any time a logical 0 to logical 1 transition is detected by setting 79RI, open interval timing will be initiated (unless prevented by other means).

3. If the following setting is made:

$$79RI = 0 \quad \text{(numeral 0)}$$

reclosing will never take place (reclosing is never initiated). The reclosing relay is effectively inoperative.

4. If the following setting is made:

$$79RIS = 0 \quad \text{(numeral 0)}$$

reclosing will never take place (the reclosing relay goes directly to the lockout state any time reclosing is initiated). The reclosing relay is effectively inoperative.

Drive-to-Lockout and Drive-to-Last Shot Settings (79DTL and 79DLS, Respectively)

When 79DTL = logical 1, the reclosing relay goes to the Lockout State (Relay Word bit 79LO = logical 1), and the front-panel LO (Lockout) LED illuminates.

79DTL has a 60-cycle dropout time. This keeps the drive-to-lockout condition up 60 more cycles after 79DTL has reverted back to 79DTL = logical 0. This is useful for situations where both of the following are true:

- Any of the trip and drive-to-lockout conditions are “pulsed” conditions (e.g., the OPEN Command Relay Word bit, OC, asserts for only 1/4 cycle—refer to the following *Factory Settings Example*).
- Reclose initiation is by the breaker contact opening (e.g., 79RI = !52A—refer to *Additional Settings Example* in the preceding setting 79RI [reclose initiation] discussion).

Then the drive-to-lockout condition overlaps reclose initiation and the SEL-351 stays in lockout after the breaker trips open.

When 79DLS = logical 1, the reclosing relay goes to the last shot, if the shot counter is not at a shot value greater than or equal to the calculated last shot (see *Reclosing Relay Shot Counter* earlier in this subsection).

Factory Settings Example

The drive-to-lockout factory setting is:

$$79DTL = !IN102 + LB3 + OC$$

Optoisolated input IN102 is set to operate as a reclose enable switch (see *Optoisolated Inputs* in *Section 7: Inputs, Outputs, Timers, and Other Control Logic*). When Relay Word bit IN102 = logical 1 (reclosing enabled), the relay is not driven to the Lockout State (assuming local bit LB3 = logical 0, too):

$$\begin{aligned} !IN102 &= !(logical\ 1) = NOT(logical\ 1) = logical\ 0 \\ 79DTL &= !IN102 + LB3 + OC = (logical\ 0) + LB3 = LB3 + OC \end{aligned}$$

When Relay Word bit IN102 = logical 0 (reclosing disabled), the relay is driven to the Lockout State:

$$\begin{aligned} !IN102 &= !(logical\ 0) = NOT(logical\ 0) = logical\ 1 \\ 79DTL &= !IN102 + LB3 + OC = (logical\ 1) + LB3 + OC = logical\ 1 \end{aligned}$$

Local bit LB3 is set to operate as a manual trip switch (see *Local Control Switches* in *Section 7: Inputs, Outputs, Timers, and Other Control Logic* and *Trip Logic* in *Section 5: Trip and Target Logic*). When Relay Word bit LB3 = logical 0 (no manual trip), the relay is not driven to the Lockout State (assuming optoisolated input IN102 = logical 1, too):

$$79DTL = !IN102 + LB3 + OC = NOT(IN102) + (logical\ 0) + OC = NOT(IN102) + OC$$

When Relay Word bit LB3 = logical 1 (manual trip), the relay is driven to the Lockout State:

$$79DTL = !IN102 + LB3 + OC = NOT(IN102) + (logical\ 1) + OC = logical\ 1$$

Relay Word bit OC asserts for execution of the OPEN Command. See the Note in the *Lockout State* discussion, following Table 6.1.

The drive-to-last shot factory setting is:

$$79DLS = 79LO$$

Two open intervals are also set in the factory settings, resulting in last shot = 2. Any time the relay is in the lockout state (Relay Word bit 79LO = logical 1), the relay is driven to last shot (if the shot counter is not already at a shot value greater than or equal to shot = 2):

$$79DLS = 79LO = logical\ 1$$

Thus, if optoisolated input IN102 (reclose enable switch) is in the “disable reclosing” position (Relay Word bit IN102 = logical 0) or local bit LB3 (manual trip switch) is operated, then the relay is driven to the Lockout State (by setting 79DTL) and, subsequently, last shot (by setting 79DLS).

Additional Settings Example 1

The preceding drive-to-lockout factory settings example drives the relay to the Lockout State immediately when the reclose enable switch (optoisolated input IN102) is put in the “reclosing disabled” position (Relay Word bit IN102 = logical 0):

$$79DTL = !IN102 + \dots = \text{NOT}(IN102) + \dots = \text{NOT}(\text{logical } 0) + \dots = \text{logical } 1$$

To disable reclosing, but not drive the relay to the Lockout State until the relay trips, make settings similar to the following:

$$79DTL = !IN102 * TRIP + \dots$$

Additional Settings Example 2

To drive the relay to the Lockout State for fault current above a certain level when tripping (e.g., level of phase instantaneous overcurrent element 50P3), make settings similar to the following:

$$79DTL = TRIP * 50P3 + \dots$$

Additionally, if the reclosing relay should go to the Lockout State for an underfrequency trip, make settings similar to the following:

$$79DTL = TRIP * 81D1T + \dots$$

Other Settings Considerations

If no special drive-to-lockout or drive-to-last shot conditions are desired, make the following settings:

$$79DTL = 0 \quad \text{(numeral 0)}$$

$$79DLS = 0 \quad \text{(numeral 0)}$$

With settings 79DTL and 79DLS inoperative, the relay still goes to the Lockout State (and to last shot) if an entire automatic reclose sequence is unsuccessful.

Overall, settings 79DTL or 79DLS are needed to take the relay to the Lockout State (or to last shot) for immediate circumstances.

Skip Shot and Stall Open Interval Timing Settings (79SKP and 79STL, Respectively)

The skip shot setting 79SKP causes a reclose shot to be skipped. Thus, an open interval time is skipped, and the next open interval time is used instead.

If 79SKP = logical 1 at the instant of successful reclose initiation (see preceding discussion on settings 79RI and 79RIS), the relay increments the shot counter to the next shot and then loads the open interval time corresponding to the new shot (see Table 6.3). If the new shot is the “last shot,” no open interval timing takes place, and the relay goes to the Lockout State if the circuit breaker is open (see *Lockout State* earlier in this subsection).

After successful reclose initiation, open interval timing does not start until allowed by the stall open interval timing setting 79STL. If 79STL = logical 1, open interval timing is stalled. If 79STL = logical 0, open interval timing can proceed.

If an open interval time has not yet started timing (79STL = logical 1 still), the 79SKP setting is still processed. In such conditions (open interval timing has not yet started timing), if 79SKP = logical 1, the relay increments the shot counter to the next shot and then loads the open interval time corresponding to the new shot (see Table 6.3). If the new shot turns out to be the “last shot,” no open interval timing takes place, and the relay goes to the Lockout State if the circuit breaker is open (see *Lockout State* earlier in this subsection).

If the relay is in the middle of timing on an open interval and 79STL changes state to 79STL = logical 1, open interval timing stops where it is. If 79STL changes state back to 79STL = logical 0, open interval timing resumes where it left off. Use the OPTMN Relay Word bit to monitor open interval timing (see *Monitoring Open Interval and Reset Timing* earlier in this subsection).

Factory Settings Example

The skip shot function is not enabled in the factory settings:

$$79SKP = 0 \quad (\text{numeral } 0)$$

The stall open interval timing factory setting is:

$$79STL = \text{TRIP}$$

After successful reclose initiation, open interval timing does not start as long as the trip condition is present (Relay Word bit TRIP = logical 1). As discussed previously, if an open interval time has not yet started timing (79STL = logical 1 still), the 79SKP setting is still processed. Once the trip condition goes away (Relay Word bit TRIP = logical 0), open interval timing can proceed.

Additional Settings Example 1

With skip shot factory setting:

$$79SKP = 50P2 * SH0$$

if shot = 0 (Relay Word bit SH0 = logical 1) and phase current is above the phase instantaneous overcurrent element 50P2 threshold (Relay Word bit 50P2 = logical 1), at the instant of successful reclose initiation, the shot counter is incremented from shot = 0 to shot = 1. Then, open interval 1 time (setting 79OI1) is skipped, and the relay times on the open interval 2 time (setting 79OI2) instead.

Table 6.5: Open Interval Time Factory Settings

Shot	Corresponding Relay Word Bit	Corresponding Open Interval	Open Interval Time Factory Setting
0	SH0	79OI1	30 cycles
1	SH1	79OI2	600 cycles

In Table 6.5, note that the open interval 1 time (setting 79OI1) is a short time, while the following open interval 2 time (setting 79OI2) is significantly longer. For a high magnitude fault (greater than the phase instantaneous overcurrent element 50P2 threshold), open interval 1 time is skipped, and open interval timing proceeds on the following open interval 2 time.

Once the shot is incremented to shot = 1, Relay Word bit SH0 = logical 0 and then setting 79SKP = logical 0, regardless of Relay Word bit 50P2.

Additional Settings Example 2

If the SEL-351 Relay is used on a feeder with a line-side independent power producer (cogenerator), the utility should not reclose into a line still energized by an islanded generator. To monitor line voltage and block reclosing, connect a line-side single-phase potential transformer to channel VS on the SEL-351 Relay as shown in Figure 6.7.

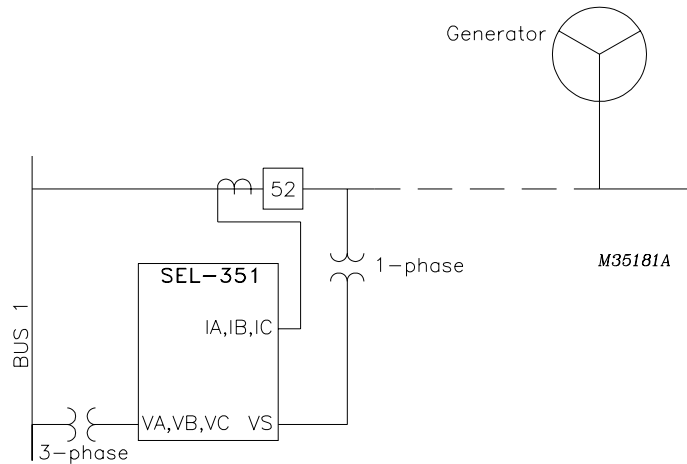


Figure 6.7: Reclose Blocking for Islanded Generator

If the line is energized, channel VS overvoltage element 59S1 can be set to assert. Make the following setting:

$$79STL = 59S1 + \dots$$

If line voltage is present, Relay Word bit 59S1 asserts, stalling open interval timing (reclose block). If line voltage is not present, Relay Word bit 59S1 deasserts, allowing open interval timing to proceed (unless some other set condition stalls open interval timing).

Additional Settings Example 3

Refer to Figure 6.4 and accompanying setting example, showing an application for setting 79STL.

Other Settings Considerations

If no special skip shot or stall open interval timing conditions are desired, make the following settings:

$$\begin{aligned} 79SKP &= 0 && \text{(numeral 0)} \\ 79STL &= 0 && \text{(numeral 0)} \end{aligned}$$

Block Reset Timing Setting (79BRS)

The block reset timing setting 79BRS keeps the reset timer from timing. Depending on the reclosing relay state, the reset timer can be loaded with either reset time:

79RSD (Reset Time from Reclose Cycle)

or

79RSLD (Reset Time from Lockout)

Depending on how setting 79BRS is set, none, one, or both of these reset times can be controlled. If the reset timer is timing and then 79BRS asserts to:

79BRS = logical 1

reset timing is stopped and does not begin timing again until 79BRS deasserts to:

79BRS = logical 0

When reset timing starts again, the reset timer is fully loaded. Thus, successful reset timing has to be continuous. Use the RSTMN Relay Word bit to monitor reset timing (see *Monitoring Open Interval and Reset Timing* earlier in this subsection).

Factory Settings Example

The block reset function is not enabled in the factory settings:

79BRS = 0 (numeral 0)

Additional Settings Example 1

The block reset timing setting is:

79BRS = (51P + 51G) * 79CY

Relay Word bit 79CY corresponds to the Reclose Cycle State. The reclosing relay is in one of the three reclosing relay states at any one time (see Figure 6.5 and Table 6.1).

When the relay is in the Reset or Lockout States, Relay Word bit 79CY is deasserted to logical 0. Thus, the 79BRS setting has no effect when the relay is in the Reset or Lockout States. When a circuit breaker is closed from lockout, there could be cold load inrush current that momentarily picks up a time-overcurrent element [e.g., phase time-overcurrent element 51PT pickup (51P) asserts momentarily]. But, this assertion of pickup 51P has no effect on reset timing because the relay is in the Lockout State (79CY = logical 0). The relay will time immediately on reset time 79RSLD and take the relay from the Lockout State to the Reset State with no additional delay because 79BRS is deasserted to logical 0.

When the relay is in the Reclose Cycle State, Relay Word bit 79CY is asserted to logical 1. Thus, the factory 79BRS setting can function to block reset timing if time-overcurrent pickup 51P or 51G is picked up while the relay is in the Reclose Cycle State. This helps prevent repetitive “trip-reclose” cycling.

Additional Settings Example 2

If the block reset timing setting is:

$$79BRS = 51P + 51G$$

then reset timing is blocked if time-overcurrent pickup 51P or 51G is picked up, regardless of the reclosing relay state.

Sequence Coordination Setting (79SEQ)

The sequence coordination setting 79SEQ keeps the relay in step with a downstream line recloser in a sequence coordination scheme, which prevents overreaching SEL-351 Relay overcurrent elements from tripping for faults beyond the line recloser. This is accomplished by incrementing the shot counter and supervising overcurrent elements with resultant shot counter elements.

In order for the sequence coordination setting 79SEQ to increment the shot counter, both the following conditions must be true:

No trip present (Relay Word bit TRIP = logical 0)

Circuit breaker closed (SELOGIC control equation setting 52A = logical 1, effectively)

The sequence coordination setting 79SEQ is usually set with some overcurrent element pickups. If the above two conditions are both true, and a set overcurrent element pickup asserts for at least 1.25 cycles and then deasserts, the shot counter increments by one count. This assertion/deassertion indicates that a downstream device (e.g., line recloser—see Figure 6.8) has operated to clear a fault. Incrementing the shot counter keeps the SEL-351 Relay “in step” with the downstream device, as is shown in the following *Additional Settings Example 1* and *Additional Settings Example 2*.

Every time a sequence coordination operation occurs, the shot counter is incremented, and the reset timer is loaded up with reset time 79RSD. Sequence coordination can increment the shot counter beyond last shot, but no further than shot = 4. The shot counter returns to shot = 0 after the reset timer times out. Reset timing is subject to SELOGIC control equation setting 79BRS [see *Block Reset Timing Setting (79BRS)* earlier in this subsection].

Sequence coordination operation does not change the reclosing relay state. For example, if the relay is in the Reset State and there is a sequence coordination operation, it remains in the Reset State.

Factory Settings Example

Sequence coordination is not enabled in the factory settings:

$$79SEQ = 0$$

Additional Settings Example 1

With sequence coordination setting:

$$79SEQ = 79RS * 51P$$

sequence coordination is operable only when the relay is in the Reset State (79RS = logical 1). Refer to Figure 6.8 and Figure 6.9.

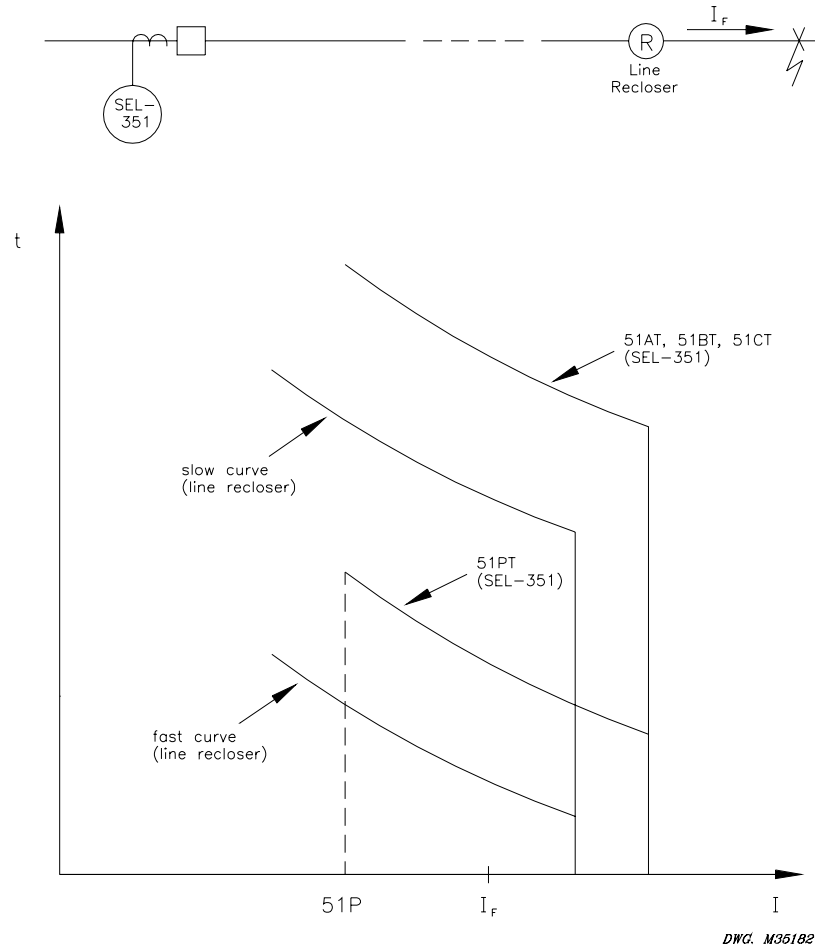


Figure 6.8: Sequence Coordination Between the SEL-351 Relay and a Line Recloser

Assume that the line recloser is set to operate twice on the fast curve and then twice on the slow curve. The slow curve is allowed to operate after two fast curve operations because the fast curves are then inoperative for tripping. The SEL-351 Relay phase time-overcurrent element 51PT is coordinated with the line recloser fast curve. The SEL-351 Relay single-phase time-overcurrent elements 51AT, 51BT, and 51CT are coordinated with the line recloser slow curve.

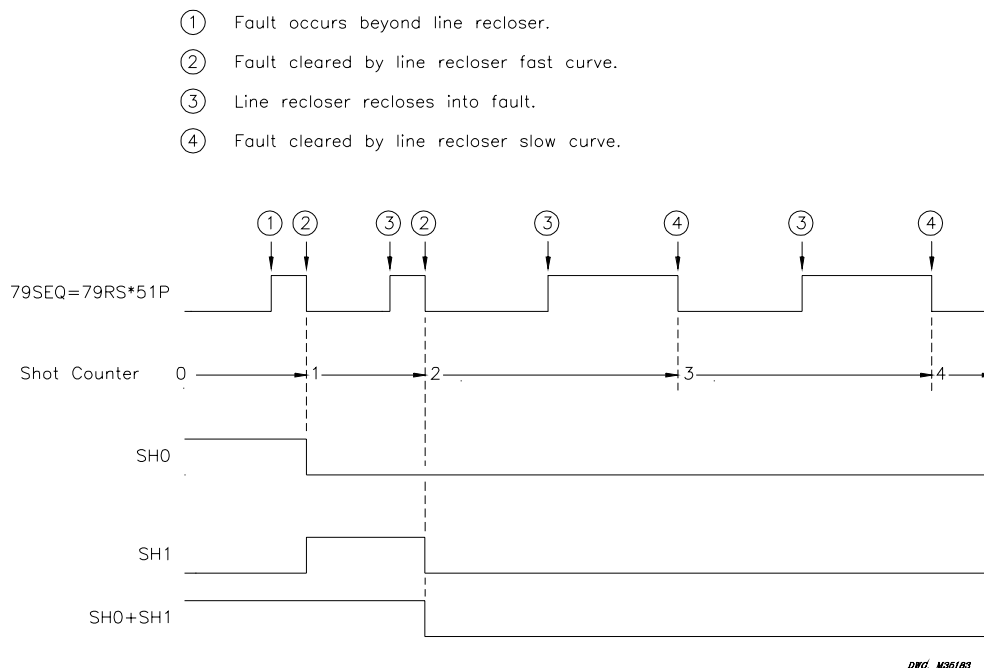


Figure 6.9: Operation of SEL-351 Relay Shot Counter for Sequence Coordination With Line Recloser (Additional Settings Example 1)

If the SEL-351 Relay is in the Reset State ($79RS = \text{logical } 1$) and then a permanent fault beyond the line recloser occurs (fault current I_F in Figure 6.8), the line recloser fast curve operates to clear the fault. The SEL-351 Relay also sees the fault. The phase time-overcurrent pickup 51P asserts and then deasserts without tripping, incrementing the relay shot counter from:

$$\text{shot} = 0 \text{ to shot} = 1$$

When the line recloser recloses its circuit breaker, the line recloser fast curve operates again to clear the fault. The SEL-351 Relay also sees the fault again. The phase time-overcurrent pickup 51P asserts and then deasserts without tripping, incrementing the relay shot counter from:

$$\text{shot} = 1 \text{ to shot} = 2$$

The line recloser fast curve is now disabled after operating twice. When the line recloser recloses its circuit breaker, the line recloser slow curve operates to clear the fault. The relay does not operate on its faster-set phase time-overcurrent element 51PT (51PT is “below” the line recloser slow curve) because the shot counter is now at shot = 2. For this sequence coordination scheme, the SELOGIC control equation trip equation is:

$$\text{TR} = 51\text{PT} * (\text{SH0} + \text{SH1}) + 51\text{AT} + 51\text{BT} + 51\text{CT}$$

With the shot counter at shot = 2, Relay Word bits SH0 (shot = 0) and SH1 (shot = 1) are both deasserted to logical 0. This keeps the 51PT phase time-overcurrent element from tripping. The 51PT phase time-overcurrent element is still operative, and its pickup (51P) can still assert and then deassert, thus continuing the sequencing of the shot counter to shot = 3, etc. The 51PT phase time-overcurrent element cannot cause a trip because $\text{shot} \geq 2$, and SH0 and SH1 both are deasserted to logical 0.

Note: Sequence coordination can increment the shot counter beyond last shot in this example (last shot = 2 in this factory setting example) but no further than shot = 4.

The following Example 2 limits sequence coordination shot counter incrementing.

The shot counter returns to shot = 0 after the reset timer (loaded with reset time 79RSD) times out.

Additional Settings Example 2

Review preceding Example 1.

Assume that the line recloser in Figure 6.8 is set to operate twice on the fast curve and then twice on the slow curve for faults beyond the line recloser.

Assume that the SEL-351 Relay is set to operate once on 51PT and then twice on 51AT, 51BT, or 51CT for faults between the SEL-351 Relay and the line recloser. This results in the following trip setting:

$$TR = 51PT * (SHO) + 51AT + 51BT + 51CT$$

This requires that two open interval settings be made (see Table 6.2 and Figure 6.6). This corresponds to the last shot being:

$$\text{last shot} = 2$$

If the sequence coordination setting is:

$$79SEQ = 79RS * 51P$$

and there is a permanent fault beyond the line recloser, the shot counter of the SEL-351 Relay will increment all the way to shot = 4 (see Figure 6.9). If there is a coincident fault between the SEL-351 Relay and the line recloser, the SEL-351 Relay will trip and go to the Lockout State. Any time the shot counter is at a value equal to or greater than last shot and the relay trips, it goes to the Lockout State.

To avoid this problem, make the following sequence coordination setting:

$$79SEQ = 79RS * 51P * SH0$$

Refer to Figure 6.10.

If the SEL-351 Relay is in the Reset State (79RS = logical 0) with the shot counter reset (shot = 0; SH0 = logical 1) and then a permanent fault beyond the line recloser occurs (fault current I_F in Figure 6.8), the line recloser fast curve operates to clear the fault. The SEL-351 Relay also sees the fault. The phase time-overcurrent pickup 51P asserts and then deasserts without tripping, incrementing the relay shot counter from:

$$\text{shot} = 0 \text{ to shot} = 1$$

Now the SEL-351 Relay cannot operate on its faster-set phase time-overcurrent element 51PT because the shot counter is at shot = 1 (SH0 = logical 0):

$$\begin{aligned} \text{TR} &= 51\text{PT} * (\text{SH0}) + 51\text{AT} + 51\text{BT} + 51\text{CT} \\ &= 51\text{PT} * (\text{logical } 0) + 51\text{AT} + 51\text{BT} + 51\text{CT} \\ &= 51\text{AT} + 51\text{BT} + 51\text{CT} \end{aligned}$$

- ① Fault occurs beyond line recloser.
- ② Fault cleared by line recloser fast curve.
- ③ Line recloser recloses into fault.
- ④ Fault cleared by line recloser slow curve.

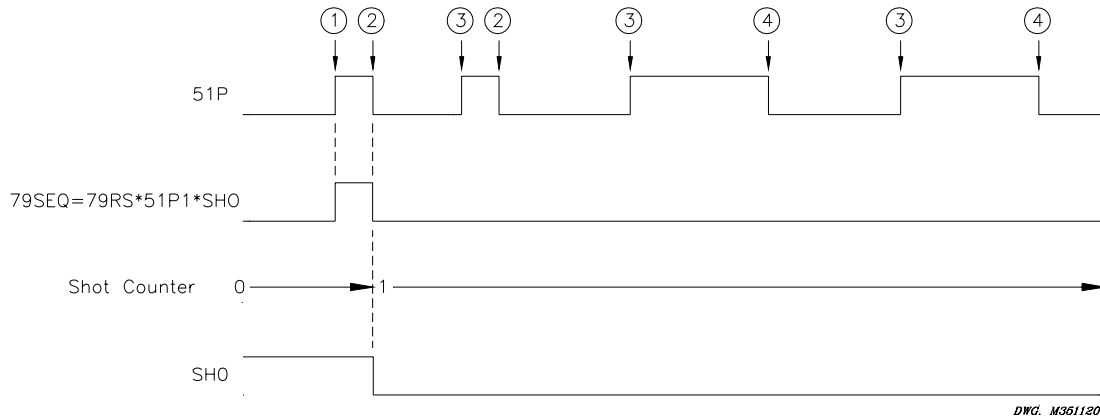


Figure 6.10: Operation of SEL-351 Relay Shot Counter for Sequence Coordination With Line Recloser (Additional Settings Example 2)

The line recloser continues to operate for the permanent fault beyond it, but the SEL-351 Relay shot counter does not continue to increment. Sequence coordination setting 79SEQ is effectively disabled by the shot counter incrementing from shot = 0 to shot = 1.

$$79\text{SEQ} = 79\text{RS} * 51\text{P} * \text{SH0} = 79\text{RS} * 51\text{P} * (\text{logical } 0) = \text{logical } 0$$

The shot counter stays at shot = 1.

Thus, if there is a coincident fault between the SEL-351 Relay and the line recloser, the SEL-351 Relay will operate on 51AT, 51BT, or 51CT and then reclose once, instead of going straight to the Lockout State (shot = 1 < last shot = 2).

As stated earlier, the reset time setting 79RSD takes the shot counter back to shot = 0 after a sequence coordination operation increments the shot counter. Make sure that reset time setting 79RSD is set long enough to maintain the shot counter at shot = 1 as shown in Figure 6.10.

Reclose Supervision Setting (79CLS)

See *Reclose Supervision Logic* earlier in this section.

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SECTION 7: INPUTS, OUTPUTS, TIMERS, AND OTHER CONTROL LOGIC

This section explains the settings and operation of:

Optoisolated inputs.....IN101–IN106	models 0351x0, 0351x1, and 0351xY
IN201–IN208	models 0351x1 and 0351xY
Local control switches.....local bits LB1–LB16	
Remote control switches.....remote bits RB1–RB16	
Latch control switches.....latch bits LT1–LT16	
Multiple setting groups.....group switching settings SS1–SS6	
SELOGIC [®] control equations variables/timers.....SV1/SV1T–SV16/SV16T	
Output contacts.....OUT101–OUT107 and ALARM.....	models 0351x0, 0351x1, and 0351xY
OUT201–OUT212	models 0351x1 and 0351xY
Rotating default displays	display points DP1–DP16

The above items are all the logic input/output of the relay. They are combined with the overcurrent, voltage, frequency, and reclosing elements in SELOGIC control equation settings to realize numerous protection and control schemes.

Relay Word bits and SELOGIC control equation setting examples are used throughout this section. See **Section 9: Setting the Relay** for more information on Relay Word bits and SELOGIC control equation settings. See **Section 10: Serial Port Communications and Commands** for more information on viewing and making SELOGIC control equation settings (commands **SHO L** and **SET L**).

OPTOISOLATED INPUTS

Figure 7.1 and Figure 7.2 show the resultant Relay Word bits (e.g., Relay Word bits IN101 through IN106 in Figure 7.1) that follow corresponding optoisolated inputs (e.g., optoisolated inputs IN101 through IN106 in Figure 7.1) for the different SEL-351 Relay models. The figures show examples of energized and deenergized optoisolated inputs and corresponding Relay Word bit states. To assert an input, apply rated control voltage to the appropriate terminal pair (see Figure 1.2 through Figure 1.4 and Figure 2.2 through Figure 2.4).

Figure 7.1 is used for following discussion/examples. The optoisolated inputs in Figure 7.2 operate similarly.

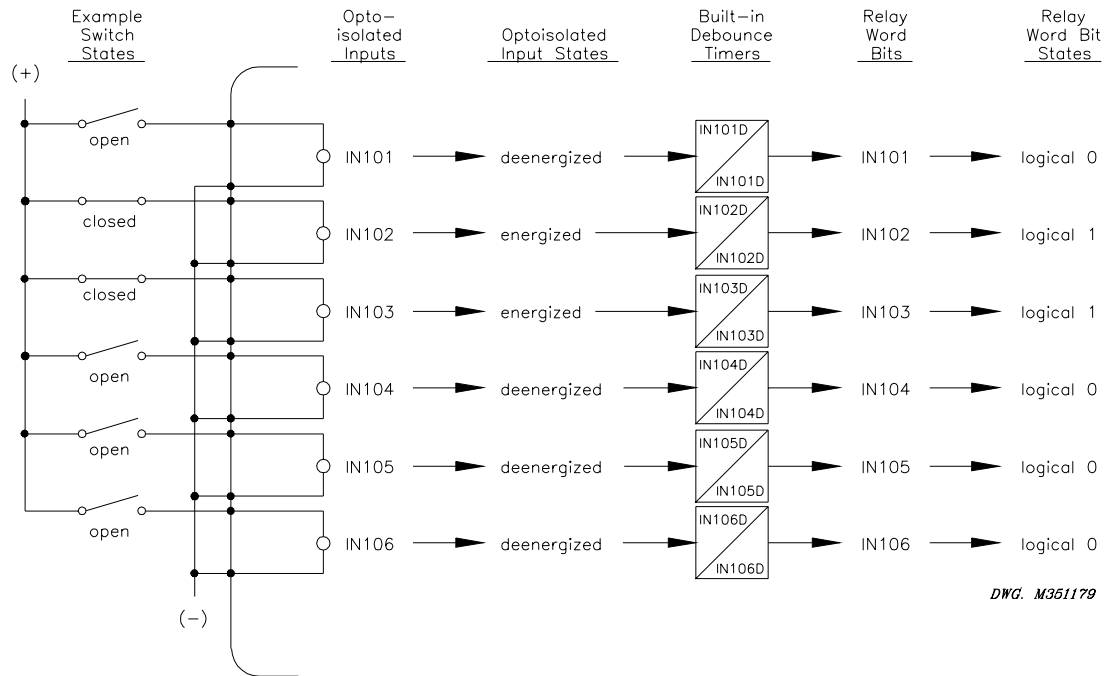


Figure 7.1: Example Operation of Optoisolated Inputs IN101 Through IN106 (Models 0351x0, 0351x1, and 0351xY)

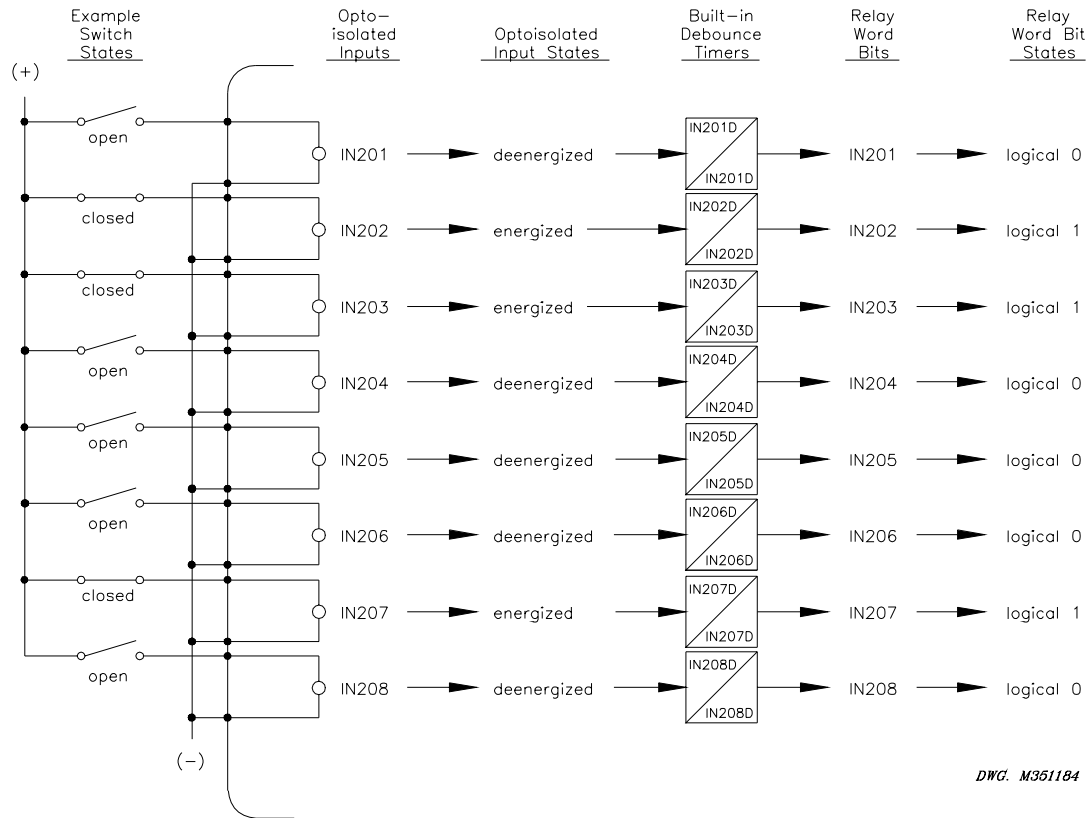


Figure 7.2: Example Operation of Optoisolated Inputs IN201 Through IN208—Extra I/O Board (Models 0351x1 and 0351xY)

Input Debounce Timers

See Figure 7.1.

Each input has settable pickup/dropout timers (IN101D through IN106D) for input energization/deenergization debounce. Note that a given time setting (e.g., IN101D = 0.50) is applied to both the pickup and dropout time for the corresponding input.

Time settings IN101D through IN106D are settable from 0.00 to 1.00 cycles, or ac. The relay takes the entered time setting and internally runs the timer at the nearest 1/16-cycle. For example, if setting IN105D = 0.80, internally the timer runs at the nearest 1/16-cycle: 13/16-cycles (13/16 = 0.8125).

The ac setting allows the input to sense ac control signals. The input has a maximum pickup time of 0.75 cycles and a maximum dropout time of 1.25 cycles. The ac setting qualifies the input by not asserting until two successive 1/16 cycle samples are higher than the optoisolated input threshold voltage and not deasserting until sixteen successive 1/16 cycle samples are lower than the optoisolated input voltage threshold.

For most dc applications, the input pickup/dropout debounce timers should be set in 1/4-cycle increments. For example, in the factory default settings, all the optoisolated input pickup/dropout debounce timers are set at 1/2-cycle (e.g., IN104 = 0.50). See ***SHO Command (Show/View Settings)*** in ***Section 10: Serial Port Communications and Commands*** for a list of the factory default settings.

Only a few applications (e.g., communications-assisted tripping schemes) might require input pickup/dropout debounce timers set less than 1/4-cycle [e.g., if setting IN105D = 0.13, internally the timer runs at the nearest 1/16-cycle: 2/16-cycles (2/16 = 0.1250)].

The relay processing interval is 1/4-cycle, so Relay Word bits IN101 through IN106 are updated every 1/4-cycle. The optoisolated input status may have made it through the pickup/dropout debounce timer (for settings less than 1/4-cycle) because these timers run each 1/16-cycle, but Relay Word bits IN101 through IN106 are updated every 1/4-cycle.

If more than 1 cycle of debounce is needed, run Relay Word bit INn (n = 1 through 6) through a SELOGIC control equation variable timer and use the output of the timer for input functions (see Figure 7.24 and Figure 7.25).

Input Functions

There are **no** optoisolated input settings such as:

IN101 =

IN102 =

Optoisolated inputs IN101 through IN106 receive their function by how their corresponding Relay Word bits IN101 through IN106 are used in SELOGIC control equations.

Factory Settings Examples

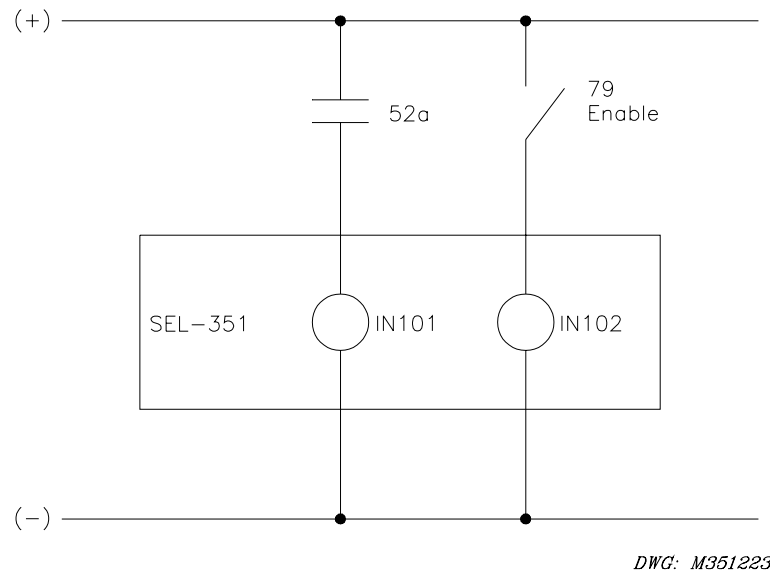


Figure 7.3: Circuit Breaker Auxiliary Contact and Reclose Enable Switch Connected to Optoisolated Inputs IN101 and IN102

The functions for inputs IN101 and IN102 are described in the following discussions.

Input IN101

Relay Word bit IN101 is used in the factory settings for the SELOGIC control equation circuit breaker status setting:

$$52A = \text{IN101}$$

Connect input IN101 to a 52a circuit breaker auxiliary contact.

If a 52b circuit breaker auxiliary contact is connected to input IN101, the setting is changed to:

$$52A = !\text{IN101} \quad [!\text{IN101} = \text{NOT}(\text{IN101})]$$

See *Close Logic* in **Section 6: Close and Reclose Logic** for more information on SELOGIC control equation setting 52A.

The pickup/dropout timer for input IN101 (IN101D) is set at:

$$\text{IN101D} = 0.75 \text{ cycles}$$

to provide input energization/deenergization debounce.

Input IN101 is also used in other factory settings [i.e., SELOGIC control equation settings BSYNCH (see **Section 3: Overcurrent, Voltage, Synchronism Check, Frequency, and Power Elements**), 79RIS (see **Section 6: Close and Reclose Logic**), and DP2 (see **Rotating Default Displays** at the end of this section)]. Using Relay Word bit IN101 for the circuit breaker status setting 52A does not prevent using Relay Word bit IN101 in other SELOGIC control equation settings.

Input IN102

Relay Word bit IN102 is used in the factory settings for the SELOGIC control equation drive-to-lockout setting:

$$79DTL = !IN102 + \dots \quad [=NOT(IN102) + \dots]$$

Connect input IN102 to a reclose enable switch.

When the reclose enable switch is open, input IN102 is deenergized and the reclosing relay is driven to lockout:

$$79DTL = !IN102 + \dots = NOT(IN102) + \dots = NOT(\text{logical } 0) + \dots = \text{logical } 1$$

When the reclose enable switch is closed, input IN102 is energized and the reclosing relay is enabled, if no other setting condition is driving the reclosing relay to lockout:

$$79DTL = !IN102 + \dots = NOT(IN102) + \dots = NOT(\text{logical } 1) + \dots = \text{logical } 0 + \dots$$

See **Section 6: Close and Reclose Logic** for more information on SELOGIC control equation setting 79DTL.

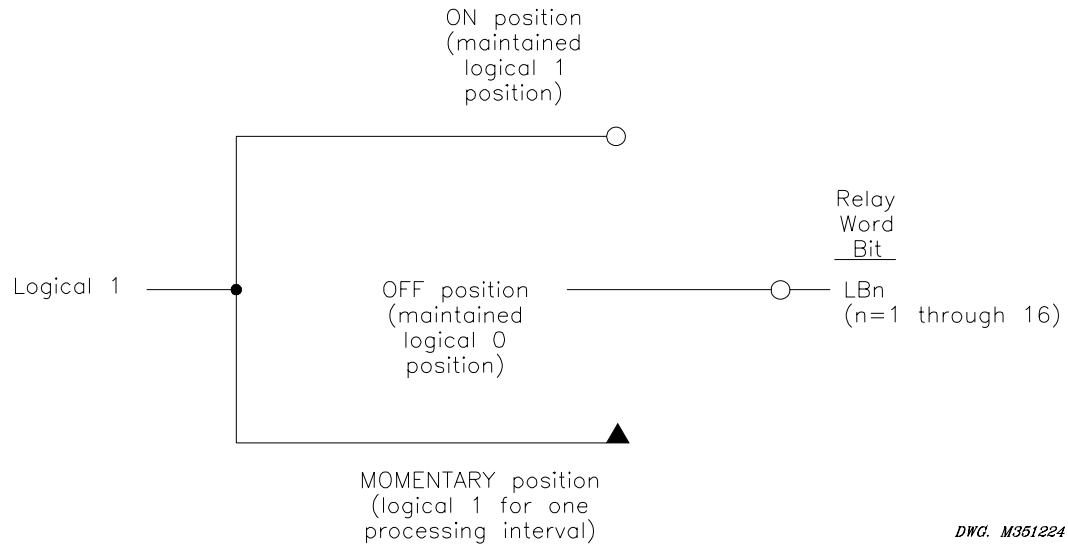
The pickup/dropout timer for input IN102 (IN102D) is set at:

$$IN102D = 1.00 \text{ cycle}$$

to provide input energization/deenergization debounce.

LOCAL CONTROL SWITCHES

The local control switch feature of this relay replaces traditional panel-mounted control switches. Operate the sixteen (16) local control switches using the front-panel keyboard/display (see *Section 11: Front-Panel Interface*).



The switch representation in this figure is derived from the standard:

Graphics Symbols for Electrical and Electronics Diagrams
IEEE Std 315-1975, CSA Z99-1975, ANSI Y32.2-1975,
4.11 Combination Locking and Nonlocking Switch, Item 4.11.1

Figure 7.4: Local Control Switches Drive Local Bits LB1 Through LB16

The output of the local control switch in Figure 7.4 is a Relay Word bit LB_n ($n = 1$ through 16), called a local bit. The local control switch logic in Figure 7.4 repeats for each local bit LB_1 through LB_{16} . Use these local bits in SELOGIC control equations. For a given local control switch, the local control switch positions are enabled by making corresponding label settings.

Table 7.1: Correspondence Between Local Control Switch Positions and Label Settings

Switch Position	Label Setting	Setting Definition	Logic State
not applicable	NLBn	Name of Local Control Switch	not applicable
ON	SLBn	“Set” Local bit LBn	logical 1
OFF	CLBn	“Clear” Local bit LBn	logical 0
MOMENTARY	PLBn	“Pulse” Local bit LBn	logical 1 for one processing interval

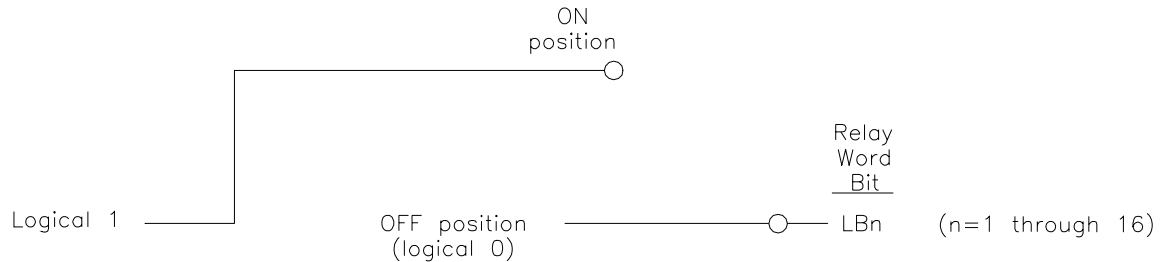
Note the first setting in Table 7.1 (NLBn) is the overall switch name setting. Make each label setting through the serial port using the command **SET T**. View these settings using the serial port command **SHO T** (see *Section 9: Setting the Relay* and *Section 10: Serial Port Communications and Commands*).

Local Control Switch Types

Configure any local control switch as one of the following three switch types:

ON/OFF Switch

Local bit LBn is in either the ON (LBn = logical 1) or OFF (LBn = logical 0) position.



DWG. M351225

Figure 7.5: Local Control Switch Configured as an ON/OFF Switch

OFF/MOMENTARY Switch

The local bit LBn is maintained in the OFF (LBn = logical 0) position and pulses to the MOMENTARY (LBn = logical 1) position for one processing interval (1/4 cycle).

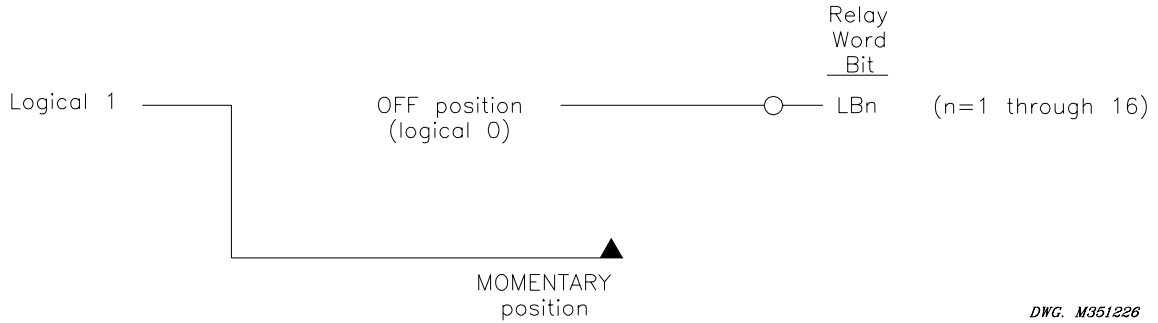


Figure 7.6: Local Control Switch Configured as an OFF/MOMENTARY Switch

ON/OFF/MOMENTARY Switch

The local bit LBn:

is in either the ON (LBn = logical 1) or OFF (LBn = logical 0) position

or

is in the OFF (LBn = logical 0) position and pulses to the MOMENTARY (LBn = logical 1) position for one processing interval (1/4 cycle).

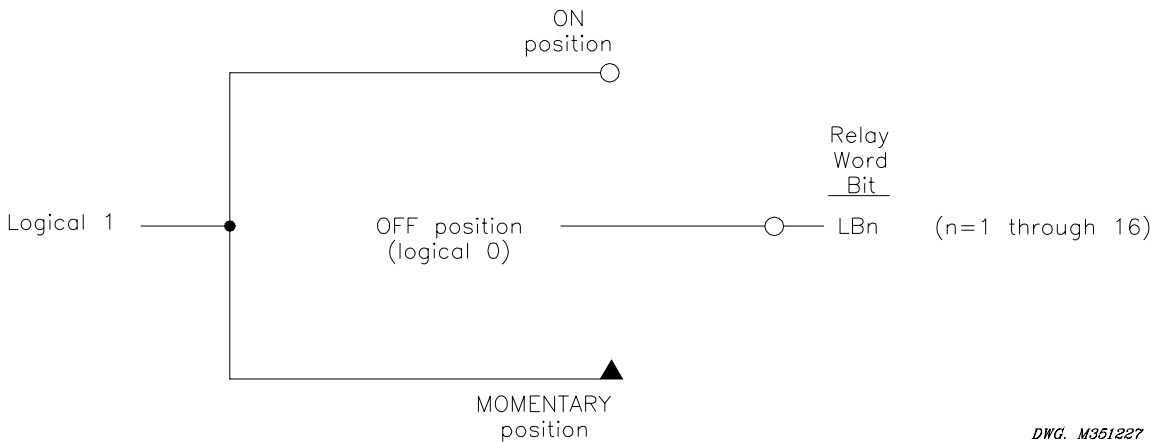


Figure 7.7: Local Control Switch Configured as an ON/OFF/MOMENTARY Switch

Table 7.2: Correspondence Between Local Control Switch Types and Required Label Settings

Local Switch Type	Label NLBn	Label CLBn	Label SLBn	Label PLBn
ON/OFF	X	X	X	
OFF/MOMENTARY	X	X		X
ON/OFF/MOMENTARY	X	X	X	X

Disable local control switches by “nulling out” all the label settings for that switch (see **Section 9: Setting the Relay**). The local bit associated with this disabled local control switch is then fixed at logical 0.

Factory Settings Examples

Local bits LB3 and LB4 are used in a few of the factory SELOGIC control equation settings for manual trip and close functions. Their corresponding local control switch position labels are set to configure the switches as OFF/MOMENTARY switches:

<u>Local Bit</u>	<u>Label Settings</u>	<u>Function</u>
LB3	NLB3 = MANUAL TRIP	trips breaker and drives reclosing relay to lockout
	CLB3 = RETURN	OFF position (“return” from MOMENTARY position)
	SLB3 =	ON position—not used (left “blank”)
	PLB3 = TRIP	MOMENTARY position
LB4	NLB4 = MANUAL CLOSE	closes breaker, separate from automatic reclosing
	CLB4 = RETURN	OFF position (“return” from MOMENTARY position)
	SLB4 =	ON position—not used (left “blank”)
	PLB3 = CLOSE	MOMENTARY position

Following Figure 7.8 and Figure 7.9 show local control switches with factory settings.

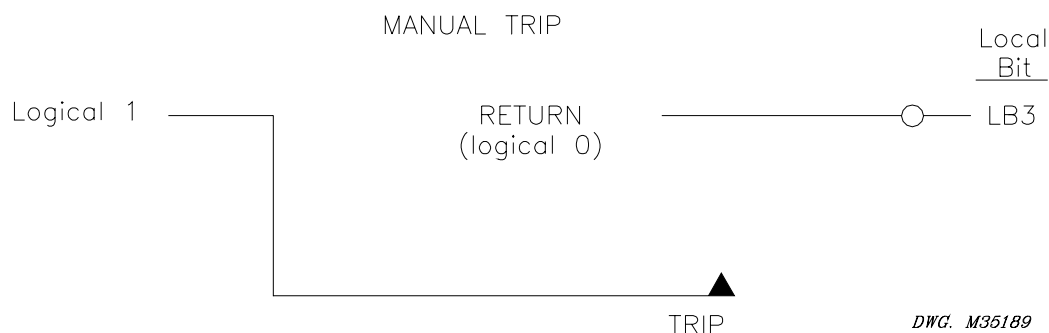


Figure 7.8: Configured Manual Trip Switch Drives Local Bit LB3

Local bit LB3 is set to trip in the following SELOGIC control equation trip setting (see Figure 5.1 in *Section 5: Trip and Target Logic*):

$$TR = \dots + LB3 + \dots$$

To keep reclosing from being initiated for this trip, set local bit LB3 to drive the reclosing relay to lockout for a manual trip (see *Section 6: Close and Reclose Logic*):

$$79DTL = \dots + LB3$$

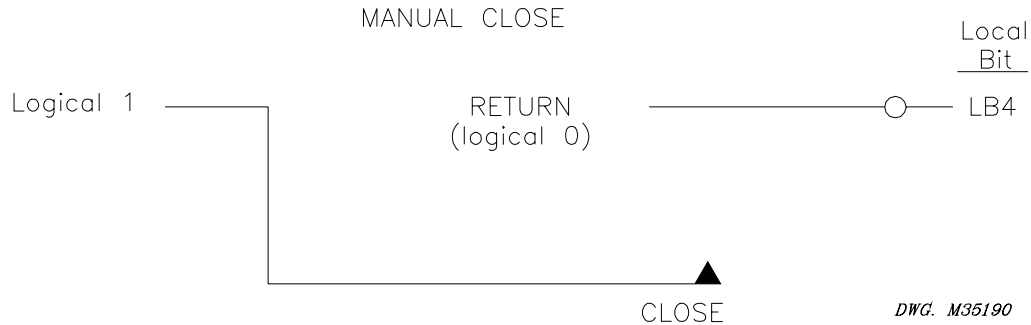


Figure 7.9: Configured Manual Close Switch Drives Local Bit LB4

Local bit LB4 is set to close the circuit breaker in the following SELOGIC control equation setting:

$$CL = LB4$$

SELOGIC control equation setting CL is for close conditions, other than automatic reclosing or serial port CLOSE command (see Figure 6.1 in *Section 6: Close and Reclose Logic*).

Additional Local Control Switch Application Ideas

The preceding factory settings examples are OFF/MOMENTARY switches. Local control switches configured as ON/OFF switches can be used for such applications as:

- Reclosing relay enable/disable
- Ground relay enable/disable
- Remote control supervision
- Sequence coordination enable/disable

Local control switches can also be configured as ON/OFF/MOMENTARY switches for applications that require such. Local control switches can be applied to almost any control scheme that traditionally requires front-panel switches.

Local Control Switch States Retained

Power Loss

The states of the local bits (Relay Word bits LB1 through LB16) are retained if power to the relay is lost and then restored. If a local control switch is in the ON position (corresponding local bit is asserted to logical 1) when power is lost, it comes back in the ON position (corresponding local bit is still asserted to logical 1) when power is restored. If a local control switch is in the OFF position (corresponding local bit is deasserted to logical 0) when power is lost, it comes back in the OFF position (corresponding local bit is still deasserted to logical 0) when power is restored. This feature makes the local bit feature behave the same as a traditional installation with panel-mounted control switches. If power is lost to the panel, the front-panel control switch positions remain unchanged.

Settings Change or Active Setting Group Change

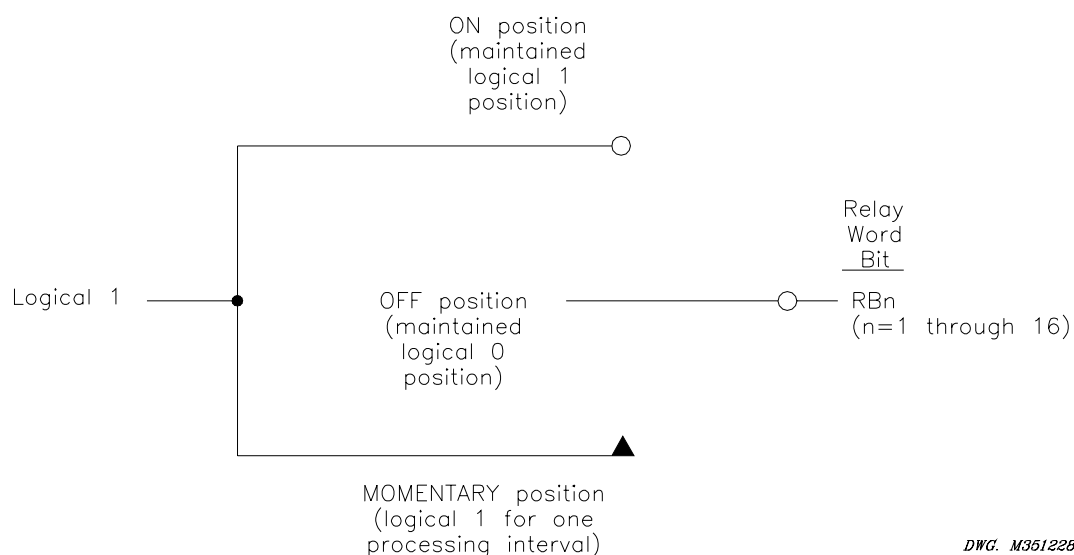
If settings are changed (for the active setting group or one of the other setting groups) or the active setting group is changed, the states of the local bits (Relay Word bits LB1 through LB16) are retained, much like in the preceding *Power Loss* explanation.

If settings are changed for a setting group other than the active setting group, there is no interruption of the local bits (the relay is not momentarily disabled).

If a local control switch is made inoperable because of a settings change (i.e., the corresponding label settings are nulled), the corresponding local bit is then fixed at logical 0, regardless of the local bit state before the settings change. If a local control switch is made newly operable because of a settings change (i.e., the corresponding label settings are set), the corresponding local bit starts out at logical 0.

REMOTE CONTROL SWITCHES

Remote control switches are operated via the serial communications port only (see *CON Command (Control Remote Bit)* in *Section 10: Serial Port Communications and Commands*).



The switch representation in this figure is derived from the standard:
Graphic Symbols for Electrical and Electronics Diagrams
IEEE Std 315-1975, CSA Z99-1975, ANSI Y32.2-1975
4.11 Combination Locking and Nonlocking Switch, Item 4.11.1

Figure 7.10: Remote Control Switches Drive Remote Bits RB1 Through RB16

The outputs of the remote control switches in Figure 7.10 are Relay Word bits RBn (n = 1 to 16), called remote bits. Use these remote bits in SELOGIC control equations.

Any given remote control switch can be put in one of the following three positions:

ON	(logical 1)
OFF	(logical 0)
MOMENTARY	(logical 1 for one processing interval)

Remote Bit Application Ideas

With SELOGIC control equations, the remote bits can be used in applications similar to those that local bits are used in (see preceding local control switch discussion).

Also, remote bits can be used much as optoisolated inputs are used in operating latch control switches (see discussion following Figure 7.15). Pulse (momentarily operate) the remote bits for this application.

Remote Bit States Not Retained When Power is Lost

The states of the remote bits (Relay Word bits RB1 through RB16) are not retained if power to the relay is lost and then restored. The remote control switches always come back in the OFF position (corresponding remote bit is deasserted to logical 0) when power is restored to the relay.

Remote Bit States Retained When Settings Changed or Active Setting Group Changed

The state of each remote bit (Relay Word bits RB1 through RB16) is retained if relay settings are changed (for the active setting group or one of the other setting groups) or the active setting group is changed. If a remote control switch is in the ON position (corresponding remote bit is asserted to logical 1) before a setting change or an active setting group change, it comes back in the ON position (corresponding remote bit is still asserted to logical 1) after the change. If a remote control switch is in the OFF position (corresponding remote bit is deasserted to logical 0) before a settings change or an active setting group change, it comes back in the OFF position (corresponding remote bit is still deasserted to logical 0) after the change.

If settings are changed for a setting group other than the active setting group, there is no interruption of the remote bits (the relay is not momentarily disabled).

Details on the Remote Control Switch MOMENTARY Position

This subsection describes remote control switch 3, which is also called remote bit 3 (RB3). All of the remote bits, RB1–RB16, operate in the same way.

The CON 3 command and PRB 3 subcommand place the remote control switch 3 into the MOMENTARY position for one processing interval, regardless of its initial state. Remote control switch 3 is then placed in the OFF position.

If RB3 is initially at logical 0, pulsing it with the CON 3 command and PRB 3 subcommand will change RB3 to a logical 1 for one processing interval, and then return it to a logical 0. In this situation, the /RB3 (rising edge operator) will also assert for one processing interval, followed by the \RB3 (falling edge operator) one processing interval later.

If RB3 is initially at logical 1 instead, pulsing it with the CON 3 command and PRB 3 subcommand will change RB3 to a logical 0. In this situation, the /RB3 (rising edge operator) will not assert, but the \RB3 (falling edge operator) will assert for one processing interval.

See *CON Command* (Control Remote Bit) in *Section 10: Serial Port Communications and Commands*.

See *Appendix G: Setting SELOGIC Control Equations* for more details on using the rising and falling edge operators in SELOGIC control equations.

LATCH CONTROL SWITCHES

The latch control switch feature of this relay replaces latching relays. Traditional latching relays maintain their output contact state when set. The SEL-351 latch bit retains memory even when control power is lost. If the latch bit is set to a programmable output contact and control power is lost, the state of the latch bit is stored in nonvolatile memory but the output contact will go to its deenergized state. When the control power is applied back to the relay, the programmed output contact will go back to the state of the latch bit.

The state of a traditional latching relay output contact is changed by pulsing the latching relay inputs (see Figure 7.11). Pulse the set input to close (“set”) the latching relay output contact. Pulse the reset input to open (“reset”) the latching relay output contact. Often the external contacts wired to the latching relay inputs are from remote control equipment (e.g., SCADA, RTU).

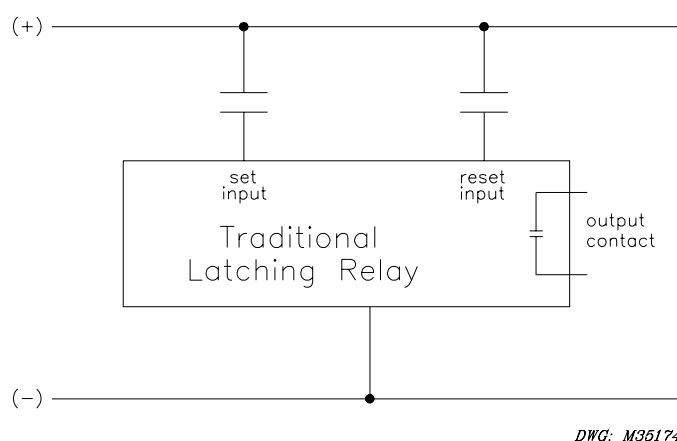


Figure 7.11: Traditional Latching Relay

The sixteen (16) latch control switches in the SEL-351 Relay provide latching relay type functions.

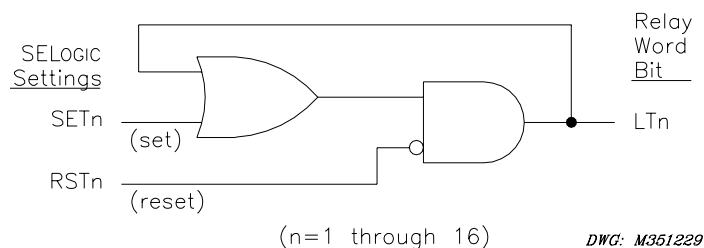


Figure 7.12: Latch Control Switches Drive Latch Bits LT1 Through LT16

The output of the latch control switch in Figure 7.12 is a Relay Word bit LT_n ($n = 1$ through 16), called a latch bit. The latch control switch logic in Figure 7.12 repeats for each latch bit LT1 through LT16. Use these latch bits in SELOGIC control equations.

These latch control switches each have the following SELOGIC control equation settings:

SETn	(set latch bit LT_n to logical 1)
RSTn	(reset latch bit LT_n to logical 0)

If setting SETn asserts to logical 1, latch bit LTn asserts to logical 1. If setting RSTn asserts to logical 1, latch bit LTn deasserts to logical 0. If both settings SETn and RSTn assert to logical 1, setting RSTn has priority and latch bit LTn deasserts to logical 0.

Latch Control Switch Application Ideas

Latch control switches can be used for such applications as:

- Reclosing relay enable/disable
- Ground relay enable/disable
- Sequence coordination enable/disable

Latch control switches can be applied to almost any control scheme. The following is an example of using a latch control switch to enable/disable the reclosing relay in the SEL-351 Relay.

Reclosing Relay Enable/Disable Setting Example

Use a latch control switch to enable/disable the reclosing relay in the SEL-351 Relay. In this example, a SCADA contact is connected to optoisolated input IN104. Each pulse of the SCADA contact changes the state of the reclosing relay. The SCADA contact is not maintained, just pulsed to enable/disable the reclosing relay.

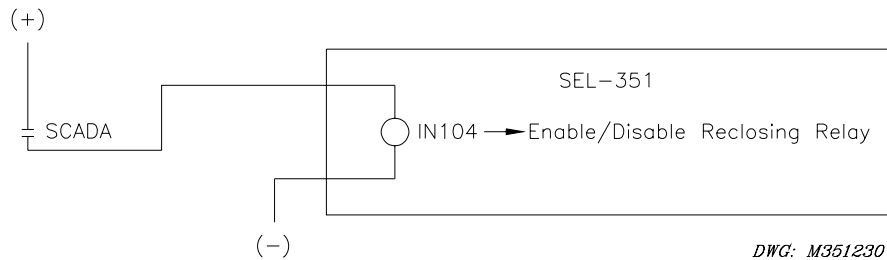


Figure 7.13: SCADA Contact Pulses Input IN104 to Enable/Disable Reclosing Relay

If the reclosing relay is enabled and the SCADA contact is pulsed, the reclosing relay is then disabled. If the SCADA contact is pulsed again, the reclosing relay is enabled again. The control operates in a cyclic manner:

pulse to enable ... pulse to disable ... pulse to enable ... pulse to disable ...

This reclosing relay logic is implemented in the following SELOGIC control equation settings and displayed in Figure 7.14.

SET1 = /IN104*!LT1	[= (rising edge of input IN104) <u>AND</u> NOT(LT1)]
RST1 = /IN104*LT1	[= (rising edge of input IN104) <u>AND</u> LT1]
79DTL = !LT1	[= NOT(LT1); drive-to-lockout setting]

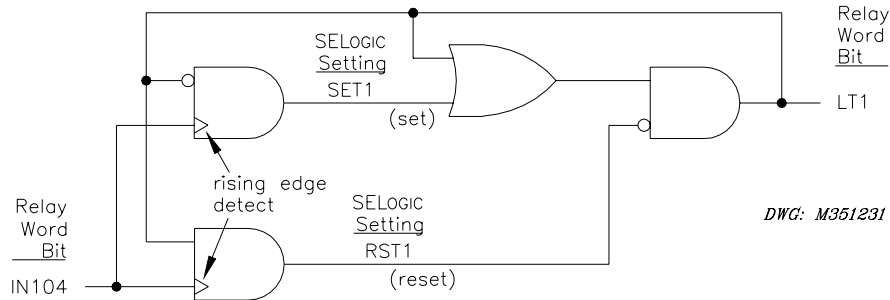


Figure 7.14: Latch Control Switch Controlled by a Single Input to Enable/Disable Reclosing

Feedback Control

Note in Figure 7.14 that the latch control switch output (latch bit LT1) is effectively used as feedback for SELOGIC control equation settings SET1 and RST1. The feedback of latch bit LT1 “guides” input IN104 to the correct latch control switch input.

If latch bit LT1 = logical 0, input IN104 is routed to setting SET1 (set latch bit LT1):

$$\begin{aligned} \text{SET1} &= /\text{IN104} * !\text{LT1} = /\text{IN104} * \text{NOT}(\text{LT1}) = /\text{IN104} * \text{NOT}(\text{logical } 0) \\ &= /\text{IN104} = \text{rising edge of input IN104} \end{aligned}$$

$$\begin{aligned} \text{RST1} &= /\text{IN104} * \text{LT1} = /\text{IN104} * (\text{logical } 0) \\ &= \text{logical } 0 \end{aligned}$$

If latch bit LT1 = logical 1, input IN104 is routed to setting RST1 (reset latch bit LT1):

$$\begin{aligned} \text{SET1} &= /\text{IN104} * !\text{LT1} = /\text{IN104} * \text{NOT}(\text{LT1}) = /\text{IN104} * \text{NOT}(\text{logical } 1) = \\ &= /\text{IN104} * (\text{logical } 0) \\ &= \text{logical } 0 \end{aligned}$$

$$\begin{aligned} \text{RST1} &= /\text{IN104} * \text{LT1} = /\text{IN104} * (\text{logical } 1) \\ &= /\text{IN104} = \text{rising edge of input IN104} \end{aligned}$$

Rising Edge Operators

Refer to Figure 7.14 and Figure 7.15.

The rising edge operator in front of Relay Word bit IN104 ($/\text{IN104}$) sees a logical 0 to logical 1 transition as a “rising edge,” and $/\text{IN104}$ asserts to logical 1 for one processing interval.

The rising edge operator on input IN104 is necessary because any single assertion of optoisolated input IN104 by the SCADA contact will last for at least a few cycles, and each individual assertion of input IN104 should only change the state of the latch control switch once (e.g., latch bit LT1 changes state from logical 0 to logical 1).

For example in Figure 7.14, if:

$$\text{LT1} = \text{logical } 0$$

input IN104 is routed to setting SET1 (as discussed previously):

$SET1 = /IN104 =$ rising edge of input IN104

If input IN104 is then asserted for a few cycles by the SCADA contact (see Pulse 1 in Figure 7.15), SET1 is asserted to logical 1 for one processing interval. This causes latch bit LT1 to change state to:

LT1 = logical 1

the next processing interval.

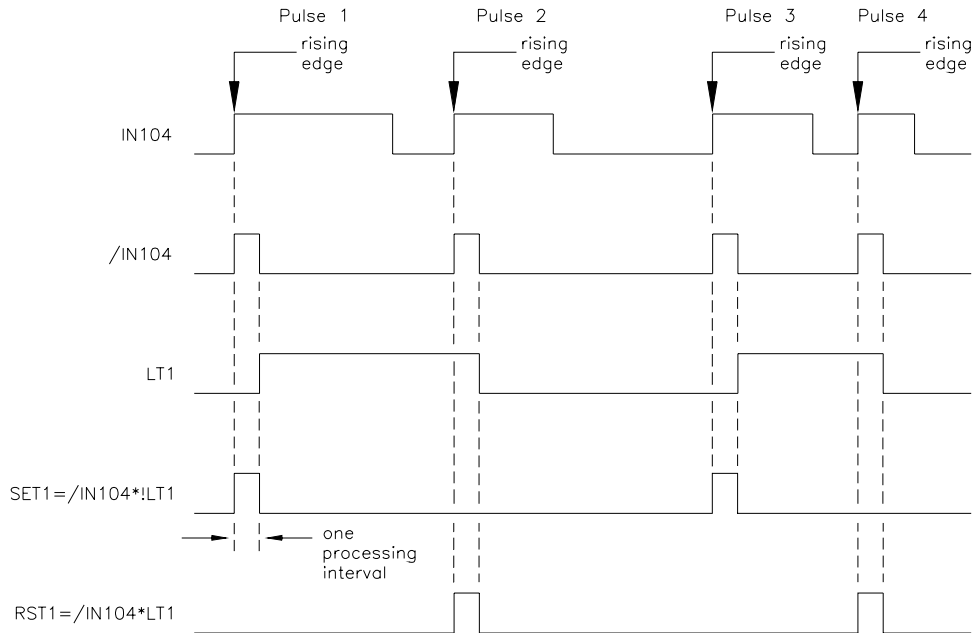
With latch bit LT1 now at logical 1 for the next processing interval, input IN104 is routed to setting RST1 (as discussed previously):

$RST1 = /IN104 =$ rising edge of input IN104

This would then appear to enable the “reset” input (setting RST1) the next processing interval. But the “rising edge” condition occurred the preceding processing interval. /IN104 is now at logical 0, so setting RST1 does not assert, even though input IN104 remains asserted for at least a few cycles by the SCADA contact.

If the SCADA contact deasserts and then asserts again (new rising edge—see Pulse 2 in Figure 7.15), the “reset” input (setting RST1) asserts and latch bit LT1 deasserts back to logical 0 again. Thus, each individual assertion of input IN104 (Pulse 1, Pulse 2, Pulse 3, and Pulse 4 in Figure 7.15) changes the state of latch control switch just once.

Note: Refer to preceding subsection *Optoisolated Inputs* and Figure 7.1. Relay Word bit IN104 shows the state of optoisolated input IN104 after the input pickup/dropout debounce timer IN104D. Thus, when using Relay Word bit IN104 in Figure 7.12 and Figure 7.13 and associated SELOGIC control equations, keep in mind any time delay produced by the input pickup/dropout debounce timer IN104D.



DWG. M351232

Figure 7.15: Latch Control Switch Operation Time Line

Use a Remote Bit Instead to Enable/Disable the Reclosing Relay

Use a remote bit to enable/disable the reclosing relay, instead of an optoisolated input. For example, substitute remote bit RB1 for optoisolated input IN104 in the settings accompanying Figure 7.14:

SET1 = /RB1*!LT1	[= (rising edge of remote bit RB1) <u>AND</u> NOT(LT1)]
RST1 = /RB1*LT1	[= (rising edge of remote bit RB1) <u>AND</u> LT1]
79DTL = !LT1	[= NOT(LT1); drive-to-lockout setting]

Pulse remote bit RB1 to enable reclosing, pulse remote bit RB1 to disable reclosing, etc.—much like the operation of optoisolated input IN104 in the previous example. Remote bits (Relay Word bits RB1 through RB16) are operated through the serial port. See Figure 7.10 and **Section 10: Serial Port Communications and Commands** for more information on remote bits.

These are just a few control logic examples—many variations are possible.

Latch Control Switch States Retained

Power Loss

The states of the latch bits (LT1 through LT16) are retained if power to the relay is lost and then restored. If a latch bit is asserted (e.g., LT2 = logical 1) when power is lost, it comes back asserted (LT2 = logical 1) when power is restored. If a latch bit is deasserted (e.g., LT3 = logical 0) when power is lost, it comes back deasserted (LT3 = logical 0) when power is restored. This feature makes the latch bit feature behave the same as traditional latching relays. In a traditional installation, if power is lost to the panel, the latching relay output contact position remains unchanged.

Note: If a latch bit is set to a programmable output contact (e.g., OUT103 = LT2) and power to the relay is lost, the state of the latch bit is stored in nonvolatile memory but the output contact will go to its deenergized state. When power to the relay is restored, the programmable output contact will go back to the state of the latch bit.

Settings Change or Active Setting Group Change

If individual settings are changed (for the active setting group or one of the other setting groups) or the active setting group is changed, the states of the latch bits (Relay Word bits LT1 through LT16) are retained, much like in the preceding “Power Loss” explanation.

If individual settings are changed for a setting group other than the active setting group, there is no interruption of the latch bits (the relay is not momentarily disabled).

If the individual settings change or active setting group change causes a change in SELOGIC control equation settings SETn or RSTn (n = 1 through 16), the retained states of the latch bits can be changed, subject to the newly enabled settings SETn or RSTn.

Reset Latch Bits for Active Setting Group Change

If desired, the latch bits can be reset to logical 0 right after a settings group change, using SELOGIC control equation setting RSTn (n = 1 through 16). Relay Word bits SG1 through SG6 indicate the active setting Group 1 through 6, respectively (see Table 7.3).

For example, when setting Group 4 becomes the active setting group, latch bit LT2 should be reset. Make the following SELOGIC control equation settings in setting Group 4:

$$SV7 = SG4$$

$$RST2 = !SV7T + \dots \quad [= \text{NOT}(SV7T) + \dots]$$

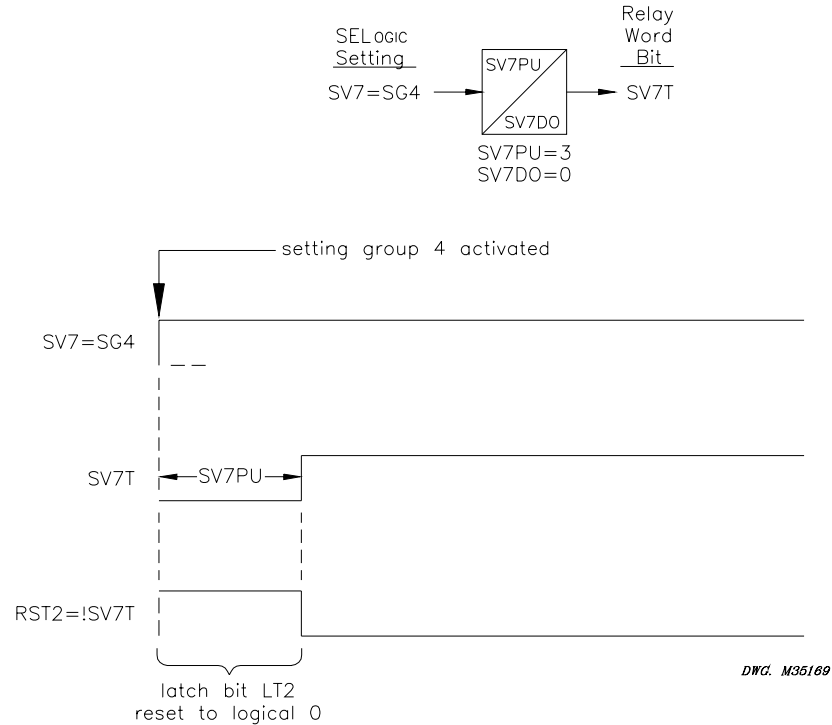


Figure 7.16: Time Line for Reset of Latch Bit LT2 After Active Setting Group Change

In Figure 7.16, latch bit LT2 is reset (deasserted to logical 0) when reset setting RST2 asserts to logical 1 for the short time right after setting Group 4 is activated. This logic can be repeated for other latch bits.

Note: Make Latch Control Switch Settings With Care

The latch bit states are stored in nonvolatile memory so they can be retained during power loss, settings change, or active setting group change. The nonvolatile memory is rated for a finite number of “writes” for all cumulative latch bit state changes. Exceeding the limit can result in an EEPROM self-test failure. An average of 70 cumulative latch bit state changes per day can be made for a 25 year relay service life.

This requires that SELOGIC control equation settings SETn and RSTn for any given latch bit LTn (n = 1 through 16; see Figure 7.12) be set with care. Settings SETn and RSTn cannot result in continuous cyclical operation of latch bit LTn. Use timers to qualify conditions set in settings SETn and RSTn. If any optoisolated inputs IN101 through IN106 are used in settings SETn and RSTn, the inputs have their own debounce timer that can help in providing the necessary time qualification (see Figure 7.1).

In the preceding reclosing relay enable/disable example application (Figure 7.14 and Figure 7.15), the SCADA contact cannot be asserting/deasserting continuously, thus causing latch bit LT1 to change state continuously. Note that the rising edge operators in the SET1 and RST1

settings keep latch bit LT1 from cyclically operating for any single assertion of the SCADA contact.

Another variation to the example application in Figure 7.14 and Figure 7.15 that adds more security is a timer with pickup/dropout times set the same (see Figure 7.17 and Figure 7.18). Suppose that SV6PU and SV6DO are both set to 300 cycles. Then the SV6T timer keeps the state of latch bit LT1 from being able to be changed at a rate faster than once every 300 cycles (5 seconds).

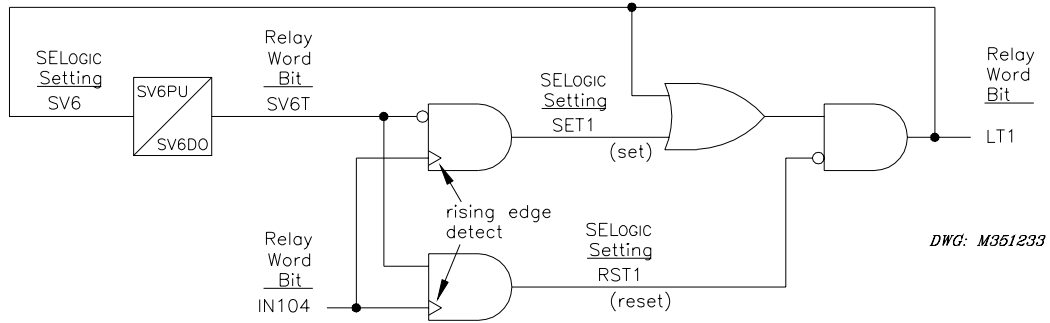


Figure 7.17: Latch Control Switch (With Time Delay Feedback) Controlled by a Single Input to Enable/Disable Reclosing

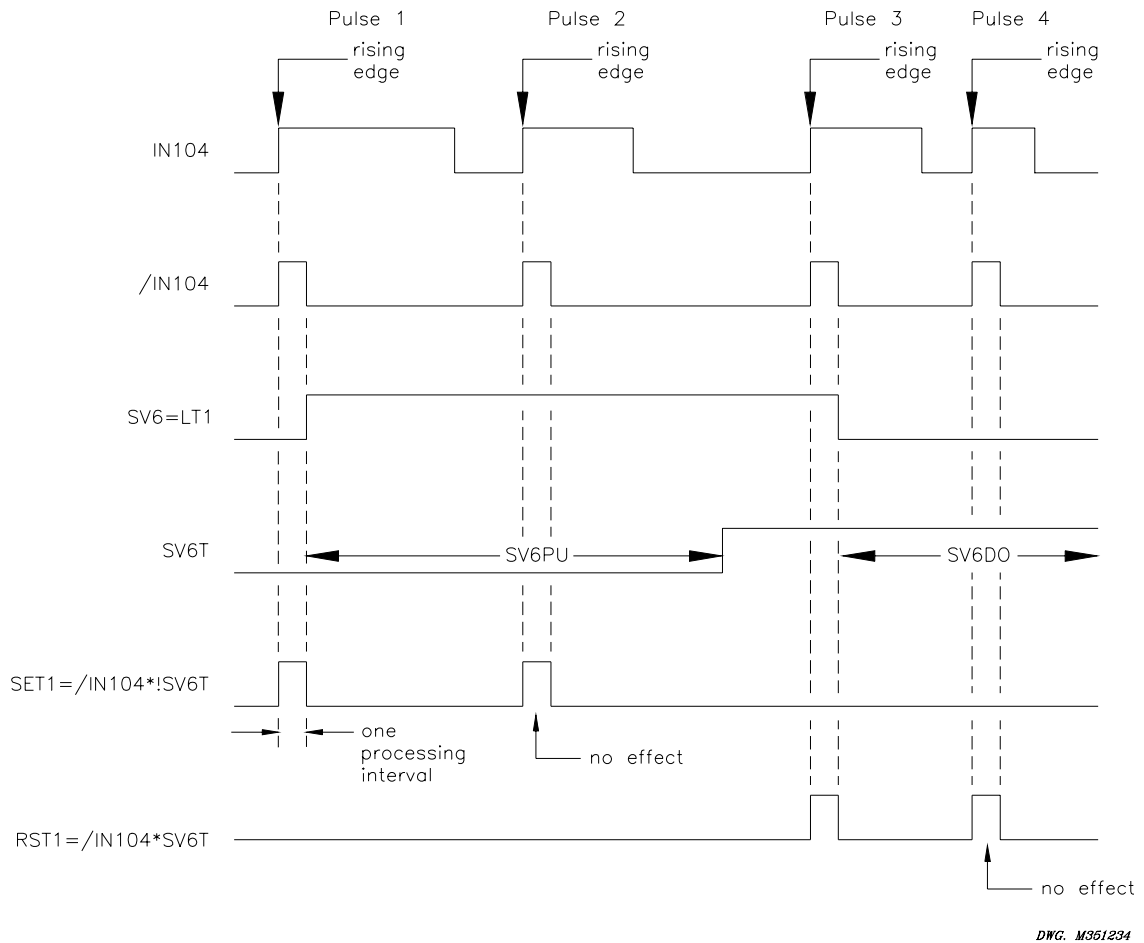


Figure 7.18: Latch Control Switch (With Time Delay Feedback) Operation Time Line

MULTIPLE SETTING GROUPS

The relay has six (6) independent setting groups. Each setting group has complete relay (overcurrent, reclosing, frequency, etc.) and SELOGIC control equation settings.

Active Setting Group Indication

Only one setting group can be active at a time. Relay Word bits SG1 through SG6 indicate the active setting group:

**Table 7.3: Definitions for Active Setting Group Indication
Relay Word Bits SG1 Through SG6**

Relay Word bit	Definition
SG1	Indication that setting Group 1 is the active setting group
SG2	Indication that setting Group 2 is the active setting group
SG3	Indication that setting Group 3 is the active setting group
SG4	Indication that setting Group 4 is the active setting group
SG5	Indication that setting Group 5 is the active setting group
SG6	Indication that setting Group 6 is the active setting group

For example, if setting Group 4 is the active setting group, Relay Word bit SG4 asserts to logical 1, and the other Relay Word bits SG1, SG2, SG3, SG5, and SG6 are all deasserted to logical 0.

Selecting the Active Setting Group

The active setting group is selected with:

- SELOGIC control equation settings SS1 through SS6.
- The serial port GROUP command (see *Section 10: Serial Port Communications and Commands*).
- Or the front-panel GROUP pushbutton (see *Section 11: Front-Panel Interface*).

SELOGIC control equation settings SS1 through SS6 have priority over the serial port GROUP command and the front-panel GROUP pushbutton in selecting the active setting group.

Operation of SELOGIC Control Equation Settings SS1 Through SS6

Each setting group has its own set of SELOGIC control equation settings SS1 through SS6.

**Table 7.4: Definitions for Active Setting Group Switching
SELOGIC Control Equation Settings SS1 Through SS6**

Setting	Definition
SS1	go to (or remain in) setting Group 1
SS2	go to (or remain in) setting Group 2
SS3	go to (or remain in) setting Group 3
SS4	go to (or remain in) setting Group 4
SS5	go to (or remain in) setting Group 5
SS6	go to (or remain in) setting Group 6

The operation of these settings is explained with the following example:

Assume the active setting group starts out as setting Group 3. Corresponding Relay Word bit SG3 is asserted to logical 1 as an indication that setting Group 3 is the active setting group (see Table 7.3).

With setting Group 3 as the active setting group, setting SS3 has priority. If setting SS3 is asserted to logical 1, setting Group 3 remains the active setting group, regardless of the activity of settings SS1, SS2, SS4, SS5, and SS6. With settings SS1 through SS6 all deasserted to logical 0, setting Group 3 still remains the active setting group.

With setting Group 3 as the active setting group, if setting SS3 is deasserted to logical 0 and one of the other settings (e.g., setting SS5) asserts to logical 1, the relay switches from setting Group 3 as the active setting group to another setting group (e.g., setting Group 5) as the active setting group, after qualifying time setting TGR:

TGR Group Change Delay Setting (settable from 0.00 to 16000.00 cycles)

In this example, TGR qualifies the assertion of setting SS5 before it can change the active setting group.

Operation of Serial Port GROUP Command and Front-Panel GROUP Pushbutton

SELOGIC control equation settings SS1 through SS6 have priority over the serial port GROUP command and the front-panel GROUP pushbutton in selecting the active setting group. If any one of SS1 through SS6 asserts to logical 1, neither the serial port GROUP command nor the front-panel GROUP pushbutton can be used to switch the active setting group. But if SS1 through SS6 all deassert to logical 0, the serial port GROUP command or the front-panel GROUP pushbutton can be used to switch the active setting group.

See *Section 10: Serial Port Communications and Commands* for more information on the serial port GROUP command. See *Section 11: Front-Panel Interface* for more information on the front-panel GROUP pushbutton.

Relay Disabled Momentarily During Active Setting Group Change

The relay is disabled for a **few seconds** while the relay is in the process of changing active setting groups. Relay elements, timers, and logic are reset, unless indicated otherwise in specific logic description [e.g., local bit (LB1 through LB16), remote bit (RB1 through RB16), and latch bit (LT1 through LT16) states are retained during a active setting group change]. The output contacts do not change state until the relay enables in the new settings group and the SELOGIC control equations are processed to determine the output contact status for the new group. For instance, if setting OUT105 = logical 1 in Group 2, and setting OUT105 = logical 1 in Group 3, and the relay is switched from Group 2 to Group 3, OUT105 stays energized before, during, and after the group change. However, if the Group 3 setting was OUT105 = logical 0 instead, then OUT105 remains energized until the relay enables in Group 3, solves the SELOGIC control equations, and causes OUT105 to deenergize. See Figure 7.27, and Figure 7.28 for examples of output contacts in the deenergized state (i.e., corresponding output contact coils deenergized).

Active Setting Group Switching Example 1

Use a single optoisolated input to switch between two setting groups in the SEL-351 Relay. In this example, optoisolated input IN105 on the relay is connected to a SCADA contact in Figure 7.19. Each pulse of the SCADA contact changes the active setting group from one setting group (e.g., setting Group 1) to another (e.g., setting Group 4). The SCADA contact is not maintained, just pulsed to switch from one active setting group to another.

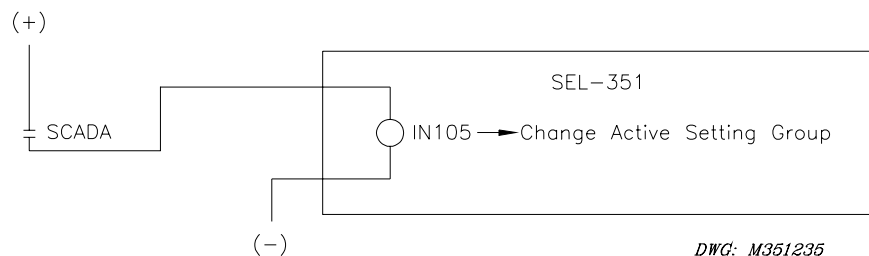


Figure 7.19: SCADA Contact Pulses Input IN105 to Switch Active Setting Group Between Setting Groups 1 and 4

If setting Group 1 is the active setting group and the SCADA contact is pulsed, setting Group 4 becomes the active setting group. If the SCADA contact is pulsed again, setting Group 1 becomes the active setting group again. The setting group control operates in a cyclical manner:

pulse to activate setting Group 4 ... pulse to activate setting Group 1 ... pulse to activate setting Group 4 ... pulse to activate setting Group 1 ...

This logic is implemented in the SELOGIC control equation settings in Table 7.5.

Table 7.5: SELOGIC Control Equation Settings for Switching Active Setting Group Between Setting Groups 1 and 4

Setting Group 1	Setting Group 4
SV8 = SG1	SV8 = SG4
SS1 = 0	SS1 = IN105*SV8T
SS2 = 0	SS2 = 0
SS3 = 0	SS3 = 0
SS4 = IN105*SV8T	SS4 = 0
SS5 = 0	SS5 = 0
SS6 = 0	SS6 = 0

SELOGIC control equation timer input setting SV8 in Table 7.5 has logic output SV8T, shown in operation in Figure 7.20 for both setting Groups 1 and 4.

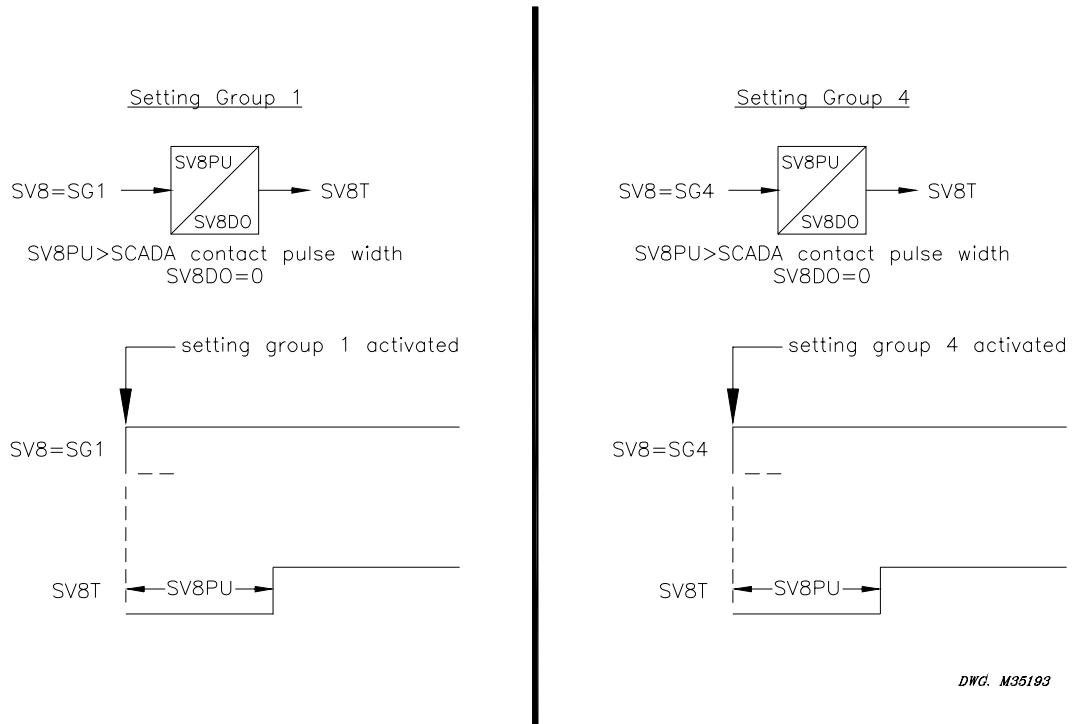


Figure 7.20: SELOGIC Control Equation Variable Timer SV8T Used in Setting Group Switching

In this example, timer SV8T is used in both setting groups—different timers could have been used with the same operational result. The timers reset during the setting group change, allowing the same timer to be used in both setting groups.

Timer pickup setting SV8PU is set greater than the pulse width of the SCADA contact (Figure 7.19). This allows only one active setting group change (e.g., from setting Group 1 to 4)

for each pulse of the SCADA contact (and subsequent assertion of input IN105). The function of the SELOGIC control equations in Table 7.5 becomes more apparent in the following example scenario.

Start Out in Setting Group 1

Refer to Figure 7.21.

The relay has been in setting Group 1 for some time, with timer logic output SV8T asserted to logical 1, thus enabling SELOGIC control equation setting SS4 for the assertion of input IN105.

Switch to Setting Group 4

Refer to Figure 7.21.

The SCADA contact pulses input IN105, and the active setting group changes to setting Group 4 after qualifying time setting TGR (perhaps set at a cycle or so to qualify the assertion of setting SS4). Optoisolated input IN105 also has its own built-in debounce timer (IN105D) available (see Figure 7.1).

Note that Figure 7.21 shows both setting Group 1 and setting Group 4 settings. The setting Group 1 settings (top of Figure 7.21) are enabled only when setting Group 1 is the active setting group and likewise for the setting Group 4 settings at the bottom of the figure.

Setting Group 4 is now the active setting group, and Relay Word bit SG4 asserts to logical 1. After the relay has been in setting Group 4 for a time period equal to SV8PU, the timer logic output SV8T asserts to logical 1, thus enabling SELOGIC control equation setting SS1 for a new assertion of input IN105.

Note that input IN105 is still asserted as setting Group 4 is activated. Pickup time SV8PU keeps the continued assertion of input IN105 from causing the active setting group to revert back again to setting Group 1 for a single assertion of input IN105. This keeps the active setting group from being changed at a time interval less than time SV8PU.

Switch Back to Setting Group 1

Refer to Figure 7.21.

The SCADA contact pulses input IN105 a second time, and the active setting group changes back to setting Group 1 after qualifying time setting TGR (perhaps set at a cycle or so to qualify the assertion of setting SS1). Optoisolated input IN105 also has its own built-in debounce timer (IN105D) available (see Figure 7.1).

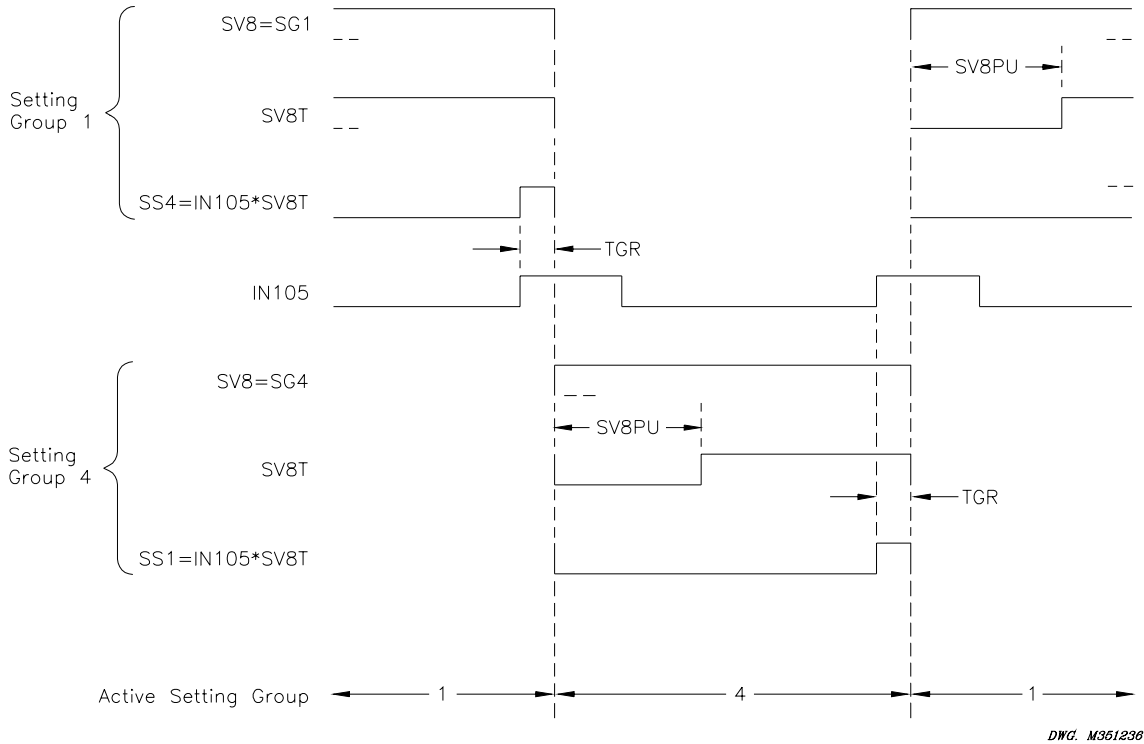


Figure 7.21: Active Setting Group Switching (With Single Input) Time Line

Active Setting Group Switching Example 2

Previous SEL relays (e.g., SEL-321 and SEL-251 Relays) have multiple settings groups controlled by the assertion of three optoisolated inputs (e.g., IN101, IN102, and IN103) in different combinations as shown in Table 7.6.

Table 7.6: Active Setting Group Switching Input Logic

Input States			Active
IN103	IN102	IN101	Setting Group
0	0	0	Remote
0	0	1	Group 1
0	1	0	Group 2
0	1	1	Group 3
1	0	0	Group 4
1	0	1	Group 5
1	1	0	Group 6

The SEL-351 Relay can be programmed to operate similarly. Use three optoisolated inputs to switch between the six setting groups in the SEL-351 Relay. In this example, optoisolated inputs IN101, IN102, and IN103 on the relay are connected to a rotating selector switch in Figure 7.22.

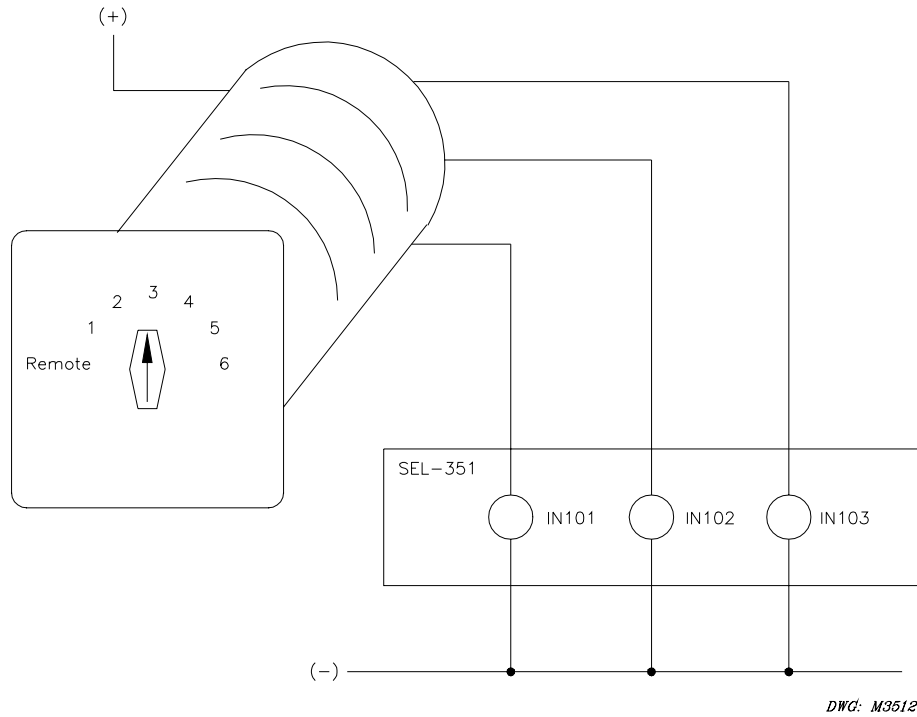


Figure 7.22: Rotating Selector Switch Connected to Inputs IN101, IN102, and IN103 for Active Setting Group Switching

The selector switch has multiple internal contacts arranged to assert inputs IN101, IN102, and IN103, dependent on the switch position. As shown in Table 7.7, the selector switch is moved from one position to another, a different setting group is activated. The logic in Table 7.6 is implemented in the SELOGIC control equation settings in Table 7.7.

Table 7.7: SELOGIC Control Equation Settings for Rotating Selector Switch Active Setting Group Switching

SS1 = !IN103 * !IN102 * IN101	= NOT(IN103) * NOT(IN102) * IN101
SS2 = !IN103 * IN102 * !IN101	= NOT(IN103) * IN102 * NOT(IN101)
SS3 = !IN103 * IN102 * IN101	= NOT(IN103) * IN102 * IN101
SS4 = IN103 * !IN102 * !IN101	= IN103 * NOT(IN102) * NOT(IN101)
SS5 = IN103 * !IN102 * IN101	= IN103 * NOT(IN102) * IN101
SS6 = IN103 * IN102 * !IN101	= IN103 * IN102 * NOT(IN101)

The settings in Table 7.7 are made in each setting Group 1 through 6.

Selector Switch Starts Out in Position 3

Refer to Table 7.7 and Figure 7.23.

If the selector switch is in position 3 in Figure 7.22, setting Group 3 is the active setting group (Relay Word bit SG3 = logical 1). Inputs IN101 and IN102 are energized and IN103 is deenergized:

$$\begin{aligned}SS3 &= !IN103 * IN102 * IN101 = \text{NOT}(IN103) * IN102 * IN101 \\ &= \text{NOT}(\text{logical } 0) * \text{logical } 1 * \text{logical } 1 = \text{logical } 1\end{aligned}$$

To get from the position 3 to position 5 on the selector switch, the switch passes through the position 4. The switch is only briefly in position 4:

$$\begin{aligned}SS4 &= IN103 * !IN102 * !IN101 = IN103 * \text{NOT}(IN102) * \text{NOT}(IN101) \\ &= \text{logical } 1 * \text{NOT}(\text{logical } 0) * \text{NOT}(\text{logical } 0) = \text{logical } 1\end{aligned}$$

but not long enough to be qualified by time setting TGR in order to change the active setting group to setting Group 4. For such a rotating selector switch application, qualifying time setting TGR is typically set at 180 to 300 cycles. Set TGR long enough to allow the selector switch to pass through intermediate positions without changing the active setting group, until the switch rests on the desired setting group position.

Selector Switch Switched to Position 5

Refer to Figure 7.23.

If the selector switch is rested on position 5 in Figure 7.22, setting Group 5 becomes the active setting group (after qualifying time setting TGR; Relay Word bit SG5 = logical 1). Inputs IN101 and IN103 are energized and IN102 is deenergized:

$$\begin{aligned}SS5 &= IN103 * !IN102 * IN101 = IN103 * \text{NOT}(IN102) * IN101 \\ &= \text{logical } 1 * \text{NOT}(\text{logical } 0) * \text{logical } 1 = \text{logical } 1\end{aligned}$$

To get from position 5 to position REMOTE on the selector switch, the switch passes through the positions 4, 3, 2, and 1. The switch is only briefly in these positions, but not long enough to be qualified by time setting TGR in order to change the active setting group to any one of these setting groups.

Selector Switch Now Rests on Position REMOTE

Refer to Figure 7.23.

If the selector switch is rested on position REMOTE in Figure 7.20, all inputs IN101, IN102, and IN103 are deenergized and all settings SS1 through SS6 in Table 7.7 are at logical 0. The last active setting group (Group 5 in this example) remains the active setting group (Relay Word bit SG5 = logical 1).

With settings SS1 through SS6 all at logical 0, the serial port GROUP command or the front-panel GROUP pushbutton can be used to switch the active setting group from Group 5, in this example, to another desired setting group.

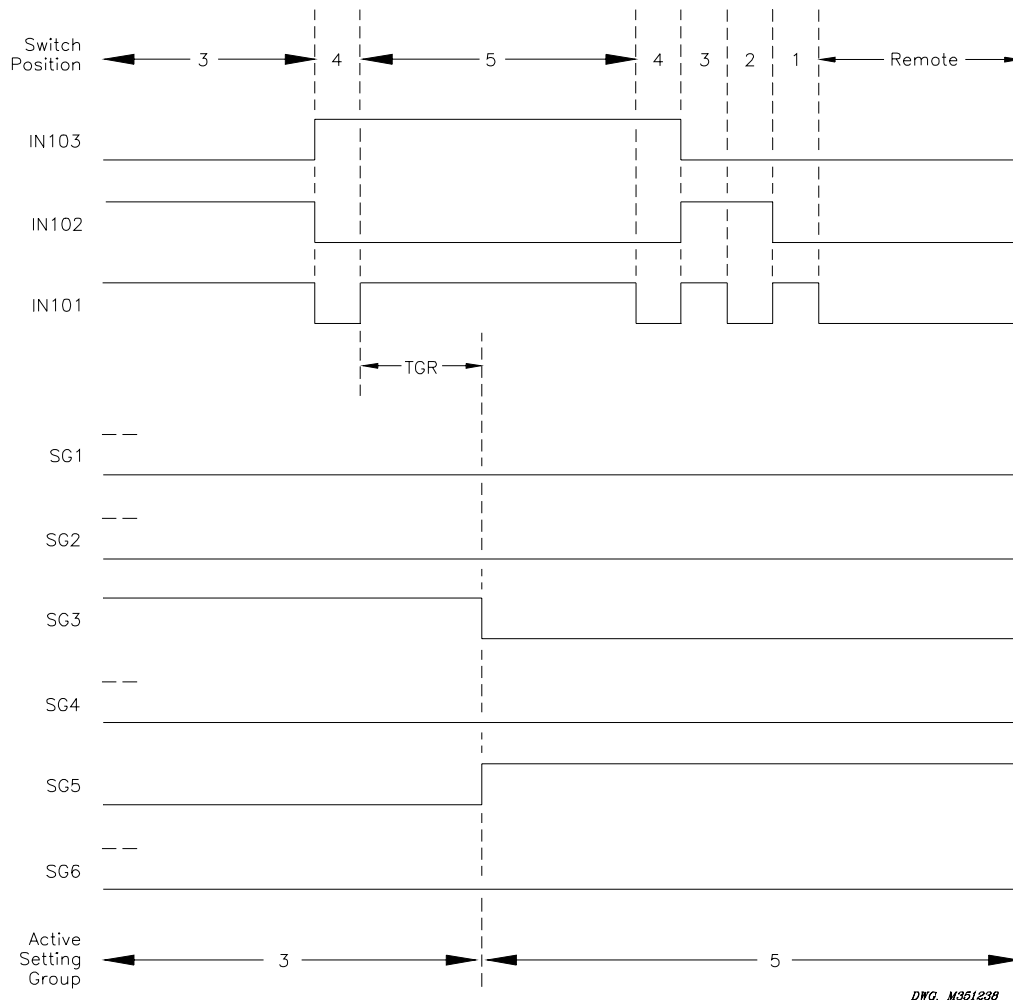


Figure 7.23: Active Setting Group Switching (With Rotating Selector Switch) Time Line

Active Setting Group Retained

Power Loss

The active setting group is retained if power to the relay is lost and then restored. If a particular setting group is active (e.g., setting Group 5) when power is lost, it comes back with the same setting group active when power is restored.

Settings Change

If individual settings are changed (for the active setting group or one of the other setting groups), the active setting group is retained, much like in the preceding **Power Loss** explanation.

If individual settings are changed for a setting group other than the active setting group, there is no interruption of the active setting group (the relay is not momentarily disabled).

If the individual settings change causes a change in one or more SELOGIC control equation settings SS1 through SS6, the active setting group can be changed, subject to the newly enabled SS1 through SS6 settings.

Note: Make Active Setting Group Switching Settings with Care

The active setting group is stored in nonvolatile memory so it can be retained during power loss or settings change. The nonvolatile memory is rated for a finite number of “writes” for all setting group changes. Exceeding the limit can result in an EEPROM self-test failure. An average of one (1) setting group change per day can be made for a 25 year relay service life.

This requires that SELOGIC control equation settings SS1 through SS6 (see Table 7.4) be set with care. Settings SS1 through SS6 cannot result in continuous cyclical changing of the active setting group. Time setting TGR qualifies settings SS1 through SS6 before changing the active setting group. If optoisolated inputs IN101 through IN106 are used in settings SS1 through SS6, the inputs have their own built-in debounce timer that can help in providing the necessary time qualification (see Figure 7.1).

SELOGIC CONTROL EQUATION VARIABLES/TIMERS

Sixteen (16) SELOGIC control equation variables/timers are available. Each SELOGIC control equation variable/timer has a SELOGIC control equation setting input and variable/timer outputs as shown in Figure 7.24 and Figure 7.25.

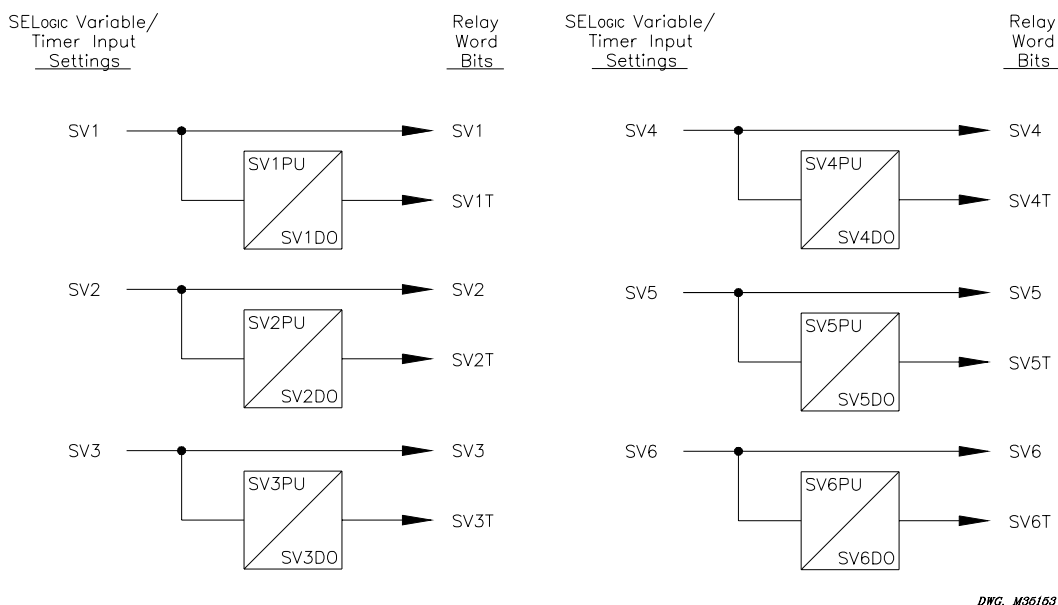
Timers SV1T through SV6T in Figure 7.24 have a setting range of a little over 4.5 hours:

0.00–999999.00 cycles in 0.25-cycle increments

Timers SV7T through SV16T in Figure 7.25 have a setting range of almost 4.5 minutes:

0.00–16000.00 cycles in 0.25-cycle increments

These timer setting ranges apply to both pickup and dropout times (SVnPU and SVnDO, n = 1 through 16).



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Figure 7.24: SELOGIC Control Equation Variables/Timers SV1/SV1T Through SV6/SV6T

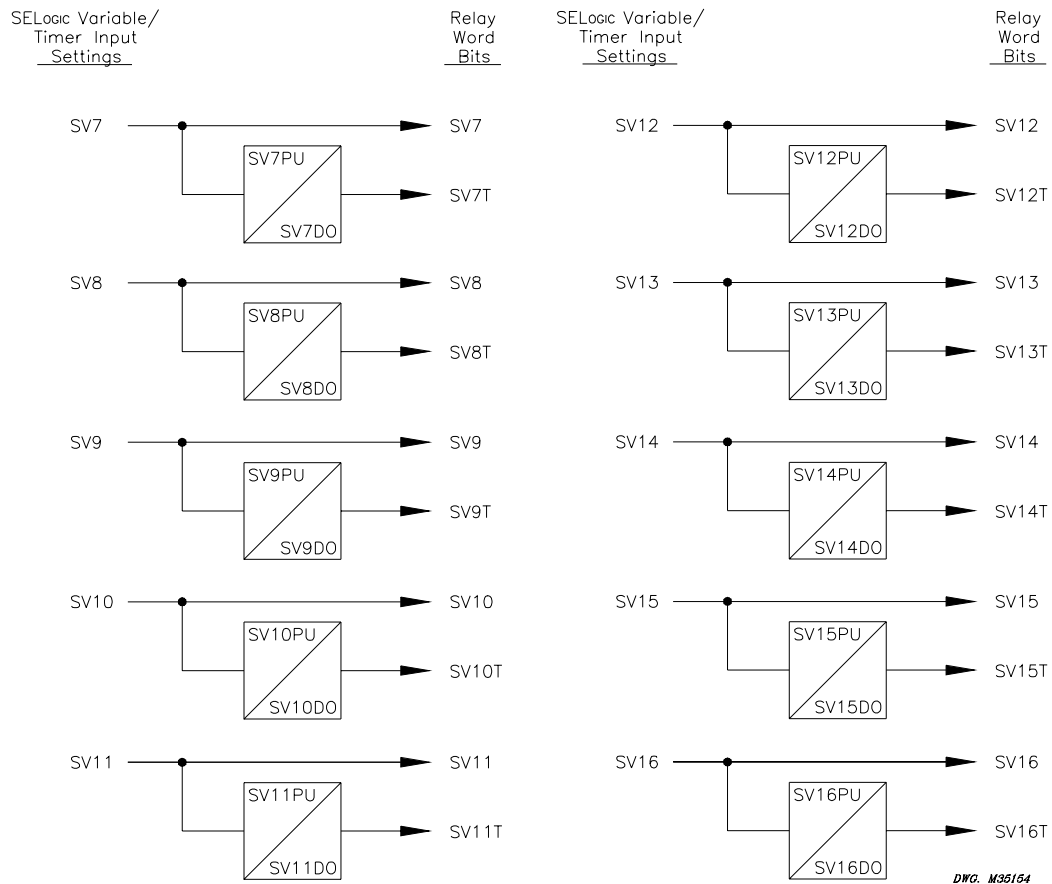


Figure 7.25: SELOGIC Control Equation Variables/Timers SV7/SV7T Through SV16/SV16T

Factory Settings Example

In the factory SELOGIC control equation settings, a SELOGIC control equation timer is used for a simple breaker failure scheme:

$$SV1 = \text{TRIP}$$

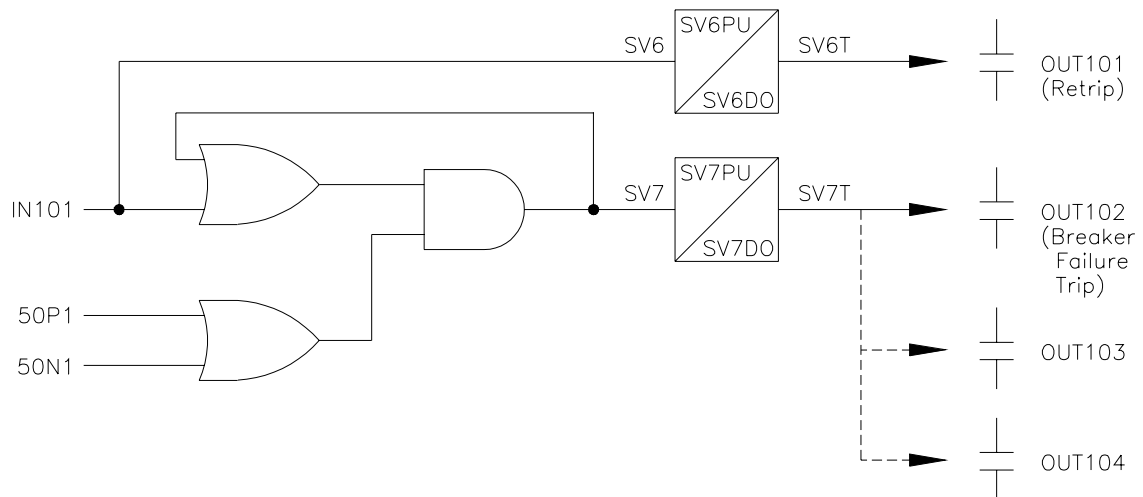
The TRIP Relay Word bit is run through a timer for breaker failure timing. Timer pickup setting SV1PU is set to the breaker failure time (SV1PU = 12 cycles). Timer dropout setting SV1DO is set for a 2-cycle dropout (SV1DO = 2 cycles). The output of the timer (Relay Word bit SV1T) operates output contact OUT103.

$$\text{OUT103} = \text{SV1T}$$

Additional Settings Example 1

Another application idea is dedicated breaker failure protection (see Figure 7.26):

SV6 = IN101 (breaker failure initiate)
 SV7 = (SV7 + IN101)*(50P1 + 50N1)
 OUT101 = SV6T (retrip)
 OUT102 = SV7T (breaker failure trip)



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Figure 7.26: Dedicated Breaker Failure Scheme Created With SELOGIC Control Equation Variables/Timers

Note that the above SELOGIC control equation setting SV7 creates a seal-in logic circuit (as shown in Figure 7.26) by virtue of SELOGIC control equation setting SV7 being set equal to Relay Word bit SV7 (SELOGIC control equation variable SV7):

$$SV7 = \underset{\uparrow}{(SV7 + IN101)} * (50P1 + 50N1)$$

Optoisolated input IN101 functions as a breaker failure initiate input. Phase instantaneous overcurrent element 50P1 and neutral ground instantaneous overcurrent element 50N1 function as fault detectors.

Timer pickup setting SV6PU provides retrip delay, if desired (can be set to zero). Timer dropout setting SV6DO holds the retrip output (output contact OUT101) closed for extra time if needed after the breaker failure initiate signal (IN101) goes away.

Timer pickup setting SV7PU provides breaker failure timing. Timer dropout setting SV7DO holds the breaker failure trip output (output contact OUT102) closed for extra time if needed after the breaker failure logic unlatches (fault detectors 50P1 and 50N1 dropout).

Note that Figure 7.26 suggests the option of having output contacts OUT103 and OUT104 operate as additional breaker failure trip outputs. This is done by making the following SELOGIC control equation settings:

OUT103 = SV7T (breaker failure trip)
 OUT104 = SV7T (breaker failure trip)

Additional Settings Example 2

The seal-in logic circuit in the dedicated breaker failure scheme in Figure 7.26 can be removed by changing the SELOGIC control equation setting SV7 to:

$$SV7 = IN101*(50P1 + 50N1)$$

If the seal-in logic circuit is removed, optoisolated input IN101 (breaker failure initiate) has to be continually asserted for a breaker failure time-out.

Timers Reset When Power is Lost, Settings are Changed, or Active Setting Group is Changed

If power is lost to the relay, settings are changed (for the active setting group), or the active setting group is changed, the SELOGIC control equation variables/timers are reset. Relay Word bits SVn and SVnT (n = 1 through 16) are reset to logical 0 and corresponding timer settings SVnPU and SVnDO load up again after power restoration, settings change, or active setting group switch.

Preceding Figure 7.26 shows an effective seal-in logic circuit, created by use of Relay Word bit SV7 (SELOGIC control equation variable SV7) in SELOGIC control equation SV7:

$$SV7 = \underbrace{(SV7 + IN101)}_{\uparrow \quad \uparrow}*(50P1 + 50N1)$$

If power is lost to the relay, settings are changed (for the active setting group), or the active setting group is changed, the seal-in logic circuit is “broken” by virtue of Relay Word bit SV7 being reset to logical 0 (assuming input IN101 is not asserted). Relay Word bit SV7T is also reset to logical 0, and timer settings SV7PU and SV7DO load up again.

OUTPUT CONTACTS

Figure 7.27 and Figure 7.28 show the example operation of output contact Relay Word bits (e.g., Relay Word bits OUT101 through OUT107 in Figure 7.27) due to:

SELOGIC control equation operation (e.g., SELOGIC control equation settings OUT101 through OUT107 in Figure 7.27)

or

PULSE command execution

The output contact Relay Word bits in turn control the output contacts (e.g., output contacts OUT101 through OUT107 in Figure 7.27).

Alarm logic/circuitry controls the ALARM output contact (see Figure 7.27)

Figure 7.27 is used for following discussion/examples. The output contacts in Figure 7.28 operate similarly.

Factory Settings Example

In the factory SELOGIC control equation settings, three output contacts are used:

OUT101 = TRIP	(overcurrent tripping/manual tripping; see <i>Section 5: Trip and Target Logic</i>)
OUT102 = CLOSE	(automatic reclosing/manual closing; see <i>Section 6: Close and Reclose Logic</i>)
OUT103 = SV1T	(breaker failure trip; see <i>SELOGIC Control Equation Variables/Timers</i> earlier in this section)
OUT104 = 0	(output contact OUT104 not used—set equal to zero)
•	
•	
•	
OUT107 = 0	(output contact OUT107 not used—set equal to zero)

Operation of Output Contacts for Different Output Contact Types

Output Contacts OUT101 Through OUT107

Refer to Figure 7.27.

The execution of the serial port command PULSE n (n = OUT101 through OUT107) asserts the corresponding Relay Word bit (OUT101 through OUT107) to logical 1. The assertion of SELOGIC control equation setting OUTm (m = 101 through 107) to logical 1 also asserts the corresponding Relay Word bit OUTm (m = 101 through 107) to logical 1.

The assertion of Relay Word bit OUTm (m = 101 through 107) to logical 1 causes the energization of the corresponding output contact OUTm coil. Depending on the contact type (a or b), the output contact closes or opens as demonstrated in Figure 7.27. An “a” type output contact is open when the output contact coil is deenergized and closed when the output contact coil is energized. A “b” type output contact is closed when the output contact coil is deenergized and open when the output contact coil is energized.

Notice in Figure 7.27 that all four possible combinations of output contact coil states (energized or deenergized) and output contact types (a or b) are demonstrated. See *Output Contact Jumpers* in *Section 2: Installation* for output contact type options.

Output contact pickup/dropout time is 4 ms.

ALARM Output Contact

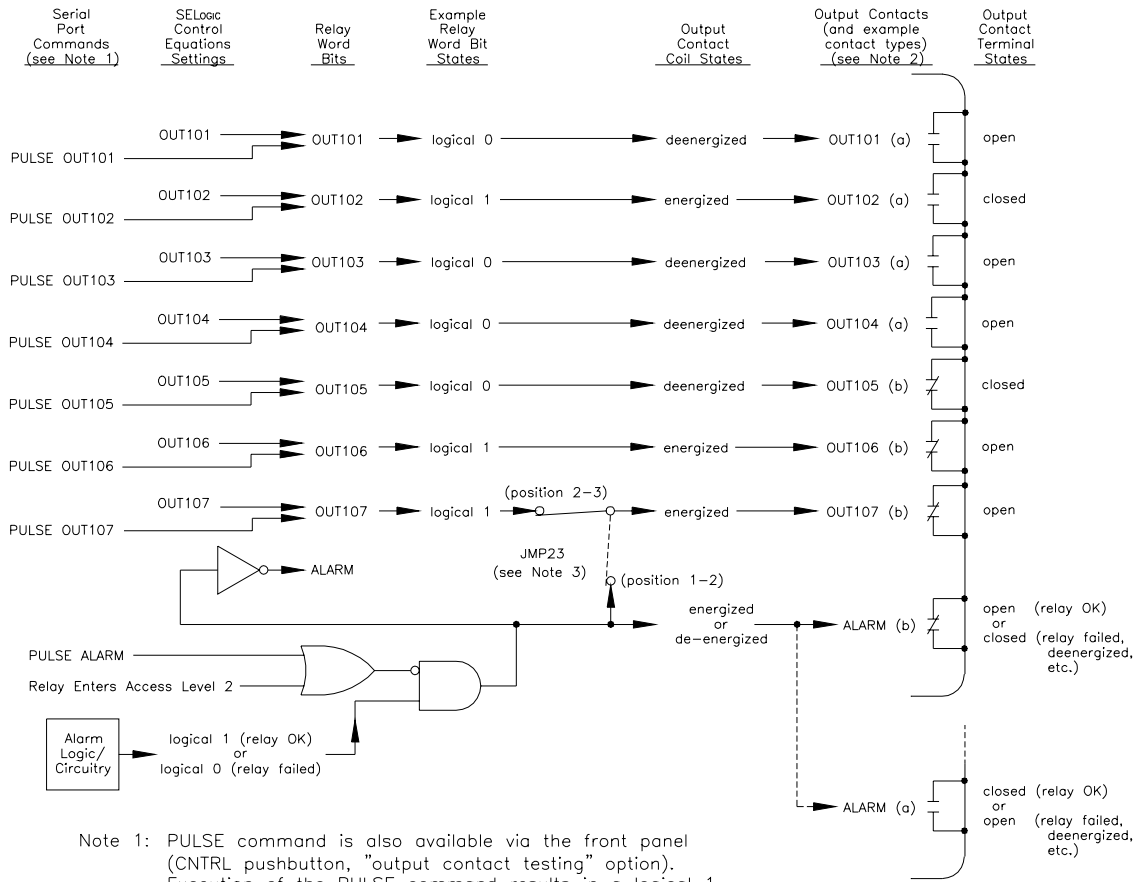
Refer to Figure 7.27 and *Relay Self-Tests* in *Section 13: Testing and Troubleshooting*.

When the relay is operational, the ALARM output contact coil is energized. The alarm logic/circuitry keeps the ALARM output contact coil energized. Depending on the ALARM output contact type (a or b), the ALARM output contact closes or opens as demonstrated in Figure 7.27. An “a” type output contact is open when the output contact coil is deenergized and closed when the output contact coil is energized. A “b” type output contact is closed when the output contact coil is deenergized and open when the output contact coil is energized.

To verify ALARM output contact mechanical integrity, execute the serial port command PULSE ALARM. Execution of this command momentarily deenergizes the ALARM output contact coil.

The Relay Word bit ALARM is deasserted to logical 0 when the relay is operational. When the serial port command PULSE ALARM is executed, the ALARM Relay Word bit momentarily asserts to logical 1. Also, when the relay enters Access Level 2, the ALARM Relay Word bit momentarily asserts to logical 1 (and the ALARM output contact coil is deenergized momentarily).

Notice in Figure 7.27 that all possible combinations of ALARM output contact coil states (energized or deenergized) and output contact types (a or b) are demonstrated. See **Output Contact Jumpers in Section 2: Installation** for output contact type options.



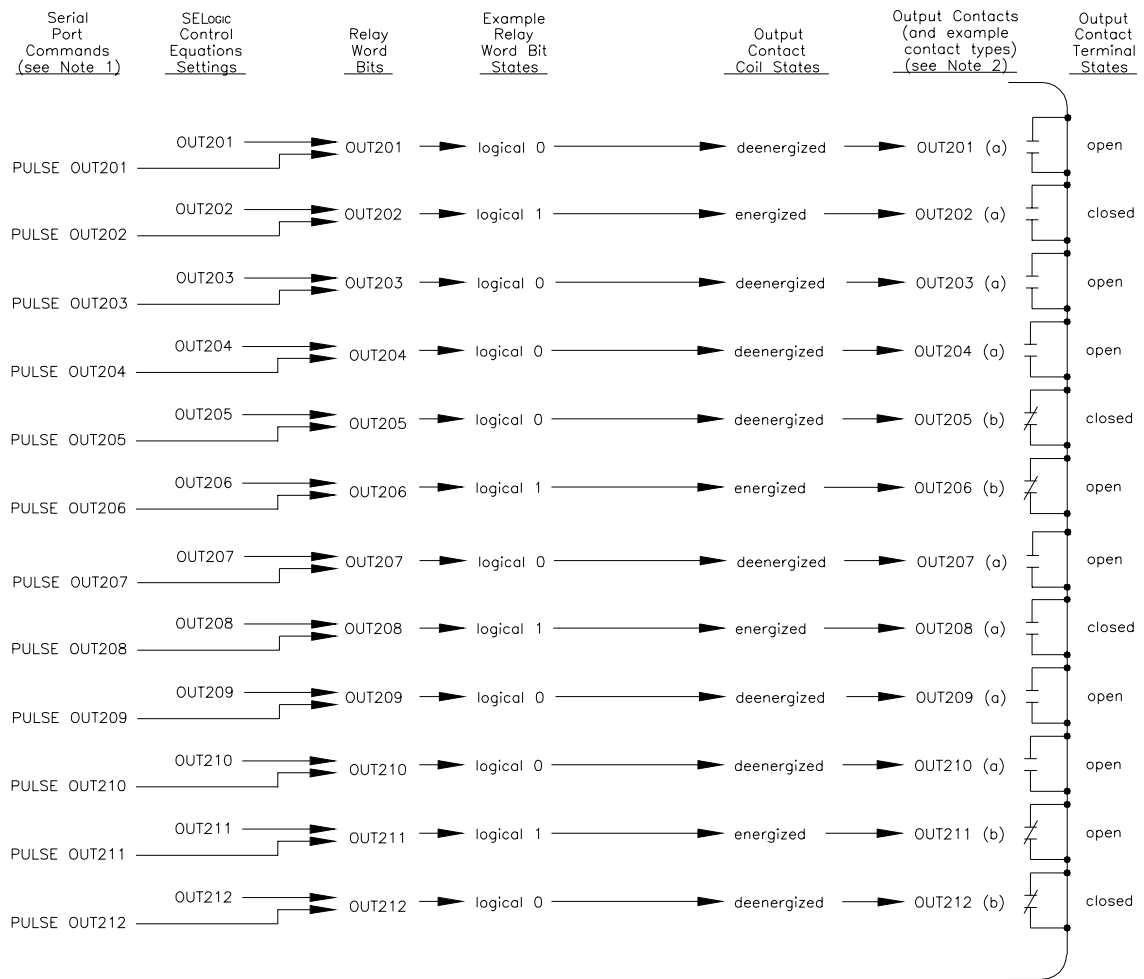
Note 1: PULSE command is also available via the front panel (CNTRL pushbutton, "output contact testing" option). Execution of the PULSE command results in a logical 1 input into the above logic (1-second default pulse width).

Note 2: Output contacts OUT101 through ALARM are configurable as "a" or "b" type output contacts. See Table 2.1 and accompanying text in Section 2: Additional Installation Details for more information on selecting output contact type.

Note 3: Main board jumper JMP23 allows output contact OUT107 to operate as:
 - regular output contact OUT107 (JMP23 in position 2-3)
 - an extra Alarm output contact (JMP23 in position 1-2)
 See Table 2.3 in Section 2: Additional Installation Details for more information on jumper JMP23.

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Figure 7.27: Logic Flow for Example Output Contact Operation (Models 0351x0, 0351x1, and 0351xY)



Note 1: PULSE command is also available via the front panel (CNTRL pushbutton, "output contact testing" option). Execution of the PULSE command results in a logical 1 input into the above logic (1-second default pulse width).

Note 2: Output contacts OUT209 through OUT212 are configurable as "a" or "b" type output contacts on plug-in connector versions. All 12 outputs are configurable on screw-terminal block versions. See Figures 2.17 and 2.18 in Section 2: Installation for more information on selecting output contact type.

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Figure 7.28: Logic Flow for Example Output Contact Operation—Extra I/O Board (Model 0351x1 and 0351xY)

ROTATING DEFAULT DISPLAY

The rotating default display on the relay front-panel replaces indicating panel lights. Traditional indicating panel lights are turned on and off by circuit breaker auxiliary contacts, front-panel switches, SCADA contacts, etc. They indicate such conditions as:

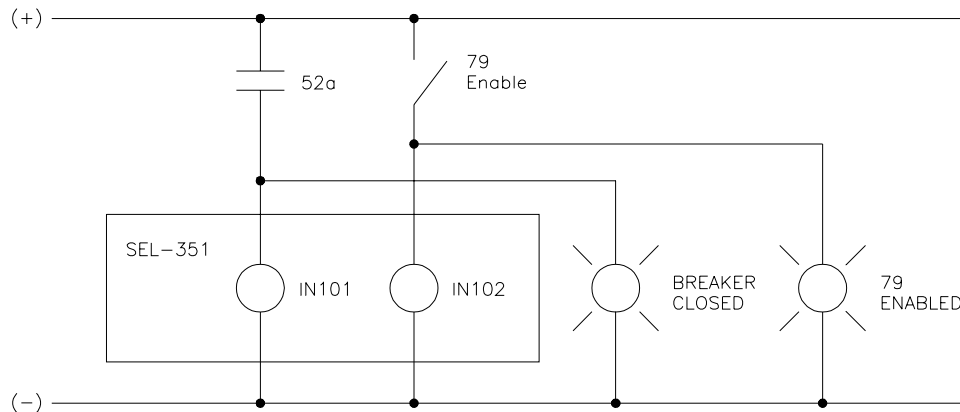
- circuit breaker open/closed
- reclosing relay enabled/disabled

Traditional Indicating Panel Lights

Figure 7.29 shows traditional indicating panel lights wired in parallel with SEL-351 Relay optoisolated inputs. Input IN101 provides circuit breaker status to the relay, and input IN102 enables/disables reclosing in the relay via the following SELOGIC control equation settings:

52A = IN101

79DTL = !IN102 [= NOT(IN102); drive-to-lockout setting]



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Figure 7.29: Traditional Panel Light Installations

Note that Figure 7.29 corresponds to Figure 7.3 (factory input settings example).

Reclosing Relay Status Indication

In Figure 7.29, the 79 ENABLED panel light illuminates when the “79 Enable” switch is closed. When the “79 Enable” switch is open, the 79 ENABLED panel light extinguishes, and it is understood that the reclosing relay is disabled.

Circuit Breaker Status Indication

In Figure 7.29, the BREAKER CLOSED panel light illuminates when the 52a circuit breaker auxiliary contact is closed. When the 52a circuit breaker auxiliary contact is open, the BREAKER CLOSED panel light extinguishes, and it is understood that the breaker is open.

Traditional Indicating Panel Lights Replaced with Rotating Default Display

The indicating panel lights are not needed if the rotating default display feature in the SEL-351 Relay is used. Figure 7.30 shows the elimination of the indicating panel lights by using the rotating default display.

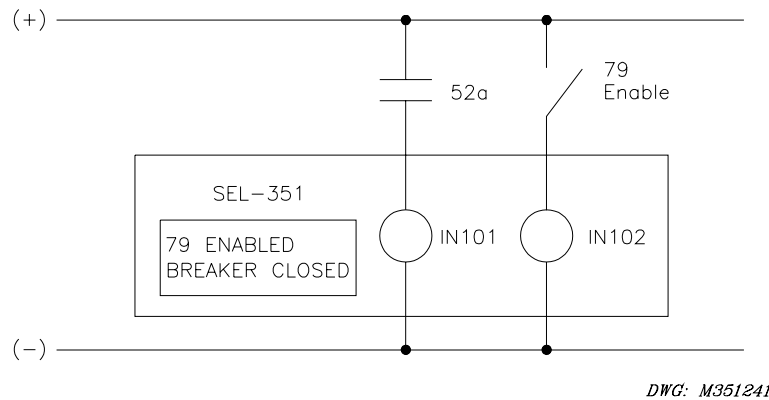


Figure 7.30: Rotating Default Display Replaces Traditional Panel Light Installations

There are sixteen (16) of these default displays available in the SEL-351 Relay. Each default display has two complementary screens (e.g., BREAKER CLOSED and BREAKER OPEN) available.

General Operation of Rotating Default Display Settings

SELOGIC control equation display point setting DPn (n = 1 through 16) controls the display of corresponding, complementary text settings:

- DPn_1 (displayed when DPn = logical 1)
- DPn_0 (displayed when DPn = logical 0)

Make each text setting through the serial port using the command **SET T**. View these text settings using the serial port command **SHO T** (see **Section 9: Setting the Relay** and **Section 10: Serial Port Communications and Commands**). These text settings are displayed on the SEL-351 Relay front-panel display on a time-variable rotation using **Global** setting **SCROLL** (see **Rotating Default Display** in **Section 11: Front-Panel Interface** for more specific operation information).

The following factory settings examples use optoisolated inputs IN101 and IN102 in the display points settings. Local bits (LB1 through LB16), latch bits (LT1 through LT16), remote bits (RB1 through RB16), setting group indicators (SG1 through SG6), and any other combination of Relay Word bits in a SELOGIC control equation setting can also be used in display point setting DPn.

Factory Settings Examples

The factory settings provide the replacement solution shown in Figure 7.30 for the traditional indicating panel lights in Figure 7.29.

Reclosing Relay Status Indication

Make SELOGIC control equation display point setting DP1:

$$DP1 = IN102$$

Make corresponding, complementary text settings:

DP1_1 = 79 ENABLED
DP1_0 = 79 DISABLED

Display point setting DP1 controls the display of the text settings.

Reclosing Relay Enabled

In Figure 7.30, optoisolated input IN102 is energized to enable the reclosing relay, resulting in:

DP1 = IN102 = logical 1

This results in the display of corresponding text setting DP1_1 on the front-panel display:

79 ENABLED

Reclosing Relay Disabled

In Figure 7.30, optoisolated input IN102 is deenergized to disable the reclosing relay, resulting in:

DP1 = IN102 = logical 0

This results in the display of corresponding text setting DP1_0 on the front-panel display:

79 DISABLED

Circuit Breaker Status Indication

Make SELOGIC control equation display point setting DP2:

DP2 = IN101

Make corresponding, complementary text settings:

DP2_1 = BREAKER CLOSED
DP2_0 = BREAKER OPEN

Display point setting DP2 controls the display of the text settings.

Circuit Breaker Closed

In Figure 7.30, optoisolated input IN101 is energized when the 52a circuit breaker auxiliary contact is closed, resulting in:

DP2 = IN101 = logical 1

This results in the display of corresponding text setting DP2_1 on the front-panel display:

BREAKER CLOSED

Circuit Breaker Open

In Figure 7.30, optoisolated input IN101 is deenergized when the 52a circuit breaker auxiliary contact is open, resulting in:

$$DP2 = IN101 = \text{logical } 0$$

This results in the display of corresponding text setting DP2_0 on the front-panel display:

BREAKER OPEN

Additional Settings Examples

Display Only One Message

To display just one screen, but not its complement, set only one of the text settings. For example, to display just the “breaker closed” condition, but not the “breaker open” condition, make the following settings:

DP2 = IN101	(52a circuit breaker auxiliary contact connected to input IN101—see Figure 7.30)
DP2_1 = BREAKER CLOSED	(displays when DP2 = logical 1)
DP2_0 =	(blank)

Circuit Breaker Closed

In Figure 7.30, optoisolated input IN101 is energized when the 52a circuit breaker auxiliary contact is closed, resulting in:

$$DP2 = IN101 = \text{logical } 1$$

This results in the display of corresponding text setting DP2_1 on the front-panel display:

BREAKER CLOSED

Circuit Breaker Open

In Figure 7.30, optoisolated input IN101 is deenergized when the 52a circuit breaker auxiliary contact is open, resulting in:

$$DP2 = IN101 = \text{logical } 0$$

Corresponding text setting DP2_0 is not set (it is “blank”), so no message is displayed on the front-panel display.

Continually Display a Message

To continually display a message in the rotation, set the SELOGIC control equation display point setting directly to 0 (logical 0) or 1 (logical 1) and the corresponding text setting. For example, if

an SEL-351 Relay is protecting a 12 kV distribution feeder, labeled “Feeder 1204,” the feeder name can be continually displayed with the following settings

DP5 = 1 (set directly to logical 1)
DP5_1 = FEEDER 1204 (displays when DP5 = logical 1)
DP5_0 = (“blank”)

This results in the continual display of text setting DP5_1 on the front-panel display:

FEEDER 1204

This can also be realized with the following settings:

DP5 = 0 (set directly to logical 0)
DP5_1 = (“blank”)
DP5_0 = FEEDER 1204 (displays when DP5 = logical 0)

This results in the continual display of text setting DP5_0 on the front-panel display:

FEEDER 1204

Active Setting Group Switching Considerations

The SELOGIC control equation display point settings DPn (n = 1 through 16) are available separately in each setting group. The corresponding text settings DPn_1 and DPn_0 are made only once and used in all setting groups.

Refer to Figure 7.30 and the following example setting group switching discussion.

Setting Group 1 is the Active Setting Group

When setting Group 1 is the active setting group, optoisolated input IN102 operates as a reclose enable/disable switch with the following settings:

SELOGIC control equation settings:

79DTL = !IN102 + ... [= NOT(IN102) + ...; drive-to-lockout setting]
DP1 = IN102

Text settings:

DP1_1 = 79 ENABLED (displayed when DP1 = logical 1)
DP1_0 = 79 DISABLED (displayed when DP1 = logical 0)

Reclosing Relay Enabled

In Figure 7.30, optoisolated input IN102 is energized to enable the reclosing relay, resulting in:

DP1 = IN102 = logical 1

This results in the display of corresponding text setting DP1_1 on the front-panel display:

79 ENABLED

Reclosing Relay Disabled

In Figure 7.30, optoisolated input IN102 is deenergized to disable the reclosing relay, resulting in:

DP1 = IN102 = logical 0

This results in the display of corresponding text setting DP1_0 on the front-panel display:

79 DISABLED

Now the active setting group is switched from setting Group 1 to 4.

Switch to Setting Group 4 as the Active Setting Group

When setting Group 4 is the active setting group, the reclosing relay is always disabled and optoisolated input IN102 has no control over the reclosing relay. The text settings cannot be changed (they are used in all setting groups), but the SELOGIC control equation settings can be changed:

SELOGIC control equation settings:

79DTL = 1 (set directly to logical 1—reclosing relay permanently “driven-to-lockout”)

DP1 = 0 (set directly to logical 0)

Text settings (remain the same for all setting groups):

DP1_1 = 79 ENABLED (displayed when DP1 = logical 1)

DP1_0 = 79 DISABLED (displayed when DP1 = logical 0)

Because SELOGIC control equation display point setting DP1 is always at logical 0, the corresponding text setting DP1_0 continually displays in the rotating default displays:

79 DISABLED

Additional Rotating Default Display Example

See Figure 5.17 and accompanying text in *Section 5: Trip and Target Logic* for an example of resetting a rotating default display with the TARGET RESET pushbutton.

Displaying Time-Overcurrent Elements on the Rotating Default Display

The LCD can display the pickup settings for the time-overcurrent elements in primary units via a special character sequence in the display points equations. As with the previously described display points, the operator does not need to press any buttons to see this information.

To program a display point to show the pickup setting of a time-overcurrent element, first enter the two-character sequence “::” (double colon) followed by the name of the desired time-overcurrent element pickup setting (e.g., 51PP, 51AP, 51BP, 51CP, 51NP, 51GP, or 51QP).

For example with the factory default settings for 51PP and CTR, setting DP1_0 = ::51PP will display **720.00 A pri**.

The relay calculates the value to display by multiplying the 51PP setting (6.00 A secondary) by the CTR setting (120), arriving at 720.00 A primary. The relay displays the display point DP1_0 because the factory default SELOGIC control equation DP1 = 0 (logical 0).

The calculations for the remaining time-overcurrent elements are similar, except for 51NP which is multiplied by the CTRN setting.

If the display point setting does not match the format correctly, the relay will display the setting text string as it was actually entered, without substituting the time-overcurrent element setting value.

Displaying Time-Overcurrent Elements Example

This example demonstrates use of the rotating display to show time-overcurrent elements in primary units. This example will set the 51PP and 51NP to display in the rotating default display.

Set the following:

SET	SET T	SET L
CTR = 100	DP1_0 = PHASE TRIPS AT	DP1 = 0
CTRN = 100	DP2_0 = ::51PP	DP2 = 0
E51P = 1	DP3_0 = NEUTRAL TRIPS AT	DP3 = 0
E51N = Y	DP4_0 = ::51NP	DP4 = 0
51PP = 5		
51NP = 1		

Setting DPn = 0 and using the DPn_0 in the text settings allows the setting to permanently rotate in the display. The DPn logic equation can be set to control the text display—turning it on and off under certain conditions. With the relay set as shown above, the LCD will show the following:

PHASE TRIPS AT
500.00 A pri

then,

NEUTRAL TRIPS AT
100.00 A pri

With the control string set on the even display points “DP2, DP4, DP6, ...” and the description set on the odd display points “DP1, DP3, ...” each screen the relay scrolls through will have a description with the value below it.

Displaying Metering Quantities on the Rotating Default Display

Display points can be programmed to display metering quantities automatically, making this information available without the use of pushbuttons. The following values can be set to automatically display on the rotating LCD screen:

IA, IB, IC, IN, VA, VB, VC, VS, IG, 3IO, I1, 3I2, 3V0, V1, V2, MWA, MWB, MWC, MW3, MVARA, MVARB, MVARC, MVAR3, PFA, PFB, PFC, PF3, FREQ, VDC, VAB, VBC, VCA

To program a display point to display one of the metering quantities above, first enter the two-character sequence “::” (double colon) followed by the name of the desired metering quantity (e.g., IA, VA, MW3, etc.).

If the display point setting does not match the format correctly, the relay will display the setting text string as it was actually entered, without substituting the metering value.

Displaying Metering Values Example

This example demonstrates use of the rotating display to show metering quantities automatically on the rotating default display. This example will set the MW3, MVAR3, PF3, and FREQ to display in the rotating default display.

Set the following:

SET T

DP1_0 = ::MW3
DP2_0 = ::MVAR3
DP3_0 = ::PF3
DP4_0 = ::FREQ

SET L

DP1 = 0
DP2 = 0
DP3 = 0
DP4 = 0

Setting DPn = 0 and using the DPn_0 in the text settings allows the setting to permanently rotate in the display. The DPn logic equation can be set to control the text display—turning it on and off under certain conditions. With the relay set as shown above, the LCD will show the following:

MW 3P= XXXX.X MVAR 3P= XXXX.X

then,

PF 3P=XX.XX XXXX FRQ=XX.X

Displaying Breaker Monitor Output Information on the Rotating Default Display

Display points can be programmed to display breaker monitor output information automatically, making this information available without using pushbuttons. The following values can be set to automatically display on the rotating LCD screen:

- Accumulated number of relay initiated trips (INTTR)
- Accumulated interrupted current from relay initiated trips (INTIA, INTIB, INTIC)
- Accumulated number of externally initiated trips (EXTTR)
- Accumulated interrupted current from externally initiated trips (EXTIA, EXTIB, EXTIC)
- Percent circuit breaker contact wear for each phase (WEARA, WEARB, WEARC)

To program a display point to display one of the Breaker Monitor outputs above, first enter the two-character sequence “:.” (double colon) followed by the name of the desired breaker monitor output (e.g., EXTTR, INTTR, INTIA, etc.).

If the display point setting does not match the format correctly, the relay will display the setting text string as it was actually entered, without substituting the breaker monitor output value.

Displaying Breaker Monitor Outputs Example

This example demonstrates use of the rotating display to show metering quantities automatically on the rotating default display. This example will set the EXTTR, INTTR, INTIA, EXTIA, and WEARA to display in the rotating default display.

Set the following:

SET T	SET L
DP1_0 = ::EXTTR	DP1 = 0
DP2_0 = ::INTTR	DP2 = 0
DP3_0 = ::INTIA	DP3 = 0
DP4_0 = ::EXTIA	DP4 = 0
DP5_0 = ::WEARA	DP5 = 0

Setting DPn = 0 and using the DPn_0 in the text settings allows the setting to permanently rotate in the display. The DPn logic equation can be set to control the text display—turning it on and off under certain conditions. With the relay set as shown above, the LCD will show the following:

EXT TRIPS=XXXXX
INT TRIPS=XXXXX

then,

INT IA=XXXXXX kA
EXT IA=XXXXXX kA

and then,

WEAR A= XXX %

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SECTION 8: BREAKER MONITOR, METERING, AND LOAD PROFILE FUNCTIONS

INTRODUCTION

The SEL-351 Relay monitoring functions include:

- Breaker Monitor
- Station DC Battery Monitor

In addition to instantaneous metering, the SEL-351 Relay metering functions include:

- Demand Metering
- Energy Metering
- Maximum/Minimum Metering

This section explains these functions in detail.

BREAKER MONITOR

The breaker monitor in the SEL-351 Relay helps in scheduling circuit breaker maintenance. The breaker monitor is enabled with the enable setting:

EBMON = Y

The breaker monitor settings in Table 8.2 are available via the SET G and SET L commands (see Table 9.1 in *Section 9: Setting the Relay* and also Settings Sheet 21 of 27 at the end of *Section 9*). Also, refer to *BRE Command (Breaker Monitor Data)* and *BRE n Command (Preload/Reset Breaker Wear)* in *Section 10: Serial Port Communications and Commands*.

The breaker monitor is set with breaker maintenance information provided by circuit breaker manufacturers. This breaker maintenance information lists the number of close/open operations that are permitted for a given current interruption level. The following is an example of breaker maintenance information for a 25 kV circuit breaker.

**Table 8.1: Breaker Maintenance Information
for a 25 kV Circuit Breaker**

Current Interruption Level (kA)	Permissible Number of Close/Open Operations*
0.00–1.20	10,000
2.00	3,700
3.00	1,500
5.00	400
8.00	150
10.00	85
20.00	12

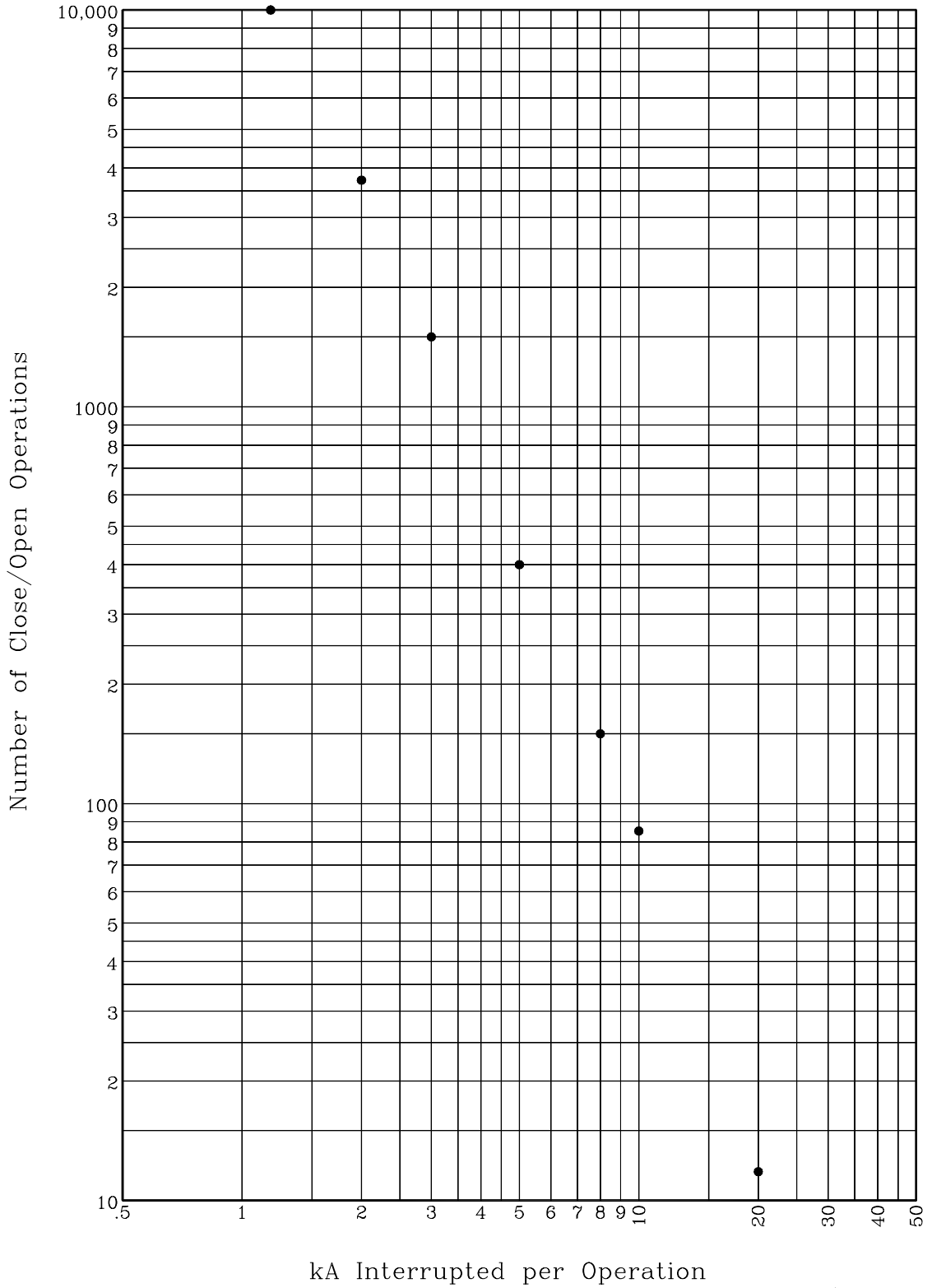
* The action of a circuit breaker closing and then later opening is counted as one close/open operation.

The breaker maintenance information in Table 8.1 is plotted in Figure 8.1.

Connect the plotted points in Figure 8.1 for a breaker maintenance curve. To estimate this breaker maintenance curve in the SEL-351 Relay breaker monitor, three set points are entered:

- Set Point 1 maximum number of close/open operations with corresponding current interruption level.
- Set Point 2 number of close/open operations that correspond to some midpoint current interruption level.
- Set Point 3 number of close/open operations that correspond to the maximum current interruption level.

These three points are entered with the settings in Table 8.2.



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Figure 8.1: Plotted Breaker Maintenance Points for a 25 kV Circuit Breaker

Breaker Monitor Setting Example

Table 8.2: Breaker Monitor Settings and Settings Ranges

Setting	Definition	Range
COSP1	Close/Open set point 1—maximum	0–65000 close/open operations
COSP2	Close/Open set point 2—middle	0–65000 close/open operations
COSP3	Close/Open set point 3—minimum	0–65000 close/open operations
KASP1*	kA Interrupted set point 1—minimum	0.00–999.00 kA in 0.01 kA steps
KASP2	kA Interrupted set point 1—middle	0.00–999.00 kA in 0.01 kA steps
KASP3*	kA Interrupted set point 1—maximum	0.00–999.00 kA in 0.01 kA steps
BKMON	SELOGIC [®] control equation breaker monitor initiation setting	Relay Word bits referenced in Table 9.3

* The ratio of settings KASP3/KASP1 must be: $5 \leq \text{KASP3/KASP1} \leq 100$

The following settings are made from the breaker maintenance information in Table 8.1 and Figure 8.1:

COSP1 = 10000
COSP2 = 150
COSP3 = 12
KASP1 = 1.20
KASP2 = 8.00
KASP3 = 20.00

Figure 8.2 shows the resultant breaker maintenance curve.

Breaker Maintenance Curve Details

In Figure 8.2, note that set points KASP1, COSP1 and KASP3, COSP3 are set with breaker maintenance information from the two extremes in Table 8.1 and Figure 8.1.

In this example, set point KASP2, COSP2 happens to be from an in-between breaker maintenance point in the breaker maintenance information in Table 8.1 and Figure 8.1, but it doesn't have to be. Set point KASP2, COSP2 should be set to provide the best "curve-fit" with the plotted breaker maintenance points in Figure 8.1.

Each phase (A, B, and C) has its own breaker maintenance curve (like that in Figure 8.2), because the separate circuit breaker interrupting contacts for phases A, B, and C don't necessarily interrupt the same magnitude current (depending on fault type and loading).

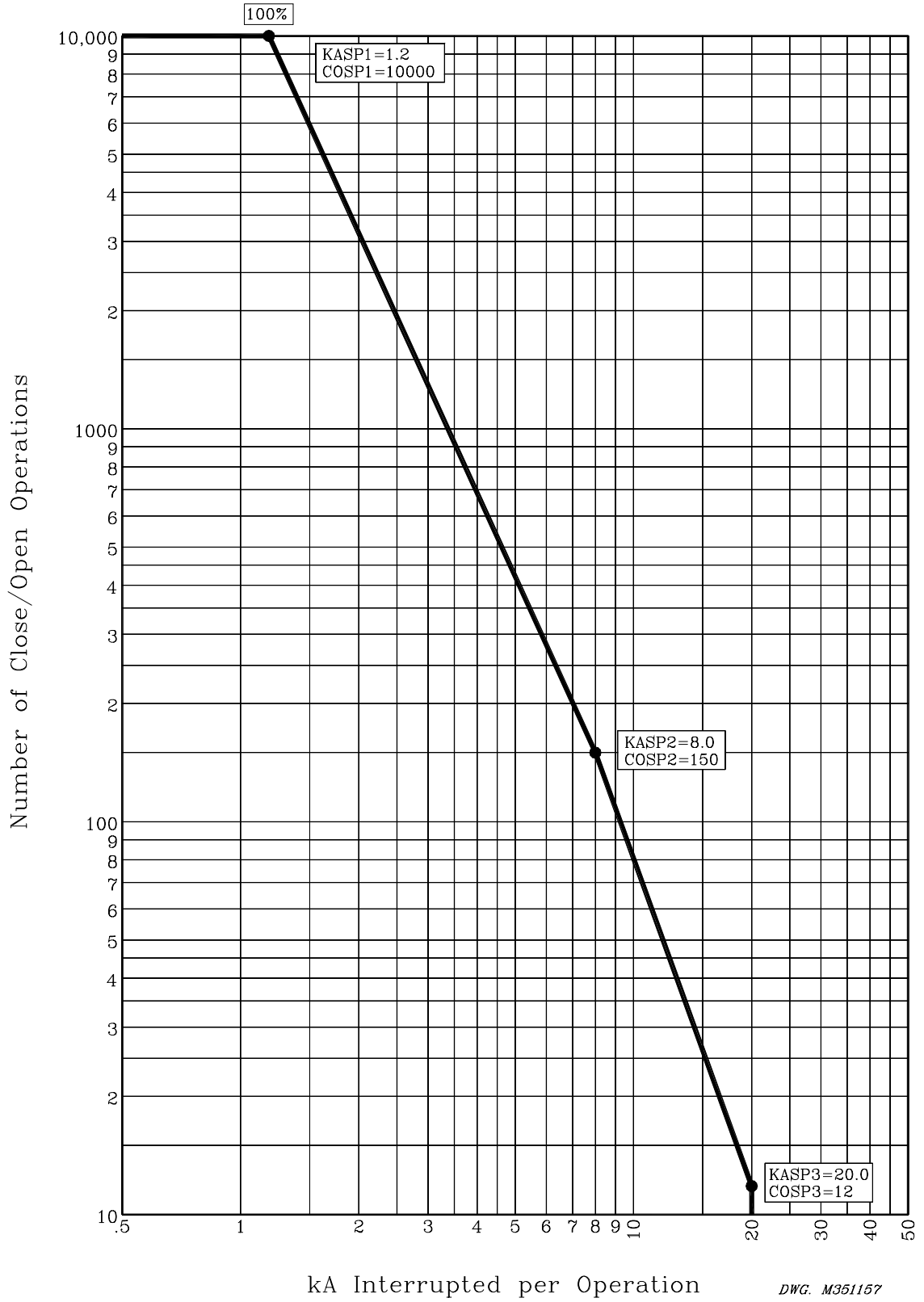


Figure 8.2: SEL-351 Relay Breaker Maintenance Curve for a 25 kV Circuit Breaker

In Figure 8.2, note that the breaker maintenance curve levels off horizontally below set point KASP1, COSP1. This is the close/open operation limit of the circuit breaker (COSP1 = 10000), regardless of interrupted current value.

Also, note that the breaker maintenance curve falls vertically above set point KASP3, COSP3. This is the maximum interrupted current limit of the circuit breaker (KASP3 = 20.0 kA). If the interrupted current is greater than setting KASP3, the interrupted current is accumulated as a current value equal to setting KASP3.

Operation of SELOGIC Control Equation Breaker Monitor Initiation Setting BKMON

The SELOGIC control equation breaker monitor initiation setting BKMON in Table 8.2 determines when the breaker monitor reads in current values (Phases A, B, and C) for the breaker maintenance curve (see Figure 8.2) and the breaker monitor accumulated currents/trips [see *BRE Command (Breaker Monitor Data)* in Section 10: *Serial Port Communications and Commands*].

The BKMON setting looks for a rising edge (logical 0 to logical 1 transition) as the indication to read in current values. The acquired current values are then applied to the breaker maintenance curve and the breaker monitor accumulated currents/trips (see references in previous paragraph).

In the factory default settings, the SELOGIC control equation breaker monitor initiation setting is set:

BKMON = TRIP (TRIP is the logic output of Figure 5.1)

Refer to Figure 8.3. When BKMON asserts (Relay Word bit TRIP goes from logical 0 to logical 1), the breaker monitor reads in the current values and applies them to the breaker monitor maintenance curve and the breaker monitor accumulated currents/trips.

As detailed in Figure 8.3, the breaker monitor actually reads in the current values 1.5 cycles after the assertion of BKMON. This helps especially if an instantaneous trip occurs. The instantaneous element trips when the fault current reaches its pickup setting level. The fault current may still be “climbing” to its full value and then levels off. The 1.5-cycle delay on reading in the current values allows time for the fault current to level off.

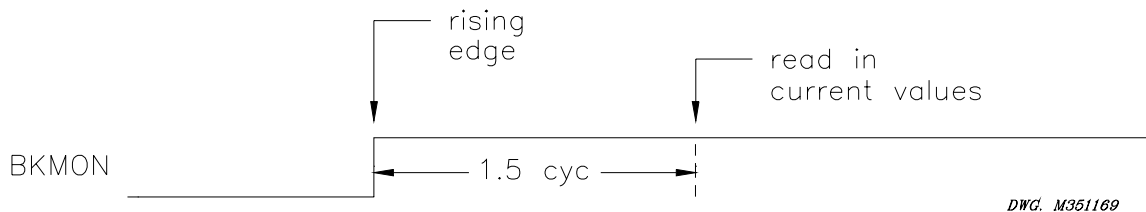


Figure 8.3: Operation of SELOGIC Control Equation Breaker Monitor Initiation Setting

See Figure 8.8 and accompanying text for more information on setting BKMON. The operation of the breaker monitor maintenance curve, when new current values are read in, is explained in the following example.

Breaker Monitor Operation Example

As stated earlier, each phase (A, B, and C) has its own breaker maintenance curve. For this example, presume that the interrupted current values occur on a single phase in Figure 8.4 through Figure 8.7. Also, presume that the circuit breaker interrupting contacts have no wear at first (brand new or recent maintenance performed).

Note in the following four figures (Figure 8.4 through Figure 8.7) that the interrupted current in a given figure is the same magnitude for all the interruptions (e.g., in Figure 8.5, 2.5 kA is interrupted 290 times). This is not realistic, but helps in demonstrating the operation of the breaker maintenance curve and how it integrates for varying current levels.

0 Percent to 10 Percent Breaker Wear

Refer to Figure 8.4. 7.0 kA is interrupted 20 times (20 close/open operations = 20 – 0), pushing the breaker maintenance curve from the 0 percent wear level to the 10 percent wear level.

Compare the 100 percent and 10 percent curves and note that for a given current value, the 10 percent curve has only 1/10 of the close/open operations of the 100 percent curve.

10 Percent to 25 Percent Breaker Wear

Refer to Figure 8.5. The current value changes from 7.0 kA to 2.5 kA. 2.5 kA is interrupted 290 times (290 close/open operations = 480 – 190), pushing the breaker maintenance curve from the 10 percent wear level to the 25 percent wear level.

Compare the 100 percent and 25 percent curves and note that for a given current value, the 25 percent curve has only 1/4 of the close/open operations of the 100 percent curve.

25 Percent to 50 Percent Breaker Wear

Refer to Figure 8.6. The current value changes from 2.5 kA to 12.0 kA. 12.0 kA is interrupted 11 times (11 close/open operations = 24 – 13), pushing the breaker maintenance curve from the 25 percent wear level to the 50 percent wear level.

Compare the 100 percent and 50 percent curves and note that for a given current value, the 50 percent curve has only 1/2 of the close/open operations of the 100 percent curve.

50 Percent to 100 Percent Breaker Wear

Refer to Figure 8.7. The current value changes from 12.0 kA to 1.5 kA. 1.5 kA is interrupted 3000 times (3000 close/open operations = 6000 – 3000), pushing the breaker maintenance curve from the 50 percent wear level to the 100 percent wear level.

When the breaker maintenance curve reaches 100 percent for a particular phase, the percentage wear remains at 100 percent (even if additional current is interrupted), until reset by the BRE R command (see *View or Reset Breaker Monitor Information* that follows later). But the current and trip counts continue to be accumulated, until reset by the BRE R command.

Additionally, logic outputs assert for alarm or other control applications—see the following discussion.

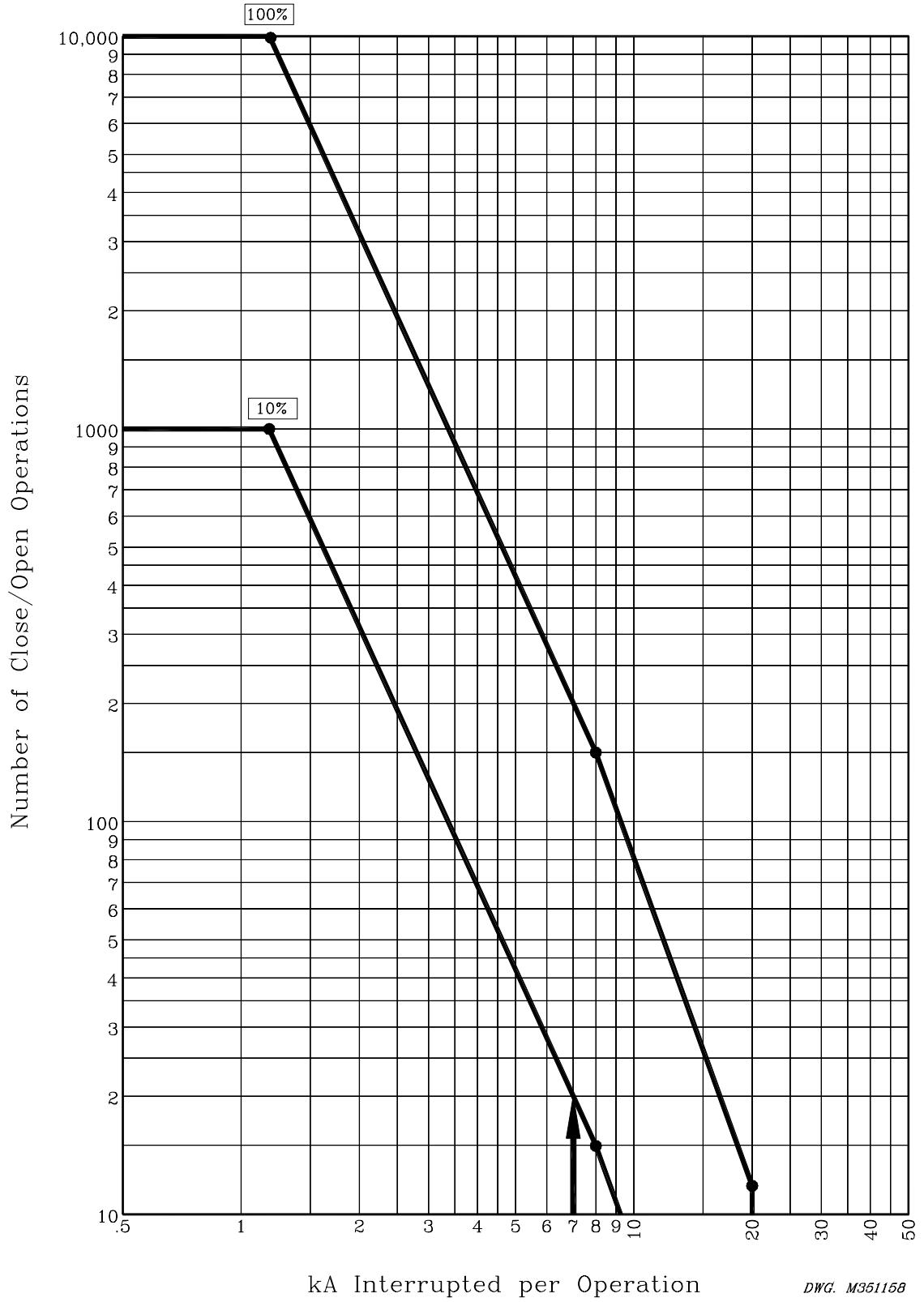
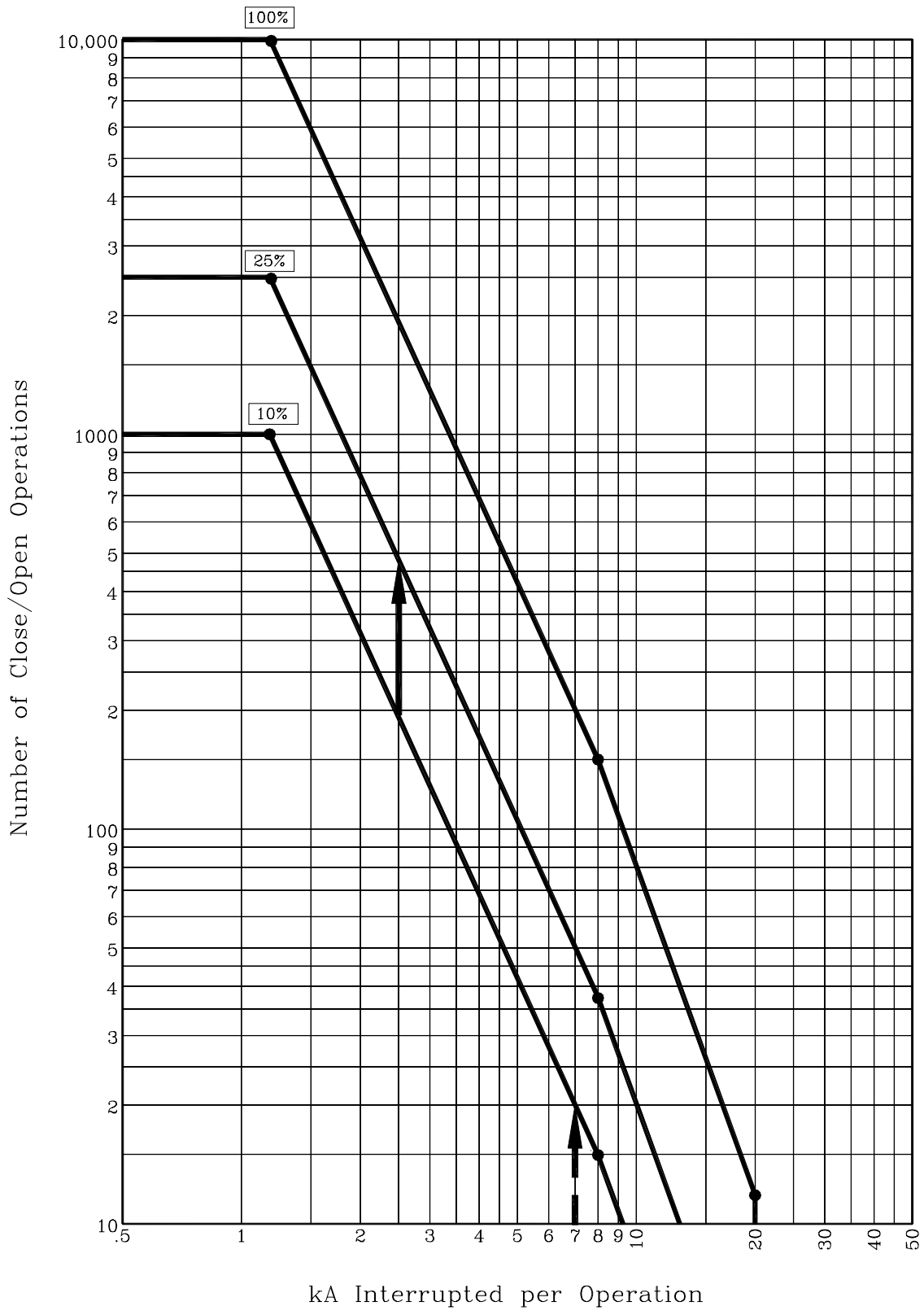


Figure 8.4: Breaker Monitor Accumulates 10 Percent Wear



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Figure 8.5: Breaker Monitor Accumulates 25 Percent Wear

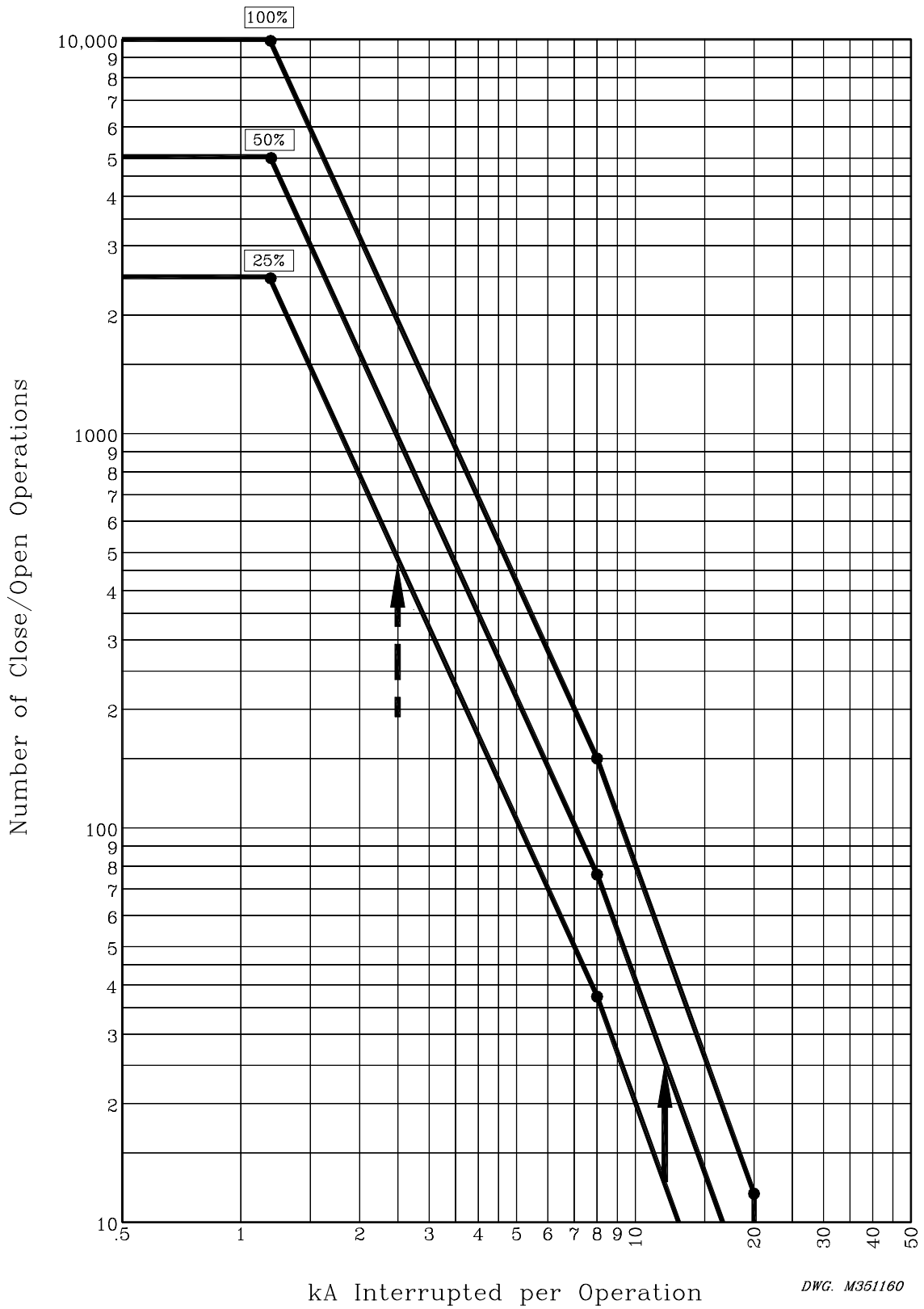


Figure 8.6: Breaker Monitor Accumulates 50 Percent Wear

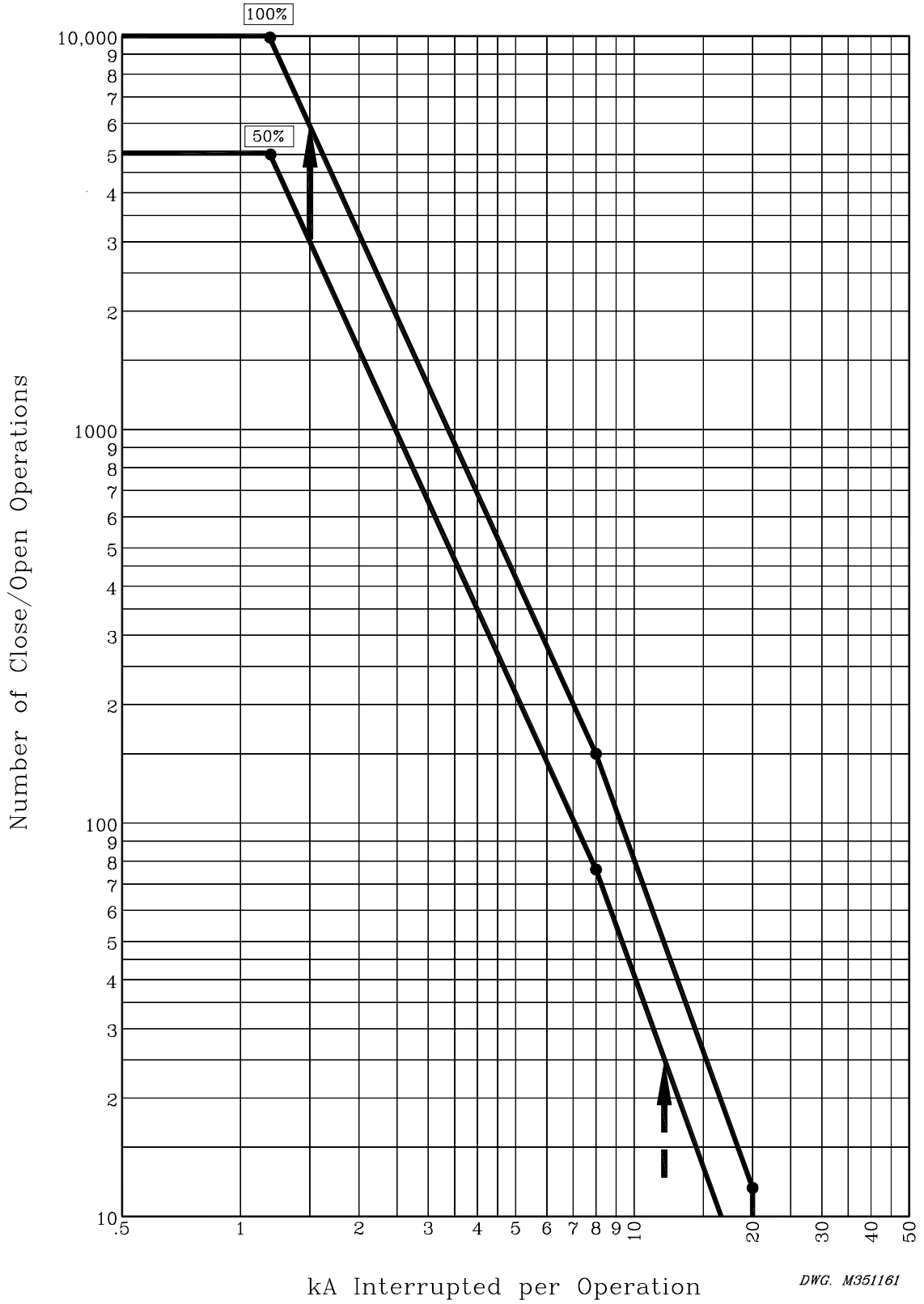


Figure 8.7: Breaker Monitor Accumulates 100 Percent Wear

Breaker Monitor Output

When the breaker maintenance curve for a particular phase (A, B, or C) reaches the 100 percent wear level (see Figure 8.7), a corresponding Relay Word bit (BCWA, BCWB, or BCWC) asserts.

<u>Relay Word Bits</u>	<u>Definition</u>
BCWA	Phase A breaker contact wear has reached the 100 percent wear level
BCWB	Phase B breaker contact wear has reached the 100 percent wear level
BCWC	Phase C breaker contact wear has reached the 100 percent wear level
BCW	BCWA + BCWB + BCWC

Example Applications

These logic outputs can be used to alarm:

OUT105 = BCW

or drive the relay to lockout the next time the relay trips:

79DTL = TRIP*BCW

View or Reset Breaker Monitor Information

Accumulated breaker wear/operations data is retained if the relay loses power or the breaker monitor is disabled (setting EBMON = N). The accumulated data can only be reset if the BRE R command is executed (see the following discussion on the BRE R command).

Via Serial Port

See *BRE Command (Breaker Monitor Data)* in *Section 10: Serial Port Communications and Commands*. The BRE command displays the following information:

- Accumulated number of relay initiated trips
- Accumulated interrupted current from relay initiated trips
- Accumulated number of externally initiated trips
- Accumulated interrupted current from externally initiated trips
- Percent circuit breaker contact wear for each phase
- Date when the preceding items were last reset (via the BRE R command)

See *BRE n Command (Preload/Reset Breaker Wear)* in *Section 10: Serial Port Communications and Commands*. The BRE W command allows the percent breaker wear to be preloaded for each individual phase.

The BRE R command resets the accumulated values and the percent wear for all three phases. For example, if breaker contact wear has reached the 100 percent wear level for A-phase, the corresponding Relay Word bit BCWA asserts (BCWA = logical 1). Execution of the BRE R command resets the wear levels for all three phases back to 0 percent and consequently causes Relay Word bit BCWA to deassert (BCWA = logical 0).

Via Front Panel

The information and reset functions available via the previously discussed serial port commands BRE and BRE R are also available via the front-panel OTHER pushbutton. See Figure 11.3 in *Section 11: Front-Panel Interface*.

Determination of Relay Initiated Trips and Externally Initiated Trips

See *BRE Command (Breaker Monitor Data)* in *Section 10: Serial Port Communications and Commands*. Note in the BRE command response that the accumulated number of trips and accumulated interrupted current are separated into two groups of data: that generated by relay initiated trips (Rly Trips) and that generated by externally initiated trips (Ext Trips). The categorization of this data is determined by the status of the TRIP Relay Word bit when the SELOGIC control equation breaker monitor initiation setting BKMON operates.

Refer to Figure 8.3 and accompanying explanation. If BKMON newly asserts (logical 0 to logical 1 transition), the relay reads in the current values (Phases A, B, and C). Now the decision has to be made: where is this current and trip count information accumulated? Under relay initiated trips or externally initiated trips?

To make this determination, the status of the TRIP Relay Word bit is checked at the instant BKMON newly asserts (TRIP is the logic output of Figure 5.1). If TRIP is asserted (TRIP = logical 1), the current and trip count information is accumulated under relay initiated trips (Rly Trips). If TRIP is deasserted (TRIP = logical 0), the current and trip count information is accumulated under externally initiated trips (Ext Trips).

Regardless of whether the current and trip count information is accumulated under relay initiated trips or externally initiated trips, this same information is routed to the breaker maintenance curve for continued breaker wear integration (see Figure 8.3 through Figure 8.7).

Factory Default Setting Example

As discussed previously, the SELOGIC control equation breaker monitor initiation factory default setting is:

$$\text{BKMON} = \text{TRIP}$$

Thus, any new assertion of BKMON will be deemed a relay trip, and the current and trip count information is accumulated under relay initiated trips (Rly Trips).

Additional Example

Refer to Figure 8.8. Output contact OUT101 is set to provide tripping:

$$\text{OUT101} = \text{TRIP}$$

Note that optoisolated input IN106 monitors the trip bus. If the trip bus is energized by output contact OUT101, an external control switch, or some other external trip, then IN106 is asserted.

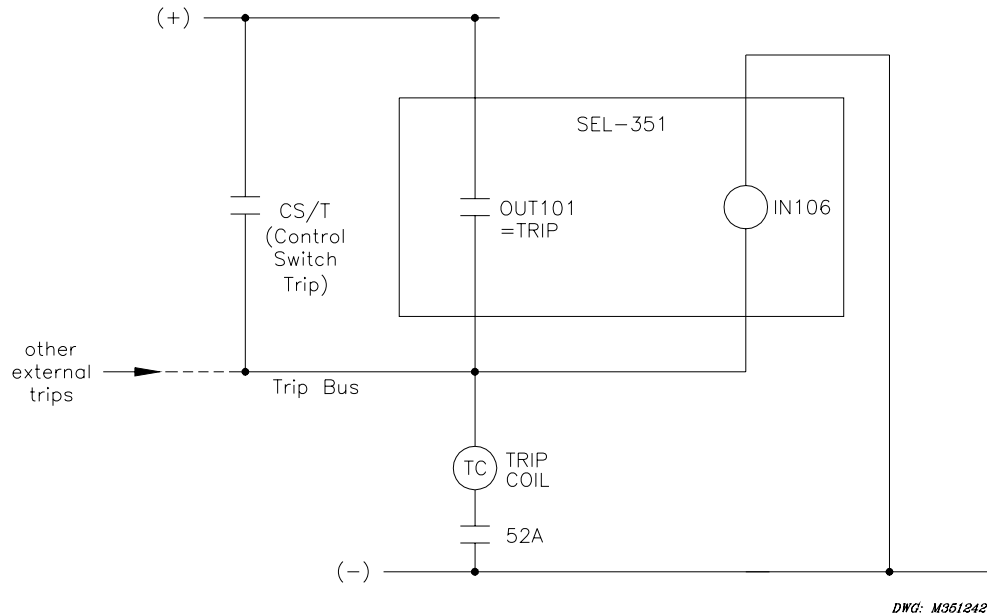


Figure 8.8: Input IN106 Connected to Trip Bus for Breaker Monitor Initiation

If the SELOGIC control equation breaker monitor initiation setting is set:

$$\text{BKMON} = \text{IN106}$$

then the SEL-351 Relay breaker monitor sees all trips.

If output contact OUT101 asserts, energizing the trip bus, the breaker monitor will deem it a relay initiated trip. This is because when BKMON is newly asserted (input IN106 energized), the TRIP Relay Word bit is asserted. Thus, the current and trip count information is accumulated under relay initiated trips (Rly Trips).

If the control switch trip (or some other external trip) asserts, energizing the trip bus, the breaker monitor will deem it an externally initiated trip. This is because when BKMON is newly asserted (input IN106 energized), the TRIP Relay Word bit is deasserted. Thus, the current and trip count information is accumulated under externally initiated trips (Ext Trips).

STATION DC BATTERY MONITOR

The station dc battery monitor in the SEL-351 Relay can alarm for under- or overvoltage dc battery conditions and give a view of how much the station dc battery voltage dips when tripping, closing, and other dc control functions take place. The monitor measures the station dc battery voltage applied to the rear-panel terminals labeled POWER (see Figures 2.2, 2.3, and 2.4). The station dc battery monitor settings (DCLOP and DCHIP) are available via the SET G command (see Table 9.1 in *Section 9: Setting the Relay* and also Settings Sheet 20 of 27 in the back of *Section 9*).

DC Under- and Overvoltage Elements

Refer to Figure 8.9. The station dc battery monitor compares the measured station battery voltage (V_{dc}) to the undervoltage (low) and overvoltage (high) pickups DCLOP and DCHIP. The setting range for pickup settings DCLOP and DCHIP is:

20 to 300 Vdc, 1 Vdc increments

This range allows the SEL-351 Relay to monitor nominal battery voltages of 24, 48, 110, 125, and 250 V. When testing the pickup settings DCLOP and DCHIP, **do not** operate the SEL-351 Relay outside of its power supply limits. The relay is shipped with either a 24/48 V supply with operating range of 20 to 60 Vdc or a 125/250 V supply with operating range of 85 to 350 Vdc. The power supply rating is located on the serial number sticker on the relay rear panel.

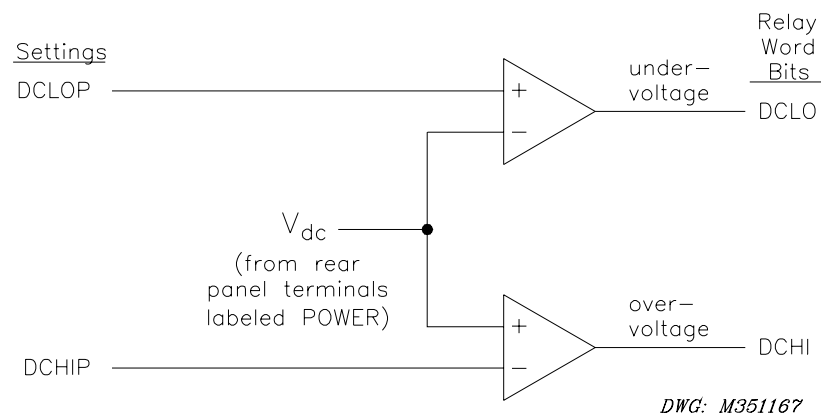


Figure 8.9: DC Under- and Overvoltage Elements

Logic outputs DCLO and DCHI in Figure 8.9 operate as follows:

- DCLO = 1 (logical 1), if $V_{dc} \leq$ pickup setting DCLOP
- DCLO = 0 (logical 0), if $V_{dc} >$ pickup setting DCLOP
- DCHI = 1 (logical 1), if $V_{dc} \geq$ pickup setting DCHIP
- DCHI = 0 (logical 0), if $V_{dc} <$ pickup setting DCHIP

Create Desired Logic for DC Under- and Overvoltage Alarming

Pickup settings DCLOP and DCHIP are set independently. Thus, they can be set:

$$\text{DCLOP} < \text{DCHIP} \quad \text{or} \quad \text{DCLOP} > \text{DCHIP}$$

Figure 8.10 shows the resultant dc voltage elements that can be created with SELOGIC control equations for these two setting cases. In these two examples, the resultant dc voltage elements are time-qualified by timer SV4T and then routed to output contact OUT106 for alarm purposes.

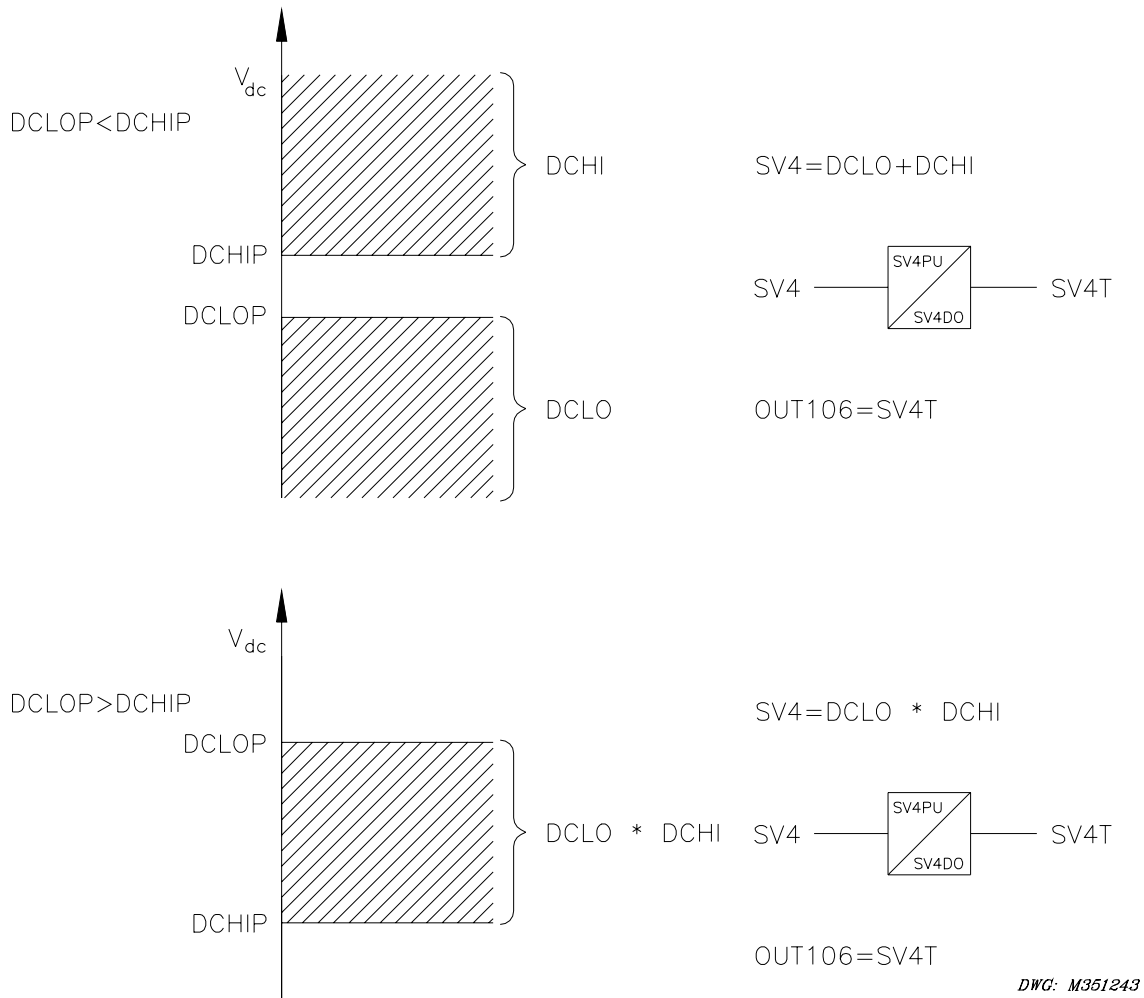


Figure 8.10: Create DC Voltage Elements with SELOGIC Control Equations

DCLO < DCHI (Top of Figure 8.10)

Output contact OUT106 asserts when:

$$V_{dc} \leq DCLOP \quad \text{or} \quad V_{dc} \geq DCHIP$$

Pickup settings DCLOP and DCHIP are set such that output contact OUT106 asserts when dc battery voltage goes below or above allowable limits.

If the relay loses power entirely ($V_{dc} = 0$ Vdc)

$$V_{dc} = < DCLOP$$

then output contact OUT106 should logically assert (according to top of Figure 8.10), but cannot because of the total loss of power (all output contacts deassert on total loss of power). Thus, the resultant dc voltage element at the bottom of Figure 8.10 would probably be a better choice—see following discussion.

DCLO > DCHI (Bottom of Figure 8.10)

Output contact OUT106 asserts when:

$$DCHIP \leq V_{dc} \leq DCLOP$$

Pickup settings DCLOP and DCHIP are set such that output contact OUT106 asserts when dc battery voltage stays between allowable limits.

If the relay loses power entirely ($V_{dc} = 0$ Vdc)

$$V_{dc} = < DCHIP$$

then output contact OUT106 should logically deassert (according to bottom of Figure 8.10), and this is surely what happens for a total loss of power (all output contacts deassert on total loss of power).

Output Contact Type Considerations ("a" or "b")

Refer to *Output Contacts* in *Section 7: Inputs, Outputs, Timers, and Other Control Logic* (especially Note 2 in Figure 7.28). Consider the output contact type ("a" or "b") needed for output contact OUT106 in the bottom of Figure 8.10 (dc voltage alarm example).

If SELOGIC control equation setting OUT106 is asserted ($OUT106 = SV4T =$ logical 1; dc voltage OK), the state of output contact OUT106 (according to contact type) is:

closed ("a" type output contact)

open ("b" type output contact)

If SELOGIC control equation setting OUT106 is deasserted ($OUT106 = SV4T =$ logical 0; dc voltage not OK), the state of output contact OUT106 (according to contact type) is:

open ("a" type output contact)

closed ("b" type output contact)

If the relay loses power entirely, all output contacts deassert, and the state of output contact OUT106 (according to contact type) is:

open ("a" type output contact)

closed ("b" type output contact)

Additional Application

Other than alarming, the dc voltage elements can be used to disable reclosing.

For example, if the station dc batteries have a problem and the station dc battery voltage is declining, drive the reclosing relay to lockout:

$$79DTL = !SV4T + \dots \quad [= \text{NOT}(SV4T) + \dots]$$

Timer output SV4T is from the bottom of Figure 8.10. When dc voltage falls below pickup DCHIP, timer output SV4T drops out (= logical 0), driving the relay to lockout:

$$79DTL = !SV4T + \dots = \text{NOT}(SV4T) + \dots = \text{NOT}(\text{logical } 0) + \dots = \text{logical } 1$$

Circuit breaker tripping and closing requires station dc battery energy. If the station dc batteries are having a problem and the station dc battery voltage is declining, the relay should not reclose after a trip—there might not be enough dc battery energy to trip a second time after a reclose.

View Station DC Battery Voltage

Via Serial Port

See *MET Command (Metering Data)*—Instantaneous Metering in *Section 10: Serial Port Communications and Commands*. The MET command displays the station dc battery voltage (labeled VDC).

Via Front Panel

The information available via the previously discussed MET serial port command is also available via the front-panel OTHER pushbutton. See Figure 11.3 in *Section 11: Front-Panel Interface*.

Analyze Station DC Battery Voltage

See *Standard 15/30-Cycle Event Reports* in *Section 12: Standard Event Reports, Sag/Swell, Interruption Report, and SER*. The station dc battery voltage is displayed in column Vdc in the example event report in Figure 12.2. Changes in station dc battery voltage for an event (e.g., circuit breaker tripping) can be observed. Use the EVE command to retrieve event reports as discussed in *Section 12*.

Station DC Battery Voltage Dips During Circuit Breaker Tripping

Event reports are automatically generated when the TRIP Relay Word bit asserts (TRIP is the logic output of Figure 5.1). For example, output contact OUT101 is set to trip:

$$\text{OUT101} = \text{TRIP}$$

Anytime output contact OUT101 closes and energizes the circuit breaker trip coil. Any dip in station dc battery voltage can be observed in column Vdc in the event report.

To generate an event report for external trips, make connections similar to Figure 8.8 and program optoisolated input IN106 (monitoring the trip bus) in the SELOGIC control equation event report generation setting:

$$\text{e.g., } \text{ER} = /\text{IN106} + \dots$$

Anytime the trip bus is energized, any dip in station dc battery voltage can be observed in column Vdc in the event report.

Station DC Battery Voltage Dips During Circuit Breaker Closing

To generate an event report when the SEL-351 Relay closes the circuit breaker, make the SELOGIC control equation event report generation setting:

$$ER = /OUT102 + \dots$$

In this example, output contact OUT102 is set to close:

$$OUT102 = CLOSE \quad (\text{CLOSE is the logic output of Figure 6.1})$$

Anytime output contact OUT102 closes and energizes the circuit breaker close coil, any dip in station dc battery voltage can be observed in column Vdc in the event report.

This event report generation setting ($ER = /OUT102 + \dots$) might be made just as a testing setting. Generate several event reports when doing circuit breaker close testing and observe the “signature” of the station dc battery voltage in column Vdc in the event reports.

Station DC Battery Voltage Dips Anytime

To generate an event report anytime there is a station dc battery voltage dip, set the dc voltage element directly in the SELOGIC control equation event report generation setting:

$$ER = \backslash SV4T + \dots$$

Timer output SV4T is an example dc voltage element from the bottom of Figure 8.10. Anytime dc voltage falls below pickup DCHIP, timer output SV4T drops out (logical 1 to logical 0 transition), creating a falling-edge condition that generates an event report.

Also, the Sequential Event Recorder (SER) report can be used to time-tag station dc battery voltage dips [see *Sequential Events Recorder (SER) Report* in *Section 12: Standard Event Reports, Sag/Swell/Interruption Report, and SER*].

Operation of Station DC Battery Monitor When AC Voltage is Powering the Relay

If the SEL-351 Relay has a 125/250 Vac/Vdc supply, it can be powered by ac voltage (85 to 264 Vac) connected to the rear-panel terminals labeled POWER. When powering the relay with ac voltage, the dc voltage elements in Figure 8.9 see the average of the sampled ac voltage powering the relay—which is very near zero volts (as displayed in column Vdc in event reports). Thus, pickup settings DCLOP and DCHIP should be set off (DCLOP = OFF, DCHIP = OFF)—they are of no real use.

If a “raw” event report is displayed (with the EVE R command), column Vdc will display the sampled ac voltage waveform, rather than the average.

DEMAND METERING

The SEL-351 Relay offers the choice between two types of demand metering, settable with the enable setting:

EDEM = THM (Thermal Demand Meter)

or

EDEM = ROL (Rolling Demand Meter)

The demand metering settings (in Table 8.3) are available via the SET command (see Table 9.1 in *Section 9: Setting the Relay* and also Settings Sheet 11 of 27 at the end of *Section 9*). Also refer to *MET Command (Metering Data)*, MET D—Demand Metering in *Section 10: Serial Port Communications and Commands*).

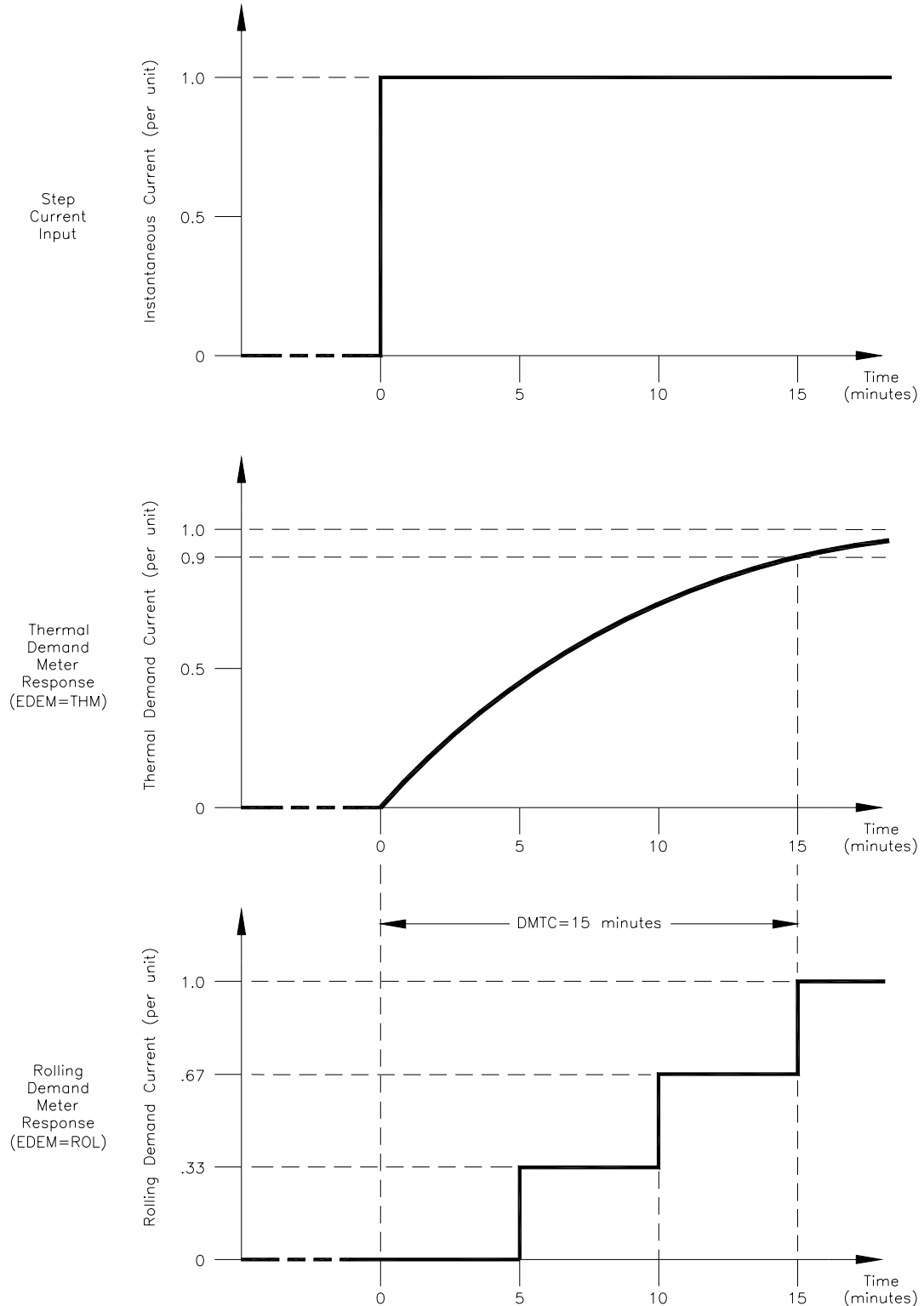
The SEL-351 Relay provides demand and peak demand metering for the following values:

Currents	$I_{A,B,C,N}$	Input currents (A primary)
	I_G	Residual ground current (A primary; $I_G = 3I_0 = I_A + I_B + I_C$)
	$3I_2$	Negative-sequence current (A primary)
Power	$MW_{A,B,C,3P}$	Single- and three-phase megawatts
	$MVAR_{A,B,C,3P}$	Single- and three-phase megavars

Depending on enable setting EDEM, these demand and peak demand values are thermal demand or rolling demand values. The differences between thermal and rolling demand metering are explained in the following discussion.

Comparison of Thermal and Rolling Demand Meters

The example in Figure 8.11 shows the response of thermal and rolling demand meters to a step current input. The current input is at a magnitude of zero and then suddenly goes to an instantaneous level of 1.0 per unit (a “step”).



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Figure 8.11: Response of Thermal and Rolling Demand Meters to a Step Input (setting DMTC = 15 minutes)

Thermal Demand Meter Response (EDEM = THM)

The response of the thermal demand meter in Figure 8.11 (middle) to the step current input (top) is analogous to the series RC circuit in Figure 8.12.

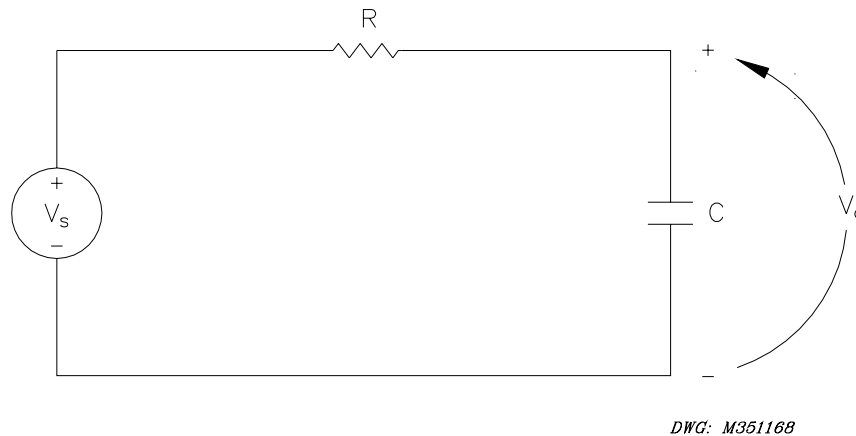


Figure 8.12: Voltage V_S Applied to Series RC Circuit

In the analogy:

Voltage V_S in Figure 8.12 corresponds to the step current input in Figure 8.11 (top).

Voltage V_C across the capacitor in Figure 8.12 corresponds to the response of the thermal demand meter in Figure 8.11 (middle).

If voltage V_S in Figure 8.12 has been at zero ($V_S = 0.0$ per unit) for some time, voltage V_C across the capacitor in Figure 8.12 is also at zero ($V_C = 0.0$ per unit). If voltage V_S is suddenly stepped up to some constant value ($V_S = 1.0$ per unit), voltage V_C across the capacitor starts to rise toward the 1.0 per unit value. This voltage rise across the capacitor is analogous to the response of the thermal demand meter in Figure 8.11 (middle) to the step current input (top).

In general, as voltage V_C across the capacitor in Figure 8.12 cannot change instantaneously, the thermal demand meter response is not immediate either for the increasing or decreasing applied instantaneous current. The thermal demand meter response time is based on the demand meter time constant setting DMTC (see Table 8.3). Note in Figure 8.11, the thermal demand meter response (middle) is at 90 percent (0.9 per unit) of full applied value (1.0 per unit) after a time period equal to setting DMTC = 15 minutes, referenced to when the step current input is first applied.

The SEL-351 Relay updates thermal demand values approximately every 2 seconds.

Rolling Demand Meter Response (EDEM = ROL)

The response of the rolling demand meter in Figure 8.11 (bottom) to the step current input (top) is calculated with a sliding time-window arithmetic average calculation. The width of the sliding time-window is equal to the demand meter time constant setting DMTC (see Table 8.3). Note in Figure 8.11, the rolling demand meter response (bottom) is at 100 percent (1.0 per unit) of full applied value (1.0 per unit) after a time period equal to setting DMTC = 15 minutes, referenced to when the step current input is first applied.

The rolling demand meter integrates the applied signal (e.g., step current) input in 5-minute intervals. The integration is performed approximately every 2 seconds. The average value for an integrated 5-minute interval is derived and stored as a 5-minute total. The rolling demand meter then averages a number of the 5-minute totals to produce the rolling demand meter response. In the Figure 8.11 example, the rolling demand meter averages the three latest 5-minute totals because setting DMTC = 15 (15/5 = 3). The rolling demand meter response is updated every 5 minutes, after a new 5-minute total is calculated.

The following is a step-by-step calculation of the rolling demand response example in Figure 8.11 (bottom).

Time = 0 Minutes

Presume that the instantaneous current has been at zero for quite some time before “Time = 0 minutes” (or the demand meters were reset). The three 5-minute intervals in the sliding time-window at “Time = 0 minutes” each integrate into the following 5-minute totals:

<u>5-Minute Totals</u>	<u>Corresponding 5-Minute Interval</u>
0.0 per unit	-15 to -10 minutes
0.0 per unit	-10 to -5 minutes
<u>0.0 per unit</u>	-5 to 0 minutes
0.0 per unit	

Rolling demand meter response at “Time = 0 minutes” = $0.0/3 = 0.0$ per unit

Time = 5 Minutes

The three 5-minute intervals in the sliding time-window at “Time = 5 minutes” each integrate into the following 5-minute totals:

<u>5-Minute Totals</u>	<u>Corresponding 5-Minute Interval</u>
0.0 per unit	-10 to -5 minutes
0.0 per unit	-5 to 0 minutes
<u>1.0 per unit</u>	0 to 5 minutes
1.0 per unit	

Rolling demand meter response at “Time = 5 minutes” = $1.0/3 = 0.33$ per unit

Time = 10 Minutes

The three 5-minute intervals in the sliding time-window at “Time = 10 minutes” each integrate into the following 5-minute totals:

<u>5-Minute Totals</u>	<u>Corresponding 5-Minute Interval</u>
0.0 per unit	-5 to 0 minutes
1.0 per unit	0 to 5 minutes
<u>1.0 per unit</u>	5 to 10 minutes
2.0 per unit	

Rolling demand meter response at “Time = 10 minutes” = $2.0/3 = 0.67$ per unit

Time = 15 Minutes

The three 5-minute intervals in the sliding time-window at “Time = 15 minutes” each integrate into the following 5-minute totals:

<u>5-Minute Totals</u>	<u>Corresponding 5-Minute Interval</u>
1.0 per unit	0 to 5 minutes
1.0 per unit	5 to 10 minutes
<u>1.0 per unit</u>	10 to 15 minutes
3.0 per unit	

Rolling demand meter response at “Time = 15 minutes” = $3.0/3 = 1.0$ per unit

Demand Meter Settings

Table 8.3: Demand Meter Settings and Settings Range

Setting	Definition	Range
EDEM	Demand meter type	THM = thermal ROL = rolling
DMTC	Demand meter time constant	5, 10, 15, 30, or 60 minutes
PDEMP	Phase demand current pickup	OFF
NDEMP	Neutral ground demand current pickup	0.50–16.00 A {5 A nominal} 0.10–3.20 A {1 A nominal} 0.005–0.160 A {0.05 A nominal channel IN current input}
GDEMP	Residual ground demand current pickup	
QDEMP	Negative-sequence demand current pickup	

Note: Changing setting EDEM or DMTC resets the demand meter values to zero. This also applies to changing the active setting group, and setting EDEM or DMTC is different in the new active setting group. Demand current pickup settings PDEMP, NDEMP, GDEMP, and QDEMP can be changed without affecting the demand meters.

The examples in this section discuss demand current, but MW and MVAR demand values are also available, as stated at the beginning of this subsection.

The demand current pickup settings in Table 8.3 are applied to demand current meter outputs as shown in Figure 8.13. For example, when residual ground demand current $I_{G(DEM)}$ goes above corresponding demand pickup GDEMP, Relay Word bit GDEM asserts to logical 1. Use these demand current logic outputs (PDEM, NDEM, GDEM, and QDEM) to alarm for high loading or unbalance conditions. Use in other schemes such as the following example.

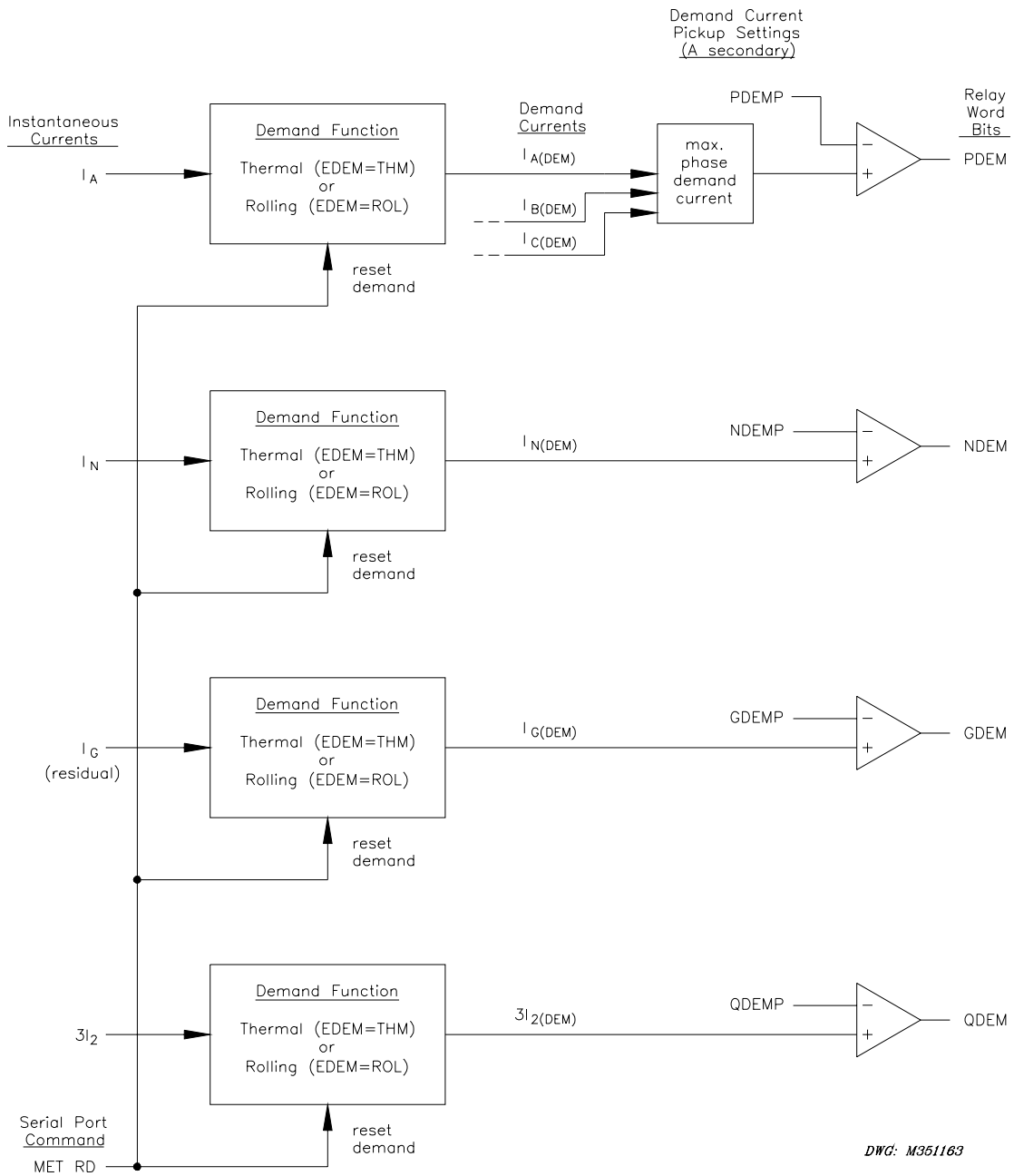


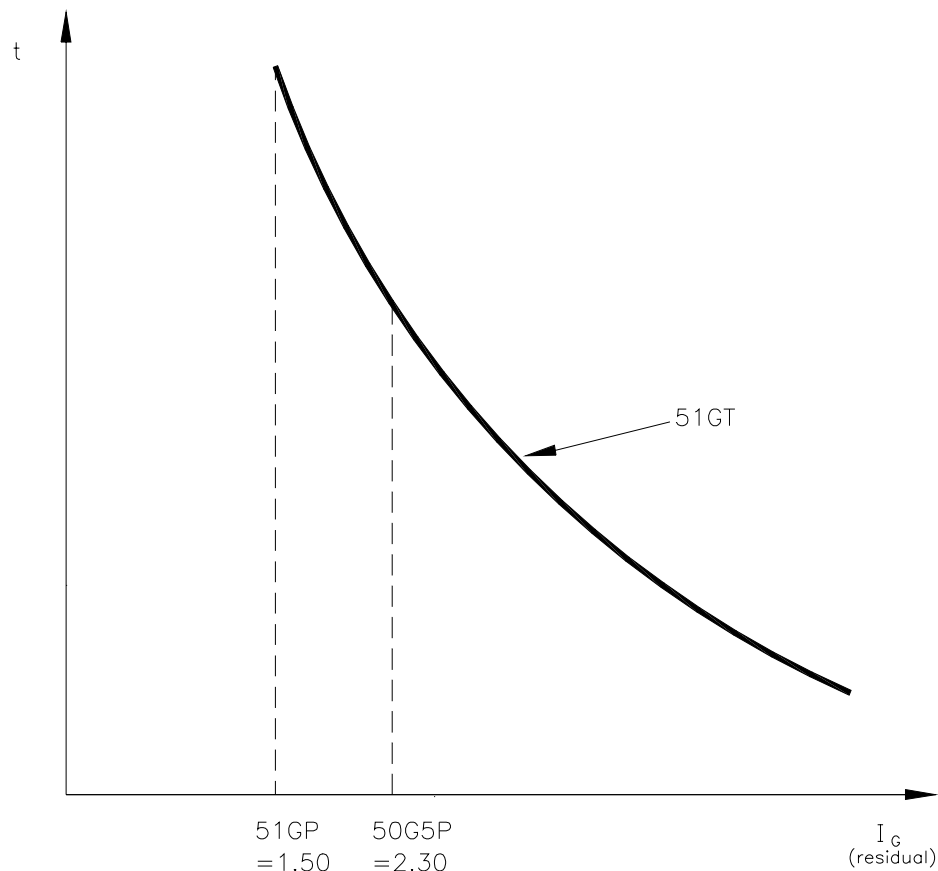
Figure 8.13: Demand Current Logic Outputs

Demand Current Logic Output Application—Raise Pickup for Unbalance Current

During times of high loading, the residual ground overcurrent elements can see relatively high unbalance current I_G ($I_G = 3I_0$). To avoid tripping on unbalance current I_G , use Relay Word bit GDEM to detect the residual ground (unbalance) demand current $I_{G(DEM)}$ and effectively raise the pickup of the residual ground time-overcurrent element 51GT. This is accomplished with the following settings from Table 8.3, pertinent residual ground overcurrent element settings, and SELLOGIC control equation torque control setting 51GTC:

EDEM = THM
DMTC = 5
GDEMP = 1.0
51GP = 1.50
50G5P = 2.30
51GTC = !GDEM + GDEM*50G5

Refer to Figure 8.13, Figure 8.14, and Figure 3.19.



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Figure 8.14: Raise Pickup of Residual Ground Time-Overcurrent Element for Unbalance Current

Residual Ground Demand Current Below Pickup GDEMP

When unbalance current I_G is low, unbalance demand current $I_{G(DEM)}$ is below corresponding demand pickup $GDEMP = 1.00$ A secondary, and Relay Word bit $GDEM$ is deasserted to logical 0. This results in SELOGIC control equation torque control setting $51GTC$ being in the state:

$$\begin{aligned} 51GTC &= !GDEM + GDEM*50G5 = \text{NOT}(GDEM) + GDEM*50G5 \\ &= \text{NOT}(\text{logical } 0) + (\text{logical } 0)*50G5 = \text{logical } 1 \end{aligned}$$

Thus, the residual ground time-overcurrent element $51GT$ operates on its standard pickup:

$$51GP = 1.50 \text{ A secondary}$$

If a ground fault occurs, the residual ground time-overcurrent element $51GT$ operates with the sensitivity provided by pickup $51GP = 1.50$ A secondary. The thermal demand meter, even with setting $DMTC = 5$ minutes, does not respond fast enough to the ground fault to make a change to the effective residual ground time-overcurrent element pickup—it remains at 1.50 A secondary. Demand meters respond to more “slow moving” general trends.

Residual Ground Demand Current Goes Above Pickup GDEMP

When unbalance current I_G increases, unbalance demand current $I_{G(DEM)}$ follows, going above corresponding demand pickup $GDEMP = 1.00$ A secondary, and Relay Word bit $GDEM$ asserts to logical 1. This results in SELOGIC control equation torque control setting $51GTC$ being in the state:

$$\begin{aligned} 51GTC &= !GDEM + GDEM*50G5 = \text{NOT}(GDEM) + GDEM*50G5 \\ &= \text{NOT}(\text{logical } 1) + (\text{logical } 1)*50G5 = \text{logical } 0 + 50G5 = 50G5 \end{aligned}$$

Thus, the residual ground time-overcurrent element $51GT$ operates with an effective, less-sensitive pickup:

$$50G5P = 2.30 \text{ A secondary}$$

The reduced sensitivity keeps the residual ground time-overcurrent element $51GT$ from tripping on higher unbalance current I_G .

Residual Ground Demand Current Goes Below Pickup GDEMP Again

When unbalance current I_G decreases again, unbalance demand current $I_{G(DEM)}$ follows, going below corresponding demand pickup $GDEMP = 1.00$ A secondary, and Relay Word bit $GDEM$ deasserts to logical 0. This results in SELOGIC control equation torque control setting $51GTC$ being in the state:

$$\begin{aligned} 51GTC &= !GDEM + GDEM*50G5 = \text{NOT}(GDEM) + GDEM*50G5 \\ &= \text{NOT}(\text{logical } 0) + (\text{logical } 0)*50G5 = \text{logical } 1 \end{aligned}$$

Thus, the residual ground time-overcurrent element $51GT$ operates on its standard pickup again:

$$51GP = 1.50 \text{ A secondary}$$

View or Reset Demand Metering Information

Via Serial Port

See *MET Command (Metering Data)*, MET D—Demand Metering in *Section 10: Serial Port Communications and Commands*. The MET D command displays demand and peak demand metering for the following values:

Currents	$I_{A,B,C,N}$	Input currents (A primary)
	I_G	Residual ground current (A primary; $I_G = 3I_0 = I_A + I_B + I_C$)
	$3I_2$	Negative-sequence current (A primary)
Power	$MW_{A,B,C}$	Single-phase megawatts (wye-connected voltages only)
	$MVAR_{A,B,C}$	Single-phase megavars (wye-connected voltages only)
	MW_{3P}	Three-phase megawatts
	$MVAR_{3P}$	Three-phase megavars

The MET RD command resets the demand metering values. The MET RP command resets the peak demand metering values.

Via Front Panel

The information and reset functions available via the previously discussed serial port commands MET D, MET RD, and MET RP are also available via the front-panel METER pushbutton. See Figure 11.2 in *Section 11: Front-Panel Interface*.

Demand Metering Updating and Storage

The SEL-351 Relay updates demand values approximately every 2 seconds.

The relay stores peak demand values to nonvolatile storage once per day (it overwrites the previous stored value if it is exceeded). Should the relay lose control power, it will restore the peak demand values saved by the relay at 23:50 hours on the previous day.

Demand metering updating and peak recording is momentarily suspended when SELOGIC control equation setting FAULT is asserted (= logical 1). See the explanation for the FAULT setting in the following *Maximum/Minimum Metering* subsection.

ENERGY METERING

View or Reset Energy Metering Information

Via Serial Port

See *MET Command (Metering Data)*, MET E—Energy Metering in *Section 10: Serial Port Communications and Commands*. The MET E command displays accumulated single- and three-phase megawatt and megavar hours. The MET RE command resets the accumulated single- and three-phase megawatt and megavar hours.

Via Front Panel

The information and reset functions available via the previously discussed serial port commands MET E and MET RE are also available via the front-panel METER pushbutton. See Figure 11.2 in *Section 11: Front-Panel Interface*.

Energy Metering Updating and Storage

The SEL-351 Relay updates energy values approximately every 2 seconds.

The relay stores energy values to nonvolatile storage once per day (it overwrites the previous stored value). Should the relay lose control power, it will restore the energy values saved by the relay at 23:50 hours on the previous day.

MAXIMUM/MINIMUM METERING

View or Reset Maximum/Minimum Metering Information

Via Serial Port

See *MET M—Maximum/Minimum Metering* in *Section 10: Serial Port Communications and Commands*. The MET M command displays maximum/minimum metering for the following values:

Currents	$I_{A,B,C,N}$	Input currents (A primary)
	I_G	Residual ground current (A primary; IG = 3I0)
Voltages	$V_{A,B,C}$	Input voltages (kV primary)
	V_S	Input voltage (kV primary)
Power	MW_{3P}	Three-phase megawatts (primary)
	$MVAR_{3P}$	Three-phase megavars (primary)

The MET RM command resets the maximum/minimum metering values.

The power maximum and minimum values can be negative or positive, indicating the range of power flow that has occurred since the last MET RM reset command. These functions simulate analog meter drag-hands, with the maximum value representing the upper drag-hand and the minimum value representing the lower drag-hand.

Table 8.4 shows the values that the relay would record for various power flow directions (either MW3P or MVAR3P).

Note: Previous firmware releases treated the positive and negative power values differently. See *Appendix A: Firmware Versions* for a list of previous firmware releases.

Table 8.4: Operation of Maximum/Minimum Metering With Directional Power Quantities

If Power Varies		Recorded MAX	Recorded MIN
From:	To:		
9.7	16.2	16.2	9.7
-4.2	1.4	1.4	-4.2
-25.3	-17.4	-17.4	-25.3
-6.2	27.4	27.4	-6.2

(For simplicity, the date and time stamps are not shown here.)

Via Front Panel

The metering and reset functions available via serial port commands MET M and MET RM are also available via the front-panel METER pushbutton. See Figure 11.2 in *Section 11: Front-Panel Interface*.

Maximum/Minimum Metering Update and Storage

The maximum/minimum metering function is intended to reflect normal load variations rather than fault conditions or outages. Therefore, the SEL-351 Relay updates maximum/minimum values only if SELOGIC control equation setting FAULT is deasserted (= logical 0) and has been deasserted for at least 3600 cycles.

[The factory default setting is set with time-overcurrent element pickups:

$$\text{FAULT} = 51\text{P} + 51\text{G}$$

If there is a fault, 51P or 51G asserts and blocks updating of maximum/minimum metering values.]

Note: SELOGIC control equation setting FAULT also controls other relay functions; see subsection *SELOGIC Control Equation Setting FAULT* in *Section 5: Trip and Target Logic*.

In addition to FAULT being deasserted for at least 3600 cycles, the following conditions must also be met:

- For voltage values $V_{A,B,C,S}$ the voltage is above the corresponding threshold:
 - 12.5 V secondary (150 V wye-connected voltage inputs)
 - 25.0 V secondary (300 V wye-connected voltage inputs)
- For current values $I_{A,B,C,N}$ the current is above the corresponding threshold:
 - 0.05 A secondary {5 A nominal current inputs}
 - 0.01 A secondary {1 A nominal current inputs}
 - 0.5 mA secondary {0.05 A nominal channel IN current input}
- For the residual current value I_G :
 - All three phase currents $I_{A,B,C}$ are above threshold.

- For power values MW_{3P} and $MVAR_{3P}$:
All three phase currents $I_{A,B,C}$ are above threshold and all three voltages $V_{A,B,C}$ are above threshold.
- The metering value is above the previous maximum or below the previous minimum for approximately four seconds.

The SEL-351 Relay stores maximum/minimum values to nonvolatile storage once per day and overwrites the previous stored value if that is exceeded. If the relay loses control power, it will restore the maximum/minimum values saved at 23:50 hours on the previous day.

Note: The values used by the maximum/minimum metering are the same values used by the regular MET command (serial port or instantaneous, front panel), which are eight-cycle averaged values. The maximum/minimum metering function updates every two seconds (approximately). These values should be relatively immune to transient conditions.

In previous firmware releases, the maximum/minimum metering values were based on high-speed protection voltage values. Because these values could update after being above the previous maximum or below the previous minimum for only two cycles, the maximum/minimum recorder occasionally responded to transient conditions. See *Appendix A: Firmware Versions* for a list of previous firmware releases.

LOAD PROFILE REPORT (AVAILABLE IN FIRMWARE VERSIONS 6 AND 7)

At the interval given by load profile acquisition rate setting LDAR, the relay adds a record to the load profile buffer. This record contains the time stamp, the present value of each of the analog quantities listed in the load profile list setting LDLIST and a checksum. These settings are made and reviewed with the SET R and SHO R serial port commands, respectively. Setting LDAR can be set to any of the following values: 5, 10, 15, 30, and 60 minutes. Setting LDLIST may contain any of the following labels shown below.

LABEL	QUANTITY RECORDED
IA, IB, IC, IN	Phase and neutral current magnitudes
VA, VB, VC, VS	Phase and sync voltage magnitudes
VAB, VBC, VCA	Phase-to-phase voltage magnitudes
IG, I1, 3I2, 3V0, V1, V2	Sequence current and voltage magnitudes
VDC	Battery voltage
FREQ	Phase frequency
MWA, MWB, MWC, MW3	Phase and 3 phase megawatts
MVARA, MVARB, MVARC, MVAR3	Phase and 3 phase megaVARs
PFA, PFB, PFC, PF3	Phase and 3 phase power factor
LDPFA, LDPFB, LDPFC, LDPF3	Phase and 3 phase power factor lead/lag status (0 = lag, 1 = lead)
IAD, IBDE, ICDE, INDE, IGDE, 3I2DE	Demand ammeter quantities
MWADI, MWBDI, MWCDI, MW3DI	Phase and 3 phase demand megaWATTs in
MWADO, MWBDO, MWCDO, MW3DO	Phase and 3 phase demand megaWATTs out
MVRADI, MVRBDI, MVRCDI, MVR3DI	Phase and 3 phase demand megaVARs in
MVRADO, MVRBDO, MVRCDO, MVR3DO	Phase and 3 phase demand megaVARs out
MWHAI, MWHBI, MWHCI, MWH3I	Phase and 3 phase megaWATT hours in
MWHAO, MWHBO, MWHCO, MWH3O	Phase and 3 phase megaWATT hours out
MVRHAI, MVRHBI, MVRHCI, MVRH3I	Phase and 3 phase megaVAR hours in
MVRHAO, MVRHBO, MVRHCO, MVRH3O	Phase and 3 phase megaVAR hours out

Labels are entered into the setting, either comma or space delimited, but are displayed as space delimited. Load profiling is disabled if the LDLIST setting is empty (i.e., set to NA or 0), which is displayed as LDLIST = 0. The load buffer is stored in non-volatile memory and the acquisition is synchronized to the time of day, with a resolution of ± 5 seconds. Changing the LDAR setting may result in up to two acquisition intervals before resynchronization occurs. If the LDAR setting is increased, the next acquisition time does not have a complete interval, therefore, no record is saved until the second acquisition time, which is a complete cycle. When the buffer fills up, newer records overwrite older records. The SEL-351 Relay is able to store at least 13 days of data at an LDAR of 5 minutes, if all 15 values are used. If less than 15 values are specified, the SEL-351 Relay will be able to store more days of data before data overwrite occurs. Likewise, if the interval is set longer, the SEL-351 Relay will be able to store more days of data before data overwrite occurs.

The load profile report is retrieved via the LDP command, which has the following format:

LDP [a] [b]

If the command is entered without parameters (i.e., LDP), the relay displays all records in the load buffer. If the command is entered with a single numeric parameter [a] (i.e., LDP 10), the relay displays the most recent [a] records in the buffer. If the command is entered with two numeric parameters [a] [b] (i.e., LDP 10 20), the relay displays load buffer records [a] through [b]. If the command is entered with a single data parameter [a] (i.e., LDP 7/7/96), the relay displays all load buffer records for the specified date. If the command is entered with two date parameters [a] [b] (i.e., LDP 7/7/96 8/8/96), the relay displays all load records occurring from date [a] through date [b] inclusive.

Example LDP

Serial Port

Commands

Format

LDP	If LDP is entered with no numbers following it, all available rows are displayed. They display with the oldest row at the beginning (top) of the report and the latest row (row 1) at the end (bottom) of the report. Chronological progression through the report is down the page and in descending row number.
LDP 17	If LDP is entered with a single number following it (17 in this example), the first 17 rows are displayed, if they exist. They display with the oldest row (row 17) at the beginning (top) of the report and the latest row (row 1) at the end (bottom) of the report. Chronological progression through the report is down the page and in descending row number.
LDP 10 33	If LDP is entered with two numbers following it (10 and 33 in this example; $10 < 33$), all the rows between (and including) rows 10 and 33 are displayed, if they exist. They display with the oldest row (row 33) at the beginning (top) of the report and the latest row (row 10) at the end (bottom) of the report. Chronological progression through the report is down the page and in descending row number.
LDP 47 22	If LDP is entered with two numbers following it (47 and 22 in this example; $47 > 22$), all the rows between (and including) rows 47 and 22 are displayed, if they exist. They display with the newest row (row 22) at the beginning (top) of the report and the oldest row (row 47) at the end

(bottom) of the report. Reverse chronological progression through the report is down the page and in ascending row number.

LDP 3/30/97

If LDP is entered with one date following it (date 3/30/97 in this example), all the rows on that date are displayed, if they exist. They display with the oldest row at the beginning (top) of the report and the latest row at the end (bottom) of the report, for the given date. Chronological progression through the report is down the page and in descending row number.

LDP 2/17/97 3/23/97

If LDP is entered with two dates following it (date 2/17/97 chronologically precedes date 3/23/97 in this example), all the rows between (and including) dates 2/17/97 and 3/23/97 are displayed, if they exist. They display with the oldest row (date 2/17/97) at the beginning (top) of the report and the latest row (date 3/23/97) at the end (bottom) of the report. Chronological progression through the report is down the page and in descending row number.

LDP 3/16/97 1/5/97

If LDP is entered with two dates following it (date 3/16/97 chronologically follows date 1/5/97 in this example), all the rows between (and including) dates 1/5/97 and 3/16/97 are displayed, if they exist. They display with the latest row (date 3/16/97) at the beginning (top) of the report and the oldest row (date 1/5/97) at the end (bottom) of the report. Reverse chronological progression through the report is down the page and in ascending row number.

The date entries in the above example LDP commands are dependent on the Date Format setting DATE_F. If setting DATE_F = MDY, then the dates are entered as in the above examples (Month/Day/Year). If setting DATE_F = YMD, then the dates are entered Year/Month/Day.

The load profile output has the following format:

```
-----  
=>LDP 7/23/96<ENTER>  
<STX>  
FEEDER 1                      Date: mm/dd/yy   Time: hh:mm:ss.sss  
STATION A  
  
FID=SEL-351-14-R300-V0-D990426   CID=ABCD  
  
#   DATE   TIME   label1  label2  label3  label4  label5  ... labeln  
512 07/23/96 07:00:35 xxxxx.xxx xxxxx.xxx xxxxx.xxx xxxxx.xxx xxxxx.xxx ... xxxxx.xxx  
511 07/23/96 08:00:15 xxxxx.xxx xxxxx.xxx xxxxx.xxx xxxxx.xxx xxxxx.xxx ... xxxxx.xxx  
510 07/23/96 09:00:01 xxxxx.xxx xxxxx.xxx xxxxx.xxx xxxxx.xxx xxxxx.xxx ... xxxxx.xxx  
<ETX>  
=>
```

If the requested load profile report rows do not exist, the relay responds:

No Load Profile Data

Determining the size of the Load Profile Buffer

The LDP D command displays maximum number of days of data the relay may acquire with the present settings, before data overwrite will occur.

```
=>LDP D <ENTER>  
There is room for a total of 45 days of data in the load profile buffer,  
with room for 21 days of data remaining.
```

Clearing the Load Profile Buffer

Clear the load profile report from nonvolatile memory with the LDP C command as shown in the following example:

```
=>LDP C <ENTER>  
Clear the load profile buffer  
Are you sure (Y/N) ? Y <ENTER>  
Clearing Complete
```

Changing the LDLIST setting will also result in the buffer being cleared.

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SECTION 9: SETTING THE RELAY

INTRODUCTION

Change or view settings with the SET and SHOWSET serial port commands and the front-panel SET pushbutton. Table 9.1 lists the serial port SET commands.

Table 9.1: Serial Port SET Commands

Command	Settings Type	Description	Settings Sheets*
SET n	Relay	Overcurrent and voltage elements, reclosing relay, timers, etc., for settings group n (n = 1, 2, 3, 4, 5, 6).	1-13
SET L n	Logic	SELOGIC [®] control equations for settings group n (n = 1, 2, 3, 4, 5, 6).	14-19
SET G	Global	Battery and breaker monitors, optoisolated input debounce timers, etc.	20-21
SET R	SER	Sequential Events Recorder trigger conditions and Load Profile settings.	22
SET T	Text	Front-panel default display and local control text.	23-26
SET P n	Port	Serial port settings for Serial Port n (n = 1, 2, 3, or F).	27

* located at end of this section

View settings with the respective serial port SHOWSET commands (SHO, SHO L, SHO G, SHO R, SHO T, SHO P). See *SHO Command (Showset)* in *Section 10: Serial Port Communications and Commands*.

SETTINGS CHANGES VIA THE FRONT PANEL

The relay front-panel SET pushbutton provides access to the Relay, Global, and Port settings only. Thus, the corresponding Relay, Global, and Port settings sheets that follow in this section can also be used when making these settings via the front panel. Refer to Figure 11.3 in *Section 11: Front-Panel Interface* for information on front-panel communications.

SETTINGS CHANGES VIA THE SERIAL PORT

Note: In this manual, commands you type appear in bold/uppercase: **SET**. Computer keys you press appear in bold/uppercase/brackets: **<ENTER>**.

See **Section 10: Serial Port Communications and Commands** for information on serial port communications and relay access levels. The SET commands in Table 9.1 operate at Access Level 2 (screen prompt: =>>). To change a specific setting, enter the command:

SET n m s TERSE

- where n = L, G, R, T, or P (parameter n is not entered for the Relay settings).
- m = group (1...6) or port (1...3). The relay selects the active group or port if m is not specified.
- s = the name of the specific setting you wish to jump to and begin setting. If S is not entered, the relay starts at the first setting.
- TERSE = instructs the relay to skip the SHOWSET display after the last setting. Use this parameter to speed up the SET command. If you wish to review the settings before saving, do not use the TERSE option.

When you issue the SET command, the relay presents a list of settings, one at a time. Enter a new setting, or press <ENTER> to accept the existing setting. Editing keystrokes are shown in Table 9.2.

Table 9.2: Set Command Editing Keystrokes

Press Key(s)	Results
<ENTER>	Retains setting and moves to the next setting.
^ <ENTER>	Returns to previous setting.
< <ENTER>	Returns to previous setting section.
> <ENTER>	Moves to next setting section.
END<ENTER>	Exits editing session, then prompts you to save the settings.
<CTRL> X	Aborts editing session without saving changes.

The relay checks each entry to ensure that it is within the setting range. If it is not, an “Out of Range” message is generated, and the relay prompts for the setting again.

When all the settings are entered, the relay displays the new settings and prompts for approval to enable them. Answer **Y<ENTER>** to enable the new settings. If changes are made to Global, SER, Text, or Port settings (see Table 9.1), the relay is disabled while it saves the new settings. If changes are made to the Relay or Logic settings for the active setting group (see Table 9.1), the relay is disabled while it saves the new settings. The ALARM contact closes momentarily (for “b” contact, opens for an “a”; see Figure 7.27) and the EN LED extinguishes (see Table 5.1) while the relay is disabled. The relay is disabled for about 1 second. If Logic settings are changed for the active group, the relay can be disabled for up to 15 seconds.

If changes are made to the Relay or Logic settings for a setting group other than the active setting group (see Table 9.1), the relay is not disabled while it saves the new settings. The ALARM contact closes momentarily (for “b” contact, opens for an “a”; see Figure 7.27), but the EN LED remains on (see Table 5.1) while the new settings are saved.

TIME-OVERCURRENT CURVES

The following information describes the curve timing for the curve and time dial settings made for the time-overcurrent elements (see Figures 3.14 through 3.20). The time-overcurrent relay curves in Figure 9.1 through Figure 9.10 conform to IEEE C37.112-1996 IEEE Standard Inverse-Time Characteristic Equations for Overcurrent Relays.

tp = operating time in seconds

tr = electromechanical induction-disk emulation reset time in seconds (if electromechanical reset setting is made)

TD = time dial setting

M = applied multiples of pickup current [for operating time (tp), $M > 1$; for reset time (tr), $M \leq 1$].

U.S. Moderately Inverse Curve: U1

$$\begin{aligned}tp &= TD * (0.0226 + 0.0104 / (M^{0.02} - 1)) \\tr &= TD * (1.08 / (1 - M^2))\end{aligned}$$

U.S. Inverse Curve: U2

$$\begin{aligned}tp &= TD * (0.180 + 5.95 / (M^2 - 1)) \\tr &= TD * (5.95 / (1 - M^2))\end{aligned}$$

U.S. Very Inverse Curve: U3

$$\begin{aligned}tp &= TD * (0.0963 + 3.88 / (M^2 - 1)) \\tr &= TD * (3.88 / (1 - M^2))\end{aligned}$$

U.S. Extremely Inverse Curve: U4

$$\begin{aligned}tp &= TD * (0.0352 + 5.67 / (M^2 - 1)) \\tr &= TD * (5.67 / (1 - M^2))\end{aligned}$$

U.S. Short-Time Inverse Curve: U5

$$\begin{aligned}tp &= TD * (0.00262 + 0.00342 / (M^{0.02} - 1)) \\tr &= TD * (0.323 / (1 - M^2))\end{aligned}$$

I.E.C. Class A Curve (Standard Inverse): C1

$$\begin{aligned}tp &= TD * (0.14 / (M^{0.02} - 1)) \\tr &= TD * (13.5 / (1 - M^2))\end{aligned}$$

I.E.C. Class B Curve (Very Inverse): C2

$$\begin{aligned}tp &= TD * (13.5 / (M - 1)) \\tr &= TD * (47.3 / (1 - M^2))\end{aligned}$$

I.E.C. Class C Curve (Extremely Inverse): C3

$$\begin{aligned}tp &= TD * (80.0 / (M^2 - 1)) \\tr &= TD * (80.0 / (1 - M^2))\end{aligned}$$

I.E.C. Long-Time Inverse Curve: C4

$$\begin{aligned}tp &= TD * (120.0 / (M - 1)) \\tr &= TD * (120.0 / (1 - M))\end{aligned}$$

I.E.C. Short-Time Inverse Curve: C5

$$\begin{aligned}tp &= TD * (0.05 / (M^{0.04} - 1)) \\tr &= TD * (4.85 / (1 - M^2))\end{aligned}$$

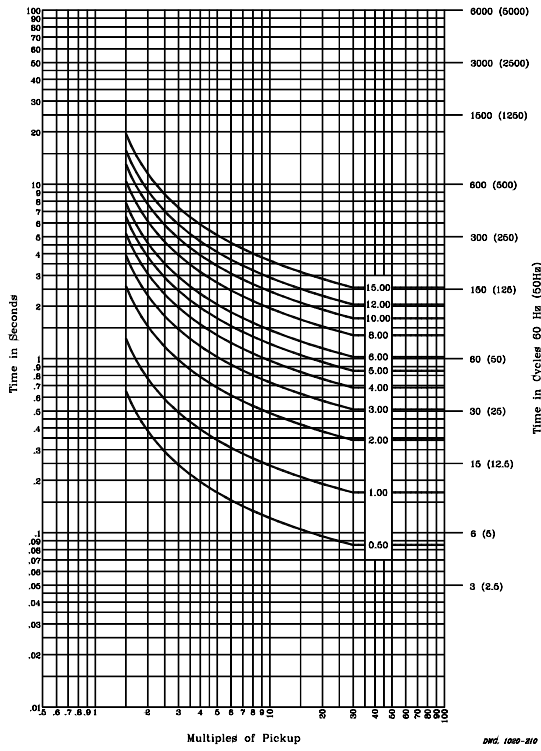


Figure 9.1: U.S. Moderately Inverse Curve: U1

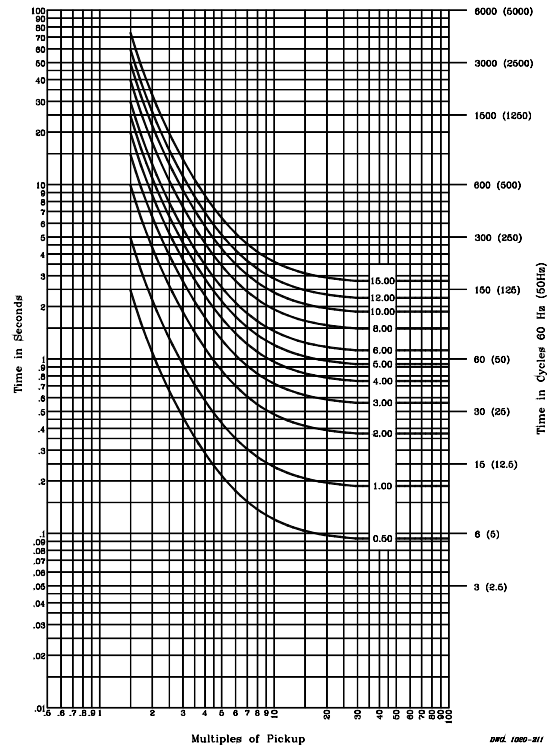


Figure 9.2: U.S. Inverse Curve: U2

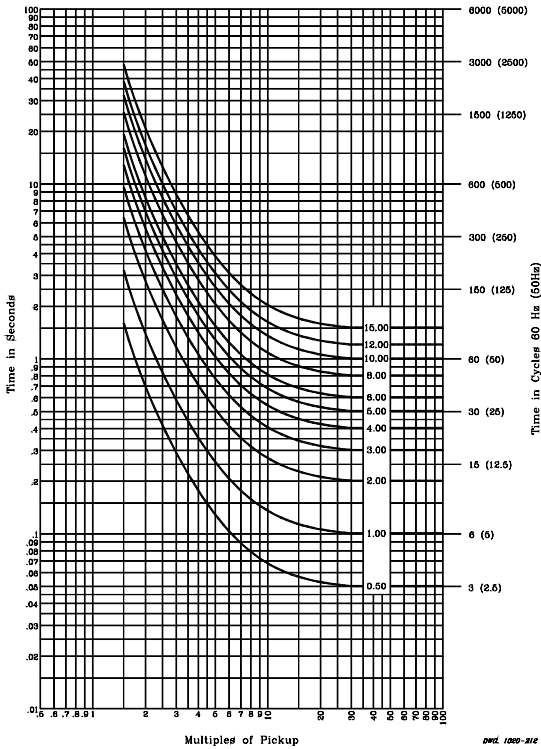


Figure 9.3: U.S. Very Inverse Curve: U3

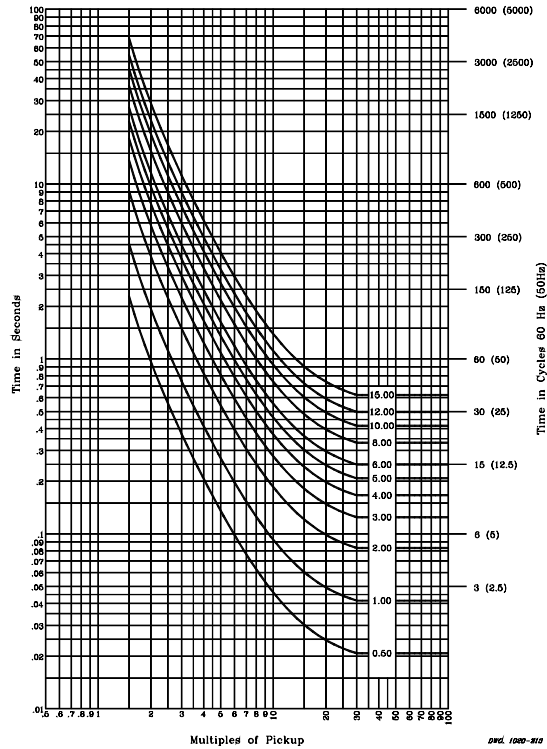


Figure 9.4: U.S. Extremely Inverse Curve: U4

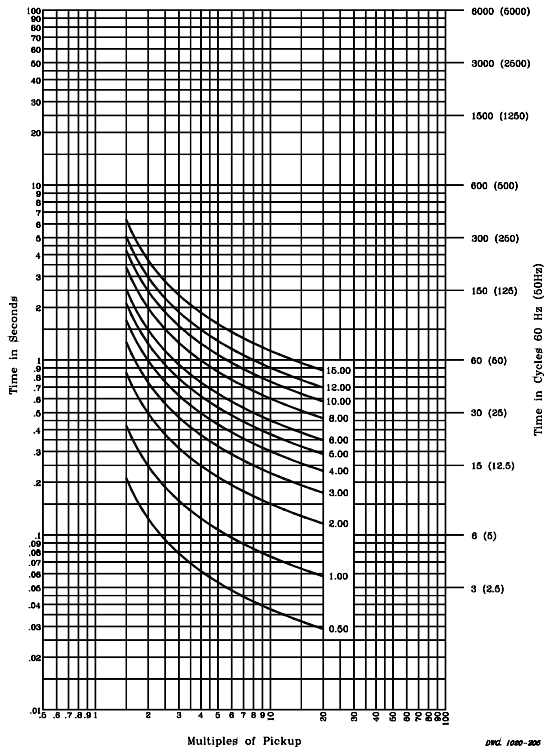


Figure 9.5: U.S. Short-Time Inverse Curve: U5

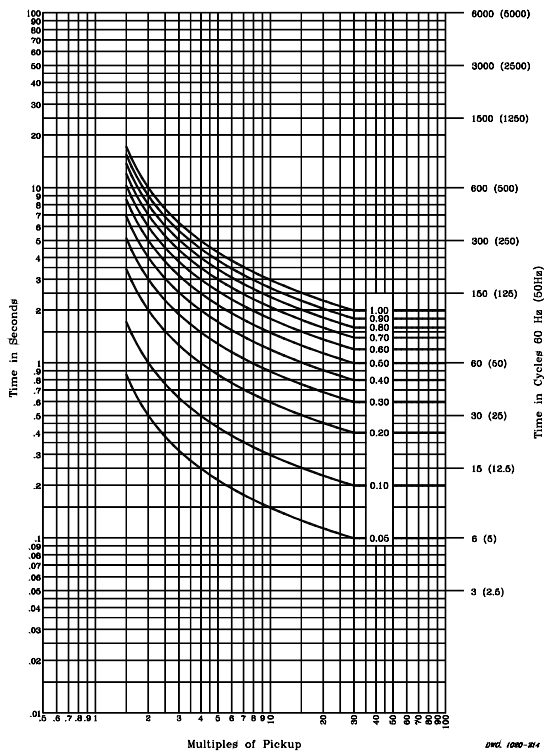


Figure 9.6: I.E.C. Class A Curve (Standard Inverse): C1

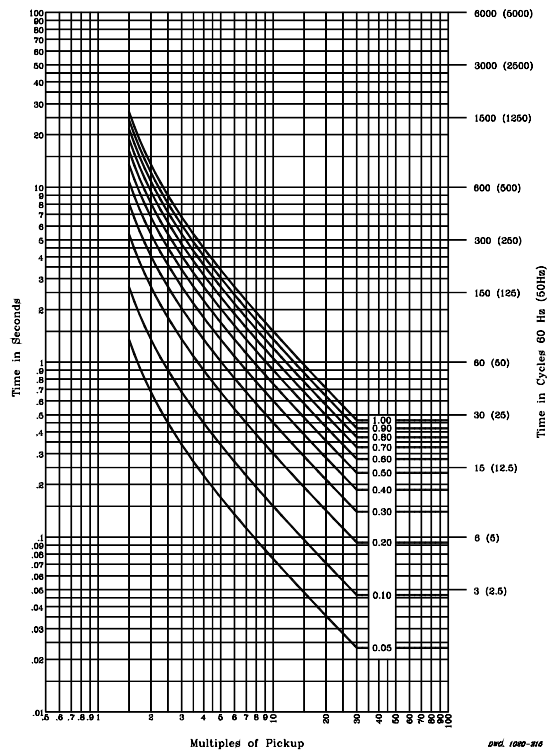


Figure 9.7: I.E.C. Class B Curve (Very Inverse): C2

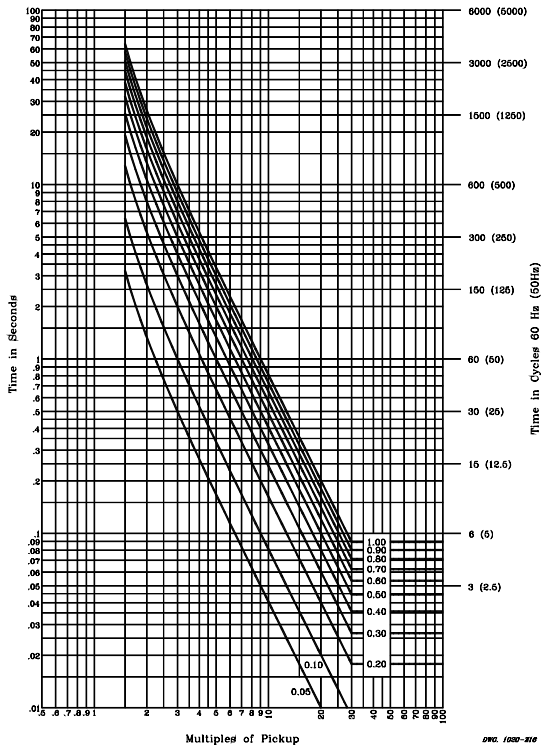


Figure 9.8: I.E.C. Class C Curve (Extremely Inverse): C3

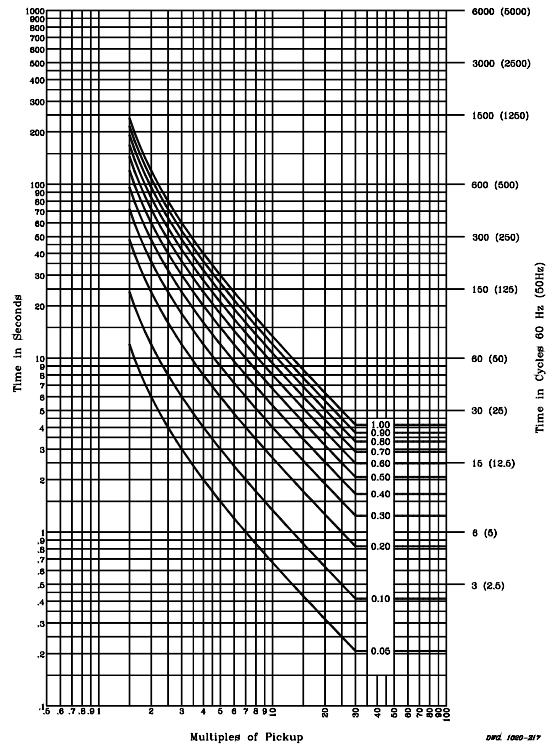


Figure 9.9: I.E.C. Long-Time Inverse Curve: C4

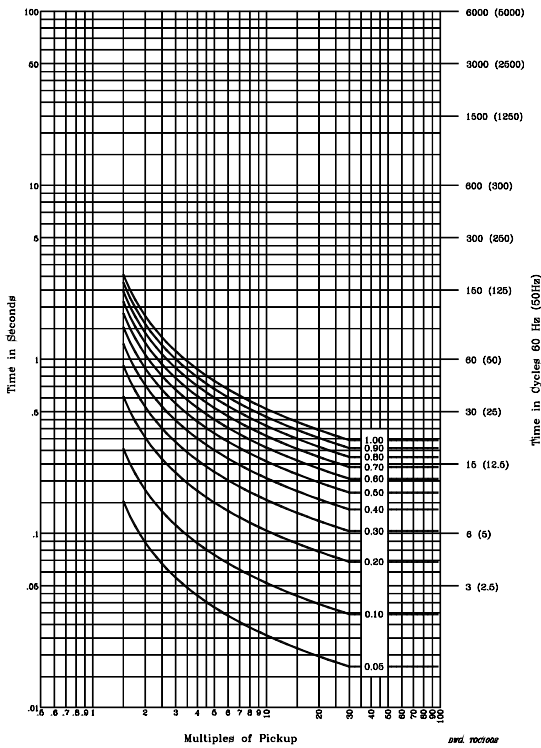


Figure 9.10: I.E.C. Short-Time Inverse Curve: C5

RELAY WORD BITS (USED IN SELOGIC CONTROL EQUATIONS)

Relay Word bits are used in SELOGIC control equation settings. Numerous SELOGIC control equation settings examples are given in *Section 3* through *Section 8*. SELOGIC control equation settings can also be set directly to 1 (logical 1) or 0 (logical 0). *Appendix G: Setting SELOGIC Control Equations* gives SELOGIC control equation details, examples, and limitations.

The Relay Word bit row numbers correspond to the row numbers used in the TAR command [see *TAR Command (Target)* in *Section 10: Serial Port Communications and Commands*]. Rows 0 and 1 are reserved for the display of the two front-panel target LED rows.

Table 9.3: SEL-351 Relay Models and Corresponding Relay Word Bit/TAR Command Reference Tables

SEL-351 Relay Model Number	Relay Word Bit Reference Tables
0351x0, 0351x1, and 0351xY, where x is the firmware version number.	Table 9.4 and Table 9.5

Table 9.4: SEL-351 Relay Models 0351x0, 0351x1, and 0351xY Relay Word Bits

Row	Relay Word Bits							
2	50A1	50B1	50C1	50A2	50B2	50C2	50A3	50B3
3	50C3	50A4	50B4	50C4	50AB1	50BC1	50CA1	50AB2
4	50BC2	50CA2	50AB3	50BC3	50CA3	50AB4	50BC4	50CA4
5	50A	50B	50C	51A	51AT	51AR	51B	51BT
6	51BR	51C	51CT	51CR	51P	51PT	51PR	51N
7	51NT	51NR	51G	51GT	51GR	51Q	51QT	51QR
8	50P1	50P2	50P3	50P4	50N1	50N2	50N3	50N4
9	67P1	67P2	67P3	67P4	67N1	67N2	67N3	67N4
10	67P1T	67P2T	67P3T	67P4T	67N1T	67N2T	67N3T	67N4T
11	50G1	50G2	50G3	50G4	50Q1	50Q2	50Q3	50Q4
12	67G1	67G2	67G3	67G4	67Q1	67Q2	67Q3	67Q4
13	67G1T	67G2T	67G3T	67G4T	67Q1T	67Q2T	67Q3T	67Q4T
14	50P5	50P6	50N5	50N6	50G5	50G6	50Q5	50Q6
15	50QF	50QR	50GF	50GR	32VE	32QGE	32IE	32QE
16	F32P	R32P	F32Q	R32Q	F32QG	R32QG	F32V	R32V
17	F32I	R32I	32PF	32PR	32QF	32QR	32GF	32GR
18	27A1	27B1	27C1	27A2	27B2	27C2	59A1	59B1
19	59C1	59A2	59B2	59C2	27AB	27BC	27CA	59AB
20	59BC	59CA	59N1	59N2	59Q	59V1	27S	59S1
21	59S2	59VP	59VS	SF	25A1	25A2	3P27	3P59
22	81D1	81D2	81D3	81D4	81D5	81D6	27B81	50L
23	81D1T	81D2T	81D3T	81D4T	81D5T	81D6T	VPOLV	LOP
24	*	*	IN106	IN105	IN104	IN103	IN102	IN101 ¹
25	LB1	LB2	LB3	LB4	LB5	LB6	LB7	LB8
26	LB9	LB10	LB11	LB12	LB13	LB14	LB15	LB16
27	RB1	RB2	RB3	RB4	RB5	RB6	RB7	RB8

Row	Relay Word Bits							
28	RB9	RB10	RB11	RB12	RB13	RB14	RB15	RB16
29	LT1	LT2	LT3	LT4	LT5	LT6	LT7	LT8
30	LT9	LT10	LT11	LT12	LT13	LT14	LT15	LT16
31	SV1	SV2	SV3	SV4	SV1T	SV2T	SV3T	SV4T
32	SV5	SV6	SV7	SV8	SV5T	SV6T	SV7T	SV8T
33	SV9	SV10	SV11	SV12	SV9T	SV10T	SV11T	SV12T
34	SV13	SV14	SV15	SV16	SV13T	SV14T	SV15T	SV16T
35	79RS	79CY	79LO	SH0	SH1	SH2	SH3	SH4
36	CLOSE	CF	RCSF	OPTMN	RSTMN	FSA	FSB	FSC
37	BCW	50P32	*	59VA	TRGTR	52A	*	*
38	SG1	SG2	SG3	SG4	SG5	SG6	ZLOUT	ZLIN
39	ZLOAD	BCWA	BCWB	BCWC	*	*	*	*
40	ALARM	OUT107	OUT106	OUT105	OUT104	OUT103	OUT102	OUT101 ²
41	3PO	SOTFE	Z3RB	KEY	EKEY	ECTT	WFC	PT
42	PTRX2	PTRX	PTRX1	UBB1	UBB2	UBB	Z3XT	DSTRT
43	NSTRT	STOP	BTX	TRIP	OC	CC	DCHI	DCLO
44	67P2S	67N2S	67G2S	67Q2S	PDEM	NDEM	GDEM	QDEM
45	OUT201	OUT202	OUT203	OUT204	OUT205	OUT206	OUT207	OUT208 ^{2,3}
46	OUT209	OUT210	OUT211	OUT212 ³	*	*	*	*
47	IN208	IN207	IN206	IN205	IN204	IN203	IN202	IN201 ^{1,3}
48	*	*	*	*	*	*	*	*
49	RMB8A	RMB7A	RMB6A	RMB5A	RMB4A	RMB3A	RMB2A	RMB1A ⁴
50	TMB8A	TMB7A	TMB6A	TMB5A	TMB4A	TMB3A	TMB2A	TMB1A
51	RMB8B	RMB7B	RMB6B	RMB5B	RMB4B	RMB3B	RMB2B	RMB1B
52	TMB8B	TMB7B	TMB6B	TMB5B	TMB4B	TMB3B	TMB2B	TMB1B

* Not used.

1 See Figure 7.1 for more information on the operation of optoisolated inputs IN101 through IN106. See Figure 7.2 for more information on the operation of optoisolated inputs IN201 through IN208.

2 All output contacts can be “a” or “b” type contacts. See Figures 2.14 and 7.27 for more information on the operation of output contacts OUT101 through ALARM. See Figures 2.15, 2.16, and 7.28 for more information on the operation of output contacts OUT201 through OUT212.

3 OUT201 through OUT212 and IN201 through IN208 only available on 0351x1 and 0351xY

4 MIRRORING™ elements only valid in Firmware Versions 6 or greater (rows 49 through 52).

**Table 9.5: Relay Word Bit Differences for SEL-351 Relay Model
0351x0, 0351x1, and 0351xY, Firmware Version 7**

Row	Relay Word Bits							
53	LBOKB	CBADB	RBADB	ROKB	LBOKA	CBADA	RBADA	ROKA
54	PWRA1	PWRB1	PWRC1	PWRA2	PWRB2	PWRC2	INTC	INT3P
55	PWRA3	PWRB3	PWRC3	PWRA4	PWRB4	PWRC4	INTA	INTB
56	SAGA	SAGB	SAGC	SAG3P	SWA	SWB	SWC	SW3P

Table 9.6: Relay Word Bit Definitions for SEL-351

Row numbers for Models 0351x0, 0351x1, and 0351xY

Row	Bit	Definition	Primary Application
2	50A1	Level 1 A-phase instantaneous overcurrent element (A-phase current above pickup setting 50P1P; see Figure 3.1)	Tripping, Control
	50B1	Level 1 B-phase instantaneous overcurrent element (B-phase current above pickup setting 50P1P; see Figure 3.1)	
	50C1	Level 1 C-phase instantaneous overcurrent element (C-phase current above pickup setting 50P1P; see Figure 3.1)	
	50A2	Level 2 A-phase instantaneous overcurrent element (A-phase current above pickup setting 50P2P; see Figure 3.1)	
	50B2	Level 2 B-phase instantaneous overcurrent element (B-phase current above pickup setting 50P2P; see Figure 3.1)	
	50C2	Level 2 C-phase instantaneous overcurrent element (C-phase current above pickup setting 50P2P; see Figure 3.1)	
	50A3	Level 3 A-phase instantaneous overcurrent element (A-phase current above pickup setting 50P3P; see Figure 3.1)	
	50B3	Level 3 B-phase instantaneous overcurrent element (B-phase current above pickup setting 50P3P; see Figure 3.1)	
3	50C3	Level 3 C-phase instantaneous overcurrent element (C-phase current above pickup setting 50P3P; see Figure 3.1)	
	50A4	Level 4 A-phase instantaneous overcurrent element (A-phase current above pickup setting 50P4P; see Figure 3.1)	
	50B4	Level 4 B-phase instantaneous overcurrent element (B-phase current above pickup setting 50P4P; see Figure 3.1)	
	50C4	Level 4 C-phase instantaneous overcurrent element (C-phase current above pickup setting 50P4P; see Figure 3.1)	

Row	Bit	Definition	Primary Application
	50AB1	Level 1 AB-phase-to-phase instantaneous overcurrent element (AB-phase-to-phase current above pickup setting 50PP1P; see Figure 3.7)	
	50BC1	Level 1 BC-phase-to-phase instantaneous overcurrent element (BC-phase-to-phase current above pickup setting 50PP1P; see Figure 3.7)	
	50CA1	Level 1 CA-phase-to-phase instantaneous overcurrent element (CA-phase-to-phase current above pickup setting 50PP1P; see Figure 3.7)	
	50AB2	Level 2 AB-phase-to-phase instantaneous overcurrent element (AB-phase-to-phase current above pickup setting 50PP2P; see Figure 3.7)	
4	50BC2	Level 2 BC-phase-to-phase instantaneous overcurrent element (BC-phase-to-phase current above pickup setting 50PP2P; see Figure 3.7)	
	50CA2	Level 2 CA-phase-to-phase instantaneous overcurrent element (CA-phase-to-phase current above pickup setting 50PP2P; see Figure 3.7)	
	50AB3	Level 3 AB-phase-to-phase instantaneous overcurrent element (AB-phase-to-phase current above pickup setting 50PP3P; see Figure 3.7)	
	50BC3	Level 3 BC-phase-to-phase instantaneous overcurrent element (BC-phase-to-phase current above pickup setting 50PP3P; see Figure 3.7)	
	50CA3	Level 3 CA-phase-to-phase instantaneous overcurrent element (CA-phase-to-phase current above pickup setting 50PP3P; see Figure 3.7)	
	50AB4	Level 4 AB-phase-to-phase instantaneous overcurrent element (AB-phase-to-phase current above pickup setting 50PP4P; see Figure 3.7)	
	50BC4	Level 4 BC-phase-to-phase instantaneous overcurrent element (BC-phase-to-phase current above pickup setting 50PP4P; see Figure 3.7)	
	50CA4	Level 4 CA-phase-to-phase instantaneous overcurrent element (CA-phase-to-phase current above pickup setting 50PP4P; see Figure 3.7)	
5	50A	50A1 + 50A2 + 50A3 + 50A4 (see Figure 3.4)	
	50B	50B1 + 50B2 + 50B3 + 50B4 (see Figure 3.4)	
	50C	50C1 + 50C2 + 50C3 + 50C4 (see Figure 3.4)	

Row	Bit	Definition	Primary Application
	51A	A-phase current above pickup setting 51AP for A-phase time-overcurrent element 51AT (see Figure 3.15)	Testing, Control
	51AT	A-phase time-overcurrent element 51AT timed out (see Figure 3.15)	Tripping
	51AR	A-phase time-overcurrent element 51AT reset (see Figure 3.15)	Testing
	51B	B-phase current above pickup setting 51BP for B-phase time-overcurrent element 51BT (see Figure 3.16)	Testing, Control
	51BT	B-phase time-overcurrent element 51BT timed out (see Figure 3.16)	Tripping
6	51BR	B-phase time-overcurrent element 51BT reset (see Figure 3.16)	Testing
	51C	C-phase current above pickup setting 51CP for C-phase time-overcurrent element 51CT (see Figure 3.17)	Testing, Control
	51CT	C-phase time-overcurrent element 51CT timed out (see Figure 3.17)	Tripping
	51CR	C-phase time-overcurrent element 51CT reset (see Figure 3.17)	Testing
	51P	Maximum phase current above pickup setting 51PP for phase time-overcurrent element 51PT (see Figure 3.14)	Testing, Control
	51PT	Phase time-overcurrent element 51PT timed out (see Figure 3.14)	Tripping
	51PR	Phase time-overcurrent element 51PT reset (see Figure 3.14)	Testing
	51N	Neutral ground current (channel IN) above pickup setting 51NP for neutral ground time-overcurrent element 51NT (see Figure 3.18)	Testing, Control
7	51NT	Neutral ground time-overcurrent element 51NT timed out (see Figure 3.18)	Tripping
	51NR	Neutral ground time-overcurrent element 51NT reset (see Figure 3.18)	Testing

Row	Bit	Definition	Primary Application
	51G	Residual ground current above pickup setting 51GP for ground time-overcurrent element 51GT (see Figure 3.19)	Testing, Control
	51GT	Residual ground time-overcurrent element 51GT timed out (see Figure 3.19)	Tripping
	51GR	Residual ground time-overcurrent element 51GT reset (see Figure 3.19)	Testing
	51Q**	Negative-sequence current above pickup setting 51QP for negative-sequence time-overcurrent element 51QT (see Figure 3.20)	Testing, Control
	51QT**	Negative-sequence time-overcurrent element 51QT timed out (see Figure 3.20)	Tripping
	51QR	Negative-sequence time-overcurrent element 51QT reset (see Figure 3.20)	Testing
8	50P1	Level 1 phase instantaneous overcurrent element (= 50A1 + 50B1 + 50C1; see Figure 3.1)	Tripping, Testing, Control
	50P2	Level 2 phase instantaneous overcurrent element (= 50A2 + 50B2 + 50C2; see Figure 3.1)	
	50P3	Level 3 phase instantaneous overcurrent element (= 50A3 + 50B3 + 50C3; see Figure 3.1)	
	50P4	Level 4 phase instantaneous overcurrent element (= 50A4 + 50B4 + 50C4; see Figure 3.1)	
	50N1	Level 1 neutral ground instantaneous overcurrent element [neutral ground current (channel IN) above pickup setting 50N1P; see Figure 3.8]	
	50N2	Level 2 neutral ground instantaneous overcurrent element [neutral ground current (channel IN) above pickup setting 50N2P; see Figure 3.8]	
	50N3	Level 3 neutral ground instantaneous overcurrent element [neutral ground current (channel IN) above pickup setting 50N3P; see Figure 3.8]	
	50N4	Level 4 neutral ground instantaneous overcurrent element [neutral ground current (channel IN) above pickup setting 50N4P; see Figure 3.8]	
9	67P1	Level 1 phase instantaneous overcurrent element (derived from 50P1; see Figure 3.3)	
	67P2	Level 2 phase instantaneous overcurrent element (derived from 50P2; see Figure 3.3)	

Row	Bit	Definition	Primary Application
	67P3	Level 3 phase instantaneous overcurrent element (derived from 50P3; see Figure 3.3)	
	67P4	Level 4 phase instantaneous overcurrent element (derived from 50P4; see Figure 3.3)	
	67N1	Level 1 neutral ground instantaneous overcurrent element (derived from 50N1; see Figure 3.8)	
	67N2	Level 2 neutral ground instantaneous overcurrent element (derived from 50N2; see Figure 3.8)	
	67N3	Level 3 neutral ground instantaneous overcurrent element (derived from 50N3; see Figure 3.8)	
	67N4	Level 4 neutral ground instantaneous overcurrent element (derived from 50N4; see Figure 3.8)	
10	67P1T	Level 1 phase definite-time overcurrent element 67P1T timed out (derived from 67P1; see Figure 3.3)	Tripping
	67P2T	Level 2 phase definite-time overcurrent element 67P2T timed out (derived from 67P2; see Figure 3.3)	
	67P3T	Level 3 phase definite-time overcurrent element 67P3T timed out (derived from 67P3; see Figure 3.3)	
	67P4T	Level 4 phase definite-time overcurrent element 67P4T timed out (derived from 67P4; see Figure 3.3)	
	67N1T	Level 1 neutral ground definite-time overcurrent element 67N1T timed out (derived from 67N1; see Figure 3.8)	
	67N2T	Level 2 neutral ground definite-time overcurrent element 67N2T timed out (derived from 67N2; see Figure 3.8)	
	67N3T	Level 3 neutral ground definite-time overcurrent element 67N3T timed out (derived from 67N3; see Figure 3.8)	
	67N4T	Level 4 neutral ground definite-time overcurrent element 67N4T timed out (derived from 67N4; see Figure 3.8)	

Row	Bit	Definition	Primary Application
11	50G1	Level 1 residual ground instantaneous overcurrent element (residual ground current above pickup setting 50G1P; see Figure 3.10)	Tripping, Testing, Control
	50G2	Level 2 residual ground instantaneous overcurrent element (residual ground current above pickup setting 50G2P; see Figure 3.10)	
	50G3	Level 3 residual ground instantaneous overcurrent element (residual ground current above pickup setting 50G3P; see Figure 3.10)	
	50G4	Level 4 residual ground instantaneous overcurrent element (residual ground current above pickup setting 50G4P; see Figure 3.10)	
	50Q1**	Level 1 negative-sequence instantaneous overcurrent element (negative-sequence current above pickup setting 50Q1P; see Figure 3.12)	Testing, Control
	50Q2**	Level 2 negative-sequence instantaneous overcurrent element (negative-sequence current above pickup setting 50Q2P; see Figure 3.12)	
	50Q3**	Level 3 negative-sequence instantaneous overcurrent element (negative-sequence current above pickup setting 50Q3P; see Figure 3.12)	
	50Q4**	Level 4 negative-sequence instantaneous overcurrent element (negative-sequence current above pickup setting 50Q4P; see Figure 3.12)	
12	67G1	Level 1 residual ground instantaneous overcurrent element (derived from 50G1; see Figure 3.10)	Tripping, Testing, Control
	67G2	Level 2 residual ground instantaneous overcurrent element (derived from 50G2; see Figure 3.10)	
	67G3	Level 3 residual ground instantaneous overcurrent element (derived from 50G3; see Figure 3.10)	
	67G4	Level 4 residual ground instantaneous overcurrent element (derived from 50G4; see Figure 3.10)	
	67Q1**	Level 1 negative-sequence instantaneous overcurrent element (derived from 50Q1; see Figure 3.12)	Testing, Control
	67Q2**	Level 2 negative-sequence instantaneous overcurrent element (derived from 50Q2; see Figure 3.12)	

Row	Bit	Definition	Primary Application
	67Q3**	Level 3 negative-sequence instantaneous overcurrent element (derived from 50Q3; see Figure 3.12)	
	67Q4**	Level 4 negative-sequence instantaneous overcurrent element (derived from 50Q4; see Figure 3.12)	
13	67G1T	Level 1 residual ground definite-time overcurrent element 67G1T timed out (derived from 67G1; see Figure 3.10)	Tripping
	67G2T	Level 2 residual ground definite-time overcurrent element 67G2T timed out (derived from 67G2; see Figure 3.10)	
	67G3T	Level 3 residual ground definite-time overcurrent element 67G3T timed out (derived from 67G3; see Figure 3.10)	
	67G4T	Level 4 residual ground definite-time overcurrent element 67G4T timed out (derived from 67G4; see Figure 3.10)	
	67Q1T**	Level 1 negative-sequence definite-time overcurrent element 67Q1T timed out (derived from 67Q1; see Figure 3.12)	
	67Q2T**	Level 2 negative-sequence definite-time overcurrent element 67Q2T timed out (derived from 67Q2; see Figure 3.12)	
	67Q3T**	Level 3 negative-sequence definite-time overcurrent element 67Q3T timed out (derived from 67Q3; see Figure 3.12)	
	67Q4T**	Level 4 negative-sequence definite-time overcurrent element 67Q4T timed out (derived from 67Q4; see Figure 3.12)	
14	50P5	Level 5 phase instantaneous overcurrent element (maximum phase current above pickup setting 50P5P; see Figure 3.2)	Tripping, Control
	50P6	Level 6 phase instantaneous overcurrent element (maximum phase current above pickup setting 50P6P; see Figure 3.2)	
	50N5	Level 5 neutral ground instantaneous overcurrent element [neutral ground current (channel IN) above pickup setting 50N5P; see Figure 3.9]	

Row	Bit	Definition	Primary Application
	50N6	Level 6 neutral ground instantaneous overcurrent element [neutral ground current (channel IN) above pickup setting 50N6P; see Figure 3.9]	
	50G5	Level 5 residual ground instantaneous overcurrent element (residual ground current above pickup setting 50G5P; see Figure 3.11)	
	50G6	Level 6 residual ground instantaneous overcurrent element (residual ground current above pickup setting 50G6P; see Figure 3.11)	
	50Q5	Level 5 negative-sequence instantaneous overcurrent element (negative-sequence current above pickup setting 50Q5P; see Figure 3.13)	Control
	50Q6	Level 6 negative-sequence instantaneous overcurrent element (negative-sequence current above pickup setting 50Q6P; see Figure 3.13)	
15	50QF	Forward direction negative-sequence overcurrent threshold exceeded (see Figures 4.4, 4.5, and 4.12)	Testing
	50QR	Reverse direction negative-sequence overcurrent threshold exceeded (see Figures 4.4, 4.5, and 4.12)	
	50GF	Forward direction residual ground overcurrent threshold exceeded (see Figures 4.4 and 4.6)	
	50GR	Reverse direction residual ground overcurrent threshold exceeded (see Figures 4.4 and 4.6)	
	32VE	Internal enable for zero-sequence voltage-polarized directional element (see Figures 4.4 and 4.6)	
	32QGE	Internal enable for negative-sequence voltage-polarized directional element (for ground; see Figures 4.4 and 4.5)	
	32IE	Internal enable for channel IN current-polarized directional element (see Figures 4.4 and 4.6)	
	32QE	Internal enable for negative-sequence voltage-polarized directional element (see Figures 4.5 and 4.13)	

Row	Bit	Definition	Primary Application
16	F32P	Forward positive-sequence voltage-polarized directional element (see Figures 4.13 and 4.15)	Testing, Special directional control schemes
	R32P	Reverse positive-sequence voltage-polarized directional element (see Figures 4.13 and 4.15)	
	F32Q	Forward negative-sequence voltage-polarized directional element (see Figures 4.13 and 4.14)	
	R32Q	Reverse negative-sequence voltage-polarized directional element (see Figures 4.13 and 4.14)	
	F32QG	Forward negative-sequence voltage-polarized directional element (for ground; see Figures 4.4 and 4.8)	
	R32QG	Reverse negative-sequence voltage-polarized directional element (for ground; see Figures 4.4 and 4.8)	
	F32V	Forward zero-sequence voltage-polarized directional element (see Figure 4.4 and 4.9)	
	R32V	Reverse zero-sequence voltage-polarized directional element (see Figure 4.4 and 4.9)	
17	F32I	Forward channel IN current-polarized directional element (see Figures 4.4 and 4.10)	
	R32I	Reverse channel IN current-polarized directional element (see Figures 4.4 and 4.10)	
	32PF	Forward directional control routed to phase overcurrent elements (see Figures 4.13 and 4.16)	
	32PR	Reverse directional control routed to phase overcurrent elements (see Figures 4.13 and 4.16)	
	32QF	Forward directional control routed to negative-sequence overcurrent elements (see Figures 4.13 and 4.16)	
	32QR	Reverse directional control routed to negative-sequence overcurrent elements (see Figures 4.13 and 4.16)	
	32GF	Forward directional control routed to neutral ground and residual ground overcurrent elements (see Figures 4.4 and 4.11)	
	32GR	Reverse directional control routed to neutral ground and residual ground overcurrent elements (see Figures 4.4 and 4.11)	

Row	Bit	Definition	Primary Application
18	27A1	A-phase instantaneous undervoltage element (A-phase voltage below pickup setting 27P1P; see Figure 3.21)	Control
	27B1	B-phase instantaneous undervoltage element (B-phase voltage below pickup setting 27P1P; see Figure 3.21)	
	27C1	C-phase instantaneous undervoltage element (C-phase voltage below pickup setting 27P1P; see Figure 3.21)	
	27A2	A-phase instantaneous undervoltage element (A-phase voltage below pickup setting 27P2P; see Figure 3.21)	
	27B2	B-phase instantaneous undervoltage element (B-phase voltage below pickup setting 27P2P; see Figure 3.21)	
	27C2	C-phase instantaneous undervoltage element (C-phase voltage below pickup setting 27P2P; see Figure 3.21)	
	59A1	A-phase instantaneous overvoltage element (A-phase voltage above pickup setting 59P1P; see Figure 3.21)	
	59B1	B-phase instantaneous overvoltage element (B-phase voltage above pickup setting 59P1P; see Figure 3.21)	
19	59C1	C-phase instantaneous overvoltage element (C-phase voltage above pickup setting 59P1P; see Figure 3.21)	
	59A2	A-phase instantaneous overvoltage element (A-phase voltage above pickup setting 59P2P; see Figure 3.21)	
	59B2	B-phase instantaneous overvoltage element (B-phase voltage above pickup setting 59P2P; see Figure 3.21)	
	59C2	C-phase instantaneous overvoltage element (C-phase voltage above pickup setting 59P2P; see Figure 3.21)	
	27AB	AB-phase-to-phase instantaneous undervoltage element (AB-phase-to-phase voltage below pickup setting 27PP; see Figure 3.22)	

Row	Bit	Definition	Primary Application
	27BC	BC-phase-to-phase instantaneous undervoltage element (BC-phase-to-phase voltage below pickup setting 27PP; see Figure 3.22)	
	27CA	CA-phase-to-phase instantaneous undervoltage element (CA-phase-to-phase voltage below pickup setting 27PP; see Figure 3.22)	
	59AB	AB-phase-to-phase instantaneous overvoltage element (AB-phase-to-phase voltage above pickup setting 59PP; see Figure 3.22)	
20	59BC	BC-phase-to-phase instantaneous overvoltage element (BC-phase-to-phase voltage above pickup setting 59PP; see Figure 3.22)	
	59CA	CA-phase-to-phase instantaneous overvoltage element (CA-phase-to-phase voltage above pickup setting 59PP; see Figure 3.22)	
	59N1	Zero-sequence instantaneous overvoltage element (zero-sequence voltage above pickup setting 59N1P; see Figure 3.22)	
	59N2	Zero-sequence instantaneous overvoltage element (zero-sequence voltage above pickup setting 59N2P; see Figure 3.22)	
	59Q	Negative-sequence instantaneous overvoltage element (negative-sequence voltage above pickup setting 59QP; see Figure 3.22)	
	59V1	Positive-sequence instantaneous overvoltage element (positive-sequence voltage above pickup setting 59V1P; see Figure 3.22)	
	27S	Channel VS instantaneous undervoltage element (channel VS voltage below pickup setting 27SP; see Figure 3.23)	
	59S1	Channel VS instantaneous overvoltage element (channel VS voltage above pickup setting 59S1P; see Figure 3.23)	
21	59S2	Channel VS instantaneous overvoltage element (channel VS voltage above pickup setting 59S2P; see Figure 3.23)	
	59VP	Phase voltage window element [selected phase voltage (VP) between threshold settings 25VLO and 25VHI; see Figure 3.24]	Testing

Row	Bit	Definition	Primary Application
	59VS	Channel VS voltage window element (channel VS voltage between threshold settings 25VLO and 25VHI; see Figure 3.24)	
	SF	Slip frequency between voltages VP and VS less than setting 25SF (see Figure 3.24)	
	25A1	Synchronism check element (see Figure 3.25)	Control
	25A2	Synchronism check element (see Figure 3.25)	
	3P27	27A1 * 27B1 * 27C1 (see Figure 3.21)	
	3P59	59A1 * 59B1 * 59C1 (see Figure 3.21)	
22	81D1	Level 1 instantaneous frequency element (with corresponding pickup setting 81D1P; see Figure 3.28)	Testing
	81D2	Level 2 instantaneous frequency element (with corresponding pickup setting 81D2P; see Figure 3.28)	
	81D3	Level 3 instantaneous frequency element (with corresponding pickup setting 81D3P; see Figure 3.28)	
	81D4	Level 4 instantaneous frequency element (with corresponding pickup setting 81D4P; see Figure 3.28)	
	81D5	Level 5 instantaneous frequency element (with corresponding pickup setting 81D5P; see Figure 3.28)	
	81D6	Level 6 instantaneous frequency element (with corresponding pickup setting 81D6P; see Figure 3.28)	
	27B81	Undervoltage element for frequency element blocking (any phase voltage below pickup setting 27B81P; see Figure 3.27)	
	50L	Phase instantaneous overcurrent element for load detection (maximum phase current above pickup setting 50LP; see Figure 5.3)	
23	81D1T	Level 1 definite-time frequency element 81D1T timed out (derived from 81D1; see Figure 3.28)	Tripping, Control
	81D2T	Level 2 definite-time frequency element 81D2T timed out (derived from 81D2; see Figure 3.28)	

Row	Bit	Definition	Primary Application
	81D3T	Level 3 definite-time frequency element 81D3T timed out (derived from 81D3; see Figure 3.28)	
	81D4T	Level 4 definite-time frequency element 81D4T timed out (derived from 81D4; see Figure 3.28)	
	81D5T	Level 5 definite-time frequency element 81D5T timed out (derived from 81D5; see Figure 3.28)	
	81D6T	Level 6 definite-time frequency element 81D6T timed out (derived from 81D6; see Figure 3.28)	
	VPOLV	Positive-sequence polarization voltage valid (see Figure 4.15)	
	LOP	Loss-of-potential (see Figure 4.1)	Testing, Special directional control schemes
24	*		
	*		
	IN106	Optoisolated input IN106 asserted (see Figure 7.1)	Circuit breaker status, Control via optoisolated inputs
	IN105	Optoisolated input IN105 asserted (see Figure 7.1)	
	IN104	Optoisolated input IN104 asserted (see Figure 7.1)	
	IN103	Optoisolated input IN103 asserted (see Figure 7.1)	
	IN102	Optoisolated input IN102 asserted (see Figure 7.1)	
IN101	Optoisolated input IN101 asserted (see Figure 7.1)		
25	LB1	Local Bit 1 asserted (see Figure 7.4)	Control via front panel—replacing traditional panel-mounted control switches
	LB2	Local Bit 2 asserted (see Figure 7.4)	
	LB3	Local Bit 3 asserted (see Figure 7.4)	
	LB4	Local Bit 4 asserted (see Figure 7.4)	
	LB5	Local Bit 5 asserted (see Figure 7.4)	
	LB6	Local Bit 6 asserted (see Figure 7.4)	
	LB7	Local Bit 7 asserted (see Figure 7.4)	
	LB8	Local Bit 8 asserted (see Figure 7.4)	
26	LB9	Local Bit 9 asserted (see Figure 7.4)	Control via front panel—replacing traditional panel-mounted control switches
	LB10	Local Bit 10 asserted (see Figure 7.4)	
	LB11	Local Bit 11 asserted (see Figure 7.4)	
	LB12	Local Bit 12 asserted (see Figure 7.4)	
	LB13	Local Bit 13 asserted (see Figure 7.4)	
	LB14	Local Bit 14 asserted (see Figure 7.4)	
	LB15	Local Bit 15 asserted (see Figure 7.4)	
	LB16	Local Bit 16 asserted (see Figure 7.4)	

Row	Bit	Definition	Primary Application
27	RB1 RB2 RB3 RB4 RB5 RB6 RB7 RB8	Remote Bit 1 asserted (see Figure 7.10) Remote Bit 2 asserted (see Figure 7.10) Remote Bit 3 asserted (see Figure 7.10) Remote Bit 4 asserted (see Figure 7.10) Remote Bit 5 asserted (see Figure 7.10) Remote Bit 6 asserted (see Figure 7.10) Remote Bit 7 asserted (see Figure 7.10) Remote Bit 8 asserted (see Figure 7.10)	Control via serial port
28	RB9 RB10 RB11 RB12 RB13 RB14 RB15 RB16	Remote Bit 9 asserted (see Figure 7.10) Remote Bit 10 asserted (see Figure 7.10) Remote Bit 11 asserted (see Figure 7.10) Remote Bit 12 asserted (see Figure 7.10) Remote Bit 13 asserted (see Figure 7.10) Remote Bit 14 asserted (see Figure 7.10) Remote Bit 15 asserted (see Figure 7.10) Remote Bit 16 asserted (see Figure 7.10)	Control via serial port
29	LT1 LT2 LT3 LT4 LT5 LT6 LT7 LT8	Latch Bit 1 asserted (see Figure 7.12) Latch Bit 2 asserted (see Figure 7.12) Latch Bit 3 asserted (see Figure 7.12) Latch Bit 4 asserted (see Figure 7.12) Latch Bit 5 asserted (see Figure 7.12) Latch Bit 6 asserted (see Figure 7.12) Latch Bit 7 asserted (see Figure 7.12) Latch Bit 8 asserted (see Figure 7.12)	Control—replacing traditional latching relays
30	LT9 LT10 LT11 LT12 LT13 LT14 LT15 LT16	Latch Bit 9 asserted (see Figure 7.12) Latch Bit 10 asserted (see Figure 7.12) Latch Bit 11 asserted (see Figure 7.12) Latch Bit 12 asserted (see Figure 7.12) Latch Bit 13 asserted (see Figure 7.12) Latch Bit 14 asserted (see Figure 7.12) Latch Bit 15 asserted (see Figure 7.12) Latch Bit 16 asserted (see Figure 7.12)	Control—replacing traditional latching relays

Row	Bit	Definition	Primary Application
31	SV1	SELOGIC control equation variable timer input SV1 asserted (see Figure 7.24)	Testing, Seal-in functions, etc. (see Figure 7.27)
	SV2	SELOGIC control equation variable timer input SV2 asserted (see Figure 7.24)	
	SV3	SELOGIC control equation variable timer input SV3 asserted (see Figure 7.24)	
	SV4	SELOGIC control equation variable timer input SV4 asserted (see Figure 7.24)	
	SV1T	SELOGIC control equation variable timer output SV1T asserted (see Figure 7.24)	Control
	SV2T	SELOGIC control equation variable timer output SV2T asserted (see Figure 7.24)	
	SV3T	SELOGIC control equation variable timer output SV3T asserted (see Figure 7.24)	
	SV4T	SELOGIC control equation variable timer output SV4T asserted (see Figure 7.24)	
32	SV5	SELOGIC control equation variable timer input SV5 asserted (see Figure 7.24)	Testing, Seal-in functions, etc. (see Figure 7.27)
	SV6	SELOGIC control equation variable timer input SV6 asserted (see Figure 7.24)	
	SV7	SELOGIC control equation variable timer input SV7 asserted (see Figure 7.25)	
	SV8	SELOGIC control equation variable timer input SV8 asserted (see Figure 7.25)	
	SV5T	SELOGIC control equation variable timer output SV5T asserted (see Figure 7.24)	Control
	SV6T	SELOGIC control equation variable timer output SV6T asserted (see Figure 7.24)	
	SV7T	SELOGIC control equation variable timer output SV7T asserted (see Figure 7.25)	
	SV8T	SELOGIC control equation variable timer output SV8T asserted (see Figure 7.25)	
33	SV9	SELOGIC control equation variable timer input SV9 asserted (see Figure 7.25)	Testing, Seal-in functions, etc. (see Figure 7.27)
	SV10	SELOGIC control equation variable timer input SV10 asserted (see Figure 7.25)	
	SV11	SELOGIC control equation variable timer input SV11 asserted (see Figure 7.25)	
	SV12	SELOGIC control equation variable timer input SV12 asserted (see Figure 7.25)	

Row	Bit	Definition	Primary Application
	SV9T	SELOGIC control equation variable timer output SV9T asserted (see Figure 7.25)	Control
	SV10T	SELOGIC control equation variable timer output SV10T asserted (see Figure 7.25)	
	SV11T	SELOGIC control equation variable timer output SV11T asserted (see Figure 7.25)	
	SV12T	SELOGIC control equation variable timer output SV12T asserted (see Figure 7.25)	
34	SV13	SELOGIC control equation variable timer input SV13 asserted (see Figure 7.25)	Testing, Seal-in functions, etc. (see Figure 7.27)
	SV14	SELOGIC control equation variable timer input SV14 asserted (see Figure 7.25)	
	SV15	SELOGIC control equation variable timer input SV15 asserted (see Figure 7.25)	
	SV16	SELOGIC control equation variable timer input SV16 asserted (see Figure 7.25)	
	SV13T	SELOGIC control equation variable timer output SV13T asserted (see Figure 7.25)	Control
	SV14T	SELOGIC control equation variable timer output SV14T asserted (see Figure 7.25)	
	SV15T	SELOGIC control equation variable timer output SV15T asserted (see Figure 7.25)	
	SV16T	SELOGIC control equation variable timer output SV16T asserted (see Figure 7.25)	
35	79RS	Reclosing relay in the Reset State (see Figure 6.5 and Table 6.1)	
	79CY	Reclosing relay in the Reclose Cycle State (see Figure 6.5 and Table 6.1)	
	79LO	Reclosing relay in the Lockout State (see Figure 6.5 and Table 6.1)	
	SH0	Reclosing relay shot counter = 0 (see Table 6.3)	
	SH1	Reclosing relay shot counter = 1 (see Table 6.3)	
	SH2	Reclosing relay shot counter = 2 (see Table 6.3)	
	SH3	Reclosing relay shot counter = 3 (see Table 6.3)	
SH4	Reclosing relay shot counter = 4 (see Table 6.3)		

Row	Bit	Definition	Primary Application
36	CLOSE	Close logic output asserted (see Figure 6.1)	Output contact assignment
	CF	Close Failure condition (asserts for 1/4 cycle; see Figure 6.1)	Indication
	RCSF	Reclose supervision failure (asserts for 1/4 cycle; see Figure 6.2)	
	OPTMN	Open interval timer is timing (see <i>Reclosing Relay</i> in <i>Section 6: Close and Reclose Logic</i>)	Testing
	RSTMN	Reset timer is timing (see <i>Reclosing Relay</i> in <i>Section 6: Close and Reclose Logic</i>)	
	FSA	A-phase fault identification logic output used in A-phase targeting (see <i>Front-Panel Target LEDs</i> in <i>Section 5: Trip and Target Logic</i>)	Control
FSB	B-phase fault identification logic output used in B-phase targeting (see <i>Front-Panel Target LEDs</i> in <i>Section 5: Trip and Target Logic</i>)		
FSC	C-phase fault identification logic output used in C-phase targeting (see <i>Front-Panel Target LEDs</i> in <i>Section 5: Trip and Target Logic</i>)		
37	BCW	BCWA + BCWB + BCWC	Indication
	50P32	Three-phase overcurrent threshold exceeded (see Figure 4.15)	Testing
	* 59VA	Channel VA voltage window element [channel VA voltage between threshold settings 25VLO and 25VHI; see Figure 3.24]	
	TRGTR	Target Reset. TRGTR pulses to logical 1 for one processing interval when either the TARGET RESET Pushbutton is pushed or the TAR R (Target Reset) serial port command is executed (see Figures 5.1 and 5.17)	Control
	52A * *	Circuit breaker status (asserts to logical 1 when circuit breaker is closed; see Figure 6.1)	Indication
38	SG1	Setting group 1 active (see Table 7.3)	Indication
	SG2	Setting group 2 active (see Table 7.3)	
	SG3	Setting group 3 active (see Table 7.3)	

Row	Bit	Definition	Primary Application
	SG4	Setting group 4 active (see Table 7.3)	
	SG5	Setting group 5 active (see Table 7.3)	
	SG6	Setting group 6 active (see Table 7.3)	
	ZLOUT	Load encroachment “load out” element (see Figure 4.2)	
	ZLIN	Load encroachment “load in” element (see Figure 4.2)	Special phase overcurrent element control
39	ZLOAD	ZLOUT + ZLIN (see Figure 4.2)	Indication
	BCWA	A-phase breaker contact wear has reached 100% wear level (see <i>Breaker Monitor in Section 8: Breaker Monitor, Metering, and Load Profile Functions</i>)	
	BCWB	B-phase breaker contact wear has reached 100% wear level (see <i>Breaker Monitor in Section 8: Breaker Monitor, Metering, and Load Profile Functions</i>)	
	BCWC	C-phase breaker contact wear has reached 100% wear level (see <i>Breaker Monitor in Section 8: Breaker Monitor, Metering, and Load Profile Functions</i>)	
	* * * *		
40	ALARM	ALARM output contact indicating that relay failed or PULSE ALARM command executed (see Figure 7.27)	
	OUT107	Output contact OUT107 asserted (see Figure 7.27)	
	OUT106	Output contact OUT106 asserted (see Figure 7.27)	
	OUT105	Output contact OUT105 asserted (see Figure 7.27)	
	OUT104	Output contact OUT104 asserted (see Figure 7.27)	
	OUT103	Output contact OUT103 asserted (see Figure 7.27)	
	OUT102	Output contact OUT102 asserted (see Figure 7.27)	
	OUT101	Output contact OUT101 asserted (see Figure 7.27)	

Row	Bit	Definition	Primary Application	
41	3PO	Three pole open condition (see Figure 5.3)	Testing	
	SOTFE	Switch-onto-fault condition (see Figure 5.3)		
	Z3RB	Zone (level) 3 reverse block (see Figure 5.6)		
	KEY	Key permissive trip signal start (see Figure 5.6)		
	EKEY	Echo key (see Figure 5.6)		
	ECTT	Echo conversion to trip condition (see Figure 5.6)		
	WFC	Weak infeed condition (see Figure 5.6)		
	PT	Permissive trip signal to POTT logic (see Figure 5.5)		
42	PTRX2	Permissive trip 2 signal from DCUB logic (see Figure 5.10)		
	PTRX	Permissive trip signal to Trip logic (see Figure 5.7)		
	PTRX1	Permissive trip 2 signal from DCUB logic (see Figure 5.10)		
	UBB1	Unblocking block 1 from DCUB logic (see Figure 5.10)		
	UBB2	Unblocking block 2 from DCUB logic (see Figure 5.10)		
	UBB	Unblocking block to Trip logic (see Figure 5.11)		
	Z3XT	Logic output from zone (level) 3 extension timer (see Figure 5.14)		
	DSTRT	Directional carrier start (see Figure 5.14)		
43	NSTRT	Nondirectional carrier start (see Figure 5.14)		
	STOP	Carrier stop (see Figure 5.14)		
	BTX	Block trip input extension (see Figure 5.14)		
	TRIP	Trip logic output asserted (see Figure 5.1)		Output contact assignment
	OC***	Asserts 1/4 cycle for Open Command execution (see the Note following Figure 5.2 and the Note in the <i>Lockout State</i> discussion, following Table 6.1)		Testing
	CC***	Asserts 1/4 cycle for Close Command execution (see the Note in the <i>Set Close</i> discussion, following Figure 6.1)		

Row	Bit	Definition	Primary Application
	DCHI	Station dc battery instantaneous overvoltage element (see Figure 8.9)	Indication
	DCLO	Station dc battery instantaneous undervoltage element (see Figure 8.9)	
44	67P2S	Level 2 directional phase definite-time (short delay) overcurrent element 67P2S timed out (derived from 67P2; see Figures 3.3 and 5.14)	Tripping in DCB schemes
	67N2S	Level 2 directional neutral ground definite-time (short delay) overcurrent element 67N2S timed out (derived from 67N2; see Figures 3.8 and 5.14)	
	67G2S	Level 2 directional residual ground definite-time (short delay) overcurrent element 67G2S timed out (derived from 67G2; see Figures 3.10 and 5.14)	
	67Q2S	Level 2 directional negative-sequence definite-time (short delay) overcurrent element 67Q2S timed out (derived from 67Q2; see Figures 3.12 and 5.14)	
	PDEM	Phase demand current above pickup setting PDEMP (see Figure 8.13)	Indication
	NDEM	Neutral ground demand current above pickup setting NDEMP (see Figure 8.13)	
	GDEM	Residual ground demand current above pickup setting GDEMP (see Figure 8.13)	
	QDEM	Negative-sequence demand current above pickup setting QDEMP (see Figure 8.13)	
45	OUT201	Output contact OUT201 asserted (see Figure 7.28)	
	OUT202	Output contact OUT202 asserted (see Figure 7.28)	
	OUT203	Output contact OUT203 asserted (see Figure 7.28)	
	OUT204	Output contact OUT204 asserted (see Figure 7.28)	
	OUT205	Output contact OUT205 asserted (see Figure 7.28)	
	OUT206	Output contact OUT206 asserted (see Figure 7.28)	
	OUT207	Output contact OUT207 asserted (see Figure 7.28)	
	OUT208	Output contact OUT208 asserted (see Figure 7.28)	
46	OUT209	Output contact OUT209 asserted (see Figure 7.28)	
	OUT210	Output contact OUT210 asserted (see Figure 7.28)	
	OUT211	Output contact OUT211 asserted (see Figure 7.28)	
	OUT212	Output contact OUT212 asserted (see Figure 7.28)	

Row	Bit	Definition	Primary Application
	* * * *		
47	IN208 IN207 IN206 IN205 IN204 IN203 IN202 IN201	Optoisolated input IN208 asserted (see Figure 7.2) Optoisolated input IN208 asserted (see Figure 7.2) Optoisolated input IN206 asserted (see Figure 7.2) Optoisolated input IN205 asserted (see Figure 7.2) Optoisolated input IN204 asserted (see Figure 7.2) Optoisolated input IN203 asserted (see Figure 7.2) Optoisolated input IN202 asserted (see Figure 7.2) Optoisolated input IN201 asserted (see Figure 7.2)	Circuit breaker status, Control via optoisolated inputs
48	* * * * * * * *		
49	RMB8A RMB7A RMB6A RMB5A RMB4A RMB3A RMB2A RMB1A	Channel A, received bit 8 Channel A, received bit 7 Channel A, received bit 6 Channel A, received bit 5 Channel A, received bit 4 Channel A, received bit 3 Channel A, received bit 2 Channel A, received bit 1	(only operable in Firmware Versions 6, 7)
50	TMB8A TMB7A TMB6A TMB5A TMB4A TMB3A TMB2A TMB1A	Channel A, transmit bit 8 Channel A, transmit bit 7 Channel A, transmit bit 6 Channel A, transmit bit 5 Channel A, transmit bit 4 Channel A, transmit bit 3 Channel A, transmit bit 2 Channel A, transmit bit 1	

Row	Bit	Definition	Primary Application
51	RMB8B	Channel B, received bit 8	
	RMB7B	Channel B, received bit 7	
	RMB6B	Channel B, received bit 6	
	RMB5B	Channel B, received bit 5	
	RMB4B	Channel B, received bit 4	
	RMB3B	Channel B, received bit 3	
	RMB2B	Channel B, received bit 2	
	RMB1B	Channel B, received bit 1	
52	TMB8B	Channel B, transmit bit 8	
	TMB7B	Channel B, transmit bit 7	
	TMB6B	Channel B, transmit bit 6	
	TMB5B	Channel B, transmit bit 5	
	TMB4B	Channel B, transmit bit 4	
	TMB3B	Channel B, transmit bit 3	
	TMB2B	Channel B, transmit bit 2	
	TMB1B	Channel B, transmit bit 1	
53	LBOKB	Channel B, looped back ok	
	CBADB	Channel B, channel unavailability over threshold	
	RBADB	Channel B, outage duration over threshold	
	ROKB	Channel B, received data ok	
	LBOKA	Channel A, looped back ok	
	CBADA	Channel A, channel unavailability over threshold	
	RBADA	Channel A, outage duration over threshold	
	ROKA	Channel A, received data ok	

Row	Bit	Definition	Primary Application
54	PWRA1 PWRB1 PWRC1 PWRA2 PWRB2 PWRC2	Level 1 A-phase power element Level 1 B-phase power element Level 1 C-phase power element Level 2 A-phase power element Level 2 B-phase power element Level 2 C-phase power element	Tripping, Control (only operable in Firmware Version 7)
	INTC INT3P	C-phase interruption element 3-phase interruption element	Sag/Swell/Int reporting (only operable in Firmware Version 7)
55	PWRA3 PWRB3 PWRC3 PWRA4 PWRB4 PWRC4	Level 3 A-phase power element Level 3 B-phase power element Level 3 C-phase power element Level 4 A-phase power element Level 4 B-phase power element Level 4 C-phase power element	Tripping, Control (only operable in Firmware Version 7)
	INTA INTB	A-phase voltage interruption element B-phase voltage interruption element	Sag/Swell/Int reporting
56	SAGA SAGB SAGC SAG3P SWA SWB SWC SW3P	A-phase voltage sag element B-phase voltage sag element C-phase voltage sag element 3-phase voltage sag element A-phase voltage swell element B-phase voltage swell element C-phase voltage swell element 3-phase voltage swell element	(only operable in Firmware Version 7)

* Not used.

** **IMPORTANT:** See *Appendix F* for special instructions on setting negative-sequence overcurrent elements.

*** The Open Command (Relay Word bit OC) and Close Command (Relay Word bit CC) are not embedded in the Trip Logic (see Figure 5.1) and Close Logic (see Figure 6.1), respectively. See the Note following Figure 5.2 and the Note in the *Lockout State* discussion, following Table 6.1, concerning the OC Relay Word bit (OPEN command). See the Note in the *Set Close* discussion, following Figure 6.1, concerning the CC Relay Word bit (CLOSE command).

SETTINGS EXPLANATIONS

Note that most of the settings in the settings sheets that follow include references for additional information. The following explanations are for settings that do not have reference information anywhere else in the instruction manual.

Identifier Labels

Refer to Settings Sheet 1 of 27.

The SEL-351 Relay has two identifier labels: the Relay Identifier (RID) and the Terminal Identifier (TID). The Relay Identifier is typically used to identify the relay or the type of protection scheme. Typical Terminal Identifiers include an abbreviation of the substation name and line terminal.

The relay tags each report (event report, meter report, etc.) with the Relay Identifier and Terminal Identifier. This allows you to distinguish the report as one generated for a specific breaker and substation.

RID and TID settings may include the following characters: 0-9, A-Z, -, /, ., space. These two settings cannot be made via the front-panel interface.

Current Transformer Ratios

Refer to Settings Sheet 1 of 27.

Phase and neutral current transformer ratios are set independently. If IN is connected residually with IA, IB, and IC, then set CTR and CTRN the same.

For sensitive earth fault (SEF) applications (channel IN rated 0.05 A nominal), some thought might be given to making the CTRN setting artificially high, to view small channel IN currents in the event report. For example if CTRN = 10000, then 5 mA secondary into channel IN appears as 50 A primary in the event report ($0.005 \times 10000 = 50$). Channel IN metering values are likewise affected. All the neutral ground overcurrent elements operate off secondary current values, so the CTRN setting has no affect on their operation.

Line Settings

Refer to Settings Sheet 1 of 27.

Line impedance settings Z1MAG, Z1ANG, Z0MAG, and Z0ANG are used in the fault locator (see *Fault Location* in **Section 12: Standard Event Reports, Sag/Swell/Interruption Report, and SER**) and in automatically making directional element settings Z2F, Z2R, Z0F, and Z0R (see *Settings Made Automatically* in **Section 4: Loss-of-Potential Logic, Load Encroachment, and Directional Element Logic**). A corresponding line length setting (LL) is also used in the fault locator.

The line impedance settings Z1MAG, Z1ANG, Z0MAG, and Z0ANG are set in Ω secondary. Line impedance (Ω primary) is converted to Ω secondary:

$$\Omega \text{ primary} \triangleright (\text{CTR/PTR}) = \Omega \text{ secondary}$$

where:

CTR = phase (IA, IB, IC) current transformer ratio

PTR = phase (VA, VB, VC) potential transformer ratio (wye-connected)

Line length setting LL is unitless and corresponds to the line impedance settings. For example, if a particular line length is 15 miles, enter the line impedance values (Ω secondary) and then enter the corresponding line length:

LL = 15.00 (miles)

If this length of line is measured in kilometers rather than miles, then enter:

LL = 24.14 (kilometers)

Enable Settings

Refer to Settings Sheets 1, 2, and 21 of 27.

The enable settings on Settings Sheets 1 and 2 (E50P through EDEM) control the settings that follow, through Sheet 11. Enable setting EBMON on Settings Sheet 21 controls the settings that immediately follow it. This helps limit the number of settings that need to be made.

Each setting subgroup on Settings Sheets 2 through 12 has a reference back to the controlling enable setting. For example, the neutral ground time-overcurrent element settings on Sheet 5 (settings 51NP through 51NRS) are controlled by enable setting E51N.

Other System Parameters

Refer to Settings Sheet 20 of 27.

The global settings NFREQ and PHROT allow you to configure the SEL-351 Relay to your specific system.

Set NFREQ equal to your nominal power system frequency, either 50 Hz or 60 Hz.

Set PHROT equal to your power system phase rotation, either ABC or ACB.

Set DATE_F to format the date displayed in relay reports and the front-panel display. Set DATE_F to MDY to display dates in Month/Day/Year format; set DATE_F to YMD to display dates in Year/Month/Day format.

SETTINGS SHEETS

The settings sheets that follow include the definition and input range for each setting in the relay. Refer to *Relay Element Pickup Ranges and Accuracies* in **Section 1: Introduction and Specifications** for information on 5 A nominal and 1 A nominal ordering options and how they influence overcurrent element setting ranges.

SETTINGS SHEET
FOR THE SEL-351-5, -6, -7 RELAY
RELAY SETTINGS (SERIAL PORT COMMAND SET AND FRONT PANEL)

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Date _____

Identifier Labels (See *Settings Explanations* in Section 9)

Relay Identifier (30 characters) RID = _____
Terminal Identifier (30 characters) TID = _____

Current and Potential Transformer Ratios (See *Settings Explanations* in Section 9)

Phase (IA, IB, IC) Current Transformer Ratio (1–6000) CTR = _____
Neutral (IN) Current Transformer Ratio (1–10000) CTRN = _____
Phase (VA, VB, VC; wye-connected)
Potential Transformer Ratio (1.00–10000.00) PTR = _____
Synchronism Voltage (VS) Potential Transformer Ratio (1.00–10000.00) PTRS = _____

Line Settings (See *Settings Explanations* in Section 9)

Positive-sequence line impedance magnitude Z1MAG = _____
(0.05–255.00 Ω secondary {150 V voltage inputs; 5 A nom.})
(0.25–1275.00 Ω secondary {150 V voltage inputs; 1 A nom.})
(0.10–510.00 Ω secondary {300 V voltage inputs; 5 A nom.})
(0.50–2550.00 Ω secondary {300 V voltage inputs; 1 A nom.})
Positive-sequence line impedance angle (40.00–90.00 degrees) Z1ANG = _____
Zero-sequence line impedance magnitude Z0MAG = _____
(0.05–255.00 Ω secondary {150 V voltage inputs; 5 A nom.})
(0.25–1275.00 Ω secondary {150 V voltage inputs; 1 A nom.})
(0.10–510.00 Ω secondary {300 V voltage inputs; 5 A nom.})
(0.50–2550.00 Ω secondary {300 V voltage inputs; 1 A nom.})
Zero-sequence line impedance angle (40.00–90.00 degrees) Z0ANG = _____
Line length (0.10–999.00, unitless) LL = _____

Instantaneous/Definite-Time Overcurrent Enable Settings

Phase element levels (N, 1–6) (see Figures 3.1, 3.2, 3.3, and 3.7) E50P = _____
Neutral ground element levels—channel IN (N, 1–6) E50N = _____
(see Figures 3.8 and 3.9)
Residual ground element levels (N, 1–6) (see Figures 3.10 and 3.11) E50G = _____
Negative-sequence element levels (N, 1–6) (see Figures 3.12 and 3.13) E50Q = _____

Time-Overcurrent Enable Settings

Phase elements (N, 1, 2) (see Table 3.1, Figures 3.14, 3.15, 3.16, and 3.17) E51P = _____
Neutral ground elements—channel IN (Y, N) (see Figure 3.18) E51N = _____
Residual ground elements (Y, N) (see Figure 3.19) E51G = _____
Negative-sequence elements (Y, N) (see Figure 3.20) E51Q = _____

SETTINGS SHEET
FOR THE SEL-351-5, -6, -7 RELAY
RELAY SETTINGS (SERIAL PORT COMMAND SET AND FRONT PANEL)

Other Enable Settings

Directional control (Y, AUTO, N) (see <i>Directional Control Settings</i> in <i>Section 4</i>)	E32= _____
Load encroachment (Y, N) (see Figure 4.2)	ELOAD= _____
Switch-onto-fault (Y, N) (see Figure 5.3)	ESOTF= _____
Voltage elements (Y, N) (see Figures 3.21, 3.22, and 3.23)	EVOLT= _____
Synchronism check (Y, N) (see Figures 3.24 and 3.25)	E25= _____
Fault location (Y, N) (see Table 12.1 and <i>Fault Location</i> in <i>Section 12</i>)	EFLOC= _____
Loss-of-potential (Y, Y1, N) (see Figure 4.1)	ELOP= _____
Communications-assisted trip scheme (N, DCB, POTT, DCUB1, DCUB2) (see <i>Communications-Assisted Trip Logic—General Overview</i> in <i>Section 5</i>)	ECOMM= _____
Frequency elements (N, 1–6) (see Figure 3.28)	E81= _____
Reclosures (N, 1–4) (see <i>Reclosing Relay</i> in <i>Section 6</i>)	E79= _____
SELOGIC [®] Control Equation Variable Timers (N, 1–16) (see Figures 7.24 and 7.25)	ESV= _____
Demand Metering (THM = Thermal, ROL = Rolling) (see Figure 8.11)	EDEM= _____
Power element levels (N, 1–4) (only available in Firmware Version 7)	EPWR= _____
Voltage Sag/Swell/Interruption (Y, N) (only available in Firmware Version 7) (see Figures 3.29, 3.30, and 3.31)	ESSI= _____

Phase Inst./Def.-Time Overcurrent Elements (See Figures 3.1, 3.2, and 3.3)

(Number of phase element pickup settings dependent on preceding enable setting E50P = 1–6)

Pickup (OFF, 0.25–100.00 A {5 A nom.}, 0.05–20.00 A {1 A nom.})	50P1P = _____
Pickup (OFF, 0.25–100.00 A {5 A nom.}, 0.05–20.00 A {1 A nom.})	50P2P = _____
Pickup (OFF, 0.25–100.00 A {5 A nom.}, 0.05–20.00 A {1 A nom.})	50P3P = _____
Pickup (OFF, 0.25–100.00 A {5 A nom.}, 0.05–20.00 A {1 A nom.})	50P4P = _____
Pickup (OFF, 0.25–100.00 A {5 A nom.}, 0.05–20.00 A {1 A nom.})	50P5P = _____
Pickup (OFF, 0.25–100.00 A {5 A nom.}, 0.05–20.00 A {1 A nom.})	50P6P = _____

Phase Definite-Time Overcurrent Elements (See Figure 3.3)

(Number of phase element time delay settings dependent on preceding enable setting E50P = 1–6; all four time delay settings are enabled if E50P ≥ 4)

Time delay (0.00–16000.00 cycles in 0.25-cycle steps)	67P1D = _____
Time delay (0.00–16000.00 cycles in 0.25-cycle steps)	67P2D = _____
Time delay (0.00–16000.00 cycles in 0.25-cycle steps)	67P3D = _____
Time delay (0.00–16000.00 cycles in 0.25-cycle steps)	67P4D = _____

SETTINGS SHEET
FOR THE SEL-351-5, -6, -7 RELAY
RELAY SETTINGS (SERIAL PORT COMMAND SET AND FRONT PANEL)

Phase-to-Phase Instantaneous Overcurrent Elements (See Figure 3.7)

(Number of phase-to-phase element pickup settings dependent on preceding enable setting E50P = 1–6; all four pickup settings are enabled if E50P ≥ 4)

Pickup (OFF, 1.00–170.00 A {5 A nom.}, 0.20–34.00 A {1 A nom.})	50PP1P = _____
Pickup (OFF, 1.00–170.00 A {5 A nom.}, 0.20–34.00 A {1 A nom.})	50PP2P = _____
Pickup (OFF, 1.00–170.00 A {5 A nom.}, 0.20–34.00 A {1 A nom.})	50PP3P = _____
Pickup (OFF, 1.00–170.00 A {5 A nom.}, 0.20–34.00 A {1 A nom.})	50PP4P = _____

Neutral Ground Inst./Def.-Time Overcurrent Elements–Channel IN (See Figures 3.8 and 3.9)

(Number of neutral ground element pickup settings dependent on preceding enable setting E50N = 1–6)

Pickup (OFF, 0.250–100.000 A {5 A nom.}, 0.050–20.000 A {1 A nom.}, 0.005–1.500A {0.05 A nom.})	50N1P = _____
Pickup (OFF, 0.250–100.000 A {5 A nom.}, 0.050–20.000 A {1 A nom.}, 0.005–1.500A {0.05 A nom.})	50N2P = _____
Pickup (OFF, 0.250–100.000 A {5 A nom.}, 0.050–20.000 A {1 A nom.}, 0.005–1.500A {0.05 A nom.})	50N3P = _____
Pickup (OFF, 0.250–100.000 A {5 A nom.}, 0.050–20.000 A {1 A nom.}, 0.005–1.500A {0.05 A nom.})	50N4P = _____
Pickup (OFF, 0.250–100.000 A {5 A nom.}, 0.050–20.000 A {1 A nom.}, 0.005–1.500A {0.05 A nom.})	50N5P = _____
Pickup (OFF, 0.250–100.000 A {5 A nom.}, 0.050–20.000 A {1 A nom.}, 0.005–1.500A {0.05 A nom.})	50N6P = _____

Neutral Ground Definite-Time Overcurrent Elements (See Figure 3.8)

(Number of neutral ground element time delay settings dependent on preceding enable setting E50N = 1–6; all four time delay settings are enabled if E50N ≥ 4)

Time delay (0.00–16000.00 cycles in 0.25-cycle steps)	67N1D = _____
Time delay (0.00–16000.00 cycles in 0.25-cycle steps)	67N2D = _____
Time delay (0.00–16000.00 cycles in 0.25-cycle steps)	67N3D = _____
Time delay (0.00–16000.00 cycles in 0.25-cycle steps)	67N4D = _____

Residual Ground Inst./Def.-Time Overcurrent Elements (See Figures 3.10 and 3.11)

(Number of residual ground element pickup settings dependent on preceding enable setting E50G = 1–6)

Pickup (OFF, 0.25–100.00 A {5 A nom.}, 0.05–20.00 A {1 A nom.})	50G1P = _____
Pickup (OFF, 0.25–100.00 A {5 A nom.}, 0.05–20.00 A {1 A nom.})	50G2P = _____
Pickup (OFF, 0.25–100.00 A {5 A nom.}, 0.05–20.00 A {1 A nom.})	50G3P = _____
Pickup (OFF, 0.25–100.00 A {5 A nom.}, 0.05–20.00 A {1 A nom.})	50G4P = _____
Pickup (OFF, 0.25–100.00 A {5 A nom.}, 0.05–20.00 A {1 A nom.})	50G5P = _____
Pickup (OFF, 0.25–100.00 A {5 A nom.}, 0.05–20.00 A {1 A nom.})	50G6P = _____

SETTINGS SHEET
FOR THE SEL-351-5, -6, -7 RELAY
RELAY SETTINGS (SERIAL PORT COMMAND SET AND FRONT PANEL)

Residual Ground Definite-Time Overcurrent Elements (See Figure 3.10)

(Number of residual ground element time delay settings dependent on preceding enable setting
E50G = 1–6; all four time delay settings are enabled if E50G ≥ 4)

Time delay (0.00–16000.00 cycles in 0.25-cycle steps)	67G1D = _____
Time delay (0.00–16000.00 cycles in 0.25-cycle steps)	67G2D = _____
Time delay (0.00–16000.00 cycles in 0.25-cycle steps)	67G3D = _____
Time delay (0.00–16000.00 cycles in 0.25-cycle steps)	67G4D = _____

Negative-Sequence Inst./Def.-Time Overcurrent Elements (See Figures 3.12 and 3.13)*

(Number of negative-sequence element time delay settings dependent on preceding enable setting
E50Q = 1–6)

Pickup (OFF, 0.25–100.00 A {5 A nom.}, 0.05–20.00 A {1 A nom.})	50Q1P = _____
Pickup (OFF, 0.25–100.00 A {5 A nom.}, 0.05–20.00 A {1 A nom.})	50Q2P = _____
Pickup (OFF, 0.25–100.00 A {5 A nom.}, 0.05–20.00 A {1 A nom.})	50Q3P = _____
Pickup (OFF, 0.25–100.00 A {5 A nom.}, 0.05–20.00 A {1 A nom.})	50Q4P = _____
Pickup (OFF, 0.25–100.00 A {5 A nom.}, 0.05–20.00 A {1 A nom.})	50Q5P = _____
Pickup (OFF, 0.25–100.00 A {5 A nom.}, 0.05–20.00 A {1 A nom.})	50Q6P = _____

Negative-Sequence Definite-Time Overcurrent Elements (See Figure 3.12)*

(Number of negative-sequence element time delay settings dependent on preceding enable setting
E50Q = 1–6; all four time delay settings are enabled if E50Q ≥ 4)

Time delay (0.00–16000.00 cycles in 0.25-cycle steps)	67Q1D = _____
Time delay (0.00–16000.00 cycles in 0.25-cycle steps)	67Q2D = _____
Time delay (0.00–16000.00 cycles in 0.25-cycle steps)	67Q3D = _____
Time delay (0.00–16000.00 cycles in 0.25-cycle steps)	67Q4D = _____

* **IMPORTANT:** See *Appendix F* for information on setting negative-sequence overcurrent elements.

Phase Time-Overcurrent Element (See Figure 3.14)

(Make the following settings if preceding enable setting E51P = 1 or 2)

Pickup (OFF, 0.50–16.00 A {5 A nom.}, 0.10–3.20 A {1 A nom.})	51PP = _____
Curve (U1–U5, C1–C5; see Figures 9.1 through 9.10)	51PC = _____
Time-Dial (0.50–15.00 for curves U1–U5, 0.05–1.00 for curves C1–C5)	51PTD = _____
Electromechanical Reset (Y, N)	51PRS = _____

SETTINGS SHEET
FOR THE SEL-351-5, -6, -7 RELAY
RELAY SETTINGS (SERIAL PORT COMMAND SET AND FRONT PANEL)

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Date _____

A-Phase Time-Overcurrent Element (See Figure 3.15)

(Make the following settings if preceding enable setting E51P = 2)

Pickup (OFF, 0.50–16.00 A {5 A nom.}, 0.10–3.20 A {1 A nom.}) 51AP = _____

Curve (U1–U5, C1–C5; see Figures 9.1 through 9.10) 51AC = _____

Time-Dial (0.50–15.00 for curves U1–U5, 0.05–1.00 for curves C1–C5) 51ATD = _____

Electromechanical Reset (Y, N) 51ARS = _____

B-Phase Time-Overcurrent Element (See Figure 3.16)

(Make the following settings if preceding enable setting E51P = 2)

Pickup (OFF, 0.50–16.00 A {5 A nom.}, 0.10–3.20 A {1 A nom.}) 51BP = _____

Curve (U1–U5, C1–C5; see Figures 9.1 through 9.10) 51BC = _____

Time-Dial (0.50–15.00 for curves U1–U5, 0.05–1.00 for curves C1–C5) 51BTD = _____

Electromechanical Reset (Y, N) 51BRS = _____

C-Phase Time-Overcurrent Element (See Figure 3.17)

(Make the following settings if preceding enable setting E51P = 2)

Pickup (OFF, 0.50–16.00 A {5 A nom.}, 0.10–3.20 A {1 A nom.}) 51CP = _____

Curve (U1–U5, C1–C5; see Figures 9.1 through 9.10) 51CC = _____

Time-Dial (0.50–15.00 for curves U1–U5, 0.05–1.00 for curves C1–C5) 51CTD = _____

Electromechanical Reset (Y, N) 51CRS = _____

Neutral Ground Time-Overcurrent Element–Channel IN (See Figure 3.18)

(Make the following settings if preceding enable setting E51N = Y)

Pickup (OFF, 0.500–16.000 A {5 A nom.}, 0.100–3.200 A {1 A nom.},
0.005–0.160 A {0.05 A nom.}) 51NP = _____

Curve (U1–U5, C1–C5; see Figures 9.1 through 9.10) 51NC = _____

Time-Dial (0.50–15.00 for curves U1–U5, 0.05–1.00 for curves C1–C5) 51NTD = _____

Electromechanical Reset (Y, N) 51NRS = _____

Residual Ground Time-Overcurrent Element (See Figure 3.19)

(Make the following settings if preceding enable setting E51G = Y)

Pickup (OFF, 0.50–16.00 A {5 A nom.}, 0.10–3.20 A {1 A nom.}) 51GP = _____

Curve (U1–U5, C1–C5; see Figures 9.1 through 9.10) 51GC = _____

Time-Dial (0.50–15.00 for curves U1–U5, 0.05–1.00 for curves C1–C5) 51GTD = _____

Electromechanical Reset (Y, N) 51GRS = _____

SETTINGS SHEET
FOR THE SEL-351-5, -6, -7 RELAY
RELAY SETTINGS (SERIAL PORT COMMAND SET AND FRONT PANEL)

Negative-Sequence Time-Overcurrent Element (See Figure 3.20)*

(Make the following settings if preceding enable setting E51Q = Y)

Pickup (OFF, 0.50–16.00 A {5 A nom.}, 0.10–3.20 A {1 A nom.}) 51QP = _____

Curve (U1–U5, C1–C5; see Figures 9.1 through 9.10) 51QC = _____

Time-Dial (0.50–15.00 for curves U1–U5, 0.05–1.00 for curves C1–C5) 51QTD = _____

Electromechanical Reset (Y, N) 51QRS = _____

* **IMPORTANT:** See *Appendix F* for information on setting negative-sequence overcurrent elements.

Load-Encroachment Elements (See Figure 4.2)

(Make the following settings if preceding enable setting ELOAD = Y)

Forward load impedance ZLF = _____

(0.05–64.00 Ω secondary {150 V voltage inputs; 5 A nom.})

(0.25–320.00 Ω secondary {150 V voltage inputs; 1 A nom.})

(0.10–128.00 Ω secondary {300 V voltage inputs; 5 A nom.})

(0.50–640.00 Ω secondary {300 V voltage inputs; 1 A nom.})

Reverse load impedance ZLR = _____

(0.05–64.00 Ω secondary {150 V voltage inputs; 5 A nom.})

(0.25–320.00 Ω secondary {150 V voltage inputs; 1 A nom.})

(0.10–128.00 Ω secondary {300 V voltage inputs; 5 A nom.})

(0.50–640.00 Ω secondary {300 V voltage inputs; 1 A nom.})

Positive forward load angle (-90.00° to +90.00°) PLAF = _____

Negative forward load angle (-90.00° to +90.00°) NLAF = _____

Positive reverse load angle (+90.00° to +270.00°) PLAR = _____

Negative reverse load angle (+90.00° to +270.00°) NLAR = _____

Directional Elements (See *Directional Control Settings* in Section 4)

(Make settings DIR1–DIR4 and ORDER if preceding enable setting E32 = Y or AUTO)

Level 1 direction: Forward, Reverse, None (F, R, N) DIR1 = _____

Level 2 direction: Forward, Reverse, None (F, R, N) DIR2 = _____

Level 3 direction: Forward, Reverse, None (F, R, N) DIR3 = _____

Level 4 direction: Forward, Reverse, None (F, R, N) DIR4 = _____

Ground directional element priority: combination of Q, V, I - or OFF ORDER = _____

(If channel IN is rated 0.05 A nominal, then setting option “I” is not available for setting ORDER.)

(Make setting 50P32P if preceding enable settings E32 = Y or AUTO and ELOAD = N)

Phase directional element 3-phase current pickup 50P32P = _____

(0.50–10.00 A {5 A nom.}, 0.10–2.00 A {1 A nom.})

(Make settings Z2F, Z2R, 50QFP, 50QRP, a2 and k2 if preceding enable setting E32 = Y. If E32 = AUTO, these settings are made automatically)

SETTINGS SHEET
FOR THE SEL-351-5, -6, -7 RELAY
RELAY SETTINGS (SERIAL PORT COMMAND SET AND FRONT PANEL)

Forward directional Z2 threshold Z2F = _____
 (-64.00–64.00 Ω secondary {150 V voltage inputs; 5 A nom.})

(-320.00–320.00 Ω secondary {150 V voltage inputs; 1 A nom.})

(-128.00–128.00 Ω secondary {300 V voltage inputs; 5 A nom.})

(-640.00–640.00 Ω secondary {300 V voltage inputs; 1 A nom.})

Reverse directional Z2 threshold Z2R = _____

(-64.00–64.00 Ω secondary {150 V voltage inputs; 5 A nom.})

(-320.00–320.00 Ω secondary {150 V voltage inputs; 1 A nom.})

(-128.00–128.00 Ω secondary {300 V voltage inputs; 5 A nom.})

(-640.00–640.00 Ω secondary {300 V voltage inputs; 1 A nom.})

Forward directional negative-sequence current pickup 50QFP = _____
 (0.25–5.00 A {5 A nom.}, 0.05–1.00 A {1 A nom.})

Reverse directional negative-sequence current pickup 50QRP = _____
 (0.25–5.00 A {5 A nom.}, 0.05–1.00 A {1 A nom.})

Positive-sequence current restraint factor, I2/I1 (0.02–0.50, unitless) a2 = _____

Zero-sequence current restraint factor, I2/I0 (0.10–1.20, unitless) k2 = _____

(Make settings 50GFP, 50GRP, and a0 if preceding enable setting E32 = Y and preceding setting ORDER contains V or I. If E32 = AUTO and ORDER contains V or I, these settings are made automatically.)

Forward directional residual ground pickup 50GFP = _____
 (0.25–5.00 A {5 A nom.}, 0.05–1.00 A {1 A nom.})

Reverse directional residual ground pickup 50GRP = _____
 (0.25–5.00A {5 A nom.}, 0.05–1.00 A {1 A nom.})

Positive-sequence current restraint factor, I0/I1 (0.02–0.50, unitless) a0 = _____

(Make settings Z0F and Z0R if preceding enable setting E32 = Y and preceding setting ORDER contains V. If E32 = AUTO and ORDER contains V, these settings are made automatically)

Forward directional Z0 threshold Z0F = _____
 (-64.00–64.00 Ω secondary {150 V voltage inputs; 5 A nom.})

(-320.00–320.00 Ω secondary {150 V voltage inputs; 1 A nom.})

(-128.00–128.00 Ω secondary {300 V voltage inputs; 5 A nom.})

(-640.00–640.00 Ω secondary {300 V voltage inputs; 1 A nom.})

Reverse directional Z0 threshold Z0R = _____

(-64.00–64.00 Ω secondary {150 V voltage inputs; 5 A nom.})

(-320.00–320.00 Ω secondary {150 V voltage inputs; 1 A nom.})

(-128.00–128.00 Ω secondary {300 V voltage inputs; 5 A nom.})

(-640.00–640.00 Ω secondary {300 V voltage inputs; 1 A nom.})

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FOR THE SEL-351-5, -6, -7 RELAY
RELAY SETTINGS (SERIAL PORT COMMAND SET AND FRONT PANEL)

Voltage Elements (See Figures 3.21, 3.22, and 3.23)

(Make the following settings if preceding enable setting EVOLT =Y)

- | | |
|---|---------------|
| Phase undervoltage pickup
(OFF, 0.0–150.0 V secondary {150 V voltage inputs})
(OFF, 0.0–300.0 V secondary {300 V voltage inputs}) | 27P1P = _____ |
| Phase undervoltage pickup
(OFF, 0.0–150.0 V secondary {150 V voltage inputs})
(OFF, 0.0–300.0 V secondary {300 V voltage inputs}) | 27P2P = _____ |
| Phase overvoltage pickup
(OFF, 0.0–150.0 V secondary {150 V voltage inputs})
(OFF, 0.0–300.0 V secondary {300 V voltage inputs}) | 59P1P = _____ |
| Phase overvoltage pickup
(OFF, 0.0–150.0 V secondary {150 V voltage inputs})
(OFF, 0.0–300.0 V secondary {300 V voltage inputs}) | 59P2P = _____ |
| Zero-sequence (3V0) overvoltage pickup
(OFF, 0.0–150.0 V secondary {150 V voltage inputs})
(OFF, 0.0–300.0 V secondary {300 V voltage inputs}) | 59N1P = _____ |
| Zero-sequence (3V0) overvoltage pickup
(OFF, 0.0–150.0 V secondary {150 V voltage inputs})
(OFF, 0.0–300.0 V secondary {300 V voltage inputs}) | 59N2P = _____ |
| Negative-sequence (V2) overvoltage pickup
(OFF, 0.0–100.0 V secondary {150 V voltage inputs})
(OFF, 0.0–200.0 V secondary {300 V voltage inputs}) | 59QP = _____ |
| Positive-sequence (V1) overvoltage pickup
(OFF, 0.0–150.0 V secondary {150 V voltage inputs})
(OFF, 0.0–300.0 V secondary {300 V voltage inputs}) | 59V1P = _____ |
| Channel VS undervoltage pickup
(OFF, 0.0–150.0 V secondary {150 V voltage inputs})
(OFF, 0.0–300.0 V secondary {300 V voltage inputs}) | 27SP = _____ |
| Channel VS overvoltage pickup
(OFF, 0.0–150.0 V secondary {150 V voltage inputs})
(OFF, 0.0–300.0 V secondary {300 V voltage inputs}) | 59S1P = _____ |
| Channel VS overvoltage pickup
(OFF, 0.0–150.0 V secondary {150 V voltage inputs})
(OFF, 0.0–300.0 V secondary {300 V voltage inputs}) | 59S2P = _____ |
| Phase-to-phase undervoltage pickup
(OFF, 0.0–260.0 V secondary {150 V voltage inputs})
(OFF, 0.0–520.0 V secondary {300 V voltage inputs}) | 27PP = _____ |
| Phase-to-phase overvoltage pickup
(OFF, 0.0–260.0 V secondary {150 V voltage inputs})
(OFF, 0.0–520.0 V secondary {300 V voltage inputs}) | 59PP = _____ |

SETTINGS SHEET
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RELAY SETTINGS (SERIAL PORT COMMAND SET AND FRONT PANEL)

Synchronism Check Elements (See Figures 3.24 and 3.25)

(Make the following settings if preceding enable setting E25 = Y)

Voltage window—low threshold (0.00–150.00 V secondary, 150 V wye-connected voltage inputs; 0.00–300.00 V secondary, 300 V wye-connected voltage inputs;)	25VLO = _____
Voltage window—high threshold (0.00–150.00 V secondary, 150 V wye-connected voltage inputs; 0.00–300.00 V secondary, 300 V wye-connected voltage inputs;)	25VHI = _____
Maximum slip frequency (0.005–0.500 Hz)	25SF = _____
Maximum angle 1 (0.00°–80.00°)	25ANG1 = _____
Maximum angle 2 (0.00°–80.00°)	25ANG2 = _____
Synchronizing phase (VA, VB, VC or 0.00° to 330.00° in 30° steps; degree option is for VS not in phase with VA, VB, or VC—set with respect to VS constantly lagging VA)	SYNCP = _____
Breaker close time for angle compensation (0.00–60.00 cycles in 0.25-cycle steps)	TCLOSD = _____

Frequency Element (See Figures 3.27 and 3.28)

(Make the following settings if preceding enable setting E81 = 1–6)

Phase undervoltage block (12.50–150.00 V secondary, 150 V wye-connected voltage inputs; 25.00–300.00 V secondary, 300 V wye-connected voltage inputs;)	27B81P = _____
Level 1 pickup (OFF, 40.10–65.00 Hz)	81D1P = _____
Level 1 time delay (2.00–16000.00 cycles in 0.25-cycle steps)	81D1D = _____
Level 2 pickup (OFF, 40.10–65.00 Hz)	81D2P = _____
Level 2 time delay (2.00–16000.00 cycles in 0.25-cycle steps)	81D2D = _____
Level 3 pickup (OFF, 40.10–65.00 Hz)	81D3P = _____
Level 3 time delay (2.00–16000.00 cycles in 0.25-cycle steps)	81D3D = _____
Level 4 pickup (OFF, 40.10–65.00 Hz)	81D4P = _____
Level 4 time delay (2.00–16000.00 cycles in 0.25-cycle steps)	81D4D = _____
Level 5 pickup (OFF, 40.10–65.00 Hz)	81D5P = _____
Level 5 time delay (2.00–16000.00 cycles in 0.25-cycle steps)	81D5D = _____
Level 6 pickup (OFF, 40.10–65.00 Hz)	81D6P = _____
Level 6 time delay (2.00–16000.00 cycles in 0.25-cycle steps)	81D6D = _____

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RELAY SETTINGS (SERIAL PORT COMMAND SET AND FRONT PANEL)

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Reclosing Relay (See Tables 6.2 and 6.3)

(Make the following settings if preceding enable setting E79 = 1–4)

Open interval 1 time (0.00–999999.00 cycles in 0.25-cycle steps) 79OI1 = _____

Open interval 2 time (0.00–999999.00 cycles in 0.25-cycle steps) 79OI2 = _____

Open interval 3 time (0.00–999999.00 cycles in 0.25-cycle steps) 79OI3 = _____

Open interval 4 time (0.00–999999.00 cycles in 0.25-cycle steps) 79OI4 = _____

Reset time from reclose cycle (0.00–999999.00 cycles in 0.25-cycle steps) 79RSD = _____

Reset time from lockout (0.00–999999.00 cycles in 0.25-cycle steps) 79RSLD = _____

Reclose supervision time limit (OFF, 0.00–999999.00 cycles in 0.25-cycle steps) (set 79CLSD = 0.00 for most applications; see Figure 6.2) 79CLSD = _____

Switch-Onto-Fault (See Figure 5.3)

(Make the following settings if preceding enable setting ESOTF = Y)

Close enable time delay (OFF, 0.00–16000.00 cycles in 0.25-cycle steps) CLOEND = _____

52 A enable time delay (OFF, 0.00–16000.00 cycles in 0.25-cycle steps) 52AEND = _____

SOTF duration (0.50–16000.00 cycles in 0.25-cycle steps) SOTFD = _____

POTT Trip Scheme Settings (Also Used in DCUB Trip Schemes) (See Figure 5.6)

(Make the following settings if preceding enable setting ECOMM = POTT, DCUB1, or DCUB2)

Zone (level) 3 reverse block time delay (0.00–16000.00 cycles in 0.25-cycle steps) Z3RBD = _____

Echo block time delay (OFF, 0.00–16000.00 cycles in 0.25-cycle steps) EBLKD = _____

Echo time delay pickup (OFF, 0.00–16000.00 cycles in 0.25-cycle steps) ETDPU = _____

Echo duration time delay (0.00–16000.00 cycles in 0.25-cycle steps) EDURD = _____

Weak-infeed enable (Y, N) EWFC = _____

Additional DCUB Trip Scheme Settings (See Figure 5.10)

(Make the following settings if preceding enable setting ECOMM = DCUB1 or DCUB2)

Guard present security time delay (0.00–16000.00 cycles in 0.25-cycle steps) GARDID = _____

DCUB disabling time delay (0.25–16000.00 cycles in 0.25-cycle steps) UBDURD = _____

DCUB duration time delay (0.00–16000.00 cycles in 0.25-cycle steps) UBEND = _____

SETTINGS SHEET
FOR THE SEL-351-5, -6, -7 RELAY
RELAY SETTINGS (SERIAL PORT COMMAND SET AND FRONT PANEL)

DCB Trip Scheme Settings (See Figure 5.14)

(Make the following settings if preceding enable setting ECOMM = DCB)

Zone (level) 3 reverse pickup time delay (0.00–16000.00 cycles in 0.25-cycle steps)	Z3XPU = _____
Zone (level) 3 reverse dropout extension (0.00–16000.00 cycles in 0.25-cycle steps)	Z3XD = _____
Block trip receive extension (0.00–16000.00 cycles in 0.25-cycle steps)	BTXD = _____
Level 2 phase short delay (0.00–60.00 cycles in 0.25-cycle steps)	67P2SD = _____
Level 2 neutral ground short delay (0.00–60.00 cycles in 0.25-cycle steps)	67N2SD = _____
Level 2 residual ground short delay (0.00–60.00 cycles in 0.25-cycle steps)	67G2SD = _____
Level 2 negative-sequence short delay (0.00–60.00 cycles in 0.25-cycle steps)	67Q2SD = _____

Demand Metering Settings (See Figures 8.11 and 8.13)

(Make the following settings, whether preceding enable setting EDEM = THM or ROL)

Time constant (5, 10, 15, 30, 60 minutes)	DMTC = _____
Phase pickup (OFF, 0.50–16.00 A {5 A nom.}, 0.10–3.20 A {1 A nom.})	PDEMP = _____
Neutral ground pickup—channel IN (OFF, 0.500–16.000 A {5 A nom.}, 0.100–3.200 A {1 A nom.}, 0.005–0.160 A {0.05 A nom.})	NDEMP = _____
Residual ground pickup (OFF, 0.50–16.00 A {5 A nom.}, 0.10–3.20 A {1 A nom.})	GDEMP = _____
Negative-sequence pickup (OFF, 0.50–16.00 A {5 A nom.}, 0.10–3.20 A {1 A nom.})	QDEMP = _____

Other Settings

(Make the following settings—they have no controlling enable setting)

Minimum trip duration time (4.00–16000.00 cycles in 0.25-cycle steps) (see Figure 5.1)	TDURD = _____
Close failure time delay (OFF, 0.00–16000.00 cycles in 0.25-cycle steps) (see Figure 6.1)	CFD = _____
Three-pole open time delay (0.00–60.00 cycles in 0.25-cycle steps) (usually set for no more than a few cycles; see Figure 5.3)	3POD = _____
Load detection phase pickup (OFF, 0.25–100.00 A {5 A nom.}, 0.05–20.00 A {1 A nom.}) (see Figure 5.3)	50LP = _____

SETTINGS SHEET
FOR THE SEL-351-5, -6, -7 RELAY
RELAY SETTINGS (SERIAL PORT COMMAND SET AND FRONT PANEL)

SELogic Control Equation Variable Timers (See Figures 7.24 and 7.25)

(Number of timer pickup/dropout settings dependent on preceding enable setting ESV = 1–16)

SV1 Pickup Time (0.00–999999.00 cycles in 0.25-cycle steps)	SV1PU = _____
SV1 Dropout Time (0.00–999999.00 cycles in 0.25-cycle steps)	SV1DO = _____
SV2 Pickup Time (0.00–999999.00 cycles in 0.25-cycle steps)	SV2PU = _____
SV2 Dropout Time (0.00–999999.00 cycles in 0.25-cycle steps)	SV2DO = _____
SV3 Pickup Time (0.00–999999.00 cycles in 0.25-cycle steps)	SV3PU = _____
SV3 Dropout Time (0.00–999999.00 cycles in 0.25-cycle steps)	SV3DO = _____
SV4 Pickup Time (0.00–999999.00 cycles in 0.25-cycle steps)	SV4PU = _____
SV4 Dropout Time (0.00–999999.00 cycles in 0.25-cycle steps)	SV4DO = _____
SV5 Pickup Time (0.00–999999.00 cycles in 0.25-cycle steps)	SV5PU = _____
SV5 Dropout Time (0.00–999999.00 cycles in 0.25-cycle steps)	SV5DO = _____
SV6 Pickup Time (0.00–999999.00 cycles in 0.25-cycle steps)	SV6PU = _____
SV6 Dropout Time (0.00–999999.00 cycles in 0.25-cycle steps)	SV6DO = _____
SV7 Pickup Time (0.00–16000.00 cycles in 0.25-cycle steps)	SV7PU = _____
SV7 Dropout Time (0.00–16000.00 cycles in 0.25-cycle steps)	SV7DO = _____
SV8 Pickup Time (0.00–16000.00 cycles in 0.25-cycle steps)	SV8PU = _____
SV8 Dropout Time (0.00–16000.00 cycles in 0.25-cycle steps)	SV8DO = _____
SV9 Pickup Time (0.00–16000.00 cycles in 0.25-cycle steps)	SV9PU = _____
SV9 Dropout Time (0.00–16000.00 cycles in 0.25-cycle steps)	SV9DO = _____
SV10 Pickup Time (0.00–16000.00 cycles in 0.25-cycle steps)	SV10PU = _____
SV10 Dropout Time (0.00–16000.00 cycles in 0.25-cycle steps)	SV10DO = _____
SV11 Pickup Time (0.00–16000.00 cycles in 0.25-cycle steps)	SV11PU = _____
SV11 Dropout Time (0.00–16000.00 cycles in 0.25-cycle steps)	SV11DO = _____
SV12 Pickup Time (0.00–16000.00 cycles in 0.25-cycle steps)	SV12PU = _____
SV12 Dropout Time (0.00–16000.00 cycles in 0.25-cycle steps)	SV12DO = _____
SV13 Pickup Time (0.00–16000.00 cycles in 0.25-cycle steps)	SV13PU = _____
SV13 Dropout Time (0.00–16000.00 cycles in 0.25-cycle steps)	SV13DO = _____
SV14 Pickup Time (0.00–16000.00 cycles in 0.25-cycle steps)	SV14PU = _____
SV14 Dropout Time (0.00–16000.00 cycles in 0.25-cycle steps)	SV14DO = _____
SV15 Pickup Time (0.00–16000.00 cycles in 0.25-cycle steps)	SV15PU = _____
SV15 Dropout Time (0.00–16000.00 cycles in 0.25-cycle steps)	SV15DO = _____
SV16 Pickup Time (0.00–16000.00 cycles in 0.25-cycle steps)	SV16PU = _____
SV16 Dropout Time (0.00–16000.00 cycles in 0.25-cycle steps)	SV16DO = _____

SETTINGS SHEET
FOR THE SEL-351-5, -6, -7 RELAY
RELAY SETTINGS (SERIAL PORT COMMAND SET AND FRONT PANEL)

Power Elements (Available in Firmware Version 7; see Figure 3.32)

(Number of power element settings dependent on preceding enable setting EPWR = 1–4)

Per Phase Power Element Pickup (OFF, 2.00–13000.00 VA secondary per phase {5 A nom}) (OFF, 0.40–2600.00 VA secondary per phase {1 A nom})	PWR1P = _____
Pwr Ele. Type (+WATTS, -WATTS, +VAR, -VAR)	PWR1T = _____
Pwr Ele. Time Delay (0.00–16000.00 cyc.)	PWR1D = _____
Per Phase Power Element Pickup (OFF, 2.00–13000.00 VA secondary per phase {5 A nom}) (OFF, 0.40–2600.00 VA secondary per phase {1 A nom})	PWR2P = _____
Pwr Ele. Type (+WATTS, -WATTS, +VAR, -VAR)	PWR2T = _____
Pwr Ele. Time Delay (0.00–16000.00 cyc.)	PWR2D = _____
Per Phase Power Element Pickup (OFF, 2.00–13000.00 VA secondary per phase {5 A nom}) (OFF, 0.40–2600.00 VA secondary per phase {1 A nom})	PWR3P = _____
Pwr Ele. Type (+WATTS, -WATTS, +VAR, -VAR)	PWR3T = _____
Pwr Ele. Time Delay (0.00–16000.00 cyc.)	PWR3D = _____
Per Phase Power Element Pickup (OFF, 2.00–13000.00 VA secondary per phase {5 A nom}) (OFF, 0.40–2600.00 VA secondary per phase {1 A nom})	PWR4P = _____
Pwr Ele. Type (+WATTS, -WATTS, +VAR, -VAR)	PWR4T = _____
Pwr Ele. Time Delay (0.00–16000.00 cyc.)	PWR4D = _____

Voltage Sag/Swell/Interrupt (Available in Firmware Version 7; see Figures 3.29, 3.30, 3.31)

(Make the following settings if preceding enable setting ESSI=Y)

%V1 Phase Voltage Interruption Pickup (OFF, 5.00–95.00; cannot be set higher than VSAG)	VINT = _____
%V1 Phase Voltage Sag Pickup (OFF, 10.00–95.00)	VSAG = _____
%V1 Phase Voltage Swell Pickup (OFF; 105.00–180.00)	VSWELL = _____

SETTINGS SHEET
FOR THE SEL-351-5, -6, -7 RELAY
SELOGIC CONTROL EQUATION SETTINGS (SERIAL PORT COMMAND SET L)

SELOGIC control equation settings consist of Relay Word bits (see Table 9.3) and SELOGIC control equation operators * (AND), + (OR), ! (NOT), / (rising edge), \ (falling edge), and () (parentheses). Numerous SELOGIC control equation settings examples are given in *Sections 3 through 8*. SELOGIC control equation settings can also be set directly to 1 (logical 1) or 0 (logical 0). *Appendix G: Setting SELOGIC Control Equations* gives SELOGIC control equation details, examples, and limitations.

Trip Logic Equations (See Figure 5.1)

Other trip conditions	TR = _____
Communications-assisted trip conditions	TRCOMM = _____
Switch-onto-fault trip conditions	TRSOTF = _____
Direct transfer trip conditions	DTT = _____
Unlatch trip conditions	ULTR = _____

Communications-Assisted Trip Scheme Input Equations

Permissive trip 1 (used for ECOMM = POTT, DCUB1, or DCUB2; see Figures 5.5, 5.7, and 5.10)	PT1 = _____
Loss-of-guard 1 (used for ECOMM = DCUB1 or DCUB2; see Figure 5.10)	LOG1 = _____
Permissive trip 2 (used for ECOMM = DCUB2; see Figures 5.5 and 5.10)	PT2 = _____
Loss of guard 2 (used for ECOMM = DCUB2; see Figure 5.10)	LOG2 = _____
Block trip (used for ECOMM = DCB; see Figure 5.14)	BT = _____

Close Logic Equations (See Figure 6.1)

Circuit breaker status (used in Figure 5.3, also)	52A = _____
Close conditions (other than automatic reclosing or CLOSE command)	CL = _____
Unlatch close conditions	ULCL = _____

Reclosing Relay Equations (See *Reclosing Relay* in *Section 6*)

Reclose initiate	79RI = _____
Reclose initiate supervision	79RIS = _____
Drive-to-lockout	79DTL = _____
Drive-to-last shot	79DLS = _____
Skip shot	79SKP = _____
Stall open interval timing	79STL = _____
Block reset timing	79BRS = _____
Sequence coordination	79SEQ = _____
Reclose supervision (see Figure 6.2)	79CLS = _____

SETTINGS SHEET
FOR THE SEL-351-5, -6, -7 RELAY
SELOGIC CONTROL EQUATION SETTINGS (SERIAL PORT COMMAND SET L)

Latch Bits Set/Reset Equations (See Figure 7.12)

Set Latch Bit LT1	SET1 = _____
Reset Latch Bit LT1	RST1 = _____
Set Latch Bit LT2	SET2 = _____
Reset Latch Bit LT2	RST2 = _____
Set Latch Bit LT3	SET3 = _____
Reset Latch Bit LT3	RST3 = _____
Set Latch Bit LT4	SET4 = _____
Reset Latch Bit LT4	RST4 = _____
Set Latch Bit LT5	SET5 = _____
Reset Latch Bit LT5	RST5 = _____
Set Latch Bit LT6	SET6 = _____
Reset latch Bit LT6	RST6 = _____
Set Latch Bit LT7	SET7 = _____
Reset Latch Bit LT7	RST7 = _____
Set Latch Bit LT8	SET8 = _____
Reset Latch Bit LT8	RST8 = _____
Set Latch Bit LT9	SET9 = _____
Reset Latch Bit LT9	RST9 = _____
Set Latch Bit LT10	SET10 = _____
Reset Latch Bit LT10	RST10 = _____
Set Latch Bit LT11	SET11 = _____
Reset Latch Bit LT11	RST11 = _____
Set Latch Bit LT12	SET12 = _____
Reset Latch Bit LT12	RST12 = _____
Set Latch Bit LT13	SET13 = _____
Reset Latch Bit LT13	RST13 = _____
Set Latch Bit LT14	SET14 = _____
Reset latch Bit LT14	RST14 = _____
Set Latch Bit LT15	SET15 = _____
Reset Latch Bit LT15	RST15 = _____
Set Latch Bit LT16	SET16 = _____
Reset Latch Bit LT16	RST16 = _____

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SELOGIC CONTROL EQUATION SETTINGS (SERIAL PORT COMMAND SET L)

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Torque Control Equations for Inst./Def.-Time Overcurrent Elements

[Note: torque control equation settings cannot be set directly to logical 0]

Level 1 phase (see Figure 3.3)	67P1TC = _____
Level 2 phase (see Figure 3.3)	67P2TC = _____
Level 3 phase (see Figure 3.3)	67P3TC = _____
Level 4 phase (see Figure 3.3)	67P4TC = _____
Level 1 neutral ground (see Figure 3.8)	67N1TC = _____
Level 2 neutral ground (see Figure 3.8)	67N2TC = _____
Level 3 neutral ground (see Figure 3.8)	67N3TC = _____
Level 4 neutral ground (see Figure 3.8)	67N4TC = _____
Level 1 residual ground (see Figure 3.10)	67G1TC = _____
Level 2 residual ground (see Figure 3.10)	67G2TC = _____
Level 3 residual ground (see Figure 3.10)	67G3TC = _____
Level 4 residual ground (see Figure 3.10)	67G4TC = _____
Level 1 negative-sequence (see Figure 3.12)	67Q1TC = _____
Level 2 negative-sequence (see Figure 3.12)	67Q2TC = _____
Level 3 negative-sequence (see Figure 3.12)	67Q3TC = _____
Level 4 negative-sequence (see Figure 3.12)	67Q4TC = _____

Torque Control Equations for Time-Overcurrent Elements

[Note: torque control equation settings cannot be set directly to logical 0]

A-phase (see Figure 3.15)	51ATC = _____
B-phase (see Figure 3.16)	51BTC = _____
C-phase (see Figure 3.17)	51CTC = _____
Phase (see Figure 3.14)	51PTC = _____
Neutral Ground (see Figure 3.18)	51NTC = _____
Residual Ground (see Figure 3.19)	51GTC = _____
Negative-Sequence (see Figure 3.20)	51QTC = _____

SELOGIC Control Equation Variable Timer Input Equations (See Figures 7.24 and 7.25)

SELOGIC Control Equation Variable SV1	SV1 = _____
SELOGIC Control Equation Variable SV2	SV2 = _____
SELOGIC Control Equation Variable SV3	SV3 = _____
SELOGIC Control Equation Variable SV4	SV4 = _____
SELOGIC Control Equation Variable SV5	SV5 = _____
SELOGIC Control Equation Variable SV6	SV6 = _____
SELOGIC Control Equation Variable SV7	SV7 = _____

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FOR THE SEL-351-5, -6, -7 RELAY
SELOGIC CONTROL EQUATION SETTINGS (SERIAL PORT COMMAND SET L)

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SELOGIC Control Equation Variable SV8	SV8 = _____
SELOGIC Control Equation Variable SV9	SV9 = _____
SELOGIC Control Equation Variable SV10	SV10 = _____
SELOGIC Control Equation Variable SV11	SV11 = _____
SELOGIC Control Equation Variable SV12	SV12 = _____
SELOGIC Control Equation Variable SV13	SV13 = _____
SELOGIC Control Equation Variable SV14	SV14 = _____
SELOGIC Control Equation Variable SV15	SV15 = _____
SELOGIC Control Equation Variable SV16	SV16 = _____

Output Contact Equations for Models 0351x0, 0351x1, and 0351xY (See Figure 7.27)

Output Contact OUT101	OUT101 = _____
Output Contact OUT102	OUT102 = _____
Output Contact OUT103	OUT103 = _____
Output Contact OUT104	OUT104 = _____
Output Contact OUT105	OUT105 = _____
Output Contact OUT106	OUT106 = _____
Output Contact OUT107	OUT107 = _____

Output Contact Equations for Models 0351x1 and 0351xY-Extra I/O Board (See Figure 7.28)

Output Contact OUT201	OUT201 = _____
Output Contact OUT202	OUT202 = _____
Output Contact OUT203	OUT203 = _____
Output Contact OUT204	OUT204 = _____
Output Contact OUT205	OUT205 = _____
Output Contact OUT206	OUT206 = _____
Output Contact OUT207	OUT207 = _____
Output Contact OUT208	OUT208 = _____
Output Contact OUT209	OUT209 = _____
Output Contact OUT210	OUT210 = _____
Output Contact OUT211	OUT211 = _____
Output Contact OUT212	OUT212 = _____

Display Point Equations (See *Rotating Default Display* in *Sections 7 and 11*)

Display Point DP1	DP1 = _____
Display Point DP2	DP2 = _____
Display Point DP3	DP3 = _____

SETTINGS SHEET
FOR THE SEL-351-5, -6, -7 RELAY
SELOGIC CONTROL EQUATION SETTINGS (SERIAL PORT COMMAND SET L)

Display Point DP4	DP4 = _____
Display Point DP5	DP5 = _____
Display Point DP6	DP6 = _____
Display Point DP7	DP7 = _____
Display Point DP8	DP8 = _____
Display Point DP9	DP9 = _____
Display Point DP10	DP10 = _____
Display Point DP11	DP11 = _____
Display Point DP12	DP12 = _____
Display Point DP13	DP13 = _____
Display Point DP14	DP14 = _____
Display Point DP15	DP15 = _____
Display Point DP16	DP16 = _____

Setting Group Selection Equations (See Table 7.4)

Select Setting Group 1	SS1 = _____
Select Setting Group 2	SS2 = _____
Select Setting Group 3	SS3 = _____
Select Setting Group 4	SS4 = _____
Select Setting Group 5	SS5 = _____
Select Setting Group 6	SS6 = _____

Other Equations

Event report trigger conditions (see <i>Section 12</i>)	ER = _____
Fault indication [used in INST, A, B, and C target logic and other relay functions, see subsection SELOGIC Control Equation Setting FAULT in <i>Section 5: Trip and Target Logic</i>]	FAULT = _____
Block synchronism check elements (see Figure 3.24)	BSYNCH = _____
Close bus monitor (see Figure 5.3)	CLMON = _____
Breaker monitor initiation (see Figure 8.3)	BKMON = _____
Enable for zero-sequence voltage-polarized and channel IN current-polarized directional elements (see Figure 4.6)	E32IV = _____

SETTINGS SHEET
FOR THE SEL-351-5, -6, -7 RELAY
SELOGIC CONTROL EQUATION SETTINGS (SERIAL PORT COMMAND SET L)

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Date _____

MIRRORED BITS™ Transmit Equations (Available in Firmware Versions 6 and Greater; see Appendix I)

Channel A, transmit bit 1	TMB1A = _____
Channel A, transmit bit 2	TMB2A = _____
Channel A, transmit bit 3	TMB3A = _____
Channel A, transmit bit 4	TMB4A = _____
Channel A, transmit bit 5	TMB5A = _____
Channel A, transmit bit 6	TMB6A = _____
Channel A, transmit bit 7	TMB7A = _____
Channel A, transmit bit 8	TMB8A = _____
Channel B, transmit bit 1	TMB1B = _____
Channel B, transmit bit 2	TMB2B = _____
Channel B, transmit bit 3	TMB3B = _____
Channel B, transmit bit 4	TMB4B = _____
Channel B, transmit bit 5	TMB5B = _____
Channel B, transmit bit 6	TMB6B = _____
Channel B, transmit bit 7	TMB7B = _____
Channel B, transmit bit 8	TMB8B = _____

SETTINGS SHEET
FOR THE SEL-351-5, -6, -7 RELAY
GLOBAL SETTINGS (SERIAL PORT COMMAND SET G AND FRONT PANEL)

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Date _____

Settings Group Change Delay (See *Multiple Setting Groups* in *Section 7*)

Group change delay (0.00–16000.00 cycles in 0.25-cycle steps) TGR = _____

Power System Configuration and Date Format (See *Settings Explanations* in *Section 9*)

Nominal frequency (50 Hz, 60 Hz) NFREQ = _____

Phase rotation (ABC, ACB) PHROT = _____

Date format (MDY, YMD) DATE_F = _____

Front-Panel Display Operation (See *Section 11*)

Front-panel display time-out (OFF, 0–30 minutes in 1-minute steps) FP_TO = _____

[If FP_TO = OFF, no time-out occurs and display remains on last display screen (e.g., continually display metering). Setting FP_TO = 0 is the same as OFF and is stored internally as OFF.]

Display update rate (1–60 seconds) SCROLLD = _____

Front panel neutral / ground display (OFF, IN, IG) FPNGD = _____

Event Report Parameters (See *Section 12*)

Length of event report (15, 30 cycles) LER = _____

Length of pre-fault in event report (1 to LER-1 cycles in 1-cycle steps) PRE = _____

Station DC Battery Monitor (See *Figures 8.9 and 8.10*)

DC battery instantaneous undervoltage pickup (OFF, 20–300 Vdc) DCLOP = _____

DC battery instantaneous overvoltage pickup (OFF, 20–300 Vdc) DCHIP = _____

Optoisolated Input Timers for Models 0351x0, 0351x1, and 0351xY (See *Figure 7.1*)

Input IN101 debounce time (AC, 0.00–1.00 cycles in 0.25-cycle steps) IN101D = _____

Input IN102 debounce time (AC, 0.00–1.00 cycles in 0.25-cycle steps) IN102D = _____

Input IN103 debounce time (AC, 0.00–1.00 cycles in 0.25-cycle steps) IN103D = _____

Input IN104 debounce time (AC, 0.00–1.00 cycles in 0.25-cycle steps) IN104D = _____

Input IN105 debounce time (AC, 0.00–1.00 cycles in 0.25-cycle steps) IN105D = _____

Input IN106 debounce time (AC, 0.00–1.00 cycles in 0.25-cycle steps) IN106D = _____

SETTINGS SHEET
FOR THE SEL-351-5, -6, -7 RELAY
GLOBAL SETTINGS (SERIAL PORT COMMAND SET G AND FRONT PANEL)

Optoisolated Input Timers for Models 0351x1 and 0351xY-Extra I/O Board (See Figure 7.2)

Input IN201 debounce time (AC, 0.00–1.00 cycles in 0.25-cycle steps)	IN201D = _____
Input IN202 debounce time (AC, 0.00–1.00 cycles in 0.25-cycle steps)	IN202D = _____
Input IN203 debounce time (AC, 0.00–1.00 cycles in 0.25-cycle steps)	IN203D = _____
Input IN204 debounce time (AC, 0.00–1.00 cycles in 0.25-cycle steps)	IN204D = _____
Input IN205 debounce time (AC, 0.00–1.00 cycles in 0.25-cycle steps)	IN205D = _____
Input IN206 debounce time (AC, 0.00–1.00 cycles in 0.25-cycle steps)	IN206D = _____
Input IN207 debounce time (AC, 0.00–1.00 cycles in 0.25-cycle steps)	IN207D = _____
Input IN208 debounce time (AC, 0.00–1.00 cycles in 0.25-cycle steps)	IN208D = _____

Breaker Monitor Settings (See *Breaker Monitor* in Section 8)

Breaker monitor enable (Y, N)	EBMON = _____
(Make the following settings if preceding enable setting EBMON = Y)	
Close /Open set point 1—max. (0–65000 operations)	COSP1 = _____
Close /Open set point 2—mid. (0–65000 operations)	COSP2 = _____
Close /Open set point 3—min. (0–65000 operations)	COSP3 = _____
kA Interrupted set point 1—min. (0.00–999.00 kA primary in 0.01 kA steps)	KASP1= _____
kA Interrupted set point 2—mid. (0.00–999.00 kA primary in 0.01 kA steps)	KASP2= _____
kA Interrupted set point 3—max. (0.00–999.00 kA primary in 0.01 kA steps)	KASP3= _____

SETTINGS SHEET
FOR THE SEL-351-5, -6, -7 RELAY

SEQUENTIAL EVENTS RECORDER AND LOAD PROFILE SETTINGS (SERIAL PORT COMMAND SET R)

Sequential Events Recorder settings are comprised of three trigger lists. Each trigger list can include up to 24 Relay Word bits delimited by commas. Enter NA to remove a list of these Relay Word bit settings. See *Sequential Events Recorder (SER) Report* in *Section 12*.

SER Trigger List 1 SER1 = _____
SER Trigger List 2 SER2 = _____
SER Trigger List 3 SER3 = _____

Load Profile settings are only available in Firmware Versions 6, and 7. See *Load Profile* in *Section 8*.

Load profile list LDLIST = _____
(15 elements max., enter NA to null) _____

Load profile acquisition rate LDAR = _____
(5,10,15,30,60 min)

LDLIST may contain any of the following elements (delimit with spaces or commas):

ELEMENT	QUANTITY RECORDED
IA, IB, IC, IN	Phase and neutral current magnitudes
VA, VB, VC, VS	Phase and sync voltage magnitudes
VAB, VBC, VCA	Phase-to-phase voltage magnitudes
IG, I1, 3I2, 3V0, V1, V2	Sequence current and voltage magnitudes
VDC	Battery voltage
FREQ	Phase frequency
MWA, MWB, MWC, MW3	Phase and 3 phase megaWATTs
MVARA, MVARB, MVARC, MVAR3	Phase and 3 phase megaVARs
PFA, PFB, PFC, PF3	Phase and 3 phase power factor
LDPFA, LDPFB, LDPFC, LDPF3	Phase and 3 phase power factor lead/lag status (0 = lag, 1 = lead)
IADEM, IBDEM, ICDEM, INDEM, IGDEM, 3I2DEM	Demand ammeter quantities
MWADI, MWBDI, MWCDI, MW3DI	Phase and 3 phase demand megaWATTs in
MWADO, MWBDO, MWCDO, MW3DO	Phase and 3 phase demand megaWATTs out
MVRADI, MVRBDI, MVRCDI, MVR3DI	Phase and 3 phase demand megaVARs in
MVRADO, MVRBDO, MVRCDO, MVR3DO	Phase and 3 phase demand megaVARs out
MWHAI, MWHBI, MWHCI, MWH3I	Phase and 3 phase megaWATT hours in
MWHAO, MWHBO, MWHCO, MWH3O	Phase and 3 phase megaWATT hours out
MVRHAI, MVRHBI, MVRHCI, MVRH3I	Phase and 3 phase megaVAR hours in
MVRHAO, MVRHBO, MVRHCO, MVRH3O	Phase and 3 phase megaVAR hours out

SETTINGS SHEET
FOR THE SEL-351-5, -6, -7 RELAY
TEXT LABEL SETTINGS (SERIAL PORT COMMAND SET T)

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Date _____

Local Bit LB8 Name (14 characters)	NLB8 = _____
Clear Local Bit LB8 Label (7 characters)	CLB8 = _____
Set Local Bit LB8 Label (7 characters)	SLB8 = _____
Pulse Local Bit LB8 Label (7 characters)	PLB8 = _____

Local Bit LB9 Name (14 characters)	NLB9 = _____
Clear Local Bit LB9 Label (7 characters)	CLB9 = _____
Set Local Bit LB9 Label (7 characters)	SLB9 = _____
Pulse Local Bit LB9 Label (7 characters)	PLB9 = _____

Local Bit LB10 Name (14 characters)	NLB10 = _____
Clear Local Bit LB10 Label (7 characters)	CLB10 = _____
Set Local Bit LB10 Label (7 characters)	SLB10 = _____
Pulse Local Bit LB10 Label (7 characters)	PLB10 = _____

Local Bit LB11 Name (14 characters)	NLB11 = _____
Clear Local Bit LB11 Label (7 characters)	CLB11 = _____
Set Local Bit LB11 Label (7 characters)	SLB11 = _____
Pulse Local Bit LB11 Label (7 characters)	PLB11 = _____

Local Bit LB12 Name (14 characters)	NLB12 = _____
Clear Local Bit LB12 Label (7 characters)	CLB12 = _____
Set Local Bit LB12 Label (7 characters)	SLB12 = _____
Pulse Local Bit LB12 Label (7 characters)	PLB12 = _____

Local Bit LB13 Name (14 characters)	NLB13 = _____
Clear Local Bit LB13 Label (7 characters)	CLB13 = _____
Set Local Bit LB13 Label (7 characters)	SLB13 = _____
Pulse Local Bit LB13 Label (7 characters)	PLB13 = _____

Local Bit LB14 Name (14 characters)	NLB14 = _____
Clear Local Bit LB14 Label (7 characters)	CLB14 = _____
Set Local Bit LB14 Label (7 characters)	SLB14 = _____
Pulse Local Bit LB14 Label (7 characters)	PLB14 = _____

Local Bit LB15 Name (14 characters)	NLB15 = _____
Clear Local Bit LB15 Label (7 characters)	CLB15 = _____
Set Local Bit LB15 Label (7 characters)	SLB15 = _____
Pulse Local Bit LB15 Label (7 characters)	PLB15 = _____

SETTINGS SHEET
FOR THE SEL-351-5, -6, -7 RELAY
TEXT LABEL SETTINGS (SERIAL PORT COMMAND SET T)

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Date _____

Local Bit LB16 Name (14 characters)	NLB16 = _____
Clear Local Bit LB16 Label (7 characters)	CLB16 = _____
Set Local Bit LB16 Label (7 characters)	SLB16 = _____
Pulse Local Bit LB16 Label (7 characters)	PLB16 = _____

Display Point Labels (See *Rotating Default Display* in Sections 7 and 11)

Display if DP1 = logical 1 (16 characters)	DP1_1 = _____
Display if DP1 = logical 0 (16 characters)	DP1_0 = _____
Display if DP2 = logical 1 (16 characters)	DP2_1 = _____
Display if DP2 = logical 0 (16 characters)	DP2_0 = _____
Display if DP3 = logical 1 (16 characters)	DP3_1 = _____
Display if DP3 = logical 0 (16 characters)	DP3_0 = _____
Display if DP4 = logical 1 (16 characters)	DP4_1 = _____
Display if DP4 = logical 0 (16 characters)	DP4_0 = _____
Display if DP5 = logical 1 (16 characters)	DP5_1 = _____
Display if DP5 = logical 0 (16 characters)	DP5_0 = _____
Display if DP6 = logical 1 (16 characters)	DP6_1 = _____
Display if DP6 = logical 0 (16 characters)	DP6_0 = _____
Display if DP7 = logical 1 (16 characters)	DP7_1 = _____
Display if DP7 = logical 0 (16 characters)	DP7_0 = _____
Display if DP8 = logical 1 (16 characters)	DP8_1 = _____
Display if DP8 = logical 0 (16 characters)	DP8_0 = _____
Display if DP9 = logical 1 (16 characters)	DP9_1 = _____
Display if DP9 = logical 0 (16 characters)	DP9_0 = _____
Display if DP10 = logical 1 (16 characters)	DP10_1 = _____
Display if DP10 = logical 0 (16 characters)	DP10_0 = _____
Display if DP11 = logical 1 (16 characters)	DP11_1 = _____
Display if DP11 = logical 0 (16 characters)	DP11_0 = _____
Display if DP12 = logical 1 (16 characters)	DP12_1 = _____
Display if DP12 = logical 0 (16 characters)	DP12_0 = _____
Display if DP13 = logical 1 (16 characters)	DP13_1 = _____
Display if DP13 = logical 0 (16 characters)	DP13_0 = _____

SETTINGS SHEET
FOR THE SEL-351-5, -6, -7 RELAY
TEXT LABEL SETTINGS (SERIAL PORT COMMAND SET T)

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Date _____

Display if DP14 = logical 1 (16 characters)	DP14_1 = _____
Display if DP14 = logical 0 (16 characters)	DP14_0 = _____
Display if DP15 = logical 1 (16 characters)	DP15_1 = _____
Display if DP15 = logical 0 (16 characters)	DP15_0 = _____
Display if DP16 = logical 1 (16 characters)	DP16_1 = _____
Display if DP16 = logical 0 (16 characters)	DP16_0 = _____

Reclosing Relay Labels (See *Functions Unique to the Front-Panel Interface in Section 1h*)

Reclosing Relay Last Shot Label (14 char.)	79LL = _____
Reclosing Relay Shot Counter Label (14 char.)	79SL = _____

SETTINGS SHEET
FOR THE SEL-351-5, -6, -7 RELAY
PORT SETTINGS (SERIAL PORT COMMAND SET P AND FRONT PANEL)

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Date _____

Protocol Settings (See Below)

Protocol (SEL, LMD, DNP, MBA, MBB, MB8A, MB8B) PROTO = _____

Protocol Settings Set PROTO = SEL for standard SEL ASCII protocol. For SEL Distributed Port Switch Protocol (LMD), set PROTO = LMD. Refer to *Appendix C* for details on the LMD protocol. For Distributed Network Protocol (DNP), set PROTO = DNP. Refer to *Appendix H* for details on DNP protocol. For MIRRORED BITS, set PROTO = MBA, MBB, MB8A, or MB8B. Refer to *Appendix I* for details on MIRRORED BITS.

The following settings are used if PROTO = LMD.

LMD Prefix (@, #, \$, %, &)

PREFIX = _____

LMD Address (01–99)

ADDR = _____

LMD Settling Time (0–30 seconds)

SETTLE = _____

Communications Settings

Baud Rate (300, 1200, 2400, 4800, 9600, 19200, 38400)

SPEED = _____

Data Bits (6, 7, 8)

BITS = _____

Parity (O, E, N) {Odd, Even, None}

PARITY = _____

Stop Bits (1, 2)

STOP = _____

Other Port Settings (See Below)

Time-out (0–30 minutes)

T_OUT = _____

Send Auto Messages to Port (Y, N, DTA)

AUTO = _____

Enable Hardware Handshaking (Y, N, MBT)

RTSCTS = _____

Fast Operate Enable (Y, N)

FASTOP = _____

Other Port Settings Set T_OUT to the number of minutes of serial port inactivity for an automatic log out. Set T_OUT = 0 for no port time out.

Set AUTO = Y to allow automatic messages at the serial port. Set AUTO = DTA to use the serial port with an SEL-DTA2 Display/Transducer Adapter.

Set RTSCTS = Y to enable hardware handshaking. With RTSCTS = Y, the relay will not send characters until the CTS input is asserted. Also, if the relay is unable to receive characters, it deasserts the RTS line. Setting RTSCTS is not applicable to serial Port 1 (EIA-485) or a port configured for SEL Distributed Port Switch Protocol.

Set RTSCTS = MBT is only available at 9600 baud (SPEED selection). In this mode, the relay deasserts the RTS line and does not monitor the CTS line. This selection is normally used with MIRRORED BITS, PROTO = MBA or MBB. See *Appendix I* for more detail.

Set FASTOP = Y to enable binary *Fast Operate* messages at the serial port. Set FASTOP = N to block binary *Fast Operate* messages. Refer to *Appendix D* for the description of the SEL-351 Relay *Fast Operate* commands.

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SECTION 10: SERIAL PORT COMMUNICATIONS AND COMMANDS

INTRODUCTION

Various serial ports are available in the following SEL-351 Relay models:

Table 10.1: SEL-351 Relay Models and Available Serial Ports

SEL-351 Relay Model Number	Reference Figures	Rear Panel			Front Panel
		Serial Port 1 (EIA-485, 4-wire)	Serial Port 2 (EIA-232)	Serial Port 3 (EIA-232)	Serial Port F (EIA-232)
0351x0	1.2, 2.2	X	X	X	X
0351x1 0351xY	1.2, 2.3, 2.4	X	X	X	X

Connect the serial port to a computer serial port for local communications or to a modem for remote communications. Other devices useful for communications include the SEL-PRTU, SEL-2020 and SEL-2030 Communications Processors, SEL-2505 Remote I/O Module, SEL-2100 Protection Logic Processor, and SEL-DTA2 Display Transducer Adapter. You can use a variety of terminal emulation programs on your personal computer to communicate with the relay. Examples of PC-based terminal emulation programs include: CROSSTALK[®], Microsoft[®] Windows[®] Terminal and HyperTerminal, Procomm[®] Plus, Relay/Gold, and SmartCOM. For the best display, use VT-100 terminal emulation or the closest variation.

The default settings for all serial ports are:

Baud Rate = 2400
 Data Bits = 8
 Parity = N
 Stop Bits = 1

To change the port settings, use the SET P command (see *Section 9: Setting the Relay*) or the front-panel SET pushbutton.

PORT CONNECTOR AND COMMUNICATIONS CABLES

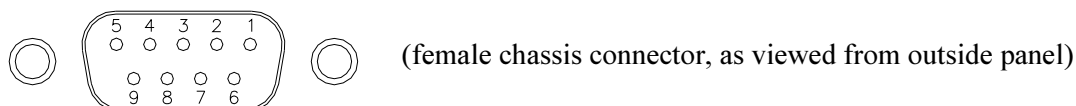


Figure 10.1: DB-9 Connector Pinout for EIA-232 Serial Ports

IRIG-B

Refer to the Reference Figures in preceding Table 10.1 and the following Table 10.2. Note that demodulated IRIG-B time code can be input into Serial Port 1 or Serial Port 2 on any of the SEL-351 Relay models. This is handled adeptly by connecting Serial Port 2 of the SEL-351 Relay to an SEL-2020 with Cable C273A (see cable diagrams that follow in this section).

Refer to the Reference Figures in preceding Table 10.1 for SEL-351 Relay models 0351x0, 0351x1, and 0351xY and the following Table 10.3. Note that demodulated IRIG-B time code can be input into the connector for Serial Port 1 on these three models. If demodulated IRIG-B time code is input into this connector, it should not be input into Serial Port 2 and vice versa.

Table 10.2: Pinout Functions for EIA-232 Serial Ports 2, 3, and F

Pin	Port 2	Port 3	Port F
1	N/C or +5 Vdc ¹	N/C or +5 Vdc ¹	N/C
2	RXD	RXD	RXD
3	TXD	TXD	TXD
4	+IRIG-B	N/C	N/C
5, 9	GND	GND	GND
6	-IRIG-B	N/C	N/C
7	RTS	RTS	RTS
8	CTS	CTS	CTS

¹ See *EIA-232 Serial Port Jumpers* in *Section 2: Installation*.

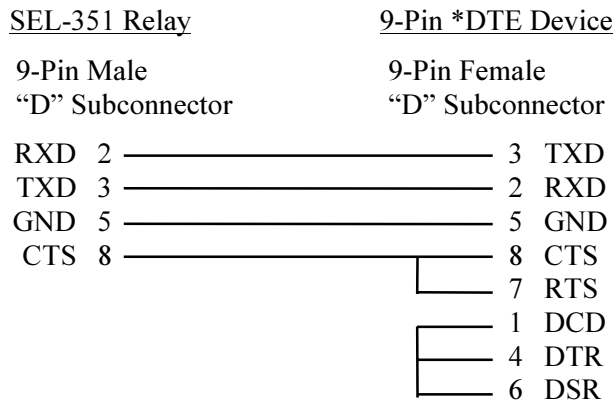
Table 10.3: Terminal Functions for EIA-485 Serial Port 1

Terminal	Function
1	+TX
2	-TX
3	+RX
4	-RX
5	SHIELD
6	N/C
7	+IRIG-B
8	-IRIG-B

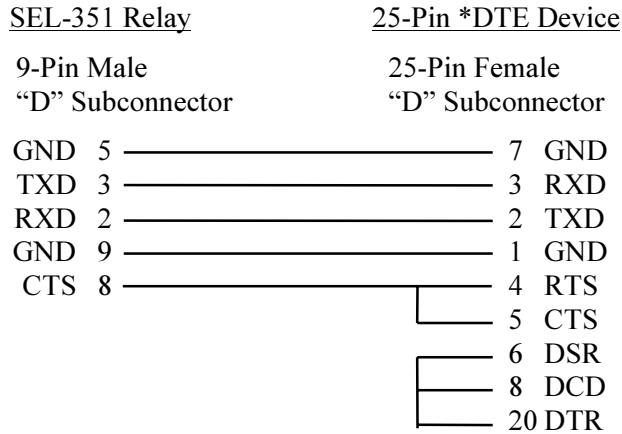
The following cable diagrams show several types of EIA-232 serial communications cables that connect the SEL-351 Relay to other devices. These and other cables are available from SEL. Contact the factory for more information.

SEL-351 to Computer

Cable C234A

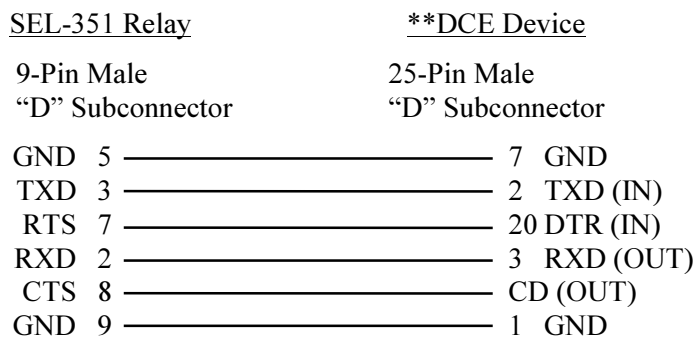


Cable C227A



SEL-351 to Modem

Cable C222



* DTE = Data Terminal Equipment (Computer, Terminal, Printer, etc.)

** DCE = Data Communications Equipment (Modem, etc.)

SEL-351 to SEL-PRTU

Cable C231

<u>SEL-PRTU</u>		<u>SEL-351 Relay</u>	
9-Pin Male Round Conxall		9-Pin Male “D” Subconnector	
GND	1	5	GND
TXD	2	2	RXD
RXD	4	3	TXD
CTS	5	7	RTS
+12	7	8	CTS
GND	9	9	GND

SEL-351 to SEL-2020, SEL-2030, or SEL 2100

Cable C273A

<u>SEL-2020</u>		<u>SEL-351 Relay</u>	
9-Pin Male “D” Subconnector		9-Pin Male “D” Subconnector	
RXD	2	3	TXD
TXD	3	2	RXD
IRIG+	4	4	IRIG+
GND	5	5	GND
IRIG-	6	6	IRIG-
RTS	7	8	CTS
CTS	8	7	RTS

SEL-351 to SEL-DTA2

Cable C272A

<u>SEL-DTA2</u>		<u>SEL-351 Relay</u>	
9-Pin Male “D” Subconnector		9-Pin Male “D” Subconnector	
RXD	2	3	TXD
TXD	3	2	RXD
GND	5	5	GND
RTS	7	7	RTS
CTS	8	8	CTS

Table 10.4: Serial Communications Port Pin/Terminal Function Definitions

Pin Function	Definition
N/C	No Connection
+5 Vdc (0.5 A limit)	5 Vdc Power Connection
RXD, RX	Receive Data
TXD, TX	Transmit Data
IRIG-B	IRIG-B Time-Code Input
GND	Ground
SHIELD	Shielded Ground
RTS	Request To Send
CTS	Clear To Send
DCD	Data Carrier Detect
DTR	Data Terminal Ready
DSR	Data Set Ready

For long-distance communications up to 500 meters and for electrical isolation of communications ports, use the SEL-2800 family of Fiber-Optic Transceivers. Contact SEL for more details on these devices.

COMMUNICATIONS PROTOCOL

Hardware Protocol

All EIA-232 serial ports support RTS/CTS hardware handshaking. RTS/CTS handshaking is not supported on the EIA-485 Serial Port 1.

To enable hardware handshaking, use the SET P command (or front-panel SET pushbutton) to set `RTSCTS = Y`. Disable hardware handshaking by setting `RTSCTS = N`.

If `RTSCTS = N`, the relay permanently asserts the RTS line.

If `RTSCTS = Y`, the relay deasserts RTS when it is unable to receive characters.

If `RTSCTS = Y`, the relay does not send characters until the CTS input is asserted.

Software Protocols

The SEL-351 Relay provides standard SEL protocols: SEL ASCII, SEL Distributed Port Switch Protocol (LMD), SEL *Fast Meter*, and SEL Compressed ASCII. In addition, the relay provides MIRRORING BITS™ and Distributed Network Protocol (DNP) 3.00 as ordering options. The relay activates protocols on a per-port basis. The SEL-351 Relay is compatible with the SEL-DTA2 Display Transducer Adapter. See Page 27 of the *Settings Sheets* in **Section 9: Setting the Relay**.

To select SEL ASCII protocol, set the port PROTO setting to SEL. To select SEL Distributed Port Switch Protocol (LMD), set `PROTO = LMD`. To select DNP protocol, set `PROTO = DNP`.

SEL *Fast Meter* and SEL Compressed ASCII commands are active when PROTO is set to either SEL or LMD. The commands are not active when PROTO is set to DNP or MIRRORED BITS.

SEL ASCII Protocol

SEL ASCII protocol is designed for manual and automatic communications.

1. All commands received by the relay must be of the form:

<command><CR> or <command><CRLF>

A command transmitted to the relay should consist of the command followed by either a CR (carriage return) or a CRLF (carriage return and line feed). You may truncate commands to the first three characters. For example, **EVENT 1 <ENTER>** would become **EVE 1 <ENTER>**. Upper and lower case characters may be used without distinction, except in passwords.

Note: The ENTER key on most keyboards is configured to send the ASCII character 13 (^M) for a carriage return. This manual instructs you to press the ENTER key after commands, which should send the proper ASCII code to the relay.

2. The relay transmits all messages in the following format:

```
<STX><MESSAGE LINE 1><CRLF>
  <MESSAGE LINE 2><CRLF>
  •
  •
  •
  <LAST MESSAGE LINE><CRLF>< ETX>
```

Each message begins with the start-of-transmission character (ASCII 02) and ends with the end-of-transmission character (ASCII 03). Each line of the message ends with a carriage return and line feed.

3. The relay implements XON/XOFF flow control.

The relay transmits XON (ASCII hex 11) and asserts the RTS output (if hardware handshaking enabled) when the relay input buffer drops below 25% full.

The relay transmits XOFF (ASCII hex 13) when the buffer is over 75% full. If hardware handshaking is enabled, the relay deasserts the RTS output when the buffer is approximately 95% full. Automatic transmission sources should monitor for the XOFF character so they do not overwrite the buffer. Transmission should terminate at the end of the message in progress when XOFF is received and may resume when the relay sends XON.

4. You can use the XON/XOFF protocol to control the relay during data transmission. When the relay receives XOFF during transmission, it pauses until it receives an XON character. If there is no message in progress when the relay receives XOFF, it blocks transmission of any message presented to its buffer. Messages will be accepted after the relay receives XON.

The CAN character (ASCII hex 18) aborts a pending transmission. This is useful in terminating an unwanted transmission.

Control characters can be sent from most keyboards with the following keystrokes:

XON: <CNTRL> Q (hold down the Control key and press Q)
XOFF: <CNTRL> S (hold down the Control key and press S)
CAN: <CNTRL> X (hold down the Control key and press X)

SEL Distributed Port Switch Protocol (LMD)

The SEL Distributed Port Switch Protocol (LMD) permits multiple SEL relays to share a common communications channel. The protocol is selected by setting the port setting PROTO = LMD. See *Appendix C* for more information on SEL Distributed Port Switch Protocol (LMD).

SEL *Fast Meter* Protocol

SEL *Fast Meter* protocol supports binary messages to transfer metering and control messages. The protocol is described in *Appendix D*.

SEL Compressed ASCII Protocol

SEL Compressed ASCII protocol provides compressed versions of some of the relay ASCII commands. The protocol is described in *Appendix E*.

SEL Unsolicited Sequential Events Recorder (SER) Protocol

SEL Unsolicited Sequential Events Recorder (SER) Protocol provides SER events to an automated data collection system. SEL Unsolicited SER Protocol is available on any serial port. The protocol is described in *Appendix J*.

Distributed Network Protocol (DNP) 3.00

The relay provides Distributed Network Protocol (DNP) 3.00 slave support. DNP is an optional protocol and is described in *Appendix H*.

MIRRORED BITS Communications

The SEL-351 Relay supports MIRRORED BITS relay-to-relay communications on two ports simultaneously (available in firmware versions 6 and 7 only). See *Appendix I*.

SERIAL PORT AUTOMATIC MESSAGES

When the serial port AUTO setting is Y, the relay sends automatic messages to indicate specific conditions. The automatic messages are described in Table 10.5.

When a serial port AUTO setting is DTA, the SEL-351 Relay is compatible with the SEL-DTA2 on that port. The MET and MET D command responses are modified to comply with the DTA2 data format for that port.

Table 10.5: Serial Port Automatic Messages

Condition	Description
Power Up	The relay sends a message containing the present date and time, Relay and Terminal Identifiers, and the Access Level 0 prompt when the relay is turned on.
Event Trigger	The relay sends an event summary each time an event report is triggered. See Section 12: Standard Event Reports, Sag/Swell/Interruption Report, and SER.
Group Switch	The relay displays the active settings group after a group switch occurs. See GRO n Command (Group) in this section.
Self-Test Warning or Failure	The relay sends a status report each time a self-test warning or failure condition is detected. See STA Command (Status) in this section.

SERIAL PORT ACCESS LEVELS

Commands can be issued to the relay via the serial port to view metering values, change relay settings, etc. The available serial port commands are listed in Table 10.6. The commands can be accessed only from the corresponding access level as shown in Table 10.6. The access levels are:

- Access Level 0 (the lowest access level)
- Access Level 1
- Access Level B
- Access Level 2 (the highest access level)

Note: In this manual, commands you type appear in bold/uppercase: **SET**. Computer keys you press appear in bold/uppercase/brackets: **<ENTER>**.

Access Level 0

Once serial port communications are established with the relay, the relay sends the following prompt:

```
=
```

This is referred to as Access Level 0. The only command that is available at Access Level 0 is the ACC command (see Table 10.6). Enter the ACC command at the Access Level 0 prompt:

```
=ACC <ENTER>
```

The ACC command takes the relay to Access Level 1 [see *ACC, BAC, and 2AC Commands (Go to Access Level 1, B, or 2)* in the *Command Explanations* subsection for more detail].

Access Level 1

When the relay is in Access Level 1, the relay sends the following prompt:

```
=>
```

Commands 2AC through TRI in Table 10.6 are available from Access Level 1. For example, enter the MET command at the Access Level 1 prompt to view metering data:

```
=>MET <ENTER>
```

The 2AC command allows the relay to go to Access Level 2 [see *ACC, BAC, and 2AC Commands (Go to Access Level 1, B, or 2)* in the *Command Explanations* subsection for more detail]. Enter the 2AC command at the Access Level 1 prompt:

```
=>2AC <ENTER>
```

The BAC command allows the relay to go to Access Level B [see *ACC, BAC, and 2AC Commands (Go to Access Level 1, B, or 2)* in the *Command Explanations* subsection for more detail]. Enter the BAC command at the Access Level 1 prompt:

```
=>BAC <ENTER>
```

Access Level B

When the relay is in Access Level B, the relay sends the prompt:

```
==>
```

Commands BRE n through PUL in Table 10.6 are available from Access Level B. For example, enter the CLO command at the Access Level B prompt to close the circuit breaker:

```
==>CLO <ENTER>
```

While in Access Level B, any of the Access Level 1 commands are also available (commands 2AC through TRI in Table 10.6).

The 2AC command allows the relay to go to Access Level 2 [see *ACC, BAC, and 2AC Commands (Go to Access Level 1, B, or 2)* in the *Command Explanations* subsection for more detail]. Enter the 2AC command at the Access Level B prompt:

```
==>2AC <ENTER>
```

Access Level 2

When the relay is in Access Level 2, the relay sends the prompt:

```
=>>
```

Commands CON through SET in Table 10.6 are available from Access Level 2. For example, enter the SET command at the Access Level 2 prompt to make relay settings:

```
=>>SET <ENTER>
```

While in Access Level 2, any of the Access Level 1 and Access Level B commands are also available (commands 2AC through PUL in Table 10.6).

COMMAND SUMMARY

Table 10.6 alphabetically lists the serial port commands within a given access level. Much of the information available from the serial port commands is also available via the front-panel pushbuttons. The correspondence between the serial port commands and the front-panel pushbuttons is also given in Table 10.6. See *Section 11: Front-Panel Interface* for more information on the front-panel pushbuttons.

The serial port commands at the different access levels offer varying levels of control:

- The Access Level 1 commands primarily allow the user to look at information only (settings, metering, etc.), not change it.
- The Access Level B commands primarily allow the user to operate output contacts or change the active setting group.
- The Access Level 2 commands primarily allow the user to change relay settings.

Again, a higher access level can access the serial port commands in a lower access level. The commands are shown in upper-case letters, but they can also be entered with lower-case letters.

Table 10.6: Serial Port Command Summary

Access Level	Prompt	Serial Port Command	Command Description	Corresponding Front-Panel Pushbutton
0	=	ACC	Go to Access Level 1	
1	=>	BAC	Go to Access Level B	
1	=>	2AC	Go to Access Level 2	
1	=>	BRE	Breaker monitor data	OTHER
1	=>	COM	MIRRORED BITS communications statistics	
1	=>	DAT	View/change date	OTHER
1	=>	EVE	Event reports	
1	=>	GRO	Display active setting group number	GROUP
1	=>	HIS	Event summaries/histories	EVENTS
1	=>	IRI	Synchronize to IRIG-B	
1	=>	LDP	Load profile report	
1	=>	MET	Metering data	METER
1	=>	QUI	Quit access level	
1	=>	SER	Sequential Events Recorder	
1	=>	SHO	Show/view settings	SET
1	=>	SSI	Voltage Sag/Swell/Interruption Report	
1	=>	STA	Relay self-test status	STATUS
1	=>	TAR	Display relay element status	OTHER
1	=>	TIM	View/change time	OTHER
1	=>	TRI	Trigger an event report	
B	==>	BRE n	Preload/reset breaker wear	OTHER
B	==>	CLO	Close breaker	
B	==>	GRO n	Change active setting group	GROUP
B	==>	OPE	Open breaker	
B	==>	PUL	Pulse output contact	CNTRL
2	==>>	CON	Control remote bit	
2	==>>	COP	Copy setting group	
2	==>>	LOO	Loopback	
2	==>>	PAS	View/change passwords	SET
2	==>>	SET	Change settings	SET
2	==>>	VER	Show relay configuration and firmware version	

The relay responds with “Invalid Access Level” if a command is entered from an access level lower than the specified access level for the command. The relay responds:

```
Invalid Command
```

to commands not listed above or entered incorrectly.

Many of the command responses display the following header at the beginning:

```
FEEDER 1                               Date: 03/05/97   Time: 17:03:26.484
STATION A
```

The definitions are:

- FEEDER 1: This is the RID setting (the relay is shipped with the default setting RID = FEEDER 1; see *Identifier Labels* in *Section 9: Setting the Relay*).
- STATION A: This is the TID setting (the relay is shipped with the default setting TID = STATION A; see *Identifier Labels* in *Section 9: Setting the Relay*).
- Date: This is the date the command response was given [except for relay response to the EVE command (Event), where it is the date the event occurred]. You can modify the date display format (Month/Day/Year or Year/Month/Day) by changing the DATE_F relay setting.
- Time: This is the time the command response was given (except for relay response to the EVE command, where it is the time the event occurred).

The serial port command explanations that follow in the *Command Explanations* subsection are in the same order as the commands listed in Table 10.6.

COMMAND EXPLANATIONS

Access Level 0 Commands

ACC, BAC, and 2AC Commands (go to Access Level 1, B, or 2)

The ACC, BAC, and 2AC commands provide entry to the multiple access levels. Different commands are available at the different access levels as shown in Table 10.6. Commands ACC, BAC, and 2AC are explained together because they operate similarly.

ACC moves from Access Level 0 to Access Level 1.

BAC moves from Access Level 1 to Access Level B.

2AC moves from Access Level 1 or B to Access Level 2

Password Requirements

Passwords are required if the main board Password jumper is not in place (Password jumper = OFF). Passwords are not required if the main board Password jumper is in place (Password jumper = ON). Refer to Tables 2.5 and 2.6 for Password jumper information. See PAS Command later in this section for the list of default passwords and for more information on changing passwords.

Access Level Attempt (Password Required)

Assume the following conditions: Password jumper = OFF (not in place), Access Level = 0.

At the Access Level 0 prompt, enter the ACC command:

=ACC <ENTER>

Because the Password jumper is not in place, the relay asks for the Access Level 1 password to be entered:

Password: ? @@@@

The relay is shipped with the default Access Level 1 password shown in the table under the PAS Command later in this section. At the prompt above, enter the default password and press the <ENTER> key. The relay responds:

```
-----  
FEEDER 1                               Date: 03/05/97   Time: 08:31:10.361  
STATION A  
  
Level 1  
=>
```

The “=>” prompt indicates the relay is now in Access Level 1.

If the entered password is incorrect, the relay asks for the password again (Password: ?). The relay will ask up to three times. If the requested password is incorrectly entered three times, the relay closes the ALARM contact for one second and remains at Access Level 0 (“=” prompt).

Access Level Attempt (Password Not Required)

Assume the following conditions: Password jumper = ON (in place), Access Level = 0.

At the Access Level 0 prompt, enter the ACC command:

=ACC <ENTER>

Because the Password jumper is in place, the relay does not ask for a password; it goes directly to Access Level 1. The relay responds:

```
-----  
FEEDER 1                               Date: 03/05/97   Time: 08:31:10.361  
STATION A  
  
Level 1  
=>
```

The “=>” prompt indicates the relay is now in Access Level 1.

The above two examples demonstrate how to go from Access Level 0 to Access Level 1. The procedure to go from Access Level 1 to Access Level B, Access Level 1 to Access Level 2, or Access Level B to Access Level 2 is much the same, with command BAC or 2AC entered at the access level screen prompt. The relay closes the ALARM contact for one second after a successful Level B or Level 2 access. If access is denied, the ALARM contact closes for one second.

Access Level 1 Commands

BRE Command (Breaker Monitor Data)

Use the BRE command to view the breaker monitor report.

```
=>BRE <ENTER>
FEEDER 1                               Date: 02/02/97   Time: 08:40:14.802
STATION A
Rly Trips=      9
IA=  40.7 IB=   41.4 IC=   53.8 kA
Ext Trips=      3
IA=   0.8 IB=   0.9 IC=   1.1 kA
Percent wear: A=  4 B=  4 C=  6
LAST RESET 12/27/96 15:32:59
=>
```

See the **BRE n** command in *Access Level B Commands* that follows in this section and *Breaker Monitor* in *Section 8: Breaker Monitor, Metering, and Load Profile Functions* for further details on the breaker monitor.

COMM Command (Communication Data—Available in Firmware Versions 6 and 7)

The COMM command displays integral relay-to-relay (MIRRORED BITS) communications data. For more information on MIRRORED BITS, see *Appendix I: MIRRORED BITS (In Firmware Versions 6 and 7)*. To get a summary report, enter the command with the channel parameter (A or B).

```

=>COMM A <ENTER>

FEEDER 1                      Date: 04/20/98   Time: 18:36:11.748
STATION A
FID=SEL-351-7-R301-V0-D990426  CID=FF27
Summary for Mirrored Bits channel A

For 04/20/01 18:36:09.279 to 04/20/01 18:36:11.746

    Total failures      1                Last error  Relay Disabled
    Relay Disabled     1
    Data error         0                Longest Failure    2.458 sec.
    Re-Sync            0
    Underrun           0                Unavailability    0.996200
    Overrun            0
    Parity error       0
    Framing error      0                Loopback          0

=>

```

If only one MIRRORRED BITS port is enabled, the channel specifier may be omitted. Use the **L** parameter to get a summary report, followed by a listing of the COMM records.

```

=>COMM L <ENTER>

FEEDER 1                      Date: 02/20/98   Time: 18:37:36.125
STATION A
FID=SEL-351-7-R301-V0-D990426  CID=FF27
Summary for Mirrored Bits channel A

For 02/05/98 17:18:12.993 to 02/20/98 18:37:36.123

    Total failures      4                Last error  Relay Disabled
    Relay Disabled     2
    Data error         0                Longest Failure    2.835 sec.
    Re-Sync            0
    Underrun           1                Unavailability    0.000003
    Overrun            0
    Parity error       1
    Framing error      0                Loopback          0

    Failure             Recovery
    #  Date   Time   Date   Time   Duration Cause
    1  02/20/98 18:36:09.279 02/20/98 18:37:36.114 2.835 Relay Disabled
    2  02/14/98 13:18:09.236 02/14/98 13:18:09.736 0.499 Parity error
    3  02/08/98 11:43:35.547 02/08/98 11:43:35.637 0.089 Underrun
    4  02/05/98 17:18:12.993 02/05/98 17:18:13.115 0.121 Relay Disabled

=>

```

There may be up to 255 records in the extended report. To limit the number of COMM records displayed in the report to the 10 most recent records, type **COMM 10 L <ENTER>**. To select lines 10 through 20 of the COMM records for display in the report, type **COMM 10 20 L <ENTER>**. To reverse the order of the COMM records in the report, supply a range of row numbers, with the larger number first, i.e., **COMM 40 10 L <ENTER>**. To display all the COMM records that started on a particular day, supply that date as a parameter, i.e., **COMM 2/8/98 L <ENTER>**. To display all the COMM records that started between a range of dates, supply both dates as parameters, i.e., **COMM 2/21/98 2/7/98 L <ENTER>**. Reversing the order of the dates will reverse the order of the records in the report. To receive a summary report for a subset of the records, use one of the above methods while omitting the **L** parameter.

To clear the COMM records, type **COMM C <ENTER>**. The prompting message “Are you sure (Y/N) ?” is displayed. Typing **N <ENTER>** aborts the clearing operation with the message “Canceled.” If both MIRRORED BITS channels are enabled, omitting the channel specifier in the clear command will cause both channels to be cleared.

DAT Command (View/Change Date)

DAT displays the date stored by the internal calendar/clock. If the date format setting DATE_F is set to MDY, the date is displayed as month/day/year. If the date format setting DATE_F is set to YMD, the date is displayed as year/month/day.

To set the date, type **DATE mm/dd/yy <ENTER>** if the DATE_F setting is MDY. If the DATE_F is set to YMD, enter **DATE yy/mm/dd <ENTER>**. To set the date to June 1, 1997, enter:

```
=>DATE 6/1/98 <ENTER>
6/1/98
=>
```

You can separate the month, day, and year parameters with spaces, commas, slashes, colons, and semicolons.

Note: After setting the date, allow at least 60 seconds before powering down the relay or the new setting may be lost.

EVE Command (Event Reports)

Use the EVE command to view event reports. See *Section 12: Standard Event Reports, Sag/Swell/Interruption Report, and SER* for further details on retrieving event reports.

GRO Command (Display Active Setting Group Number)

Use the GRO command to display the active settings group number. See the **GRO n** command in *Access Level B Commands* that follows in this section and *Multiple Setting Groups* in *Section 7: Inputs, Outputs, Timers, and Other Control Logic* for further details on settings groups.

HIS Command (Event Summaries/History)

HIS **x** displays event summaries or allows you to clear event summaries (and corresponding event reports) from nonvolatile memory.

If no parameters are specified with the HIS command:

```
=HIS <ENTER>
```

the relay displays the most recent event summaries in reverse chronological order.

If **x** is a number (1–29):

=HIS X <ENTER>

the relay displays the **x** most recent event summaries. The maximum number of available event summaries is a function of the LER (length of event report) setting and the features present in the relay firmware.

If **x** is “C” or “c”, the relay clears the event summaries and all corresponding event reports from nonvolatile memory.

The event summaries include the date and time the event was triggered, the type of event, the fault location, the maximum phase current in the event, the power system frequency, the number of the active setting group, the reclose shot count, and the front-panel targets.

To display the relay event summaries, enter the following command:

```
=>HIS <ENTER>
FEEDER 1                      Date: 02/01/97   Time: 08:40:16.740
STATION A

#   DATE      TIME      EVENT  LOCAT  CURR  FREQ  GRP  SHOT  TARGETS
1  02/01/97  08:33:00.365 TRIG  $$$$$$  1 60.00  3   2
2  01/31/97  20:32:58.361 ER   $$$$$$ 231 60.00  2   2
3  01/29/97  07:30:11.055 AG T   9.65 2279 60.00  3   2 INST 50

=>
```

The fault locator has influence over information in the EVENT and LOCAT columns. If the fault locator is enabled (enable setting EFLOC = Y), the fault locator will attempt to run if the event report is generated by a trip (assertion of TRIP Relay Word bit) or other programmable event report trigger condition (SELOGIC[®] control equation setting ER).

If the fault locator runs successfully, the location is listed in the LOCAT column, and the event type is listed in the EVENT column:

- AG for A-phase to ground faults
- BG for B-phase to ground faults
- CG for C-phase to ground faults
- AB for A-B phase-to-phase faults
- BC for B-C phase-to-phase faults
- CA for C-A phase-to-phase faults
- ABG for A-B phase-to-phase to ground faults
- BCG for B-C phase-to-phase to ground faults
- CAG for C-A phase-to-phase to ground faults
- ABC for three-phase faults

If a trip occurs in the same event report, a “T” is appended to the event type (e.g., AG T).

If the fault locator does not run successfully, \$\$\$\$\$\$ is listed in the LOCAT column. If the fault locator is disabled (enable setting EFLOC = N), the LOCAT column is left blank. For either of these cases where the fault locator does not run, the event type listed in the EVENT column is one of the following:

TRIP	event report generated by assertion of Relay Word bit TRIP
ER	event report generated by assertion of SELOGIC control equation event report trigger condition setting ER
PULSE	event report generated by execution of the PUL (Pulse) command
TRIG	event report generated by execution of the TRI (Trigger) command

The TARGETS column will display any of the following illuminated front-panel target LEDs if the event report is generated by a trip (assertion of TRIP Relay Word bit):

INST COMM SOTF 50 51 81

For more information on front-panel target LEDs, see *Section 5: Trip and Target Logic*. For more information on event reports, see *Section 12: Standard Event Reports, Sag/Swell/Interruption Report, and SER*.

IRI Command (Synchronize to IRIG-B Time Code)

IRI directs the relay to read the demodulated IRIG-B time code at the serial port input.

To force the relay to synchronize to IRIG-B, enter the following command:

=>IRI <ENTER>

If the relay successfully synchronizes to IRIG, it sends the following header and access level prompt:

```

-----
FEEDER 1                               Date: 03/05/97   Time: 10:15:09.609
STATION A
=>
-----

```

If no IRIG-B code is present at the serial port input or if the code cannot be read successfully, the relay responds:

```

-----
IRIG-B DATA ERROR
=>
-----

```

If an IRIG-B signal is present, the relay synchronizes its internal clock with IRIG-B. It is not necessary to issue the IRI command to synchronize the relay clock with IRIG-B. Use the IRI command to determine if the relay is properly reading the IRIG-B signal.

LDP Command (Load Profile Report—Available in Firmware Versions 6 and 7)

Use the LDP command to view the Load Profile report. For more information on Load Profile reports, see *Section 8: Breaker Monitor, Metering, and Load Profile Functions*.

MET Command (Metering Data)

The MET commands provide access to the relay metering data. Metered quantities include phase voltages and currents, sequence component voltages and currents, power, frequency, substation battery voltage, energy, demand, and maximum/minimum logging of selected quantities. To

make the extensive amount of meter information manageable, the relay divides the displayed information into four groups: Instantaneous, Demand, Energy, and Maximum/Minimum.

Note: If the serial port AUTO setting is DTA, the SEL-351 Relay response for MET, MET X, and MET D will be formatted differently on that serial port than shown below.

MET k–Instantaneous Metering

The MET k command displays instantaneous magnitudes (and angles if applicable) of the following quantities:

Currents	$I_{A,B,C,N}$	Input currents (A primary)
	I_G	Residual ground current (A primary; $I_G = 3I_0 = I_A + I_B + I_C$)
Voltages	$V_{A,B,C,S}$	Wye-connected voltage inputs (kV primary)
Power	$MW_{A,B,C}$	Single-phase megawatts
	MW_{3P}	Three-phase megawatts
	$MVAR_{A,B,C}$	Single- and three-phase megavars
	$MVAR_{3P}$	Three-phase megavars
Power Factor	$PF_{A,B,C,3P}$	Single- and three-phase power factor; leading or lagging
Sequence	$I_1, 3I_2, 3I_0$	Positive-, negative-, and zero-sequence currents (A primary)
	V_1, V_2	Positive- and negative-sequence voltages (kV primary)
	$3V_0$	Zero-sequence voltage (kV primary)
Frequency	FREQ (Hz)	Instantaneous power system frequency (measured on voltage channel VA)
Station DC	VDC (V)	Voltage at POWER terminals (input into station battery monitor)

The angles are referenced to the A-phase voltage if it is greater than 13 V secondary; otherwise, the angles are referenced to A-phase current. The angles range from -179.99 to 180.00 degrees.

To view instantaneous metering values, enter the command:

=>MET k <ENTER>

where **k** is an optional parameter to specify the number of times (1–32767) to repeat the meter display. If **k** is not specified, the meter report is displayed once. The output from an SEL-351 Relay with wye-connected voltage inputs is shown:

```

=>MET <ENTER>

FEEDER 1                               Date: 02/01/97   Time: 15:00:52.615
STATION A

      A           B           C           N           G
I MAG (A)  195.146  192.614  198.090  0.302  4.880
I ANG (DEG) -8.03   -128.02  111.89   52.98  81.22

      A           B           C           S
V MAG (KV)  11.691  11.686  11.669  11.695
V ANG (DEG)  0.00   -119.79  120.15  0.05

      A           B           C           3P
MW          2.259  2.228  2.288  6.774
MVAR        0.319  0.322  0.332  0.973
PF          0.990  0.990  0.990  0.990
           LAG    LAG    LAG    LAG

      I1          3I2          3I0          V1           V2           3V0
MAG         195.283  4.630  4.880  11.682  0.007  0.056
ANG (DEG)   -8.06   -103.93  81.22  0.12   -80.25  -65.83

FREQ (Hz)   60.00                               VDC (V)   129.5
=>

```

MET X k—Extended Instantaneous Metering

The MET X k command displays the same data as the MET k command with the addition of calculated phase-to-phase voltage quantities V_{ab} , V_{bc} , V_{ca} , and the V_{base} quantity used by the Voltage Sag/Swell/Interruption Recorder.

Currents	$I_{A,B,C,N}$ I_G	Input currents (A primary) Residual ground current (A primary; $I_G = 3I_0 = I_A + I_B + I_C$)
Voltages	$V_{A,B,C,S}$	Wye-connected phase-to-neutral voltage inputs (kV primary)
	$V_{AB,BC,CA}$	Calculated phase-to-phase voltages (kV primary)
	V_{base}	Demand average value based on V1, subject to the operating logic of the SSI Elements (see <i>Section 3: Overcurrent, Voltage, Synchronism Check, Frequency, and Power Element</i>) when setting $ESSI=Y$ in the active setting group. V_{base} only registers a value after valid three-phase voltage signals have been present since the last V_{base} initializing. The V_{base} quantity is used in SEL-351-7 relay model. V_{base} is always shown as 0.00 kV in SEL-351-5, -6 relay models.
Power	$MW_{A,B,C}$	Single-phase megawatts
	MW_{3P}	Three-phase megawatts
	$MVAR_{A,B,C}$	Single- and three-phase megavars
	$MVAR_{3P}$	Three-phase megavars
Power Factor	$PF_{A,B,C,3P}$	Single- and three-phase power factor; leading or lagging
Sequence	$I_1, 3I_2, 3I_0$	Positive-, negative-, and zero-sequence currents (A primary)
	V_1, V_2	Positive- and negative-sequence voltages (kV primary)
	$3V_0$	Zero-sequence voltage (kV primary)

Frequency FREQ (Hz) Instantaneous power system frequency (measured on voltage channel VA)

Station DC VDC (V) Voltage at POWER terminals (input into station battery monitor)

The angles are referenced to the A-phase voltage if it is greater than 13 V secondary; otherwise, the angles are referenced to A-phase current. The angles range from -179.99 to 180.00 degrees.

To view instantaneous metering values, enter the command:

=>MET X k <ENTER>

where **k** is an optional parameter to specify the number of times (1–32767) to repeat the meter display. If **k** is not specified, the meter report is displayed once. The output from an SEL-351 Relay with wye-connected voltage inputs is shown:

```

=>>MET X <ENTER>

FEEDER 12                      Date: 12/12/00   Time: 11:31:22.626
SUB B

  I MAG (A)      A      B      C      N      G
  I ANG (DEG)    -2.02  -121.88  119.60  -115.20  -117.52

  V MAG (KV)     A      B      C      S
  V ANG (DEG)    0.00  -119.95  120.94  29.93

  V MAG (KV)     AB     BC     CA     Vbase
  V ANG (DEG)    29.89  -89.23  150.34

  MW             A      B      C      3P
  MVAR           0.016  0.018  0.010  0.044
  PF             0.999  0.999  1.000  1.000
                LAG     LAG     LAG     LAG

  MAG            I1     3I2     3I0     V1     V2     3V0
  ANG (DEG)     -1.47  106.38  -117.52  0.33  -59.08  157.40

  FREQ (Hz)     60.00                      VDC (V)   125.6

=>>

```

MET D–Demand Metering

The MET D command displays the demand and peak demand values of the following quantities:

Currents	$I_{A,B,C,N}$	Input currents (A primary)
	I_G	Residual ground current (A primary; $I_G = 3I_0 = I_A + I_B + I_C$)
	$3I_2$	Negative-sequence current (A primary)
Power	$MW_{A,B,C}$	Single-phase megawatts
	MW_{3P}	Three-phase megawatts
	$MVAR_{A,B,C}$	Single-phase megavars
	$MVAR_{3P}$	Three-phase megavars
Reset Time	Demand, Peak Last time the demands and peak demands were reset	

To view demand metering values, enter the command:

=>**MET D** <ENTER>

The output from an SEL-351 Relay with wye-connected voltage inputs is shown:

```
=>MET D <ENTER>

FEEDER 1                               Date: 02/01/97   Time: 15:08:05.615
STATION A

DEMAND   IA      IB      IC      IN      IG      3I2
PEAK     188.6   186.6   191.8   0.2     4.5     4.7
MWA      188.6   186.6   191.8   0.3     4.5     4.7
MWB      188.6   186.6   191.8   0.3     4.5     4.7
MWC      188.6   186.6   191.8   0.3     4.5     4.7
MW3P     188.6   186.6   191.8   0.3     4.5     4.7
MVARA    188.6   186.6   191.8   0.3     4.5     4.7
MVARB    188.6   186.6   191.8   0.3     4.5     4.7
MVARC    188.6   186.6   191.8   0.3     4.5     4.7
MVAR3P   188.6   186.6   191.8   0.3     4.5     4.7
DEMAND IN 0.0     0.0     0.0     0.0     0.0     0.0
PEAK IN   0.0     0.0     0.0     0.0     0.0     0.0
DEMAND OUT 2.2     2.2     2.2     6.6     0.3     0.3
PEAK OUT  3.1     3.1     3.1     9.3     0.4     0.4
LAST DEMAND RESET 01/27/97 15:31:51.238  LAST PEAK RESET 01/27/97 15:31:56.239

=>
```

Reset the accumulated demand values using the **MET RD** command. Reset the peak demand values using the **MET RP** command. For more information on demand metering, see *Demand Metering* in **Section 8: Breaker Monitor, Metering, and Load Profile Functions**.

MET E—Energy Metering

The MET E command displays the following quantities:

Energy	MWh _{A,B,C}	Single-phase megawatt hours (in and out)
	MWh _{3P}	Three-phase megawatt hours (in and out)
	MVARh _{A,B,C}	Single-phase megavar hours (in and out)
	MVARh _{3P}	Three-phase megavar hours (in and out)
Reset Time		Last time the energy meter was reset

To view energy metering values, enter the command:

=>**MET E** <ENTER>

The output from an SEL-351 Relay with wye-connected voltage inputs is shown:

```
=>MET E <ENTER>

FEEDER 1                               Date: 02/01/97   Time: 15:11:24.056
STATION A

IN       MWhA    MWhB    MWhC    Mwh3P    MVARhA    MVARhB    MVARhC    MVARh3P
OUT      36.0    36.6    36.7    109.2    5.1       5.2       5.3       15.6
LAST RESET 01/31/97 23:31:28.864

=>
```

Reset the energy values using the **MET RE** command. For more information on energy metering, see *Energy Metering* in **Section 8: Breaker Monitor, Metering, and Load Profile Functions**.

MET M—Maximum/Minimum Metering

The MET M command displays the maximum and minimum values of the following quantities:

Currents	$I_{A,B,C,N}$ I_G	Input currents (A primary) Residual ground current (A primary; $I_G = 3I_0 = I_A + I_B + I_C$)
Voltages	$V_{A,B,C,S}$	Wye-connected voltage inputs (kV primary)
Power	MW_{3P} $MVAR_{3P}$	Three-phase megawatts Three-phase megavars
Reset Time		Last time the maximum/minimum meter was reset

To view maximum/minimum metering values, enter the command:

=>MET M <ENTER>

The output from an SEL-351 Relay with wye-connected voltage inputs is shown:

```
=>MET M <ENTER>

FEEDER 1                      Date: 02/01/97   Time: 15:16:00.239
STATION A

Max   Date   Time           Min   Date   Time
IA(A) 196.8 02/01/97 15:00:42.574 30.0 02/01/97 14:51:02.391
IB(A) 195.0 02/01/97 15:05:19.558 31.8 02/01/97 14:50:55.536
IC(A) 200.4 02/01/97 15:00:42.578 52.2 02/01/97 14:51:02.332
IN(A)  42.6 02/01/97 14:51:02.328 42.6 02/01/97 14:51:02.328
IG(A)  42.0 02/01/97 14:50:55.294 42.0 02/01/97 14:50:55.294
VA(kV) 11.7 02/01/97 15:01:01.576  3.4 02/01/97 15:00:42.545
VB(kV) 11.7 02/01/97 15:00:42.937  2.4 02/01/97 15:00:42.541
VC(kV) 11.7 02/01/97 15:00:42.578  3.1 02/01/97 15:00:42.545
VS(kV) 11.7 02/01/97 15:01:01.576  3.4 02/01/97 15:00:42.545
MW3P   6.9 02/01/97 15:00:44.095  0.4 02/01/97 15:00:42.545
MVAR3P  1.0 02/01/97 15:00:42.578  0.1 02/01/97 15:00:42.545
LAST RESET 01/27/97 15:31:41.237
=>
```

Reset the maximum/minimum values using the **MET RM** command. All values will display **RESET** until new maximum/minimum values are recorded. For more information on maximum/minimum metering, see *Maximum/Minimum Metering* in **Section 8: Breaker Monitor, Metering, and Load Profile Functions**.

QUI Command (Quit Access Level)

The QUI command returns the relay to Access Level 0.

To return to Access Level 0, enter the command:

=>QUI <ENTER>

The relay sets the port access level to 0 and responds:

```
-----  
FEEDER 1                               Date: 03/05/97   Time: 08:55:33.986  
STATION A  
  
=  
-----
```

The “=” prompt indicates the relay is back in Access Level 0.

The QUI command terminates the SEL Distributed Port Switch Protocol (LMD) connection if it is established [see *Appendix C* for details on SEL Distributed Port Switch Protocol (LMD)].

SER Command (Sequential Events Recorder Report)

Use the SER command to view the Sequential Events Recorder report. For more information on SER reports, see *Section 12: Standard Event Reports, Sag/Swell/Interruption Report, and SER*.

SHO Command (Show/View Settings)

Use the SHO command to view relay settings, SELOGIC control equations, global settings, serial port settings, sequential events recorder (SER) settings, and text label settings. Below are the SHO command options.

SHO n	Show relay settings. n specifies the setting group (1, 2, 3, 4, 5, or 6); n defaults to the active setting group if not listed.
SHO L n	Show SELOGIC control equation settings. n specifies the setting group (1, 2, 3, 4, 5, or 6); n defaults to the active setting group if not listed.
SHO G	Show global settings.
SHO P n	Show serial port settings. n specifies the port (1, 2, 3, or F); n defaults to the active port if not listed.
SHO R	Show sequential events recorder (SER) settings.
SHO T	Show text label settings.

You may append a setting name to each of the commands to specify the first setting to display (e.g., **SHO 1 E50P** displays the setting Group 1 relay settings starting with setting E50P). The default is the first setting.

The SHO commands display only the enabled settings. To display all settings, including disabled/hidden settings, append an **A** to the SHO command (e.g., **SHO 1 A**).

Below are sample SHOWSET commands for the SEL-351 Relay model 0351x1, showing all the **factory default settings** (firmware version 7; see table 1.2). The factory default settings for the SEL-351 Relay models 0351x0, 0351x1, and 0351xY are similar.

```

=>SHO <ENTER>
Group 1
Group Settings:

RID =FEEDER 1          TID =STATION A
CTR = 120      CTRN = 120      PTR = 180.00  PTRS = 180.00
ZIMAG = 2.14   ZIANG = 68.86
ZOMAG = 6.38   ZOANG = 72.47  LL = 4.84
E50P = 1      E50N = N      E50G = N      E50Q = N
E51P = 1      E51N = N      E51G = Y      E51Q = N
E32 = N      ELOAD = N     ESOTF = N     EVOLT = N
E25 = N      EFLOC = Y     ELOP = Y     ECOMM = N
E81 = 1      E79 = 2      ESV = 1      EDEM = THM    ESSI = N

50P1P = 15.00
67P1D = 0.00
50PP1P= OFF
51PP = 6.00    51PC = U3    51PTD = 3.00  51PRS = N
51GP = 1.50    51GC = U3    51GTD = 1.50  51GRS = N
27B81P= 40.00  81D1P = 59.10  81D1D = 6.00
790I1 = 30.00  790I2 = 600.00

Press RETURN to continue
79RSD = 1800.00  79RSLD= 300.00  79CLSD= 0.00
DMTC = 5
PDEMP = 5.00    NDEMP = 1.500  GDEMP = 1.50  QDEMP = 1.50
TDURD = 9.00    CFD = 60.00    3POD = 1.50  50LP = 0.25
SV1PU = 12.00   SV1DO = 2.00

=>>

```

```

=>SHO L <ENTER>
SELogic group 1
=>>SHO L
SELogic group 1

SELogic Control Equations:
TR =0C + 51PT + 51GT + 81D1T + LB3 + 50P1 * SHO
TRCOMM=0
TRSOTF=0
DTT =0
ULTR =!(51P + 51G)
PT1 =0
LOG1 =0
PT2 =0
LOG2 =0
BT =0
52A =IN101
CL =CC + LB4
ULCL =TRIP
79RI =TRIP
79RIS =52A + 79CY
79DTL =0C + !IN102 + LB3
79DLS =79L0

Press RETURN to continue
79SKP =0
79STL =TRIP
79BRS =0
79SEQ =0
79CLS =1

```

```
SET1 =0
RST1 =0
SET2 =0
RST2 =0
SET3 =0
RST3 =0
SET4 =0
RST4 =0
SET5 =0
RST5 =0
SET6 =0
RST6 =0
SET7 =0
RST7 =0
SET8 =0
```

Press RETURN to continue

```
RST8 =0
SET9 =0
RST9 =0
SET10 =0
RST10 =0
SET11 =0
RST11 =0
SET12 =0
RST12 =0
SET13 =0
RST13 =0
SET14 =0
RST14 =0
SET15 =0
RST15 =0
SET16 =0
RST16 =0
67P1TC=1
67P2TC=1
67P3TC=1
```

Press RETURN to continue

```
67P4TC=1
67N1TC=1
67N2TC=1
67N3TC=1
67N4TC=1
67G1TC=1
67G2TC=1
67G3TC=1
67G4TC=1
67Q1TC=1
67Q2TC=1
67Q3TC=1
67Q4TC=1
51ATC =1
51BTC =1
51CTC =1
51PTC =1
51NTC =1
51GTC =1
51QTC =1
```

Press RETURN to continue

```
SV1 =TRIP
SV2 =0
SV3 =0
SV4 =0
SV5 =0
```



```
SV6 =0
SV7 =0
SV8 =0
SV9 =0
SV10 =0
SV11 =0
SV12 =0
SV13 =0
SV14 =0
SV15 =0
SV16 =0
OUT101=TRIP
OUT102=CLOSE
OUT103=SV1T
OUT104=0
```

Press RETURN to continue

```
OUT105=0
OUT106=0
OUT107=0
OUT201=0
OUT202=0
OUT203=0
OUT204=0
OUT205=0
OUT206=0
OUT207=0
OUT208=0
OUT209=0
OUT210=0
OUT211=0
OUT212=0
DP1 =IN102
DP2 =52A
DP3 =0
DP4 =0
DP5 =0
```

Press RETURN to continue\

```
DP6 =0
DP7 =0
DP8 =0
DP9 =0
DP10 =0
DP11 =0
DP12 =0
DP13 =0
DP14 =0
DP15 =0
DP16 =0
SS1 =0
SS2 =0
SS3 =0
SS4 =0
SS5 =0
SS6 =0
ER =/51P + /51G + /OUT103
FAULT =51P + 51G
BSYNCH=52A
```

Press RETURN to continue

```
CLMON =0
BKMON =TRIP
E32IV =1
TMB1A =0
TMB2A =0
```

```
TMB3A =0
TMB4A =0
TMB5A =0
TMB6A =0
TMB7A =0
TMB8A =0
TMB1B =0
TMB2B =0
TMB3B =0
TMB4B =0
TMB5B =0
TMB6B =0
TMB7B =0
TMB8B =0
```

```
=>>
```

```
=>>SHO G <ENTER>
```

```
Global Settings:
```

```
TGR = 180.00   NFREQ = 60   PHROT = ABC
DATE_F= MDY   FP_TO = 15.00   SCROLD= 2   FPNGD = IN
LER = 15      PRE = 4       DCLOP = OFF   DCHIP = OFF
IN101D= 0.50  IN102D= 0.50  IN103D= 0.50  IN104D= 0.50
IN105D= 0.50  IN106D= 0.50
IN201D= 0.50  IN202D= 0.50  IN203D= 0.50  IN204D= 0.50
IN205D= 0.50  IN206D= 0.50  IN207D= 0.50  IN208D= 0.50
EBMON = Y     COSP1 = 10000  COSP2 = 150   COSP3 = 12
KASP1 = 1.20  KASP2 = 8.00   KASP3 = 20.00
```

```
=>>
```

```
=>>SHO P <ENTER>
```

```
Port F
```

```
PROTO = SEL
SPEED = 38400   BITS = 8   PARITY= N   STOP = 1
T_OUT = 0      AUTO = Y   RTSCTS= N   FASTOP= N
```

```
=>>
```

```
=>>SHO R <ENTER>
```

```
Sequential Events Recorder trigger lists:
```

```
SER1 =51P 51G 50P1
SER2 =LB3 LB4 IN101 IN102 OUT101 OUT102 OUT103
SER3 =CF 79CY 79LO
```

```
Load Profile settings:
```

```
LDLIST=0
LDAR = 5
```

```
=>>
```

```

=>>SHO T <ENTER>

Text Labels:
NLB1 =          CLB1 =          SLB1 =          PLB1 =
NLB2 =          CLB2 =          SLB2 =          PLB2 =
NLB3 =MANUAL TRIP  CLB3 =RETURN  SLB3 =          PLB3 =TRIP
NLB4 =MANUAL CLOSE CLB4 =RETURN  SLB4 =          PLB4 =CLOSE
NLB5 =          CLB5 =          SLB5 =          PLB5 =
NLB6 =          CLB6 =          SLB6 =          PLB6 =
NLB7 =          CLB7 =          SLB7 =          PLB7 =
NLB8 =          CLB8 =          SLB8 =          PLB8 =
NLB9 =          CLB9 =          SLB9 =          PLB9 =
NLB10 =         CLB10 =         SLB10 =         PLB10 =
NLB11 =         CLB11 =         SLB11 =         PLB11 =
NLB12 =         CLB12 =         SLB12 =         PLB12 =
NLB13 =         CLB13 =         SLB13 =         PLB13 =
NLB14 =         CLB14 =         SLB14 =         PLB14 =
NLB15 =         CLB15 =         SLB15 =         PLB15 =
NLB16 =         CLB16 =         SLB16 =         PLB16 =
DP1_1 =79 ENABLED  DP1_0 =79 DISABLED

Press RETURN to continue
DP2_1 =BREAKER CLOSED  DP2_0 =BREAKER OPEN
DP3_1 =          DP3_0 =
DP4_1 =          DP4_0 =
DP5_1 =          DP5_0 =
DP6_1 =          DP6_0 =
DP7_1 =          DP7_0 =
DP8_1 =          DP8_0 =
DP9_1 =          DP9_0 =
DP10_1=         DP10_0=
DP11_1=         DP11_0=
DP12_1=         DP12_0=
DP13_1=         DP13_0=
DP14_1=         DP14_0=
DP15_1=         DP15_0=
DP16_1=         DP16_0=
79LL =SET RECLOSURES 79SL =RECLOSE COUNT

=>>

```

SSI Command (Voltage Sag/Swell/Interruption Report—Available in Firmware Version 7)

Use the SSI command to view the voltage Sag, Swell, and Interruption report. For more information on SSI reports, see *Section 12: Standard Event Reports, Sag/Swell/Interruption Report, and SER*.

STA Command (Relay Self-Test Status)

The STA command displays the status report, showing the relay self-test information.

To view a status report, enter the command:

```
=>>STA n <ENTER>
```

where **n** is an optional parameter to specify the number of times (1–32767) to repeat the status display. If **n** is not specified, the status report is displayed once. The output of an SEL-351 Relay with wye-connected voltage inputs and no extra I/O board is shown:

```

=>STA <ENTER>

FEEDER 1                               Date: 02/01/97   Time: 12:21:48.226
STATION A

FID=SEL-351-7-R301-V0-D990426         CID=1F00

SELF TESTS
W=Warn   F=Fail
  IA      IB      IC      IN      VA      VB      VC      VS      MOF
OS   -5    -19    -9      -16    35W    9      -6     15     3

      +5V_PS +5V_REG -5V_REG +12V_PS -12V_PS +15V_PS -15V_PS
PS   4.92   5.06  -4.95  12.03 -12.07  14.92 -14.82

      TEMP   RAM    ROM    A/D    CR_RAM EEPROM IO_BRD
      26.8   OK     OK     OK     OK     OK     OK

Relay Enabled

```

STA Command Row and Column Definitions

- FID** FID is the firmware identifier string. It identifies the firmware revision.
- CID** CID is the firmware checksum identifier.
- OS** OS = Offset; displays measured dc offset voltages in millivolts for the current and voltage channels. The MOF (master) status is the dc offset in the A/D circuit when a grounded input is selected.
- PS** PS = Power Supply; displays power supply voltages in Vdc for the power supply outputs.
- TEMP** Displays the internal relay temperature in degrees Celsius.
- RAM, ROM, CR_RAM (critical RAM), and EEPROM**
These tests verify the relay memory components. The columns display OK if memory is functioning properly; the columns display FAIL if the memory area has failed.
- A/D** Analog to Digital convert status.
- IO_BRD** Extra I/O board status (model 0351x1 only—see Table 1.1 and Figure 2.3 and 2.16).

W (Warning) or F (Failure) is appended to the values to indicate an out-of-tolerance condition. The relay latches all self-test warnings and failures in order to capture transient out-of-tolerance conditions. To reset the self-test statuses, use the **STA C** command from Access Level 2:

==>>STA C <ENTER>

The relay responds:

```

Reboot the relay and clear status
Are you sure (Y/N) ?

```

If you select “N” or “n”, the relay displays:

Canceled

and aborts the command.

If you select “Y”, the relay displays:

Rebooting the relay

The relay then restarts (just like powering down, then powering up relay), and all diagnostics are rerun before the relay is enabled.

Refer to Table 13.1 in *Section 13: Testing and Troubleshooting* for self-test thresholds and corrective actions.

TAR Command (Display Relay Element Status)

The TAR command displays the status of front-panel target LEDs or relay elements, whether they are asserted or deasserted. The elements are represented as Relay Word bits and are listed in rows of eight, called Relay Word rows. The first 2 rows correspond to Table 10.7. The remaining rows correspond to the Relay Word as described in *Section 9: Setting the Relay*.

A Relay Word bit is either at a logical 1 (asserted) or a logical 0 (deasserted). Relay Word bits are used in SELOGIC control equations. See *Section 9: Setting the Relay and Appendix G: Setting SELOGIC Control Equations*.

The TAR command does not remap the front-panel target LEDs, as is done in some previous SEL relays. But the execution of the equivalent TAR command via the front-panel display does remap the bottom row of the front-panel target LEDs (see Figure 11.3, pushbutton OTHER).

The TAR command options are:

- | | |
|-------------------|--|
| TAR n k | Shows Relay Word row number n (0–56). k is an optional parameter to specify the number of times (1–32767) to repeat the Relay Word row display. If k is not specified, the Relay Word row is displayed once. |
| TAR name k | Shows Relay Word row containing Relay Word bit name (e.g., TAR 50C displays Relay Word Row 5). Valid names are shown in Table 10.7, and Table 9.4 and Table 9.5. k is an optional parameter to specify the number of times (1–32767) to repeat the Relay Word row display. If k is not specified, the Relay Word row is displayed once. |
| TAR R | Clears front-panel tripping target LEDs TRIP, INST, COMM, SOTF, 50, 51, 81, A, B, C, G, and N. Unlatches the trip logic for testing purposes (see Figure 5.1). Shows Relay Word Row 0.
Note: The TAR R Command cannot reset the latched Targets if a TRIP condition is present. |

Table 10.7: SEL-351 Relay Word and Its Correspondence to TAR Command

TAR 0 (Front-Panel LEDs)	EN	TRIP	INST	COMM	SOTF	50	51	81
TAR 1 (Front-Panel LEDs)	A	B	C	G	N	RS	CY	LO

Command TAR SH1 10 is executed in the following example:

```

=>TAR SH1 10 <ENTER>

79RS  79CY  79LO  SH0  SH1  SH2  SH3  SH4
0      0      1      0      0      1      0      0
0      0      1      0      0      1      0      0
0      0      1      0      0      1      0      0
0      0      1      0      0      1      0      0
0      0      1      0      0      1      0      0
0      0      1      0      0      1      0      0
0      0      1      0      0      1      0      0
0      0      1      0      0      1      0      0
0      0      1      0      0      1      0      0
0      0      1      0      0      1      0      0

79RS  79CY  79LO  SH0  SH1  SH2  SH3  SH4
0      0      1      0      0      1      0      0
0      0      1      0      0      1      0      0

=>

```

Note that Relay Word row containing the SH1 bit is repeated 10 times. In this example, the reclosing relay is in the Lockout State (79LO = logical 1), and the shot is at shot = 2 (SH2 = logical 1). Command TAR 35 will report the same data since the SH1 bit is in Row 35 of the Relay Word.

TIM Command (View/Change Time)

TIM displays the relay clock. To set the clock, type **TIM** and the desired setting, then press **<ENTER>**. Separate the hours, minutes, and seconds with colons, semicolons, spaces, commas, or slashes. To set the clock to 23:30:00, enter:

```

=>TIM 23:30:00 <ENTER>
23:30:00
=>

```

Note: After setting the time, allow at least 60 seconds before powering down the relay or the new setting may be lost.

TRI Command (Trigger Event Report)

Issue the TRI command to generate an event report:

```

=>TRI <ENTER>
Triggered
=>

```

If the serial port AUTO setting = Y, the relay sends the summary event report:

```
FEEDER 1                      Date: 02/02/97   Time: 12:57:01.737
STATION A

Event: TRIG Location: $$$$$$ Shot: 2 Frequency: 60.00
Targets:
Currents (A Pri), ABCNGQ:   235  236  237    0    2    0
==>
```

See *Section 12: Standard Event Reports, Sag/Swell/Interruption Report, and SER* for more information on event reports.

Access Level B Commands

BRE n Command (Preload/Reset Breaker Wear)

Use the BRE W command to preload breaker wear. For example, to preload the breaker wear to 25%, 28%, and 24% for the respective phases, issue the command below.

```
==>BRE W <ENTER>
Breaker Wear Percent Preload

A-phase % = 13 ? 25 <ENTER>
B-phase % = 13 ? 28 <ENTER>
C-phase % = 13 ? 24 <ENTER>
Are you sure (Y/N) ? Y <ENTER>

FEEDER 1                      Date: 02/02/97   Time: 08:44:33.920
STATION A

Rly Trips=    11
IA=    40.7 IB=    40.8 IC=    40.8 kA

Ext Trips=     3
IA=     0.8 IB=     0.9 IC=     1.1 kA

Percent wear: A= 25 B= 28 C= 24

LAST RESET 01/27/97 15:32:59
==>
```

Use the BRE R command to reset the breaker monitor:

```
==>BRE R <ENTER>
Reset Trip Counters and Accumulated Currents/Wear
Are you sure (Y/N) ? Y <ENTER>
FEEDER 1                               Date: 02/03/97   Time: 05:41:07.289
STATION A
Rly Trips=      0
IA=      0.0 IB=      0.0 IC=      0.0 kA
Ext Trips=      0
IA=      0.0 IB=      0.0 IC=      0.0 kA
Percent wear: A=  0 B=  0 C=  0
LAST RESET 02/03/97 05:41:07
```

See *Breaker Monitor* in *Section 8: Breaker Monitor, Metering, and Load Profile Functions* for further details on the breaker monitor.

CLO Command (Close Breaker)

The CLO (CLOSE) command asserts Relay Word bit CC for 1/4 cycle when it is executed. Relay Word bit CC can then be programmed into the CL SELOGIC control equation to assert the CLOSE Relay Word bit, which in turn asserts an output contact (e.g., OUT102 = CLOSE) to close a circuit breaker. See Figure 6.1.

See the Note in the *Set Close* discussion, following Figure 6.1, for more information concerning Relay Word bit CC and its recommended use, as used in the factory settings.

To issue the CLO command, enter the following:

```
=>>CLO <ENTER>
Close Breaker (Y/N) ? Y <ENTER>
Are you sure (Y/N) ? Y <ENTER>
=>>
```

Typing **N** <ENTER> after either of the above prompts will abort the command.

The CLO command is supervised by the main board Breaker jumper (see Table 2.5 and Table 2.6). If the Breaker jumper is not in place (Breaker jumper = OFF), the relay does not execute the CLO command and responds:

```
Aborted: No Breaker Jumper
```


GRO n Command (Change Active Setting Group)

The GRO **n** command changes the active setting group to setting Group **n**. To change to settings Group 2, enter the following:

```
==>GRO 2 <ENTER>
Change to Group 2
Are you sure (Y/N) ? Y <ENTER>
Active Group = 2
==>
```

The relay switches to Group 2 and pulses the ALARM contact. If the serial port AUTO setting = Y, the relay sends the group switch report:

```
==>
FEEDER 1                               Date: 02/02/97   Time: 09:40:34.611
STATION A

Active Group = 2
==>
```

If any of the SELOGIC control equations settings SS1 through SS6 are asserted to logical 1, the active setting group may not change with the GRO command—SELOGIC control equations settings SS1 through SS6 have priority over the GRO command in active setting group control.

For example, assume setting Group 1 is the active setting group and the SS1 setting is asserted to logical 1 (e.g., SS1 = IN101 and optoisolated input IN101 is asserted). An attempt to change to setting Group 2 with the GRO 2 command will not be accepted:

```
==>GRO 2 <ENTER>
No group change (see manual)
Active Group = 1
==>
```

For more information on setting group selection, see *Multiple Setting Groups* in *Section 7: Inputs, Outputs, Timers, and Other Control Logic*.

OPE Command (Open Breaker)

The OPE (OPEN) command asserts Relay Word bit OC for 1/4 cycle when it is executed. Relay Word bit OC can then be programmed into the TR SELOGIC control equation to assert the TRIP Relay Word bit, which in turn asserts an output contact (e.g., OUT101 = TRIP) to trip a circuit breaker. See Figure 5.1.

See the Note following Figure 5.2 and the Note in the *Lockout State* discussion, following Table 6.1, for more information concerning Relay Word bit OC and its recommended use, as used in the factory settings.

To issue the OPE command, enter the following:

```
=>>OPE <ENTER>
Open Breaker (Y/N) ? Y <ENTER>
Are you sure (Y/N) ? Y <ENTER>
=>>
```

Typing **N** <ENTER> after either of the above prompts will abort the command.

The OPE command is supervised by the main board Breaker jumper (see Table 2.5 and Table 2.6). If the Breaker jumper is not in place (Breaker jumper = OFF), the relay does not execute the OPE command and responds:

```
Aborted: No Breaker Jumper
```

PUL Command (Pulse Output Contact)

The PUL command allows you to pulse any of the output contacts for a specified length of time. The command format is:

PUL x y

- where: **x** is the output name (e.g. OUT101, OUT107, ALARM, OUT211—see Figure 7.27 to Figure 7.28).
- y** is the pulse duration (1-30) in seconds. If **y** is not specified, the pulse duration defaults to 1 second.

To pulse OUT101 for 5 seconds:

```
=>>PUL OUT101 5 <ENTER>
Are you sure (Y/N) ? Y <ENTER>
=>>
```

If the response to the “Are you sure (Y/N) ?” prompt is “N” or “n”, the command is aborted.

The PUL command is supervised by the main board Breaker jumper (see Table 2.5 and Table 2.6). If the Breaker is not in place (Breaker jumper = OFF), the relay does not execute the PUL command and responds:

```
Aborted: No Breaker Jumper
```

The relay generates an event report if any of the OUT101 through OUT107 (Models 0351x0, 0351x1, or 0351xY) contacts are pulsed. The PULSE command is primarily used for testing purposes.

Access Level 2 Commands

CON Command (Control Remote Bit)

The CON command is a two-step command that allows you to control Relay Word bits RB1 through RB16 (see Rows 27 and 28 in Table 9.4). At the Access Level 2 prompt, type CON, a space, and the number of the remote bit you wish to control (1-16). The relay responds by repeating your command followed by a colon. At the colon, type the Control subcommand you wish to perform (see Table 10.8).

The following example shows the steps necessary to pulse Remote Bit 5 (RB5):

```
=>>CON 5 <ENTER>
CONTROL RB5: PRB 5 <ENTER>
=>>
```

You must enter the same remote bit number in both steps in the command. If the bit numbers do not match, the relay responds “Invalid Command.”

Table 10.8: SEL-351 Relay Control Subcommands

Subcommand	Description
SRB n	Set Remote Bit n (“ON” position)
CRB n	Clear Remote Bit n (“OFF” position)
PRB n	Pulse Remote Bit n for 1/4 cycle (“MOMENTARY” position)

See *Remote Control Switches* in *Section 7: Inputs, Outputs, Timers, and Other Control Logic* for more information.

COP m n Command (Copy Setting Group)

Copy relay and SELOGIC control equation settings from setting Group **m** to setting Group **n** with the **COP m n** command. Setting group numbers range from 1 to 6. After entering settings into one setting group with the SET and SET L commands, copy them to the other groups with the COP command. Use the SET and SET L commands to modify the copied settings. The relay disables for a few seconds and the ALARM output pulses if you copy settings into the active group. This is similar to a Group Change (see *Section 7: Inputs, Outputs, Timers, and Other Control Logic*).

For example, to copy settings from Group 1 to Group 3 issue the following command:

```
=>>COP 1 3 <ENTER>
Copy 1 to 3
Are you sure (Y/N) ? Y <ENTER>

Please wait...
Settings copied
=>>
```

LOO Command (Loop Back—Available in Firmware Versions 6 and 7)

The LOO (LOOP) command is used for testing the MIRRORRED BITS communications channel. For more information on MIRRORRED BITS, see *Appendix I: MIRRORRED BITS (In Firmware Versions 6 and 7)*. With the transmitter of the communications channel physically looped back to the receiver, the MIRRORRED BITS addressing will be wrong and ROK will be de-asserted. The LOO command tells the MIRRORRED BITS software to temporarily expect to see its own data looped back as its input. In this mode, LBOK will assert if error-free data is received.

The LOO command with just the channel specifier, enables looped back mode on that channel for 5 minutes, while the inputs are forced to the default values.

```
=>> LOO A <ENTER>
Loopback will be enabled on Mirrored Bits channel A for the next 5 minutes.
The RMB values will be forced to default values while loopback is enabled
Are you sure (Y/N) ?
=>>
```

If only one MIRRORRED BITS port is enabled, the channel specifier may be omitted. To enable looped back mode for other than the default 5 minutes, enter the desired number of minutes (1–5000) as a command parameter. To allow the looped back data to modify the RMB values, include the **DATA** parameter.

```
=>> LOO 10 DATA <ENTER>
Loopback will be enabled on Mirrored Bits channel A for the next 10 minutes.
The RMB values will be allowed to change while loopback is enabled.
Are you sure (Y/N) ? N
Canceled.
=>>
```

To disable looped back mode before the selected number of minutes, re-issue the **LOOP** command with the **R** parameter. If both MIRRORRED BITS channels are enabled, omitting the channel specifier in the disable command will cause both channels to be disabled.

```
=>> LOO R <ENTER>
loopback is disabled on both channels.
=>>
```

PAS Command (View/Change Passwords)

PAS allows you to inspect or change existing passwords.

The factory default passwords for Access Levels 1, B, and 2 are:

<u>Access Level</u>	<u>Factory Default Password</u>
1	OTTER
B	EDITH
2	TAIL

To inspect passwords, type:

```
=>>PAS <ENTER>
1:OTTER
B:EDITH
2:TAIL
=>>
```



This device is shipped with default passwords. Default passwords should be changed to private passwords at installation. Failure to change each default password to a private password may allow unauthorized access. SEL shall not be responsible for any damage resulting from unauthorized access.

To change the password for Access Level 1 to Ot3579, enter the following:

```
=>>PAS 1 Ot3579 <ENTER>
Set
=>>
```

Similarly, **PAS B** and **PAS 2** can be used to change the Level B and Level 2 passwords, respectively.

Passwords may include up to six characters. Valid characters consist of: ‘A-Z’, ‘a-z’, ‘0-9’, ‘-’, and ‘.’. Upper- and lower-case letters are treated as different characters. Strong passwords consist of six characters, with at least one special character or digit and mixed case sensitivity, but do not form a name, date, acronym, or word. Passwords formed in this manner are less susceptible to password guessing and automated attacks. Examples of valid, distinct strong passwords include:

Ot3579 A24.68 lh2dcs 4u-lwg .351s.

After entering new passwords, type **PAS <ENTER>** to inspect them. Make sure they are what you intended, and record the new passwords. If the passwords are lost or you wish to operate the relay without password protection, put the main board Password jumper in place (Password jumper = ON). Refer to Tables 2.6 and 2.7 for Password jumper information.

If you wish to disable password protection for a specific access level [even if the Password jumper is not in place (Password jumper = OFF)], simply set the password to **DISABLE**. For example, **PAS 1 DISABLE** disables password protection for Level 1.

SET Command (Change Settings)

The SET command allows the user to view or change the relay settings—see Table 9.1 in *Section 9: Setting the Relay*.

VER Command (Show Relay Configuration and Firmware Version)

The VER command provides relay configuration and information such as nominal current input ratings.

An example printout of the VER command for an SEL-351 Relay follows:

```
Level 2
=>VER <ENTER>
Partnumber: 035150H4254XXX

Mainboard: 0311
Appearance: Horizontal, Conventional
Data FLASH Size: 1024 KBytes
Analog Input Voltage (PT): 150 Vac, wye-connected
Analog Input Current (CT): 5 Amp Phase, 5 Amp Neutral
Extended Relay Features:
    Enhanced Integration Bits & SOE

SELboot checksum 1AB5 OK
FID=SEL-351-5-R303-V0-Z001001-D19990914

No SELboot FID

If above information is unexpected...
contact SEL for assistance

=>>
```

SEL-351-5, -6, -7 RELAY COMMAND SUMMARY

<u>Access Level 0 Command</u>	Access Level 0 is the initial relay access level. The relay automatically returns to Access Level 0 when a serial port time-out setting expires or after a QUIT command. The screen prompt is: =
ACC	Enter Access Level 1. If the main board password jumper is not in place, the relay prompts the user for the Access Level 1 password in order to enter Access Level 1.
<u>Access Level 1 Commands</u>	The Access Level 1 commands allow the user to look at settings information and not change it, and to retrieve and reset event, recorder, and metering data. The screen prompt is: =>
2AC	Enter Access Level 2. If the main board password jumper is not in place, the relay prompts for the entry of the Access Level 2 password in order to enter Access Level 2.
BAC	Enter Breaker Access Level (Access Level B). If the main board password jumper is not in place, the relay prompts the user for the Access Level B password.
BRE	Display breaker monitor data (trips, interrupted current, wear).
COM ¹ p	Show communications summary report (COM report) on MIRRORED BITS™ channel p (where p = A or B) using all failure records in the channel calculations.
COM ¹ p n	Show a COM report for MIRRORED BITS channel p using the latest n failure records (n = 1–512, where 1 is the most recent entry).
COM ¹ p m n	Show COM report for MIRRORED BITS channel p using failure records m through n (m = 1–512).
COM ¹ p d1	Show COM report for MIRRORED BITS channel p using failures recorded on date d1 (see DAT command for date format).
COM ¹ p d1 d2	Show COM report for MIRRORED BITS channel p using failures recorded between dates d1 and d2 inclusive.
COM ¹ ... L	For all COM commands, L causes the specified COM report records to be listed after the summary.
COM ¹ p C	Clears communications records for MIRRORED BITS channel p (or both channels if p is not specified, COM C command).
DAT	Show date.
DAT mm/dd/yy	Enter date in this manner if global Date Format setting, DATE_F, is set to MDY.
DAT yy/mm/dd	Enter date in this manner if global Date Format setting, DATE_F, is set to YMD.
EVE n	Show event report n with 4 samples per cycle (n = 1 to highest numbered event report, where 1 is the most recent report: see HIS command). If n is omitted, (EVE command) most recent report is displayed.
EVE n R	Show event report n in raw (unfiltered) format with 16 samples per cycle resolution.
EVE n C	Show event report n in compressed ASCII format for use with the SEL-5601 Analytic Assistant.
EVE n A	Show event report n with analog section only.
EVE n D	Show event report n with digital section only.
EVE n M	Show event report n with communications section only.
EVE n Sx	Show event report n with x samples per cycle (x = 4 or 16).
EVE n L	Show event report n with 16 samples per cycle (similar to EVE n S16).
EVE n Ly	Show first y cycles of event report n (y = 1 to global setting LER).
GRO	Display active group number.

HIS n	Show brief summary of n latest event reports, where 1 is the most recent entry. If n is not specified, (HIS command) all event summaries are displayed.
HIS C	Clear all event reports from nonvolatile memory.
IRI	Force synchronization attempt of internal relay clock to IRIG-B time-code input.
LDP ¹	Show entire Load Profile (LDP) report.
LDP ¹ n	Show latest n rows in the LDP report (n = 1 to several thousand, where 1 is the most recent entry).
LDP ¹ m n	Show rows m through n in the LDP report (m = 1 to several thousand).
LDP ¹ d1	Show all rows in the LDP report recorded on the specified date (see DAT command for date format).
LDP ¹ d1 d2	Show all rows in the LDP report recorded between dates d1 and d2, inclusive.
LDP ¹ D	Display the number of days of LDP storage capacity before data overwrite will occur.
LDP ¹ C	Clears the LDP report from nonvolatile memory.
MET k	Display instantaneous metering data. Enter k for repeat count (k = 1–32767, if not specified, default is 1).
MET X k	Display same data as MET command with phase-to-phase voltages and Vbase. Enter k for repeat count (k=1–32767, if not specified default is 1)
MET D	Display demand and peak demand data. Select MET RD or MET RP to reset.
MET E	Display energy metering data. Select MET RE to reset.
MET M	Display maximum/minimum metering data. Select MET RM to reset.
QUI	Quit. Returns to Access Level 0. Terminates SEL Distributed Port Switch Protocol (LMD) connection.
SER	Show entire Sequential Events Recorder (SER) report.
SER n	Show latest n rows in the SER report (n = 1–512, where 1 is the most recent entry).
SER m n	Show rows m through n in the SER report (m = 1–512).
SER d1	Show all rows in the SER report recorded on the specified date (see DAT command for date format).
SER d1 d2	Show all rows in the SER report recorded between dates d1 and d2, inclusive.
SER C	Clears SER report from nonvolatile memory.
SHO n	Show relay settings (overcurrent, reclosing, timers, etc.) for group n (n = 1–6, if not specified, default is active setting group).
SHO n L	Show SELOGIC [®] Control Equation settings for group n (n = 1–6, if not specified, default is the SELOGIC Control Equations for the active setting group).
SHO G	Show global settings.
SHO R	Show SER and LDP Recorder ¹ settings.
SHO T	Show text label settings.
SHO P p	Show serial port p settings, (p = 1, 2, 3, or F; if not specified, default is active port).
SHO ... name	For all SHO commands, jump ahead to specific setting by entering setting name.
SSI ²	Show entire Voltage Sag/Swell/Interruption (SSI) report.
SSI ² n	Show latest n rows in SSI report (n = 1 to several thousand, where 1 is the most recent entry).
SSI ² m n	Show rows m through n in SSI report (m = 1 to several thousand).
SSI ² d1	Show all rows in SSI report recorded on the specified date (see DAT command for date format).
SSI ² d1 d2	Show all rows in SSI report recorded between dates d1 and d2, inclusive.

SSI ² C	Clears SSI report from nonvolatile memory.
SSI ² R	Resets Vbase element. See Vbase initialization.
SSI ² T	Trigger the SSI recorder.
STA	Show relay self-test status.
TAR R	Reset front-panel tripping targets.
TAR n k	Display Relay Word row. If n = 0–56, display row n. If n is an element name (e.g., 50A1) display row containing element n. Enter k for repeat count (k = 1–32767, if not specified, default is 1).
TIM	Show or set time (24 hour time). Show current relay time by entering TIM. Set the current time by entering TIM followed by the time of day (e.g., set time 22:47:36 by entering TIM 22:47:36).
TRI	Trigger an event report.
<u>Access Level B Commands</u>	Access Level B commands primarily allow the user to operate the breaker and output contacts. All Access Level 1 commands can also be executed from Access Level B. The screen prompt is: ==>
BRE n	Enter BRE W to preload breaker wear. Enter BRE R to reset breaker monitor data.
CLO	Close circuit breaker (assert Relay Word bit CC).
GRO n	Change active group to group n (n = 1–6).
OPE	Open circuit breaker (assert Relay Word bit OC).
PUL n k	Pulse output contact n (where n is one of ALARM, OUT101–OUT107, OUT201–OUT212) for k seconds. Specify parameter n; k = 1–30 seconds; if not specified, default is 1.
<u>Access Level 2 Commands</u>	The Access Level 2 commands allow unlimited access to relay settings, parameters, and output contacts. All Access Level 1 and Access Level B commands are available from Access Level 2. The screen prompt is: ==>
CON n	Control Relay Word bit RBn (Remote Bit n; n = 1–16). Execute CON n and the relay responds: CONTROL RBn. Then reply with one of the following: SRB n set Remote Bit n (assert RBn). CRB n clear Remote Bit n (deassert RBn). PRB n pulse Remote Bit n [assert RBn for 1/4 cycle].
COP m n	Copy relay and logic settings from group m to group n (m and n are numbers 1–6).
LOO ¹ p t	Set MIRRORING BITS port p to loopback (p = A or B). The received MIRRORING BITS elements are forced to default values during the loopback test; t specifies the loopback duration in minutes (t = 1–5000, default is 5).
LOO ¹ p DATA	Set MIRRORING BITS port p to loopback. DATA allows the received MIRRORING BITS elements to change during the loopback test.
PAS	Show existing Access Level 1, Level B, and Level 2 passwords.
PAS 1 xxxxxx	Change Access Level 1 password to xxxxxx.
PAS B xxxxxx	Change Access Level B password to xxxxxx.
PAS 2 xxxxxx	Change Access Level 2 password to xxxxxx.
	Entering DISABLE as the password disables the password requirement for the specified access level.

SET n	Change relay settings (overcurrent, reclosing, timers, etc.) for group n (n = 1–6, if not specified, default is active setting group).
SET n L	Change SELOGIC Control Equation settings for group n (n = 1–6, if not specified, default is the SELOGIC Control Equations for the active setting group).
SET G	Change global settings.
SET R	Change SER and LDP Recorder ¹ settings.
SET T	Change text label settings.
SET P p	Change serial port p settings, (p = 1, 2, 3, or F; if not specified, default is active port).
SET ... name	For all SET commands, jump ahead to specific setting by entering setting name.
SET ... TERSE	For all SET commands, TERSE disables the automatic SHO command after settings entry.
STA C	Resets self-test warnings/failures and reboots the relay.
VER	Show relay configuration and firmware version.

Key Stroke Commands

Ctrl - Q	Send XON command to restart communications port output previously halted by XOFF.
Ctrl - S	Send XOFF command to pause communications port output.
Ctrl - X	Send CANCEL command to abort current command and return to current access level prompt.

Key Stroke Commands when using SET command

<ENTER>	Retains setting and moves on to next setting.
^ <ENTER>	Returns to previous setting.
< <ENTER>	Returns to previous setting section.
> <ENTER>	Skips to next setting section.
END <ENTER>	Exits setting editing session, then prompts user to save settings.
Ctrl - X	Aborts setting editing session without saving changes.

¹ Available in firmware versions 6 and 7.

² Available in firmware version 7.

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SECTION 11: FRONT-PANEL INTERFACE

INTRODUCTION

This section describes how to get information, make settings, and execute control operations from the relay front panel. It also describes the default displays.

FRONT-PANEL PUSHBUTTON OPERATION

Overview

Note in Figure 11.1 that most of the pushbuttons have dual functions (primary/secondary).

A primary function is selected first (e.g., METER pushbutton).

After a primary function is selected, the pushbuttons then revert to operating on their secondary functions (CANCEL, SELECT, left/right arrows, up/down arrows, EXIT). For example, after the METER pushbutton is pressed, the up/down arrows are used to scroll through the front-panel metering screens. The primary functions are activated again when the present selected function (metering) is exited (press EXIT pushbutton) or the display goes back to the default display after no front-panel activity for a settable time period (see global setting FP_TO in Settings Sheet 20 of 27 at the end of *Section 9: Setting the Relay*; relay shipped with FP_TO = 15 minutes).

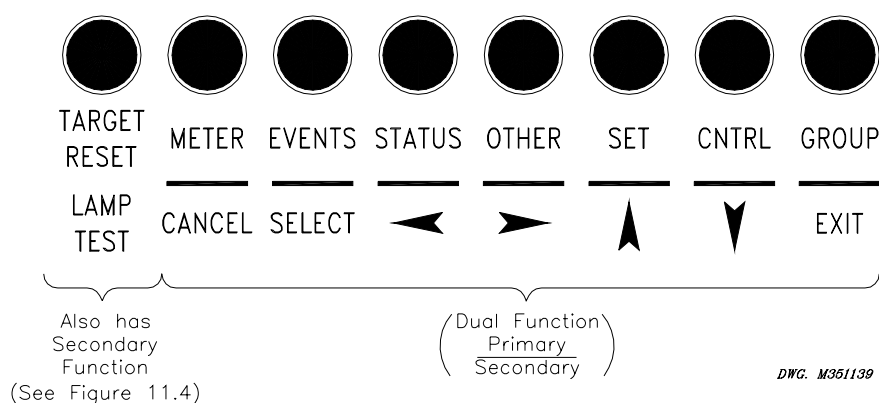
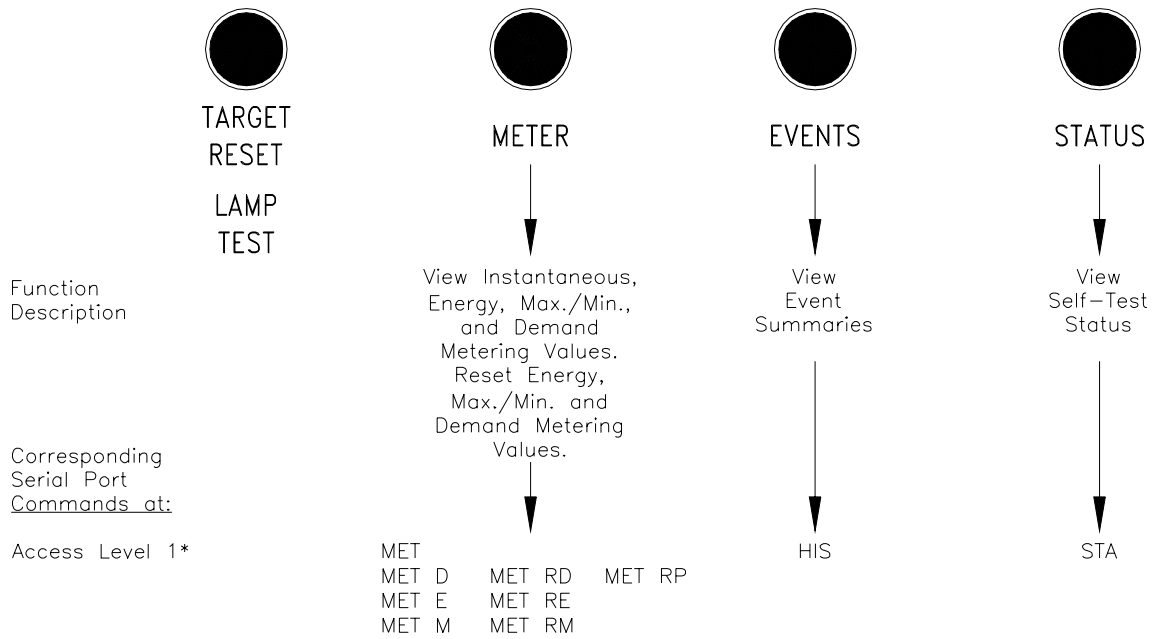


Figure 11.1: SEL-351 Relay Front-Panel Pushbuttons—Overview

Primary Functions

Note in Figure 11.2 and Figure 11.3 that the front-panel pushbutton primary functions correspond to serial port commands—both retrieve the same information or perform the same function. To get more detail on the information provided by the front-panel pushbutton primary functions, refer to the corresponding serial port commands in Table 10.5 in *Section 10: Serial Port Communications and Commands*. For example, to get more information on the metering values available via the front-panel METER pushbutton, refer to the *MET Command (Metering Data)* in *Section 10*.

Some of the front-panel primary functions do not have serial port command equivalents. These are discussed in the following *Functions Unique to the Front-Panel Interface*.



* Front-panel pushbutton functions that correspond to Access Level 1 serial port commands do not require the entry of the Access Level 1 password through the front panel.

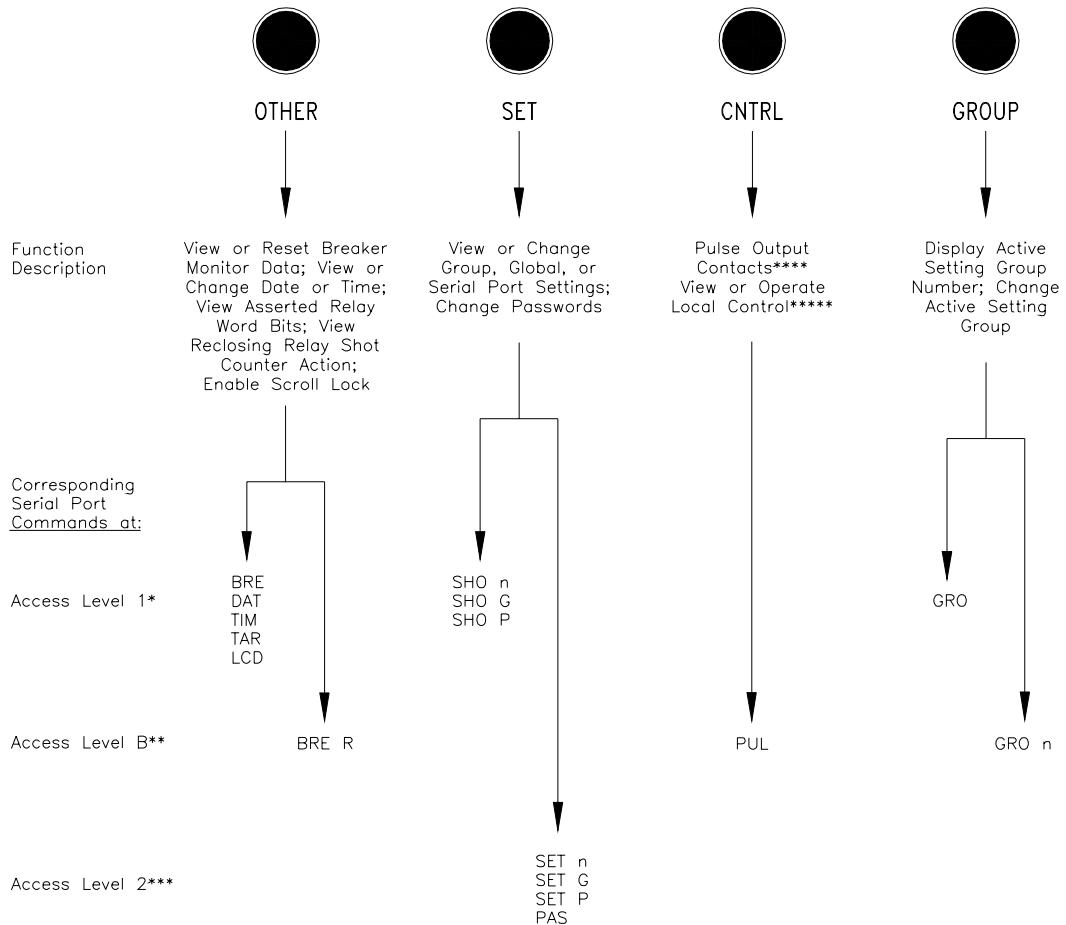
DWG. M351140

Figure 11.2: SEL-351 Relay Front-Panel Pushbuttons—Primary Functions

Front-Panel Password Security

Refer to the comments at the bottom of Figure 11.3 concerning Access Level B and Access Level 2 passwords. See *PAS Command (View/Change Password)* in *Section 10* for the list of default passwords and for more information on changing passwords.

To enter the Access Level B and Access Level 2 passwords from the front panel (if required), use the left/right arrow pushbuttons to underscore a password digit position. Use the up/down arrow pushbuttons to then change the digit. Press the SELECT pushbutton once the correct Access Level B or Access Level 2 password is ready to enter.



- * Front-panel pushbutton functions that correspond to Access Level 1 serial port commands do not require the entry of the Access Level 1 password through the front panel.
- ** Front-panel pushbutton functions that correspond to Access Level B or Access Level 2 passwords through the front panel if the main board Password jumper is not in place (see Tables 2.6 and 2.7).
- *** Front-panel pushbutton functions that correspond to Access Level 2 serial port commands do require the entry of the Access Level 2 password through the front panel if the main board Password jumper is not in place (see Tables 2.6 and 2.7).
- **** Output contacts are pulsed for only 1 second from the front panel.
- ***** Local control is not available through the serial port and does not require the entry of a password.

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Figure 11.3: SEL-351 Relay Front-Panel Pushbuttons—Primary Functions (continued)

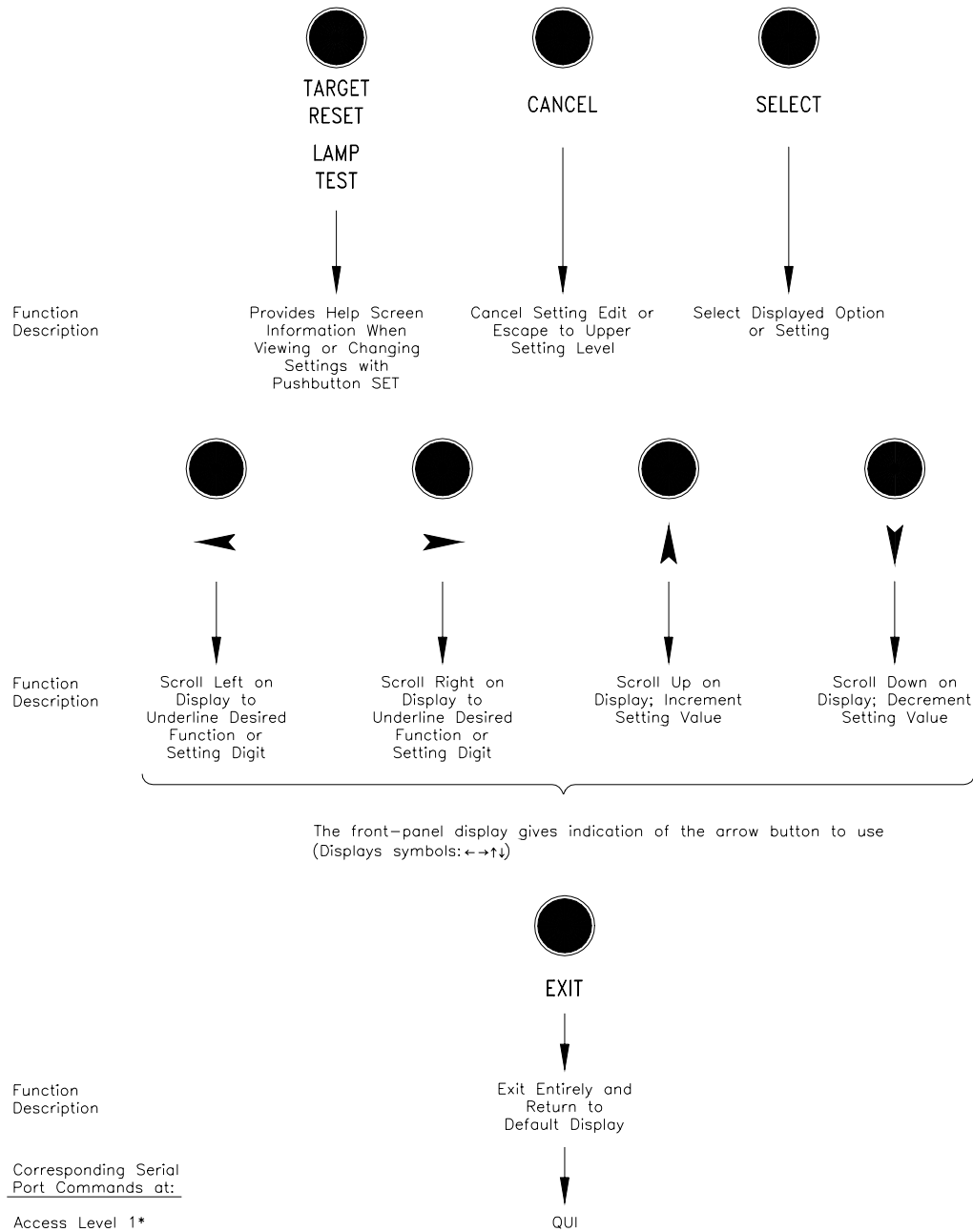
Secondary Functions

After a primary function is selected (see Figure 11.2 and Figure 11.3), the pushbuttons then revert to operating on their secondary functions (see Figure 11.4).

Use the left/right arrows to underscore a desired function. Then press the SELECT pushbutton to select the function.

Use left/right arrows to underscore a desired setting digit. Then use the up/down arrows to change the digit. After the setting changes are complete, press the SELECT pushbutton to select/enable the setting.

Press the CANCEL pushbutton to abort a setting change procedure and return to the previous display. Press the EXIT pushbutton to return to the default display and have the primary pushbutton functions activated again (see Figure 11.2 and Figure 11.3).



* Front-panel pushbutton functions that correspond to Access Level 1 serial port commands do not require the entry of the Access Level 1 password through the front panel.

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Figure 11.4: SEL-351 Relay Front-Panel Pushbuttons—Secondary Functions

FUNCTIONS UNIQUE TO THE FRONT-PANEL INTERFACE

Three front-panel primary functions do not have serial port command equivalents. These are:

- Reclosing relay shot counter screen (accessed via the OTHER pushbutton)
- Local control (accessed via the CNTRL pushbutton)
- Modified rotating display with scroll lock control (accessed via the OTHER pushbutton)

Reclosing Relay Shot Counter Screen

Use this screen to see the progression of the shot counter during reclosing relay testing.

Access the reclosing relay shot counter screen via the OTHER pushbutton. The following screen appears:

```
DATE   TIME   79
TAR BRK_MON LCD
```

Scroll right with the right arrow button and select function “79.” Upon selecting function “79,” the following screen appears (shown here with example settings):

```
SET RECLOSURES=2
RECLOSE COUNT =0      (or = 2)
```

If the reclosing relay doesn’t exist (see *Reclosing Relay* in *Section 6: Close and Reclose Logic*), the following screen appears:

```
No Reclosing set
```

The corresponding text label settings (shown with factory default settings) are:

79LL = SET RECLOSURES (Last Shot Label—limited to 14 characters)
79SL = RECLOSE COUNT (Shot Counter Label—limited to 14 characters)

These text label settings are set with the SET T command or viewed with the SHOWSET T command via the serial port [see *Section 9: Setting the Relay* and *SHO Command (Show/View Settings)* in *Section 10: Serial Port Communications and Commands*].

The top numeral in the above example screen (SET RECLOSURES=2) corresponds to the “last shot” value, which is a function of the number of set open intervals. There are two set open intervals in the factory default settings, thus two reclosures (shots) are possible in a reclose sequence.

The bottom numeral in the above example screen [RECLOSE COUNT = 0 (or = 2)] corresponds to the “present shot” value. If the breaker is closed and the reclosing relay is reset (RS LED on front panel is illuminated), RECLOSE COUNT = 0. If the breaker is open and the reclosing relay is locked out after a reclose sequence (LO LED on front panel is illuminated), RECLOSE COUNT = 2.

Reclosing Relay Shot Counter Screen Operation (With Factory Settings)

With the breaker closed and the reclosing relay in the reset state (front-panel RS LED illuminated), the reclosing relay shot counter screen appears as:

```
SET RECLOSURES=2
RECLOSE COUNT =0
```

The relay trips the breaker open, and the reclosing relay goes to the reclose cycle state (front-panel CY LED illuminates). The reclosing relay shot counter screen still appears as:

```
SET RECLOSURES=2
RECLOSE COUNT =0
```

The first open interval (e.g., 79OI1 = 30) times out, the shot counter increments from 0 to 1, and the relay recloses the breaker. The reclosing relay shot counter screen shows the incremented shot counter:

```
SET RECLOSURES=2
RECLOSE COUNT =1
```

The relay trips the breaker open again. The reclosing relay shot counter screen still appears as:

```
SET RECLOSURES=2
RECLOSE COUNT =1
```

The second open interval (e.g., 79OI2 = 600) times out, the shot counter increments from 1 to 2, and the relay recloses the breaker. The reclosing relay shot counter screen shows the incremented shot counter:

```
SET RECLOSURES=2
RECLOSE COUNT =2
```

If the relay trips the breaker open again, the reclosing relay goes to the lockout state (front-panel LO LED illuminates). The reclosing relay shot counter screen still appears as:

```
SET RECLOSURES=2
RECLOSE COUNT =2
```

If the breaker is closed, the reclosing relay reset timer times out (e.g., 79RSLD = 300), the relay goes to the reset state (front-panel LO LED extinguishes and RS LED illuminates), and the shot counter returns to 0. The reclosing relay shot counter screen appears as:

```
SET RECLOSURES=2
RECLOSE COUNT =0
```

Local Control

Use local control to enable/disable schemes, trip/close breakers, etc., via the front panel.

In more specific terms, local control asserts (sets to logical 1) or deasserts (sets to logical 0) what are called local bits LB1 through LB16. These local bits are available as Relay Word bits and are used in SELOGIC[®] control equations (see Row 25 in Table 9.4).

Local control can emulate the following switch types in Figure 11.5 through Figure 11.7.

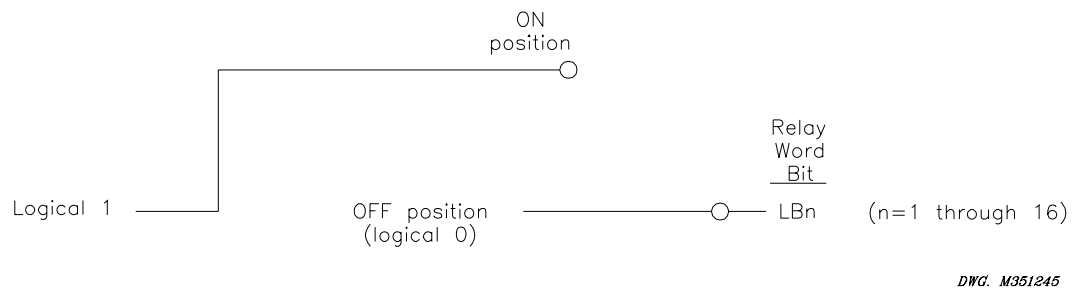


Figure 11.5: Local Control Switch Configured as an ON/OFF Switch

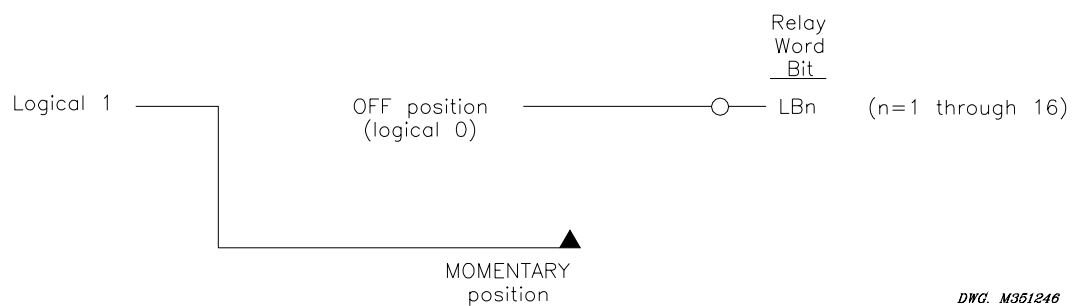


Figure 11.6: Local Control Switch Configured as an OFF/MOMENTARY Switch

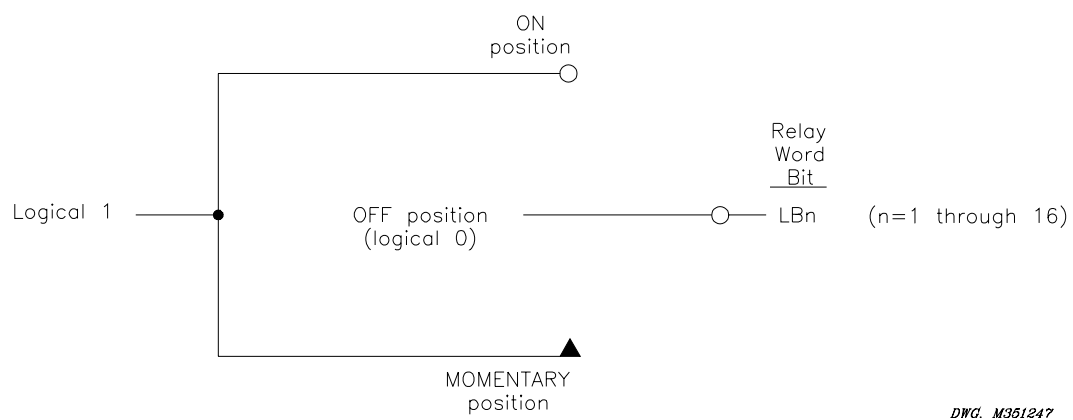


Figure 11.7: Local Control Switch Configured as an ON/OFF/MOMENTARY Switch

Local control switches are created by making corresponding switch position label settings. These text label settings are set with the SET T command or viewed with the SHO T command via the serial port [see *Section 9: Setting the Relay* and *SHO Command (Show/View Settings)* in *Section 10: Serial Port Communications and Commands*]. See *Local Control Switches* in *Section 7: Inputs, Outputs, Timers, and Other Control Logic* for more information on local control.

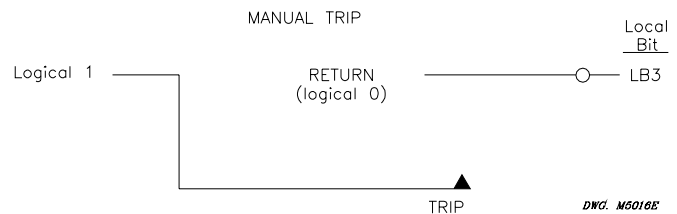
View Local Control (With Factory Settings)

Access local control via the CNTRL pushbutton. If local control switches exist (i.e., corresponding switch position label settings were made), the following message displays with the rotating default display messages.

Press CNTRL for
Local Control

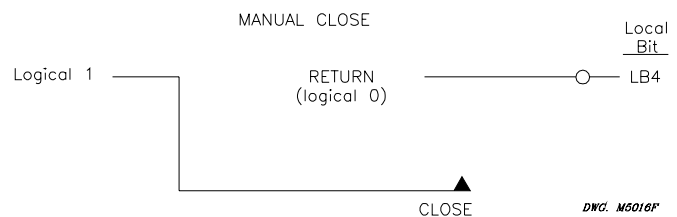
Press the CNTRL pushbutton, and the first set local control switch displays (shown here with factory default settings):

MANUAL TRIP ←→
Position: RETURN



Press the right arrow pushbutton, and scroll to the next example local control switch:

MANUAL CLOSE ←→
Position: RETURN



The MANUAL TRIP: RETURN/TRIP and MANUAL CLOSE: RETURN/CLOSE switches are both OFF/MOMENTARY switches (see Figure 11.6).

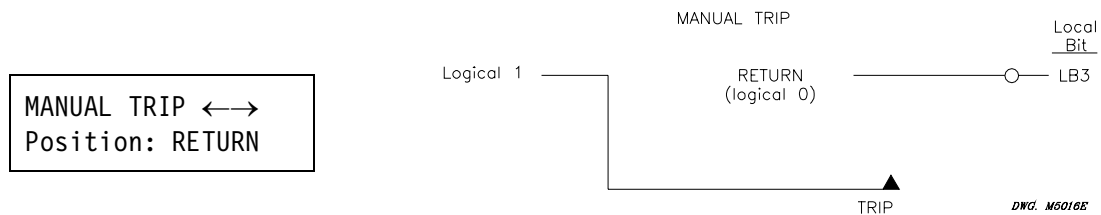
There are no more local control switches in the factory default settings. Press the right arrow pushbutton, and scroll to the “output contact testing” function:

Output Contact←→
Testing

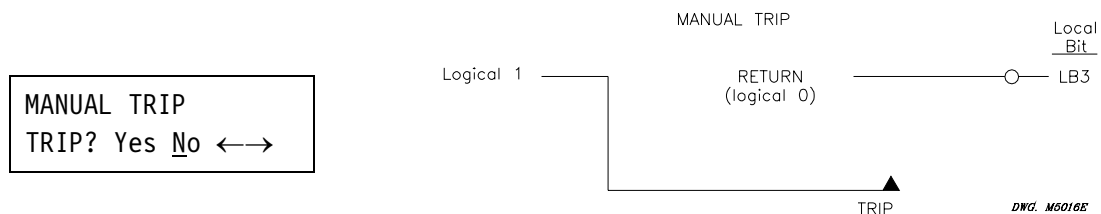
This front-panel function provides the same function as the serial port PUL command (see Figure 11.3).

Operate Local Control (With Factory Settings)

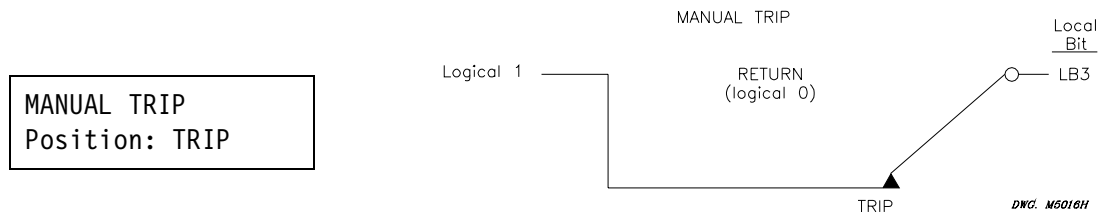
Press the right arrow pushbutton, and scroll back to the first set local control switch in the factory default settings:



Press the SELECT pushbutton, and the operate option for the displayed local control switch displays:



Scroll left with the left arrow button and then select “Yes”. The display then shows the new local control switch position:



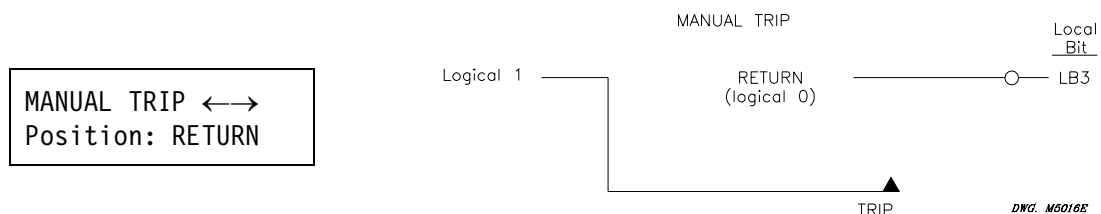
Because this is an OFF/MOMENTARY type switch, the MANUAL TRIP switch returns to the RETURN position after momentarily being in the TRIP position. Technically, the MANUAL TRIP switch (being an OFF/MOMENTARY type switch) is in the:

TRIP position for one processing interval (1/4 cycle; long enough to assert the corresponding local bit LB3 to logical 1).

and then returns to the:

RETURN position (local bit LB3 deasserts to logical 0 again).

On the display, the MANUAL TRIP switch is shown to be in the TRIP position for 2 seconds (long enough to be seen), and then it returns to the RETURN position:



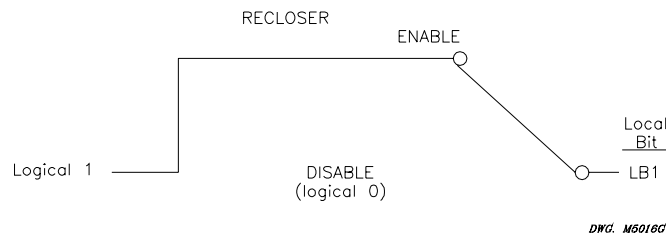
The MANUAL CLOSE switch is an OFF/MOMENTARY type switch, like the MANUAL TRIP switch, and operates similarly.

See *Local Control Switches* in *Section 7: Inputs, Outputs, Timers, and Other Control Logic* for details on how local bit outputs LB3 and LB4 are set in SELOGIC control equation settings to respectively trip and close a circuit breaker.

Local Control State Retained When Relay Deenergized

Local bit states are stored in nonvolatile memory, so when power to the relay is turned off, the local bit states are retained.

For example, suppose the local control switch with local bit output LB1 is configured as an ON/OFF type switch (see Figure 11.5). Additionally, suppose it is used to enable/disable reclosing. If local bit LB1 is at logical 1, reclosing is enabled:



If power to the relay is turned off and then turned on again, local bit LB1 remains at logical 1, and reclosing is still enabled. This is akin to a traditional panel, where enabling/disabling of reclosing and other functions is accomplished by panel-mounted switches. If dc control voltage to the panel is lost and then restored again, the switch positions are still in place. If the reclosing switch is in the enable position (switch closed) before the power outage, it will be in the same position after the outage when power is restored.

Note: In the factory default settings, the reclose enable/disable function is provided by optoisolated input IN102 with the following SELOGIC control equation drive-to-lockout setting:

$$79DTL = !IN102 + LB3 \quad [=NOT(IN102) + LB3]$$

Local bit LB3 is the output of the previously discussed local control switch configured as a manual trip switch. The relay is driven to lockout for any manual trip via LB3.

When input IN102 is energized (IN102 = logical 1), reclosing is enabled (not driven-to-lockout):

$$79DTL = !IN102 + \dots = !(logical\ 1) + \dots = NOT(logical\ 1) + \dots = logical\ 0 + \dots$$

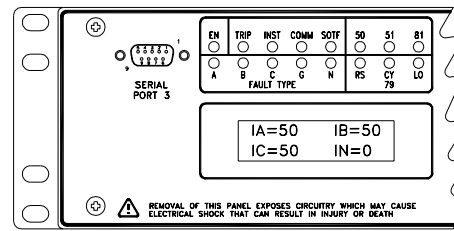
If local bit LB1 is substituted for input IN102 to provide the reclose enable/disable function, the SELOGIC control equation drive-to-lockout setting is set as follows:

$$79DTL = !LB1 + LB3 \quad [=NOT(LB1) + LB3]$$

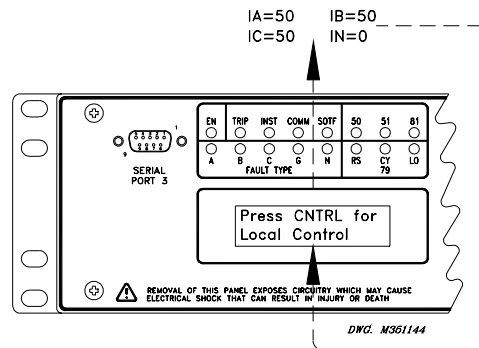
See *Drive-to-Lockout and Drive-to-Last Shot Settings (79DTL and 79DLS, respectively)* in *Section 6: Close and Reclose Logic* for more information on setting 79DTL.

ROTATING DEFAULT DISPLAY

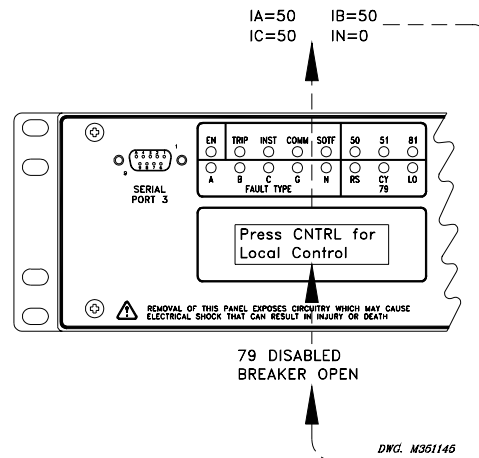
The channel IA, IB, IC, and IN current values (in A primary) display continually if no local control is operational (i.e., no corresponding switch position label settings were made) and no display point labels are enabled for display.



The “Press CNTRL for Local Control” message displays in rotation (display time = SCROLL) with the default metering screen if at least one local control switch is operational. It is a reminder of how to access the local control function. See the preceding discussion in this section and *Local Control Switches* in *Section 7: Inputs, Outputs, Timers, and Other Control Logic* for more information on local control.



If display point labels (e.g., “79 DISABLED” and “BREAKER OPEN”) are enabled for display, they also enter into the display rotation (display time = SCROLL).



The following table and figures demonstrate the correspondence between changing display point states (e.g., DP1 and DP2) and enabled display point labels (DP1_1/DP1_0 and DP2_1/DP2_0, respectively). The display time is equal to global setting SCROLL for each screen.

The display point example settings are:

- DP1 = IN102 (optoisolated input IN102)
- DP2 = 52A (breaker status, see Figure 7.3)

Optoisolated input IN102 is used as a recloser enable/disable. 52A is the circuit breaker status (see *Optoisolated Inputs* in *Section 7: Inputs, Outputs, Timers and Other Control Logic*).

**Display Points
(SELOGIC Control Equation Settings)**

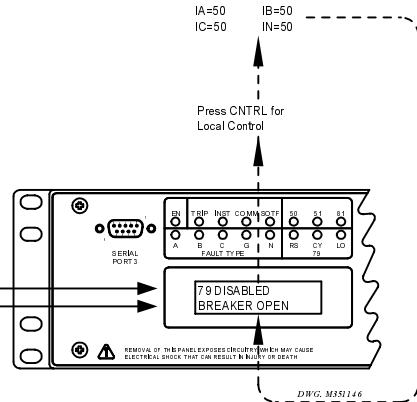
Example Display Point States

Display Point Label Settings

DP1 = IN102 = logical 0
 DP1_1 = 79 ENABLED
 DP1_0 = 79 DISABLED

DP2 = 52A = logical 0
 DP2_1 = BREAKER CLOSED
 DP2_0 = BREAKER OPEN

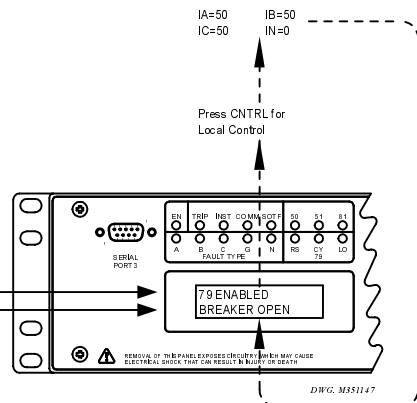
DWG. M551265A



DP1 = IN102 = logical 1
 DP1_1 = 79 ENABLED
 DP1_0 = 79 DISABLED

DP2 = 52A = logical 0
 DP2_1 = BREAKER CLOSED
 DP2_0 = BREAKER OPEN

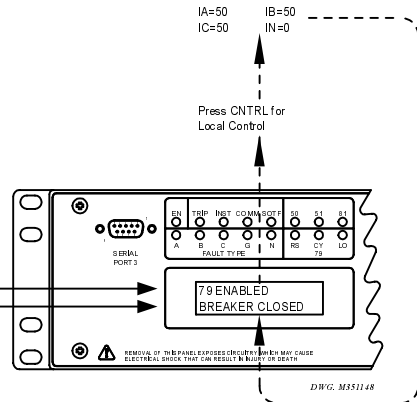
DWG. M551265B



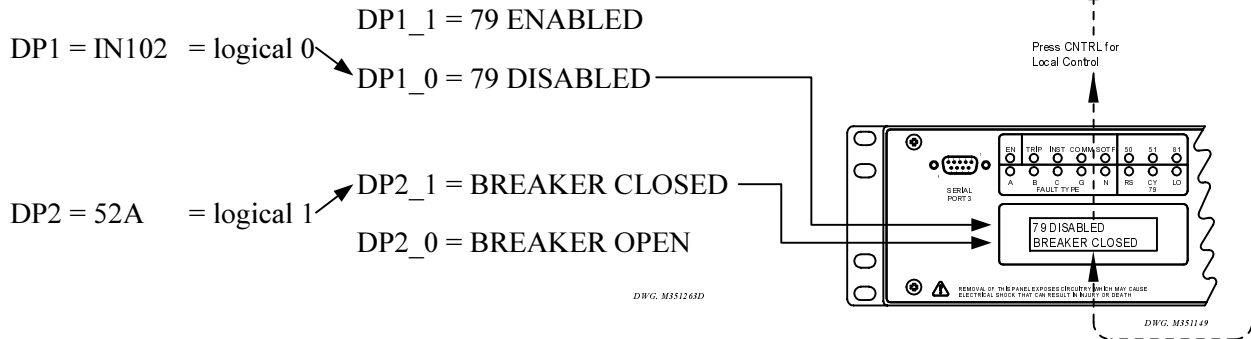
DP1 = IN102 = logical 1
 DP1_1 = 79 ENABLED
 DP1_0 = 79 DISABLED

DP2 = 52A = logical 1
 DP2_1 = BREAKER CLOSED
 DP2_0 = BREAKER OPEN

DWG. M551265C



<u>Display Points (SELOGIC Control Equation Settings)</u>	<u>Example Display Point States</u>	<u>Display Point Label Settings</u>
---	-------------------------------------	-------------------------------------



In the preceding example, only two display points (DP1 and DP2) and their corresponding display point labels are set. If additional display points and corresponding display point labels are set, the additional enabled display point labels join the rotation (display time = SCROLL) on the front-panel display. The SCROLL setting is made with the SET G command and reviewed with the SHO G command.

Display point label settings are set with the SET T command or viewed with the SHO T command via the serial port [see *Section 9: Setting the Relay* and *SHO Command (Show/View Settings)* in *Section 10: Serial Port Communications and Commands*].

For more detailed information on the logic behind the rotating default display, see *Rotating Default Display* in *Section 7: Inputs, Outputs, Timers, and Other Control Logic*.

Scroll Lock Control of Front-Panel LCD

The rotating default display can be locked on a single screen. (See *Rotating Default Display* in *Section 7: Inputs, Output, Timers, and Other Control Logic*). Access the scroll lock control with the OTHER push-button.

DATE	TIME	79
TAR	BRK_MON	LCD

Select LCD for Scroll Lock Control mode. The rotating display will then appear, and the scroll mode reminder screen will appear every 8 seconds for 1 second as a reminder that the display is in Scroll Lock Control mode.

Scroll lock OFF
SELECT to Lock

Stop Scrolling (Lock)

When in the Scroll Lock Control mode, press the SELECT key to stop display rotation. Scrolling can be stopped on any of the display point screens, or on the current-meter display screen. While rotation is stopped, the active display is updated continuously so that current or display point changes can be seen. If no button is pressed for eight seconds, the reminder message will appear for 1 second, followed by the active screen.

Scroll lock ON SELECT to Unlock

Restart Scrolling (Unlock)

The SELECT key unlocks the LCD and resumes the rotating display.

Single Step

From the Scroll Locked state, single-step through the display screens, by pressing the SELECT key twice. Wait for the first press to display the next screen as the active display, then press the SELECT key a second time to freeze scrolling.

Exit

Press the EXIT key to leave Scroll Lock Control and return the rotating display to normal operation.

Cancel

Press the CANCEL key to return to the OTHER menu.

DATE	TIME	79
TAR	BRK_MON	LCD

Front-Panel Neutral / Ground Current Display

Global setting FPNGD (Front-Panel Neutral/Ground Display) selects whether IG, IN, or neither is displayed on the front-panel rotating display. Setting choices are:

FPNGD = IN

IA=	1	IB=	1
IC=	1	IN=	1

FPNGD = IG

IA=	1	IB=	1
IC=	1	IG=	1

FPNGD = OFF

IA=	1	IB=	1
IC=	1		

Additional Rotating Default Display Example

See Figure 5.17 and accompanying text in *Section 5: Trip and Target Logic* for an example of resetting a rotating default display with the TARGET RESET pushbutton.

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SECTION 12: STANDARD EVENT REPORTS, SAG/SWELL/ INTERRUPTION REPORT, AND SER

INTRODUCTION

The SEL-351 Relay offers two styles of event reports:

- Standard 15/30-cycle event reports.
- Sequential events recorder (SER) report.

Resolution: 1 ms

Accuracy: +1/4 cycle

The event reports contain date, time, current, voltage, frequency, relay element, optoisolated input, output contact, and fault location information.

The relay generates (triggers) standard 15/30-cycle event reports by fixed and programmable conditions. These reports show information for 15 or 30 continuous cycles which depends on the LER setting (see the following subsection). The relay stores the most recent event report data in nonvolatile memory. Twenty-nine 15-cycle or fifteen 30-cycle reports are maintained; if more reports are triggered, the latest event report overwrites the oldest event report. See Figure 12.2 for an example standard 15-cycle event report.

The relay adds lines in the sequential events recorder (SER) report for a change of state of a programmable condition. The SER lists date and time-stamped lines of information each time a programmed condition changes state. The relay stores the latest 512 lines of the SER report in nonvolatile memory. If the report fills up, newer rows overwrite the oldest rows in the report. See Figure 12.5 for an example SER report.

The SEL-351-7 Relay offers an additional style of event report:

- Sag/Swell/Interruption (SSI) report

The SSI report (available in Firmware Version 7) records date, time, current, voltage, and Voltage Sag/Swell/Interruption (VSSI) element status during voltage disturbances, as determined by programmable settings, VINT, VSAG, and VSWELL. When the relay is recording a disturbance, entries are automatically added to the SSI report at one of four rates: once per quarter-cycle, once per cycle, once per 64-cycles, or once per day. The most recent 3,855 SSI entries are always available from nonvolatile memory, and up to 3,855 older entries may also be available. See Figure 12.6 for an example SSI report.

STANDARD 15/30-CYCLE EVENT REPORTS

See Figure 12.2 for an example event report (**Note:** Figure 12.2 is on multiple pages).

Event Report Length (Settings LER and PRE)

The SEL-351 Relay provides user-programmable event report length and predefault length. Event report length is either 15 or 30 cycles. Prefault length ranges from 1 to 29 cycles. Prefault length is the first part of the event report that precedes the event report triggering point.

Set the event report length with the LER setting. Set the predefault length with the PRE setting. See the SET G command in Table 9.1 and corresponding Settings Sheet 20 of 27 in **Section 9: Setting the Relay** for instructions on setting the LER and PRE settings.

Changing the LER setting will erase all events stored in nonvolatile memory. Changing the PRE setting has no effect on the nonvolatile reports.

Standard Event Report Triggering

The relay triggers (generates) a standard event report when any of the following occur:

- Relay Word bit TRIP asserts
- Programmable SELOGIC[®] control equation setting ER asserts to logical 1
- TRI (Trigger Event Reports) serial port command executed
- Output contacts OUT101 through OUT107 (Models 0351x0, 0351x1, and 0351xY) pulsed via the serial port or front-panel PUL (Pulse Output Contact) command

Relay Word Bit TRIP

Refer to Figure 5.1. If Relay Word bit TRIP asserts to logical 1, an event report is automatically generated. Thus, any condition that causes a trip does not have to be entered in SELOGIC control equation setting ER.

For example, SELOGIC control equation trip setting TR is unsupervised. Any trip condition that asserts in setting TR causes the TRIP Relay Word bit to assert immediately. The factory setting for trip setting TR is:

$$TR = 51PT + 51GT + 81D1T + LB3 + 50P1*SH0$$

If any of the individual conditions 51PT, 51GT, 81D1T, LB3, or 50P1*SH0 assert, Relay Word bit TRIP asserts, and an event report is automatically generated. Thus, these conditions do not have to be entered in SELOGIC control equation setting ER.

Relay Word bit TRIP (in Figure 5.1) is usually assigned to an output contact for tripping a circuit breaker (e.g., SELOGIC control equation setting OUT101 = TRIP).

Programmable SELOGIC Control Equation Setting ER

The programmable SELOGIC control equation event report trigger setting ER is set to trigger standard event reports for conditions other than trip conditions. When setting ER sees a logical 0

to logical 1 transition, it generates an event report (if the SEL-351 Relay is not already generating a report that encompasses the new transition). The factory setting is:

$$ER = /51P + /51G + /OUT103$$

The elements in this example setting are:

- 51P Maximum phase current above pickup setting 51PP for phase time-overcurrent element 51PT (see Figure 3.14).
- 51G Residual ground current above pickup setting 51GP for residual ground time-overcurrent element 51GT (see Figure 3.18).
- OUT103 Output contact OUT103 is set as a breaker failure trip output (see Figure 7.27).

Note the rising edge operator / in front of each of these elements. See *Appendix G: Setting SELOGIC Control Equations* for more information on rising edge operators and SELOGIC control equations in general.

Rising edge operators are especially useful in generating an event report at fault inception and then generating another later if a breaker failure condition occurs. For example, at the inception of a ground fault, pickup indicator 51G asserts and an event report is generated:

$$ER = \dots + /51G + \dots = \text{logical 1 (for one processing interval)}$$

Even though the 51G pickup indicator will remain asserted for the duration of the ground fault, the rising edge operator / in front of 51G (/51G) causes setting ER to be asserted for only one processing interval.

If the fault is not interrupted after the relay trips, then the relay outputs a breaker failure trip with output contact OUT103 and another event report is generated:

$$ER = \dots + /OUT103 = \text{logical 1 (for one processing interval)}$$

As stated earlier, the 51G pickup indicator is still asserted at the time of breaker failure trip, but the rising edge operators allow each individual action to generate a separate event report.

Falling edge operators \ are also used to generate event reports. See Figure G.2 in *Appendix G: Setting SELOGIC Control Equations* for more information on falling edge operators.

TRI (Trigger Event Report) and PUL (Pulse Output Contact) Commands

The sole function of the TRI serial port command is to generate standard event reports, primarily for testing purposes.

The PUL command asserts the output contacts for testing purposes or for remote control. If output contact OUT101 through OUT107 (Models 0351x0, 0351x1, and 0351xY) asserts via the PUL command, the relay triggers a standard event report. The PUL command is available at the serial port and the relay front-panel CNTRL pushbutton.

See *Section 10: Serial Port Communications and Commands* and *Section 11: Front-Panel Interface* (Figure 11.3) for more information on the TRI (Trigger Event Report) and PUL (Pulse Output Contact) commands.

Standard Event Report Summary

Each time the relay generates a standard event report, it also generates a corresponding event summary (see Figure 12.1). Event summaries contain the following information:

- Relay and terminal identifiers (settings RID and TID)
- Date and time when the event was triggered
- Event type
- Fault location
- Recloser shot count at the trigger time
- System frequency at the front of the event report
- Front-panel fault type targets at the time of trip
- Phase (IA, IB, IC), neutral ground (IN), calculated residual ground ($I_G = 3I_0$), and negative-sequence ($3I_2$) currents

The relay includes the event summary in the standard event report. The identifiers, date, and time information is at the top of the standard event report, and the other information follows at the end. See Figure 12.2.

The example event summary in Figure 12.1 corresponds to the full-length standard 15-cycle event report in Figure 12.2. (**Note:** Figure 12.2 is on multiple pages.)

```
-----  
FEEDER 1                               Date: 02/11/97   Time: 09:52:14.881  
STATION A  
  
Event: AG T Location: 2.41 Shot: 0 Frequency: 60.00  
Targets: INST 50  
Currents (A Pri), ABCNGQ: 2749 210 209 0 2690 2688  
-----
```

Figure 12.1: Example Event Summary

The relay sends event summaries to all serial ports with setting AUTO = Y each time an event triggers.

The latest event summaries are stored in nonvolatile memory and are accessed by the HIS (Event Summaries/History) command.

Event Type

The “Event:” field shows the event type. The possible event types and their descriptions are shown in the table below. Note the correspondence to the preceding event report triggering conditions (see *Standard Event Report Triggering* in this section).

Table 12.1: Event Types

Event Type	Description
AG, BG, CG	Single phase-to-ground faults. Appends T if TRIP asserted.
ABC	Three-phase faults. Appends T if TRIP asserted.
AB, BC, CA	Phase-to-phase faults. Appends T if TRIP asserted.
ABG, BCG, CAG	Two phase-to-ground faults. Appends T if TRIP asserted.
TRIP	Assertion of Relay Word bit TRIP (fault locator could not operate successfully to determine the phase involvement, so just TRIP is displayed).
ER	SELOGIC control equation setting ER. Phase involvement is indeterminate.
TRIG	Execution of TRIGGER command.
PULSE	Execution of PULSE command.

The event type designations AG through CAG in Table 12.1 are only entered in the “Event:” field if the fault locator operates successfully. If the fault locator does not operate successfully, just TRIP or ER is displayed.

Fault Location

The relay reports the fault location if the EFLOC setting = Y and the fault locator operates successfully after an event report is generated. If the fault locator does not operate successfully, \$\$\$\$\$\$ is listed in the field. If EFLOC = N, the field is blank. Fault location is based upon the line impedance settings Z1MAG, Z1ANG, Z0MAG, and Z0ANG and corresponding line length setting LL. See the SET command in Table 9.1 and corresponding Settings Sheet 1 of 27 in *Section 9: Setting the Relay* for information on the line parameter settings.

Note: The fault locator will not operate properly unless three-phase voltages are connected. The fault locator is most accurate when the fault currents last longer than two cycles.

Targets

The relay reports the targets at the rising edge of TRIP. The targets include: INST, COMM, S0TF, 50, 51, and 81. If there is no rising edge of TRIP in the report, the Targets field is blank. See *Front-Panel Target LEDs* in *Section 5: Trip and Target Logic*.

Currents

The “Currents (A pri), ABCNGQ:” field shows the currents present in the event report row containing the maximum phase current. The listed currents are:

- Phase (A = channel IA, B = channel IB, C = channel IC)
- Neutral ground (N = channel IN)
- Calculated residual ($I_G = 3I_0$; calculated from channels IA, IB, and IC)
- Negative-sequence ($Q = 3I_2$; calculated from channels IA, IB, and IC)

Retrieving Full-Length Standard Event Reports

The latest event reports are stored in nonvolatile memory. Each event report includes four sections:

- Current, voltage, station battery, frequency, contact outputs, optoisolated inputs
- Protection and control elements
- Event summary
- Group, SELOGIC control equations, and global settings

Use the EVE command to retrieve the reports. There are several options to customize the report format. The general command format is:

```
EVE [n Sx Ly L R A D C M]
```

where:

- | | |
|----|--|
| n | Event number (1—number of events stored). Defaults to 1 if not listed, where 1 is the most recent event. |
| Sx | Display x samples per cycle (4 or 16); defaults to 4 if not listed. |
| Ly | Display y cycles of data (1—LER). Defaults to LER value if not listed. Unfiltered reports (R parameter) display an extra cycle of data. |
| L | Display 16 samples per cycle; same as the S16 parameter. |
| R | Specifies the unfiltered (raw) event report. Defaults to 16 samples per cycle unless overridden with the Sx parameter. |
| A | Specifies that only the analog section of the event is displayed (current, voltage, station battery, frequency, output contacts, optoisolated inputs). |
| D | Specifies that only the digital section (Protection and Control Elements) of the event is displayed. |
| C | Display the report in Compressed ASCII format. |
| M | Specifies only the Communication element section of the event is displayed. |

Below are example EVE commands.

Serial Port Command

<u>Command</u>	<u>Description</u>
EVE	Display the most recent event report at 1/4-cycle resolution.
EVE 2	Display the second event report at 1/4-cycle resolution.
EVE S16 L10	Display 10 cycles of the most recent report at 1/16-cycle resolution.
EVE C 2	Display the second report in Compressed ASCII format at 1/4-cycle resolution.
EVE L	Display most recent report at 1/16-cycle resolution.
EVE R	Display most recent report at 1/16-cycle resolution; analog and digital data are unfiltered (raw).

EVE 2 D L10	Display 10 cycles of the protection and control elements section of the second event report at 1/4-cycle resolution.
EVE 2 A R S4	Display the unfiltered analog section of the second event report at 1/4-cycle resolution.

If an event report is requested that does not exist, the relay responds:

“Invalid Event”

Compressed ASCII Event Reports

The SEL-351 Relay provides compressed ASCII event reports to facilitate event report storage and display. The SEL-2020 Communications Processor and the SEL-5601 Analytic Assistant software take advantage of the compressed ASCII format. Use the EVE C command or CEVENT command to display compressed ASCII event reports. See the CEVENT command discussion in *Appendix E: Compressed ASCII Commands* for further information.

Filtered and Unfiltered Event Reports

The SEL-351 Relay samples the basic power system measurands (ac voltage, ac current, station battery, and optoisolated inputs) 16 times per power system cycle. The relay filters the measurands to remove transient signals. The relay operates on the filtered values and reports them in the event report.

To view the raw inputs to the relay, select the unfiltered event report (e.g., EVE R). Use the unfiltered event reports to observe:

- Power system harmonics on channels IA, IB, IC, IN, VA, VB, VC, VAB, VBC, VCA, VS
- Decaying dc offset during fault conditions on IA, IB, IC
- Optoisolated input contact bounce on channels IN101 through IN106 (Models 0351x0 and 0351x1)
- Transients on the station dc battery channel Vdc (power input terminals Z25 and Z26)

The filters for ac current and voltage and station battery are fixed. You can adjust the optoisolated input debounce via debounce settings (see Figures 7.1 through 7.3 in *Section 7: Inputs, Outputs, Timers, and Other Control Logic*).

Raw event reports display one extra cycle of data at the beginning of the report.

Clearing Standard Event Report Buffer

The HIS C command clears the event summaries and corresponding standard event reports from nonvolatile memory. See *Section 10: Serial Port Communications and Commands* for more information on the HIS (Event Summaries/History) command.

Standard Event Report Column Definitions

Refer to the example event report in Figure 12.2 to view event report columns (**Note:** Figure 12.2 is on multiple pages). This example event report displays rows of information each 1/4 cycle and was retrieved with the EVE command.

The columns contain ac current, ac voltage, station dc battery voltage, frequency, output, input, and protection and control element information.

Current, Voltage, and Frequency Columns

Table 12.2 summarizes the event report current, voltage, and frequency columns.

Table 12.2: Standard Event Report Current, Voltage, and Frequency Columns

Column Heading	Definition
IA	Current measured by channel IA (primary A)
IB	Current measured by channel IB (primary A)
IC	Current measured by channel IC (primary A)
IN	Current measured by channel IN (primary A)
IG	Calculated residual current $IG = 3I_0 = IA + IB + IC$ (primary A)
VA	Voltage measured by channel VA (primary kV, wye-connected)
VB	Voltage measured by channel VB (primary kV, wye-connected)
VC	Voltage measured by channel VC (primary kV, wye-connected)
VS	Voltage measured by channel VS (primary kV)
Vdc	Voltage measured at power input terminals Z15 and Z16 (Vdc)
Freq	Frequency of channel VA (Hz)

Note that the ac values change from plus to minus (-) values in Figure 12.2, indicating the sinusoidal nature of the waveforms.

Other figures help in understanding the information available in the event report current columns:

Figure 12.3: shows how event report current column data relates to the actual sampled current waveform and RMS current values.

Figure 12.4: shows how event report current column data can be converted to phasor RMS current values.

Output, Input, and Protection, and Control Columns

Table 12.3 summarizes the event report output, input, protection and control columns. See Table 9.4 in *Section 9: Setting the Relay* for more information on Relay Word bits shown in Table 12.3.

Note: The event report does not show the output contacts or optoisolated inputs for the extra I/O board on models 0351x1 and 0351xY. See Table 1.1 (and figures referenced therein) for more information on all the available models.

Table 12.3: Output, Input, and Protection, and Control Element Event Report Columns

Column Heading	Corresponding Elements (Relay Word Bits)	Symbol	Definition
All columns		.	Element/input/output not picked up or not asserted, unless otherwise stated.
**Out 12	OUT101, OUT102	1 2 b	Output contact OUT101 asserted. Output contact OUT102 asserted. Both OUT101 and OUT102 asserted.
**Out 34	OUT103, OUT104	3 4 b	Output contact OUT103 asserted. Output contact OUT104 asserted. Both OUT103 and OUT104 asserted.
**Out 56	OUT105, OUT106	5 6 b	Output contact OUT105 asserted. Output contact OUT106 asserted. Both OUT105 and OUT106 asserted.
**Out 7A	OUT107, ALARM	7 A b	Output contact OUT107 asserted. Output contact ALARM asserted. Both OUT107 and ALARM asserted.
In 12	IN101, IN102	1 2 b	Optoisolated input IN101 asserted. Optoisolated input IN102 asserted. Both IN101 and IN102 asserted.
In 34	IN103, IN104	3 4 b	Optoisolated input IN103 asserted. Optoisolated input IN102 asserted. Both IN103 and IN104 asserted.
In 56	IN105, IN106	5 6	Optoisolated input IN105 asserted. Optoisolated input IN106 asserted. Both IN105 and IN106 asserted.
51 A 51 B 51 C 51 P 51 N 51 G 51 Q	51A, 51AT, 51AR 51B, 51BT, 51BR 51C, 51CT, 51CR 51P, 51PT, 51PR 51N, 51N, 51NR 51G, 51GT, 51GR 51Q, 51QT, 51QR	. p T r 1	Time-overcurrent element reset (51_R). Time-overcurrent element picked up and timing (51_). Time-overcurrent element timed out (51_T). Time-overcurrent element timing to reset. Time-overcurrent element timing to reset after having timed out (when element reset is set for 1 cycle, not electromechanical reset).

Column Heading	Corresponding Elements (Relay Word Bits)	Symbol	Definition
50 P	50A, 50B, 50C	A B C a b c 3	Single-phase instantaneous overcurrent element 50A picked up. Single-phase instantaneous overcurrent element 50B picked up. Single-phase instantaneous overcurrent element 50C picked up. Both 50A and 50B picked up. Both 50B and 50C picked up. Both 50C and 50A picked up. 50A, 50B, and 50C picked up.
50 PP	50AB1, 50AB2, 50AB3, 50AB4, 50BC1, 50BC2, 50BC3, 50BC4, 50CA1, 50CA2, 50CA3, 50CA4	A B C a b c 3	Phase-to-phase instantaneous overcurrent element 50AB1, 50AB2, 50AB3, or 50AB4 picked up. Phase-to-phase instantaneous overcurrent element 50BC1, 50BC2, 50BC3, or 50BC4 picked up. Phase-to-phase instantaneous overcurrent element 50CA1, 50CA2, 50CA3, or 50CA4 picked up. 50AB_ and 50CA_ picked up. 50AB_ and 50BC_ picked up. 50BC_ and 50CA_ picked up. 50AB_, 50BC_, and 50CA_ picked up.
32 PQ	F32P R32P F32Q R32Q	P p Q q	Forward phase directional element F32P picked up. Reverse phase directional element R32P picked up. Forward negative-sequence directional element F32Q picked up. Reverse negative-sequence directional element R32Q picked up.
32 NG	F32QG R32QG F32V R32V F32I R32I	Q q V v I i	Forward negative-sequence directional element F32QG picked up. Reverse negative-sequence R32QG picked up. Forward zero-sequence voltage-polarized element F32V picked up. Reverse zero-sequence voltage-polarized R32V picked up. Forward channel IN current-polarized directional element F32I picked up. Reverse channel IN current-polarized directional element R32I picked up.

Column Heading	Corresponding Elements (Relay Word Bits)	Symbol	Definition
67 P 67 N 67 G 67 Q	67P1–67P4 67N1–67N4 67G1–67G4 67Q1–67Q4	4 3 2 1	Level 4 instantaneous element 67_4 picked up; levels 1, 2, and 3 not picked up. Level 3 instantaneous element 67_3 picked up; levels 1 and 2 not picked up. Level 2 instantaneous element 67_2 picked up; Level 1 not picked up. Level 1 instantaneous element 67_1 picked up.
DM PQ	PDEM, QDEM	P Q b	Phase demand ammeter element PDEM picked up. Negative-sequence demand ammeter element QDEM picked up. Both PDEM and QDEM picked up.
DM NG	NDEM, GDEM	N G b	Neutral ground demand ammeter element NDEM picked up. Residual ground demand ammeter element GDEM picked up. Both NDEM and GDEM picked up.
27 P	27A1, 27A2, 27B1, 27B2, 27C1, 27C2	A B C a b c 3	A-phase instantaneous undervoltage element 27A1 or 27A2 picked up. B-phase instantaneous undervoltage element 27B1 or 27B2 picked up. C-phase instantaneous undervoltage element 27C1 or 27C2 picked up. 27A_ and 27B_ elements picked up. 27B_ and 27C_ elements picked up. 27C_ and 27A_ elements picked up. 27A_, 27B_ and 27C_ elements picked up.

Column Heading	Corresponding Elements (Relay Word Bits)	Symbol	Definition
27 PP	27AB, 27BC, 27CA	A B C a b c 3	AB phase-to-phase instantaneous undervoltage element 27AB picked up. BC phase-to-phase instantaneous undervoltage element 27BC picked up. CA phase-to-phase instantaneous undervoltage element 27CA picked up. 27AB and 27CA elements picked up. 27AB and 27BC elements picked up. 27BC and 27CA elements picked up. 27AB, 27BC and 27CA elements picked up.
27 S	27S	*	Channel VS instantaneous undervoltage element 27S picked up.
59 P	59A1, 59A2, 59B1, 59B2, 59C1, 59C2	A B C a b c 3	A-phase instantaneous overvoltage element 59A1 or 59A2 picked up. B-phase instantaneous overvoltage element 59B1 or 59B2 picked up. C-phase instantaneous overvoltage element 59C1 or 59C2 picked up. 59A_ and 59B_ elements picked up. 59B_ and 59C_ elements picked up. 59C_ and 59A_ elements picked up. 59A_, 59B_ and 59C_ elements picked up.
59 PP	59AB, 59BC, 59CA	A B C a b c 3	AB phase-to-phase instantaneous overvoltage element 59AB picked up. BC phase-to-phase instantaneous overvoltage element 59BC picked up. CA phase-to-phase instantaneous overvoltage element 59CA picked up. 59AB and 59CA elements picked up. 59AB and 59BC elements picked up. 59BC and 59CA elements picked up. 59AB, 59BC and 59CA elements picked up.
59 V1Q	59V1, 59Q	1 Q b	Positive-sequence instantaneous overvoltage element 59V1 picked up. Negative-sequence instantaneous overvoltage element 59Q picked up. Both 59V1 and 59Q picked up.

Column Heading	Corresponding Elements (Relay Word Bits)	Symbol	Definition
59 N	59N1, 59N2	1	First ground instantaneous overvoltage element 59N1 picked up.
		2	Second ground instantaneous overvoltage element 59N2 picked up.
		b	Both 59N1 and 59N2 picked up.
59 S	59S1, 59S2	1	First channel VS instantaneous overvoltage element 59S1 picked up.
		2	Second channel VS instantaneous overvoltage element 59S2 picked up.
		b	Both 59S1 and 59S2 picked up.
59 V	59VP, 59VS	P	Phase voltage window element 59VP picked up (used in synchronism check).
		S	Channel VS voltage window element 59VS picked up (used in synchronism check).
		b	Both 59VP and 59VS picked up.
25 SF	SF	*	Slip frequency element SF picked up (used in synchronism check).
25 A	25A1, 25A2	1	First synchronism check element 25A1 element picked up.
		2	Second synchronism check element 25A2 element picked up.
		b	Both 25A1 and 25A2 picked up.
81 27B	27B81	*	Frequency logic instantaneous undervoltage element 27B81 picked up.
81 12	81D1, 81D2	1	Frequency element 81D1 picked up.
		2	Frequency element 81D2 picked up.
		b	Both 81D1 and 81D2 picked up.
81 34	81D3, 81D4	3	Frequency element 81D3 picked up.
		4	Frequency element 81D4 picked up.
		b	Both 81D3 and 81D4 picked up.
81 56	81D5, 81D6	5	Frequency element 81D5 picked up.
		6	Frequency element 81D6 picked up.
		b	Both 81D5 and 81D6 picked up.

Column Heading	Corresponding Elements (Relay Word Bits)	Symbol	Definition
79	RCSF, CF, 79RS, 79CY, 79LO	. S F R C L	Reclosing relay nonexistent. Reclose supervision failure condition (RCSF asserts for only 1/4 cycle). Close failure condition (CF asserts for only 1/4 cycle). Reclosing relay in Reset State (79RS). Reclosing relay in Reclose Cycle State (79CY). Reclosing relay in Lockout State (79LO).
Time	OPTMN, RSTMN	o r	Recloser open interval timer is timing. Recloser reset interval timer is timing.
Shot	SH0, SH1, SH2 SH3, SH4	. 0 1 2 3 4	Reclosing relay nonexistent. shot = 0 (SH0). shot = 1 (SH1). shot = 2 (SH2). shot = 3 (SH3). shot = 4 (SH4).
Zld	ZLIN, ZLOUT	i o	Load encroachment "load in" element ZLIN picked up. Load encroachment "load out" element ZLOUT picked up.
LOP	LOP	*	Loss-of-potential element LOP picked up.
Vdc	DCHI, DCLO	H L b	Station battery instantaneous overvoltage element DCHI picked up. Station battery instantaneous undervoltage element DCLO picked up. Both DCHI and DCLO asserted.
Lcl 12	LB1, LB2	1 2 b	Local bit LB1 asserted. Local bit LB2 asserted. Both LB1 and LB2 asserted.
Lcl 34	LB3, LB4	3 4 b	Local bit LB3 asserted. Local bit LB4 asserted. Both LB3 and LB4 asserted.
Lcl 56	LB5, LB6	5 6 b	Local bit LB5 asserted. Local bit LB6 asserted. Both LB5 and LB6 asserted.
Lcl 78	LB7, LB8	7 8 b	Local bit LB7 asserted. Local bit LB8 asserted. Both LB7 and LB8 asserted.

Column Heading	Corresponding Elements (Relay Word Bits)	Symbol	Definition
Rem 12	RB1, RB2	1	Remote bit RB1 asserted.
		2	Remote bit RB2 asserted.
		b	Both RB1 and RB2 asserted.
Rem 34	RB3, RB4	3	Remote bit RB3 asserted.
		4	Remote bit RB4 asserted.
		b	Both RB3 and RB4 asserted.
Rem 56	RB5, RB6	5	Remote bit RB5 asserted.
		6	Remote bit RB6 asserted.
		b	Both RB5 and RB6 asserted.
Rem 78	RB7, RB8	7	Remote bit RB7 asserted.
		8	Remote bit RB8 asserted.
		b	Both RB7 and RB8 asserted.
Rem OC	OC, CC	o	OPE (Open) command executed.
		c	CLO (Close) command executed.
Ltch 12	LT1, LT2	1	Latch bit LT1 asserted.
		2	Latch bit LT2 asserted.
		b	Both LT1 and LT2 asserted.
Ltch 34	LT3, LT4	3	Latch bit LT3 asserted.
		4	Latch bit LT4 asserted.
		b	Both LT3 and LT4 asserted.
Ltch 56	LT5, LT6	5	Latch bit LT5 asserted.
		6	Latch bit LT6 asserted.
		b	Both LT5 and LT6 asserted.
Ltch 78	LT7, LT8	7	Latch bit LT7 asserted.
		8	Latch bit LT8 asserted.
		b	Both LT7 and LT8 asserted.

Column Heading	Corresponding Elements (Relay Word Bits)	Symbol	Definition
SELOGIC Var 1	SV1, SV1T	P	SELOGIC control equation variable timer input SV_ asserted; timer timing on pickup time; timer output SV_T not asserted.
SELOGIC Var 2	SV2, SV2T		
SELOGIC Var 3	SV3, SV3T		
SELOGIC Var 4	SV4, SV4T		
SELOGIC Var 5	SV5, SV5T	T	
SELOGIC Var 6	SV6, SV6T		
SELOGIC Var 7	SV7, SV7T		
SELOGIC Var 8	SV8, SV8T		
SELOGIC Var 9	SV9, SV9T		
SELOGIC Var 10	SV10, SV10T	d	
SELOGIC Var 11	SV11, SV11T		
SELOGIC Var 12	SV12, SV12T		
SELOGIC Var 13	SV13, SV13T		
SELOGIC Var 14	SV14, SV14T		
SELOGIC Var 15	SV15, SV15T		
SELOGIC Var 16	SV16, SV16T		
3PO	3PO	*	Three pole open condition 3PO asserted.
SOTF	SOTF	*	Switch-onto-fault condition SOTF asserted.
PT	PT	*	Permissive trip signal to POTT logic PT asserted.
PTRX	PTRX1, PTRX2	1	Permissive trip 1 signal from DCUB logic PTRX1 asserted.
		2	Permissive trip 2 signal from DCUB logic PTRX2 asserted.
		b	Both PTRX1 and PTRX2 asserted
Z3RB	Z3RB	*	Zone (level) 3 reverse block Z3RB asserted.
KEY	KEY	*	Key permissive trip signal start KEY asserted.
EKEY	EKEY	*	Echo key EKEY asserted.
ECTT	ECTT	*	Echo conversion to trip condition ECTT asserted.
WFC	WFC	*	Weak infeed condition WFC asserted.
UBB	UBB1, UBB2	1	Unblocking block 1 from DCUB logic UBB1 asserted.
		2	Unblocking block 2 from DCUB logic UBB2 asserted.
		b	Both UBB1 and UBB2 asserted.

Column Heading	Corresponding Elements (Relay Word Bits)	Symbol	Definition
Z3XT	Z3XT	*	Logic output from zone (level) 3 extension timer Z3XT asserted.
DSTR	DSTRT	*	Directional carrier start DSTRT asserted.
NSTR	NSTRT	*	Nondirectional carrier start NSTRT asserted.
STOP	STOP	*	Carrier stop STOP asserted.
BTX	BTX	*	Block trip input extension BTX asserted.
TMB A 12	TMB1A, TMB2A	1	MIRRORED BITS™ channel A transmit bit 1 TMB1A asserted.
		2	MIRRORED BITS channel A transmit bit 2 TMB2A asserted.
		b	Both TMB1A and TMB2A asserted.
TMB A 34	TMB3A, TMB4A	3	MIRRORED BITS channel A transmit bit 3 TMB3A asserted.
		4	MIRRORED BITS channel A transmit bit 4 TMB4A asserted.
		b	Both TMB3A and TMB4A asserted.
TMB A 56	TMB5A, TMB6A	5	MIRRORED BITS channel A transmit bit 5 TMB5A asserted.
		6	MIRRORED BITS channel A transmit bit 6 TMB6A asserted.
		b	Both TMB5A and TMB6A asserted.
TMB A 78	TMB7A, TMB8A	7	MIRRORED BITS channel A transmit bit 7 TMB7A asserted.
		8	MIRRORED BITS channel A transmit bit 8 TMB8A asserted.
		b	Both TMB7A and TMB8A asserted.
RMB A 12	RMB1A, RMB2A	1	MIRRORED BITS channel A receive bit 1 RMB1A asserted.
		2	MIRRORED BITS channel A receive bit 2 RMB2A asserted.
		b	Both RMB1A and RMB2A asserted.
RMB A 34	RMB3A, RMB4A	3	MIRRORED BITS channel A receive bit 3 RMB3A asserted.
		4	MIRRORED BITS channel A receive bit 4 RMB4A asserted.
		b	Both RMB3A and RMB4A asserted.

Column Heading	Corresponding Elements (Relay Word Bits)	Symbol	Definition
RMB A 56	RMB5A, RMB6A	5	MIRRORED BITS channel A receive bit 5 RMB5A asserted.
		6	MIRRORED BITS channel A receive bit 6 RMB6A asserted.
		b	Both RMB5A and RMB6A asserted.
RMB A 78	RMB7A, RMB8A	7	MIRRORED BITS channel A receive bit 7 RMB7A asserted.
		8	MIRRORED BITS channel A receive bit 8 RMB8A asserted.
		b	Both RMB7A and RMB8A asserted.
TMB B 12	TMB1B, TMB2B	1	MIRRORED BITS channel B transmit bit 1 TMB1B asserted.
		2	MIRRORED BITS channel B transmit bit 2 bit TMB2B asserted.
		b	Both TMB1B and TMB2B asserted.
TMB B 34	TMB3B, TMB4B	3	MIRRORED BITS channel B transmit bit 3 TMB3B asserted.
		4	MIRRORED BITS channel B transmit bit 4 TMB4B asserted.
		b	Both TMB3B and TMB4B asserted.
TMB B 56	TMB5B, TMB6B	5	MIRRORED BITS channel B transmit bit 5 TMB5B asserted.
		6	MIRRORED BITS channel B transmit bit 6 TMB6B asserted.
		b	Both TMB5B and TMB6B asserted.
TMB B 78	TMB7B, TMB8B	7	MIRRORED BITS channel B transmit bit 7 TMB7B asserted.
		8	MIRRORED BITS channel B transmit bit 8 TMB8B asserted.
		b	Both TMB7B and TMB8B asserted.
RMB B 12	RMB1B, RMB2B	1	MIRRORED BITS channel B receive bit 1 RMB1B asserted.
		2	MIRRORED BITS channel B receive bit 2 RMB2B asserted.
		b	Both RMB1B and RMB2B asserted.
RMB B 34	RMB3B, RMB4B	3	MIRRORED BITS channel B receive bit 3 RMB3B asserted.
		4	MIRRORED BITS channel B receive bit t 4 RMB4B asserted.
		b	Both RMB3B and RMB4B asserted.

Column Heading	Corresponding Elements (Relay Word Bits)	Symbol	Definition
RMB B 56	RMB5B, RMB6B	5	MIRRORED BITS channel B receive bit 5 RMB5B asserted.
		6	MIRRORED BITS channel B receive bit 6 RMB6B asserted.
		b	Both RMB5B and RMB6B asserted.
RMB B 78	RMB7B, RMB8B	7	MIRRORED BITS channel B receive bit 7 RMB7B asserted.
		8	MIRRORED BITS channel B receive bit 8 RMB8B asserted.
		b	Both RMB7B and RMB8B asserted.
ROK	ROKA, ROKB	A	MIRRORED BITS channel A receive ok ROKA asserted.
		B	MIRRORED BITS channel B receive ok ROKB asserted.
		b	Both ROKA and ROKB asserted.
RBAD	RBADA, RBADB	A	MIRRORED BITS channel A extended outage RBADA asserted.
		B	MIRRORED BITS channel B extended outage RBADB asserted.
		b	Both RBADA and RBADB asserted.
CBAD	CBADA, CBADB	A	MIRRORED BITS channel A unavailability CBADA asserted.
		B	MIRRORED BITS channel B unavailability CBADB asserted.
		b	Both CBADA and CBADB asserted.
LBOK	LBOKA, LBOKB	A	MIRRORED BITS channel A loop back ok LBOKA asserted.
		B	MIRRORED BITS channel A loop back ok LBOKB asserted.
		b	Both LBOKA and LBOKB asserted.
*PWR A 12	PWRA1, PWRA2	1	Level 1 A-phase power element PWR1A picked up.
		2	Level 2 A-phase power element PWR2A picked up.
		b	Both PWR1A and PWR2A picked up.
*PWR A 34	PWRA3, PWRA4	3	Level 3 A-phase power element PWR3A picked up.
		4	Level 4 A-phase power element PWR4A picked up.
		b	Both PWR3A and PWR4A picked up.

Column Heading	Corresponding Elements (Relay Word Bits)	Symbol	Definition
‡PWR B 12	PWRB1, PWRB2	1	Level 1 B-phase power element PWR1B picked up.
		2	Level 2 B-phase power element PWR2B picked up.
		b	Both PWR1B and PWR2B picked up.
‡PWR B 34	PWRB3, PWRB4	3	Level 3 B-phase power element PWR3B picked up.
		4	Level 4 B-phase power element PWR4B picked up.
		b	Both PWR3B and PWR4B picked up.
‡PWR C 12	PWRC1, PWRC2	1	Level 1 C-phase power element PWR1C picked up.
		2	Level 2 C-phase power element PWR2C picked up.
		b	Both PWR1C and PWR2C picked up.
‡PWR C 34	PWRC3, PWRC4	3	Level 3 C-phase power element PWR3C picked up.
		4	Level 4 C-phase power element PWR4C picked up.
		b	Both PWR3C and PWR4C picked up.

** Output contacts can be A or B type contacts (see Table 2.2 and Figures 7.27 through 7.28).

‡ Available in Firmware Version 7.

SEQUENTIAL EVENTS RECORDER (SER) REPORT

See Figure 12.5 for an example SER report.

SER Triggering

The relay triggers (generates) an entry in the SER report for a change of state of any one of the elements listed in the SER1, SER2, and SER3 trigger settings. The factory default settings are:

```
SER1 = 51P 51G 50P1
SER2 = LB3 LB4 IN101 IN102 OUT101 OUT102 OUT103
SER3 = CF 79CY 79LO
```

The elements are Relay Word bits referenced in Table 9.3. The relay monitors each element in the SER lists every 1/4 cycle. If an element changes state, the relay time-tags the changes in the SER. For example, setting SER1 contains:

```
time-overcurrent element pickups (51P and 51G)
instantaneous overcurrent element (50P1)
```

Thus, any time one of these overcurrent elements picks up or drops out, the relay time-tags the change in the SER.

The other two SER factory settings (SER2 and SER3) trigger rows in the SER event report for such things as optoisolated input (IN101), output contact (OUT101, OUT102, or OUT103), and lockout state (79LO).

The relay adds a message to the SER to indicate power up or settings change (to active setting group) conditions:

Relay newly powered up or settings changed

Each entry in the SER includes SER row number, date, time, element name, and element state.

Making SER Trigger Settings

Enter up to 24 element names in each of the SER settings via the SET R command. See Table 9.3 for references to valid relay element (Relay Word bit) names. See the SET R command in Table 9.1 and corresponding Settings Sheet 22 of 27 at the end of **Section 9: Setting the Relay**. Use commas to delimit the elements. For example, if you enter setting SER1 as:

SER1 = 51P,51G,51PT,,51GT , 50P1, , 50P2

The relay displays the setting as:

SER1 = 51P,51G,51PT,51GT,50P1,50P2

The relay can monitor up to 72 elements in the SER (24 in each of SER1, SER2, and SER3).

Make Sequential Events Recorder (SER) Settings With Care

The relay triggers a row in the Sequential Events Recorder (SER) event report for any change of state in any one of the elements listed in the SER1, SER2, or SER3 trigger settings. Nonvolatile memory is used to store the latest 512 rows of the SER event report so they can be retained during power loss. The nonvolatile memory is rated for a finite number of "writes." Exceeding the limit can result in an EEPROM self-test failure. An average of one state change every three minutes can be made for a 25-year relay service life.

Retrieving SER Reports

The relay saves the latest 512 rows of the SER in nonvolatile memory. Row 1 is the most recently triggered row, and row 512 is the oldest. View the SER report by date or SER row number as outlined in the examples below.

Example SER Serial Port

<u>Commands</u>	<u>Format</u>
SER	If SER is entered with no numbers following it, all available rows are displayed (up to row number 512). They display with the oldest row at the beginning (top) of the report and the latest row (row 1) at the end (bottom) of the report. Chronological progression through the report is down the page and in descending row number.
SER 17	If SER is entered with a single number following it (17 in this example), the first 17 rows are displayed, if they exist. They display with the oldest

row (row 17) at the beginning (top) of the report and the latest row (row 1) at the end (bottom) of the report. Chronological progression through the report is down the page and in descending row number.

SER 10 33 If SER is entered with two numbers following it (10 and 33 in this example; $10 < 33$), all the rows between (and including) rows 10 and 33 are displayed, if they exist. They display with the oldest row (row 33) at the beginning (top) of the report and the latest row (row 10) at the end (bottom) of the report. Chronological progression through the report is down the page and in descending row number.

SER 47 22 If SER is entered with two numbers following it (47 and 22 in this example; $47 > 22$), all the rows between (and including) rows 47 and 22 are displayed, if they exist. They display with the newest row (row 22) at the beginning (top) of the report and the oldest row (row 47) at the end (bottom) of the report. Reverse chronological progression through the report is down the page and in ascending row number.

SER 3/30/97 If SER is entered with one date following it (date 3/30/97 in this example), all the rows on that date are displayed, if they exist. They display with the oldest row at the beginning (top) of the report and the latest row at the end (bottom) of the report, for the given date. Chronological progression through the report is down the page and in descending row number.

SER 2/17/97 3/23/97 If SER is entered with two dates following it (date 2/17/97 chronologically precedes date 3/23/97 in this example), all the rows between (and including) dates 2/17/97 and 3/23/97 are displayed, if they exist. They display with the oldest row (date 2/17/97) at the beginning (top) of the report and the latest row (date 3/23/97) at the end (bottom) of the report. Chronological progression through the report is down the page and in descending row number.

SER 3/16/97 1/5/97 If SER is entered with two dates following it (date 3/16/97 chronologically follows date 1/5/97 in this example), all the rows between (and including) dates 1/5/97 and 3/16/97 are displayed, if they exist. They display with the latest row (date 3/16/97) at the beginning (top) of the report and the oldest row (date 1/5/97) at the end (bottom) of the report. Reverse chronological progression through the report is down the page and in ascending row number.

The date entries in the above example SER commands are dependent on the Date Format setting DATE_F. If setting DATE_F = MDY, then the dates are entered as in the above examples (Month/Day/Year). If setting DATE_F = YMD, then the dates are entered Year/Month/Day.

If the requested SER event report rows do not exist, the relay responds:

No SER Data

Clearing SER Report

Clear the SER report from nonvolatile memory with the SER C command as shown in the following example:

```

=>SER C <ENTER>
Clear the SER
Are you sure (Y/N) ? Y <ENTER>
Clearing Complete
  
```

EXAMPLE STANDARD 15-CYCLE EVENT REPORT

The following example standard 15-cycle event report in Figure 12.2 (from a Model 03517 Relay) also corresponds to the example sequential events recorder (SER) report in Figure 12.5. The circled numbers in Figure 12.2 correspond to the SER row numbers in Figure 12.5. The row explanations follow Figure 12.5.

In Figure 12.2, the arrow (>) in the column following the **Freq** column identifies the “trigger” row. This is the row that corresponds to the Date and Time values at the top of the event report.

The asterisk (*) in the column following the **Freq** column identifies the row with the maximum phase current. The maximum phase current is calculated from the row identified with the asterisk and the row one quarter-cycle previous (see Figure 12.3 and Figure 12.4). These currents are listed at the end of the event report in the event summary. If the “trigger” row (>) and the maximum phase current row (*) are the same row, the * symbol takes precedence.

FEEDER 1		Date: 04/12/99	Time: 09:28:31.721	← see Figure 12.1										
STATION A		← firmware identifier												
FID=SEL-351-14-R300-V0-D990426		← firmware checksum identifier												
CID=2516		← firmware checksum identifier												
Currents (Amps Pri)					Voltages (kV Pri)					Out	In			
IA	IB	IC	IN	IG	VA	VB	VC	VS	Vdc	Freq	246A	246B		
[1]	241	26	-268	-1	-1	9.6	1.5	-11.1	0.0	24	60.01	b..] one cycle of data
	-169	293	-124	0	0	-7.2	11.9	-4.7	0.0	24	60.01	b..	
	-242	-26	267	-1	-1	-9.6	-1.5	11.0	-0.0	24	60.01	b..	
	168	-294	124	-1	-2	7.2	-11.9	4.7	0.0	24	60.01	b..	
[Two cycles of data not shown in this example]														
[4]	243	22	-266	-1	-1	9.7	1.3	-11.0	-0.0	24	60.01	b..	
	-166	294	-128	0	0	-7.1	11.9	-4.8	0.0	24	60.01	b..	
	-542	-32	255	-1	-319	-8.7	-1.9	10.8	0.0	24	60.01	b..	
	-485	-271	107	0	-649	6.5	-11.7	4.8	-0.0	24	60.01>	b..	
[5]	1586	37	-220	-1	1404	6.9	3.1	-10.2	-0.0	24	60.01	b..	7
	1295	226	-82	0	1439	-4.9	11.0	-4.9	0.0	24	59.81	1...	b..	
	-2332	-33	194	0	-2171	-6.2	-3.6	9.9	0.0	24	59.81	1...	b..	
	-1460	-208	77	-1	-1590	3.9	-10.5	5.0	0.0	24	59.70	1...	b..	
[6]	2328	32	-194	0	2166	6.2	3.6	-9.9	-0.0	24	59.70	1...	b..	
	1465	207	-79	0	1594	-3.9	10.5	-5.0	-0.0	24	59.70	1...	b..	
	-2326	-32	193	-1	-2165	-6.2	-3.6	9.9	0.0	24	59.70	1...	b..	
	-1470	-208	79	0	-1599	3.9	-10.5	5.0	0.0	24	59.89	1...	b..	

```

[7]
2323 31 -194 0 2160 6.2 3.5 -9.9 -0.0 24 59.89 1... b..
1474 207 -80 -1 1601 -3.9 10.5 -5.0 0.0 24 60.01 1... b..
-2320 -31 193 0 -2158 -6.2 -3.5 9.9 0.0 24 60.01 1... b..
-1479 -208 80 0 -1607 3.8 -10.5 5.1 0.0 24 60.01 1... b..
2317 31 -194 0 2154 6.2 3.5 -9.9 -0.0 24 60.01 1... b..
1482 207 -80 0 1609 -3.8 10.5 -5.1 -0.0 24 60.01 1... b..
-2317 -31 193 -1 -2154 -6.2 -3.5 9.9 0.0 24 60.01 1... b..
-1484 -208 80 -1 -1612 3.8 -10.5 5.1 0.0 24 60.01 1... b..
[9]
2317 30 -194 -1 2153 6.2 3.5 -9.9 -0.0 24 60.01*1... b..
1483 207 -80 0 1609 -3.8 10.5 -5.1 0.0 24 60.01 1... b..
-1965 -41 160 0 -1846 -7.2 -2.9 10.1 0.0 24 60.01 1... b..
-849 -146 39 -1 -956 4.4 -10.7 5.1 -0.0 24 60.01 1... b..
[10]
805 26 -64 -1 767 9.0 1.7 -10.6 -0.0 24 60.01 1... b..
108 41 0 0 149 -6.0 11.4 -5.1 0.0 24 60.25 1... b..
-1 0 0 -1 -1 -9.8 -1.2 10.9 0.0 24 60.25 1... 2..
0 0 -1 -1 -1 7.0 -12.0 5.0 -0.0 24 60.32 1... 2..
[11]
-1 -1 0 0 -1 9.8 1.2 -10.9 -0.0 24 60.32 1... 2..
-1 0 0 0 -1 -7.0 11.9 -4.9 0.0 24 60.32 1... 2..
0 0 -1 -1 -1 -9.7 -1.2 10.9 0.0 24 60.32 1... 2..
-1 -1 -1 -1 -2 7.0 -11.9 4.9 -0.0 24 60.08 1... 2..
[Two cycles of data not shown in this example ]
[14]
-1 0 -1 -1 -1 9.7 1.2 -11.0 0.0 24 60.01 1... 2..
0 0 0 -1 0 -7.0 11.9 -4.9 0.0 24 60.01 .... 2..
0 -1 0 -1 -1 -9.7 -1.2 10.9 -0.0 24 60.01 .... 2..
-1 -1 -1 0 -2 7.0 -11.9 4.9 0.0 24 60.01 .... 2..
[15]
-1 -1 -1 0 -2 9.8 1.2 -10.9 -0.0 24 60.01 .... 2..
0 0 0 -1 0 -7.0 11.9 -5.0 0.0 24 60.01 .... 2..
0 0 0 0 0 -9.8 -1.1 10.9 0.0 24 60.01 .... 2..
0 -1 -1 -1 -1 7.0 -11.9 5.0 0.0 24 60.01 .... 2..

```

see Figure 12.3 and Figure 12.4 for details on this example one cycle of phase A (channel IA) current

3

2

Protection and Control Elements

```

51 50 32 67 Dm 27 59 25 81 TS Lc1 Rem Ltch SELogic
V 5 2 ih ZLV Variable
P PN PN P P1 9S 7135 7mo 10d 1357135701357 1111111
ABCPNGQPP QG PNGQ QG PPSPPQNS VFA B246 9et dPc 24682468C2468 1234567890123456

```

```

[1]
..... R.0 .....
..... R.0 .....
..... R.0 .....
..... R.0 .....

```

[Two cycles of data not shown in this example]

```

[4]
..... R.0 .....
..... R.0 .....
...p... R.0 .....
...p.p... R.0 .....

```

```

[5]
...p.p... R.0 .....
...p.p.A.. 1... C.0 .....
...p.p.A.. 1... Cr0 .....
...p.p.A.. 1... Cr0 .....

```

```

[6]
...p.p.A.. 1... Cr0 .....
...p.p.A.. 1... Cr0 .....
...p.p.A.. 1... Cr0 .....
...p.p.A.. 1... Cr0 .....

```

8, 9, 10, 11

```

[7]
...p.p.A. .. 1... .. Cr0 .. p.....
...p.p.A. .. 1... .. Cr0 .. p.....
...p.p.A. .. 1... .. Cr0 .. p.....
...p.p.A. .. 1... .. Cr0 .. p.....
[8]
...p.p.A. .. 1... .. Cr0 .. p.....
...p.p.A. .. 1... .. Cr0 .. p.....
...p.p.A. .. 1... .. Cr0 .. p.....
...p.p.A. .. 1... .. Cr0 .. p.....
[9]
...p.p.A. .. 1... .. Cr0 .. p.....
...p.p.A. .. 1... .. Cr0 .. p.....
...p.p.A. .. 1... .. Cr0 .. p.....
...p.p.A. .. 1... .. Cr0 .. p.....
[10]
...p.p..... [6] Cr0 .. p.....
...p.p..... Cr0 .. p.....
...r.r..... Cr0 .. p.....
...r.r..... Cr0 .. p.....
[11]
...r.r..... [5] C.0 .. p.....
...r.r..... C.0 .. p.....
..... C.0 .. p.....
..... C.0 .. p.....

```

[Two cycles of data not shown in this example]

```

[14]
..... C.0 .. p.....
..... Co0 ..
..... Co0 ..
..... Co0 ..
[15]
..... Co0 ..
..... Co0 ..
..... Co0 ..
..... Co0 ..

```

(The Communication Elements Section is only available in Firmware Versions 6 and 7.)

Communication Elements

```

S PZ EE ZDNS TMB RMB TMB RMB RRCL PWR
30 T3KKCWU 3SSTB A A B B OBBB A B C
PT PRREETFB XTTOT 1357 1357 1357 1357 KAAO 131313
OF TXBYTCB TRRPX 2468 2468 2468 2468 DDK 242424

```

These columns are displayed only in Firmware Version 7

```

[1]
.....
.....
.....
.....
[2]
.....
.....
.....
.....

```

[Thirteen cycles of data not shown in this example]

```

[15]
** .....
** .....
** .....
** .....

```

Event: AG T Location: 2.36 Shot: 0 Frequency: 60.01
 Targets: INST 50
 Currents (A Pri), ABCNGQ: 2752 209 209 1 2689 2689

see Figure 12.1

Group 1

Group Settings:

RID =FEEDER 1 TID =STATION A
 CTR = 120 CTRN = 120 PTR = 180.00 PTRS = 180.00
 Z1MAG = 2.14 Z1ANG = 68.86
 ZOMAG = 6.38 ZOANG = 72.47 LL = 4.84
 E50P = 1 E50N = N E50G = N E50Q = N
 E51P = 1 E51N = N E51G = Y E51Q = N
 E32 = N ELOAD = N ESOTF = N EVOLT = N
 E25 = N EFLOC = Y ELOP = Y ECOMM = N
 E81 = 1 E79 = 2 ESV = 1 EDEM = THM EPWR = N
 ESSI = N
 50P1P = 15.00
 67P1D = 0.00
 50PP1P= OFF
 51PP = 6.00 51PC = U3 51PTD = 3.00 51PRS = N
 51GP = 1.50 51GC = U3 51GTD = 1.50 51GRS = N
 27B81P= 40.00 81D1P = 59.10 81D1D = 6.00
 790I1 = 30.00 790I2 = 600.00
 79RSD = 1800.00 79RSLD= 300.00 79CLSD= 0.00
 DMTC = 5
 PDEMP = 5.00 NDEMP = 1.50 GDEMP = 1.50 QDEMP = 1.50
 TDURD = 9.00 CFD = 60.00 3POD = 1.50 50LP = 0.25
 SV1PU = 12.00 SV1DO = 2.00

SELogic group 1

SELogic Control Equations:

TR =0C + 51PT + 51GT + 81D1T + LB3 + 50P1 * SHO
 TRCOMM=0
 TRSOTF=0
 DTT =0
 ULTR =!(51P + 51G)
 PT1 =0
 LOG1 =0
 PT2 =0
 LOG2 =0
 BT =0
 52A =IN101
 CL =CC + LB4
 ULCL =TRIP
 79RI =TRIP
 79RIS =52A + 79CY
 79DTL =0C + !IN102 + LB3
 79DLS =79LO
 79SKP =0
 79STL =TRIP
 79BRS =0
 79SEQ =0
 79CLS =1
 SET1 =0
 RST1 =0
 SET2 =0
 RST2 =0
 SET3 =0
 RST3 =0
 SET4 =0
 RST4 =0
 SET5 =0
 RST5 =0
 SET6 =0
 RST6 =0

SET7 =0
RST7 =0
SET8 =0
RST8 =0
SET9 =0
RST9 =0
SET10 =0
RST10 =0
SET11 =0
RST11 =0
SET12 =0
RST12 =0
SET13 =0
RST13 =0
SET14 =0
RST14 =0
SET15 =0
RST15 =0
SET16 =0
RST16 =0
67P1TC=1
67P2TC=1
67P3TC=1
67P4TC=1
67N1TC=1
67N2TC=1
67N3TC=1
67N4TC=1
67G1TC=1
67G2TC=1
67G3TC=1
67G4TC=1
67Q1TC=1
67Q2TC=1
67Q3TC=1
67Q4TC=1
51ATC =1
51BTC =1
51CTC =1
51PTC =1
51NTC =1
51GTC =1
51QTC =1
SV1 =TRIP
SV2 =0
SV3 =0
SV4 =0
SV5 =0
SV6 =0
SV7 =0
SV8 =0
SV9 =0
SV10 =0
SV11 =0
SV12 =0
SV13 =0
SV14 =0
SV15 =0
SV16 =0
OUT101=TRIP
OUT102=CLOSE
OUT103=SV1T
OUT104=0
OUT105=0
OUT106=0

```
OUT107=0
OUT201=0
OUT202=0
OUT203=0
OUT204=0
OUT205=0
OUT206=0
OUT207=0
OUT208=0
OUT209=0
OUT210=0
OUT211=0
OUT212=0
DP1 =IN102
DP2 =52A
DP3 =0
DP4 =0
DP5 =0
DP6 =0
DP7 =0
DP8 =0
DP9 =0
DP10 =0
DP11 =0
DP12 =0
DP13 =0
DP14 =0
DP15 =0
DP16 =0
SS1 =0
SS2 =0
SS3 =0
SS4 =0
SS5 =0
SS6 =0
ER =/51P + /51G + /OUT103
FAULT =51P + 51G
BSYNCH=52A
CLMON =0
BKMON =TRIP
E32IV =1
TMB1A =0
TMB2A =0
TMB3A =0
TMB4A =0
TMB5A =0
TMB6A =0
TMB7A =0
TMB8A =0
TMB1B =0
TMB2B =0
TMB3B =0
TMB4B =0
TMB5B =0
TMB6B =0
TMB7B =0
TMB8B =0
```

```

Global Settings:
TGR   = 180.00  NFREQ = 60      PHROT = ABC
DATE_F= MDY    FP_TO = 15.00   SCROLL= 2      FPNGD = IN
LER   = 15     PRE   = 4       DCLOP = OFF    DCHIP = OFF
IN101D= 0.50  IN102D= 0.50  IN103D= 0.50  IN104D= 0.50
IN105D= 0.50  IN106D= 0.50
IN201D= 0.50  IN202D= 0.50  IN203D= 0.50  IN204D= 0.50
IN205D= 0.50  IN206D= 0.50  IN207D= 0.50  IN208D= 0.50
EBMON = Y     COSP1 = 10000  COSP2 = 150   COSP3 = 12
KASP1 = 1.20  KASP2 = 8.00   KASP3 = 20.00
-
=>>

```

Figure 12.2: Example Standard 15-Cycle Event Report 1/4-Cycle Resolution

Figure 12.3 and Figure 12.4 look in detail at 1 cycle of A-phase current (channel IA) identified in Figure 12.2. Figure 12.3 shows how the event report ac current column data relates to the actual sampled waveform and RMS values. Figure 12.4 shows how the event report current column data can be converted to phasor RMS values. Voltages are processed similarly.

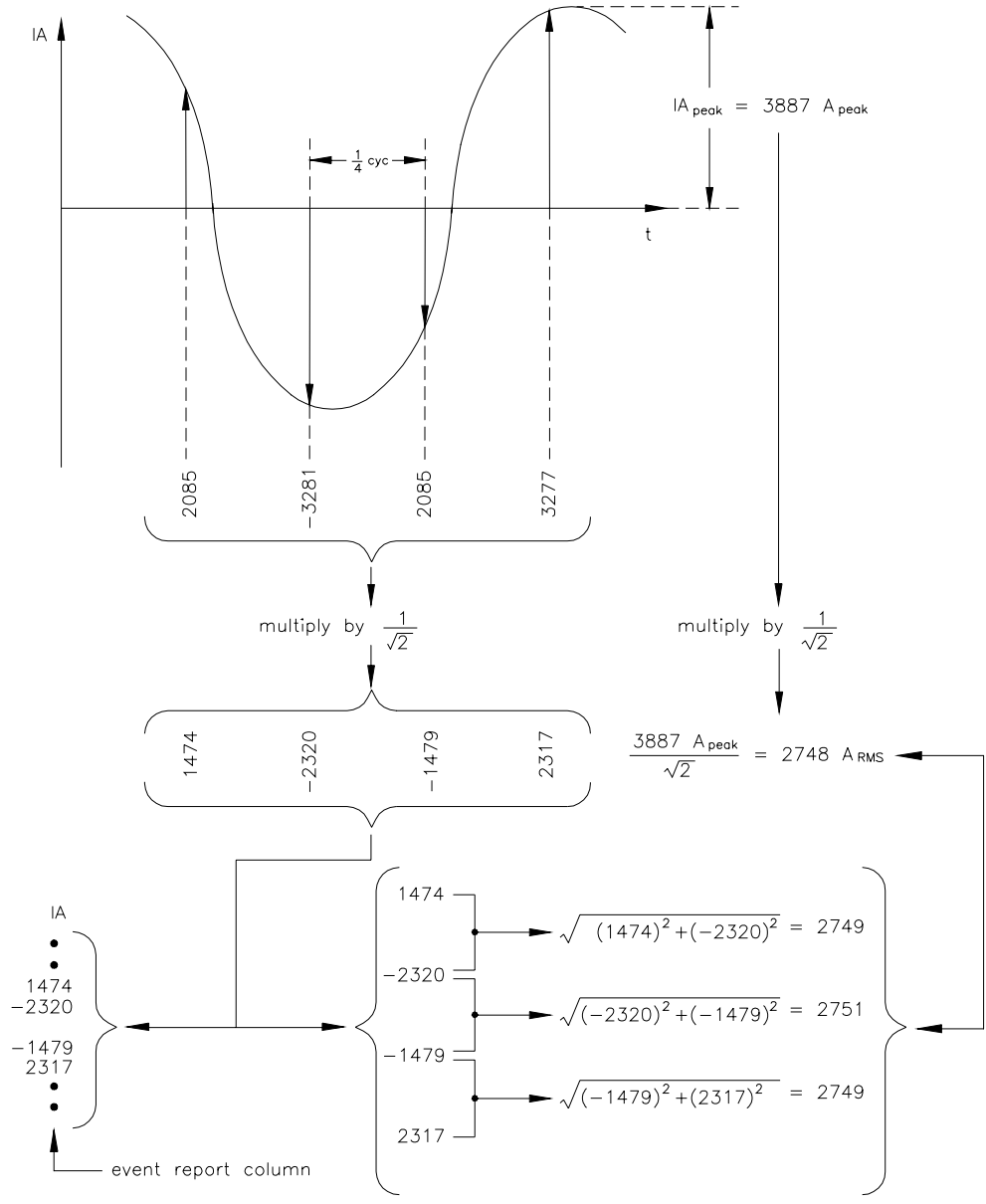


Figure 12.3: Derivation of Event Report Current Values and RMS Current Values From Sampled Current Waveform

In Figure 12.3, note that any two rows of current data from the event report in Figure 12.2, 1/4 cycle apart, can be used to calculate RMS current values.

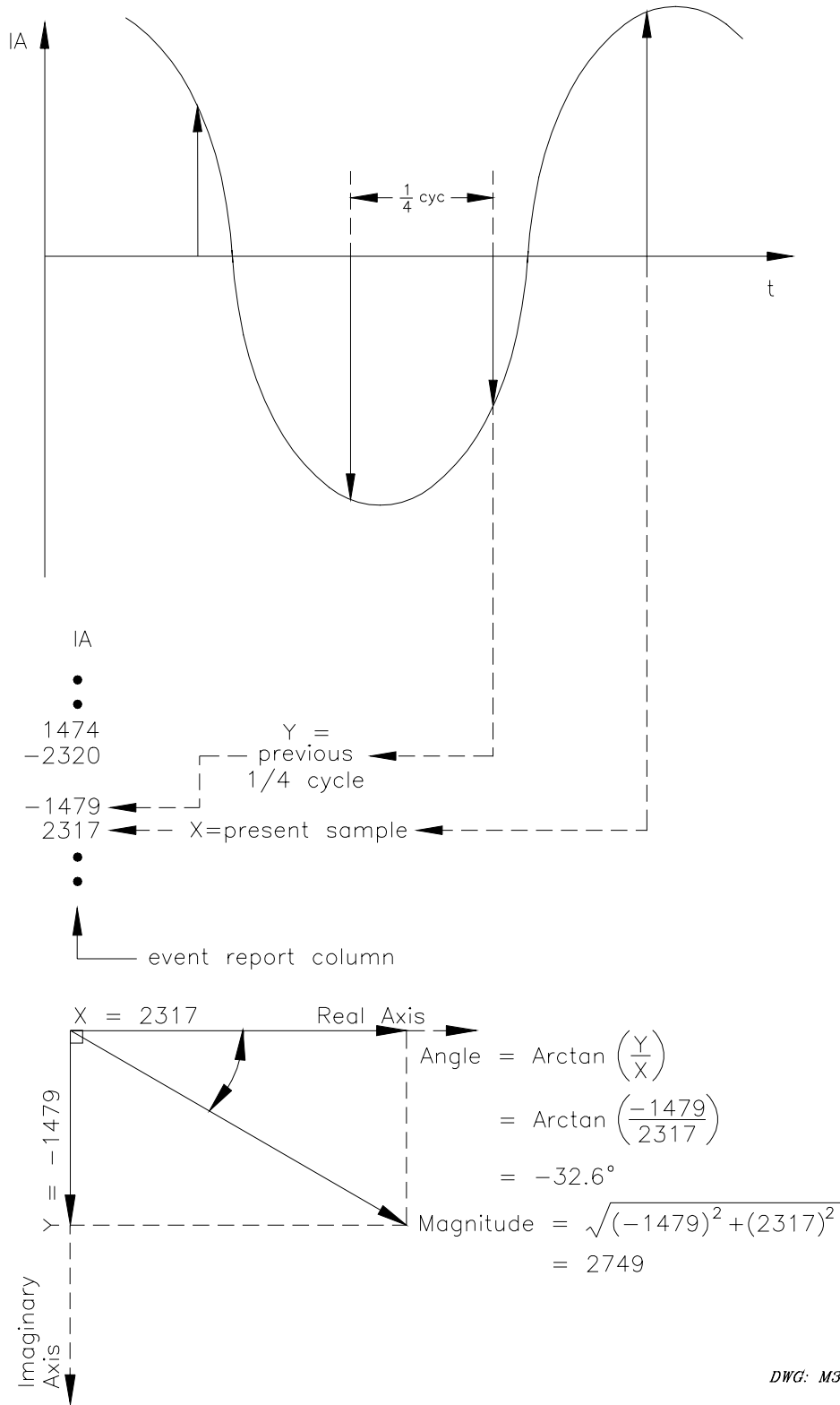


Figure 12.4: Derivation of Phasor RMS Current Values From Event Report Current Values

In Figure 12.4, note that two rows of current data from the event report in Figure 12.2, 1/4 cycle apart, can be used to calculate phasor RMS current values. In Figure 12.4, at the present sample, the phasor RMS current value is:

$$IA = 2749 \text{ A } \angle -32.6^\circ$$

The present sample (IA = 2317 A) is a real RMS current value that relates to the phasor RMS current value:

$$2749 \text{ A } * \cos(-32.6^\circ) = 2317 \text{ A}$$

EXAMPLE SEQUENTIAL EVENTS RECORDER (SER) REPORT

The following example sequential events recorder (SER) report in Figure 12.5 (from a Model 0351x0 relay) also corresponds to the example standard 15-cycle event report in Figure 12.2.

#	DATE	TIME	ELEMENT	STATE
19	04/12/99	08:30:33.222	Relay newly powered up or settings changed	
18	04/12/99	09:20:22.830	IN102	Asserted
17	04/12/99	09:27:58.364	LB4	Asserted
16	04/12/99	09:27:58.364	OUT102	Asserted
15	04/12/99	09:27:58.368	LB4	Deasserted
14	04/12/99	09:27:58.385	IN101	Asserted
13	04/12/99	09:27:58.385	OUT102	Deasserted
12	04/12/99	09:28:03.385	79L0	Deasserted
11	04/12/99	09:28:31.717	51G	Asserted
10	04/12/99	09:28:31.721	51P	Asserted
9	04/12/99	09:28:31.729	50P1	Asserted
8	04/12/99	09:28:31.729	79CY	Asserted
7	04/12/99	09:28:31.729	OUT101	Asserted
6	04/12/99	09:28:31.808	50P1	Deasserted
5	04/12/99	09:28:31.816	51G	Deasserted
4	04/12/99	09:28:31.816	51P	Deasserted
3	04/12/99	09:28:31.816	IN101	Deasserted
2	04/12/99	09:28:31.879	OUT101	Deasserted
1	04/12/99	09:28:32.374	OUT102	Asserted

Figure 12.5: Example Sequential Events Recorder (SER) Event Report

The SER event report rows in Figure 12.5 are explained in the following text, numbered in correspondence to the # column. The boxed, numbered comments in Figure 12.2 also correspond to the # column numbers in Figure 12.5. The SER event report in Figure 12.5 contains records of events that occurred before and after the standard event report in Figure 12.2.

SER

Row No.	Explanation
19	Relay newly powered up.
18	Input IN102 is asserted to enable reclosing. Related setting: 79DTL = !IN102 + ... [=NOT(IN102) + ...]
17, 16	Local bit LB4 is operated from the front panel to assert close output contact OUT102 to close the circuit breaker (see Figure 6.1). Related settings: CL = LB4 (LB4 operates as a manual close) OUT102 = CLOSE
15	Local bit LB4 deasserts automatically the next 1/4 cycle—close signal is latched in by close logic.
14, 13	Input IN101 asserts, indicating that the circuit breaker closed. Close output contact OUT102 consequently deasserts. Related setting: 52A = IN101
12	The relay leaves the Lockout State (79LO) and goes to the Reset State, 300 cycles after the circuit breaker closes. Related setting: 79RSLD = 300.000 cycles Time difference: 09:28:03.385 – 09:27:58.364 = 5.021 seconds (= 300 cycles)
11, 10	Time-overcurrent elements 51PT and 51GT pickup and start timing at fault inception (51P and 51G are the respective pickup indicators).
9, 8, 7	Instantaneous overcurrent element 50P1 picks up and asserts trip output contact OUT101 to trip the circuit breaker (see Figure 5.1). Relay goes to the Reclose Cycle State (79CY). Related settings: TR = ...+ 50P1*SH0 OUT101 = TRIP
6, 5, 4	Instantaneous overcurrent element 50P1 and time-overcurrent element pickups 51P and 51G drop out as the circuit breaker interrupts fault current.
3	Input IN101 deasserts, indicating that the circuit breaker opened.
2	Trip output contact OUT101 deasserts after being asserted a minimum of 9 cycles. Related settings: TDURD = 9.000 cycles Time difference: 09:28:31.879 – 09:28:31.729 = 0.150 seconds (= 9 cycles) Open interval 79OI1 does not start timing until trip output contact OUT101 deasserts. Related settings: 79STL = TRIP
1	Close output contact OUT102 asserts for first automatic reclose. Related settings: 79OI1 = 30.000 Time difference: 09:28:32.374 – 09:28:31.879 = 0.495 seconds (= 30 cycles)

SAG/SWELL/INTERRUPTION (SSI) REPORT (AVAILABLE IN FIRMWARE VERSION 7)

See Figure 12.6 for an example SSI report.

SSI Triggering and Recording

The SEL-351-7 Relay can perform automatic voltage disturbance monitoring for three-phase systems. The SSI Recorder uses the SSI Relay Word bits to determine when to start (trigger) and when to stop recording. The recorded data is available through the SSI Report.

See *Voltage Sag, Swell, and Interruption Elements (Available in Firmware Version 7)* in *Section 3: Overcurrent, Voltage, Synchronism Check, Frequency, and Power Elements* for details on the operation of the SSI Relay Word bits.

The SSI recorder operates (adds new entries to the stored SSI report) only when group setting $ESSI = Y$ in the active setting group, although the SSI report can be viewed at any time.

The SSI recorder uses nonvolatile memory, so any stored SSI data will not be erased by deenergizing the relay. The relay needs some time to store new SSI data in nonvolatile memory, so if a system power outage also causes the relay power to fail, there may not be an SSI record of the disturbance. This is not a concern in substations where the relay is powered by a substation battery.

The relay triggers (generates) entries in the SSI report on the assertion of any single-phase sag, swell, or interruption relay element (Relay Word bits SAG_p , SW_p , INT_p , where $p = A, B, \text{ or } C$), or when manually triggered by the **SSI T** Command.

SSI Report Entries

- Entry number (1 is the most recent entry)
- Date and time stamp of entry
- Phase current magnitudes ($I_{A,B,C}$) as a percentage of the nominal current rating of the phase current inputs (5 A or 1 A)
- Calculated residual current magnitude (I_G) as a percentage of the nominal current rating of the phase current inputs (5 A or 1 A)
- Neutral current magnitude (I_N) as a percentage of the nominal current rating of the neutral current input (5 A, 1 A, or 0.05 A)
- Phase-neutral voltage magnitudes (V_A, V_B, V_C) as a percentage of V_{BASE}
- Synchronizing voltage magnitude (V_S) as a percentage of V_{BASE} ; displayed value
$$V_S = \frac{V_S(\text{secondary}) \cdot PTRS}{1000 \cdot V_{base}} \cdot 100\%$$
- Base voltage magnitude (V_{BASE}) in kV primary (memorized positive-sequence voltage)
- Phase A, B, and C SSI element status columns; see Table 12.4
- Trigger state, "*" if present (in the column marked "S")
- SSI recorder status; see Table 12.5

Note: Any current or voltage value greater than 999 percent will be replaced by “\$\$\$” in the SSI report.

Table 12.4: Phase SSI columns

Symbol	Meaning (for Each Column p = A, B, or C)
.	No SSI bits asserted for phase p
O	Overvoltage (SWp asserted)
U	Undervoltage (SAGp asserted)
I	Interruption (INTp asserted; SAGx asserted, unless setting VSAG = OFF)

Table 12.5: Status SSI column

Symbol	Meaning (Action)	Duration
R	Ready (when the SSI logic first acquires a valid V_{BASE} value)	Single entry
P	Pre-disturbance (4 samples per cycle). Always signifies a new disturbance.	12 samples (3 cycles)
F	Fast recording mode (4 samples per cycle)	Varies. At least one SSI element must be asserted.
E	End (post-disturbance at 4 samples per cycle)	Up to 16 samples (4 cycles). No SSI elements asserted.
M	Medium recording mode (one sample per cycle)	Maximum of 176 cycles
S	Slow recording mode (one sample per 64 cycles)	Maximum of 4096 cycles
D	Daily recording mode (one sample per day, just after midnight)	Indefinite
X	Data overflow (single entry that indicates that data was lost prior to the present entry)	Single entry

See Figure 12.6 for an example Sag/Swell/Interruption (SSI) report.

SSI Recorder Operation: Overview

The SSI Recorder operation can be summarized as follows: When power is first applied to the relay and setting ESSI = “Y”, (or setting ESSI is changed from “N” to “Y”), the relay measures the voltage inputs to determine if a valid three-phase signal is present. When the conditions are satisfied for at least twelve seconds, the positive-sequence voltage, V1, is “memorized” as the Vbase reference voltage. This causes a single “R” entry to be placed in the SSI archive, which indicates that the recorder is ready. The Vbase value is allowed to change on a gradual basis to follow normal system voltage variations, but is “locked” when a disturbance occurs.

When any SSI Relay Word Bit asserts or the **SSI T** serial port command is issued, the recorder will begin recording.

When operating, the SSI Recorder archives the following information:

- Currents Ia, Ib, Ic, Ig, and In as a percent of the nominal current rating (shown in the report heading)
- Voltages Va, Vb, Vc, and Vs as a percent of the Vbase quantity
- The Vbase quantity, in kV primary
- The state of the Sag/Swell/Interruption Relay Word bits, by phase
- The trigger status
- The recorder status

Entries are made at a varying recording rate: fastest when the SSI Relay Word bits are changing states, and slowest if the SSI Relay Word bits are quiet. Eventually, it can get as slow as one sample per day. The faster recording mode will be initiated from any of the slower recording modes, as soon as any SSI bit or the **SSI T** condition changes state.

Recording is stopped when all SSI Relay Word bits and the trigger condition stay deasserted for at least four cycles.

SSI Recorder Operation: Detailed Description

From the SSI Recorder Ready state, upon the initial assertion of one of the single-phase SSI Relay Word bits or a manual trigger condition, the relay records SSI data in the following sequence:

- **Pre-disturbance recording:** Record pre-trigger entries at $\frac{1}{4}$ -cycle intervals with the SSI Recorder status field displaying “P”. Since no SSI elements are asserted, the Phase columns A, B, and C will display “.”. The pre-disturbance state lasts for a total of twelve samples, or three cycles, unless there are “back-to-back” disturbances that reduce the number of “P” entries.
- **Fast recording (also End recording):** Record one entry every $\frac{1}{4}$ -cycle, with the SSI Recorder status field displaying “F” (if any single-phase SSI elements are asserted or the manual trigger condition is asserted), or “E” (if none of the single-phase SSI elements are asserted). If the manual trigger condition is present, a “*” will be recorded. The Phase columns will show one of “.”, “O”, “U”, “I”. The Fast/End recording mode continues until four cycles elapse with no single-phase SSI element or manual trigger condition changing state. The relay then proceeds to the state determined by the following tests (processed in the order shown):
 - If INT3P is asserted, switch to daily recording mode. (This keeps the relay from recording medium and slow speed detailed information during a complete outage.)
 - Otherwise, if any single-phase SSI elements are asserted, switch to the medium recording mode.
 - Otherwise, stop recording.

- **Medium recording:** Record one entry per cycle, with the SSI Recorder status field displaying “M”. The phase columns will show one of “.”, “O”, “U”, “I”. The medium recording mode continues for 176 cycles, unless one of the single-phase SSI elements or the manual trigger condition changes state, which causes the recorder to start over in Fast mode (with up to three samples prior to the change). At the end of medium recording mode, the recorder switches to the slow recording mode.
- **Slow recording:** Record one entry every 64 cycles, with the SSI Recorder status field displaying “S”. The phase columns will show one of “.”, “O”, “U”, “I”. The slow recording mode continues for 4,096 cycles (64 entries), unless one of the single-phase SSI elements or the manual trigger condition changes state, which causes the recorder to start over in fast mode (with up to eight samples prior to the change). At the end of slow recording mode, the recorder switches to the daily recording mode.
- **Daily recording:** record one entry every day just past midnight (00:00:00), with the SSI Recorder status field displaying “D”. The phase columns will show one of “.”, “O”, “U”, “I”. The daily recording mode continues until any SSI Relay element or the manual trigger condition changes state, which causes the recorder to start over in fast mode (with up to eight samples prior to the change).

An overflow condition can occur when the SSI recorder cannot keep up with the data generated during disturbances that create a large number of SSI entries. The nonvolatile memory that is used for the SSI archive has a longer “write” time than the Random Access Memory (RAM) that is used to temporarily store the SSI data, so it is possible that the data in RAM will overwrite itself if the transfer to Flash memory gets too far behind. The SSI report will show an “X” in the REC column if this happens, and it will be on the first entry after the overflow. The overflow condition may also occur if the relay is saving an event report to nonvolatile memory, since the memory can only be used by one procedure at a time.

SSI Report Memory Details

The relay retains a minimum of 3855 of the most recent SSI entries in nonvolatile memory. The relay can hold a maximum of 7710 entries. When the recorder memory reaches 7710 entries and further entries occur, the oldest 3855 memory locations are cleared in a block to make room for newer entries. Therefore, the apparent SSI memory size can vary between 3855 and 7710 entries. If the SSI recorder memory clears while an SSI report is being displayed, the SSI report will stop and display this message:

Command Aborted, Data overwrite occurred

Retrieving the SSI Report

The recorded SSI data can be viewed from any setting group, even if setting ESSI = N. Row 1 is the most recently triggered row. View the SSI report by date or SSI row number as outlined in the examples below.

**Example SSI
Serial Port
Commands**

Format

- SSI** If **SSI** is entered with no numbers following it, all available rows are displayed. They display with the oldest row at the beginning (top) of the report and the latest row (row 1) at the end (bottom) of the report. Chronological progression through the report is down the page and in descending row number.
- SSI 17** If **SSI** is entered with a single number following it (17 in this example), the first 17 rows are displayed, if they exist. They display with the oldest row (row 17) at the beginning (top) of the report and the latest row (row 1) at the end (bottom) of the report. Chronological progression through the report is down the page and in descending row number.
- SSI 10 33** If **SSI** is entered with two numbers following it (10 and 33 in this example; $10 < 33$), all the rows between (and including) rows 10 and 33 are displayed, if they exist. They display with the oldest row (row 33) at the beginning (top) of the report and the latest row (row 10) at the end (bottom) of the report. Chronological progression through the report is down the page and in descending row number.
- SSI 47 22** If **SSI** is entered with two numbers following it (47 and 22 in this example; $47 > 22$), all the rows between (and including) rows 47 and 22 are displayed, if they exist. They display with the newest row (row 22) at the beginning (top) of the report and the oldest row (row 47) at the end (bottom) of the report. Reverse chronological progression through the report is down the page and in ascending row number.
- SSI 3/30/00** If **SSI** is entered with one date following it (date 3/30/00 in this example), all the rows on that date are displayed, if they exist. They display with the oldest row at the beginning (top) of the report and the latest row at the end (bottom) of the report, for the given date. Chronological progression through the report is down the page and in descending row number.
- SSI 2/17/00 3/23/00** If **SSI** is entered with two dates following it (date 2/17/00 chronologically precedes date 3/23/00 in this example), all the rows between (and including) dates 2/17/00 and 3/23/00 are displayed, if they exist. They display with the oldest row (date 2/17/00) at the beginning (top) of the report and the latest row (date 3/23/00) at the end (bottom) of the report. Chronological progression through the report is down the page and in descending row number.
- SSI 3/16/00 1/5/00** If **SSI** is entered with two dates following it (date 3/16/00 chronologically follows date 1/5/00 in this example), all the rows between (and including) dates 1/5/00 and 3/16/00 are displayed, if they exist. They display with the latest row (date 3/16/00) at the beginning (top) of the report and the oldest row (date 1/5/00) at the end (bottom) of the report. Reverse chronological progression through the report is down the page and in ascending row number.

The date entries in the above example **SSI** commands are dependent on the Date Format setting `DATE_F`. If setting `DATE_F = MDY`, then the dates are entered as in the above examples (Month/Day/Year). If setting `DATE_F = YMD`, then the dates are entered Year/Month/Day.

If the requested **SSI** event report rows do not exist, the relay responds:

No Voltage Sag/Swell/Interruption Data

Clearing the SSI Report

Clear the **SSI** report from nonvolatile memory with the **SSI C** command as shown in the following example:

```
=>SSI C <ENTER>
Clear the Voltage Sag/Swell/Interruption buffer
Are you sure (Y/N)? Y <ENTER>
Clearing Complete
```

The **SSI C** command is available in any setting group and on any serial port.

If the **SSI C** command is issued on one serial port while another serial port is being used to display an SSI report, the clearing action will terminate the SSI report retrieval.

If maximum SSI recorder capacity is desired, the SSI Report should be checked periodically, with the data captured to a computer file using a terminal emulation program. Once the data has been viewed or captured, use the **SSI C** command to clear the SSI recorder.

Clearing the SSI Recorder makes it easier to tell if any new disturbances have been recorded, and it also allows the SSI Archive to record the maximum of 7710 entries. If more than 7710 entries occur, the oldest half of the SSI archive will be erased to make room for the new entries. The most recent 3855 entries are always available.

Triggering the SSI Recorder

Manually force the SSI Recorder to trigger using the **SSI T** command as shown in the following example:

```
=>SSI T <ENTER>
Triggered
```

The **SSI T** command is only available if group setting `ESSI = Y` in the active setting group.

If an **SSI T** command is issued when setting `ESSI = N`, the relay will respond as follows:

```
Command is not available
```

If an **SSI T** command is issued before Vbase has initialized, the relay will respond as follows:

```
Did Not Trigger
```

See Vbase Initialization in *Section 3: Overcurrent, Voltage, Synchronism Check, Frequency, and Power Elements* for details on the initializing conditions.

The **SSI T** command is useful for testing, because it provides an easy method of creating some SSI Report entries without the need to remove voltage signals or connect a test set, providing Vbase has already been initialized.

Resetting the SSI Recorder Logic

During relay commissioning or test procedures, the SSI recorder may memorize the Vbase quantity when test voltages or settings are applied. This could cause the recorder to declare a false SAG or SWELL condition when normal system voltages are applied. Reset the SSI Recorder logic and clear the Vbase value by issuing the **SSI R** command as shown in the following example:

```
=>SSI R <ENTER>
Reset the Voltage Sag/Swell/Interruption monitor
Are you sure (Y/N)? Y <ENTER>
Voltage Sag/Swell/Interruption monitor reset
```

After the relay detects satisfactory voltage signals for at least twelve seconds, the SSI Recorder is armed and a START entry is written to the SSI archive.

The **SSI R** command is only available if group setting **ESSI = Y** in the active setting group. Attempting the **SSI R** command when **ESSI = N** will display:

```
Command is not available
```

The relay automatically performs an equivalent action to the **SSI R** command:

- When the relay is powered-up and setting **ESSI = Y**
- After a group change or setting change that changes active setting **ESSI = N** to **ESSI = Y**.
- After a **STA C** command (Level 2)

Sample SSI Report

The Sag/Swell/Interruption (SSI) report in Figure 12.6 shows a voltage sag on B-phase and a voltage swell on C-phase caused by a single-phase fault on B-phase that is cleared by a remote device. (Relay inputs I_n and V_s are not connected.)

```

=>SSI <ENTER>

FEEDER A27                      Date: 12/06/00   Time: 09:12:07.369
CROWN SUB

FID=SEL-351-7-R3xx-V0-Zxxxxxx-D2000xxxx   CID=xxxx

      I nom. A B C G = 5 Amp  N = 5 Amp

#      Date      Time      Current(% I nom.)  Voltage(% Vbase) Vbase Ph ST
      #          #          #          Ia Ib Ic Ig In Va Vb Vc Vs (kV) ABC
36  11/22/00 08:47:24.272  11 13 15 3 0 100 99 100 0 14.94 ... R
35  12/05/00 16:21:12.635  20 23 28 7 0 98 98 98 0 15.29 ... P
34  12/05/00 16:21:12.639  20 22 29 8 0 98 98 98 0 15.29 ... P
33  12/05/00 16:21:12.644  20 22 28 7 0 98 98 98 0 15.29 ... P
32  12/05/00 16:21:12.648  20 23 28 7 0 98 98 98 0 15.29 ... P
31  12/05/00 16:21:12.652  20 23 28 8 0 98 98 98 0 15.29 ... P
30  12/05/00 16:21:12.656  20 22 29 8 0 98 98 98 0 15.29 ... P
29  12/05/00 16:21:12.660  20 31 29 26 0 98 98 99 0 15.29 ... P
28  12/05/00 16:21:12.664  20 62 30 40 0 98 90 101 0 15.29 ... P
27  12/05/00 16:21:12.669  20 67 32 50 0 98 89 105 0 15.29 ... P
26  12/05/00 16:21:12.673  20 112 33 88 0 98 78 108 0 15.29 ... P
25  12/05/00 16:21:12.677  20 111 34 86 0 98 78 111 0 15.29 ... P
24  12/05/00 16:21:12.681  20 125 34 99 0 98 75 111 0 15.29 ... P
23  12/05/00 16:21:12.685  20 125 34 99 0 98 75 111 0 15.29 .U. F
22  12/05/00 16:21:12.689  20 125 35 99 0 98 75 111 0 15.29 .U. F
21  12/05/00 16:21:12.694  20 122 34 94 0 98 76 110 0 15.29 .U0 F
20  12/05/00 16:21:12.698  20 88 33 62 0 98 82 108 0 15.29 .U0 F
19  12/05/00 16:21:12.702  20 88 31 60 0 98 83 104 0 15.29 .U0 F
18  12/05/00 16:21:12.706  20 34 30 8 0 98 94 101 0 15.29 .U0 F
17  12/05/00 16:21:12.710  20 34 29 9 0 98 94 98 0 15.29 .U0 F
16  12/05/00 16:21:12.714  20 15 28 12 0 98 98 98 0 15.29 .U. F
15  12/05/00 16:21:12.718  19 15 28 12 0 98 98 98 0 15.29 .U. F
14  12/05/00 16:21:12.723  20 14 29 12 0 98 98 98 0 15.29 ... E
13  12/05/00 16:21:12.727  20 14 28 12 0 98 98 98 0 15.29 ... E
12  12/05/00 16:21:12.731  20 15 28 12 0 98 98 98 0 15.29 ... E
11  12/05/00 16:21:12.735  20 15 29 12 0 98 98 98 0 15.29 ... E
10  12/05/00 16:21:12.739  20 14 29 12 0 98 98 98 0 15.29 ... E
9   12/05/00 16:21:12.743  20 14 28 12 0 98 98 98 0 15.29 ... E
8   12/05/00 16:21:12.748  20 15 28 12 0 98 98 98 0 15.29 ... E
7   12/05/00 16:21:12.752  19 15 28 12 0 98 98 98 0 15.29 ... E
6   12/05/00 16:21:12.756  19 14 28 12 0 98 98 98 0 15.29 ... E
5   12/05/00 16:21:12.760  20 14 28 12 0 98 98 98 0 15.29 ... E
4   12/05/00 16:21:12.764  20 15 28 12 0 98 98 98 0 15.29 ... E
3   12/05/00 16:21:12.768  19 15 28 12 0 98 98 98 0 15.29 ... E
2   12/05/00 16:21:12.773  19 14 29 12 0 98 98 98 0 15.29 ... E
1   12/05/00 16:21:12.777  20 14 28 12 0 98 98 98 0 15.29 ... E

```

Figure 12.6: Example Sag/Swell/Interruption (SSI) Report

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SECTION 13: TESTING AND TROUBLESHOOTING

INTRODUCTION

This section provides guidelines for determining and establishing test routines for the SEL-351 Relay. Included are discussions on testing philosophies, methods, and tools. Relay self-tests and troubleshooting procedures are shown at the end of the section.

TESTING PHILOSOPHY

Protective relay testing may be divided into three categories: acceptance, commissioning, and maintenance testing. The categories are differentiated by when they take place in the life cycle of the relay as well as in the test complexity.

The paragraphs below describe when to perform each type of test, the goals of testing at that time, and the relay functions that you need to test at each point. This information is intended as a guideline for testing SEL relays.

Acceptance Testing

When: When qualifying a relay model to be used on the utility system.

- Goals:
- a) Ensure relay meets published critical performance specifications such as operating speed and element accuracy.
 - b) Ensure that the relay meets the requirements of the intended application.
 - c) Gain familiarity with relay settings and capabilities.

What to test: All protection elements and logic functions critical to the intended application.

SEL performs detailed acceptance testing on all new relay models and versions. We are certain the relays we ship meet their published specifications. It is important for you to perform acceptance testing on a relay if you are unfamiliar with its operating theory, protection scheme logic, or settings. This helps ensure the accuracy and correctness of the relay settings when you issue them.

Commissioning Testing

When: When installing a new protection system.

- Goals:
- a) Ensure that all system ac and dc connections are correct.
 - b) Ensure that the relay functions as intended using your settings.
 - c) Ensure that all auxiliary equipment operates as intended.

What to test: All connected or monitored inputs and outputs, polarity and phase rotation of ac connections, simple check of protection elements.

SEL performs a complete functional check and calibration of each relay before it is shipped. This helps ensure that you receive a relay that operates correctly and accurately. Commissioning tests should verify that the relay is properly connected to the power system and all auxiliary

equipment. Verify control signal inputs and outputs. Check breaker auxiliary inputs, SCADA control inputs, and monitoring outputs. Use an ac connection check to verify that the relay current and voltage inputs are of the proper magnitude and phase rotation.

Brief fault tests ensure that the relay settings are correct. It is not necessary to test every relay element, timer, and function in these tests.

At commissioning time, use the relay METER command to verify the ac current and voltage magnitude and phase rotation. Use the PULSE command to verify relay output contact operation. Use the TARGET command to verify optoisolated input operation.

Maintenance Testing

When: At regularly scheduled intervals or when there is an indication of a problem with the relay or system.

Goals: a) Ensure that the relay is measuring ac quantities accurately.
b) Ensure that scheme logic and protection elements are functioning correctly.
c) Ensure that auxiliary equipment is functioning correctly.

What to test: Anything not shown to have operated during an actual fault within the past maintenance interval.

SEL relays use extensive self-testing capabilities and feature detailed metering and event reporting functions that lower the utility dependence on routine maintenance testing.

Use the SEL relay reporting functions as maintenance tools. Periodically verify that the relay is making correct and accurate current and voltage measurements by comparing the relay METER output to other meter readings on that line. Review relay event reports in detail after each fault. Using the event report current, voltage, and relay element data, you can determine that the relay protection elements are operating properly. Using the event report input and output data, you can determine that the relay is asserting outputs at the correct instants and that auxiliary equipment is operating properly. At the end of your maintenance interval, the only items that need testing are those that have not operated during the maintenance interval.

The basis of this testing philosophy is simple: If the relay is correctly set and connected, is measuring properly, and no self-test has failed, there is no reason to test it further.

Each time a fault occurs the protection system is tested. Use event report data to determine areas requiring attention. Slow breaker auxiliary contact operations and increasing or varying breaker operating time can be detected through detailed analysis of relay event reports.

Because SEL relays are microprocessor-based, their operating characteristics do not change over time. Time-overcurrent operating times are affected only by the relay settings and applied signals. It is not necessary to verify operating characteristics as part of maintenance checks.

At SEL, we recommend that maintenance tests on SEL relays be limited under the guidelines provided above. The time saved may be spent analyzing event data and thoroughly testing those systems that require more attention.

TESTING METHODS AND TOOLS

Test Features Provided by the Relay

The following features assist you during relay testing.

METER Command	The METER command shows the ac currents and voltages (magnitude and phase angle) presented to the relay in primary values. In addition, the command shows power system frequency (FREQ) and the voltage input to the relay power supply terminals (VDC). Compare these quantities against other devices of known accuracy. The METER command is available at the serial ports and front-panel display. See <i>Section 10: Serial Port Communications and Commands</i> and <i>Section 11: Front-Panel Interface</i> .
EVENT Command	The relay generates a 15- or 30-cycle event report in response to faults or disturbances. Each report contains current and voltage information, relay element states, and input/output contact information. If you question the relay response or your test method, use the event report for more information. The EVENT command is available at the serial ports. See <i>Section 12: Standard Event Reports, Sag/Swell/Interruption Report, and SER</i> .
SER Command	The relay provides a Sequential Events Recorder (SER) event report that time-tags changes in relay element and input/output contact states. The SER provides a convenient means to verify the pickup/dropout of any element in the relay. The SER command is available at the serial ports. See <i>Section 12: Standard Event Reports, Sag/Swell/Interruption Report, and SER</i> .
TARGET Command	Use the TARGET command to view the state of relay control inputs, relay outputs, and relay elements individually during a test. The TARGET command is available at the serial ports and the front panel. See <i>Section 10: Serial Port Communications and Commands</i> and <i>Section 11: Front-Panel Interface</i> .
PULSE Command	Use the PULSE command to test the contact output circuits. The PULSE command is available at the serial ports and the front panel. See <i>Section 10: Serial Port Communications and Commands</i> .

Low-Level Test Interface

The SEL-351 Relay has a low-level test interface between the calibrated input module and the separately-calibrated processing module. You may test the relay in either of two ways: conventionally, by applying ac current signals to the relay inputs or by applying low magnitude ac voltage signals to the low-level test interface. Access the test interface by removing the relay front panel.

Figure 13.1 shows the low-level interface connections. This drawing also appears on the inside of the relay front panel. Remove the ribbon cable between the two modules to access the outputs of the input module and the inputs to the processing module (relay main board).

You can test the relay processing module using signals from the SEL-RTS Low-Level Relay Test System. Never apply voltage signals greater than 9 volts peak-peak to the low-level test interface. Figure 13.1 shows the signal scaling factors.

Access the front-panel TAR command from the front-panel OTHER pushbutton menu. To display the state of the 51PT element on the front-panel display, press the OTHER pushbutton, cursor to the TAR option, and press SELECT. Press the up arrow pushbutton until TAR 6 is displayed on the top row of the LCD. The bottom row of the LCD displays all elements asserted in Relay Word Row 6. The relay maps the state of the elements in Relay Word Row 6 on the bottom row of LEDs. The 51PT element state is reflected on the LED labeled RS. See Table 9.3 for the correspondence between the Relay Word elements and the TAR command.

To view the 51PT element status from the serial port, issue the **TAR 51PT** command. The relay will display the state of all elements in the Relay Word row containing the 51PT element.

Review TAR command descriptions in *Section 10: Serial Port Communications and Commands* and *Section 11: Front-Panel Interface* for further details on displaying element status via the TAR commands.

Testing Via Output Contacts

You can set the relay to operate an output contact for testing a single element. Use the SET L command (SELOGIC control equations) to set an output contact (e.g., OUT101 through OUT107 for Model 0351x1) to the element under test. The available elements are the Relay Word bits referenced in Table 9.3.

Use this method especially for time testing time-overcurrent elements. For example, to test the phase time-overcurrent element 51PT via output contact OUT104, make the following setting:

OUT104 = 51PT

Time-overcurrent curve and time-dial information can be found in *Section 9: Setting the Relay*. Do not forget to reenter the correct relay settings when you are finished testing and ready to place the relay in service.

Testing Via Sequential Events Recorder

You can set the relay to generate an entry in the Sequential Events Recorder (SER) for testing relay elements. Use the SET R command to include the element(s) under test in any of the SER trigger lists (SER1 through SER3). See *Section 12: Standard Event Reports, Sag/Swell/Interruption Report, and SER*.

To test the phase time-overcurrent element 51PT with the SER, make the following setting:

SER1 = 51P 51PT

Element 51P asserts when phase current is above the pickup of the phase time-overcurrent element. Element 51PT asserts when the phase time-overcurrent element times out. The assertion and deassertion of these elements is time-stamped in the SER report. Use this method to verify timing associated with time-overcurrent elements, reclosing relay operation, etc. Do not forget to reenter the correct relay settings when you are ready to place the relay in service.

RELAY SELF-TESTS

The relay runs a variety of self-tests. The relay takes the following corrective actions for out-of-tolerance conditions (see Table 13.1):

- **Protection Disabled:** The relay disables overcurrent elements and trip/close logic. All output contacts are deenergized. The EN front-panel LED is extinguished.
- **ALARM Output:** The ALARM output contact signals an alarm condition by going to its deenergized state. If the ALARM output contact is a B contact (normally closed), it closes for an alarm condition or if the relay is deenergized. If the ALARM output contact is an A contact (normally open), it opens for an alarm condition or if the relay is deenergized. Alarm condition signaling can be a single 5-second pulse (Pulsed) or permanent (Latched).
- The relay generates automatic STATUS reports at the serial port for warnings and failures.
- The relay displays failure messages on the relay LCD display for failures.

Use the serial port STATUS command or front-panel STATUS pushbutton to view relay self-test status.

Table 13.1: Relay Self-Tests

Self-Test	Condition	Limits	Protection Disabled	ALARM Output	Description
IA, IB, IC, IN, VA, VB, VC, VS Offset	Warning	30 mV	No	Pulsed	Measures the dc offset at each of the input channels every 10 seconds.
Master Offset +5 V PS	Warning	20 mV	No	Pulsed	Measures the dc offset at the A/D every 10 seconds.
	Failure	30 mV	Yes	Latched	
	Warning	+4.80 V +5.20 V	No	Pulsed	Measures the +5 V power supply every 10 seconds.
	Failure	+4.65 V +5.40 V	Yes	Latched	
±5 V REG	Warning	±4.75 V +5.20, -5.25 V	No	Pulsed	Measures the regulated 5 V power supply every 10 seconds.
	Failure	±4.50 V +5.40, -5.50 V	Yes	Latched	

Self-Test	Condition	Limits	Protection Disabled	ALARM Output	Description
±12 V PS	Warning	±11.50 V ±12.50 V	No	Pulsed	Measures the 12 V power supply every 10 seconds.
	Failure	±11.20 V ±14.00 V	Yes	Latched	
±15 V PS	Warning	±14.40 V ±15.60 V	No	Pulsed	Measures the 15 V power supply every 10 seconds.
	Failure	±14.00 V ±16.00 V	Yes	Latched	
TEMP	Warning	-40°C +85°C	No		Measures the temperature at the A/D voltage reference every 10 seconds.
	Failure	-50°C +100°C	Yes	Latched	
RAM	Failure		Yes	Latched	Performs a read/write test on system RAM every 60 seconds.
ROM	Failure	checksum	Yes	Latched	Performs a checksum test on the relay program memory every 10 seconds.
A/D	Failure		Yes	Latched	Validates proper number of conversions each 1/4 cycle.
CR_RAM	Failure	checksum	Yes	Latched	Performs a checksum test on the active copy of the relay settings every 10 seconds.
EEPROM	Failure	checksum	Yes	Latched	Performs a checksum test on the nonvolatile copy of the relay settings every 10 seconds.

Self-Test	Condition	Limits	Protection Disabled	ALARM Output	Description
The following self-tests are performed by dedicated circuitry in the microprocessor and the SEL-351 Relay main board. Failures in these tests shut down the microprocessor and are not shown in the STATUS report.					
Micro-processor Crystal	Failure		Yes	Latched	The relay monitors the microprocessor crystal. If the crystal fails, the relay displays "CLOCK STOPPED" on the LCD display. The test runs continuously.
Micro-processor	Failure		Yes	Latched	The microprocessor examines each program instruction, memory access, and interrupt. The relay displays "VECTOR nn" on the LCD upon detection of an invalid instruction, memory access, or spurious interrupt. The test runs continuously.

RELAY TROUBLESHOOTING

Inspection Procedure

Complete the following procedure before disturbing the relay. After you finish the inspection, proceed to the *Troubleshooting Procedure*.

1. Measure and record the power supply voltage at the power input terminals.
2. Check to see that the power is on. Do not turn the relay off.
3. Measure and record the voltage at all control inputs.
4. Measure and record the state of all output relays.

Troubleshooting Procedure

All Front-Panel LEDs Dark

1. Input power not present or fuse is blown.
2. Self-test failure.

Cannot See Characters on Relay LCD Screen

1. Relay is deenergized. Check to see if the ALARM contact is closed.
2. LCD contrast is out of adjustment. Use the steps below to adjust the contrast.
 - a) Remove the relay front panel by removing the six front-panel screws.
 - b) Press any front-panel button. The relay should turn on the LCD back lighting.
 - c) Locate the contrast adjust potentiometer adjacent to the serial port connector.
 - d) Use a small screwdriver to adjust the potentiometer.
 - e) Replace the relay front panel.

Relay Does Not Respond to Commands From Device Connected to Serial Port

1. Communications device not connected to relay.
2. Relay or communications device at incorrect baud rate or other communication parameter incompatibility, including cabling error.
3. Relay serial port has received an XOFF, halting communications. Type <CTRL>Q to send relay an XON and restart communications.

Relay Does Not Respond to Faults

1. Relay improperly set.
2. Improper test source settings.
3. CT or PT input wiring error.
4. Analog input cable between transformer secondary and main board loose or defective.
5. Failed relay self-test.

RELAY CALIBRATION

The SEL-351 Relay is factory-calibrated. If you suspect that the relay is out of calibration, please contact the factory.

FACTORY ASSISTANCE

The employee-owners of Schweitzer Engineering Laboratories are dedicated to making electric power safer, more reliable, and more economical.

We appreciate your interest in SEL products, and we are committed to making sure you are satisfied. If you have any questions, please contact us at:

Schweitzer Engineering Laboratories
2350 NE Hopkins Court
Pullman, WA USA 99163-5603
Tel: (509) 332-1890
Fax: (509) 332-7990

We provide prompt, courteous, and professional service. We appreciate receiving any comments and suggestions about new products or product improvements that would help us make your job easier.

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APPENDIX A: FIRMWARE VERSIONS

DETERMINING THE FIRMWARE VERSION IN YOUR RELAY

To find the firmware revision number in your relay, view the status report using the serial port STATUS command or the front-panel STATUS pushbutton. For firmware versions prior to August 27, 1999, the status report displays the Firmware Identification (FID) label:

FID=SEL-351-x-Rxxx-Vx-Dxxxxxx

For firmware versions with the date code of August 27, 1999, or later, the FID label will appear as follows with the Part/Revision number in bold:

FID=SEL-351-x-Rxxx-Vx-Z001001-Dxxxxxxxx

The firmware revision number is after the “R” and the release date is after the “D”. The single “x” after “SEL-351” is the firmware version number and will be a 5, 6, or 7, depending on the firmware features ordered with the relay:

x = 5	Standard Features
x = 6	Standard Features plus MIRRORRED BITS™ and Load Profile
x = 7	Same as x = 6, plus Power Elements and Voltage Sag/Swell/Interrupt Elements

For example:

FID=SEL-351-5-R303-V0-Z001001-D19990914

is firmware version number 5, firmware revision number 303, release date September 14, 1999.

This manual covers SEL-351 Relays that contain firmware bearing the following part numbers and revision numbers (most recent firmware listed at top):

Firmware Part/Revision No.	Description of Firmware
SEL-351-x-R306-V0-Z003003-D20010307	<p>This firmware differs from the previous versions as follows:</p> <ul style="list-style-type: none"> – Redesigned the Voltage Sag, Swell, Interruption (VSSI) logic and VSSI recorder. – Added Extended Metering MET X command, which includes phase-to-phase voltages. – Added phase-to-phase voltage recording capability to the Load Profile Recorder. – Increased event report storage capacity in 03517 models to match that of 03515 and 03516 models. – Improved front-panel target logic so that correct phase targeting appears when tripping with no intentional delay, most noticeable during testing. – Corrected substation battery monitor DCLO to prevent it from asserting when the relay is powered by ac. – Improved fault locator event type determination during short duration faults, most likely seen during testing. – Added ac mode for optoisolated input debounce timers in global settings IN101D–IN106D, IN201D–IN208D. This allows ac control signals to be sensed on selected inputs. – Added metering quantities and breaker wear monitor data to display points. – Redesigned Maximum/Minimum Metering Logic. – Added support for SEL-5030 ACSELERATOR™
SEL-351-x-R305-V0-Z002002-D20001005	<p>This firmware differs from the previous versions as follows:</p> <ul style="list-style-type: none"> – Internal changes to support Flash memory revision and battery-backed clock hardware change. – Lowered the minimum allowable setting for 27B81P (undervoltage block for frequency elements). – Added SEL-DTA2 compatibility. – A5C0 Relay Definition Block Changed. – Updated ID Message Response (see <i>Appendix D.</i>)
SEL-351-x-R304-V0-Z001001-D20000105	<p>This firmware differs from the previous versions as follows:</p> <ul style="list-style-type: none"> – Target LEDs can no longer be reset if a TRIP condition is present.

Firmware Part/Revision No.	Description of Firmware
SEL-351-x-R303-V0-Z001001-D19990914	<p>This firmware differs from the previous versions as follows:</p> <ul style="list-style-type: none"> – Fixed scaling problems with the directional elements and fault locator associated with the SEL-351-7 Relay (300 V voltage inputs). – Added the MB8A and MB8B serial port protocol settings options for MIRRORED BITS protocol operating on communication channels requiring an eight bit data format. – Expanded the setting range for the SYNC (synchronizing phase) setting to accommodate compensation angle settings for synchronism check. – Changed DNP mapping command so that it now requests a confirmation before saving the map modification.
SEL-351-x-R300-V0-D990621	Original Firmware Release

APPENDIX B: FIRMWARE UPGRADE INSTRUCTIONS

FIRMWARE (FLASH) UPGRADE INSTRUCTIONS

SEL may occasionally offer firmware upgrades to improve the performance of your relay. The SEL-351 Relay stores firmware in Flash memory; therefore, changing physical components is not necessary. A firmware loader program called SELBOOT resides in the SEL-351 Relay. These instructions give a step-by-step procedure to upgrade the relay firmware by downloading a file from a personal computer to the relay via a serial port.

IMPORTANT NOTE REGARDING SETTINGS

The firmware Upgrade Procedure may result in lost relay settings due to the addition of new features and changes in the way memory is used. It is imperative to have a copy of the original relay settings available in case they need to be re-entered. Carefully following these upgrade instructions will minimize the chance of inadvertently losing relay settings.

REQUIRED EQUIPMENT

- Personal computer.
- Terminal emulation software that supports XMODEM/CRC protocol (e.g., Procomm[®] Plus, Relay Gold[™], Microsoft Windows[®] Terminal[™], Microsoft Windows[®] HyperTerminal[™], SmartCOM[™], or CROSSTALK[®]).
- Serial communications cable (SEL-234A or equivalent).
- Disk containing firmware upgrade file.

UPGRADE PROCEDURE

The instructions below assume you have a working knowledge of your personal computer terminal emulation software. In particular, you must be able to modify your serial communications parameters (baud rate, data bits, parity, etc.), disable any hardware or software flow control in your computer terminal emulation software, select transfer protocol (i.e., XMODEM/CRC), and transfer files (e.g., send and receive binary files).

1. If the relay is in service, disable its control functions.

Note: If the SEL-351 Relay contains History (HIS) data, Event (EVE) data, Metering (MET) data, Sequential Events Recorder (SER) data, Load Profile (LDP) data, Sag/Swell/Interruption (SSI) reports, or Breaker Wear Monitor (BRE) data that you want to retain, it must be retrieved prior to performing the firmware upgrade, because all of these data sets may be erased in the upgrade procedure.

2. Connect the personal computer to the relay serial port 2, 3, or F, and enter Access Level 2 by issuing the ACC and 2AC commands. (Disconnect any other serial port connections.)

3. Execute the Show Calibration (**SHO C**) command to retrieve the relay calibration settings. Record the displayed settings (or save them to a computer file) for possible reentry after the firmware upgrade.

If you do not already have copies of the Global, Group, Logic, Port, SER, and Text label settings, use the following Show commands to retrieve the necessary settings: **SHO G**, **SHO 1**, **SHO L 1**, **SHO 2**, **SHO L 2**, **SHO 3**, **SHO L 3**, **SHO 4**, **SHO L 4**, **SHO 5**, **SHO L 5**, **SHO 6**, **SHO L 6**, **SHO P 1**, **SHO P 2**, **SHO P 3**, **SHO P F**, **SHO R**, and **SHO T**. (The SEL-5030 software makes saving the settings easier.)

Issue the Password (**PAS**) command and save the original password settings in case they are needed later.

Normally, the relay will preserve the settings during the firmware upgrade. However, depending on the firmware version that was previously installed and the use of relay memory, this cannot be ensured. Saving settings is always recommended.

4. Set up your communication connection to the highest possible baud rate. The relay will support speeds up to 38,400 baud. Use the **SET P** command to change the **SPEED** setting to the desired baud rate.
5. Issue the **L_D <ENTER>** command to the relay (L underscore D ENTER) to start the SELBOOT program.
6. Type **Y <ENTER>** to the “Disable relay to send or receive firmware (Y/N)?” prompt and **Y <ENTER>** to the “Are you sure (Y/N)?” prompt. The relay will send the SELBOOT prompt **!>**.

Note: SELBOOT does not echo nonalphanumeric characters as the first character of a line. This may make it appear that the relay is not functioning properly when just the **<ENTER>** key is pressed on the connected PC, even though everything is OK.

7. Make a copy of the firmware currently in the relay. This is recommended in case the new firmware download is unsuccessful. To make a backup of the firmware, you will need approximately 2.3 MB of free disk space. The procedure takes approximately 11 minutes at 38,400 baud.

Issue the Send (**SEN <ENTER>**) command to the relay to initiate the firmware transfer from the relay to your computer. No activity will be seen on the PC screen, because the relay is waiting for the PC to request the first XMODEM data packet. Select the “Receive File” function with the XMODEM protocol in your terminal emulation software. Give the file a unique name to clearly identify the firmware version (e.g., 351_R200.S19). After the transfer, the relay will respond: “Download completed successfully!”

8. Begin the transfer of the new firmware to the relay by issuing the Receive (**REC <ENTER>**) command to instruct the relay to receive new firmware.

Note: If the relay power fails during a firmware receive after the old firmware is erased, the relay will restart in SELBOOT, but the baud rate will default to 2400 baud. (If this happens, connect to the relay at 2400 baud and type **BAUD 38400** at the SELBOOT prompt. The firmware receive can be started again at step 8.)

9. The relay will ask if you are sure you want to erase the existing firmware. Type **Y** to erase the existing firmware and load new firmware, or just **<ENTER>** to abort.
10. The relay then prompts you to press a key and begin the transfer. Press a key (e.g., **<ENTER>**).

Note: The relay will display one or more “C” characters as it waits for your PC Terminal Emulation program to send the new firmware. If you do not start the transfer quickly enough (within about 18 seconds), it may time out and respond “Remote system is not responding.” If this happens, begin again in step 8, above.

11. Start the file transfer by selecting the “Send File” function in your terminal emulation software. Use the XMODEM or 1k-XMODEM (fastest) protocol and send the file that contains the new firmware (e.g., Relay.S19).

Note: The file transfer takes approximately 6 minutes at 38,400 baud using the 1k-XMODEM protocol. After the transfer completes, the relay will reboot and return to Access Level 0. The following screen capture shows the entire process.

```

->>L_D <ENTER>
Disable relay to send or receive firmware(Y/N) ? Y <ENTER>
Are you sure (Y/N) ? Y <ENTER>
Relay Disabled
!>SEN <ENTER>
Download completed successfully!

!>REC <ENTER>
Caution! - This command erases the relay's firmware.
If you erase the firmware, new firmware must be loaded into the relay
before it can be put back into service.

Are you sure you wish to erase the existing firmware? (Y/N)Y
Erasing
Erase successful
Press any key to begin transfer, then start transfer at the PC <ENTER>

Upload completed successfully. Attempting a restart

```

12. The relay illuminates the EN front-panel LED if the original relay settings were retained through the download. If the EN LED is illuminated, proceed to Step 13; otherwise, the relay may display various self-test failures because of changes in the way memory is used.

If this occurs, press **<ENTER>** to see if the level 0 prompt “ = ” appears on your terminal screen. If it does, enter Access Level 2 by issuing the **ACC** and **2AC** commands and proceed to self-test failure: **IO_BRD**, Step 12a.

If the relay does not display the level 0 “ = ” prompt, the Relay baud rate has changed back to the factory default of 2400 baud; go to self-test failure: **CR_RAM**, **EEPROM**, and **IO_BRD**, Step 12d.

Self-test failure: **IO_BRD**

- a. Issue the Initialize (**INI**) command to reinitialize the I/O board(s). If this command is not available, go to Step 12e.
- b. Answer **Y** <ENTER> to the question: “Are the new I/O board(s) correct (Y/N)” After about one minute, the EN LED will illuminate. The original relay settings have been retained, but should be checked for accuracy.
- c. Enter Access Level 2 by issuing the **ACC** and **2AC** commands. Go to Step 13.

Self-test failure: **CR_RAM, EEPROM, and IO_BRD**

- d. Set your communications software settings to 2400 baud, 8 data bits, 1 stop bit. Now enter Access Level 2 by issuing the **ACC** and **2AC** commands (the factory default passwords will be in effect).
- e. Issue the Restore Settings (**R_S**) command to restore the factory default settings in the relay. This takes about two minutes, then the EN LED will illuminate.

Note: If the relay asks for a part number to be entered, use the number from the label on the firmware diskette, or from the new part number sticker (if supplied).

- f. Enter Access Level 2 by issuing the **ACC** and **2AC** commands, (the factory default passwords will be in effect).
- g. Restore the original settings as necessary with each of the following commands: **SET G, SET 1, SET L 1, SET 2, SET L 2, SET 3, SET L 3, SET 4, SET L 4, SET 5, SET L 5, SET 6, SET L 6, SET P 1, SET P 2, SET P 3, SET P F, SET R** and **SET T**.
- h. Set the original relay passwords saved in Step 3 via the **PAS** command.

For example, **PAS 1:APPLE** <ENTER> sets the level 1 password to APPLE. Use a similar format for **PAS B** and **PAS 2**. The **PAS** command is case-sensitive, so the lower and upper-case letters are treated differently.

If there are still any FAIL codes on the Relay LCD, see *Section 13: Testing and Troubleshooting*.

13. Verify the calibration settings by issuing the **SHO C** command. If the settings do not match the settings recorded in Step 3, reissue the settings with the **SET C** command.
14. Issue the Version command (**VER** <ENTER>) and check the part number from the label on the firmware diskette against the part number on the screen. If they match, go to Step 15; otherwise, type **PAR** <ENTER> and type the number from the diskette label and press <ENTER>. If the relay re-initializes after saving the changes, go to Access Level 2.
15. Execute the Status (**STA**) command to verify that all relay self-test parameters are within tolerance, and that the relay is enabled.

16. If the Breaker Wear Monitor was being used, check the date using the BRE command to see if the breaker wear data were retained through the upgrade procedure. If the data were not retained, use the BRE W command to reload the values saved in step 1.
17. Apply current and voltage signals to the relay. Issue the **MET** command; verify that the current and voltage signals are correct. Issue the Trigger (**TRI**) and Event (**EVE**) commands. Verify that the current and voltage signals are correct in the event report.

The relay is now ready for your commissioning procedure.

APPENDIX C: SEL DISTRIBUTED PORT SWITCH PROTOCOL

SEL Distributed Port Switch Protocol (LMD) permits multiple SEL relays to share a common communications channel. It is appropriate for low-cost, low-speed port switching applications where updating a real-time database is not a requirement.

SETTINGS

Use the front-panel SET pushbutton or the serial port SET P command to activate the LMD protocol. Change the port PROTO setting from the default SEL to LMD to reveal the following settings:

- PREFIX:** One character to precede the address. This should be a character that does not occur in the course of other communications with the relay. Valid choices are one of the following: “@”, “#”, “\$”, “%”, “&”. The default is “@”.
- ADDR:** Two-character ASCII address. The range is “01” to “99”. The default is “01”.
- SETTLE:** Time in seconds that transmission is delayed after the request to send (RTS line) asserts. This delay accommodates transmitters with a slow rise time.

OPERATION

1. The relay ignores all input from this port until it detects the prefix character and the two-byte address.
2. Upon receipt of the prefix and address, the relay enables echo and message transmission.
3. Wait until you receive a prompt before entering commands to avoid losing echoed characters while the external transmitter is warming up.
4. Until the relay connection terminates, you can use the standard commands that are available when PROTO is set to SEL.
5. The QUIT command terminates the connection. If no data are sent to the relay before the port timeup period, it automatically terminates the connection.
6. Enter the sequence CTRL-X QUIT <CR> before entering the prefix character if all relays in the multidrop network do not have the same prefix setting.

Note: You can use the front-panel SET pushbutton to change the port settings to return to SEL protocol.

APPENDIX D: CONFIGURATION, *FAST METER*, AND *FAST OPERATE* COMMANDS

INTRODUCTION

SEL relays have two separate data streams that share the same serial port. The human data communications with the relay consist of ASCII character commands and reports that are intelligible to humans using a terminal or terminal emulation package. The binary data streams can interrupt the ASCII data stream to obtain information and then allow the ASCII data stream to continue. This mechanism allows a single communications channel to be used for ASCII communications (e.g., transmission of a long event report) interleaved with short bursts of binary data to support fast acquisition of metering data. The device connected to the other end of the link requires software that uses the separate data streams to exploit this feature. The binary commands and ASCII commands can also be accessed by a device that does not interleave the data streams.

SEL Application Guide AG95-10, *Configuration and Fast Meter Messages*, is a comprehensive description of the SEL binary messages. Below is a description of the messages provided in the SEL-351 Relay.

MESSAGE LISTS

Binary Message List

<u>Request to Relay (hex)</u>	<u>Response From Relay</u>
A5C0	Relay Definition Block
A5C1	<i>Fast Meter</i> Configuration Block
A5D1	<i>Fast Meter</i> Data Block
A5C2	Demand <i>Fast Meter</i> Configuration Block
A5D2	Demand <i>Fast Meter</i> Data Message
A5C3	Peak Demand <i>Fast Meter</i> Configuration Block
A5D3	Peak Demand <i>Fast Meter</i> Data Message
A5B9	<i>Fast Meter</i> Status Acknowledge
A5CE	<i>Fast Operate</i> Configuration Block
A5E0	<i>Fast Operate</i> Remote Bit Control
A5E3	<i>Fast Operate</i> Breaker Control

ASCII Configuration Message List

<u>Request to Relay (ASCII)</u>	<u>Response From Relay</u>
ID	ASCII Firmware ID String and Terminal ID Setting (TID)
DNA	ASCII Names of Relay Word bits
BNA	ASCII Names of bits in the A5B9 Status Byte

MESSAGE DEFINITIONS

A5C0 Relay Definition Block

In response to the A5C0 request, the relay sends the following block:

<u>Data</u>	<u>Description</u>
A5C0	Command
44	Message length (74)
04	Support four protocols: SEL, MIRRORED BITS, DNP, and LMD.
03	Support <i>Fast Meter</i> , fast demand, and fast peak
05	Status flag for Warn, Fail, Group, or Settings change
A5C1	<i>Fast Meter</i> configuration
A5D1	<i>Fast Meter</i> message
A5C2	Fast demand configuration
A5D2	Fast demand message
A5C3	Fast peak configuration
A5D3	Fast peak message
0002	Self-test warning bit
5354410D0000(STA<CR>)	Check status
0003	Self-test failure bit
5354410D0000(STA<CR>)	Check status
0004	Settings change bit
A5C100000000	Reconfigure <i>Fast Meter</i> on settings change
0004	Settings change bit
53484F0D0000(SHO<CR>)	Check the settings
0004	Settings change bit
53484F20470D(SHO G<CR>)	Check the group settings
0300	SEL protocol with <i>Fast Operate</i> and fast message (unsolicited SER messaging)
0301	LMD protocol with <i>Fast Operate</i> and fast message (unsolicited SER messaging)
0005	DNP 3.00
0006	MIRRORED BITS protocol, no <i>Fast Operate</i>
00	Reserved
xx	Checksum

A5C1 Fast Meter Configuration Block

In response to the A5C1 request, relay models 0351x0, 0351x1 and 0351xY send the following block:

<u>Data</u>	<u>Description</u>
A5C1	<i>Fast Meter</i> command
84	Length
01	One status flag byte
00	Scale factors in <i>Fast Meter</i> message
00	No scale factors
0A	# of analog input channels
02	# of samples per channel

39	# of digital banks
01	One calculation block
0004	Analog channel offset
0054	Time stamp offset
005C	Digital offset
494100000000	Analog channel name (IA)
01	Analog channel type
FF	Scale factor type
0000	Scale factor offset in <i>Fast Meter</i> message
494200000000	Analog channel name (IB)
01	Analog channel type
FF	Scale factor type
0000	Scale factor offset in <i>Fast Meter</i> message
494300000000	Analog channel name (IC)
01	Analog channel type
FF	Scale factor type
0000	Scale factor offset in <i>Fast Meter</i> message
494E00000000	Analog channel name (IN)
01	Analog channel type
FF	Scale factor type
0000	Scale factor offset in <i>Fast Meter</i> message
564100000000	Analog channel name (VA)
01	Analog channel type
FF	Scale factor type
0000	Scale factor offset in <i>Fast Meter</i> message
564200000000	Analog channel name (VB)
01	Analog channel type
FF	Scale factor type
0000	Scale factor offset in <i>Fast Meter</i> message
564300000000	Analog channel name (VC)
01	Analog channel type
FF	Scale factor type
0000	Scale factor offset in <i>Fast Meter</i> message
565300000000	Analog channel name (VS)
01	Analog channel type
FF	Scale factor type
0000	Scale factor offset in <i>Fast Meter</i> message
465245510000	Analog channel name (FREQ)
01	Analog channel type
FF	Scale factor type
0000	Scale factor offset in <i>Fast Meter</i> message
564241540000	Analog channel name (VBAT)
01	Analog channel type
FF	Scale factor type
0000	Scale factor offset in <i>Fast Meter</i> message
00	Line Configuration (0-ABC, 1-ACB)
00	Standard Power Calculations
FFFF	No Deskew angle
FFFF	No Rs compensation (-1)
FFFF	No Xs compensation (-1)
00	IA channel index

01	IB channel index
02	IC channel index
04	VA channel index
05	VB channel index
06	VC channel index
00	Reserved
checksum	1-byte checksum of all preceding bytes

A5D1 Fast Meter Data Block

In response to the A5D1 request, relay models 0351x0, 0351x1 and 0351xY, Firmware Version ?, send the following block:

<u>Data</u>	<u>Description</u>
A5D1	Command
98	Length
1 byte	1 Status Byte
80 bytes	X and Y components of: IA, IB, IC, IN, VA, VB, VC, VS, Freq and Vbatt in 4-byte IEEE FPS
8 bytes	Time stamp
57 bytes	57 Digital banks: TAR0–TAR56
1 byte	Reserved
checksum	1-byte checksum of all preceding bytes

A5C2/A5C3 Demand/Peak Demand Fast Meter Configuration Messages

In response to the A5C2 or A5C3 request, the relay sends the following block:

<u>Data</u>	<u>Description</u>
A5C2 or A5C3	Command; Demand (A5C2) or Peak Demand (A5C3)
EE	Length
01	# of status flag bytes
00	Scale factors in meter message
00	# of scale factors
16	# of analog input channels
01	# of samples per channel
00	# of digital banks
00	# of calculation blocks
0004	Analog channel offset
00B4	Time stamp offset
FFFF	Digital offset
494100000000	Analog channel name (IA)
02	Analog channel type
FF	Scale factor type
0000	Scale factor offset in <i>Fast Meter</i> message
494200000000	Analog channel name (IB)
02	Analog channel type
FF	Scale factor type
0000	Scale factor offset in <i>Fast Meter</i> message
494300000000	Analog channel name (IC)

02	Analog channel type
FF	Scale factor type
0000	Scale factor offset in <i>Fast Meter</i> message
494E00000000	Analog channel name (IN)
02	Analog channel type
FF	Scale factor type
0000	Scale factor offset in <i>Fast Meter</i> message
494700000000	Analog channel name (IG)
02	Analog channel type
FF	Scale factor type
0000	Scale factor offset in <i>Fast Meter</i> message
334932000000	Analog channel name (3I2)
02	Analog channel type
FF	Scale factor type
0000	Scale factor offset in <i>Fast Meter</i> message
50412B000000	Analog channel name (PA+)
02	Analog channel type
FF	Scale factor type
0000	Scale factor offset in <i>Fast Meter</i> message
50422B000000	Analog channel name (PB+)
02	Analog channel type
FF	Scale factor type
0000	Scale factor offset in <i>Fast Meter</i> message
50432B000000	Analog channel name (PC+)
02	Analog channel type
FF	Scale factor type
0000	Scale factor offset in <i>Fast Meter</i> message
50332B000000	Analog channel name (P3+)
02	Analog channel type
FF	Scale factor type
0000	Scale factor offset in <i>Fast Meter</i> message
51412B000000	Analog channel name (QA+)
02	Analog channel type
FF	Scale factor type
0000	Scale factor offset in <i>Fast Meter</i> message
51422B000000	Analog channel name (QB+)
02	Analog channel type
FF	Scale factor type
0000	Scale factor offset in <i>Fast Meter</i> message
51432B000000	Analog channel name (QC+)
02	Analog channel type
FF	Scale factor type
0000	Scale factor offset in <i>Fast Meter</i> message
51332B000000	Analog channel name (Q3+)
02	Analog channel type
FF	Scale factor type
0000	Scale factor offset in <i>Fast Meter</i> message
50412D000000	Analog channel name (PA-)
02	Analog channel type
FF	Scale factor type
0000	Scale factor offset in <i>Fast Meter</i> message

50422D000000	Analog channel name (PB-)
02	Analog channel type
FF	Scale factor type
0000	Scale factor offset in <i>Fast Meter</i> message
50432D000000	Analog channel name (PC-)
02	Analog channel type
FF	Scale factor type
0000	Scale factor offset in <i>Fast Meter</i> message
50332D000000	Analog channel name (P3-)
02	Analog channel type
FF	Scale factor type
0000	Scale factor offset in <i>Fast Meter</i> message
51412D000000	Analog channel name (QA-)
02	Analog channel type
FF	Scale factor type
0000	Scale factor offset in <i>Fast Meter</i> message
51422D000000	Analog channel name (QB-)
02	Analog channel type
FF	Scale factor type
0000	Scale factor offset in <i>Fast Meter</i> message
51432D000000	Analog channel name (QC-)
02	Analog channel type
FF	Scale factor type
0000	Scale factor offset in <i>Fast Meter</i> message
51332D000000	Analog channel name (Q3-)
02	Analog channel type
FF	Scale factor type
0000	Scale factor offset in <i>Fast Meter</i> message
00	Reserved
checksum	1-byte checksum of preceding bytes

A5D2/A5D3 Demand/Peak Demand *Fast Meter* Message

In response to the A5D2 or A5D3 request, the relay sends the following block:

A5D2 or A5D3	Command
BE	Length
1 byte	1 Status Byte
176-bytes	Demand: IA, IB, IC, IN, IG, 3I2, MWA I, MWB I, MWC I, MW3PI, MVA I, MVB I, MVC I, MV3PI, MWA O, MWB O, MWC O, MW3PO, MVA O, MVB O, MVC O, MV3PO in 8-byte IEEE FPS
8 bytes	Time stamp
1 byte	Reserved
1 byte	1-byte checksum of all preceding bytes

A5B9 Fast Meter Status Acknowledge Message

In response to the A5B9 request, the relay clears the *Fast Meter* (message A5D1) Status Byte. The SEL-351 Status Byte contains one active bit, STSET (bit 4). The bit is set on power up and on settings changes. If the STSET bit is set, the external device should request the A5C1, A5C2, and A5C3 messages. The external device can then determine if the scale factors or line configuration parameters have been modified.

A5CE Fast Operate Configuration Block

In response to the A5CE request, the relay sends the following block:

<u>Data</u>	<u>Description</u>
A5CE	Command
3C	Length
01	Support 1 circuit breaker
0010	Support 16 remote bit set/clear commands
0100	Allow remote bit pulse commands
31	Operate code, open breaker 1
11	Operate code, close breaker 1
00	Operate code, clear remote bit RB1
20	Operate code, set remote bit RB1
40	Operate code, pulse remote bit RB1
01	Operate code, clear remote bit RB2
21	Operate code, set remote bit RB2
41	Operate code, pulse remote bit RB2
02	Operate code, clear remote bit RB3
22	Operate code, set remote bit RB3
42	Operate code, pulse remote bit RB3
03	Operate code, clear remote bit RB4
23	Operate code, set remote bit RB4
43	Operate code, pulse remote bit RB4
04	Operate code, clear remote bit RB5
24	Operate code, set remote bit RB5
44	Operate code, pulse remote bit RB5
05	Operate code, clear remote bit RB6
25	Operate code, set remote bit RB6
45	Operate code, pulse remote bit RB6
06	Operate code, clear remote bit RB7
26	Operate code, set remote bit RB7
46	Operate code, pulse remote bit RB7
07	Operate code, clear remote bit RB8
27	Operate code, set remote bit RB8
47	Operate code, pulse remote bit RB8
08	Operate code, clear remote bit RB9
28	Operate code, set remote bit RB9
48	Operate code, pulse remote bit RB9
09	Operate code, clear remote bit RB10
29	Operate code, set remote bit RB10
49	Operate code, pulse remote bit RB10
0A	Operate code, clear remote bit RB11

2A	Operate code, set remote bit RB11
4A	Operate code, pulse remote bit RB11
0B	Operate code, clear remote bit RB12
2B	Operate code, set remote bit RB12
4B	Operate code, pulse remote bit RB12
0C	Operate code, clear remote bit RB13
2C	Operate code, set remote bit RB13
4C	Operate code, pulse remote bit RB13
0D	Operate code, clear remote bit RB14
2D	Operate code, set remote bit RB14
4D	Operate code, pulse remote bit RB14
0E	Operate code, clear remote bit RB15
2E	Operate code, set remote bit RB15
4E	Operate code, pulse remote bit RB15
0F	Operate code, clear remote bit RB16
2F	Operate code, set remote bit RB16
4F	Operate code, pulse remote bit RB16
00	Reserved
checksum	1-byte checksum of all preceding bytes

A5E0 Fast Operate Remote Bit Control

The external device sends the following message to perform a remote bit operation:

<u>Data</u>	<u>Description</u>
A5E0	Command
06	Length
1 byte	Operate code: 00–0F clear remote bit RB1–RB16 20–2F set remote bit RB1–RB16 40–4F pulse remote bit for RB1–RB16 for one processing interval
1 byte	Operate validation: $4 \cdot \text{Operate code} + 1$
checksum	1-byte checksum of preceding bytes

The relay performs the specified remote bit operation if the following conditions are true:

1. The Operate code is valid.
2. The Operate validation = $4 \cdot \text{Operate code} + 1$.
3. The message checksum is valid.
4. The FASTOP port setting is set to Y.
5. The relay is enabled.

Remote bit set and clear operations are latched by the relay. Remote bit pulse operations assert the remote bit for one processing interval (1/4 cycle).

It is common practice to route remote bits to output contacts to provide remote control of the relay outputs. If you wish to pulse an output contact closed for a specific duration, SEL recommends using the remote bit pulse command and SELOGIC[®] control equations to provide secure and accurate contact control. The remote device sends the remote bit pulse command; the relay controls the timing of the output contact assertion. You can use any remote bit (RB1 through RB16), and any SELOGIC control equation timer (SV1 through SV16) to control

any of the output contacts (OUT101 through OUT107). For example, to pulse output contact OUT104 for 30 cycles with Remote Bit RB4 and SELOGIC control equation timer SV4, issue the following relay settings:

via the SET L command,

SV4 = RB4

SV4 input is RB4

OUT104 = SV4T

route SV4 timer output to OUT104

via the SET command,

SV4PU = 0

SV4 pickup time = 0

SV4DO = 30

SV4 dropout time is 30 cycles

To pulse the contact, send the A5E006430DDB command to the relay.

A5E3 Fast Operate Breaker Control

The external device sends the following message to perform a fast breaker open/close:

<u>Data</u>	<u>Description</u>
A5E3	Command
06	Length
1 byte	Operate code: 31—OPEN breaker 11—CLOSE breaker
1 byte	Operate Validation: $4 \cdot \text{Operate code} + 1$
checksum	1-byte checksum of preceding bytes

The relay performs the specified breaker operation if the following conditions are true:

1. Conditions 1–5 defined in the A5E0 message are true.
2. The breaker jumper (JMP2B) is in place on the SEL-351 Relay main board.

A5CD Fast Operate Reset Definition Block

In response to an A5CD request, the relay sends the configuration block for the *Fast Operate* Reset message

<u>Data</u>	<u>Description</u>
A5CD	Command
0E	Message length
01	The number of <i>Fast Operate</i> reset codes supported
00	Reserved for future use
	Per <i>Fast Operate</i> reset code, repeat:
00	<i>Fast Operate</i> reset code (e.g., “00” for target reset)
54415220520000	<i>Fast Operate</i> reset description string (e.g., “TAR R”)
xx	Checksum

A5ED Fast Operate Reset Command

The *Fast Operate* Reset commands take the following form:

<u>Data</u>	<u>Description</u>
A5ED	Command
06	Message Length—always 6
00	Operate Code (e.g., “00” for target reset, “TAR R”)
01	Operate Validation—(4 + Operate Code) + 1
xx	Checksum

ID Message

In response to the ID command, the relay sends the firmware ID (FID), boot firmware ID (BFID), firmware checksum (CID), relay TID setting (DEVID), Modbus device code (DEVCODE)—for use by SEL-2020 and SEL-230 Communications Processors, relay part number (PARTNO), and configuration string (CONIG)—for use by other IEDs or software. A sample response is shown below; responses will differ depending on relay model, settings, and firmware.

```
<STX>"FID=SEL-351-x-R305-V0-Z002002-D20000925","yyyy"<CR>
"BFID= SELBOOT-311-R102","yyyy"<CR><LF>
"CID=xxxx","yyyy"<CR><LF>
"DEVID=STATION A","yyyy"<CR><LF>
"DEVCODE=30","yyyy"<CR><LF>
"PARTNO=035170H4554XXX","yyyy"<CR><LF>
"CONFIG=111122","yyyy"<CR><LF><ETX>
```

where <STX> is the STX character (02)
<ETX> is the ETX character (03)
xxxx is the 4-byte ASCII hex representation of the checksum of the relay firmware
yyyy is the 4-byte ASCII hex representation of the checksum for each line.

The ID message is available from Access Level 0 and higher.

DNA Message

In response to the DNA command, the relay sends names of the Relay Word bits transmitted in the A5D1 message. The first name is associated with the MSB, the last name with the LSB. These names are listed in the Relay Word Bits table for the appropriate model in *Section 9* of this manual. The DNA command is available from Access Level 1 and higher.

The DNA message for relay model 0351x0, 0351x1, or 0351xY Firmware Version 7, is:

```
<STX>
"EN","TRIP","INST","COMM","SOTF","50","51","81","yyyy"<CR><LF>
"A","B","C","G","N","RS","CY","LO","yyyy"<CR><LF>
"50A1","50B1","50C1","50A2","50B2","50C2","50A3","50B3","yyyy"<CR><LF>
"50C3","50A4","50B4","50C4","50AB1","50BC1","50CA1","50AB2","yyyy"<CR><LF>
"50BC2","50CA2","50AB3","50BC3","50CA3","50AB4","50BC4","50CA4","yyyy"<CR><LF>
"50A","50B","50C","51A","51AT","51AR","51B","51BT","yyyy"<CR><LF>
"51BR","51C","51CT","51CR","51P","51PT","51PR","51N","yyyy"<CR><LF>
"51NT","51NR","51G","51GT","51GR","51Q","51QT","51QR","yyyy"<CR><LF>
```

"50P1","50P2","50P3","50P4","50N1","50N2","50N3","50N4","yyyy"<CR><LF>
 "67P1","67P2","67P3","67P4","67N1","67N2","67N3","67N4","yyyy"<CR><LF>
 "67P1T","67P2T","67P3T","67P4T","67N1T","67N2T","67N3T","67N4T","yyyy"<CR><LF>
 "50G1","50G2","50G3","50G4","50Q1","50Q2","50Q3","50Q4","yyyy"<CR><LF>
 "67G1","67G2","67G3","67G4","67Q1","67Q2","67Q3","67Q4","yyyy"<CR><LF>
 "67G1T","67G2T","67G3T","67G4T","67Q1T","67Q2T","67Q3T","67Q4T","yyyy"<CR><LF>
 "50P5","50P6","50N5","50N6","50G5","50G6","50Q5","50Q6","yyyy"<CR><LF>
 "50QF","50QR","50GF","50GR","32VE","32QGE","32IE","32QE","yyyy"<CR><LF>
 "F32P","R32P","F32Q","R32Q","F32QG","R32QG","F32V","R32V","yyyy"<CR><LF>
 "F32I","R32I","32PF","32PR","32QF","32QR","32GF","32GR","yyyy"<CR><LF>
 "27A1","27B1","27C1","27A2","27B2","27C2","59A1","59B1","yyyy"<CR><LF>
 "59C1","59A2","59B2","59C2","27AB","27BC","27CA","59AB","yyyy"<CR><LF>
 "59BC","59CA","59N1","59N2","59Q","59V1","27S","59S1","yyyy"<CR><LF>
 "59S2","59VP","59VS","SF","25A1","25A2","3P27","3P59","yyyy"<CR><LF>
 "81D1","81D2","81D3","81D4","81D5","81D6","27B81","50L","yyyy"<CR><LF>
 "81D1T","81D2T","81D3T","81D4T","81D5T","81D6T","VPOLV","LOP","yyyy"<CR><LF>
 "*",*","IN106","IN105","IN104","IN103","IN102","IN101","yyyy"<CR><LF>
 "LB1","LB2","LB3","LB4","LB5","LB6","LB7","LB8","yyyy"<CR><LF>
 "LB9","LB10","LB11","LB12","LB13","LB14","LB15","LB16","yyyy"<CR><LF>
 "RB1","RB2","RB3","RB4","RB5","RB6","RB7","RB8","yyyy"<CR><LF>
 "RB9","RB10","RB11","RB12","RB13","RB14","RB15","RB16","yyyy"<CR><LF>
 "LT1","LT2","LT3","LT4","LT5","LT6","LT7","LT8","yyyy"<CR><LF>
 "LT9","LT10","LT11","LT12","LT13","LT14","LT15","LT16","yyyy"<CR><LF>
 "SV1","SV2","SV3","SV4","SV1T","SV2T","SV3T","SV4T","yyyy"<CR><LF>
 "SV5","SV6","SV7","SV8","SV5T","SV6T","SV7T","SV8T","yyyy"<CR><LF>
 "SV9","SV10","SV11","SV12","SV9T","SV10T","SV11T","SV12T","yyyy"<CR><LF>
 "SV13","SV14","SV15","SV16","SV13T","SV14T","SV15T","SV16T","yyyy"<CR><LF>
 "79RS","79CY","79LO","SH0","SH1","SH2","SH3","SH4","yyyy"<CR><LF>
 "CLOSE","CF","RCSF","OPTMN","RSTMN","FSA","FSB","FSC","yyyy"<CR><LF>
 "BCW","50P32","*","59VA","TRGTR","52A","*","*","yyyy"<CR><LF>
 "SG1","SG2","SG3","SG4","SG5","SG6","ZLOUT","ZLIN","yyyy"<CR><LF>
 "ZLOAD","BCWA","BCWB","BCWC","*","*","*","*","yyyy"<CR><LF>
 "ALARM","OUT107","OUT106","OUT105","OUT104","OUT103","OUT102","OUT101","yyyy"
 <CR><LF>
 "3PO","SOTFE","Z3RB","KEY","EKEY","ECTT","WFC","PT","yyyy"<CR><LF>
 "PTRX2","PTRX","PTRX1","UBB1","UBB2","UBB","Z3XT","DSTRT","yyyy"<CR><LF>
 "NSTRT","STOP","BTX","TRIP","OC","CC","DCHI","DCLO","yyyy"<CR><LF>
 "67P2S","67N2S","67G2S","67Q2S","PDEM","NDEM","GDEM","QDEM","yyyy"<CR><LF>
 "OUT201","OUT202","OUT203","OUT204","OUT205","OUT206","OUT207","OUT208","yyyy"
 <CR><LF>
 "OUT209","OUT210","OUT211","OUT212","*","*","*","*","yyyy"<CR><LF>
 "IN208","IN207","IN206","IN205","IN204","IN203","IN202","IN201","yyyy"<CR><LF>
 "*",*","*","*","*","*","*","*","yyyy"<CR><LF>
 "RMB8A","RMB7A","RMB6A","RMB5A","RMB4A","RMB3A","RMB2A","RMB1A","yyyy"
 <CR><LF>
 "TMB8A","TMB7A","TMB6A","TMB5A","TMB4A","TMB3A","TMB2A","TMB1A","yyyy"
 <CR><LF>
 "RMB8B","RMB7B","RMB6B","RMB5B","RMB4B","RMB3B","RMB2B","RMB1B","yyyy"
 <CR><LF>
 "TMB8B","TMB7B","TMB6B","TMB5B","TMB4B","TMB3B","TMB2B","TMB1B","yyyy"
 <CR><LF>

```
"LBOKB","CBADB","RBADB","ROKB","LBOKA","CBADA","RBADA","ROKA","yyyy"
<CR><LF>
"PWRA1","PWRB1","PWRC1","PWRA2","PWRB2","PWRC2","INTC","INT3P","yyyy"<CR><LF>
"PWRA3","PWRB3","PWRC3","PWRA4","PWRB4","PWRC4","INTA","INTB","yyyy"<CR><LF>
"SAGA","SAGB","SAGC","SAG3P","SWA","SWB","SWC","SW3P","yyyy"<CR><LF>
<ETX>
```

where <STX> is the STX character (02).
 <ETX> is the ETX character (03).
 the last field in each line (yyyy) is the 4-byte ASCII hex representation of the checksum for the line.
 "*" indicates an unused bit location.

Messages for other relay models may be derived from the appropriate tables in *Section 9* of this manual, using the above format.

BNA Message

In response to the BNA command, the relay sends names of the bits transmitted in the Status Byte in the A5D1 message. The first name is the MSB, the last name is the LSB. The BNA message is:

```
<STX>"*","*","*","STSET","*","*","*","*","yyyy"<CR><LF><ETX>
```

where: "yyyy" is the 4-byte ASCII representation of the checksum.
 "*" indicates an unused bit location.

The BNA command is available from Access Level 1 and higher.

SNS Message

In response to the SNS command, the relay sends the name string of the SER(SER1 SER2 SER3) settings. SNS command is available at Access Level 1.

The relay responds to the SNS command with the name string in the SER settings. The name string starts with SER1, followed by SER2 and SER3.

For example: If SER1 = 50A1 OUT101; SER2 = 67P1T 81D1T; SER3 = OUT102 52A; the name string will be "50A1","OUT101","67P1T","81D1T","OUT102","52A".

If there are more than eight settings in SER, the SNS message will have several rows. Each row will have eight strings, followed by the checksum and carriage return. The last row may have less than eight strings.

SNS message for the SEL-351 is:

```
<STX>"xxxx","xxxx","xxxx","xxxx","xxxx","xxxx","xxxx","xxxx","yyyy"<CR><LF>
"xxxx","xxxx","xxxx","xxxx","xxxx","xxxx","xxxx","xxxx","yyyy"<CR><LF>
"xxxx","xxxx","xxxx", <CR><LF><ETX>
```

where: xxxx is a string from the settings in SER (SER1, SER2 and SER3)

yyyy is the 4-byte ASCII representation of the checksum.

APPENDIX E: COMPRESSED ASCII COMMANDS

INTRODUCTION

The SEL-351 Relay provides compressed ASCII versions of some of the relay's ASCII commands. The compressed ASCII commands allow an external device to obtain data from the relay, in a format which directly imports into spreadsheet or database programs, and which can be validated with a checksum.

The SEL-351 Relay provides the following compressed ASCII commands:

<u>Command</u>	<u>Description</u>
CASCII	Configuration message
CSTATUS	Status message
CHISTORY	History message
CEVENT	Event message

CASCII COMMAND—GENERAL FORMAT

The compressed ASCII configuration message provides data for an external computer to extract data from other compressed ASCII commands. To obtain the configuration message for the compressed ASCII commands available in an SEL relay, type:

CAS <CR>

The relay sends:

```
<STX>"CAS",n,"yyyy"<CR><LF>
"COMMAND 1",ll,"yyyy"<CR><LF>
"#H","xxxxx","xxxxx",.....,"xxxxx","yyyy"<CR><LF>
"#D","ddd","ddd","ddd","ddd",.....,"ddd","yyyy"<CR><LF>
"COMMAND 2",ll,"yyyy"<CR><LF>
"#h","ddd","ddd",.....,"ddd","yyyy"<CR><LF>
"#D","ddd","ddd","ddd","ddd",.....,"ddd","yyyy"<CR><LF>
.
.
.
"COMMAND n",ll,"yyyy"<CR><LF>
"#H","xxxxx","xxxxx",.....,"xxxxx","yyyy"<CR><LF>
"#D","ddd","ddd","ddd","ddd",.....,"ddd","yyyy"<CR><LF><ETX>
```

where: n is the number of compressed ASCII command descriptions to follow.

COMMAND is the ASCII name for the compressed ASCII command as sent by the requesting device. The naming convention for the compressed ASCII commands is a 'C' preceding the typical command. For example, CSTATUS (abbreviated to CST) is the compressed STATUS command.

ll is the minimum access level at which the command is available.

#H identifies a header line to precede one or more data lines; '#' is the number of subsequent ASCII names. For example, "21H" identifies a header line with 21 ASCII labels.

#h identifies a header line to precede one or more data lines; '#' is the number of subsequent format fields. For example, "8h" identifies a header line with 8 format fields.

xxxxx is an ASCII name for corresponding data on following data lines. Maximum ASCII name width is 10 characters.

#D identifies a data format line; '#' is the maximum number of subsequent data lines.

ddd identifies a format field containing one of the following type designators:

I	Integer data
F	Floating point data
mS	String of maximum m characters (e.g., 10S for a 10 character string)

yyyy is the 4-byte hex ASCII representation of the checksum.

A compressed ASCII command may require multiple header and data configuration lines.

If a compressed ASCII request is made for data that are not available, (e.g. the history buffer is empty or invalid event request), the relay responds with the following message:

```
<STX>"No Data Available","yyyy"<CR><LF><ETX>
```

CASCII COMMAND—SEL-351

Display the SEL-351 Relay compressed ASCII configuration message by sending:

```
CAS <CR>
```

Relay models 0351x0, 0351x1 and 0351xY, Firmware Versions 5, 6, and 7, send:

```
<STX>
"CAS",5,"yyyy"<CR><LF>
"CST",1,"yyyy"<CR><LF>
"1H","FID","yyyy"<CR><LF>
"1D","45S","yyyy"<CR><LF>
"7H","MONTH","DAY","YEAR","HOUR","MIN","SEC","MSEC","yyyy"<CR><LF>
"1D","I","I","I","I","I","I","I","I","yyyy"<CR><LF>
"23H","IA","IB","IC","IN","VA","VB","VC","VS","MOF","+5V_PS","+5V_REG",
"-5V_REG","+12V_PS",-12V_PS","+15V_PS",
"-15V_PS","TEMP","RAM","ROM","A/D","CR_RAM",
"EEPROM","IO_BRD","yyyy"<CR><LF>
"1D","9S","9S","9S","9S","9S","9S","9S","9S","9S","9S","9S","9S","9S",
"9S","9S","9S","9S","9S","9S","9S","9S","9S","9S","9S","9S","9S",
"9S","9S","9S","9S","9S","9S","9S","9S","9S","9S","9S","9S","9S",
"CHI",1,"yyyy"<CR><LF>
"1H","FID","yyyy"<CR><LF>
"1D","45S","yyyy"<CR><LF>
"15H","REC_NUM","MONTH","DAY","YEAR","HOUR","MIN","SEC","MSEC",
"EVENT","LOCATION","CURR","FREQ","GROUP","SHOT","TARGETS",
```


CSTATUS COMMAND—SEL-351

Display status data in compressed ASCII format by sending:

CST <CR>

Relay models 0351x0 and 0351x send:

```
<STX>"FID","yyyy"<CR><LF>
Relay FID string,"yyyy"<CR><LF>
"MONTH","DAY","YEAR","HOUR","MIN","SEC","MSEC","yyyy"<CR><LF>
xxxx,xxxx,xxxx,xxxx,xxxx,xxxx,xxxx,xxxx,"yyyy"<CR><LF>
"IA","IB","IC","IN","VA","VB","VC","VS","MOF","+5V_PS","+5V_REG",
"-5V_REG","+12V_PS",-12V_PS","+15V_PS",-15V_PS",
"TEMP","RAM","ROM","A/D","CR_RAM","EEPROM","IO_BRD","yyyy"<CR><LF>
,"xxxx","xxxx","xxxx","xxxx","xxxx","xxxx",
"xxxx","xxxx","xxxx","xxxx","xxxx","xxxx","xxxx","xxxx","xxxx","xxxx",
"xxxx","xxxx","xxxx","xxxx","xxxx","xxxx","xxxx","yyyy"<CR><LF><ETX>
```

where: xxxx are the data values corresponding to the first line labels and
 yyyy is the 4-byte hex ASCII representation of the checksum.

CHISTORY COMMAND—SEL-351

Display history data in compressed ASCII format by sending:

CHI <CR>

The relay sends:

```
<STX>"FID","yyyy"<CR><LF>
Relay FID string,"yyyy"<CR><LF>
"REC_NUM","MONTH","DAY","YEAR","HOUR","MIN","SEC","MSEC",
"EVENT","LOCATION","CURR","FREQ","GROUP","SHOT","TARGETS",
"yyyy"<CR><LF>
xxxx,xxxx,xxxx,xxxx,xxxx,xxxx,xxxx,xxxx,"xxxx",xxxx,xxxx,xxxx,xxxx,xxxx,
"xxxx","yyyy"<CR><LF><ETX>
```

(the last line is then repeated for each record)

where: xxxx are the data values corresponding to the first line labels and
 yyyy is the 4-byte hex ASCII representation of the checksum.

If the history buffer is empty, the relay responds:

```
<STX>"No Data Available","yyyy"<CR><LF><ETX>
```

CEVENT COMMAND—SEL-351

Display event report in compressed ASCII format by sending:

CEV [**n Sx Ly L R C**] (parameters in [] are optional)

- where: **n** event number (1–29) if LER = 15, (1–15) if LER = 30, defaults to 1
Sx x samples per cycle (4 or 16); defaults to 4
If Sx parameter is present, it overrides the L parameter
Ly y cycles event report length (1 - LER) for filtered event reports,
(1 - LER+1) for raw event reports, defaults to 15 if not specified
L 16 samples per cycle; overridden by the Sx parameter, if present
R specifies raw (unfiltered) data; defaults to 16 samples per cycle unless
overridden by the Sx parameter. Defaults to 16 cycles in length unless
overridden with the Ly parameter.
C specifies 16 samples per cycle, 15 cycle length

The relay responds to the **CEV** command with the **n**th event report as shown below. Items in *italics* will be replaced with the actual relay data.

```
<STX>"FID","yyyy"<CR><LF>
"Relay FID string","yyyy"<CR><LF>
"MONTH","DAY","YEAR","HOUR","MIN","SEC","MSEC","yyyy"<CR><LF>
xxxx,xxxx,xxxx,xxxx,xxxx,xxxx,xxxx,"yyyy"<CR><LF>
"FREQ","SAM/CYC_A","SAM/CYC_D","NUM_OF_CYC","EVENT",
"LOCATION","SHOT","TARGETS","IA","IB","IC","IN","IG","3I2","yyyy"<CR><LF>
xxxx,xxxx,xxxx,xxxx,"xxxx",xxxx,xxxx,"xxxx",xxxx,xxxx,xxxx,xxxx,xxxx,
"yyyy"<CR><LF>
"IA","IB","IC","IN","IG","VA(kV)","VB(kV)","VC(kV)","VS(kV)","VDC","FREQ","TRIG",
"Names of elements in the relay word separated by spaces","yyyy"<CR><LF>
xxxx,xxxx,xxxx,xxxx,xxxx,xxxx,xxxx,xxxx,xxxx,xxxx,z,"HEX-ASCII Relay
Word","yyyy"<CR><LF>
"SETTINGS","yyyy"<CR><LF>
"Relay group, global, and logic settings as displayed with the showset command (surrounded
by quotes)","yyyy"<CR><LF><ETX>
```

- where: xxxx are the data values corresponding to the line labels.
yyyy is the 4-byte hex ASCII representation of the checksum.
FREQ is the power system frequency at the trigger instant.
SAM/CYC_A is the number of analog data samples per cycle (4 or 16).
SAM/CYC_D is the number of digital data samples per cycle (4 or 16).
NUM_OF_CYC is the number of cycles of data in the event report.
EVENT is the event type.
LOCATION is the fault location.
SHOT is the recloser shot counter.
TARGETS are the front-panel tripping targets.
IA, IB, IC, IN, IG, 3I2 is the fault current.
TRIG refers to the trigger record.

z is ">" for the trigger row, "*" for the fault current row and empty for all others. If the trigger row and fault current row are the same, both characters are included (e.g., ">*").

HEX-ASCII Relay Word is the hex ASCII format of the relay word. The first element in the relay word is the most significant bit in the first character.

If samples per cycle are specified as 16, the analog data are displayed at 1/16-cycle intervals and digital data at 1/4-cycle intervals. The digital data are displayed as a series of hex ASCII characters. The relay displays digital data only when they are available. When no data are available, the relay sends only the comma delimiter in the digital data field.

If the specified event does not exist, the relay responds:

```
<STX>"No Data Available","yyyy"<CR><LF><ETX>
```

The "*Names of elements in the Relay Word separated by spaces*" field is shown below for relay model 03517:

```
"50A1 50B1 50C1 50A2 50B2 50C2 50A3 50B3 50C3 50A4 50B4 50C4 50AB1 50BC1 50CA1
50AB2 50BC2 50CA2 50AB3 50BC3 50CA3 50AB4 50BC4 50CA4 50A 50B 50C 51A 51AT
51AR 51B 51BT 51BR 51C 51CT 51CR 51P 51PT 51PR 51N 51NT 51NR 51G 51GT 51GR
51Q 51QT 51QR 50P1 50P2 50P3 50P4 50N1 50N2 50N3 50N4 67P1 67P2 67P3 67P4 67N1
67N2 67N3 67N4 67P1T 67P2T 67P3T 67P4T 67N1T 67N2T 67N3T 67N4T 50G1 50G2 50G3
50G4 50Q1 50Q2 50Q3 50Q4 67G1 67G2 67G3 67G4 67Q1 67Q2 67Q3 67Q4 67G1T 67G2T
67G3T 67G4T 67Q1T 67Q2T 67Q3T 67Q4T 50P5 50P6 50N5 50N6 50G5 50G6 50Q5 50Q6
50QF 50QR 50GF 50GR 32VE 32QGE 32IE 32QE F32P R32P F32Q R32Q F32QG R32QG
F32V R32V F32I R32I 32PF 32PR 32QF 32QR 32GF 32GR 27A1 27B1 27C1 27A2 27B2 27C2
59A1 59B1 59C1 59A2 59B2 59C2 27AB 27BC 27CA 59AB 59BC 59CA 59N1 59N2 59Q
59V1 27S 59S1 59S2 59VP 59VS SF 25A1 25A2 3P27 3P59 81D1 81D2 81D3 81D4 81D5
81D6 27B81 50L 81D1T 81D2T 81D3T 81D4T 81D5T 81D6T VPOLV LOP * * IN106 IN105
IN104 IN103 IN102 IN101 LB1 LB2 LB3 LB4 LB5 LB6 LB7 LB8 LB9 LB10 LB11 LB12
LB13 LB14 LB15 LB16 RB1 RB2 RB3 RB4 RB5 RB6 RB7 RB8 RB9 RB10 RB11 RB12 RB13
RB14 RB15 RB16 LT1 LT2 LT3 LT4 LT5 LT6 LT7 LT8 LT9 LT10 LT11 LT12 LT13 LT14
LT15 LT16 SV1 SV2 SV3 SV4 SV1T SV2T SV3T SV4T SV5 SV6 SV7 SV8 SV5T SV6T
SV7T SV8T SV9 SV10 SV11 SV12 SV9T SV10T SV11T SV12T SV13 SV14 SV15 SV16
SV13T SV14T SV15T SV16T 79RS 79CY 79LO SH0 SH1 SH2 SH3 SH4 CLOSE CF RCSF
OPTMN RSTMN FSA FSB FSC BCW 50P32 * 59VA TRGTR 52A * * SG1 SG2 SG3 SG4 SG5
SG6 ZLOUT ZLIN ZLOAD BCWA BCWB BCWC * * * * ALARM OUT107 OUT106
OUT105 OUT104 OUT103 OUT102 OUT101 3PO SOTFE Z3RB KEY EKEY ECTT WFC PT
PTRX2 PTRX PTRX1 UBB1 UBB2 UBB Z3XT DSTRT NSTRT STOP BTX TRIP OC CC
DCHI DCLO 67P2S 67N2S 67G2S 67Q2S PDEM NDEM GDEM QDEM OUT201 OUT202
OUT203 OUT204 OUT205 OUT206 OUT207 OUT208 OUT209 OUT210 OUT211 OUT212 *
* * * IN208 IN207 IN206 IN205 IN204 IN203 IN202 IN201 * * * * * RMB8A RMB7A
RMB6A RMB5A RMB4A RMB3A RMB2A RMB1A TMB8A TMB7A TMB6A TMB5A
TMB4A TMB3A TMB2A TMB1A RMB8B RMB7B RMB6B RMB5B RMB4B RMB3B
RMB2B RMB1B TMB8B TMB7B TMB6B TMB5B TMB4B TMB3B TMB2B TMB1B
LBOKB CBADB RBADB ROKB LBOKA CBADA RBADA ROKA PWRA1 PWRB1 PWRC1
PWRA2 PWRB2 PWRC2 INTC INT3P PWRA3 PWRB3 PWRC3 PWRA4 PWRB4 PWRC4
INTA INTB SAGA SAGB SAGC SAG3P SWA SWB SWC SW3P"
```


APPENDIX F: SETTING NEGATIVE-SEQUENCE OVERCURRENT ELEMENTS

SETTING NEGATIVE-SEQUENCE DEFINITE-TIME OVERCURRENT ELEMENTS

Negative-sequence instantaneous overcurrent elements 50Q1 through 50Q6 and 67Q1 through 67Q4 should not be set to trip directly. This is because negative-sequence current can transiently appear when a circuit breaker is closed and balanced load current suddenly appears.

To avoid tripping for this transient condition, use negative-sequence definite-time overcurrent elements 67Q1T through 67Q4T with at least 1.5 cycles of time delay (transient condition lasts less than 1.5 cycles). For example, make time delay setting:

$$67Q1D = 1.50$$

for negative-sequence definite-time overcurrent element 67Q1T. Refer to Figures 3.12 and 3.13 for more information on negative-sequence instantaneous and definite-time overcurrent elements.

Negative-sequence instantaneous overcurrent elements 50Q5 and 50Q6 do not have associated timers (compare Figure 3.13 to Figure 3.12). If 50Q5 or 50Q6 need to be used for tripping, run them through SELOGIC[®] control equation variable timers (see Figures 7.25 and 7.26) and use the outputs of the timers for tripping.

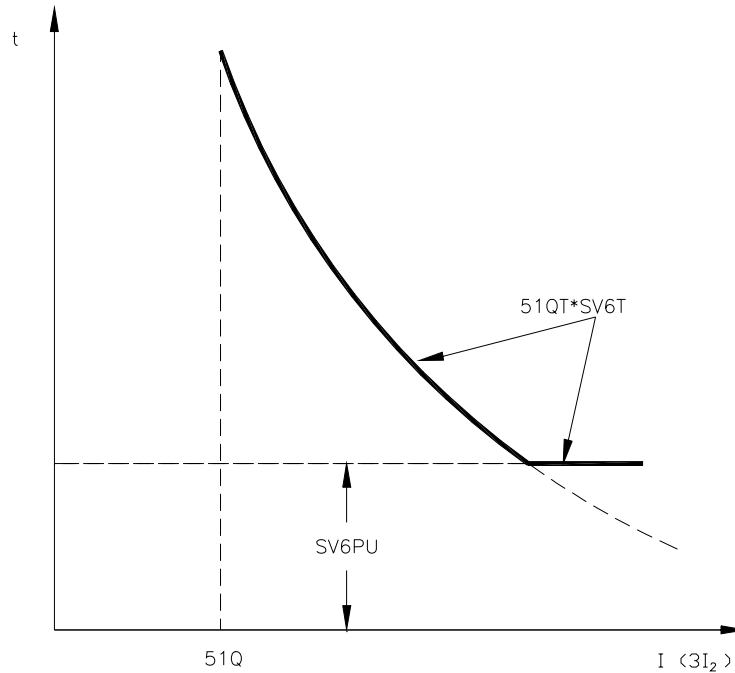
Continue reading in *Coordinating Negative-Sequence Overcurrent Elements* in this appendix for guidelines on coordinating negative-sequence definite-time overcurrent elements and a following coordination example. The coordination example uses time-overcurrent elements, but the same principles can be applied to definite-time overcurrent elements.

SETTING NEGATIVE-SEQUENCE TIME-OVERCURRENT ELEMENTS

Negative-sequence time-overcurrent element 51QT should not be set to trip directly when it is set with a low time-dial setting 51QTD, that results in curve times below 3 cycles (see curves in Figures 9.1 through 9.10 in *Section 9: Setting the Relay*). This is because negative-sequence current can transiently appear when a circuit breaker is closed and balanced load current suddenly appears. Refer to Figure 3.20 for more information on negative-sequence time-overcurrent element 51QT.

To avoid having negative-sequence time-overcurrent element 51QT with such low time-dial settings trip for this transient negative-sequence current condition, make settings similar to the following:

- SV6PU = 1.50 cycles (minimum response time; transient condition lasts less than 1.5 cycles)
- SV6 = 51Q (run pickup of negative-sequence time-overcurrent element 51QT through SELOGIC control equation variable timer SV6)
- TR = ..+51QT*SV6T+.. (trip conditions; SV6T is the output of the SELOGIC control equation variable timer SV6)



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Figure F.1: Minimum Response Time Added to a Negative-Sequence Time-Overcurrent Element 51QT

Continue reading in *Coordinating Negative-Sequence Overcurrent Elements* in this appendix for guidelines on coordinating negative-sequence time-overcurrent elements and a following coordination example.

COORDINATING NEGATIVE-SEQUENCE OVERCURRENT ELEMENTS

The following coordination guidelines and example assume that the negative-sequence overcurrent elements operate on $3I_2$ magnitude negative-sequence current and that the power system is radial. The negative-sequence overcurrent elements in the SEL-351 Relay operate on $3I_2$ magnitude negative-sequence current.

The coordination example is a generic example that can be used with any relay containing negative-sequence overcurrent elements that operate on $3I_2$ magnitude negative-sequence current.

The SEL-351 Relay can be inserted as the feeder relay in this example. Note that the overcurrent element labels in the example are not the same as the labels of the corresponding SEL-351 Relay overcurrent elements.

Coordination Guidelines

1. Start with the furthest downstream negative-sequence overcurrent element (e.g., distribution feeder relay in a substation).
2. Identify the phase overcurrent device (e.g., line recloser, fuse) downstream from the negative-sequence overcurrent element that is of greatest concern for coordination. This is usually the phase overcurrent device with the longest clearing time.
3. Consider the negative-sequence overcurrent element as an “equivalent” phase overcurrent element. Derive pickup, time dial (lever), curve type, or time-delay settings for this “equivalent” element to coordinate with the downstream phase overcurrent device, as any phase coordination would be performed. Load considerations can be disregarded when deriving the “equivalent” phase overcurrent element settings.
4. Multiply the “equivalent” phase overcurrent element pickup setting by $\sqrt{3}$ to convert it to the negative-sequence overcurrent element pickup setting in terms of $3I_2$ current.

$$\left. \begin{array}{l} \text{Negative-} \\ \text{sequence} \\ \text{overcurrent} \\ \text{element} \\ \text{pickup} \end{array} \right\} = \sqrt{3} \cdot (\text{“equivalent” phase overcurrent element pickup})$$

Any time dial (lever), curve type, or time delay calculated for the “equivalent” phase overcurrent element is also used for the negative-sequence overcurrent element with no conversion factor applied.

5. Set the next upstream negative-sequence overcurrent element to coordinate with the first downstream negative-sequence overcurrent element and so on. Again, coordination is not influenced by load considerations.

Coordination Example

In Figure F.2, the phase and negative-sequence overcurrent elements of the feeder relay (51F and 51QF, respectively) must coordinate with the phase overcurrent element of the line recloser (51R).

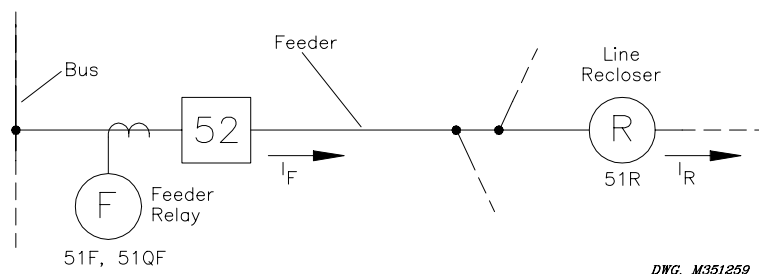


Figure F.2: Distribution Feeder Protective Devices

- I_F = Maximum load current through feeder relay = 450 A
- I_R = Maximum load current through line recloser = 150 A
- 51F = Feeder relay phase time-overcurrent element
- 51QF = Feeder relay negative-sequence time-overcurrent element
- 51R = Line recloser phase time-overcurrent element (phase “slow curve”)

Traditional Phase Coordination

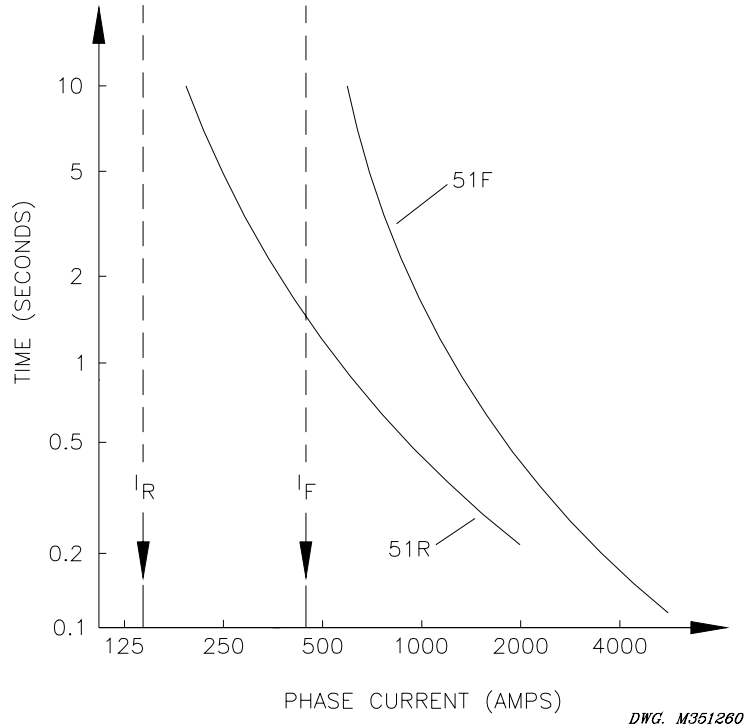


Figure F.3: Traditional Phase Coordination

51F: pickup = 600 A (above max. feeder load, I_F)

51R: pickup = 200 A (above max. line recloser load, I_R)

Figure F.3 shows traditional phase overcurrent element coordination between the feeder relay and line recloser phase overcurrent elements. Phase overcurrent elements must accommodate load and cold load pickup current. The 450 A maximum feeder load current limits the sensitivity of the feeder phase overcurrent element, 51F, to a pickup of 600 A. The feeder relay cannot back up the line recloser for phase faults below 600 A.

Apply the Feeder Relay Negative-Sequence Overcurrent Element (Guidelines 1 to 3)

Applying negative-sequence overcurrent element coordination Guidelines 1 to 3 results in the feeder relay “equivalent” phase overcurrent element (51EP) in Figure F.4. Curve for 51F is shown for comparison only.

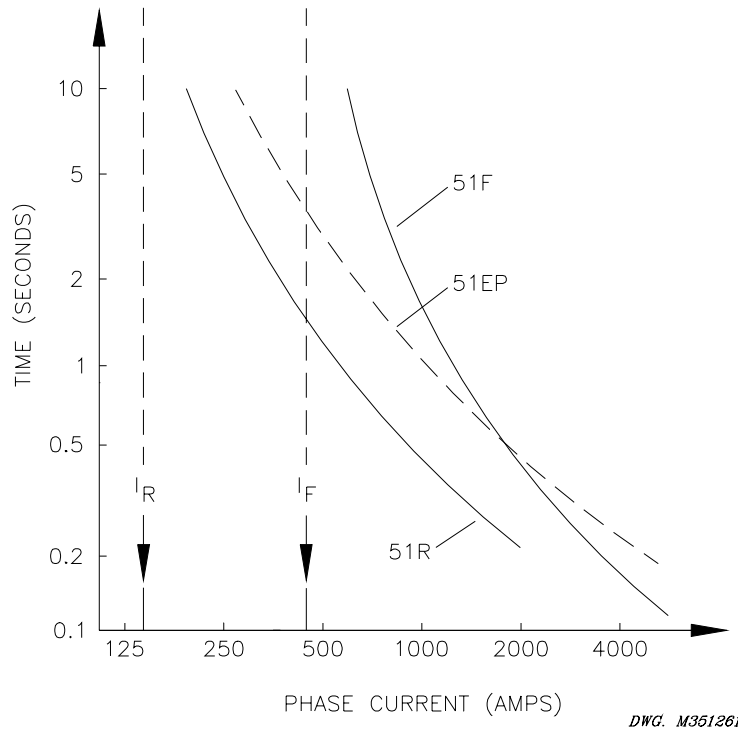


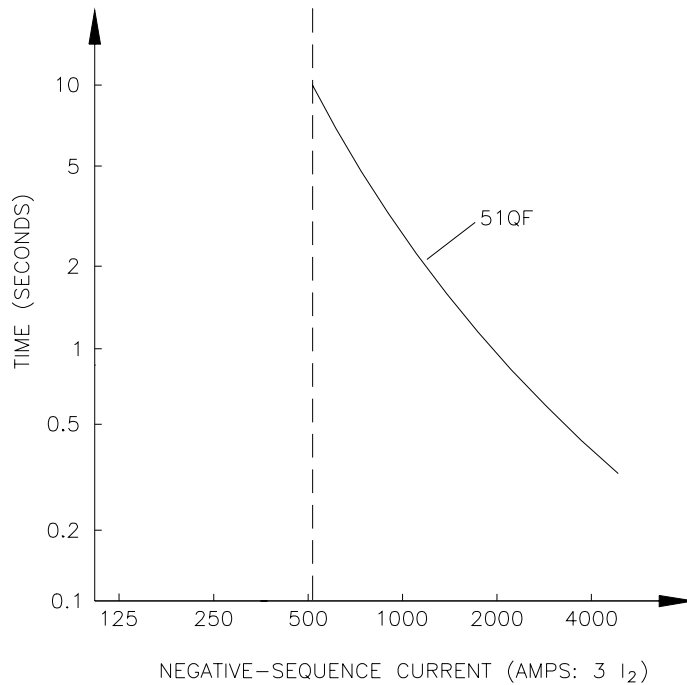
Figure F.4: Phase-to-Phase Fault Coordination

51EP: pickup = 300 A (below max. feeder load, I_F)

Considerable improvement in sensitivity and speed of operation for phase-to-phase faults is achieved with the 51EP element. The 51EP element pickup of 300 A has twice the sensitivity of the 51F element pickup of 600 A. The 51EP element speed of operation for phase-to-phase faults below about 2000 A is faster than that for the 51F element.

Convert “Equivalent” Phase Overcurrent Element Settings to Negative-Sequence Overcurrent Element Settings (Guideline 4)

The “equivalent” phase overcurrent element (51EP element in Figure F.4) converts to true negative-sequence overcurrent element settings (51QF in Figure F.5) by applying the equation given in Guideline 4. The time dial (lever) and curve type of the element remain the same (if the element is a definite-time element, the time delay remains the same).



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Figure F.5: Negative-Sequence Overcurrent Element Derived from “Equivalent” Phase Overcurrent Element, 51EP

$$51QF : \text{pickup} = \sqrt{3} \cdot (300A) = 520A$$

Having achieved coordination between the feeder relay negative-sequence overcurrent element (51QF) and the downstream line recloser phase overcurrent element (51R) for phase-to-phase faults, coordination between the two devices for other fault types is also achieved.

Negative-Sequence Overcurrent Element Applied at a Distribution Bus (Guideline 5)

The preceding example was for a distribution feeder. A negative-sequence overcurrent element protecting a distribution bus provides an even more dramatic improvement in phase-to-phase fault sensitivity.

The distribution bus phase overcurrent element pickup must be set above the combined load of all the feeders on the bus, plus any emergency load conditions. The bus phase overcurrent element pickup is often set at least four times greater than the pickup of the feeder phase overcurrent element it backs up. Thus, sensitivity to both bus and feeder phase faults is greatly reduced. Feeder relay backup by the bus relay is limited.

Negative-sequence overcurrent elements at the distribution bus can be set significantly below distribution bus load levels and provide dramatically increased sensitivity to phase-to-phase faults. It is coordinated with the distribution feeder phase or negative-sequence overcurrent elements and provides more-sensitive and faster phase-to-phase fault backup.

Ground Coordination Concerns

If the downstream protective device includes ground overcurrent elements, in addition to phase overcurrent elements, there should be no need to check the coordination between the ground overcurrent elements and the upstream negative-sequence overcurrent elements. The downstream phase overcurrent element, whether it operates faster or slower than its complementary ground overcurrent element, will operate faster than the upstream negative-sequence overcurrent element for all faults, including those that involve ground.

OTHER NEGATIVE-SEQUENCE OVERCURRENT ELEMENT REFERENCES

A. F. Elneweihi, E. O. Schweitzer, M. W. Feltis, "Negative-Sequence Overcurrent Element Application and Coordination in Distribution Protection," IEEE Transactions on Power Delivery, Volume 8, Number 3, July 1993, pp. 915-924.

This IEEE paper is the source of the coordination guidelines and example given in this appendix. The paper also contains analyses of system unbalances and faults and the negative-sequence current generated by such conditions.

A. F. Elneweihi, "Useful Applications for Negative-Sequence Overcurrent Relaying," 22nd Annual Western Protective Relay Conference, Spokane, Washington, October 24-26, 1995.

This conference paper gives many good application examples for negative-sequence overcurrent elements. The focus is on the transmission system, where negative-sequence overcurrent elements provide better sensitivity than zero-sequence overcurrent elements in detecting some single-line-to-ground faults.

If the maximum phase current is above the level of the phase time-overcurrent pickup setting 51PP, phase time-overcurrent element 51PT is either timing on its curve or is already timed out.

Phase Time-Overcurrent Element 51PT Time-Out Indication

If phase time-overcurrent element 51PT is not timed out on its curve, Relay Word bit 51PT is in the following state:

$$51PT = 0 \quad (\text{logical } 0)$$

If phase time-overcurrent element 51PT is timed out on its curve, Relay Word bit 51PT is in the following state:

$$51PT = 1 \quad (\text{logical } 1)$$

Phase Time-Overcurrent Element 51PT Reset Indication

If phase time-overcurrent element 51PT is not fully reset, Relay Word bit 51PR is in the following state:

$$51PR = 0 \quad (\text{logical } 0)$$

If phase time-overcurrent element is fully reset, Relay Word bit 51PR is in the following state:

$$51PR = 1 \quad (\text{logical } 1)$$

If phase time-overcurrent element 51PT is not fully reset, the element is either:

- Timing on its curve
- Already timed out
- Is timing to reset (one-cycle reset or electromechanical emulation—see setting 51PRS)

Relay Word Bit Application Examples—Phase Time-Overcurrent Element 51PT

Common uses for Relay Word bits 51P, 51PT, and 51PR:

- | | |
|------|---|
| 51P | testing (e.g., assign to an output contact for pickup testing)
trip unlatch logic (see SELOGIC control equation unlatch trip setting ULTR example later in this section) |
| 51PT | trip logic (see SELOGIC control equation trip setting TR example later in this section) |
| 51PR | used in testing (e.g., assign to an output contact for reset indication) |

Other Relay Word Bits

The preceding example was for a phase time-overcurrent element, demonstrating Relay Word bit operation for pickup, time-out, and reset conditions. Other Relay Word bits (e.g., those for definite-time overcurrent elements, voltage elements, frequency elements) behave similarly in their assertion or deassertion to logical 1 or logical 0, respectively. The time-overcurrent

elements (like the preceding phase time-overcurrent element example) are rather unique because they have a Relay Word bit (e.g., 51PR) that asserts for the reset state of the element.

Relay Word bits are used in SELOGIC control equations, which are explained in the following subsection.

SELOGIC CONTROL EQUATIONS

Many of the protection and control element logic inputs shown in the various figures in *Section 3* through *Section 8* are SELOGIC control equations (labeled “SELOGIC Settings” in most of the Figures). SELOGIC control equations are set with combinations of Relay Word bits to accomplish such functions as:

- Tripping circuit breakers
- Assigning functions to optoisolated inputs
- Operating output contacts
- Torque-controlling overcurrent elements
- Switching active setting groups
- Enabling/disabling reclosing

Traditional or advanced custom schemes can be created with SELOGIC control equations.

SELOGIC Control Equation Operators

SELOGIC control equation settings use logic similar to Boolean algebra logic, combining Relay Word bits together using one or more of the six SELOGIC control equation operators listed in Table G.1.

Table G.1: SELOGIC Control Equation Operators (Listed in Processing Order)

Operator	Logic Function
/	rising edge detect
\	falling edge detect
()	parentheses
!	NOT
*	AND
+	OR

Operators in a SELOGIC control equation setting are processed in the order shown in Table G.1.

SELOGIC Control Equation Parentheses Operator ()

More than one set of parentheses () can be used in a SELOGIC control equation setting. For example, the following SELOGIC control equation setting has two sets of parentheses:

$$SV7 = (SV7+IN101)*(50P1+50N1)$$

In the above example, the logic within the parentheses is processed first and then the two parentheses resultants are ANDed together. The above example is from Figure 7.27 in **Section 7: Inputs, Outputs, Timers, and Other Control Logic**. Parentheses cannot be “nested” (parentheses within parentheses) in a SELOGIC control equation setting.

SELOGIC Control Equation NOT Operator !

The NOT operator ! is applied to a single Relay Word bit and also to multiple elements (within parentheses). Following are examples of both.

Example of NOT Operator ! Applied to Single Element

The internal circuit breaker status logic in the SEL-351 Relay operates on 52a circuit breaker auxiliary contact logic. The SELOGIC control equation circuit breaker status setting is labeled 52A. See **Optoisolated Inputs** in **Section 7: Inputs, Outputs, Timers, and Other Control Logic** and **Close Logic** in **Section 6: Close and Reclose Logic** for more information on SELOGIC control equation circuit breaker status setting 52A.

When a circuit breaker is closed, the 52a circuit breaker auxiliary contact is closed. When a circuit breaker is open, the 52a contact is open.

The opposite is true for a 52b circuit breaker auxiliary contact. When a circuit breaker is closed, the 52b circuit breaker auxiliary contact is open. When the circuit breaker is open, the 52b contact is closed.

If a 52a contact is connected to optoisolated input IN101, the SELOGIC control equation circuit breaker status setting 52A is set:

$$52A = IN101$$

Conversely, if a 52b contact is connected to optoisolated input IN101, the SELOGIC control equation circuit breaker status setting 52A is set:

$$52A = !IN101 \quad [=NOT(IN101)]$$

With a 52b contact connected, if the circuit breaker is closed, the 52b contact is open and input IN101 is deenergized [IN101 = 0 (logical 0)]:

$$52A = !IN101 = NOT(IN101) = NOT(0) = 1$$

Thus, the SELOGIC control equation circuit breaker status setting 52A sees a closed circuit breaker.

With a 52b contact connected, if the circuit breaker is open, the 52b contact is closed and input IN101 is energized [IN101 = 1 (logical 1)]:

$$52A = !IN101 = \text{NOT}(IN101) = \text{NOT}(1) = 0$$

Thus, the SELOGIC control equation circuit breaker status setting 52A sees an open circuit breaker.

Example of NOT Operator ! Applied to Multiple Elements (Within Parentheses)

The SELOGIC control equation trip unlatch setting is set as follows:

$$ULTR = !(51P + 51G)$$

Refer also to *Trip Logic* in *Section 5: Trip and Target Logic*.

In this factory setting example, the unlatch condition comes true only when both the 51P (phase time-overcurrent element pickup indication) and 51G (residual ground time-overcurrent element pickup indication) Relay Word bits deassert:

$$ULTR = !(51P + 51G) = \text{NOT}(51P + 51G)$$

As stated previously, the logic within the parentheses is performed first. In this example, the states of Relay Word bits 51P and 51G are ORed together. Then the NOT operator is applied to the logic resultant from the parentheses.

If either one of 51P or 51G is still asserted [e.g., 51G = 1 (logical 1)], the unlatch condition is not true:

$$ULTR = \text{NOT}(51P + 51G) = \text{NOT}(0 + 1) = \text{NOT}(1) = 0$$

If both 51P and 51G are deasserted [i.e., 51P = 0 and 51G = 0 (logical 0)], the unlatch condition is true:

$$ULTR = \text{NOT}(51P + 51G) = \text{NOT}(0 + 0) = \text{NOT}(0) = 1$$

and the trip condition can unlatch, subject to other conditions in the trip logic (see Figure 5.1).

SELogic Control Equation Rising Edge Operator /

The rising edge operator / is applied to individual Relay Word bits only—not to groups of elements within parentheses. For example, the SELOGIC control equation event report generation setting uses rising edge operators:

$$ER = /51P + /51G + /OUT103$$

The Relay Word bits in this factory setting example are:

- 51P Maximum phase current above pickup setting 51PP for phase time-overcurrent element 51PT (see Figure 3.14)
- 51G Maximum residual ground current above pickup setting 51GP for residual ground time-overcurrent element 51GT (see Figure 3.19)
- OUT103 Output contact OUT103 is set as a breaker failure trip output (see Output Contacts in *Section 7: Inputs, Outputs, Timers, and Other Control Logic*)

When setting ER sees a logical 0 to logical 1 transition, it generates an event report (if the relay is not already generating a report that encompasses the new transition). The rising edge operators in the above factory setting example allow setting ER to see each transition individually.

Suppose a ground fault occurs and a breaker failure condition finally results. Figure G.1 demonstrates the action of the rising edge operator / on the individual elements in setting ER.

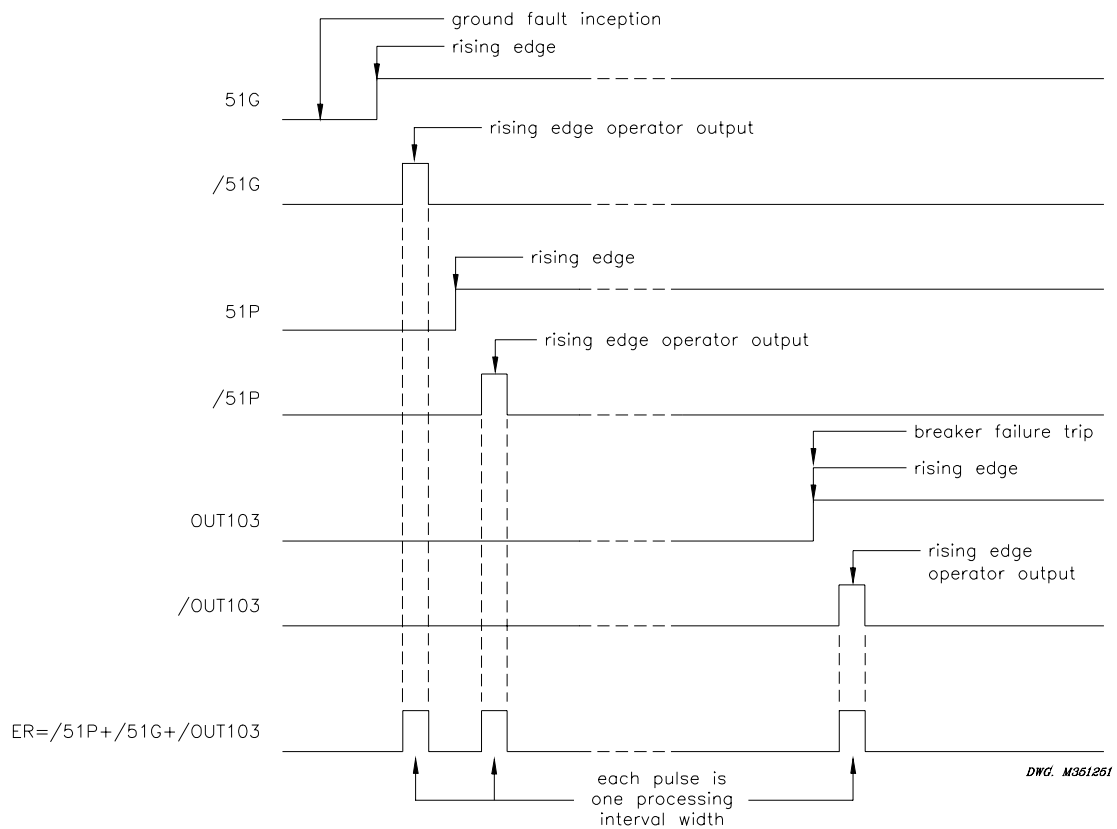


Figure G.1: Result of Rising Edge Operators on Individual Elements in Setting ER

Note in Figure G.1 that setting ER sees three separate rising edges, due to the application of rising edge operators /. The rising edge operator / in front of a Relay Word bit sees this logical 0 to logical 1 transition as a “rising edge” and the resultant asserts to logical 1 for one processing interval. The assertions of 51G and 51P are close enough that they will be on the same event report (generated by 51G asserting first). The assertion of OUT103 for a breaker failure condition is some appreciable time later and will generate another event report, if the first event report capture has ended when OUT103 asserts.

If the rising edge operators / were not applied and setting ER was:

$$ER = 51P + 51G + OUT103$$

the ER setting would not see the assertion of OUT103, because 51G and 51P would continue to be asserted at logical 1, as shown in Table G.1.

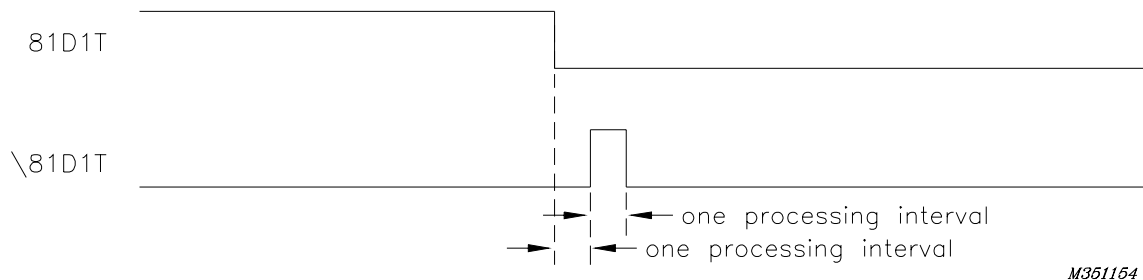
SELogic Control Equation Falling Edge Operator \

The falling edge operator \ is applied to individual Relay Word bits only—not to groups of elements within parentheses. The falling edge operator \ operates similar to the rising edge operator, but looks for Relay Word bit deassertion (element going from logical 1 to logical 0). The falling edge operator \ in front of a Relay Word bit sees this logical 1 to logical 0 transition as a “falling edge” and asserts to logical 1 for one processing interval.

For example, suppose the SELOGIC control equation event report generation setting is set with the detection of the falling edge of an underfrequency element:

$$ER = \dots + \backslash 81D1T$$

When frequency goes above the corresponding pickup level 81D1P, Relay Word bit 81D1T deasserts and an event report is generated (if the relay is not already generating a report that encompasses the new transition). This allows a recovery from an underfrequency condition to be observed. See Figure 3.30 and Table 3.11 in *Section 3: Overcurrent, Voltage, Synchronism Check, Frequency, and Power Elements*. Figure G.2 demonstrates the action of the falling edge operator \ on the underfrequency element in setting ER.



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Figure G.2: Result of Falling Edge Operator on a Deasserting Underfrequency Element

SELogic Control Equation Operation Example—Tripping

If tripping does not involve communications-assisted or switch-onto-fault trip logic, the SELOGIC control equation trip setting TR is the only trip setting needed. Refer to *Trip Logic* in *Section 5: Trip and Target Logic*.

Note that Figure 5.1 in *Section 5: Trip and Target Logic* appears quite complex. But since tripping does not involve communications-assisted or switch-onto-fault trip logic in this example, respective SELOGIC control equation trip settings TRCOMM and TRSOTF are not used. The only effective input into logic gate OR-1 in Figure 5.1 is SELOGIC control equation trip setting TR.

TR	=	51PT+51GT+50P1*SH0	(fuse saving example)
TRCOMM	=	0	(not used—set directly to logical 0)
TRSOTF	=	0	(not used—set directly to logical 0)
ULTR	=	!(51P + 51G)	(discussed in preceding subsection)

Analysis of SELogic Control Equation Trip Setting TR

Again, the example trip equation is:

$$TR = 51PT+51GT+50P1*SH0$$

The Relay Word bit definitions are:

51PT	phase time-overcurrent element timed out
51GT	residual ground time-overcurrent element timed out
50P1	phase instantaneous overcurrent element asserted
SH0	reclosing relay shot counter at shot = 0

In the trip equation, the AND operator * is executed before the OR operators +, Table G.1:

$$50P1*SH0$$

Element 50P1 can only cause a trip if the reclosing relay shot counter is at shot = 0. When the reclosing relay shot counter is at shot = 0 (see Table 6.3), Relay Word bit SH0 is in the following state:

$$SH0 = 1 \quad (\text{logical 1})$$

If maximum phase current is above the phase instantaneous overcurrent element pickup setting 50P1P (see Figure 3.1), Relay Word bit 50P1 is in the following state:

$$50P1 = 1 \quad (\text{logical 1})$$

With SH0 = 1 and 50P1 = 1, the ANDed combination results in:

$$50P1*SH0 = 1*1 = 1 \quad (\text{logical 1})$$

and an instantaneous trip results. This logic is commonly used in fuse saving schemes for distribution feeders.

If the reclosing relay shot counter advances to shot = 1 for the reclose that follows the trip, Relay Word bit SH0 is in the following state:

$$SH0 = 0 \quad (\text{logical 0})$$

If maximum phase current is above the phase instantaneous overcurrent element pickup setting 50P1P for the reoccurring fault, Relay Word bit 50P1 is in the following state:

$$50P1 = 1 \quad (\text{logical 1})$$

With SH0 = 0 and 50P1 = 1, the ANDed combination results in:

$$50P1 * SH0 = 1 * 0 = 0 \quad (\text{logical } 0)$$

and no trip results from phase instantaneous overcurrent element 50P1.

A trip will eventually result if time-overcurrent element 51PT or 51GT times out. If residual ground time-overcurrent element 51GT times out, Relay Word bit 51GT is in the following state:

$$51GT = 1 \quad (\text{logical } 1)$$

When shot = 1, SH0 = 0 and the result is:

$$TR = 51PT + 51GT + 50P1 * SH0 = 0 + 1 + 1 * 0 = 0 + 1 + 0 = 1$$

and a time-delayed trip results from residual ground time-overcurrent element 51GT.

Set an Output Contact for Tripping

To assert output contact OUT101 to trip a circuit breaker, make the following SELOGIC control equation output contact setting (see *Output Contacts* in *Section 7: Inputs, Outputs, Timers, and Other Control Logic*):

$$OUT101 = TRIP$$

All SELOGIC Control Equations Must Be Set

All SELOGIC control equations must be set one of the following ways (they cannot be “blank”):

- Single Relay Word bit (e.g., 52A = IN101)
- Combination of Relay Word bits (e.g., TR = 51PT+51GT+50P1*SH0)
- Directly to logical 1 (e.g., 67P1TC = 1)
- Directly to logical 0 (e.g., TRCOMM = 0)

Set SELOGIC Control Equations Directly to 1 or 0

SELOGIC control equations can be set directly to:

$$1 \text{ (logical } 1) \quad \text{or} \quad 0 \text{ (logical } 0)$$

instead of with Relay Word bits. If a SELOGIC control equation setting is set directly to 1, it is always “asserted/on/enabled.” If a SELOGIC control equation setting is set equal to 0, it is always “deasserted/off/disabled.”

Note: SELOGIC control equation torque control settings (e.g., 67P1TC, 51P1TC) cannot be set directly to logical 0.

Under the *SHO Command (Show/View Settings)* in *Section 10: Serial Port Communications and Commands*, note that a number of the factory SELOGIC control equation settings are set directly to 1 or 0.

The individual SELOGIC control equation settings explanations (referenced in Settings Sheets 11 through 15 at the end of **Section 9: Setting the Relay**) discuss whether it makes logical sense to set the given SELOGIC control equation setting to 0 or 1 for certain criteria.

Set SELOGIC Control Equations Directly to 1 or 0—Example

Of special concern are the SELOGIC control equation torque control settings 67P1TC through 51QTC for the overcurrent elements. In the factory settings the SEL-351 Relay ships with in a standard relay shipment, these are all set directly to logical 1. See these factory settings in **SHO Command (Show/View Settings)** in **Section 10: Serial Port Communications and Commands**.

If one of these torque control settings is set directly to logical 1

e.g., 51PTC = 1 (set directly to logical 1)

then the corresponding overcurrent element (e.g., phase time-overcurrent element 51PT) is subject only to the directional control. See Figure 3.14 in **Section 3: Overcurrent, Voltage, Synchronism Check, Frequency, and Power Elements** for phase time-overcurrent element 51PT logic.

If the directional control enable setting E32 = N (and 51PTC = 1), then time-overcurrent element 51PT is enabled (assuming pickup setting 51PP is made) and nondirectional.

SELOGIC Control Equation Limitations

Any single SELOGIC control equation setting is limited to 15 Relay Word bits that can be combined together with the SELOGIC control equation operators listed in Table G.1. If this limit must be exceeded, use a SELOGIC control equation variable (SELOGIC control equation settings SV1 through SV12) as an intermediate setting step.

For example, assume that the trip equation (SELOGIC control equation trip setting TR) needs more than 15 Relay Word bits in its equation setting. Instead of placing all Relay Word bits into TR, program some of them into the SELOGIC control equation setting SV1. Next, use the resultant SELOGIC control equation variable output (Relay Word bit SV1) in the SELOGIC control equation trip setting TR.

Note in Table G.3 that the SELOGIC control equation variables (SELOGIC control equation settings SV1 through SV16) are processed after the trip equation (SELOGIC control equation trip setting TR). Thus, any tripping via Relay Word bits SV1 through SV16 can be delayed as much as 1/4 cycle. For most applications, this is probably of no consequence.

The SELOGIC control equation settings as a whole in a particular setting group have the following limitations, according to model number (see Table 1.2):

Table G.2: SELOGIC Control Equation Settings Limitations for Different SEL-351 Relay Models

Model Number	SELOGIC Control Equation Settings Limitations per Setting Group
03515 03516 03517	Average of 3 Relay Word bits per equation. Average of 1 rising edge or falling edge operator per three equations (54 edges maximum).

SELOGIC control equation settings that are set directly to 1 (logical 1) or 0 (logical 0) also have to be included in these limitations—each such setting counted as one Relay Word bit.

After SELOGIC control equation settings changes have been made and the settings are saved, the SEL-351 responds with the following message:

xxx Elements and yy Edges remain available

indicating that “xxx” Relay Word bits can still be used and “yy” rising or falling edge operators can still be applied in the SELOGIC control equations for the particular settings group.

PROCESSING ORDER AND PROCESSING INTERVAL

The relay elements and logic (and corresponding SELOGIC control equation settings and resultant Relay Word bits) are processed in the order shown in Table G.3 (top to bottom). They are processed every quarter-cycle (1/4-cycle), and the Relay Word bit states (logical 1 or logical 0) are updated with each quarter-cycle pass. Thus, the relay processing interval is 1/4-cycle. Once a Relay Word bit is asserted, it retains the state (logical 1 or logical 0) until it is updated again in the next processing interval.

Table G.3: Processing Order of Relay Elements and Logic (Top to Bottom)

Relay Elements and Logic (corresponding SELOGIC Control Equations listed in parentheses)	Resultant Relay Word Bits	Reference Instruction Manual Section
Substation Battery Voltage	DCHI, DCLO	Section 8
Optoisolated Inputs	IN101–IN106 (Models 0351x0, 0351x1, and 0351xY) IN201–IN208 (Models 0351x1 and 0351xY)	Section 7
Polarizing Voltage	VPOLV	Section 4
Power Elements	PWRA1, PWRA2, PWRA3, PWRA4, PWRB1, PWRB2, PWRB3, PWRB4, PWRC1, PWRC2, PWRC3, PWRC4,	Section 3
Miscellaneous Instantaneous Overcurrent Elements	50A1-50A4, 50B1-50B4, 50C1-50C4, 50A, 50B, 50C, 50AB1-50AB4, 50BC1-50BC4, 50CA1-50CA4, 50QF, 50QR, 50GF, 50GR, 50L	Section 3
Demand Ammeters	PDEM, NDEM, GDEM, QDEM	Section 8
Open Breaker Logic (52A)	3PO	Section 5
Loss-of-Potential	LOP, ILOP	Section 4
Fault Identification Logic	FSA, FSB, FSC	Section 5
Load Encroachment	ZLOUT, ZLIN, ZLOAD	Section 4
Local Control Switches	LB1-LB16	Section 7
Remote Control Switches	RB1-RB16	Section 7
Latch Control Switches (SET1-SET16, RST1-RST16)	LT1-LT16	Section 7
Voltage Elements	27A1, 27B1, 27C1, 27A2, 27B2, 27C2, 59A1, 59B1, 59C1, 59A2, 59B2, 59C2, 27AB, 27BC, 27CA, 59AB, 59BC, 59CA, 59N1, 59N2, 59Q, 59V1, 27S, 59S1, 59S2, 59VP, 59VS, 3P27, 3P59, 27B81, 27AB1, 27BC1, 27CA1, 27AB2, 27BC2, 27CA2, 59AB1, 59BC1, 59CA1, 59AB2, 59BC2, 59CA2, 59Q1, 59Q2	Section 3
Voltage Sag/Swell/Interruption Elements	INTA-INT3P, SAGA-SAG3P, SWA-SW3P	Section 3
Frequency Elements	81D1, 81D2, 81D3, 81D4, 81D5, 81D6, 81D1T, 81D2T, 81D3T, 81D4T, 81D5T, 81D6T	Section 3
Synchronism Check Elements (BSYNCH)	SF, 25A1, 25A2	Section 3

Relay Elements and Logic (corresponding SELOGIC Control Equations listed in parentheses)	Resultant Relay Word Bits	Reference Instruction Manual Section
Directional Elements (E32IV)	32QE, 32QGE, 32VE, 32IE, F32P, R32P, F32Q, R32Q, F32QG, R32QG, F32V, R32V, F32I, R32I, 32PF, 32PR, 32QF, 32QR, 32GF, 32GR	Section 4
Instantaneous/Definite-Time Overcurrent Elements (67P1TC-67P4TC, 67N1TC-67N4TC, 67G1TC-67G4TC, 67Q1TC-67Q4TC)	50P1-50P6, 50N1-50N6, 50G1-50G6, 50Q1- 50Q6, 67P1-67P4, 67P1T-67P4T, 67N1- 67N4, 67N1T-67N4T, 67G1-67G4, 67Q1T- 67Q4T, 67P2S, 67N2S, 67G2S, 67Q2S	Section 3
Time-Overcurrent Elements (51PTC, 51ATC, 51BTC, 51CTC, 51NTC, 51GTC, 51QTC)	51P, 51A, 51B, 51C, 51N, 51G, 51Q, 51PT, 51AT, 51BT, 51CT, 51NT, 51GT, 51QT, 51PR, 51AR, 51BR, 51CR, 51NR, 51GR, 51QR	Section 3
Switch-onto-Fault Logic (CLMON)	SOTFE	Section 5
Communications-Assisted Trip Schemes (PT1, LOG1, PT2, LOG2, BT)	PT, PTRX1, PTRX2, PTRX, UBB1, UBB2, UBB, Z3RB, KEY, EKEY, ECTT, WFC, Z3XT, DSTRT, NSTRT, STOP, BTX	Section 5
Trip Logic (TR, TRSOTF, TRCOMM, DTT, ULTR)	TRIP	Section 5
Close Logic (CL, ULCL) Reclosing Relay (79RI, 79RIS, 79DTL, 79DLS, 79SKP, 79STL, 79BRS, 79SEQ, 79CLS)	CLOSE, CF, RCSF, OPTMN, RSTMN, 79RS, 79CY, 79LO, SH0, SH1, SH2, SH3, SH4	Section 6
Breaker Monitor (BKMON)	BCWA, BCWB, BCWC, BCW	Section 8
SELOGIC Control Equation Variables/Timers (SV1-SV16)	SV1-SV16, SV1T-SV16T	Section 7
OUT101–OUT107 (Models 0351x0 and 0351x1) OUT201–OUT212 (Model 0351x1)	OUT101–OUT107 (Models 0351x0 and 0351x1) OUT201–OUT212 (Model 0351x1)	Section 7
Display Points (DP1-DP16)		Section 7
Setting Group (SS1-SS6)	SG1-SG6	Section 7
Event Report Trigger (ER)		Section 12
Target Logic	TRGTR	Section 5

APPENDIX H: DISTRIBUTED NETWORK PROTOCOL (DNP) 3.00

OVERVIEW

Some versions of the SEL-351 family of relays support Distributed Network Protocol (DNP) 3.00 L2 Slave protocol. This includes access to metering data, protection elements (Relay Word), contact I/O, targets, sequential events recorder, breaker monitor, relay summary event reports, settings groups, and time synchronization. The SEL-351 supports DNP point re-mapping.

CONFIGURATION

To configure a port for DNP, set the port PROTO setting to DNP. Although DNP may be selected on any of the available ports, DNP may not be enabled on more than one port at a time. The following information is required to configure a port for DNP operation:

Label	Description	Default
SPEED	Baud rate (300–38400)	2400
DNPADR	DNP Address (0–65534)	0
ECLASS	Class for event data (0–3)	2
TIMERQ	Time-set request interval (0–32767 min.)	0
DECPLA	Currents scaling (0–3 decimal places)	1
DECPLV	Voltages scaling (0–3 decimal places)	1
DECPLM	Miscellaneous data scaling (0–3 decimal places)	1
STIMEO	Select/operate time-out (0–30 sec.)	1.0
DRETRY	Data link retries (0–15)	3
DTIMEO	Data link time-out (0–5 sec.)	1
MINDLY	Minimum time from DCD to Tx (0–1 sec.)	0.05
MAXDLY	Maximum time from DCD to Tx (0–1 sec.)	0.10
PREDLY	Settle time from RTS on to Tx (OFF,0–30 sec.)	0
PSTDLY	Settle time after Tx to RTS off (0–30 sec.)	0
ANADB	Analog reporting dead band (0–32767 counts)	100
UNSOL	Enable Unsolicited reporting (Y,N)	N
PUNSOL	Enable Unsolicited reporting at power-up (Y,N)	N
REPADR	DNP Address to report to (0–65534)	0
NUMEVE	Number of events to transmit on (1–200)	10
AGEEVE	Age of oldest event to transmit on (0–60 sec.)	2.0
UTIMEO	Unsolicited confirmation timeout (0–50 sec.)	2

The RTS signal may be used to control an external transceiver. The CTS signal is used as a DCD input, indicating when the medium is in use. Transmissions are only initiated if DCD is deasserted. When DCD drops, the next pending outgoing message may be sent once an idle time is satisfied. This idle time is randomly selected between the minimum and maximum allowed idle times (i.e., MAXDLY and MINDLY). In addition, the SEL-351 monitors received data and treats receipt of data as a DCD indication. This allows RTS to be looped back to CTS in cases where the external transceiver does not support DCD. When the SEL-351 transmits a DNP message, it delays transmitting after asserting RTS by at least the time in the PREDLY setting. After transmitting the last byte of the message, the SEL-351 delays for at least PSTDLY milliseconds before deasserting RTS. If the PSTDLY time delay is in progress (RTS still high) following a transmission, and another transmission is initiated, the SEL-351 transmits the message without

completing the PSTDLY delay and without any preceding PREDLY delay. The RTS/CTS handshaking may be completely disabled by setting PREDLY to OFF. In this case, RTS is forced high and CTS is ignored, with only received characters acting as a DCD indication. The timing is the same as above, but PREDLY functions as if it were set to 0, and RTS is not actually deasserted after the PSTDLY time delay expires.

DATA-LINK OPERATION

It is necessary to make two important decisions about the data-link layer operation. One is how to handle data-link confirmation; the other is how to handle data-link access. If a highly reliable communications link exists, the data-link access can be disabled altogether, which significantly reduces communications overhead. Otherwise, it is necessary to enable confirmation and determine how many retries to allow and what the data-link time-out should be. The noisier the communications channel, the more likely a message will be corrupted. Thus, the number of retries should be set higher on noisy channels. Set the data-link time-out long enough to allow for the worst-case response of the master plus transmission time. When the SEL-351 decides to transmit on the DNP link, it has to wait if the physical connection is in use. The SEL-351 monitors physical connections by using CTS input (treated as a Data Carrier Detect) and monitoring character receipt. Once the physical link goes idle, as indicated by CTS being deasserted and no characters being received, the SEL-351 will wait a configurable amount of time before beginning a transmission. This hold-off time will be a random value between the MINDLY and MAXDLY setting values. The hold-off time is random which prevents multiple devices waiting to communicate on the network from continually colliding.

DATA ACCESS METHOD

Based on the capabilities of the system, it is necessary to determine which method is desired to retrieve data on the DNP connection. The following table summarizes the main options, listed from least to most efficient, and corresponding key related settings are indicated.

Table H.1: Data Access Methods

Data Retrieval Method	Description	Relevant SEL-351 Settings
Polled Static	The master polls for static (Class 0) data only.	Set ECLASS = 0, Set UNSOL = N.
Polled Report-by-Exception	The master polls frequently for event data and occasionally for static data.	Set ECLASS to a non-zero value, Set UNSOL = N.
Unsolicited Report-by-Exception	The slave devices send unsolicited event data to the master and the master occasionally sends integrity polls for static data.	Set ECLASS to a non-zero value, Set UNSOL = Y, Set NUMEVE and AGEEVE according to how often messages are desired to be sent.
Quiescent	The master never polls and relies on unsolicited reports only.	Set ECLASS to a non-zero value, Set UNSOL = Y, Set NUMEVE and AGEEVE according to how often messages are desired to be sent.

DEVICE PROFILE

The following is the device profile as specified in the *DNP 3.00 Subset Definitions* document:

<p>DNP 3.00 DEVICE PROFILE DOCUMENT This document must be accompanied by a table having the following headings: Object Group Request Function Codes Response Function Codes Object Variation Request Qualifiers Response Qualifiers Object Name (optional)</p>	
<p>Vendor Name: Schweitzer Engineering Laboratories, Inc.</p>	
<p>Device Name: SEL-351</p>	
<p>Highest DNP Level Supported: For Requests Level 2 For Responses Level 2</p>	<p>Device Function: <input type="checkbox"/> Master <input checked="" type="checkbox"/> Slave</p>
<p>Notable objects, functions, and/or qualifiers supported in addition to the Highest DNP Levels Supported (the complete list is described in the attached table):</p> <p><u>Supports enabling and disabling of unsolicited reports on a class basis.</u></p>	

<p>Expects Binary Input Change Events:</p> <ul style="list-style-type: none"> <input type="checkbox"/> Either time-tagged or non-time-tagged for a single event <input type="checkbox"/> Both time-tagged and non-time-tagged for a single event <input type="checkbox"/> Configurable (attach explanation) 	
<p>FILL OUT THE FOLLOWING ITEMS FOR SLAVE DEVICES ONLY</p>	
<p>Reports Binary Input Change Events when no specific variation requested:</p> <ul style="list-style-type: none"> <input type="checkbox"/> Never <input checked="" type="checkbox"/> Only time-tagged <input type="checkbox"/> Only non-time-tagged <input type="checkbox"/> Configurable to send both, one or the other (attach explanation) 	<p>Reports time-tagged Binary Input Change Events when no specific variation requested:</p> <ul style="list-style-type: none"> <input type="checkbox"/> Never <input checked="" type="checkbox"/> Binary Input Change With Time <input type="checkbox"/> Binary Input Change With Relative Time <input type="checkbox"/> Configurable (attach explanation)
<p>Sends Unsolicited Responses:</p> <ul style="list-style-type: none"> <input type="checkbox"/> Never <input checked="" type="checkbox"/> Configurable (attach explanation) <input type="checkbox"/> Only certain objects <input type="checkbox"/> Sometimes (attach explanation) <input checked="" type="checkbox"/> ENABLE/DISABLE UNSOLICITED <p style="text-align: center;">Function codes supported</p>	<p>Sends Static Data in Unsolicited Responses:</p> <ul style="list-style-type: none"> <input checked="" type="checkbox"/> Never <input type="checkbox"/> When Device Restarts <input type="checkbox"/> When Status Flags Change <p>No other options are permitted.</p>
<p>Default Counter Object/Variation:</p> <ul style="list-style-type: none"> <input type="checkbox"/> No Counters Reported <input type="checkbox"/> Configurable (attach explanation) <input checked="" type="checkbox"/> Default object <u>20</u> <input type="checkbox"/> Default variation <u>6</u> <input type="checkbox"/> Point-by-point list attached 	<p>Counters Roll Over at:</p> <ul style="list-style-type: none"> <input type="checkbox"/> No Counters Reported <input type="checkbox"/> Configurable (attach explanation) <input checked="" type="checkbox"/> 16 Bits <input type="checkbox"/> 32 Bits <input type="checkbox"/> Other Value _____ <input type="checkbox"/> Point-by-point list attached
<p>Sends Multi-Fragment Responses: <input type="checkbox"/> Yes <input checked="" type="checkbox"/> No</p>	

In all cases within the device profile that an item is configurable, it is controlled by SEL-351 settings.

OBJECT TABLE

The supported object, function, and qualifier code combinations are given by the following object table.

Table H.2: SEL-351 DNP Object Table

Object			Request (supported)		Response (may generate)	
Obj	*default Var	Description	Func Codes (dec)	Qual Codes (hex)	Func Codes (dec)	Qual Codes (hex)
1	0	Binary Input—All Variations	1	0,1,6,7,8		
1	1	Binary Input	1	0,1,6,7,8	129	0,1,7,8
1	2*	Binary Input with Status	1	0,1,6,7,8	129	0,1,7,8
2	0	Binary Input Change—All Variations	1	6,7,8		
2	1	Binary Input Change without Time	1	6,7,8	129	17,28
2	2*	Binary Input Change with Time	1	6,7,8	129,130	17,28
2	3	Binary Input Change with Relative Time	1	6,7,8	129	17,28
10	0	Binary Output—All Variations	1	0,1,6,7,8		
10	1	Binary Output				
10	2*	Binary Output Status	1	0,1,6,7,8	129	0,1
12	0	Control Block—All Variations				
12	1	Control Relay Output Block	3,4,5,6	17,28	129	echo of request
12	2	Pattern Control Block				
12	3	Pattern Mask				
20	0	Binary Counter—All Variations	1	0,1,6,7,8		
20	1	32-Bit Binary Counter				
20	2	16-Bit Binary Counter				
20	3	32-Bit Delta Counter				
20	4	16-Bit Delta Counter				
20	5	32-Bit Binary Counter without Flag	1	0,1,6,7,8	129	0,1,7,8
20	6*	16-Bit Binary Counter without Flag	1	0,1,6,7,8	129	0,1,7,8
20	7	32-Bit Delta Counter without Flag				
20	8	16-Bit Delta Counter without Flag				
21	0	Frozen Counter—All Variations				
21	1	32-Bit Frozen Counter				
21	2	16-Bit Frozen Counter				
21	3	32-Bit Frozen Delta Counter				
21	4	16-Bit Frozen Delta Counter				
21	5	32-Bit Frozen Counter with Time of Freeze				
21	6	16-Bit Frozen Counter with Time of Freeze				
21	7	32-Bit Frozen Delta Counter with Time of Freeze				

Object			Request (supported)		Response (may generate)	
Obj	*default Var	Description	Func Codes (dec)	Qual Codes (hex)	Func Codes (dec)	Qual Codes (hex)
21	8	16-Bit Frozen Delta Counter with Time of Freeze				
21	9	32-Bit Frozen Counter without Flag				
21	10	16-Bit Frozen Counter without Flag				
21	11	32-Bit Frozen Delta Counter without Flag				
21	12	16-Bit Frozen Delta Counter without Flag				
22	0	Counter Change Event—All Variations	1	6,7,8		
22	1	32-Bit Counter Change Event without Time	1	6,7,8	129	17,28
22	2*	16-Bit Counter Change Event without Time	1	6,7,8	129,130	17,28
22	3	32-Bit Delta Counter Change Event without Time				
22	4	16-Bit Delta Counter Change Event without Time				
22	5	32-Bit Counter Change Event with Time	1	6,7,8	129	17,28
22	6	16-Bit Counter Change Event with Time	1	6,7,8	129	17,28
22	7	32-Bit Delta Counter Change Event with Time				
22	8	16-Bit Delta Counter Change Event with Time				
23	0	Frozen Counter Event—All Variations				
23	1	32-Bit Frozen Counter Event without Time				
23	2	16-Bit Frozen Counter Event without Time				
23	3	32-Bit Frozen Delta Counter Event without Time				
23	4	16-Bit Frozen Delta Counter Event without Time				
23	5	32-Bit Frozen Counter Event with Time				
23	6	16-Bit Frozen Counter Event with Time				
23	7	32-Bit Frozen Delta Counter Event with Time				
23	8	16-Bit Frozen Delta Counter Event with Time				
30	0	Analog Input—All Variations	1	0,1,6,7,8		
30	1	32-Bit Analog Input	1	0,1,6,7,8	129	0,1,7,8
30	2	16-Bit Analog Input	1	0,1,6,7,8	129	0,1,7,8
30	3	32-Bit Analog Input without Flag	1	0,1,6,7,8	129	0,1,7,8
30	4*	16-Bit Analog Input without Flag	1	0,1,6,7,8	129	0,1,7,8
31	0	Frozen Analog Input—All Variations				
31	1	32-Bit Frozen Analog Input				
31	2	16-Bit Frozen Analog Input				
31	3	32-Bit Frozen Analog Input with Time of Freeze				
31	4	16-Bit Frozen Analog Input with Time of Freeze				
31	5	32-Bit Frozen Analog Input without Flag				
31	6	16-Bit Frozen Analog Input without Flag				
32	0	Analog Change Event—All Variations	1	6,7,8		

Object			Request (supported)		Response (may generate)	
Obj	*default Var	Description	Func Codes (dec)	Qual Codes (hex)	Func Codes (dec)	Qual Codes (hex)
32	1	32-Bit Analog Change Event without Time	1	6,7,8	129	17,28
32	2*	16-Bit Analog Change Event without Time	1	6,7,8	129,130	17,28
32	3	32-Bit Analog Change Event with Time	1	6,7,8	129	17,28
32	4	16-Bit Analog Change Event with Time	1	6,7,8	129	17,28
33	0	Frozen Analog Event—All Variations				
33	1	32-Bit Frozen Analog Event without Time				
33	2	16-Bit Frozen Analog Event without Time				
33	3	32-Bit Frozen Analog Event with Time				
33	4	16-Bit Frozen Analog Event with Time				
40	0	Analog Output Status—All Variations	1	0,1,6,7,8		
40	1	32-Bit Analog Output Status	1	0,1,6,7,8	129	0,1,7,8
40	2*	16-Bit Analog Output Status	1	0,1,6,7,8	129	0,1,7,8
41	0	Analog Output Block—All Variations				
41	1	32-Bit Analog Output Block	3,4,5,6	17,28	129	echo of request
41	2	16-Bit Analog Output Block	3,4,5,6	17,28	129	echo of request
50	0	Time and Date—All Variations				
50	1	Time and Date	1,2	7,8 index = 0	129	07, quantity=1
50	2	Time and Date with Interval				
51	0	Time and Date CTO—All Variations				
51	1	Time and Date CTO				
51	2	Unsynchronized Time and Date CTO				07, quantity=1
52	0	Time Delay—All Variations				
52	1	Time Delay Coarse				
52	2	Time Delay Fine			129	07, quantity=1
60	0	All Classes of Data	1,20,21	6		
60	1	Class 0 Data	1	6		
60	2	Class 1 Data	1,20,21	6,7,8		
60	3	Class 2 Data	1,20,21	6,7,8		
60	4	Class 3 Data	1,20,21	6,7,8		
70	1	File Identifier				
80	1	Internal Indications	2	0,1 index = 7		
81	1	Storage Object				
82	1	Device Profile				
83	1	Private Registration Object				
83	2	Private Registration Object Descriptor				

Object			Request (supported)		Response (may generate)	
Obj	*default Var	Description	Func Codes (dec)	Qual Codes (hex)	Func Codes (dec)	Qual Codes (hex)
90	1	Application Identifier				
100	1	Short Floating Point				
100	2	Long Floating Point				
100	3	Extended Floating Point				
101	1	Small Packed Binary-Coded Decimal				
101	2	Medium Packed Binary-Coded Decimal				
101	3	Large Packed Binary-Coded Decimal				
No object			13,14,23			

DATA MAP

Each version of the SEL-351 has a slightly different data map. The following is the default object map supported by the SEL-351 Connectorized[®] wye-connected PTs (see Table 1.1, Table 9.3, and Appendix A).

Table H.3: SEL-351-Wye DNP Data Map

DNP Object Type	Index	Description
01,02	000–499	Relay Word, where 50B3 is 0 and 67P2S is 343.
01,02	500–999	Relay Word from the SER, encoded same as inputs 000–499 with 500 added.
01,02	1000–1015	Relay front-panel targets, where 1015 is A, 1008 is LO, 1007 is EN and 1000 is 81.
01,02	1016–1019	Power factor leading for A-, B-, C-, and 3-phase.
01,02	1020	Relay Disabled.
01,02	1021	Relay diagnostic failure.
01,02	1022	Relay diagnostic warning.
01,02	1023	New relay event available.
01,02	1024	Settings change or relay restart.
10,12	00–15	Remote bits RB1–RB16
10,12	16	Pulse Open command OC.
10,12	17	Pulse Close command CC.
10,12	18	Reset demands.
10,12	19	Reset demand peaks.
10,12	20	Reset energies.

DNP Object Type	Index	Description
10,12	21	Reset breaker monitor.
10,12	22	Reset front-panel targets.
10,12	23	Read next relay event.
10,12	24–31	Remote bit pairs RB1–RB16.
10,12	32	Open/Close pair OC & CC.
20,22	00	Active settings group.
20,22	01	Internal breaker trips.
20,22	02	External breaker trips.
30,32	00,01	IA magnitude and angle.
30,32	02,03	IB magnitude and angle.
30,32	04,05	IC magnitude and angle.
30,32	06,07	IN magnitude and angle.
30,32	08,09	VA magnitude (kV) and angle.
30,32	10,11	VB magnitude (kV) and angle.
30,32	12,13	VC magnitude (kV) and angle.
30,32	14,15	VS magnitude (kV) and angle.
30,32	16,17	IG magnitude and angle.
30,32	18,19	I1 magnitude and angle.
30,32	20,21	3I2 magnitude and angle.
30,32	22,23	3V0 magnitude (kV) and angle.
30,32	24,25	V1 magnitude (kV) and angle.
30,32	26,27	V2 magnitude (kV) and angle.
30,32	28–31	MW A-, B-, C-, and 3-phase.
30,32	32–35	MVAR A-, B-, C-, and 3-phase.
30,32	36–39	Power factor A-, B-, C-, and 3-phase.
30,32	40	Frequency.
30,32	41	VDC.
30,32	42,43	A-phase MWhr in and out.
30,32	44,45	B-phase MWhr in and out.
30,32	46,47	C-phase MWhr in and out.
30,32	48,49	3-phase MWhr in and out.
30,32	50,51	A-phase MVARhr in and out.
30,32	52,53	B-phase MVARhr in and out.

DNP Object Type	Index	Description
30,32	54,55	C-phase MVARhr in and out.
30,32	56,57	3-phase MVARhr in and out.
30,32	58–63	Demand IA, IB, IC, IN, IG, and 3I2 magnitudes.
30,32	64–67	A-, B-, C-, and 3-phase demand MW in.
30,32	68–71	A-, B-, C-, and 3-phase demand MVAR in.
30,32	72–75	A-, B- C-, and 3-phase demand MW out.
30,32	76–79	A-, B-, C-, and 3-phase demand MVAR out.
30,32	80–85	Peak demand IA, IB, IC, IN, IG, and 3I2 magnitudes.
30,32	86–89	A-, B-, C-, and 3-phase peak demand MW in.
30,32	90–93	A-, B-, C-, and 3-phase peak demand MVAR in.
30,32	94–97	A-, B-, C-, and 3-phase peak demand MW out.
30,32	98–101	A-, B-, C-, and 3-phase peak demand MVAR out.
30,32	102–104	Breaker contact wear percentage (A, B, C).
30	105	Fault type (see table for definition).
30	106	Fault location.
30	107	Fault current.
30	108	Fault frequency.
30	109	Fault settings group.
30	110	Fault recloser shot counter.
30	111–113	Fault time in DNP format (high, middle, and low 16 bits).
40,41	00	Active settings group.

Binary inputs (objects 1 and 2) are supported as defined by the previous table. Binary inputs 0–499 and 1000–1023 are scanned approximately once per second to generate events. When time is reported with these event objects, it is the time at which the scanner observed the bit change. This may be significantly delayed from when the original source change and should not be used for sequence-of-events determination. In order to determine an element's point index, consult the Relay Word Bits table in **Section 9: Setting the Relay** (see Table 9.3). Locate the element in question in the table and note the Relay Word row number. From that row number, subtract the row number of the first Relay Word row (usually 2) and multiply that result by 8. This is the index of the right-most element of the Relay Word row of the element in question. Count over to the original element and add that to get the point index. Binary Inputs 500–999 are derived from the Sequential Events Recorder (SER) and carry the time stamp of actual occurrence. Static reads from these inputs will show the same data as a read from the corresponding index in the 0–499 group. Only points that are actually in the SER list (SET R) will generate events in the 500–999 group.

Analog Input (objects 30 and 32) are supported as defined by the preceding table. The values are reported in primary units. Analog inputs 28–35, 42–57, 64–79, 86–104, and 106 are further

scaled according to the DECPLM setting (e.g., if DECPLM is 3, then the value is multiplied by 1000). Analog inputs 58–63, 80–85, and the even-numbered points in 0–7 and 16–21 (current magnitudes) are scaled according to the DECPLA setting. The even-numbered points in 8–15 and 22–27 (voltage magnitudes) are scaled according to the DECPLV setting. Analog inputs 36–41, 108, and the odd-numbered points in 0–27 (angles) are scaled by 100. The remaining analogs are not scaled. Event-class messages are generated whenever an input changes beyond the value given by the ANADB setting. The dead-band check is done after any scaling is applied. The angles (the odd numbered points in 0–27) will only generate an event if, in addition to their dead-band check, the corresponding magnitude (the preceding point) contains a value greater than the value given by the ANADB setting. Analog inputs are scanned at approximately a 1-second rate, except for analogs 105–113. During a scan, all events generated will use the time the scan was initiated. Analog 105 is a 16-bit composite value, where the upper byte is defined as follows:

Value	Event Cause
1	Trigger command
2	Pulse command
4	Trip element
8	ER element

And the lower byte is defined as follows:

Value	Fault Type
0	Indeterminate
1	A-Phase
2	B-Phase
4	C-Phase
8	Ground

The lower byte may contain any combination of the above bits (e.g., a 6 is a B to C fault and a 9 is an A to Ground fault). If Analog 105 is 0, fault information has not been read and the related analogs (106–113) do not contain valid data.

Control Relay Output Blocks (object 12, variation 1) are supported. The control relays correspond to the remote bits and other functions, as shown above. The Trip/Close bits take precedence over the control field. The control field is interpreted as follows:

Index	Close (0x4X)	Trip (0x8X)	Latch On (3)	Latch Off (4)	Pulse On (1)	Pulse Off (2)
0-15	Set	Clear	Set	Clear	Pulse	Clear
16-23	Pulse	Do nothing	Pulse	Do nothing	Pulse	Do nothing
24	Pulse RB2	Pulse RB1	Pulse RB2	Pulse RB1	Pulse RB2	Pulse RB1
25	Pulse RB4	Pulse RB3	Pulse RB4	Pulse RB3	Pulse RB4	Pulse RB3
26	Pulse RB6	Pulse RB5	Pulse RB6	Pulse RB5	Pulse RB6	Pulse RB5
27	Pulse RB8	Pulse RB7	Pulse RB8	Pulse RB7	Pulse RB8	Pulse RB7
28	Pulse RB10	Pulse RB9	Pulse RB10	Pulse RB9	Pulse RB10	Pulse RB9
29	Pulse RB12	Pulse RB11	Pulse RB12	Pulse RB11	Pulse RB12	Pulse RB11
30	Pulse RB14	Pulse RB13	Pulse RB14	Pulse RB13	Pulse RB14	Pulse RB13
31	Pulse RB16	Pulse RB15	Pulse RB16	Pulse RB15	Pulse RB16	Pulse RB15
32	Pulse CC	Pulse OC	Pulse CC	Pulse OC	Pulse CC	Pulse OC

The Status field is used exactly as defined. All other fields are ignored. A pulse operation asserts a point for a single processing interval. Caution should be exercised with multiple remote bit pulses in a single message (i.e., point count > 1), as this may result in some of the pulse commands being ignored and returning an already active status.

Analog Outputs (objects 40 and 41) are supported as defined by the preceding table. Flags returned with object 40 responses are always set to 0. The Control Status field of object 41 requests are ignored. If the value written to index 0 is outside of the range 1 through 6, the relay will not accept the value and will return a hardware error status.

Relay Summary Event Data

Whenever there is unread relay event summary data (fault data), binary input point 1023 will be set. In order to load the next available relay event summary, the master should pulse binary output point 23. This will cause the event summary analogs (points 105–113) to be loaded with information from next oldest relay event summary. Since the summary data is stored in a first in, first out manner, loading the next event will cause the data from the previous load to be discarded. The event summary analogs will retain this information until the next event is loaded. If no further event summaries are available, attempting to load the next event will cause the event type analog (point 105) to be set to 0.

POINT REMAPPING

The analog and binary input points (objects 1, 2, 30, and 32) may be remapped via the DNP command. The map is composed of 2 lists of indices, one for the analogs (30 and 32) and the other for the binaries (1 and 2). The indices correspond to those given by the relay's default DNP data map. The order they occur in the list determines the index that the corresponding value is reported as to the DNP master. If a value is not in the list, it is not available to the DNP master. All 1025 binaries and 114 analogs may be included in the list, but may occur only once. The maps are stored in nonvolatile memory. The DNP command is only available if DNP has been selected on one of the ports. The DNP command has the following format:

DNP [type]

where type may be A, B, S, T, or omitted.

If the DNP command is issued without parameters, the relay displays both the analog and binary maps, which have the following format:

```
==>DNP<STX>
Analogs = 112 28 17 35 1 56 57 58 59 60 61 62 63 64 65 \
          66 67 100 101 102 103
Binaries = Default Map<ETX>
==>
```

If the DNP command is issued with an S parameter, the relay displays only the analog map; likewise, a T causes the relay to display only the binary map. If the map checksum is determined to be invalid, the map will be reported as corrupted during a display command, as follows:

```
==>DNP T<STX>
Binaries = Map Corrupted<ETX>
==>
```

If the map is determined to be corrupted, DNP will respond to all master data requests with an unknown point error. If the DNP command is issued with an A or B parameter at level 2 or greater, the relay requests the user enter indices for the corresponding list, where a parameter of A specifies the Analog list and B specifies the Binary list. The relay accepts lines of indices until a line without a final continuation character (\) is entered. Each line of input is constrained to 80 characters, but all the points may be re-mapped, using multiple lines with continuation characters (\) at the end of the intermediate lines. If a single blank line is entered as the first line, the re-mapping is disabled for that type (i.e., the relay uses the default analog or binary map). For example, the first example remap could be produced with the following commands:

```
==>DNP A
Enter the new DNP Analog map
112 28 17 \
```

SETTINGS SHEET—DNP PORT—SET P

Protocol (SEL, LMD, DNP)	PROTO = <u> DNP </u>
Baud rate (300,600,1200,2400,4800,9600,19200,38400)	SPEED = <u> </u>
DNP Address (0–65534)	DNPADR = <u> </u>
Class for event data (0 for no event, 1–3)	ECLASS = <u> </u>
Time-set request interval, minutes (0 for never, 1–32767)	TIMERQ = <u> </u>
Currents scaling (0–3 decimal places)	DECPLA = <u> </u>
Voltages scaling (0–3 decimal places)	DECPLV = <u> </u>
Miscellaneous data scaling (0–3 decimal places)	DECPLM = <u> </u>
Select/Operate time-out interval, seconds (0.0–30.0)	STIMEO = <u> </u>
Number of data-link retries (0 for no confirm, 1–15)	DRETRY = <u> </u>
Data Link Time-out interval, seconds (0–5)	DTIMEO = <u> </u>
Minimum Delay from DCD to transmission, seconds (0.00–1.00)	MINDLY = <u> </u>
Maximum Delay from DCD to transmission, seconds (0.00–1.00)	MAXDLY = <u> </u>
Transmission delay from RTS assertion, seconds (OFF,0.00–30.00)	PREDLY = <u> </u>
Post-transmit RTS deassertion delay, seconds (0.00–30.00)	PSTDLY = <u> </u>
Analog reporting dead band, counts (0–32767)	ANADB = <u> </u>
Allow Unsolicited Reporting (Y/N)	UNSOL = <u> </u>
Enable unsolicited messages on power-up (Y/N)	PUNSOL = <u> </u>
Address of master to Report to (0–65534)	REPADR = <u> </u>
Number of events to transmit on (1–200)	NUMEVE = <u> </u>
Age of oldest event to force transmit on, seconds (0.0–60.0)	AGEEVE = <u> </u>
Time-out for confirmation of unsolicited message, seconds (0–50)	UTIMEO = <u> </u>

APPENDIX I: MIRRORED BITS™ (IN FIRMWARE VERSIONS 6 AND 7)

OVERVIEW

MIRRORED BITS is a direct relay-to-relay communications protocol that allows protective relays to exchange information quickly and securely, and with minimal expense. The information exchanged can facilitate remote control, remote sensing, or communications-assisted protection schemes such as POTT, DCB, etc. The SEL-351 supports two MIRRORED BITS channels, differentiated by the channel specifiers A and B. Bits transmitted are called TMB1x through TMB8x, where x is the channel specifier (e.g., A or B), and are controlled by the corresponding SELOGIC control equations. Bits received are called RMB1x through RMB8x and are usable as inputs to any SELOGIC control equations. Channel status bits are called ROKx, RBADx, CBADx and LBOKx and are also usable as inputs to any SELOGIC control equations. Further channel status information is available via the COM command.

Important: Do not connect an unconfigured port to a MIRRORED BITS device. Otherwise, the relay will appear to be locked up. Configure the port first, and then connect the device.

OPERATION

Message Transmission

All messages are transmitted without idle bits between characters. Idle bits are allowed between messages.

- At 4800 baud, one message is transmitted each 1/2 power system cycle.
- At 9600 baud, one message is transmitted each 1/4 power system cycle.
- At 19200 and 38400 baud, one message is transmitted each 1/8 power system cycle for the SEL-321 and 1/4 power system cycle for the SEL-351.

Message Decoding and Integrity Checks

The relay will deassert a user-accessible flag per channel (hereafter called ROKx) upon failing any of the following received-data checks:

- Parity, framing, or overrun errors.
- Receive data redundancy error.
- Receive message identification error.
- No message received in the time three messages have been sent.

While ROKx is not asserted, the relay will:

1. Prevent new data from being transferred to the pickup dropout security counters described later. Instead, the relay will send one of the following user selectable values (hereafter called default values) to the security counter inputs:
 - 1
 - 0
 - The last valid value

The user will be allowed to select one of the default values for each RMB.

2. Enter the synchronization process described below.

The relay will assert ROKx only after successful synchronization as described below and 2 consecutive messages pass all of the data checks described above. After ROKx is reasserted, received data may be delayed while passing through the security counters described below.

Transfer of received data to RMB1x–RMB8x is supervised by 8 user-programmable pickup/dropout security counters settable from 1 (allow every occurrence to pass) to at least 8 (require 8 consecutive occurrences to pass). The pickup and dropout security count settings are separate.

A pickup/dropout security counter operates identically to a pickup/dropout timer, except that it is set in counts of received messages instead of time. An SEL-351 talking to another SEL-351 sends and receives MIRRORRED BITS messages 4 times per power system cycle. Therefore, a security counter set to 2 counts will delay a bit by about 1/2 power system cycle. Things get a little more complicated when two relays of different processing rates are connected via MIRRORRED BITS. For instance an SEL-321 talking to an SEL-351. The SEL-321 processes power system information each 1/8 power system cycle, but processes the pickup/dropout security counters as messages are received. Since the SEL-321 is receiving messages from the SEL-351, it will receive a message per 1/4 cycle processing interval. So a counter set to two will again delay a bit by about 1/2 cycle. However, in that same example, a security counter set to two on the SEL-351 will delay a bit by 1/4 cycle, because the SEL-351 is receiving new MIRRORRED BITS messages each 1/8 cycle from the SEL-321.

Synchronization

When a node detects a communications error, it deasserts ROKx and transmits an attention message, which includes its TX_ID setting.

When a node receives an attention message, it checks to see if its TX_ID is included.

If its own TX_ID is included and at least one other TX_ID is included, the node transmits data.

If its own TX_ID is not included, the node deasserts ROKx, includes its TX_ID in the attention message, and transmits the new attention message.

If its own TX_ID is the only TX_ID included, the relay assumes the message is corrupted unless the loop back mode has been enabled. If loop back is not enabled, the node deasserts ROKx and transmits the attention message with its TX_ID included. If loop back is enabled, the relay transmits data.

In summary, when a node detects an error, it transmits attention until it receives an attention with its own TX_ID included. If three or four relays are connected in a ring topology, then the attention message will go all the way around the loop, and will eventually be received by the originating node. It will then be killed, and data transmission will resume. This method of synchronization allows the relays to reliably determine which byte is the first byte of the message. It also forces mis-synchronized UARTs to become re-synchronized. On the down side, this method takes down the entire loop for a receive error at any node in the loop. This decreases availability. It also makes one-way communications impossible.

Loop-Back Testing

Use the LOOP command to enable loop-back testing.

While in loop-back mode, ROKx is deasserted, and another user accessible flag, LBOKx will assert and deassert based on the received data checks.

Channel Monitoring

Based on the results of data checks described above, the relay will collect information regarding the 255 most recent communications errors. Each record will contain at least the following fields:

- Dropout Time/Date
- Pickup Time/Date
- Time elapsed during dropout
- Reason for dropout (See Message Decoding and Integrity Checks)

Use the COMM command to generate a long or summary report of the communications errors.

There is only a single record for each outage, but an outage can evolve. For example, the initial cause could be a data disagreement, but the outage can be perpetuated by framing errors. If the channel is presently down, the COMM record will only show the initial cause, but the COMM summary will display the present cause of failure.

When the duration of an outage exceeds a user-settable threshold, the relay will assert a user-accessible flag, hereafter called RBADx.

Note: The user will typically combine RBADx with other alarm conditions using SELOGIC control equations.

When channel unavailability exceeds a user-settable threshold, the relay will assert a user accessible flag, hereafter called CBADx.

Note: The user will typically combine CBADx with other alarm conditions using SELOGIC control equations.

MIRRORED BITS PROTOCOL FOR THE PULSAR 9600 BAUD MODEM

The user indicates that a Pulsar MBT modem is to be used by responding "MBT" to the RTS/CTS setting prompt. When the user selects MBT, the baud rate setting will be limited to 9600 baud.

Note: The MBT mode will not work with PROTO = MB8A or MB8B.

The MIRRORED BITS protocol compatible with the Pulsar MBT-9600 modem is identical to the standard MIRRORED BITS protocol with the following exceptions:

The relay injects a delay (idle time) between messages. The length of the delay is one relay processing interval.

Note: An idle processing interval guarantees at least 19 idle bits at 9600 baud in an SEL-321 Relay with the system frequency at 65 Hz.

The relay resets RTS (to a negative voltage at the EIA-232 connector) for MIRRORED BITS communications using this specification. The relay sets RTS (to a positive voltage at the EIA-232 connector) for MIRRORED BITS communications using the R6 or original R version of MIRRORED BITS.

SETTINGS

```

-----
protocol (SEL,LMD,MBA,MBB,MB8A,MB8B)          PROTO = MBA  ?
-----
    
```

Set PROTO = MBA or MB8A to enable the MIRRORED BITS protocol channel A on this port. Set PROTO = MBB or MB8B to enable the MIRRORED BITS protocol channel B on this port. The standard MIRRORED BITS protocols MBA and MBB use a 7-data bit format for data encoding. The MB8 protocols MB8A and MB8B use an 8-data bit format, which allows MIRRORED BITS to operate on communication channels requiring an 8-data bit format. For the remainder of this section, PROTO = MBA is assumed.

```

-----
baud rate (300-38400)                          SPEED = 9600  ?
-----
    
```

Use the SPEED setting to control the rate at which the MIRRORED BITS messages are transmitted, in power system cycles (~), based on the following table:

SPEED	SEL-321	SEL-351
38400	1 message per 1/8 cycle	1 message per 1/4 cycle
19200	1 message per 1/8 cycle	1 message per 1/4 cycle
9600	1 message per 1/4 cycle	1 message per 1/4 cycle
4800	1 message per 1/2 cycle	1 message per 1/2 cycle

```
enable hardware handshaking (Y,N,MBT)          RTSCTS= N    ?
```

Use the MBT option if you are using a Pulsar MBT 9600 baud modem. With this option set, the relay will transmit a message every 1/2 power system cycle and the relay will deassert the RTS signal on the EIA-232 connector. Also, the relay will monitor the CTS signal on the EIA-232 connector, which the modem will deassert if the channel has too many errors. The modem uses the relay's RTS signal to determine whether the new or old MIRRORED BITS protocol is in use.

```
Mirrored Bits Receive bad pickup (1- 10000 sec)  RBADPU= 60    ?
```

Use the RBADPU setting to determine how long a channel error must last before the relay element RBADA is asserted. RBADA is deasserted when the channel error is corrected. RBADPU is accurate to ±1 second.

```
Mirrored Bits Channel bad pickup (1- 10000 10E-6) CBADPU= 1000  ?
```

Use the CBADPU setting to determine the ratio of channel down time to the total channel time before the relay element CBADA is asserted. The time used in the calculation are those that are available in the COMM records. See the COMM command in the 321 or 351 manuals for a description of the COMM records.

```
Mirrored Bits transmit identifier(1 - 4)         TX_ID = 1    ?
Mirrored Bits receive identifier(1 - 4)          RX_ID = 2    ?
```

Set the RX_ID of the local relay to match the TX_ID of the remote relay. For example, in the three-terminal case, where Relay X transmits to Relay Y, Relay Y transmits to Relay Z, and Relay Z transmits to Relay X:

	TX_ID	RX_ID
Relay X	1	3
Relay Y	2	1
Relay Z	3	2

```
Mirrored Bits receive default state (string of 1s, 0s or Xs)
87654321
RXDFLT=00000X11
?
```

Use the RXDFLT setting to determine the default state the MIRRORED BITS should use in place of received data if an error condition is detected. The setting is a mask of 1s, 0s and/or Xs, for RMB1A-RMB8A, where X represents the most recently received valid value.

Mirrored Bits RMB_ Debounce PU msgs (1-8)	RMB1PU= 1	?
Mirrored Bits RMB_ Debounce DO msgs (1-8)	RMB1DO= 1	?
Mirrored Bits RMB_ Debounce PU msgs (1-8)	RMB2PU= 1	?
Mirrored Bits RMB_ Debounce DO msgs (1-8)	RMB2DO= 1	?
Mirrored Bits RMB_ Debounce PU msgs (1-8)	RMB3PU= 1	?
Mirrored Bits RMB_ Debounce DO msgs (1-8)	RMB3DO= 1	?
Mirrored Bits RMB_ Debounce PU msgs (1-8)	RMB4PU= 1	?
Mirrored Bits RMB_ Debounce DO msgs (1-8)	RMB4DO= 1	?
Mirrored Bits RMB_ Debounce PU msgs (1-8)	RMB5PU= 1	?
Mirrored Bits RMB_ Debounce DO msgs (1-8)	RMB5DO= 1	?
Mirrored Bits RMB_ Debounce PU msgs (1-8)	RMB6PU= 1	?
Mirrored Bits RMB_ Debounce DO msgs (1-8)	RMB6DO= 1	?
Mirrored Bits RMB_ Debounce PU msgs (1-8)	RMB7PU= 1	?
Mirrored Bits RMB_ Debounce DO msgs (1-8)	RMB7DO= 1	?
Mirrored Bits RMB_ Debounce PU msgs (1-8)	RMB8PU= 1	?
Mirrored Bits RMB_ Debounce DO msgs (1-8)	RMB8DO= 1	?

Supervise the transfer of received data (or default data) to RMB1A–RMB8A with the **MIRRORED BITS** pickup and dropout security counters. Set the pickup and dropout counters individually for each bit.

Settings Sheet—MIRRORED BITS—SET P

Baud Rate (300–38400)	SPEED = _____
Enable Hardware Handshaking (Y,N,MBT)	RTSCTS = _____
Seconds to MIRRORED BITS Rx Bad Pickup (1–10000)	RBADPU = _____
PPM MIRRORED BITS Channel Bad Pickup (1–10000)	CBADPU = _____
MIRRORED BITS Receive Identifier (1–4)	RXID = _____
MIRRORED BITS Transmit Identifier (1–4)	TXID = _____
MIRRORED BITS Receive Default State (string of 1s, 0s, or Xs)	RXDFLT = _____
MIRRORED BITS RMB_Pickup Debounce msgs (1–8)	RMB1PU = _____
MIRRORED BITS RMB_Dropout Debounce msgs (1–8)	RMB1DO = _____
MIRRORED BITS RMB_Pickup Debounce msgs (1–8)	RMB2PU = _____
MIRRORED BITS RMB_Dropout Debounce msgs (1–8)	RMB2DO = _____
MIRRORED BITS RMB_Pickup Debounce msgs (1–8)	RMB3PU = _____
MIRRORED BITS RMB_Dropout Debounce msgs (1–8)	RMB3DO = _____
MIRRORED BITS RMB_Pickup Debounce msgs (1–8)	RMB4PU = _____
MIRRORED BITS RMB_Dropout Debounce msgs (1–8)	RMB4DO = _____
MIRRORED BITS RMB_Pickup Debounce msgs (1–8)	RMB5PU = _____
MIRRORED BITS RMB_Dropout Debounce msgs (1–8)	RMB5DO = _____
MIRRORED BITS RMB_Pickup Debounce msgs (1–8)	RMB6PU = _____
MIRRORED BITS RMB_Dropout Debounce msgs (1–8)	RMB6DO = _____
MIRRORED BITS RMB_Pickup Debounce msgs (1–8)	RMB7PU = _____
MIRRORED BITS RMB_Dropout Debounce msgs (1–8)	RMB7DO = _____
MIRRORED BITS RMB_Pickup Debounce msgs (1–8)	RMB8PU = _____
MIRRORED BITS RMB_Dropout Debounce msgs (1–8)	RMB8DO = _____

APPENDIX J: SEL-351 UNSOLICITED SER PROTOCOL

INTRODUCTION

This appendix describes special binary Sequential Events Recorder (SER) messages that are not included in *Section 10: Serial Port Communications and Commands* of the instruction manual. Devices with embedded processing capability can use these messages to enable and accept unsolicited binary SER messages from the SEL-351 Relay.

SEL relays and communications processors have two separate data streams that share the same serial port. The normal serial interface consists of ASCII character commands and reports that are intelligible to people using a terminal or terminal emulation package. The binary data streams can interrupt the ASCII data stream to obtain information, and then allow the ASCII data stream to continue. This mechanism allows a single communications channel to be used for ASCII communications (e.g., transmission of a long event report) interleaved with short bursts of binary data to support fast acquisition of metering or SER data. To exploit this feature, the device connected to the other end of the link requires software that uses the separate data streams. The binary commands and ASCII commands can also be accessed by a device that does not interleave the data streams.

MAKE SEQUENTIAL EVENTS RECORDER (SER) SETTINGS WITH CARE

The relay triggers a row in the Sequential Events Recorder (SER) event report for any change of state in any one of the elements listed in the SER1, SER2, or SER3 trigger settings. Nonvolatile memory is used to store the latest 512 rows of the SER event report so they can be retained during power loss. The nonvolatile memory is rated for a finite number of "writes." Exceeding the limit can result in an EEPROM self-test failure. An average of four state changes per minute can be made for a 25-year relay service life.

RECOMMENDED MESSAGE USAGE

Use the following sequence of commands to enable unsolicited binary SER messaging in the SEL-351 Relay:

1. On initial connection, send the SNS command to retrieve and store the ASCII names for the digital I/O points assigned to trigger SER records. The order of the ASCII names matches the point indices in the unsolicited binary SER messages. Send the "Enable Unsolicited Data Transfer" message to enable the SEL-351 Relay to transmit unsolicited binary SER messages.
2. When SER records are triggered in the SEL-351, the relay responds with an unsolicited binary SER message. If this message has a valid checksum, it must be acknowledged by sending an acknowledge message with the same response number as contained in the original message. The relay will wait approximately 100 ms to 500 ms to receive an acknowledge message, at which time the relay will resend the same unsolicited SER message with the same response number.

3. Upon receiving an acknowledge message with a matching response number, the relay increments the response number, and continues to send and seek acknowledgment for unsolicited SER messages, if additional SER records are available. When the response number reaches three it wraps around to zero on the next increment.

FUNCTIONS AND FUNCTION CODES

In the messages shown below, all numbers are in hexadecimal unless otherwise noted.

01—Function Code: Enable Unsolicited Data Transfer, Sent From Master to Relay

Upon power-up, the SEL-351 Relay disables its own unsolicited transmissions. This function enables the SEL-351 Relay to begin sending unsolicited data to the device which sent the enable message, if the SEL-351 has such data to transfer. The message format for function code 01 is shown below.

<u>Data</u>	<u>Description</u>
A546	Message header
12	Message length in bytes (18 decimal)
0000000000	Five bytes reserved for future use as a routing address
YY	Status byte (LSB = 1 indicates an acknowledge is requested)
01	Function code
C0	Sequence byte (Always C0. Other values are reserved for future use in multiple frame messages.)
XX	Response number (XX = 00, 01, 02, 03, 00, 01...).
18	Function to enable (18—unsolicited SER messages)
0000	Reserved for future use as function code data
nn	Maximum number of SER records per message, 01–20 hex
cccc	Two byte CRC-16 check code for message

The SEL-351 Relay verifies the message by checking the header, length, function code, and enabled function code against the expected values. It also checks the entire message against the CRC-16 field. If any of the checks fail, except the function code or the function to enable, the message is ignored.

If an acknowledge is requested as indicated by the least significant bit of the status byte, the relay transmits an acknowledge message with the same response number received in the enable message.

The “nn” field is used to set the maximum number of SER records per message. The relay checks for SER records approximately every 500 ms. If there are new records available, the relay immediately creates a new unsolicited SER message and transmits it. If there are more than “nn” new records available, or if the first and last record are separated by more than 16 seconds, the relay will break the transmission into multiple messages so that no message contains more than “nn” records, and the first and last record of each message are separated by no more than 16 seconds.

If the function to enable is not 18 or the function code is not recognized, the relay responds with an acknowledge message containing a response code 01 (function code unrecognized), and no functions are enabled. If the SER triggers are disabled (SER1, SER2, and SER3 are all set to NA), the unsolicited SER messages are still enabled, but the only SER records generated are due

to settings changes, and power being applied to the relay. If the SER1, SER2, or SER3 settings are subsequently changed to any non-NA value and SER entries are triggered, unsolicited SER messages will be generated with the new SER records.

02—Function Code: Disable Unsolicited Data Transfer, Sent From Master to Relay

This function disables the SEL-351 Relay from transferring unsolicited data. The message format for function code 02 is shown below.

<u>Data</u>	<u>Description</u>
A546	Message header
10	Message length (16 decimal)
0000000000	Five bytes reserved for future use as a routing address.
YY	Status byte (LSB = 1 indicates an acknowledge is requested)
02	Function code
C0	Sequence byte (Always C0. Other values are reserved for future use in multiple frame messages.)
XX	Response number (XX = 00, 01, 02, 03, 01, 02...)
18	Function to disable (18 = Unsolicited SER)
00	Reserved for future use as function code data
cccc	Two byte CRC-16 check code for message

The SEL-351 Relay verifies the message by checking the header, length, function code, and disabled function code against the expected values, and checks the entire message against the CRC-16 field. If any of the checks fail, except the function code or the function to disable, the message is ignored.

If an acknowledge is requested as indicated by the least significant bit of the status byte, the relay transmits an acknowledge message with the same response number received in the enable message.

If the function to disable is not 18 or the function code is not recognized, the relay responds with an acknowledge message containing the response code 01 (function code unrecognized) and no functions are disabled.

18—Function: Unsolicited SER Response, Sent From Relay to Master

The function 18 is used for the transmission of unsolicited Sequential Events Recorder (SER) data from the SEL-351 Relay. This function code is also passed as data in the “Enable Unsolicited Data Transfer” and the “Disable Unsolicited Data Transfer” messages to indicate which type of unsolicited data should be enabled or disabled. The message format for function code 18 is shown below.

<u>Data</u>	<u>Description</u>
A546	Message header
ZZ	Message length (Up to 34 + 4 · nn decimal, where nn is the maximum number of SER records allowed per message as indicated in the “Enable Unsolicited Data Transfer” message.)
0000000000	Five bytes reserved for future use as a routing address.
YY	Status Byte (01 = need acknowledgment; 03 = settings changed and need acknowledgment. If YY=03, the master should re-read the SNS data because the element index list may have changed.)
18	Function code
C0	Sequence byte (Always C0. Other values are reserved for future use in multiple frame messages.)
XX	Response number (XX = 00, 01, 02, 03, 01, 02...)
00000000	Four bytes reserved for future use as a return routing address.
dddd	Two-byte day of year (1–366)
yyyy	Two-byte, four-digit year (e.g., 1999 or 07CF hex)
mmmmmmmm	Four-byte time of day in milliseconds since midnight
XX	1st element index (match with the response to the SNS command; 00 for 1st element, 01 for second element, and so on)
uuuuuu	Three-byte time tag offset of 1st element in microseconds since time indicated in the time of day field.
XX	2nd element index
uuuuuu	Three-byte time tag offset of 2nd element in microseconds since time indicated in the time of day field.
.	
.	
.	
xx	last element index
uuuuuu	Three-byte time tag offset of last element in microseconds since time indicated in the time of day field.
FFFFFFFE	Four-byte end-of-records flag
sssssss	Packed four-byte element status for up to 32 elements (LSB for the 1st element)
cccc	Two-byte CRC-16 checkcode for message

If the relay determines that SER records have been lost, it sends a message with the following format:

<u>Data</u>	<u>Description</u>
A546	Message header
22	Message length (34 decimal)
0000000000	Five bytes reserved for future use as a routing address.
YY	Status Byte (01 = need acknowledgement; 03 = settings changed and need acknowledgement)
18	Function code
C0	Sequence byte (Always C0. Other values are reserved for future use in multiple frame messages.)
XX	Response number (XX = 00, 01, 02, 03, 00, 01, ...)
00000000	Four bytes reserved for future use as a return routing address.
dddd	Two-byte day of year (1–366) of overflow message generation

yyyy	Two-byte, four-digit year (e.g., 1999 or 07CF hex) of overflow message generation.
mmmmmmmm	Four-byte time of day in milliseconds since midnight
FFFFFFFE	Four-byte end-of-records flag
00000000	Element status (unused)
cccc	Two byte CRC-16 checkcode for message

Acknowledge Message Sent from Master to Relay, and From Relay to Master

The acknowledge message is constructed and transmitted for every received message which contains a status byte with the LSB set (except another acknowledge message), and which passes all other checks, including the CRC. The acknowledge message format is shown below.

<u>Data</u>	<u>Description</u>
A546	Message header
0E	Message length (14 decimal)
0000000000	Five bytes reserved for future use as a routing address.
00	Status byte (always 00)
XX	Function code, echo of acknowledged function code with MSB set.
RR	Response code (see below)
XX	Response number (XX = 00, 01, 02, 03, 00, 01, ...) must match response number from message being acknowledged.)
cccc	Two byte CRC-16 checkcode for message

The SEL-351 supports the following response codes:

RR	Response
00	Success.
01	Function code not recognized.

Examples

- Successful acknowledge for “Enable Unsolicited Data Transfer” message from a relay with at least one of SER1, SER2, or SER3 not set to NA:
A5 46 0E 00 00 00 00 00 81 00 XX cc cc
(XX is as same as the Response Number in the “Enable Unsolicited Data Transfer” message to which it responds)
- Unsuccessful acknowledge for “Enable Unsolicited Data Transfer” message from a relay with all of SER1, SER2, and SER3 set to NA:
A5 46 0E 00 00 00 00 00 81 02 XX cc cc
(XX is as same as the response number in the “Enable Unsolicited Data Transfer” message to which it responds.)
- Disable Unsolicited Data Transfer message, acknowledge requested:
A5 46 10 00 00 00 00 01 02 C0 XX 18 00 cc cc
(XX = 0, 1, 2, 3)

4. Successful acknowledge from the relay for the “Disable Unsolicited Data Transfer” message:
A5 46 0E 00 00 00 00 00 82 00 XX cc cc
(XX is as same as the response number in the “Disable Unsolicited Data Transfer” message to which it responds.)

5. Successful acknowledge message from the master for an unsolicited SER message:
A5 46 0E 00 00 00 00 00 98 00 XX cccc
(XX is as same as the response number in the unsolicited SER message to which it responds.)

Notes:

Once the relay receives an acknowledge with response code 00 from the master, it will clear the settings changed bit (bit 1) in its status byte, if that bit is asserted, and it will clear the settings changed bit in fast meter, if that bit is asserted.

An element index of FE indicates that the SER record is due to power up. An element index of FF indicates that the SER record is due to setting change. An element index of FD indicates that the element identified in this SER record is no longer in the SER trigger settings.

When the relay sends an SER message packet, it will put a sequential number (0, 1, 2, 3, 0, 1, ...) into the response number. If the relay does not receive an acknowledge from the master before approximately 500 mS, the relay will resend the same message packet with the same response number until it receives an acknowledge message with that response number. For the next SER message, the relay will increment the response number (it will wrap around to zero from three).

A single SER message packet from the relay can have a maximum number 32 records and the data may span a time period of no more than 16 seconds. The master may limit the number records in a packet with the third byte of function code data in the “Enable Unsolicited Data Transfer” message (function code 01). The relay may generate an SER packet that with less than the requested number of records, if the record time stamps span more than 16 seconds.

The relay always requests acknowledgment in unsolicited SER messages (LSB of the status byte is set).

Unsolicited SER messages can be enabled on multiple ports simultaneously.

APPENDIX K: SEL-5030 ACSELERATOR™

INTRODUCTION

The SEL-5030 ACSELERATOR is an easy-to-use yet powerful tool to help get the most out of your SEL-351-5, -6, -7 Relay.

Using the SEL-5030 ACSELERATOR, you will be able to:

- Create, test, and manage settings with a Windows® interface.
- Visually design SELOGIC® control equations with a powerful Logic Editor.
- Verify SELOGIC control equations with an integrated Logic Simulator.
- Analyze power system events from SEL relays with integrated Waveform and Harmonic Analysis tools.
- Communicate with SEL devices via an HMI interface with integrated Meter and Control functions.
- Create, manage, copy, merge, and read relay settings with a settings database manager.

This document gives instructions for installing the SEL-5030 ACSELERATOR. A Quick Tour guide is available as part of the online help. After installation, the Quick Tour will show how to create a circuit breaker (CB) simulator. The CB simulator is useful for testing and evaluation.

Note 1: Like all SEL relay products, the SEL-351-5, -6, -7 can also be set and operated by a simple ASCII terminal.

Note 2: Using SEL-5030 ACSELERATOR Software in SEL-351-5, -6, -7 Relays requires relay Firmware Version R306 or later.

ACSELERATOR SYSTEM REQUIREMENTS

CPU: Pentium class (recommended 90 MHz or faster)

Operating System: Windows 95/98 with 16 MB ram (32 MB ram recommended)
Windows NT4 SP3 or later with 32 MB ram (64 MB ram recommended)
Windows 2000 with 64 MB ram

Disk Space: 25 Mb

Communications: EIA-232 serial port for communicating with the relay

CD drive: required for installation

INSTALLATION

Note: Your PC must be restarted after the installation for the changes to take effect.

To install the ACSELERATOR software, perform the following steps.

1. Close all other software applications on your PC.
2. Insert the ACSELERATOR software CD into your PC's CD-ROM drive. The installation program should start automatically. If the install program does not start, select Run from the windows start menu and type in the following command **D:\SETUP** (substitute D:\ with your PC's CD-ROM drive letter).
3. Follow the steps that appear on the screen. The installation program will perform all the necessary steps to load the ACSELERATOR software onto your PC.

It is necessary to have the correct comctl32.dll file installed on your computer in order to see the toolbar buttons. If you do not see the toolbar buttons, run the 40ComUpd.exe, located in the install directory. This file will install the proper windows system drivers.

STARTING ACSELERATOR

You can start ACSELERATOR the following ways:

1. Double-click the ACSELERATOR icon if you have a desktop shortcut.
2. Choose "Programs | SEL Applications" and select the ACSELERATOR icon to start the program.

SEL-351-5, -6, -7 RELAY COMMAND SUMMARY

<u>Access Level 0 Command</u>	Access Level 0 is the initial relay access level. The relay automatically returns to Access Level 0 when a serial port time-out setting expires or after a QUIT command. The screen prompt is: =
ACC	Enter Access Level 1. If the main board password jumper is not in place, the relay prompts the user for the Access Level 1 password in order to enter Access Level 1.
<u>Access Level 1 Commands</u>	The Access Level 1 commands allow the user to look at settings information and not change it, and to retrieve and reset event, recorder, and metering data. The screen prompt is: =>
2AC	Enter Access Level 2. If the main board password jumper is not in place, the relay prompts for the entry of the Access Level 2 password in order to enter Access Level 2.
BAC	Enter Breaker Access Level (Access Level B). If the main board password jumper is not in place, the relay prompts the user for the Access Level B password.
BRE	Display breaker monitor data (trips, interrupted current, wear).
COM ¹ p	Show communications summary report (COM report) on MIRRORED BITS™ channel p (where p = A or B) using all failure records in the channel calculations.
COM ¹ p n	Show a COM report for MIRRORED BITS channel p using the latest n failure records (n = 1–512, where 1 is the most recent entry).
COM ¹ p m n	Show COM report for MIRRORED BITS channel p using failure records m through n (m = 1–512).
COM ¹ p d1	Show COM report for MIRRORED BITS channel p using failures recorded on date d1 (see DAT command for date format).
COM ¹ p d1 d2	Show COM report for MIRRORED BITS channel p using failures recorded between dates d1 and d2 inclusive.
COM ¹ ... L	For all COM commands, L causes the specified COM report records to be listed after the summary.
COM ¹ p C	Clears communications records for MIRRORED BITS channel p (or both channels if p is not specified, COM C command).
DAT	Show date.
DAT mm/dd/yy	Enter date in this manner if global Date Format setting, DATE_F, is set to MDY.
DAT yy/mm/dd	Enter date in this manner if global Date Format setting, DATE_F, is set to YMD.
EVE n	Show event report n with 4 samples per cycle (n = 1 to highest numbered event report, where 1 is the most recent report: see HIS command). If n is omitted, (EVE command) most recent report is displayed.
EVE n R	Show event report n in raw (unfiltered) format with 16 samples per cycle resolution.
EVE n C	Show event report n in compressed ASCII format for use with the SEL-5601 Analytic Assistant.
EVE n A	Show event report n with analog section only.
EVE n D	Show event report n with digital section only.
EVE n M	Show event report n with communications section only.
EVE n Sx	Show event report n with x samples per cycle (x = 4 or 16).
EVE n L	Show event report n with 16 samples per cycle (similar to EVE n S16).
EVE n Ly	Show first y cycles of event report n (y = 1 to global setting LER).
GRO	Display active group number.

HIS n	Show brief summary of n latest event reports, where 1 is the most recent entry. If n is not specified, (HIS command) all event summaries are displayed.
HIS C	Clear all event reports from nonvolatile memory.
IRI	Force synchronization attempt of internal relay clock to IRIG-B time-code input.
LDP ¹	Show entire Load Profile (LDP) report.
LDP ¹ n	Show latest n rows in the LDP report (n = 1 to several thousand, where 1 is the most recent entry).
LDP ¹ m n	Show rows m through n in the LDP report (m = 1 to several thousand).
LDP ¹ d1	Show all rows in the LDP report recorded on the specified date (see DAT command for date format).
LDP ¹ d1 d2	Show all rows in the LDP report recorded between dates d1 and d2, inclusive.
LDP ¹ D	Display the number of days of LDP storage capacity before data overwrite will occur.
LDP ¹ C	Clears the LDP report from nonvolatile memory.
MET k	Display instantaneous metering data. Enter k for repeat count (k = 1–32767, if not specified, default is 1).
MET X k	Display same data as MET command with phase-to-phase voltages and Vbase. Enter k for repeat count (k=1–32767, if not specified default is 1)
MET D	Display demand and peak demand data. Select MET RD or MET RP to reset.
MET E	Display energy metering data. Select MET RE to reset.
MET M	Display maximum/minimum metering data. Select MET RM to reset.
QUI	Quit. Returns to Access Level 0. Terminates SEL Distributed Port Switch Protocol (LMD) connection.
SER	Show entire Sequential Events Recorder (SER) report.
SER n	Show latest n rows in the SER report (n = 1–512, where 1 is the most recent entry).
SER m n	Show rows m through n in the SER report (m = 1–512).
SER d1	Show all rows in the SER report recorded on the specified date (see DAT command for date format).
SER d1 d2	Show all rows in the SER report recorded between dates d1 and d2, inclusive.
SER C	Clears SER report from nonvolatile memory.
SHO n	Show relay settings (overcurrent, reclosing, timers, etc.) for group n (n = 1–6, if not specified, default is active setting group).
SHO n L	Show SELOGIC [®] Control Equation settings for group n (n = 1–6, if not specified, default is the SELOGIC Control Equations for the active setting group).
SHO G	Show global settings.
SHO R	Show SER and LDP Recorder ¹ settings.
SHO T	Show text label settings.
SHO P p	Show serial port p settings, (p = 1, 2, 3, or F; if not specified, default is active port).
SHO ... name	For all SHO commands, jump ahead to specific setting by entering setting name.
SSI ²	Show entire Voltage Sag/Swell/Interruption (SSI) report.
SSI ² n	Show latest n rows in SSI report (n = 1 to several thousand, where 1 is the most recent entry).
SSI ² m n	Show rows m through n in SSI report (m = 1 to several thousand).
SSI ² d1	Show all rows in SSI report recorded on the specified date (see DAT command for date format).
SSI ² d1 d2	Show all rows in SSI report recorded between dates d1 and d2, inclusive.

SSI ² C	Clears SSI report from nonvolatile memory.
SSI ² R	Resets Vbase element. See Vbase initialization.
SSI ² T	Trigger the SSI recorder.
STA	Show relay self-test status.
TAR R	Reset front-panel tripping targets.
TAR n k	Display Relay Word row. If n = 0–56, display row n. If n is an element name (e.g., 50A1) display row containing element n. Enter k for repeat count (k = 1–32767, if not specified, default is 1).
TIM	Show or set time (24 hour time). Show current relay time by entering TIM. Set the current time by entering TIM followed by the time of day (e.g., set time 22:47:36 by entering TIM 22:47:36).
TRI	Trigger an event report.
<u>Access Level B Commands</u>	Access Level B commands primarily allow the user to operate the breaker and output contacts. All Access Level 1 commands can also be executed from Access Level B. The screen prompt is: ==>
BRE n	Enter BRE W to preload breaker wear. Enter BRE R to reset breaker monitor data.
CLO	Close circuit breaker (assert Relay Word bit CC).
GRO n	Change active group to group n (n = 1–6).
OPE	Open circuit breaker (assert Relay Word bit OC).
PUL n k	Pulse output contact n (where n is one of ALARM, OUT101–OUT107, OUT201–OUT212) for k seconds. Specify parameter n; k = 1–30 seconds; if not specified, default is 1.
<u>Access Level 2 Commands</u>	The Access Level 2 commands allow unlimited access to relay settings, parameters, and output contacts. All Access Level 1 and Access Level B commands are available from Access Level 2. The screen prompt is: ==>
CON n	Control Relay Word bit RBn (Remote Bit n; n = 1–16). Execute CON n and the relay responds: CONTROL RBn. Then reply with one of the following: SRB n set Remote Bit n (assert RBn). CRB n clear Remote Bit n (deassert RBn). PRB n pulse Remote Bit n [assert RBn for 1/4 cycle].
COP m n	Copy relay and logic settings from group m to group n (m and n are numbers 1–6).
LOO ¹ p t	Set MIRRORING BITS port p to loopback (p = A or B). The received MIRRORING BITS elements are forced to default values during the loopback test; t specifies the loopback duration in minutes (t = 1–5000, default is 5).
LOO ¹ p DATA	Set MIRRORING BITS port p to loopback. DATA allows the received MIRRORING BITS elements to change during the loopback test.
PAS	Show existing Access Level 1, Level B, and Level 2 passwords.
PAS 1 xxxxxx	Change Access Level 1 password to xxxxxx.
PAS B xxxxxx	Change Access Level B password to xxxxxx.
PAS 2 xxxxxx	Change Access Level 2 password to xxxxxx.
	Entering DISABLE as the password disables the password requirement for the specified access level.

SET n	Change relay settings (overcurrent, reclosing, timers, etc.) for group n (n = 1–6, if not specified, default is active setting group).
SET n L	Change SELOGIC Control Equation settings for group n (n = 1–6, if not specified, default is the SELOGIC Control Equations for the active setting group).
SET G	Change global settings.
SET R	Change SER and LDP Recorder ¹ settings.
SET T	Change text label settings.
SET P p	Change serial port p settings, (p = 1, 2, 3, or F; if not specified, default is active port).
SET ... name	For all SET commands, jump ahead to specific setting by entering setting name.
SET ... TERSE	For all SET commands, TERSE disables the automatic SHO command after settings entry.
STA C	Resets self-test warnings/failures and reboots the relay.
VER	Show relay configuration and firmware version.

Key Stroke Commands

Ctrl - Q	Send XON command to restart communications port output previously halted by XOFF.
Ctrl - S	Send XOFF command to pause communications port output.
Ctrl - X	Send CANCEL command to abort current command and return to current access level prompt.

Key Stroke Commands when using SET command

<ENTER>	Retains setting and moves on to next setting.
^ <ENTER>	Returns to previous setting.
< <ENTER>	Returns to previous setting section.
> <ENTER>	Skips to next setting section.
END <ENTER>	Exits setting editing session, then prompts user to save settings.
Ctrl - X	Aborts setting editing session without saving changes.

¹ Available in firmware versions 6 and 7.

² Available in firmware version 7.

SEL-351-5, -6, -7 RELAY COMMAND SUMMARY

<u>Access Level 0 Command</u>	Access Level 0 is the initial relay access level. The relay automatically returns to Access Level 0 when a serial port time-out setting expires or after a QUIT command. The screen prompt is: =
ACC	Enter Access Level 1. If the main board password jumper is not in place, the relay prompts the user for the Access Level 1 password in order to enter Access Level 1.
<u>Access Level 1 Commands</u>	The Access Level 1 commands allow the user to look at settings information and not change it, and to retrieve and reset event, recorder, and metering data. The screen prompt is: =>
2AC	Enter Access Level 2. If the main board password jumper is not in place, the relay prompts for the entry of the Access Level 2 password in order to enter Access Level 2.
BAC	Enter Breaker Access Level (Access Level B). If the main board password jumper is not in place, the relay prompts the user for the Access Level B password.
BRE	Display breaker monitor data (trips, interrupted current, wear).
COM ¹ p	Show communications summary report (COM report) on MIRRORED BITS™ channel p (where p = A or B) using all failure records in the channel calculations.
COM ¹ p n	Show a COM report for MIRRORED BITS channel p using the latest n failure records (n = 1–512, where 1 is the most recent entry).
COM ¹ p m n	Show COM report for MIRRORED BITS channel p using failure records m through n (m = 1–512).
COM ¹ p d1	Show COM report for MIRRORED BITS channel p using failures recorded on date d1 (see DAT command for date format).
COM ¹ p d1 d2	Show COM report for MIRRORED BITS channel p using failures recorded between dates d1 and d2 inclusive.
COM ¹ ... L	For all COM commands, L causes the specified COM report records to be listed after the summary.
COM ¹ p C	Clears communications records for MIRRORED BITS channel p (or both channels if p is not specified, COM C command).
DAT	Show date.
DAT mm/dd/yy	Enter date in this manner if global Date Format setting, DATE_F, is set to MDY.
DAT yy/mm/dd	Enter date in this manner if global Date Format setting, DATE_F, is set to YMD.
EVE n	Show event report n with 4 samples per cycle (n = 1 to highest numbered event report, where 1 is the most recent report: see HIS command). If n is omitted, (EVE command) most recent report is displayed.
EVE n R	Show event report n in raw (unfiltered) format with 16 samples per cycle resolution.
EVE n C	Show event report n in compressed ASCII format for use with the SEL-5601 Analytic Assistant.
EVE n A	Show event report n with analog section only.
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GRO	Display active group number.

HIS n	Show brief summary of n latest event reports, where 1 is the most recent entry. If n is not specified, (HIS command) all event summaries are displayed.
HIS C	Clear all event reports from nonvolatile memory.
IRI	Force synchronization attempt of internal relay clock to IRIG-B time-code input.
LDP ¹	Show entire Load Profile (LDP) report.
LDP ¹ n	Show latest n rows in the LDP report (n = 1 to several thousand, where 1 is the most recent entry).
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LDP ¹ d1	Show all rows in the LDP report recorded on the specified date (see DAT command for date format).
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MET k	Display instantaneous metering data. Enter k for repeat count (k = 1–32767, if not specified, default is 1).
MET X k	Display same data as MET command with phase-to-phase voltages and Vbase. Enter k for repeat count (k=1–32767, if not specified default is 1)
MET D	Display demand and peak demand data. Select MET RD or MET RP to reset.
MET E	Display energy metering data. Select MET RE to reset.
MET M	Display maximum/minimum metering data. Select MET RM to reset.
QUI	Quit. Returns to Access Level 0. Terminates SEL Distributed Port Switch Protocol (LMD) connection.
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SER d1	Show all rows in the SER report recorded on the specified date (see DAT command for date format).
SER d1 d2	Show all rows in the SER report recorded between dates d1 and d2, inclusive.
SER C	Clears SER report from nonvolatile memory.
SHO n	Show relay settings (overcurrent, reclosing, timers, etc.) for group n (n = 1–6, if not specified, default is active setting group).
SHO n L	Show SELOGIC [®] Control Equation settings for group n (n = 1–6, if not specified, default is the SELOGIC Control Equations for the active setting group).
SHO G	Show global settings.
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<u>Access Level 2 Commands</u>	The Access Level 2 commands allow unlimited access to relay settings, parameters, and output contacts. All Access Level 1 and Access Level B commands are available from Access Level 2. The screen prompt is: ==>
CON n	Control Relay Word bit RBn (Remote Bit n; n = 1–16). Execute CON n and the relay responds: CONTROL RBn. Then reply with one of the following: SRB n set Remote Bit n (assert RBn). CRB n clear Remote Bit n (deassert RBn). PRB n pulse Remote Bit n [assert RBn for 1/4 cycle].
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SET ... name	For all SET commands, jump ahead to specific setting by entering setting name.
SET ... TERSE	For all SET commands, TERSE disables the automatic SHO command after settings entry.
STA C	Resets self-test warnings/failures and reboots the relay.
VER	Show relay configuration and firmware version.

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