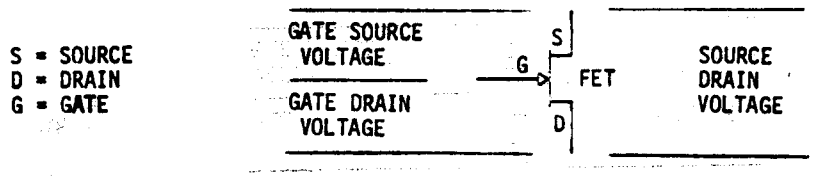
STATIC SWITCHES WITH JUNCTION FET'S

I. INTRODUCTION

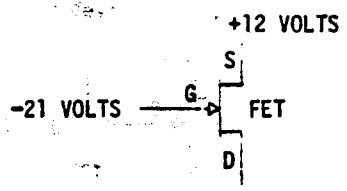
Reed relays have been replaced by static switches using field effect transistors (FETs). This change was made in order to improve the reliability of linear controllers as moving mechanical parts are more susceptable to failure than their electronic replacements. Due to the limitations of the electronic components used, it was not possible to directly replace reed relays in all applications. Voltage breakdown restrictions have necessitated various engineering considerations in the design of controllers using static switches. This instruction leaflet will discuss the basic components of static switches, their limitations and the various considerations that should be observed when designing with these devices.

II. BASIC FET OPERATION

The FET's presently in use are electrically symmetrical, and as a result the function of the source and drain can be interchanged. The device will be in the "on" state if either gate - source voltage or gate - drain voltage is zero volts, regardless of the drain - source voltage polarity. Because of controller voltages going positive and negative and because of the symmetry of the FET, the device can be turned off only when the gate is more negative (by greater than the FET pinch - off voltage) than the most negative of the source or the drain voltage.



The maximum voltage that can be applied to the FET is determined by the reverse breakdown voltage of the gate to channel diodes. This voltage restricts the voltage which can be applied to the FET. If -21V is used on the gate to insure turn off, then a +12V signal on the source would create a 33V differential across the gate to channel diode. This voltage must be less than the breakdown voltage of the FET. In order to limit the maximum voltages on a FET, circuitry in which the FET is used as a static switch must be designed to limit the voltage range within ±12V.



III. BASIC STATIC SWITCH

A. Basic Static Switch With Fixed Reference

In order to utilize the FET, it must be connected to an external signal. The simplest FET switch using n-channel J-FET's is shown in Figure 1.

This switch is a normally closed contact: low resistance with no input signal. The switch opens when (RN) -24V is applied to A. 11D is used to prevent positive signals from getting to the gate of 11TR. 17R is used to discharge the gate-drain and gate-source capacitances when 11D is reverse biased. 11C and 12R form an input noise filter. 11R is used to generate contact current if an external relay is used to sequence the static switch. 11R changes value (10K if PSC, 21.5K if PSP) depending upon the switch reference. To maintain 11TR in the off state, the gate voltage must always be more negative than -17 volts.

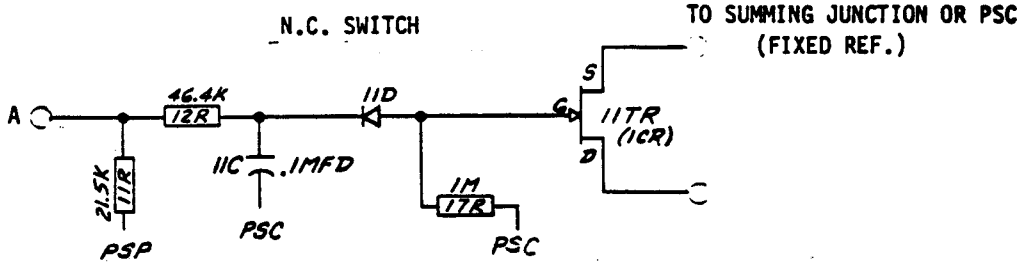


FIGURE 1

B. Basic Static Switch with Floating Reference

Figure 2 is a static switch with a floating reference. In order to insure proper FET operation, the driver reference voltage is PSP (+24V). The FET is conductive when PSP is applied to the gate diode, 12D. The FET is non-conductive when the appropriate negative voltage is applied. If 12TR is to be turned off, the gate must be more negative than the source or the drain. The source of 12TR will be at zero volts through a load. Resistors 16R & 15R form a voltage divider between the input term 33 which can be anywhere between +12V and PSN. If the input voltage at term 33 is +12V, the gate will be at -17.2V. If the input voltage at term 33 is at -12V, the gate will be at -21V. In both cases 12TR will be non-conductive. To obtain an output at terminal 49, RN (-24V) must be applied to terminal 41. 13TR conducts and applies +24V to the cathode of 12D allowing 12TR to conduct.

NOTE: When checking gate voltage a scope with a 10 meg ohm probe should be used.

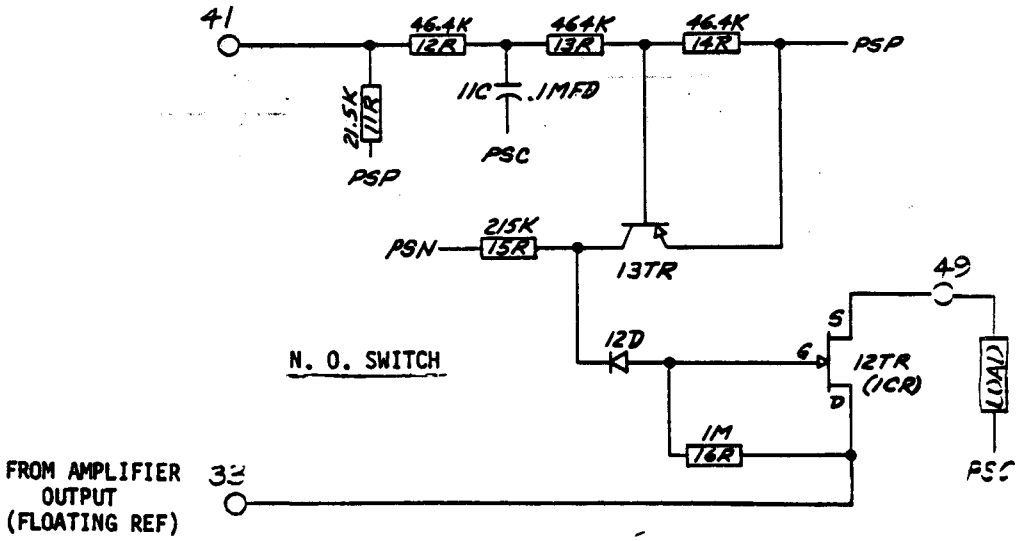


FIGURE 2

The following figure shows the various FET switches in an uncommitted form and their simplified representations.

A This potential is either +24V or PSC depending on resistor value of 11R (10K-PSC or 21.5K - PSP).

B is tied to PSC when C is tied to a summing junction (SJ)

B and C are tied together and marked as the low impedance signal side.

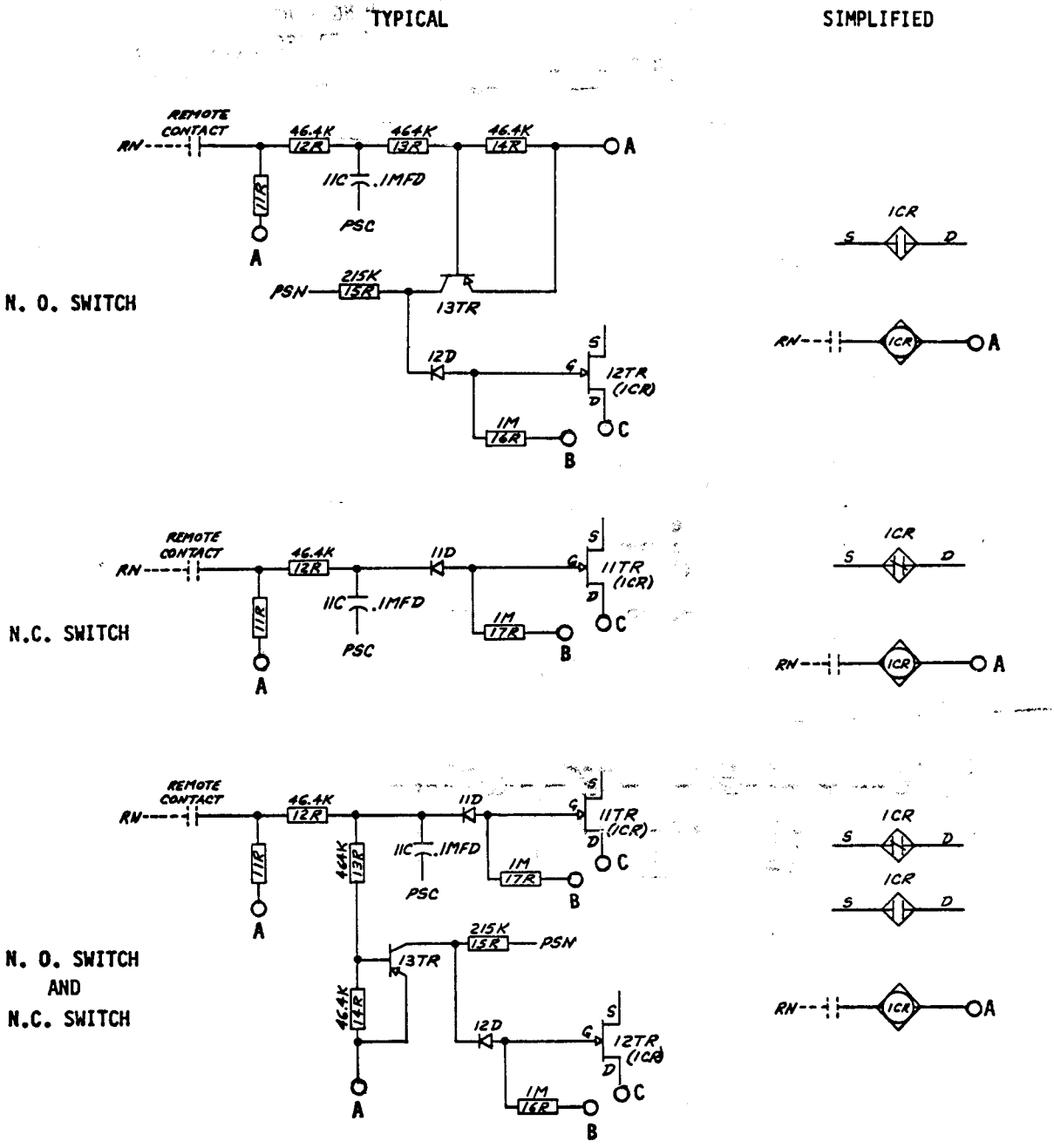


FIGURE 3

IV. CHARACTERISTICS AND RATINGS

A. Ambient Temperature: 0-55°C

B. Static Contact (FET):

Maximum voltage ±12VDC.

Maximum current 10 ma.

Maximum "on" resistance 80 ohms.

Minimum "off" resistance 10^9 ohms.

C. Static Switch Power Supply Requirements:

Energizing power + static switch power = Total power

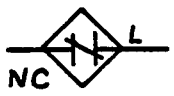
1) Energizing voltage -24V ± 5%, 2.5 ma.

2)

Static Coil Referenced to PSC		Static Coil Referenced to PSP
PSN (-24V) ± 5% 0 ma PSP (+24V) ± 5% 0 ma	N.C. switch	PSN (-24V) ± 5% 0 ma PSP (+24V) ± 5% 2.5 ma
PSN (-24V) ± 5% .5 ma PSP (+24V) ± 5% .5 ma	N.O. switch or N.O. & N.C. pair of switch	PSN (-24V) ± 5% .5 ma PSP (+24V) ± 5% 3 ma

D. Switch Symbols:

To maintain a single symbol for static contacts the FET switch contacts will be designated as follows regardless of where they are connected in the circuitry:



When both sides of FET contacts operate at a floating level, the 1MΩ gate resistor and the drain terminals must be tied together (B connected to C in Figure 3). This connection point is marked L and must be connected to a low impedance source.

When one side of the FET contact is tied to the summing junction or PSC (C to SV or PSC) and the 1MΩ gate resistor should be tied to PSC (B to PSC).

V. APPLICATION OF STATIC SWITCHES

As mentioned earlier in this I.L. the FET's used are electrically symmetrical. After the low impedance side of the static contact (marked "L") is determined (by appropriate connection of the gate resistor and the drain and source terminals) it is unsymmetrical and may only be applied as designed. The following typical circuits will show proper and improper applications of static switches. The application discussed refer only to the standard FET circuits of Figure 3.

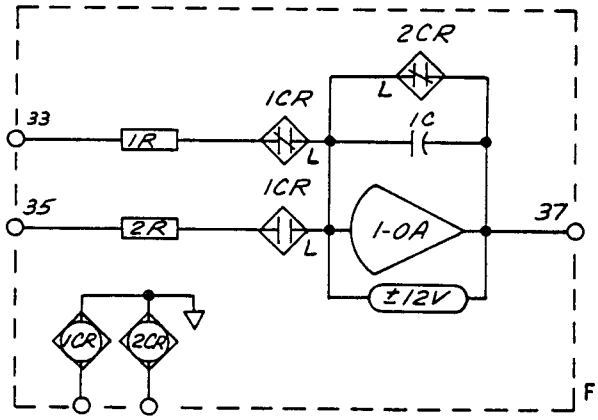


FIG. 4

Maximum voltage on 33, 35 & 37 is ± 12V

Energizing Voltage: -24V

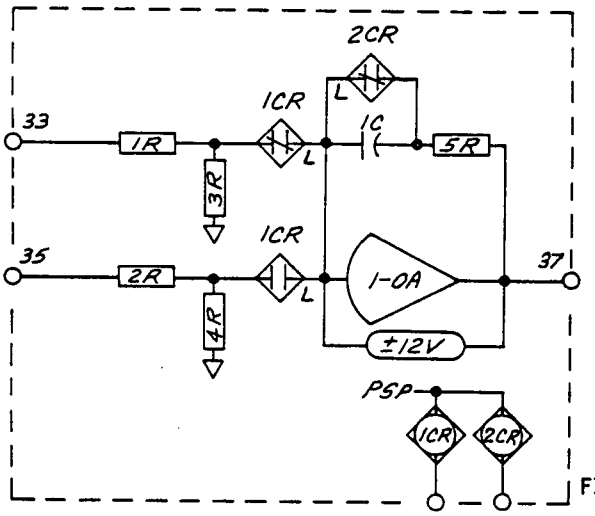


FIG. 5

Maximum voltage on 37 is ± 12V

Maximum voltage on 33 & 35 is

$$\pm \left(\frac{3R + 1R}{3R}\right) 12$$

Order of 1C & 5R cannot be reversed.

Note different reference voltages for static relays in Fig. 4 & Fig. 5.

Energizing Voltage: -24V

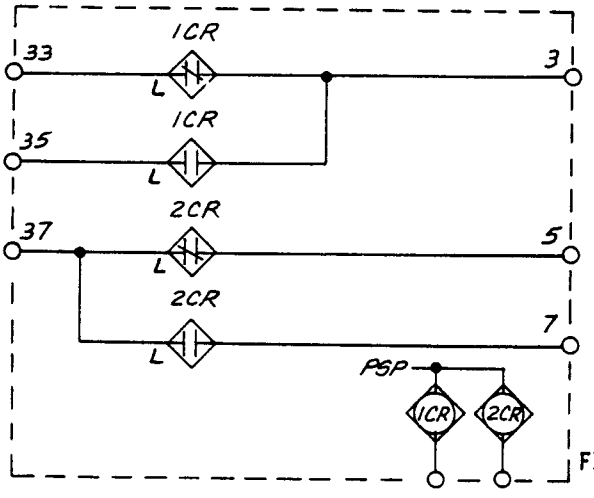


FIG. 6

Maximum voltage on 33,35,37,3,5,7 is ± 12V

Although switches 1CR & 2CR are similar they are not the same and cannot be interchanged. The contact side marked L must be tied to a low impedance signal source. The unmarked contact side should be tied to a higher impedance load.

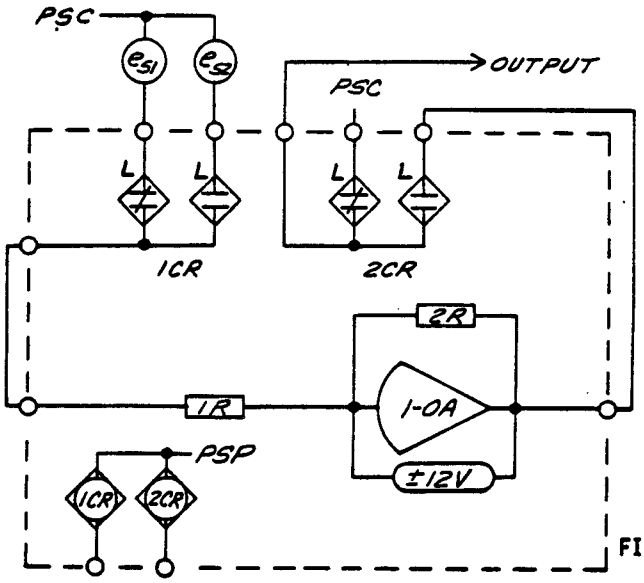


FIG. 7

Proper connection of static switches. L side of contacts tied to signal sources or PSC.

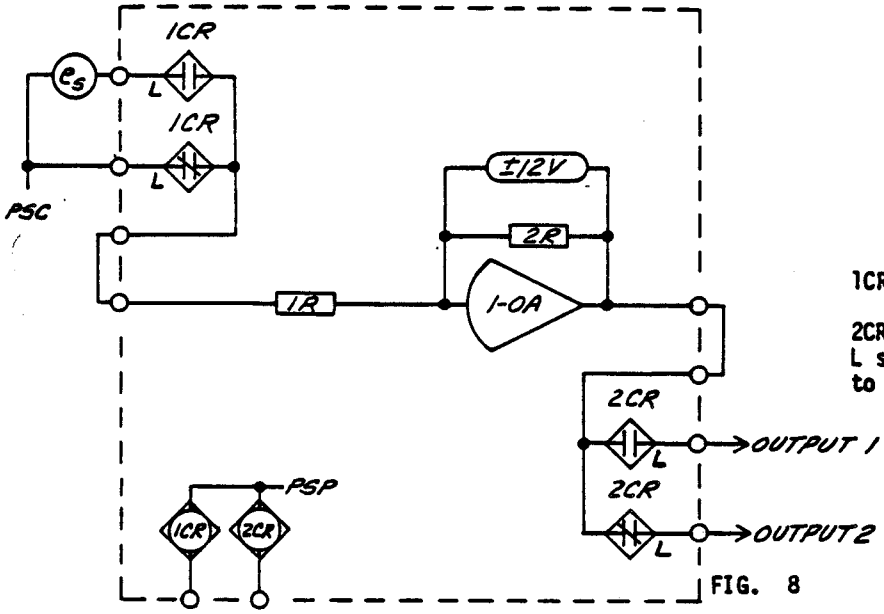


FIG. 8

1CR contacts connected properly.

2CR contacts connected incorrectly
L side of contacts is not connected to signal source (low impedance).
The contacts of 2CR might still function but when the contacts are open gate current of the FET appears as an output signal.

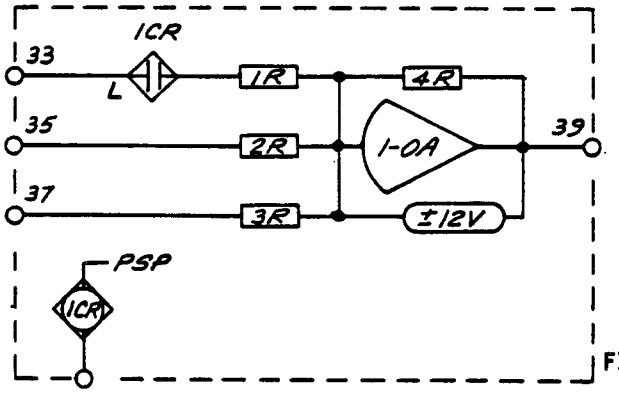


FIG. 9

If terminal 33 is not used it must be tied to PSC externally.

If 33 is left unconnected, the contact will be closed and FET gate current will flow into 1R. Proper operation of the static switch requires that terminal 33 be connected to a low impedance source.

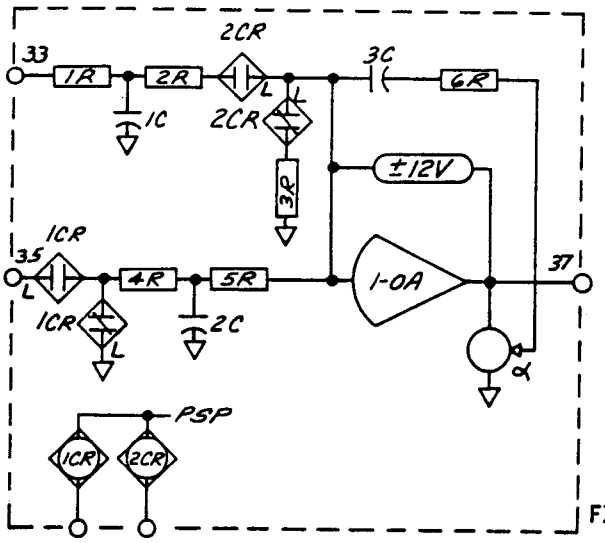


FIG. 10

If possible, 2CR is a preferred method for connection of the static switch.

The switches will function properly as shown, but terminal 35 must be tied to a signal source or PSC. Terminal 33 can be left open and it will not effect the operation of 2CR.

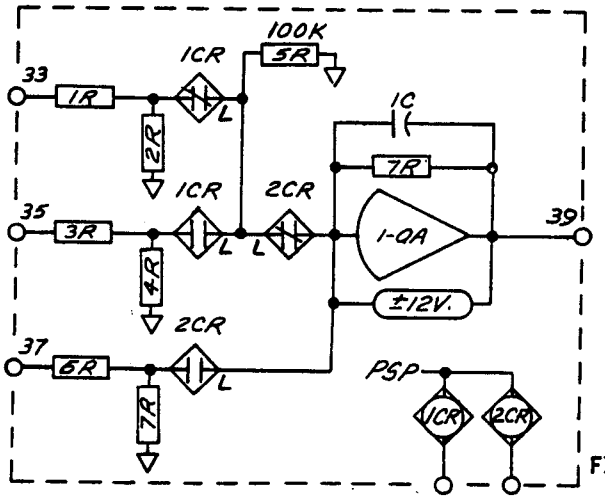


FIG. 11

When sequencing as shown, terminals 33 and 35 should be tied to PSC if not used. The paralled combination of 1R & 2R and 3R & 4R should be less than 100K to insure proper operation of 1CR. With this type of sequencing 5R must be included. This resistor provides a reference for the contacts of 1CR when 2CR is engerized.

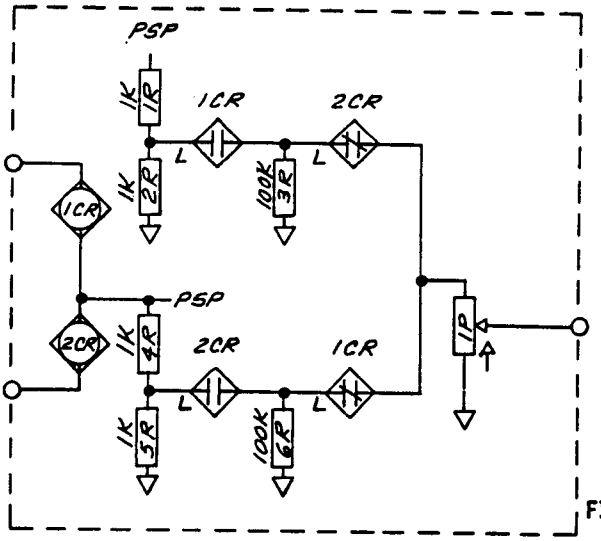


FIG. 12

When interlocking static relays as shown 3R and 6R must be included. 3R provides a path for FET gate current when 2CR is energized 6R provides a path for gate current when 1CR is energized. If 3R & 6R are not included the switches will not function properly.

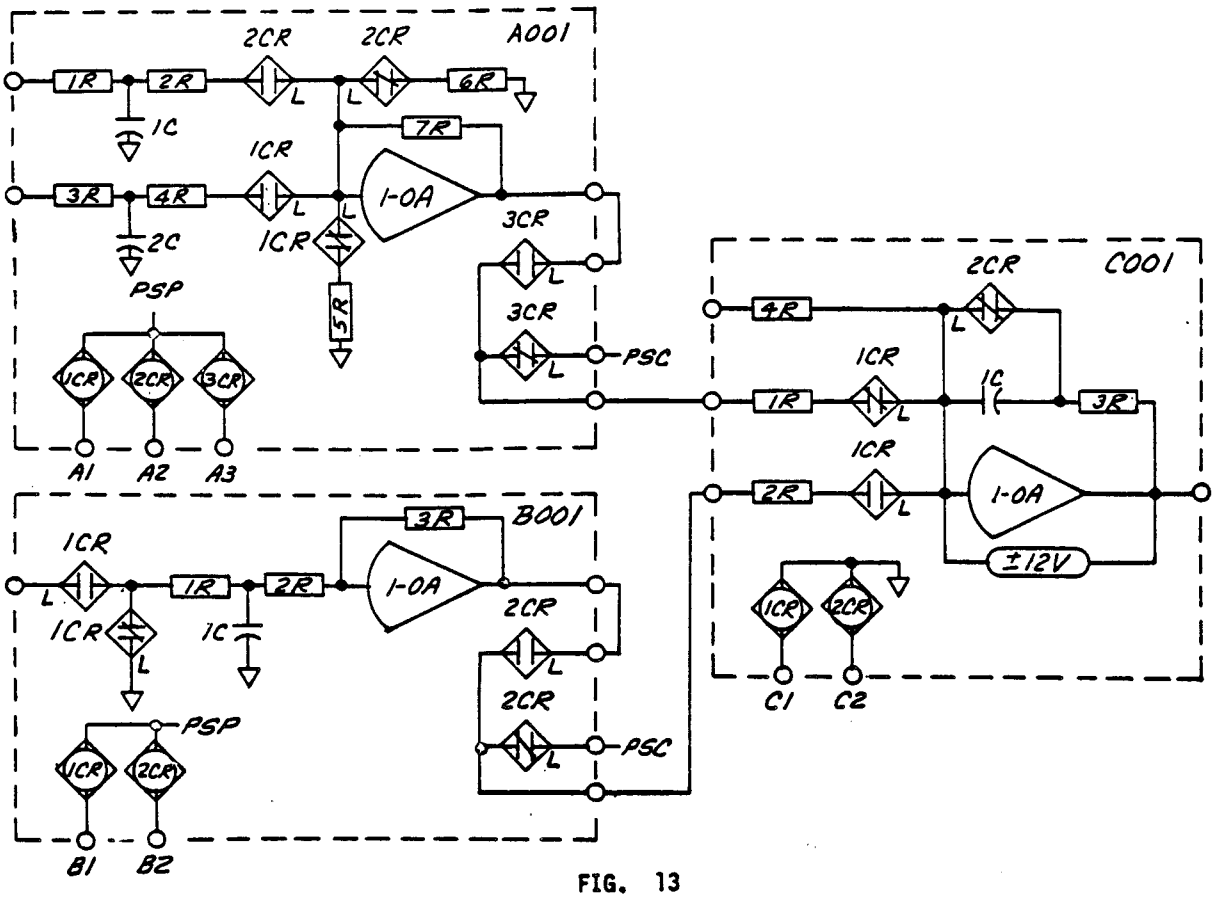
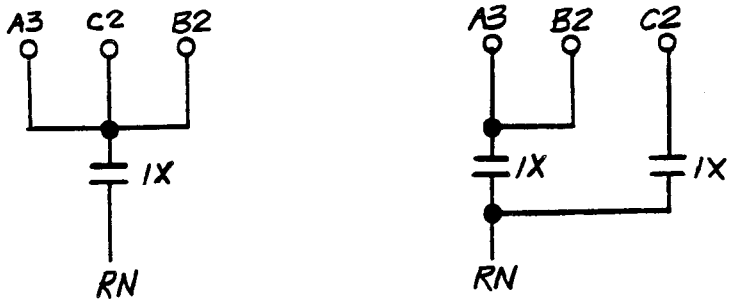


FIG. 13

Sequence Control. If 3CR of A001, 2CR of C001 & 2CR of B001 are to be energized at the same time, they must be sequenced properly



INCORRECT CORRECT

If the reference voltage for the static switches that are to be energized at the same time is the same, they can be tied together before going to an external relay.

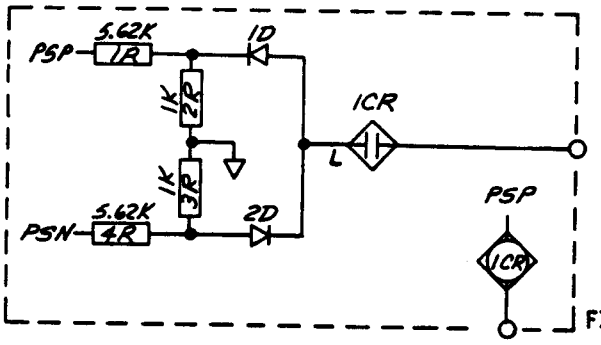


FIG. 14

When using diodes in conjunction with static switches, there must be a path for gate current. In this example, gate current flows from the Thevenin equivalent circuit composed of 4R & 3R connected between PSN & PSC through 2D into the gate circuit of the FET to PSN.

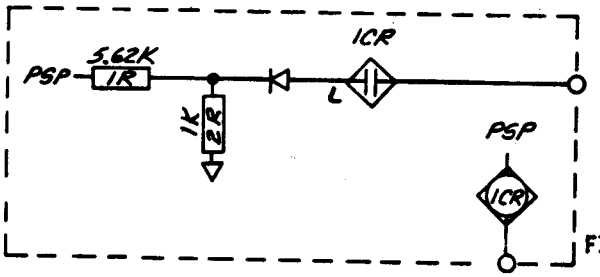


FIG. 15

This circuit will not work because FET gate current cannot flow.