INSTALLATION • OPERATION • MAINTENANCE

INSTRUCTIONS

TYPE SKBU-2A
DUAL PHASE COMPARISON RELAY

CAUTION: It is recommended that the user of this equipment become acquainted with the information in this instruction leaflet and in the system instruction leaflet before energizing the system.

Printed circuit modules should not be removed or inserted where the relay is energized. Failure to observe this precaution can result in an undesired tripping output and can cause component damage.

APPLICATION

The type SKBU-2A is a high-speed relay used in conjunction with frequency shift type channels. Simultaneous tripping of the relays at each line terminal is obtained in less than 22 milliseconds for all internal faults within the limits of the relay settings.

The system can be used with a frequency-shift carrier channel or a frequency-shift audio tone over a voice-grade pilot-wire or microwave channel.

In contrast to the carrier blocking scheme, this is a transfer trip system; accordingly, the blocking-start function is not required.

The SKBU-2A relay may be applied to two-terminal or three-terminal lines. Two-terminal applications require one transmitter and one receiver per terminal. Three-terminal applications require one transmitter and two receivers per terminal.

The overcurrent fault detector in the SKBU-2A relay responds to all fault types. Therefore, distance relays are not required to be used with the SKBU-2A, although they may be added to improve arming sensitivity.

CONSTRUCTION

The phase comparison relays consist of a composite positive and negative sequence current network, a saturating transformer, a 20-volt power supply, and printed circuit boards mounted on a standard 19-inch wide panel, 8¾ inches high (5 rack units). Edge slots are provided for mounting the rack on a standard relay rack.

Sequence Network

The sequence network consists of a three-legged iron core reactor and a set of resistors, R_1 and R_0. The reactor has three windings: two primary and a tapped secondary winding, wound on the center leg of an "F" type of lamination. The secondary taps are wired to the A, B and C tap connections in the front of the relay (R_1 taps). Ro consists of three tube resistors with taps wired to F, G and H tap connections in the front of the relay. The R1 resistor is a formed resistor associated with the tapped secondary of the reactor.

Saturating Transformer

The voltage from the sequence network is fed into the tapped primary of a saturating transformer which has two secondary windings. One winding supplies the fault detector and the other winding supplies a keying circuit.

Power Supply

The solid-state circuits of the relay are regulated from a 20-volt supply on the relay panel. This voltage is taken from a Zener diode mounted

All possible contingencies which may arise during installation, operation, or maintenance, and all details and variations of this equipment do not purport to be covered by these instructions. If further information is desired by purchaser regarding his particular installation, operation or maintenance of his equipment, the local Westinghouse Electric Corporation representative should be contacted.

on a heat sink. A voltage dropping resistor is provided between the source dc supply and the 20 volt regulated supply.

Printed Circuit Boards

Seven printed circuit boards are used in the SKBU-2A relay. A fault detector board, protective relay interface board, supervision board, amplifier and keying board, output board and a low pass filter board.

All of the circuitry that is suitable for mounting on printed boards is contained in an enclosure that projects from the rear of the front panel and is accessible by opening a hinged door on the front of the panel. The printed circuit boards slide in position in slotted guides at the top and bottom of each compartment and the board terminals engage a terminal block at the rear of the compartment. Each board and terminal block is keyed so that if a board is placed in the wrong compartment, it cannot be inserted into the terminal block. A handle on the front of each board is labeled to identify its function in the relay.

1. **FD BOARD (FAULT DETECTOR BOARD)**
   The fault detector board contains a resistor-Zener diode combination, a phase splitting network, a solid state fault detector, and a pulse width detector. The control for setting pickup of the fault detector is mounted on the fault detector board. This unit operates when the fault current exceeds a definite value. The pulse width detector is activated when the keying pulse width decreases to a value of 4 milliseconds.

   The location of components on the board is shown in Fig. 2 and the schematic of the board is shown in Fig. 3.

2. **LOW PASS FILTER BOARD (LPF)**
   The Low Pass Filter Board contains a low pass filter for interfacing the secondary of the saturing transformer with the Sine wave to Square Wave Convertors of the Amplifier and Keying Board. Also six buffer outputs are contained on this board to connect the squaring amplifiers to external oscillograph connections.

   The following Figures apply to this board: Fig. 13 Component location, Fig.14 Schematic of the Board.

3. **SUPERVISION BOARD (SUPRV. BOARD)**
   This board contains interface circuits to the channel receivers and a 150 millisecond pickup and 0 millisecond dropout alarm timer circuit. The interface circuits connects the SKBU-2A relay to the channel receiver, and the timer circuit locks out the relay for failure of the channel equipment.

   The following figures apply to this board: Fig. 15, Component Location, Fig. 16, Schematic of the Board.

4. **AMPL. AND KEY BOARD (AMPLIFIER AND KEYING BOARD).**
   The Amplifier and Keying Board contains three sine wave to square wave convertors, a transmitter keying circuit, two dc phase delay circuits, and four connections for remote signals. One sine wave to square wave convertor produces a square wave pulse that is used to key the channel transmitter. The other two convertors product two square waves on alternate half cycles of a 60 Hz. voltage. These two square waves are applied to the dc phase delay circuits. Links are provided on the board to connect the relay for two or three terminal applications. For two-terminal applications, both link 1 and link 2 on the Amplifier and Keying Board must be connected C to 2. For three-terminal applications, these links must be connected C to 3.

   The location of components on the board is shown in Fig. 7 the schematic of the board in Fig. 8, and the logic diagram in Fig. 9.

5. **ARMING BOARD**
   The Arming Board contains AND circuits that compare pulses obtained from the Amplifier and Keying Board. The output obtained from the AND circuits is proportional to the time difference in the phase angle between the input quantities. This board also contains other logic circuits such as 4/0 timer, and a 2 or 3 count transient unblock circuit. A link is provided on

this board such that the relay is armed by either solid state distance fault detectors or the SKBU-2A fault detector. The link must be open for arming by the solid state distance fault detector only.

The location of components on the board is shown in Fig. 4, the schematic of the board in Fig. 5, and the logic diagram in Fig. 6.

6. **OUTPUT BOARD**

The Output Board contains two NAND gates connected as flip-flop circuits for tripping. Other logic on the board includes a trip amplifier, transient blocking circuit, and two time delay circuits. The Flip-Flop circuit operates when all the inputs to the Arming Board are of the correct polarity. The Transient block circuit operates after a time delay on fault detector operation to prevent tripping. One time delay circuit maintains transient blocking on the trip flip-flop after the fault detector resets. The second time delay circuit resets the first time delay circuit in the case of an interval fault.

The following figures apply to this Board: Fig. 10 Component location, Fig. 11 Schematic of the Board, Fig. 12 logic of board.

7. **PROTECTIVE RELAY INTERFACE BOARD (PR. INTER.)**

The Protective Relay Board contains logic circuits to connect the distance fault detectors and squelch relays into the Phase Comparison Relaying System. This board contains buffer circuits, and OR circuits to connect the distance fault detectors into the system. A 6/0 timer, 10/150 signal squelch circuit, and a 2.5 second alarm circuit for sustained fault detector operation are also provided on this board. The following figures apply to this board: Fig. 17, Component Location, Fig. 18, Schematic of the Board.

Card Extender

A card extender (style no. 644B315G02) is available for facilitating circuit voltage measurements or major adjustments. After withdrawing anyone of the circuit boards, the extender is inserted into the terminal block on the front of the extender. This restores all components and test points on the boards are readily accessible.

Test Points

Test points are located on each printed circuit board for the major components on the board. Complete circuit test points are wired to the front panel of the relay for convenience in adjusting and testing the relay.

OPERATION

A. System

In phase comparison relaying, the phase position of fault currents at the ends of a transmission line are compared over a pilot channel to determine if the fault is internal or external to the line section. When a frequency shift channel is used as the pilot channel, a dual comparison system can be utilized. This means that the system can trip on either half-cycle of power system frequency as contrasted to a blocking scheme where tripping occurs on alternate half-cycles during the absence of a carrier signal.

The three-phase line currents energize a sequence network in the SKBU-2A relay which produces a single-phase output voltage proportional to a combination of sequence components of the line current. This single-phase voltage energizes the primary of a saturating transformer with two secondary winding. One secondary winding energizes the fault detector circuit and the second secondary winding energizes the keying circuit through a low pass filter. The keying circuit shifts the frequency of the transmitter from a space frequency to a mark frequency. These frequencies are transmitted over the pilot channel to the channel receiver which converts the mark and space frequencies to two dc output voltages, a space output that corresponds to the space frequency and a mark output that corresponds to the mark frequency. Thus, on each half cycle of power system frequency either a space or mark output is obtained from the channel receiver and applied as pulses to the remote squaring amplifiers to the SKBU-

2A relay. Each of these half-cycle pulses are compared with the phase positions of each half-cycle of the voltage from the sequence network of the SKBU-2A relay at the channel receiver terminal. The space pulse is compared to one half cycle of the voltage and the mark pulse to the other half-cycle. If the local and remote pulses are in an internal fault relationship and the fault detector has operated, tripping will occur 4 milliseconds later through operation of the trip flip-flop and trip amplifier circuits on the output board.

Current transformer connections to the sequence networks at the two line terminals are such that the space and mark pulses are in phase with their respective local pulses during an internal fault to allow tripping. However, if the fault is external to the protected line section, the space and mark pulses are out-of-phase with their respective local pulses and tripping does not occur.

The four-millisecond delay previously mentioned is added to allow for differences in current transformer performance at opposite line terminals and relay coordination.

B. Relay

With reference to the logic diagram of figure 19, the three-phase line currents energize a sequence network that produces a single phase voltage proportional to a combination of sequence components. (See Tables I and II). This voltage is applied to the primary winding of a saturating transformer which produces two secondary voltages.

The secondary voltages are applied to two separate boards:

1. Fault Detector Board
2. Low-Pass Filter Board

1. FAULT DETECTOR BOARD

With reference to schematic dwg. of Fig. 3, the ac voltage from the secondary of the saturating transformer is applied to terminals 5 and 6 of the fault detector board. This voltage is then applied to a phase-splitting network (R2, R3, C3, C4, and R4) and a polyphase rectifier (diodes D1 to D6) The dc voltage obtained from the rectifier has minimum ripple and is applied to the fault detector circuit Q1, Q2, Q3, and Q4.

Fault Detector (FD)

Under non-fault conditions, transister Q1 is not conducting and is turned off. The collector of Q1 is thus at positive potential and provides base drive to transistor Q2, driving it to conduction. With Q2 conducting, transistors Q3, and Q4 are turned off.

When fault current causes the dc input voltage from the polyphase rectifier (across R5 and R6) to exceed the 6.8 volt rating of Zener diode, Z2, a positive input is applied to the base of Q1 causing it to conduct. In turn, Q2 stops conducting and capacitor, C7 charges, giving 8 milliseconds time delay before Q3 and Q4 are switched to full conduction. The feedback path of resistor R12 and Diode D8 increase the voltage to Z2 after the fault detector operates. This seals in the fault detector and allows the fault detector to drop out at a high droput ratio when the ac current is reduced.

Pulse Width Detector

Another circuit on the Fault Detector Board is the pulse width detector. This circuit checks the time between every adjacent transition of an input square wave which represents the voltage produced by the sequence network. If two transitions occur within a certain time period, a block output occurs which will remain until no two transitions occur within the time period. The time period can be adjusted from 2 to 8 milliseconds by means of an adjustable timer. This setting range represents frequencies of 60 Hz to 250 Hz expressed in terms of a symmetrical wave. It is factory set for a frequency of 120 Hz which represents a detection period of 4 milliseconds. Figure 29 shows the timing chart of the pulse width detector for pulse transitions of 4 milliseconds and 8 milliseconds. With reference to the internal schematic of Figure 3, the pulse width detector consists of the following parts:

1. **Generated pulse circuit** which produces a 5 μs pulse for each transition of the input square wave. The component parts of this circuit are as follows:

a. Nand Gate IC1 (pins 11 and 10, pins 9 and 8)
b. Nand Gate IC2 (pins 10, 9, and 8)
c. Capacitors C11 and C12
d. Diodes D15 and D16

A transition of the input square wave produces pulses due to the capacitor action which occurs when the output at either pin 10 or pin 8 of IC1 goes low. The capacitor initially discharged by the diode will act as a "0" to the input of IC2 (either pin 10 or pin 9). A "1" output will be obtained from pin 8 to IC2 until the capacitor charges above the threshold voltage of IC2 through the internal IC resistance to 15 Vdc. The output will then change to a "0". This will produce a 5 μs positive pulse on the output of IC2 (pin 8) during the charging time of the capacitor.

When the input square wave makes a "0" to "1" transition pin 10 (IC1) goes low causing the pulse output through C12. When the input square wave makes a "1" to "0" transition, pin 8 (IC1) goes low causing the pulse output through C11.

2. **Timer circuit** (**oscillator**) serves as a reference for the time between the generated pulses. The component parts of this circuit consists of:
   a. Timer – Trimpot R22, resistor R23, and Capacitor C9.
   b. Programmable unijunction transistor Q6
   c. Voltage divider network R26 and R27
   d. Discharge circuit R21 and D14
   e. Resistors R24, R25, and Diode D13.

The timer circuit is actually an adjustable free running oscillator which is synchronized with the transitions of the input square wave.

C9 is charged through the path of trimpot R22 and resistor R23. It is discharged by one of two paths.

1. Through R21 and D14 and pin 6 of IC1 when at "0". The "0" at pin 6 of IC1 is produced by the generated pulse circuit for each transition of the input square wave.
2. Through the breakdown of the unijunction transistor Q6. If the charge is not removed by pin 6 of IC1 going to "0", capacitor C9 will charge to approximately 10 volts (as determined by the R26, R27 voltage divider relationship). Q6 will conduct
   a. to lower the junction point voltage of R26 and R27 which will act as a "0" to diode D17 and D20.
   b. to discharge C9. Once the anode current reaches the valley current of Q6, Q6 will turn off. However, the time for this is approximately 15 μs, thereby allowing an adequate resetting pulse.

3. **Flip-flop circuits** compare information from the timer circuit (oscillator) and the generated pulse circuit. These circuits compare the pulse width of the input square wave and initiates a block signal if the input square wave is not of a certain duration.

Flip-flop number 1 IC2 (pins 13, 12, and 11) IC1 (pins 3 and 4) Flip-flop number 2 IC2 (pins 1, 2, and 3) IC1 (pins 1 and 2) Diodes D18 and D19.

The generated pulses enable pin 4 (IC2) and are inverted through pin 5 and 6 of IC1. The inverted pulse when at "0"

a. Sets flip-flop number 1
b. Resets the oscillator timer by discharging capacitor C9 through R21 and D14. Therefore, every time a pulse occurs, the timer circuit is reset. As soon as the pulse disappears, the timer starts again in order to check the time before the next pulse occurs.

The output of the first flip-flop pin 11 (IC2) after being set becomes "1" and works into a 20 μs timer of R28 and C10 before enabling pin 5 (IC2). Since a "0" output on pin 6 (IC2) sets the second flip-flop, the 20 μs delay from the first flip-flop prevents that signal from reaching IC2 (pin 5) while the generated pulse remains on IC2 (pin 4) Both Flip-flops will reset when the timer times out to breakdown the unijunction transistor Q6. This will lower the voltage at the junction of R26 and R27 to supply a "0" to diodes D17 and D20.

If a second generated pulse occurs before the unijunction transistor Q6 breaks down, the first flip-flop is not reset. Both inputs (4, 5) of IC2 will then be enabled ("1") to cause pin 6 to become "0". This sets the second flip-flop to cause pin 2 of IC1 to become "0". The "0" will block the fault detector.

2. **LOW PASS FILTER BOARD**
With reference to Fig. 14, the ac voltage from the second winding of the saturating transformer is applied to terminals 10 and 12 of the low pass filter board. The low pass filter (C1, L1, and C2) removes the harmonics from this voltage and applies a voltage that is essentially sinusoidal in waveform to resistor R7. (note:-With the Amplifier and Keying Board in place, this voltage is clamped in magnitude by two Zenior diodes on that board. Due to this clamp the voltage is not a sine wave.) This voltage is applied to the three sine wave to square wave convertors on the Amplifier and Keying Board.

3. **AMPLIFIER AND KEYING BOARD**
The output of the low pass filter is applied to the sine wave to square wave convertors of the Amplifier and Keying Board. These convertors consist of four resistors and an operational amplifier as shown in Fig. 20. Resistors R1 and R2 are set equal to each other and their junction point is connected to the inverting input of the amplifier through a resistor R7 of the Low Pass Filter Board. Resistors R3 and R4 are biasing resistors whose junction point is connected to the non-inverting input of the amplifier. By selecting the value of R3 and R4, the dc voltage V1 can be made less than or greater than the voltage V2. By varying the magnitude of this voltage, the square wave voltages produced when ac is applied to the convertor can be made to vary in width. Also the output of the convertor can be made sensitive to the polarity of the input ac voltage. This relationship is shown in Fig. 21.

The output of the keying convertor is connected through transistors to the transmitter of the channel equipment. Also the output of one transistor of the keying circuit is connected to the pulse width detector on the Fault Detector Board.

The output of the local convertors are connected to the AND circuits of the Arming Board through two dc phase delay circuits. The timing waves of these circuits are shown on Figures 22 and 23.

Connections are provided on the Amplifier and Keying Board to connect the channel interface circuits of the Supervision Board to the AND circuits of the Arming board. Links on the Amplifier and Keying Board can be changed for two or three terminal applications.

4. **SUPERVISION BOARD**
The circuits on the Supervision Board include the interface to the channel receiver and a low signal timer.

As shown in Fig. 16, there are four interface circuits in the SKBU-2A. These circuits include input buffers and a transistor that connects the channel receiver to the Amplifier and Keying Board. Space interface 1 includes Q1 of the Supervision Board and Resistor R27 of the Amplifier and Keying Board. Space interface 2 includes transister Q6 of the Supervision Board and R26 of the Amplifier and Keying Board. Mark interface 1 includes transistor Q2 of the Supervision Board and Resistor R24 of the Amplifier and Keying Board. Mark interface 2 includes transistor Q7 of the Supervision Board and Resistor R25 of the Amplifier and Keying Board.

The remote interface circuits are in one of three states:

1. Loss-of-channel state.
2. Receiving space frequency only.
3. Receiving alternate half-cycles of space and mark frequency.

With reference to the supervision board of Fig. 16 for a serviceable channel Q1 and Q2 are either alternately turned on and off or Q1 is turned on and Q2 is turned off. Under both conditions, base current is supplied to transistor Q3 and Q3 is turned on at all times. With Q3 turned on, C1 can not charge and Q4 is turned off.

When the relay is used with a TCF carrier channel, the carrier receiver is clamped into

both a mark and space output on a loss of channel. This turns on transistors Q1 and Q2 and shorts the base of Q3 to negative potential and Q3 turns off. Positive potential is applied to C1 through R12 and R13 and 150 milliseconds later, Zener diode Z5 breaks down to allow base current to flow to Q4. Q4 turns on which provides a path through R16 for base current of Q5 to flow to negative. Q5 turns on to apply positive voltage to R17. This voltage is then applied to AND 1 and AND 2 of the arming board to block tripping. The voltage is also applied to an external alarm circuit.

When this relay is used on either a TA2.2 tone channel or an MC-22 microwave channel, the low-signal clamp is not utilized. If these channels are not serviceable, the channel receiver is clamped into neither a mark nor a space output. This instantaneously places a blocking signal on the AND circuits of the SKBU-2A relay. Hence, the relays will not trip on a low signal clamp. However, the low signal timer is not activated and will not produce an alarm output to the next device. This alarm information is supplied directly to the next device by the channel receivers.

For either internal or external fault conditions, the outputs of both interface circuits are square-wave voltages. Both voltages vary from zero volts to approximately 20 volts dc and are out of phase with each other i.e., when one voltage is at zero volts the other voltage is + 20 volts dc.

5. **ARMING BOARD**

The remote signals are compared to the local signals by two AND gates on the Arming board. These circuits are shown in figures 5 and 6.

As shown in figure 5, AND 1 consists of transistor Q2, diodes D1, D3, D4, Zener diode Z5, and resistors R1, R2, R3, and R4. AND 2 consists of transistor Q1, diodes D5, D6, D8, Zener diode Z4, and resistors R6, R7, R8, and R9. Both transistors Q1 and Q2 have a common input through resistor R5 and Diodes D9 and D10.

Positive input voltages on any of the input terminals of AND 1 will turn transistor Q1 on. Also positive input voltages on any of the input terminals to AND 2 will turn transistor Q2 on. With both Q1 and Q2 conducting, transistor Q3 is turned off, and the collector of Q3 is at positive potential. As a result, base current is supplied to Q8 through R35 to turn on transistor Q8. This places transistor Q8 at negative potential to prevent capacitor C2 from charging. This is a non-trip state.

Base current is also supplied through R34 to Q8 from the collector of transistor Q4. Transistor Q4 is normally not conducting, and its collector is at positive potential. If a fault detector operates (either the SKBU-2A or supplementary distance fault detectors), a positive input is applied to either terminal 12 or 14 of the Arming Board. This positive input will:

1. Provide a positive output at terminal 9 of the Arming Board.
2. Provide base current to transistor Q4. Q4 will conduct and remove the base current drive to Q8 through resistor R34. However, Q8 will not turn off until Q3 conducts. This occurs when either Q1 or Q2 stops conducting. Q1 and Q2 will not stop conducting until all positive potentials are removed from the input terminals of AND 1 and AND 2.

In examining the condition of the input signals to AND 1 and AND 2, it will be found that:

a. Three inputs to AND 1 are dedicated to the comparison of one local square wave to two remote square waves. In a similar manner, three inputs to AND 2 are dedicated to the comparison of a second local signal to a set of two remote square waves. Provisions for four remote square waves are necessary for three terminal line applications. For two terminal line applications, one input to both AND 1 and AND 2 is connected to negative by means of links on the amplifier and Keying board so that these inputs cannot provide base drive to either Q1 or Q2. Hence, for two terminal line applications, a local derived square wave is compared to a remote square wave on AND 1 and a second local derived square wave is com-

pared to a second derived square wave on AND 2.

b. Other inputs to AND 1 and AND 2 are dedicated to low signal clamps from the Supervision Board. These inputs are zero potential with a serviceable channel. As such they will not provide base current to either transistor Q1 and Q2 which will allow the AND gates to be actived if all other inputs are at negative potential.

On either load conditions or external fault conditions, the local and remote pulses lineup such that a posititive potential is supplied to the input terminals of AND 1 and AND 2 during these conditions. As a result, base current is supplied to transistors Q1 and Q2 and the two transistors remain conducting.

On an internal fault, one set of pulses on each AND circuit will be of opposite polarity from their mates. This means that the input to AND 1 will be negative for a short period of time (less than 8 milliseconds) and that the input to AND 2 will be negative for another period of time. (Less than 8 milliseconds). As a result, either Q1 or Q2 will stop conducting during these periods of negative potential to cause Q3 to conduct. Base drive is then removed from Q8 through R35. If the fault detector has operated, Q8 will stop conducting to apply posititive potential to capacitor C2. Four milliseconds later, the potential on C2 breaks down the Zener diode Z3 to allow base current to flow into Q9. This turns on Q9 to provide a zero input at:

1. Terminal 6 of the Arming Board.
2. Counting circuit of the 2/3 count circuit of the Arming Board. (On the internal fault, small positive pulses are applied to the base of Q8 each half cycle. These pulses are created by the difference in pulse widths of the local and remote signals see fig. 27. This small difference insures that the timer can be reset and activated three separate times.)
   The 2/3 count circuit consists of several NAND gates connected such that they will count the number of times that a zero is obtained from transistor Q9. However, the count circuit cannot be activated until the "0" on pin 5 of AND 6 is removed. This is accomplished by terminal 5 of the Arming Board going negative. This condition occurs when the transient block circuit on the Output Board is activated. The first count will then occur with the first conduction of Q9. This will set the output of the flip-flop of AND 5 and AND 6 to a "0".

   a. Pin 1 (IC1) goes to "0" to set pin 3 (IC1) at a "1".
   b. Pin 4 (IC1) and Pin 5 (IC1) is thus at a "1" condition.
   c. Pin 6 (IC1) goes to a "0" to apply a "1" to pin 13 (IC1) of the flip-flop of AND 7 and AND 8.

The second count will occur when pin 3 (IC3) of AND 9 and AND 10 goes to a "0". This will arm the flip-flop circuit of AND 11 and AND 12 such that the output of AND 13 will change to a "0" when Q9 changes to a "0" for the third time. The output of AND 13 (terminal 10 of the Arming Board) will remain until the counting chain is reset at terminal 5 by changing to a "1". This will occur when the transient blocking circuit of the Output Board is reset.

6. **OUTPUT BOARD**

Signals from the Arming Board are applied to the Output Board of figures 11 and 12. With reference to figure 11, the following results will occur when the various inputs to the Output Board are activated.

a. **Fault Detector Operation Only**

Positive potential is applied to both terminals 9 and 19 of the Board.

1. **Arming of Flip-Flop**
   With reference to the positive input to terminal 19 one condition of trip is set up. Q1 will turn on to cause Q2 to stop conducting. The collector of Q2 will go to positive potential which will interrupt the base current path of D9 and R36 of Q11. This will not turn Q11 off since Q11 base current has an additional path to negative through R39 and R40. However, one condition (arming) for trip has been set up on the trip flip-flop (AND 4 and AND 5).
2. **Transient Block**
   With reference to the application of a positive input to terminal 9 of the Output

Board, Q3 will turn on to cause Q4 to turn on. Turning on Q4 will apply positive potential to TP4. This positive potential will:

a. Charge capacitor C2.
b. Turn on Q6 to connect the collector of Q6 to negative potential. This will turn off Q8 and apply positive potential to capacitor C6 through the path of Q11 collector (TP6), R28, Z5, and D8. Twenty-two (22) milliseconds later, the potential on C6 breaks down the Zener diode Z6 to allow base current to flow into Q9. Q9 turns on to connect diode D10 to negative potential. A path for Q11 base current is then established through R37, D10, and Q9 to negative. This condition prevents Q11 from turning off. Thus, a trip inhibit signal is applied to Q11 after a 22 millisecond time delay (transient block).

b. **Fault Detector Reset Only**

When the fault detector resets, positive input is removed from terminal 9 and 19 of the Output Board. With the removal of voltage on terminal 19, Q1 turns off to turn Q2 on. The Q11 base current path of R36, D9 and Q2 is re-established and the arming signal is removed from the trip flip-flop.

0/1000 Time Delay

With the removal of positive potential from terminal 9, Q3 turns off. This turns off Q4 to remove positive input to TP4. However, capacitor C2 is charged to positive potential and will discharge through R11, R16 and D3 into the base of Q6. As a result, Q6 will remain turned on until the charge on capacitor C2 is reduced below the "potential hill" of D3 and Q6. This will require approximately 1000 milliseconds during which time Q8 does not conduct and Q9 remains turned on. As a result, transient blocking (Q11 base current path of Q9, D10, and R37) is maintained for 1000 milliseconds after the fault detector is reset.

c. **Trip Condition**

For a trip signal to appear on terminals 1 and 13 of the Output Board, two input signals have to be present at the input terminals of the Output Board within 22 milliseconds after the fault detector operates. These are:

1. Positive potential at terminal 19. (Fault Detector Operation)
2. Negative potential at terminal 6. (Output from 4/0 timer of Arming Board)

With application of positive potential at terminal 19, Q1 will turn on to turn off Q2. The Q11 base current path of R36, D9, and Q2 will be removed and the flip-flop circuit is armed.

With the application of negative potential at terminal 6 (due to Q9 of the Arming Board turning on), base current will flow from positive potential, through Q10 to R33 and Zener diode Z10 to negative. As a result, Q10 will turn on and apply positive potential to the junction of resistors R39 and R40 of the Output Board. This prevents the flow of Q11 base current through R39 and R40, and Q11 turns off. With Q11 turned off, positive potential is removed from:

a. R28, Z5, D8, and C6 to prevent the activation of transient block.
b. Junction of Resistors R42, and R43. As a result, current flows through Z7, emitter-base of Q12, R42 and R43 to negative. Q12 turns on to apply positive potential to Q13. Q13 turns on to turn on Q14. When Q14 turns on, positive potential is applied to:
   1. Base of transistor Q15 to turn on transistor Q15.
   2. Terminal 13 of the Output Board to provide a trip voltage to the next device in the relay system.

3. To D1. From D1, the voltage is applied to Capacitor C3, resistor R13 and Resistor R14. Applying the voltage to resistor R14 causes base current to flow into transistor Q5. Q5 will turn on to discharge capacitor C2 and to turn off Q6. This will turn on Q8. Hence, with a trip output, the 0/1000 timer (C3) is reset and transistor Q8 is turned on. With the removal of the trip output, capacitor

C3 will discharge through R14 to maintain Q5 conducting for approximately 100 milliseconds. This time delay assures that the 0/1000 timer is completely reset during the reclosing cycle.

d. **Reset of Transient Blocking**

On the clearing of a fault on an adjacent line section, the filter circuits in the SKBU-2A have stored energy which will be dissipated at fault clearing. This stored energy may cause a misalignment of pulses to allow an output from the 4/0 timer with the fault detector in an operate condition. To prevent operation of the relay under this condition, transient blocking is utilized. With transient blocking, the relay is setup to prevent tripping 22 milliseconds after the fault detector has been picked up. (At the inception of the fault). It can only be reset in 1 of 2 ways.

a. By reset of the fault detector which removes a positive input at terminal 9 of the Output Board. 1000 milliseconds later, transient blocking will reset.
b. By a negative input at terminal 10 of the Output Board. This input is supplied by the output of the 2/3 count circuit of the Arming Board. The 2/3 count circuit output is obtained by the activation of transient block and three separate outputs from the 4/0 timer. These conditions are produced in service on the power system by an external fault followed by an internal fault. Such an event of faults is referred to as a sequential fault.

The fault detector will operate on the external fault but tripping will not occur because the lineup of the local and remote pulses will not activate the 4/0 timer circuit. As a result, transient blocking will be setup 22 milliseconds after the fault detector has operated. If an internal fault now occurs, the phase angle of the fault current will change at the inception of the internal fault. The pulse lineup of the local and remote circuits will change in polarity to allow the 4/0 timer to be activated one time. Tripping will not occur after the first 4 milliseconds even though positive potential is applied to terminal 19 and negative potential is applied to terminal 6 of the Output Board. Transient blocking (Q9 conducting) will prevent tripping. Tripping can only occur in this case with three conditions:

1. Positive input to terminal 19 of Output Board.
2. Negative input to terminal 6 of Output Board.
3. Negative input to terminal 10 of Output Board.

Operation of the 2/3 count circuit will apply negative potential to terminal 10 of the Output Board. Base current will flow from positive potential, through Z4, to emitter base of Q7, to R22, diode D5 and D4 to negative. Q7 will turn on which will apply positive potential to capacitor C5 and Resistor R24. With the application of positive potential to resistor R24, base current flows into Q8. This turns Q8 on to discharge capacitor C6 and turn off transistor Q9. Transient block is thus reset and the three conditions for operation of the flip-flop are fulfilled. The flip-flop will operate to produce a voltage output on terminal 13 of the Output Board.

The reset of transient block will also reset the 2/3 count circuit of the Arming Board. This will turn off transistor Q7 of the Output Board. However, the voltage on capacitor C5 will maintain Q8 conducting until the base path of R25 and D7 is activated. (This path is activated by the trip output turning on transmitter Q5 which turns off transistor Q6.)

The timing waves of Figure 24 show the performance of the logic circuits of fig. 6 for a sequential fault (an external fault followed by an internal fault)

With reference to fig. 19 and 24, for the external fault, the local and remote signals overlap such that no output is obtained from the AND circuits of the Arming Board. Consequently, the 4/0 timer is inhibited from operating and AND 4 of the Output Board does not change states. Eight (8) milliseconds after time A, the fault detector may operate to provide an input to AND 5 of the Output Board. (Through OR 2, AND 3. LINE DRVR. and BUFF. of the ARMING BOARD). If the fault detector

operates, 22 ms later, OR5 of the Output Board changes states to place a second inhibit signal on AND 5 of the Output Board (through OR3 of Arming Board) upon the occurance of the internal fault at time B, a set of pulses (either remote or local) on the AND circuits of the Arming Board change phase relationship with reference to their mates. For the case of the timing waves of Fig. 24 the remote pulses change polarity. The 4/0 timer of the Arming Board is activated and 4 milliseconds later OR4 changes states. Because of this change in state AND 4 of the Output Board removes its inhibit signal from AND 5. However, a trip does not occur as OR 5 of the Output Board has an inhibit signal on AND 5. Before this inhibit signal can be removed, the 2/3 count input to terminal 10 of the Output Board has to change state. This is accomplished by a counting circuit on the Arming Board. This circuit counts the number of times an output is obtained from the 4/0 timer. After the 4/0 timer has been activated three separate times (at time C), the output of the 2/3 count circuit of the Arming Board changes state. This removes the inhibit signal from OR 5 on AND 5 of the Output Board to allow tripping. Transient Blocking is removed which resets the counting chain of the Arming Board.

The 4/0 timer is reset each half cycle by small pulses created by the discrepancy in pulse widths of the local and remote signals. This discrepancy insures that the timer can be reset and activated three separate times.

In the case of internal faults other than sequential faults, the phase relationship of the local and remote pulses change states as shown at time B of the timing waves. However, fault detector operation occurs 8 milliseconds after time B. Hence, the 4/0 timer is activated before transient blocking, and trip will occur without the 3 count circuit being activated.

7. **PR INTER BOARD** (Protective Relay Interface Board) Fig. 18
The protective relay board includes the interface to the protective relays as well as the auxiliary circuits associated with the protective relays. This board contains a 6/0 timer, 2500 sustained arming timer, and a 10/150 signal squelch timer.

a. Signal Squelch Timer
When an input is applied to terminal 18 of the protective relay board, positive potential is applied to base of Q10, Q10 turns on to provide a discharge path for C8 through R41. 10 milliseconds after the input to terminal 18, Q11 turns off to turn on Q12. Turning on Q12 applies a negative input to the keying circuit of the amplifier and keying board which keeps the keying transistor from turning on.

Upon removal of the input to terminal 18 of the protective relay board Q10 turns off to apply positive potential to C8. 150 milliseconds later Q11 turns on to turn off Q12 which removes negative potential to the keying circuit.

b. Sustained Arming Alarm (2500 Timer)
When arming occurs, positive potential is applied to terminal 1 and capacitor C3 of the PR INTER Board from terminal 19 of the arming board. Two-and-a-half seconds later, the potential on C3 breaks down the Zener diode Z8 to allow base current to flow into Q5. This turns on Q5 which turns off Q6. Turning Q6 off applies positive potential to the base of Q7 and Q7 turns off. This removes positive potential from R26 and an external alarm is energized.

c. Arming Delay by Distance Fault Detectors
(6/0) Timer)
The distance supervision arming is delayed by 6 milliseconds to allow time for the circuits feeding AND 1 and AND 2 to respond at fault inception. Operation of the distance fault detectors will apply positive potential to the protective relay board. This turns on Q1 which removes the base current to transistor Q2, Q2 turns off and positive potential is applied to capacitor C2. Six milliseconds later the voltage on C2 reaches a value to break down Zener diode Z7. This turns on Q3,

which connects the base of Q4 to negative through resistor, R15. Q4 turns on to apply positive potential to resistor, R16 and terminal 2. From terminal 2 the voltage is applied to the arming board.

CHARACTERISTICS

Taps are available in the relay to set the sensitivity to different combinations of positive, negative, and zero sequence components of the line current. The T taps on the left hand tap plate indicate the balanced three phase positive sequence amperes which will operate the fault detector FD. These taps are as follows:

3, 4, 5, 6, 7, 8 and 10.

For distance fault detector applications, the user should reset the SKBU-2A fault detector for a pick-up of twice tap value by means of the trimpot at the front of the fault detector board.

Positive and Negative Sequence Current-R1 Taps

The upper half of the right hand tap plate of R1 taps changes the number of turns on the third winding of the mutual reactor. This reapportions the components of the sequence network which changes the positive and negative sequence sensitivity of the fault detector. Operation of the fault detector with the various taps is given in the following table:

TABLE I

COMB.	SEQUENCE COMPONENTS IN NETWORK OUTPUT	TAPS ON RIGHT HAND TAP BLOCK		FAULT DETECTOR PICK-UP †	
		R_1	R_0#	3Ø FAULT	ØØ FAULT
1	Pos., Neg., Zero	C	G or H	Tap Value	86% Tap Value (53% on BC Fault)
2	Pos., Neg., Zero	B	G or H	2 x Tap Value	90% Tap Value (65% on BC Fault)
3	Neg., Zero	A	G or H	—	100% Tap Value

– Taps F, G and H are zero-sequence taps for adjusting ground fault sensitivity. See section on zero-sequence current tap.

† – When taps A and 3, or B and 3 are used, the fault detector will pickup 10 to 15 percent higher than the above values because of the variation in self-impedance of the sequence network and the saturating transformer.

Zero Sequence Current – R_0 Taps

The lower half of the right-hand tap plate (R_0 taps) is for setting the response of the relay to ground faults. Taps G and H give the approximate ground fault sensitivities listed in Table II. Tap F is used in applications where no response to zero sequence current is required. When this tap is used, the voltage output of the network caused by zero-sequence current is eliminated.

NOTE: Because of inherent characteristics of the sequence network, there will be small variations (from the values listed in Tables I and II) in the pick-up current for various phase or ground fault combinations.

TABLE II

COMB.	R_1 TAP	GROUND FAULT PICK-UP	PERCENT OF T TAP SETTING
		TAP G	TAP H
1	C	25%	12%
2	B	20%	10%
3	A	20%	10%

The operating time of the fault detector of the SKBU-2A is shown in Fig. 25. As shown in the figure, the fault detector has a maximum and minimum value. This is due to the point on the current wave that fault current is applied as well as the affect of the Pulse Width Detector. Fig. 26 shows the operating times for different points on the fault wave for ground fault current of 3 amperes.

Operating Time .....15 to 22 Milliseconds
Alarm .....2.5 seconds for FD operation
150 Milliseconds Loss-of-Channel
Transient Block Time .....22 to 25 Milliseconds
Transient Unblock Time 23 to 27 Milliseconds

Ambient Temperature Range ....-20°C to 55°C
dc Drain .....0.28 Amps at 48 Volts DC
Reset Time of Transient Block
1. After Fault Detector has Operated .....1000 Milliseconds
2. When unblock time is utilized 25ms

ENERGY REQUIREMENTS

Burdens measured at a balanced three-phase current of five amperes.

Relay Taps	PHASE A		PHASE B		PHASE C	
	VA	Angle	VA	Angle	VA	Angle
A-F-3	2.4	5°	0.6	0°	2.5	50°
A-H-10	3.25	0°	0.8	100°	1.28	55°
B-F-3	2.3	0°	0.63	0°	2.45	55°
B-H-10	4.95	0°	2.35	90°	0.3	60°
C-F-3	2.32	0°	0.78	0°	2.36	50°
C-H-10	6.35	342°	3.83	80°	1.98	185°

Burdens measured at a single-phase to netural current of five amperes.

Relay Taps	PHASE A		PHASE B		PHASE C	
	VA	Angle	VA	Angle	VA	Angle
A-F-3	2.47	0°	2.1	10°	1.97	20°
A-H-10	7.3	60°	12.5	53°	6.7	26°
B-F-3	2.45	0°	2.09	15°	2.07	10°
B-H-10	16.8	55°	22.0	50°	12.3	38°
C-F-3	2.49	0°	1.99	15°	2.11	15°
C-H-10	31.2	41°	36.0	38°	23.6	35°

The angles above are the degrees by which the current lags its respective voltage.

SETTINGS

Continuous Ratings:

The Continuous Rating of the SKBU-2A Relay is 10 amperes. The two second overload rating of the SKBU-2A is 150 A phase and 125 A ground.

If settings in between taps are desired, the tap screw should set in the next lowest tap. Trim Pot on FD board should then be adjusted for the desired pickup value.

The SKBU-2A relay has separate tap plates for adjustment of the phase and ground fault sensitivities and the sequence components included in the network output. The method of determining the correct taps for a given installation is discussed in the following paragraphs.

Setting Principles

Tap C provides the best balance between 3-phase and phase-to-phase fault sensitivity. Always use this tap where distance fault detector supervision is used. Where only the SKBU-2A fault detector is used and where the full load current (maximum through any terminal) is approximately five amperes or more, tap B will provide increased phase-to-phase fault sensitivity with little or no sacrifice in 3-phase fault sensitivity. For example, if a left-hand tap (T) of 6 is needed with tap C (6C), then use a 3 B setting instead.

NOTE: From Table I, pickup will be 105% of Tap 3 on 3B and 90% of Tap 6 for ØA to ØB fault. 3Ø pickup is 6 amp. both settings.

Use tap A only where satisfactory unbalanced fault sensitivity cannot otherwise be obtained and where other protection is available for 3-phase faults. Since with Tap A, no 3-phase fault protection is available.

In all cases provide identical response at all stations to insure proper phase comparison and adequate keying for any fault detected by remote-end relays. To accomplish this, the letter taps (A, B, C, F, G, H) should be identical at all stations. Also, the taps should be identical with CT ratios, or inversely proportional to CT ratios where different.

After selecting tap C or B, pick the T tap to allow reset of the fault detector in the presence of load flow. That is, fault detector pick-up should be at least 111 percent of full load current (maximum through any terminal).

Now select tap G or H for desired ground-fault sensitivity.

For distance fault detector applications, set 3C to provide the maximum sequence-network voltage for the squaring amplifiers. The SKBU-2A current fault detector is then independently desensitized (by adjustment trim pot on FD board) to permit reset in the presence of full-load current. Phase faults which do not operate the SKBU-2A fault detector will be detected by the supplementary distance fault detectors.

EXAMPLE

Assume a two-terminal line with current transformers rated 400/5 at both terminals. Also assume that full load current is 300 amperes, and that a minimum intenal phase-to-phase faults of 2000 amperes is fed in from one end and 600 amperes from the other end. Further assume that on minimum internal ground faults, 400 amperes is fed in from one end, and 100 amperes from the other end. No distance fault detectors are employed.

POSITIVE-SEQUENCE CURRENT TAP

Secondary Values:

$$\text{Load Current} = 300 \times \frac{5}{400} = 3.75 \text{ amperes} \quad (1)$$

Minimum Phase-to-Phase Fault Currents:

$$600 \times \frac{5}{400} = 7.5 \text{ amperes} \quad (2)$$

Fault detector setting (three phase) must be at least:

$$\frac{3.75}{0.9} = 4.18 \text{ amperes (0.9 is dropped ratio of fault detector. Setting will insure that the fault detector will reset on load current.)} \quad (3)$$

In order to complete the trip circuit on a 7.5 ampere phase-to-phase fault, the fault detector pick-up from Table I must not be more than:
(based on a three phase fault)

$$7.5 \times \frac{1}{0.86} = 8.7 \text{ amperes} \quad (4)$$

ZERO SEQUENCE TAP

Secondary Value:

$$100 \times \frac{5}{400} = 1.25 \text{ amperes minimum ground fault current}$$

With T, tap 6 and R1 Tap B in use, the fault detector pick-up currents for ground faults (See Table II) are as follows:

Tap G $0.2 \times 6 = 1.2$ amperes

Tap H $0.1 \times 6 = 0.6$ amperes

From the above, tap H would be used to trip for a minimum ground fault of 1.25 amperes.

SEQUENCE COMBINATION TAP

From a comparison of (3) and (4) above it is evident that the fault detector can be set to trip under minimum phase fault conditions and yet not operate under maximum load. From (3) we can select tap 5 (T). In this case, also select tap C (R_1). Current tap (6) would be used in preference to tap 5 to allow for occurrence of higher load current. However, if more margin is desired over load current, instead of setting 6C, use 3B for improved phase-to-phase fault sensitivity.

INSTALLATION

The relays should be mounted on switchboard panels or their equivalent in a location free from dirt, moisture, excessive vibration and heat. The maximum ambient temperature around the chassis must not exceed 55°C. Mount the relay by means of the four slotted holes on the front of the case. Additional support should be provided toward the rear of the relay in addition to the front panel mounting. This will protect against warping of the front panel due to the extended weight within the relay case. Ground relay chassis with No. 12 AWG copper wire to grounding post.

ADJUSTMENTS AND MAINTENANCE

NOTE: The phase comparison relay is normally supplied as part of a relaying system, and its calibration should be checked after the system has been installed and interconnected. Details are

given in the instructions of the assembly. **The assembly instructions and not the following instruction should be followed when the relay is received as an integral part of the relaying system.**

In those cases where the relay is not part of a relaying system, the following procedure will verify that the circuits of the relay are functioning properly.

TEST EQUIPMENT

1. Oscilloscope (Dual Trace)
2. AC Current Source
3. Electronic Timer
4. AC Voltmeter
5. DC Voltmeter
6. Single Pole Single Throw Switch

ACCEPTANCE TEST

Connect the relay to the test circuit of Fig. 28 which represents the channel equipment for test purposes.

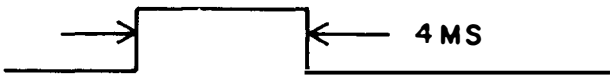
The following tests are in reference to an individual relay separated from a system. If a recalibration of the circuits is desired, the recalibration in certain cases can be done with the relay connected in the system. Those tests that can be made in the system will be so designated in the following procedures.

Caution: The following tests involve a single relay but some system type tests are being described. If the relay is tested in a relay system, the remote line terminal should be disengaged from the trip circuit of the breaker by means of the relay system test switches.

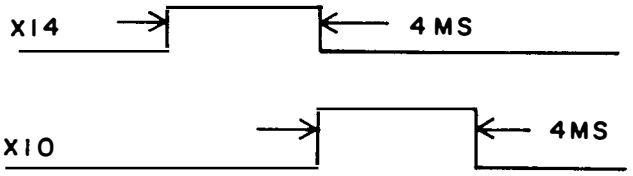
1. **FD Pickup and Dropout**
   Not a system type test. Requires an adjustable test current.
   a. Set relay on taps 5, C, and H.
   b. Connect a high resistance dc voltmeter across X22 and X4 (neg.)
   c. Apply 60 hertz current to terminals 1 and 3 of the relay. Gradually increase the current until the voltmeter changes reading from approximately zero volts to 20 volts. This is the operating current of the fault detector and should occur at values of current whithin the limits of 4.33 ± 5% amperes.
   d. Gradually lower ac test current until the dc voltmeter drops to approximately zero volts. This is the dropout current of the fault detector and should occur at values of current greater than 3.80 amperes.
   e. Pickup of the fault detector should not be erratic at pickup. The waveform of voltage across X21 to X4 (grd.) should be as follows for positive results at pickup. (Output of Phase Splitter)

   f. Adjustment of pickup can be made by means of the trim pot on front of the fault detector board. There are no adjustments for either the dropout ratio or the phase splitter.

2. **Pulse Width Detector**
   Not a system type test. Requires a test current.
   a. Place a scope probe into X14 with ground on X4. Place a second probe of scope into X10. Close switch A of test circuit. (Note: Switch A connects the keying circuit of the SKBU-2A to the channel transmitter)
   b. Apply ac current (approximately 0.2 amperes) into terminals 1 and 3 until the pulse width on X14 is as follows:



   c. Adjust the vertical trim pot. on the fault detector board until the following relationship is observed on X14 and X10.



d. Raise the ac current slightly. The pulse on X10 should change to a constant zero.

3. **Timers Associated With Fault Detectors.**

No ac current to be applied to the relay during these tests. Hence, tests can be performed in a system as well as with the test circuit of Fig. 28.

NOTE: A scope is specified in the following tests to measure time delay. The accuracy of the scope on the time scale would be verified by checking against a 60 hertz waveform. (1 cycle = 16.7 milliseconds) If an electronic timer is used, timer start would be considered the external trigger of scope. Timer stop would be the points to which the scope probe is connected.

a. **Fault Detector Time Delay**
(8 to 10 milliseconds)

1. Connect scope probe across X22 and X4 (grd.)
2. Connect X21 to X2 through a SPST switch. (Closure of the switch will simulate a fault detector operation.)
3. Trigger scope on X2. Set scope trigger on external, positive slope.
4. Close SPST switch. Scope should sweep and voltage on scope should change from 0 to 20 volts as shown in the following sketch:

b. **Transient Block Delay** (22 to 25 milliseconds pick-up—950 to 1050 milliseconds dropout)

1. Connect scope probe to X7 and X4 (grd.)
2. Connect scope trigger to X3. Set scope trigger on external, positive slope.
3. Close PR1 switch of test circuit if test fixture is used. Otherwise connect a SPST switch across terminal 7 of the Protective Relay Board (PR INTER) and terminal 4 of the same board. (**Note:** This test simulates a distance fault detector operation). Scope should change from 18 volts to zero in 22 to 25 milliseconds as illustrated in the following sketch.

4. Set scope on negative slope.
5. Open PR1 switch. (or SPST switch) Voltage on scope will rise from zero to 18 volts in 950 to 1050 milliseconds.

c. **Sustained Arming Timer**
(2300 to 2700 milliseconds)

1. Connect scope probe to X20 and X4 (grd.)
2. Trigger scope on X3. Set scope trigger on external, positive slope.
3. Close PR1 switch if test fixture is used. Otherwise connect a SPST switch across terminals 7 and 4 of the Protective Relay Board (PR INTER). (**Note:** This test simulates a distance fault detector operation.) Voltage on scope will change from 20 volts to zero volts in 2300 to 2700 milliseconds.

4. **Lineup of Local and Remote Pulses**

Note: This is a system type test that requires a signal from the remote terminal. Hence, the test switches in a system type test have to be set in an external fault condition. Lineup of the pulses should be made as follows before the system is put into service.

Test circuit of Fig. 28 can be used to check the relay but not to put the relay system in service.

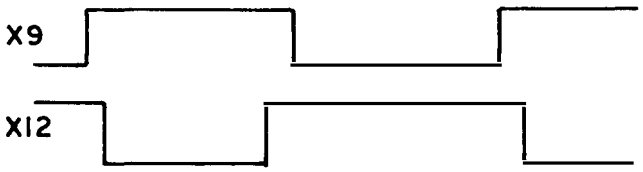
a. Place one scope probe on X9 and X4 (grd.) and a second scope probe on X12.

b. Close switches A, B, C, E, and F. Open

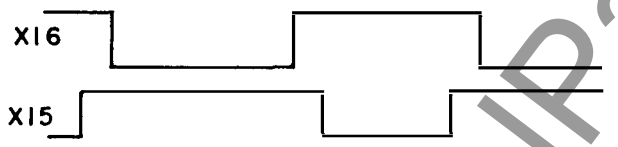
switch I. Set L on external fault. (Test fixture simulates receiving a signal from the remote line terminal-with the system functional test switches set up in an external fault condition.)

c. Apply 6.0 to 8.0 amperes ac into terminals 1 and 3. (If a system-type test is utilized, use the test current supplied by the test transformer.)

d. Adjust the lower trim pot. on the front of the Amplifier and Keying Board (AMPL. AND KEY) until the pulses line up as follows:



e. Connect scope probe in X15 and X16 and adjust the upper trip pot. on the Amplifier and Keying Board (AMPL. AND KEY) until the pulses line up as follows:



5. **4/0 TIMER** 4 to 4.4 milliseconds

Note: The following is a system type test. Signals must be received from the remote terminals and the system functional test switches set in an external fault positions.

Tests can also be made with the test circuit of Fig. 28.

a. Connect a scope probe to TP3 and terminal 8 (grd.) of the ARMING BOARD.

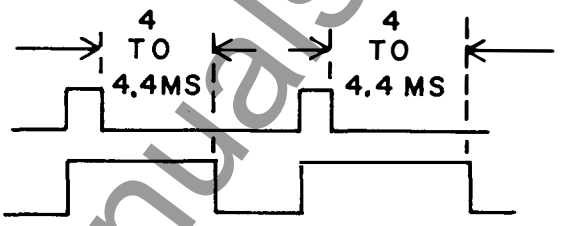
b. Connect a second probe of scope to terminal 6 of ARMING BOARD.

c. Connect a dc voltmeter from X11 to X4 (grd.) This is the trip output and the voltmeter should read zero volts.

d. Apply 6.0 to 8.0 amperes ac into terminal 1 and out terminal 3. (If relay is connected in a system, use test current supplied by the test transformers)

e. Close switch L to internal fault. Voltmeter should read 20 volts dc. (Note: In system functional test units, the test switches must be set up in an internal fault position)

f. The difference in transition time between TP3 and terminal 6 going negative will be 4 to 4.4 milliseconds as illustrated in the following sketch.



6. **Three-Count Circuit**

The following tests can be performed either in the system or with the test circuit of Fig. 28

No ac current is to be applied to the relay during the tests.

a. Connect a SPST switch from TP3 to terminal 8 (grd.) of the ARMING BOARD

b. Connect second probe of scope to X11. (trip output) Voltage will be zero volts.

c. Close PR1 switch or jumper X22 to X2. (This simulates a fault detector operation.)

d. Close SPST switch one time. Voltage should not change on X11. Open SPST switch.

e. Close SPST switch second time. Voltage should not change on X11. Open SPST switch.

f. Close SPST switch third time. Voltage on X21 should change to 20 volts dc. Open SPST switch voltage on X11 should remain 20 volts.

g. With SPST switch open and X11 voltage at 20 volts dc, Close and then release the test reset switch on the front panel of the SKBU-2A Relay. The voltage on X11 should change to zero volts.

h. If a re-check of the three count circuit is desired, the test reset switch should be closed first and then released before closing the SPST switch across TP3 and terminal 8 of the ARMING BOARD.

7. **Fast Rest Timer** 80 to 120 milliseconds

The following tests can be performed either in the system or with the test circuit of Fig. 28.

No ac current is to be applied to the relay during the tests.

a. Connect SPST switch across TP3 and terminal 8 of the ARMING BOARD.

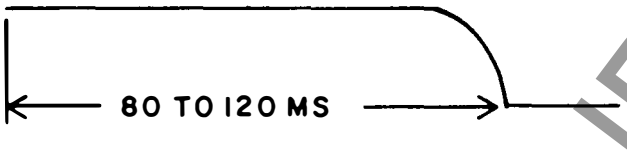
b. Place scope probe across TP6 and terminal 8 (grd.) of the OUTPUT BOARD.

c. Connect scope trigger to X11. Set trigger on external, negative slope.

d. Close PR1 switch or jumper X22 to X2 to simulate a fault detector operation.

e. Open and close the SPST switch three times to obtain a trip output on X11.

f. Close and release the test reset switch on the SKBU-2A. The scope should sweep and change states as follows:



8. **Signal Squelch Timer**
8 to 12 milliseconds pickup
130 to 180 milliseconds dropout

a. Connect scope probe to TP8 of Protective Relay Interface Board (PR INTER) with ground on terminal 8. Zero volts will appear on scope.

b. Trigger scope on timer start of pilot trip switch. (If relay is connected in a system, connect a SPST switch between terminal 18 and 4 of Protective Relay Interface Board)

c. Close pilot trip switch (or SPST switch) Scope should sweep and voltage should change from approximately 0 to 16 volts in 8 to 12 milliseconds.

d. Set scope on negative slope.

e. Open pilot trip switch (or SPST) Voltage on scope should change from approximately 16 to zero volts in 130 to 180 milliseconds.

9. **Low Signal timer #1** 130 to 180 milliseconds.

Following procedures are to be used where test circuit of Fig. 28 is utilized.

a. Connect scope proble across X19 and X4 (grd.) Set switch L to internal fault position.

b. Trigger scope on timer start of switch L. Set scope trigger on external, positive slope.

c. Close switches B, C, and G.

d. Close switch L to external fault position. Scope will sweep and voltage will change from approximately 0 to 20 volts in 135 to 165 milliseconds.

e. Open switches B, C, and G. Set L to internal fault position.

The following procedure is to be used where relay is connected in a system:

Channel condition has a bearing on the results of this test. The local terminal must be receiving a steady space signal from the remote terminal. Hence, ac current should not be applied to either relay terminal. To determine if the status of the channel equipment is as specified, check the voltage across terminal 13 to terminal 8 of the Supervision Board (SUPRV. BOARD). Voltage should be approximately zero volts. Also the voltage across terminal 12 to terminal 8 of the Supervision Board should be approximately 13.5 volts dc.

a. Connect SPST switch from terminal 10 to terminal 4 of the Supervision Board (SUPRV. BOARD).

b. Connect scope probe to terminal 18 of the SUPRV. BOARD with ground on terminal 8 of the board.

c. Trigger scope on terminal 10 of the SUPRV. BOARD. Set scope trigger on positive slope.

d. Close SPST switch. Scope should sweep and change from approximately zero volts to 20 volts in 130 to 180 milliseconds.

10. **Low Signal Timer #2** 130 to 180 milliseconds.

Following procedures are to be used where test circuit of Fig. 28 is utilized.

a. Connect scope probe across X19 and X4 (grd.) Set switch L to internal fault position.

b. Trigger scope on timer start switch of switch L. Set scope trigger on external, positive pulse.

c. Close switches E, F, and G.

d. Close switch L to external fault position. Scope will change from zero volts to 20 volts in 135 to 165 milliseconds.

Following procedure is to be used where relay is connected in a system.

Channel condition has a bearing on the results of this test. The local terminal must be receiving a space signal from the remote terminal. Hence, no ac current should be applied to either terminal. To determine if the status of channel equipment is as specified, check the voltage across terminal 17 to terminal 8 of the Supervision Board (SUPRV. BOARD). Voltage should be approximately zero volts. Also the voltage across terminal 16 to terminal 8 of the Supervision Board should be approximately 13.5 volts dc. In case the voltage from terminal 17 to terminal 8 is not zero volts, connect a jumper from terminal 4 to terminal 2 of the Supervision Board. This latter condition could occur if the relay system is a two-terminal application instead of a three-terminal application.

a. Connect SPST switch from terminal 2 to terminal 4 of the Supervision Board. (SUPRV. BOARD)

b. Connect scope probe to terminal 18 of the SUPRV. BOARD with ground on terminal 8 of the board.

c. Trigger scope on terminal 2 of the SUPRV. BOARD. Set scope trigger on positive slope.

d. Close SPST switch. Scope should sweep and change from approximately zero volts to 20 volts in 130 to 180 milliseconds.

TROUBLE SHOOTING PROCEDURE

To trouble shoot the equipment, the logic diagram of fig. 19 should be used to isolate the circuit that is not performing correctly. The schematic of the individual board, should then be used to isolate the faulty component.

RENEWAL PARTS

Repair work can be done most satisfactorily at the factory. However, interchangeable parts can be furnished to the customers who are equipped for doing the repair work. When ordering parts, always give the complete nameplate data. For components mounted on the printed circuit board, give circuit symbol and the electrical value (ohms, mfd., etc.) and component style number.

ELECTRICAL PARTS LIST

Fault Detector Board Style 1456C49G01

CIRCUIT SYMBOL	DESCRIPTION	WESTINGHOUSE STYLE NUMBER
	Capacitor	
C1	.005 MFD 100V	184A663H13
C2	0.27 MFD 200V	188A669H05
C3	0.47 MFD	18A669H01
C4	.22 MFD	876A409H15
C5	0.47 MFD 200V	188A669H01
C6	1.500 MFD 35V	187A508H09
C7	0.470MFD 200V	188A669H01
C8	1.500MFD 35V	187A508H09
C9	0.010MFD 100V	763A219H24
C10	0.010MFD 100V	763A219H24
C11	500.000PF 500V	187A694H03
C12	500.000PF 500V	187A694H03
	Diode	
D1	IN457A	184A855H07
D2	IN457A	184A855H07
D3	IN457A	184A855H07
D4	IN457A	184A855H07
D5	IN457A	184A855H07
D6	IN457A	184A855H07
D7	IN457A	184A855H07
D8	IN457A	184A855H07
D9	IN457A	184A855H07
D10	IN457A	184A855H07
D11	IN645A	837A692H03
D12	IN645A	837A692H03
D13	IN414B	836A928H06
D14	IN414B	836A928H06
D15	IN414B	836A928H06
D16	IN414B	836A928H06
D17	IN414B	836A928H06
D18	IN414B	836A928H06
D19	IN414B	836A928H06
D20	IN4148	836A928H06
D21	IN4143	836A928H06
D22	IN457A	184A855H07
	INT CKT	
IC1	MC680L	6296D58H03
IC2	MC672L	6296058H01

CIRCUIT SYMBOL	DESCRIPTION	WESTINGHOUSE STYLE NUMBER
	Potentiometer	
R5	100.0K 0.75W	880A826H07
R22	1.0M 0.75W	880A826H02
	Resistor	
R1	50.0 ohms 5.00W 5%	185A209H06
R2	12.0K0.50W 2%	629A531H58
R3	5.1 0.50W 2%	629A531H49
R4	12.0K0.50W 2%	629A531H58
R6	20.0K0.50W 2%	629A531H63
R7	10.0K0.50W 2%	629A531H56
R8	12.0K0.50W 2%	629A531H58
R9	470.0 ohms 0.50W 2%	629A531H24
R10	12.0K0.50W 2%	629A531H58
R11	10.0K0.50W 2%	629A531H56
R12	270.0K0.50W 2%	184A763H85
R13	22.0K0.50W 2%	629A531H64
R14	470.0 ohms 0.50W 2%	629A531H24
R15	10.0K0.50W 2%	629A531H56
R16	10.0K0.50W 2%	629A531H56
R17	6.8 0.50W 2%	629A531H52
R18	82.0K0.50W 2%	629A531H78
R19	150.0 ohms 3.00W 5%	762A679H01
R20	150.0 ohms 3.00W 5%	762A679H01
R21	47.0 ohms 0.50W 5%	187A290H17
R23	150.0K0.50W 2%	629A531H84
R24	47.0 ohms 0.50W 2%	187A290H17
R25	1.0M0.50W 5%	184A763H99
R26	20.0K0.50W 2%	629A531H63
R27	47.0K0.50W 2%	629A531H72
R28	100.0 ohms 0.50W 2%	629A531H08
R29	3.3K0.50W 2%	629A531H44
R30	1.0K0.50W 5%	184A763H27
	Transistor	
Q1	2N3417	848A851H02
Q2	2N3417	848A851H02
Q3	2N3417	848A851H02
Q4	2N3645	848A441H01
Q6	2N6027	878A289H01
	Zener Diode	
Z1	IN1832C	184A617H06
Z2	IN957B 6.8V	186A797H06
Z3	IN957B 6.8V	186A797H06
Z4	IN3688A 24.0V	862A288H01
Z5	SZ15 15.0V	848A487H02

CIRCUIT SYMBOL	DESCRIPTION	WESTINGHOUSE STYLE NUMBER
Supervision Board Style 202C565G01		
	Capacitors	
C1	6.8 MFD	184C61H10
C2	0.27 MFD	188A669H05
C3	6.8 MFD	184A661H10
C4	0.27 MFD	188A669H05
	Diodes	
D1	IN645A	837A692H03
D2	IN645A	837A692H03
D3	IN645A	837A692H03
D4	IN645A	837A692H03
D5	IN645A	837A692H03
D6	IN645A	837A692H03
D7	IN645A	837A692H03
D8	IN645A	837A692H03
	Resistors	
R1	4.7 K .5W 2%	629A531H48
R2	4.7 K .5W 2%	629A531H48
R3	82 K .5W 2%	629A531H78
R4	10 K .5W 2%	629A531H56
R5	4.7 K .5W 2%	629A531H48
R6	4.7 K .5W 2%	629A531H48
R7	82 K .5W 2%	629A531H78
R8	10 K .5W 2%	629A531H56
R9	27 K .5W 2%	629A531H66
R10	27 K .5W 2%	629A531H66
R11	10 K .5W 2%	629A531H56
R12	47 K .5W 2%	629A531H72
R13	470 ohms .5W 2%	629A531H24
R14	10 K .5W 2%	629A531H56
R15	10 K .5W 2%	629A531H56
R16	6.9 K .5W 2%	629A531H52
R17	82 K .5W 2%	629A531H78
R18	150 ohms 3W	762A679H01
R19	4.7 K .5W 2%	629A531H48
R20	4.7 K .5W 2%	629A531H48
R21	82 K .5W 2%	629A531H78
R22	10 K .5W 2%	629A531H56
R23	4.7 K .5W 2%	629A531H48
R24	4.7 K .5W 2%	629A531H48
R25	82 K .5W 2%	629A531H78
R26	10 K .5W 2%	629A531H56
R27	27 K .5W 2%	629A531H66
R28	27 K .5W 2%	629A531H66
R29	10 K .5W 2%	629A531H56
R30	47 K .5W 2%	629A531H72
R31	470 ohms .5W 2%	629A531H24

CIRCUIT SYMBOL	DESCRIPTION	WESTINGHOUSE STYLE NUMBER
R32	10 K .5W 2%	629A531H56
R33	10 K .5W 2%	629A531H56
R34	6.8 K .5W 2%	629A531H52
R35	82 K .5W 2%	629A531H78
R36	150 ohms 3W	762A679H01
	Transistors	
Q1	2N3417	848A851H02
Q2	2N3417	848A851H02
Q3	2N3417	848A851H02
Q4	2N3417	848A851H02
Q5	2N3645	849A441H01
Q6	2N3417	848A851H02
Q7	2N3417	848A851H02
Q8	2N3417	848A851H02
Q9	2N3417	848A851H02
Q10	2N3645	849A441H01
	Zener Diodes	
Z1	IN3686B, 20 V	185A212H06
Z2	IN957B, 6.8 V	186A797H06
Z3	IN3686B, 20 V	185A212H06
Z4	IN957B, 6.8 V	186A797H06
Z5	IN957B, 6.8 V	186A797H06
Z6	IN3688A, 24 V	862A288H01
Z7	IN3686B, 20 V	185A797H06
Z8	IN957B, 6.8 V	186A797H06
Z9	IN3686B, 20 V	185A212H06
Z10	IN957B, 6.8 V	186A797H06
Z11	IN957B, 6.8 V	186A797H06
Z12	IN3688A, 24 V	862A288H01

Amplifier & Keying Board Style 1440C83G01

	Capacitor	
C1	.330MFD 200V	188A669H06
C2	.330MFD 200V	188A669H06
	Diode	
D1	IN645A	837A692H03
D2	IN645A	837A692H03
D3	IN645A	837A692H03
D4	IN645A	837A692H03
D5	IN645A	837A692H03
D6	IN645A	837A692H03

CIRCUIT SYMBOL	DESCRIPTION	WESTINGHOUSE STYLE NUMBER
D7	IN645A	837A692H03
D8	IN645A	837A692H03
D9	IN645A	837A692H03
D10	IN645A	837A692H03
D11	IN645A	837A692H03
D12	IN645A	837A692H03
D13	IN645A	837A692H03
	INT CKT	
IC1	747DM	1443C52H01
IC2	747DM	1443C52H01
IC3	MC680L	6296D58H03
IC4	MC672L	6296D58H01
IC5	MC660	6677D51H01
IC6	MC660	6677D51H01
	Potentiometer	
R18	50.0K .75W	880A826H06
R40	50.0K .75W	880A826H06
	Resistor	
R1	10.0K .50W 1%	848A820H45
R2	11.3K .50W 1%	848A820H50
R3	10.0K .50W 2%	629A531H56
R4	10.0K .50W 2%	629A531H56
R5	22.0K .50W 2%	629A531H64
R6	10.0K .50W 2%	629A531H56
R7	10.0K .50W 2%	629A531H56
R8	27.0K .50W 2%	629A531H66
R9	10.0K .50W 1%	848A820H45
R10	17.8K .50W 1%	848A820H69
R11	6.8K .50W 2%	629A531H52
R12	150.0 ohms 3.00W 5%	762A679H01
R13	10.0K .50W 2%	629A531H56
R14	10.0K .50W 2%	629A531H56
R15	10.0K .50W 2%	629A531H56
R16	2K .50W 2%	629A531H39
R17	47.0 ohms .50W 2%	187A290H17
R19	10.0K .50W 2%	629A531H56
R20	10.0K .50W 2%	629A531H56
R21	82.0K .50W 2%	629A531H78
R22	10.0K .50W 2%	629A531H56
R23	150.0 ohms 3.00W 5%	762A679H01
R24	6.8K .50W 2%	629A531H52
R25	6.8K .50W 2%	629A531H52
R26	6.8K .50W 2%	629A531H52
R27	6.8K .50W 2%	629A531H52

CIRCUIT SYMBOL	DESCRIPTION	WESTINGHOUSE STYLE NUMBER
R28	1.0K .50W 2%	629A531H32
R29	10.0K .50W 1%	848A820H45
R30	10.0K .50W 1%	848A820H45
R31	10.0K .50W 1%	848A820H45
R32	10.0K .50W 1%	848A820H45
R33	17.8K .50W 1%	848A820H69
R34	10.0K .50W 1%	848A820H45
R35	10.0K .50W 2%	629A531H56
R36	10.0K .50W 2%	629A531H56
R37	2K .50W 2%	629A531H39
R38	10.0K .50W 2%	629A531H56
R39	47.0 ohms .50W 5%	187A290H17
R41	10.0K .50W 2%	629A531H56
R42	10.0K .50W 2%	629A531H56
R43	1.0K .50W 2%	629A531H32
	Transistor	
Q1	2N3417	848A851H02
Q2	2N699	184A638H19
Q3	2N3417	848A851H02
Q4	2N3417	848A851H02
Q5	2N3645	849A441H01
Q6	2N3417	848A851H02
Q7	2N3417	848A851H02
	Zener	
Z1	IN957B 6.8V	186A797H06
Z2	IN957B 6.8V	816A797H06
Z3	SZ15 15.0V	848A487H02
Z4	UZ5875 75.0V	837A693H04
Z5	IN3686B 20.0V	185A212H06
Z6	IN705 4.8V	837A693H06
Z7	IN705 4.8V	837A693H06
Z8	IN9578 6.8V	186A797H06

Arming Board Style 1439C95G01

	Capacitor	
C1	.270MFD 200V	188A669H05
C2	.330MFD 200V	188A669H06
C3	.470MFD 50V	762A680H04
C4	.470MFD 50V	762A680H04
C5	.470MFD 50V	762A680H04
C6	.470MFD 50V	762A680H04

CIRCUIT SYMBOL	DESCRIPTION	WESTINGHOUSE STYLE NUMBER
	Diode	
D1	IN645A	837A692H03
D3	IN645A	837A692H03
D4	IN645A	837A692H03
D5	IN645A	837A692H03
D6	IN645A	837A692H03
D8	IN645A	837A692H03
D9	IN645A	837A692H03
D10	IN645A	837A692H03
D11	IN645A	837A692H03
D12	IN645A	837A692H03
D13	IN645A	837A692H03
D14	IN645A	837A692H03
D15	IN645A	837A692H03
D16	IN645A	837A692H03
D17	IN645A	837A692H03
D18	IN645A	837A692H03
D19	IN645A	837A692H03
	INT CKT	
IC1	MC672L	6296D58H01
IC2	MC680L	6296D58H03
IC3	MC672L	6296D58H01
IC4	MC672L	6296D58H01
	Resistor	
R1	22.0K .50W 2%	629A531H64
R2	22.0K .50W 2%	629A531H64
R3	22.0K .50W 2%	629A531H64
R4	22.0K .50W 2%	629A531H64
R5	22.0K .50W 2%	629A531H64
R6	22.0K .50W 2%	629A531H64
R7	22.0K .50W 2%	629A531H64
R8	22.0K .50W 2%	629A531H64
R9	22.0K .50W 2%	629A531H64
R10	10.0K .50W 2%	629A531H56
R11	22.0K .50W 2%	629A531H64
R12	10.0K .50W 2%	629A531H56
R13	22.0K .50W 2%	629A531H64
R14	22.0K .50W 2%	629A531H64
R15	10.0K .50W 2%	629A531H56
R16	22.0K .50W 2%	629A531H64
R17	22.0K .50W 2%	629A531H64
R18	22.0K .50W 2%	629A531H64
R19	22.0K .50W 2%	629A531H64
R20	10.0K .50W 2%	629A531H56
R21	10.0K .50W 2%	629A531H56

CIRCUIT SYMBOL	DESCRIPTION	WESTINGHOUSE STYLE NUMBER
R22	22.0K .50W 2%	629A531H64
R23	10.0K .50W 2%	629A531H56
R24	10.0K .50W 2%	629A531H56
R25	22.0K .50W 2%	629A531H64
R26	10.0K .50W 2%	629A531H56
R27	10.0K .50W 2%	629A531H56
R28	6.8K .50W 2%	629A531H52
R29	82.0K .50W 2%	629A531H78
R30	22.0K .50W 2%	629A531H64
R31	22.0K .50W 2%	629A531H64
R32	100.0 ohms 1.00W 2%	187A643H03
R33	150.0 ohms 3.00W 5%	762A679H01
R34	22.0K .50W 2%	629A531H64
R35	22.0K .50W 2%	629A531H64
R36	10.0K .50W 2%	629A531H56
R37	15.0K .50W 2%	629A531H60
R38	47.0 ohms .50W 5%	187A290H17
R39	10.0K .50W 2%	629A531H56
R40	10.0K .50W 2%	629A531H56
R41	1.0K .50W 2%	629A531H32
	Transistor	
Q1	2N3417	848A851H02
Q2	2N3417	848A851H02
Q3	2N3417	848A851H02
Q4	2N3417	848A851H02
Q5	2N3417	848A851H02
Q6	2N3417	848A851H02
Q7	2N3645	848A441H01
Q8	2N3417	848A851H02
Q9	2N3417	848A851H02
	Zener	
Z1	IN3688A 24.0V	862A288H01
Z2	SZ15 15.0V	849A487H02
Z3	IN957B 6.9V	186A797H06
Z4	IN957B 6.8V	186A797H06
Z5	IN957B 6.8V	186A797H06

Output Board Style 1448C15G03

	Capacitor	
C1	.047MFD 200V	848A437H04
C2	22.000MFD 35V	184A661H16
C3	3.300MFD 35V	862A530H01

CIRCUIT SYMBOL	DESCRIPTION	WESTINGHOUSE STYLE NUMBER
C5	.220MFD 100V	763A219H21
C6	4.700MFD 35V	184A661H12
C8	500.000PF 500V	762A757H26
C9	500.000PF 500V	762A757H26
C10	.220MFD 100V	763A219H21
C11	.100MFD 200V	188A669H03
C12	1.500MFD 35V	187A508H09
	Diode	
D1	IN645A	837A692H03
D2	IN645A	837A692H03
D3	IN645A	837A692H03
D4	IN645A	837A692H03
D5	IN645A	837A692H03
D6	IN645A	837A692H03
D7	IN645A	837A692H03
D8	IN645A	837A692H03
D9	IN645A	837A692H03
D10	IN645A	837A692H03
D11	IN645A	837A692H03
	Jumper	
J1	0 OHM RESISTOR	862A476H01
J2	0 OHM RESISTOR	862A478H01
J3	0 OHM RESISTOR	862A478H01
J4	0 OHM RESISTOR	862A478H01
	Resistor	
R1	4.7K .50W 2%	629A531H48
R2	4.7K .50W 2%	629A531H48
R3	82.0K .50W 2%	629A531H78
R4	10.0K .50W 2%	629A531H56
R5	6.8K .50W 2%	629A531H52
R6	27.0K .50W 2%	629A531H66
R7	10.0K .50W 2%	629A531H56
R8	10.0K .50W 2%	629A531H56
R9	10.0K .50W 2%	629A531H56
R10	6.8K .50W 2%	629A531H52
R11	2.0K .50W 2%	629A531H39
R12	100.0 ohms .50W 2%	629A531H08
R13	1.0K .50W 2%	629A531H32
R14	15.0K .50W 2%	629A531H60
R15	10.0K .50W 2%	629A531H56
R16	13.0K .50W 2%	629A531H59
R17	10.0K .50W 2%	629A531H56
R18	6.8K .50W 2%	629A531H52

CIRCUIT SYMBOL	DESCRIPTION	WESTINGHOUSE STYLE NUMBER
R21	22.0K .50W 2%	629A531H64
R22	6.8K .50W 2%	629A531H52
R23	47.0 ohms .50W 2%	187A290H17
R24	27.0K .50W 2%	629A531H66
R25	27.0K .50W 2%	629A531H66
R26	10.0K .50W 2%	629A531H56
R28	6.2K .50W 2%	629A531H51
R29	470.0 ohms .50W 2%	629A531H24
R30	470.0 ohms .50W 1%	184A764H91
R31	10.0K .50W 2%	629A531H56
R33	22.0K .50W 2%	629A531H64
R34	10.0K .50W 2%	629A531H56
R35	22.0K .50W 2%	629A531H64
R36	10.0K .50W 2%	629A531H56
R37	10.0K .50W 2%	629A531H56
R38	10.0K .50W 2%	629A531H56
R39	6.2K .50W 2%	629A531H51
R40	4.7K .50W 2%	629A531H48
R41	10.0K .50W 2%	629A531H56
R42	6.8K .50W 2%	629A531H52
R43	4.7K .50W 2%	629A531H48
R44	22.0K .50W 2%	629A531H64
R45	10.0K .50W 2%	629A531H56
R46	10.0K .50W 2%	629A531H56
R47	6.8K .50W 2%	629A531H52
R48	82.0K .50W 2%	629A531H78
R49	150.0 ohms 3.00W 5%	762A679H01
R51	10.0K .50W 2%	629A531H56
R52	10.0K .50W 2%	629A531H56
	Transistor	
Q1	2N3417	848A851H02
Q2	2N3417	848A851H02
Q3	2N3417	848A851H02
Q4	2N3645	848A441H01
Q5	2N3417	848A851H02
Q6	2N3417	848A851H02
Q7	2N3645	849A441H01
Q8	2N3417	848A851H02
Q9	2N3417	848A851H02
Q10	2N3645	848A441H01
Q11	2N3645	849A441H01
Q12	2N3645	848A441H01
Q13	2N3417	848A851H02
Q14	2N3645	848A441H01
Q15	2N699	184A638H19

CIRCUIT SYMBOL	DESCRIPTION	WESTINGHOUSE STYLE NUMBER
	Zener	
Z1	IN3686B 0.0V	185A212H06
Z2	IN857B6.8V	186A797H06
Z3	IN3688A 24.0V	862A288H01
Z4	IN960B 9.1V	186A797H10
Z5	IN957B 6.8V	186A797H06
Z6	IN957B 6.8V	186A797H06
Z7	IN957B 6.8V	186A797H06
Z8	IN3688A 24.0V	862A288H01
Z9	IN1789 56.0V	584C434H08
Z10	IN960B 9.1V	186A797H10

PROTECTIVE RELAY BOARD STYLE 202C563G01

	Capacitors	
C1	0.047 MFD.	848A437H04
C2	0.47 MFD.	188A669H01
C3	68 MFD.	187A508H02
C4	0.27 MFD.	188A669H05
C5	0.047 MFD.	849A437H04
C6	0.27 MFD.	188A669H05
C7	0.047 MFD.	848A437H04
C8	6.8 MFD.	184A661H10
	Diodes	
D1	IN645A	837A692H03
D2	IN645A	837A692H03
D3	IN645A	837A692H03
D4	IN645A	837A692H03
D5	IN645A	836A692H03
D6	IN645A	837A692H03
D7	IN645A	837A692H03
D8	IN645A	837A692H03
	Resistors	
R1	4.7 K .5W 2%	629A531H48
R2	4.7 K .5W 2%	629A531H48
R3	4.7 K .5W 2%	629A531H48
R4	4.7 K .5W 2%	629A531H48
R5	4.7 K .5W 2%	629A531H48
R6	82 K .5W 2%	629A531H78
R7	10 K .5W 2%	629A531H56
R8	6.8 K .5W 2%	629A531H52
R9	10 K .5W 2%	629A531H56
R10	10 K .5W 2%	629A531H56
R11	27 K .5W 2%	629A531H66
R12	27 K .5W 2%	629A531H24

CIRCUIT SYMBOL	DESCRIPTION	WESTINGHOUSE STYLE NUMBER
R13	10 K .5W 2%	629A531H56
R14	10 K .5W 2%	629A531H56
R15	6.8 K .5W 2%	629A531H52
R16	82 K .5W 2%	629A531H78
R18	470 ohms .5W 2%	629A531H24
R19	47 K .5W 2%	629A531H72
R20	10 K .5W 2%	629A531H56
R21	10 K .5W 2%	629A531H56
R22	27 K .5W 2%	629A531H66
R24	10 K .5W 2%	629A531H56
R24	10 K .5W 2%	629A531H56
R25	6.8 K .5W 2%	629A531H52
R26	82 K .5W 2%	629A531H78
R27	4.7 K .5W 2%	629A531H48
R28	4.7 K .5W 2%	629A531H48
R29	22 K .5W 2%	629A531H64
R30	4.7 K .5W 2%	629A531H48
R31	82 K .5W 2%	629A531H78
R32	10 K .5W 2%	629A531H56
R33	10 K .5W 2%	629A531H56
R34	6.8 K .5W 2%	629A521H52
R35	82 K .5W 2%	629A531H78
R36	4.7 K .5W 2%	629A531H48
R37	4.7 K .5W 2%	629A531H48
R38	82 K .5W 2%	629A531H78
R39	10 K .5W 2%	629A531H56
R40	6.8 K .5W 2%	629A531H52
R41	10 K .5W 2%	629A531H56
R42	33 K .5W 2%	629A531H68
R43	10 K .5W 2%	629A531H56
R44	6.8 K .5W 2%	629A531H52
R45	27 K .5W 2%	629A531H66
R46	10 K .5W 2%	629A531H56
	Transistors	
Q1	2N3417	848A851H02
Q2	2N3417	848A851H02
Q3	2N3417	848A851H02
Q4	2N3645	848A441H01
Q5	2N3417	848A851H02
Q6	2N3417	848A851H02
Q7	2N3645	848A441H01
Q8	2N3417	848A851H02
Q9	2N3645	849A441H01
Q10	2N3417	848A851H02
Q11	2N3417	848A851H02
Q12	2N3417	848A851H02

CIRCUIT SYMBOL	DESCRIPTION	WESTINGHOUSE STYLE NUMBER
	Zener Diodes	
Z1	IN3686B, 20 V.	185A212H06
Z2	IN3686B, 20 V.	185A212H06
Z3	IN3686B, 20 V.	185A212H06
Z4	IN3686B, 20 V.	185A212H06
Z5	IN3686B, 20 V.	185A212H06
Z6	IN957B, 6.8 V.	186A797H06
Z7	IN957B, 6.8 V.	186A797H06
Z8	IN957B, 6.8 V.	186A797H06
Z9	IN3688A, 24 V.	862A288H01
Z10	IN3686B, 20 V.	185A212H06
Z11	IN3686B, 20 V.	185A212H06
Z12	IN3686B, 20 V.	185A212H06
Z13	IN3686B, 20 V.	185A212H06
Z14	IN957B, 6.8 V.	186A797H06
Z15	IN3688A, 24 V.	862A288H01
Z16	IN3686B, 20 V.	185A212H06
Z17	IN957B, 6.8 V.	186A797H06
Z18	IN957B, 6.8 V.	186A797H06

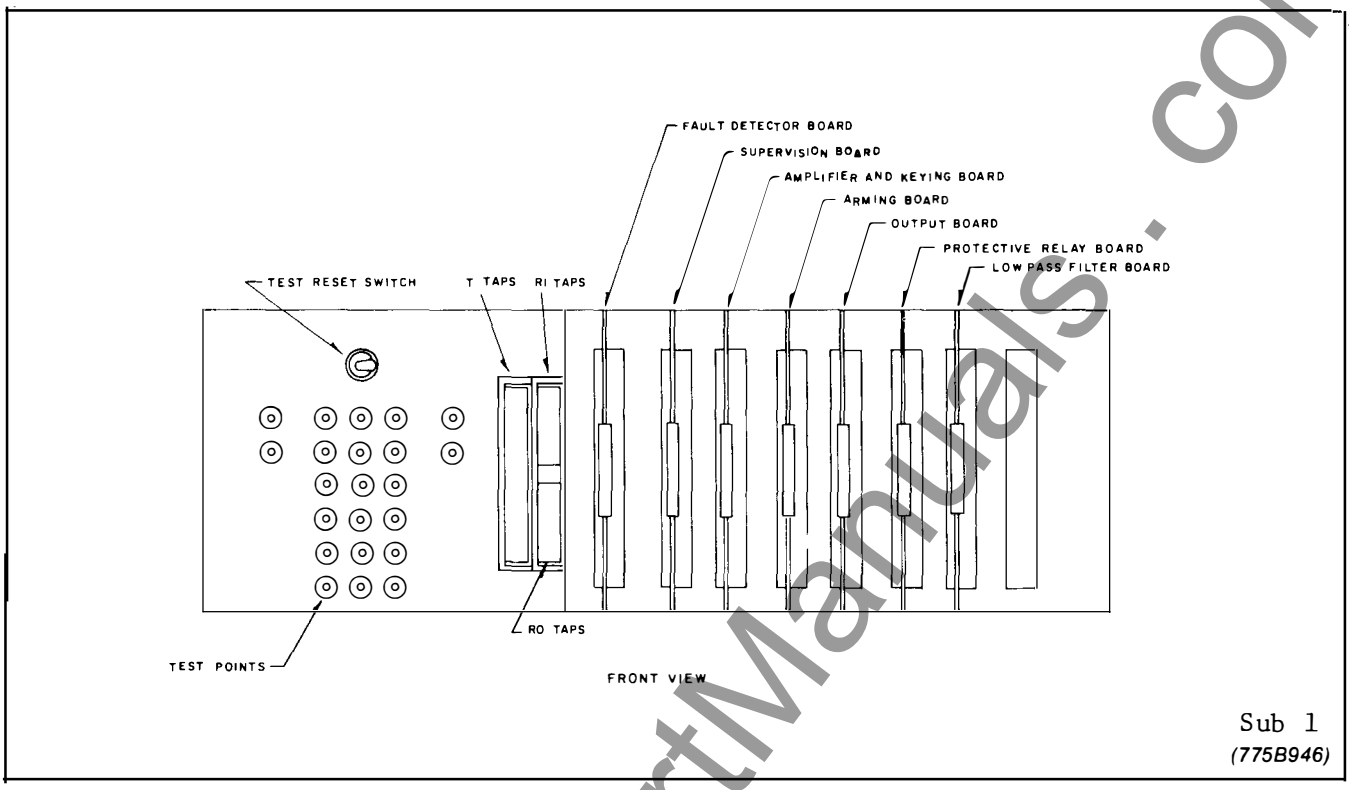


Fig. 1. Front View of the SKBU-2A Relay

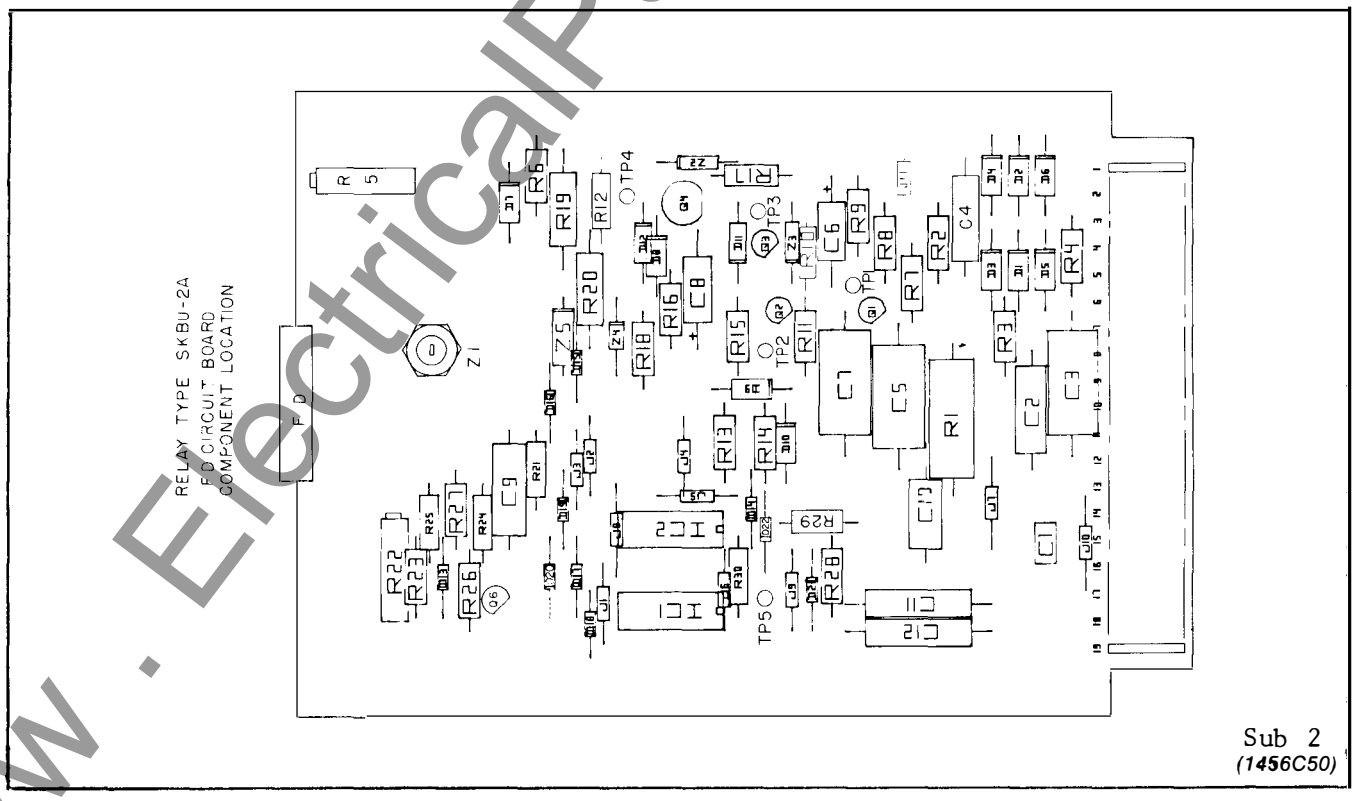


Fig. 2. Location of Components on Fault Detector Board

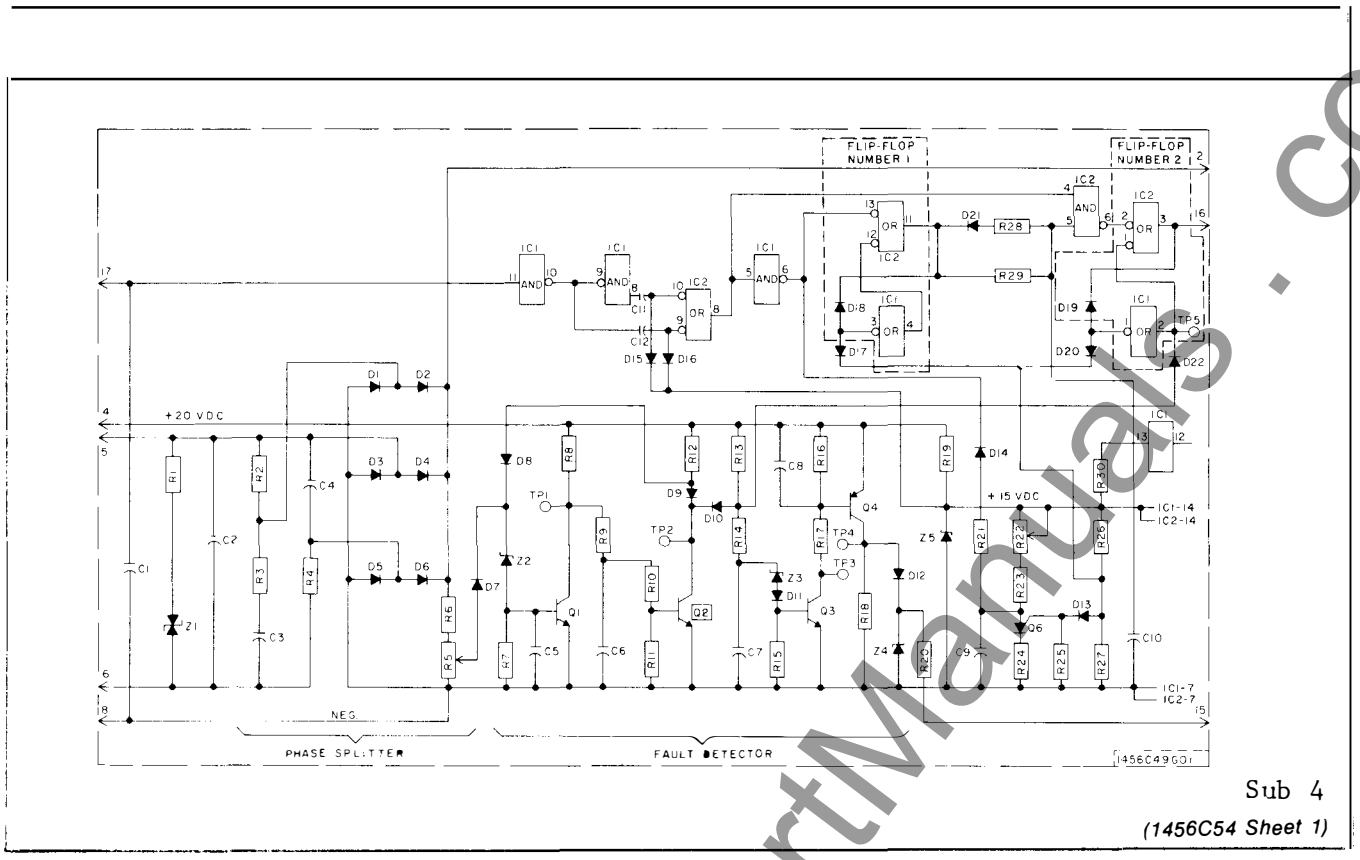


Fig. 3. Schematic of Fault Detector Board

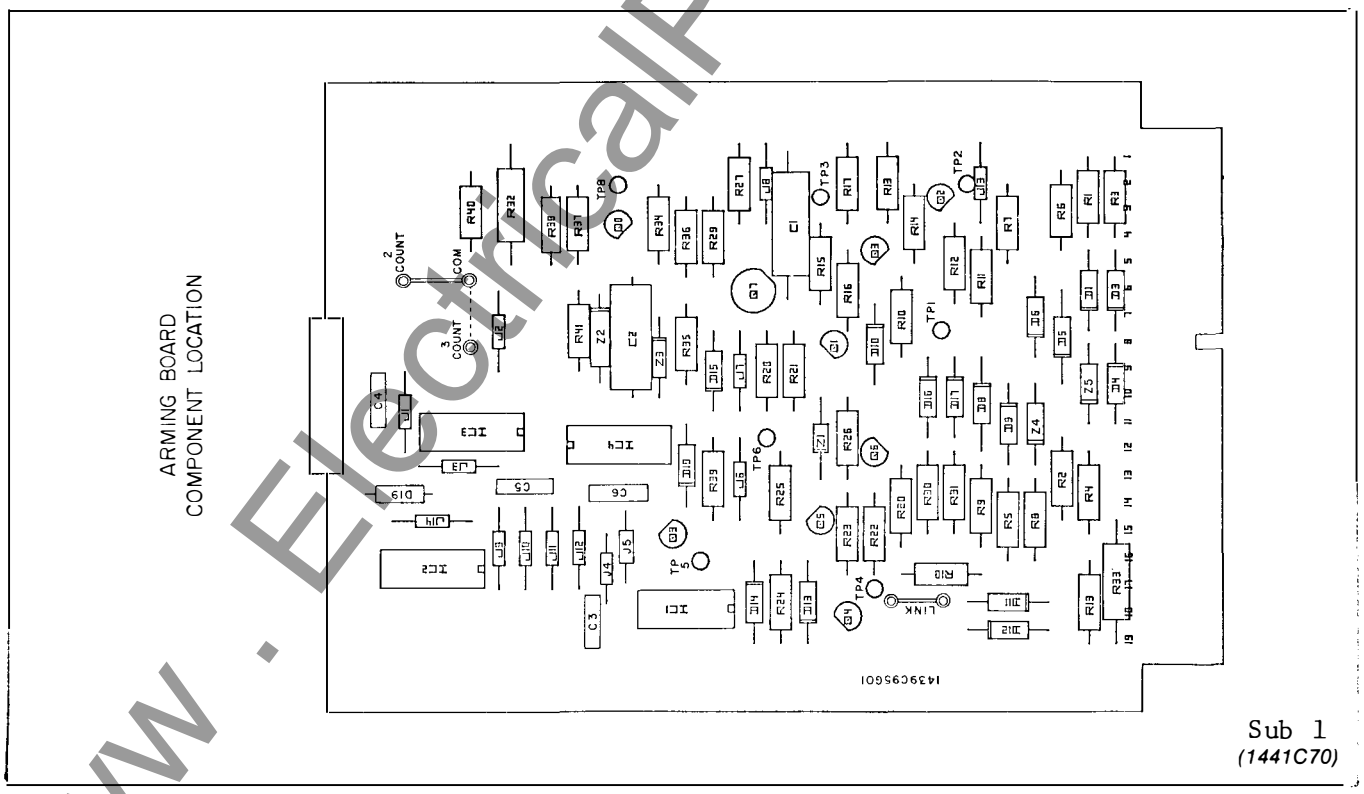
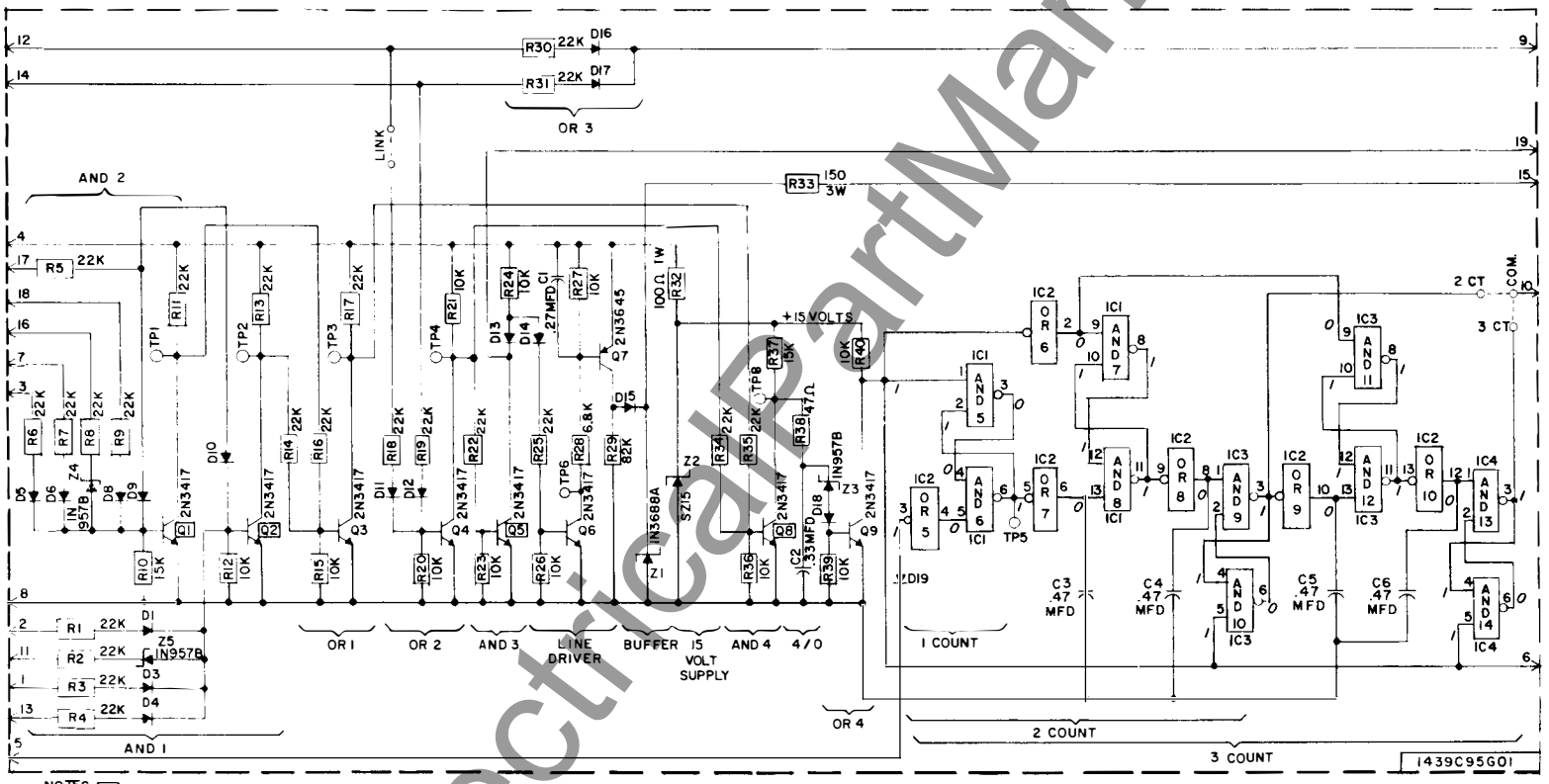


Fig. 4. Location of Components on Arming Board



NOTES [Q1] = NORMALLY CONDUCTING TRANSISTORS

ALL DIODES IN645A

ONE RESISTOR (R41 NOT SHOWN) CONNECTED TO 4 UNUSED INPUTS ON IC4-9,-10,-12,8-13. WITH OTHER END OF RESISTOR CONNECTED TO +15 VOLTS.

LOGIC STATES SHOWN FOR CONDITIONS OF NO A.C CURRENT APPLIED TO SEQUENCE NETWORK.

Sub 3
(1440C26 Sheet 1)

Fig. 5. Schematic of Arming Board

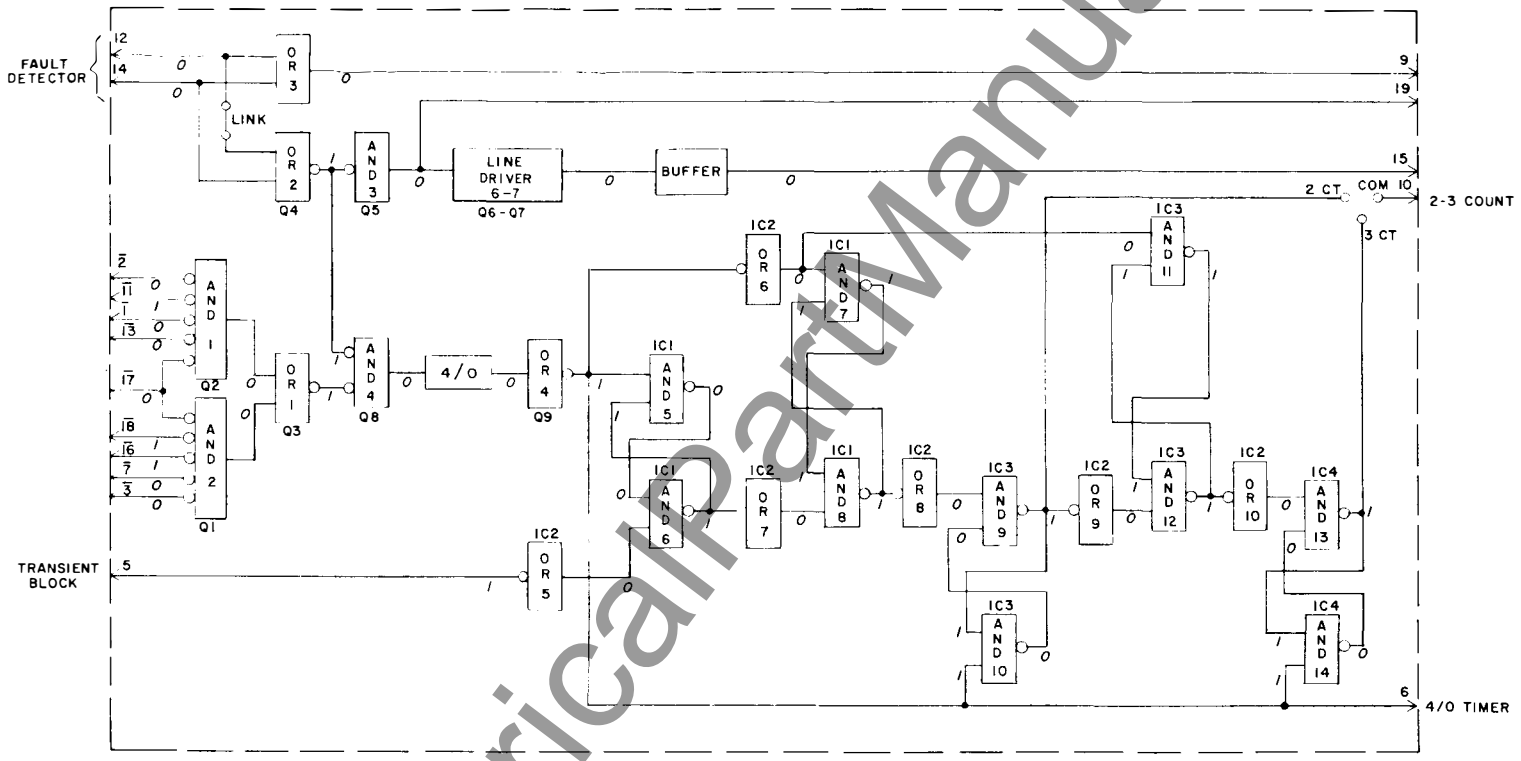
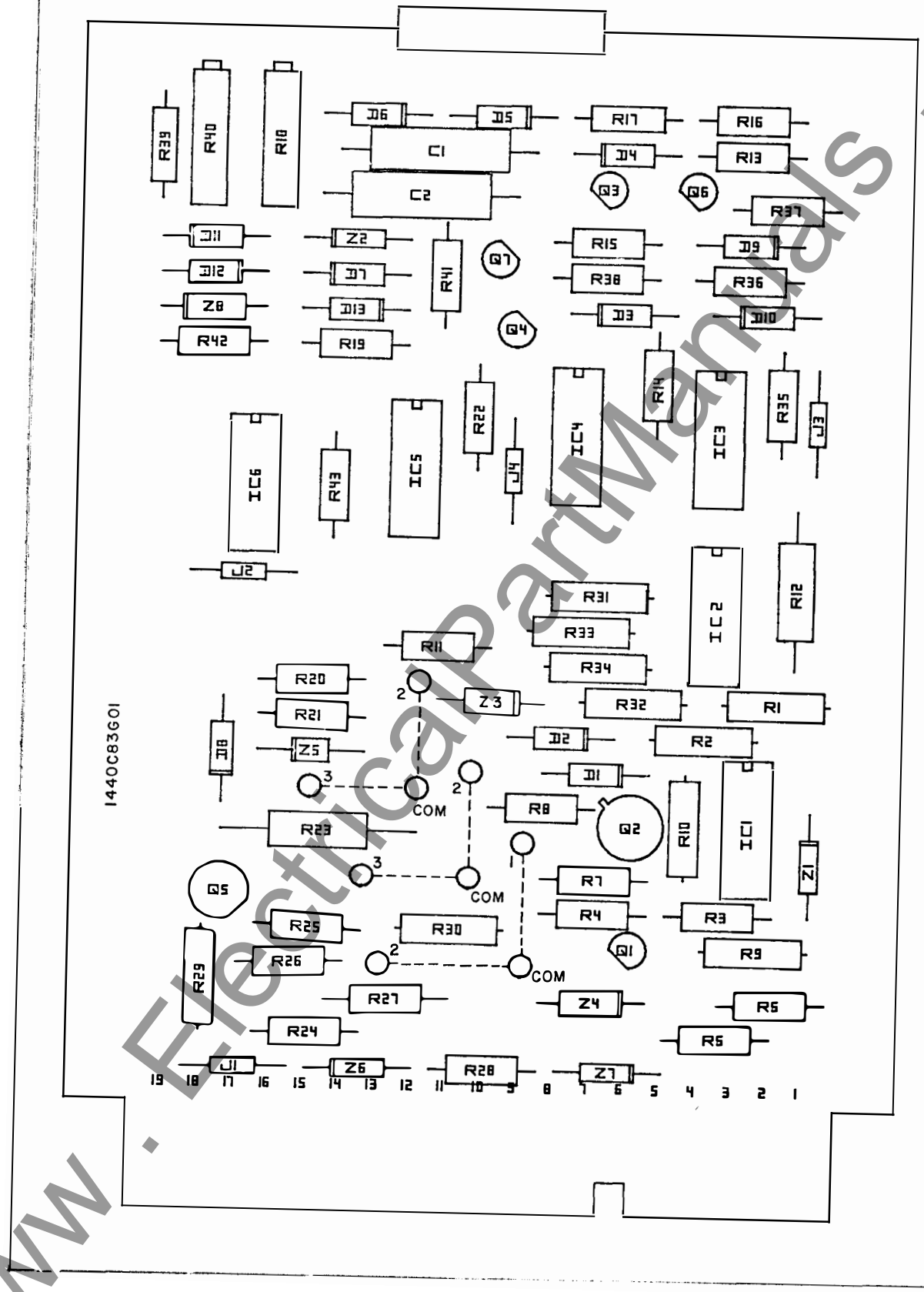
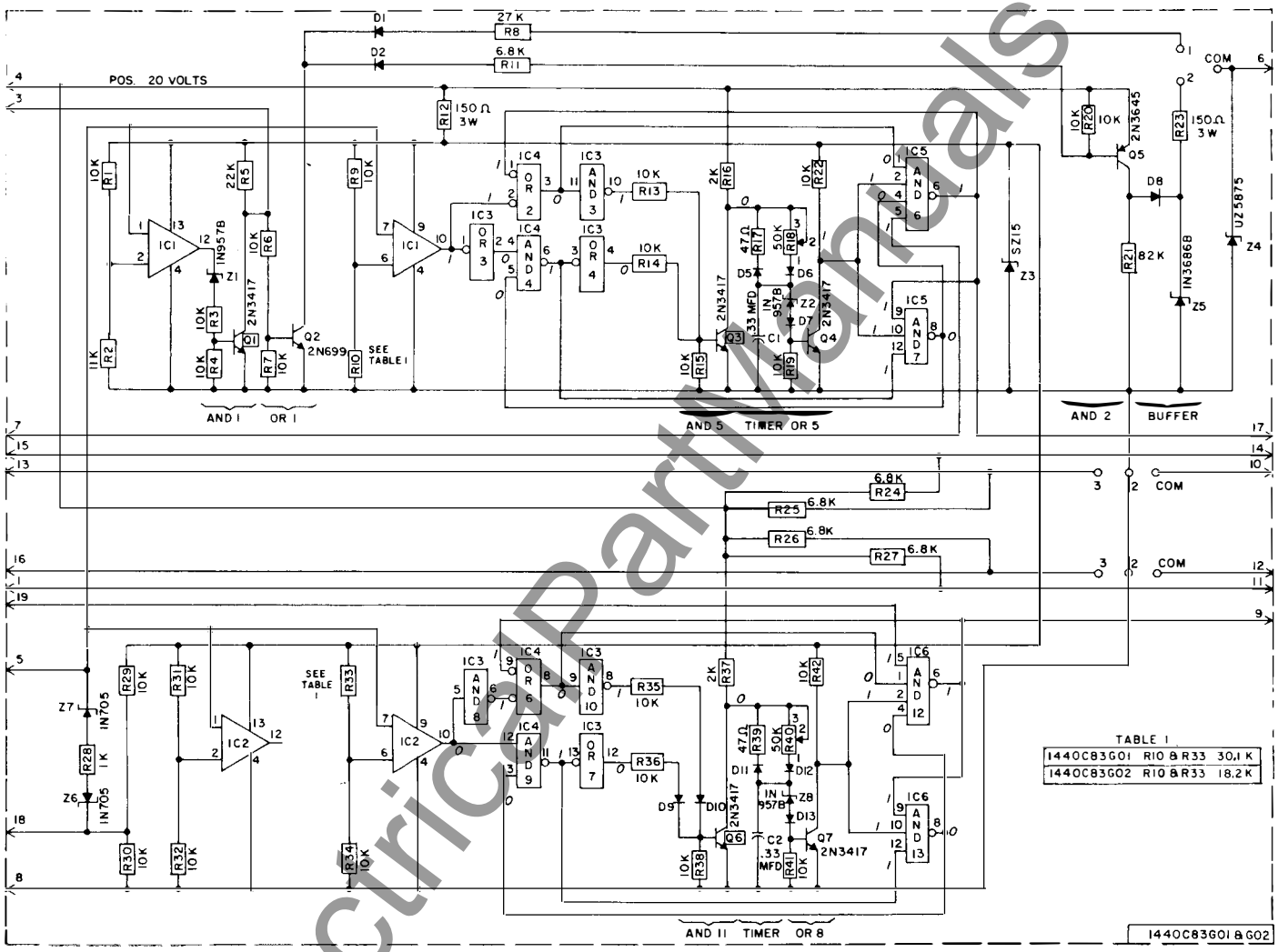


Fig. 6. Logic Drawing of Arming Board



Sub 1
(1441C71)

Fig. 7. Location of Components on Amplifier and Keying Board



NOTES: ALL DIODES IN645A.

Q1 = NORMALLY CONDUCTING TRANSISTORS.

ONE RESISTOR (R43 NOT SHOWN) CONNECTOR TO UNUSED TERMINALS IC5-13 & IC6-13, OTHER END OF RESISTOR CONNECTED TO + 15 VOLTS.

LOGIC STATES SHOWN WITH NO A.C. VOLTAGE APPLIED TO TERMINAL 5 AND 18.

Sub 7
(1441C19 Sheet 1)

Fig. 8. Schematic of Amplifier and Keying Board

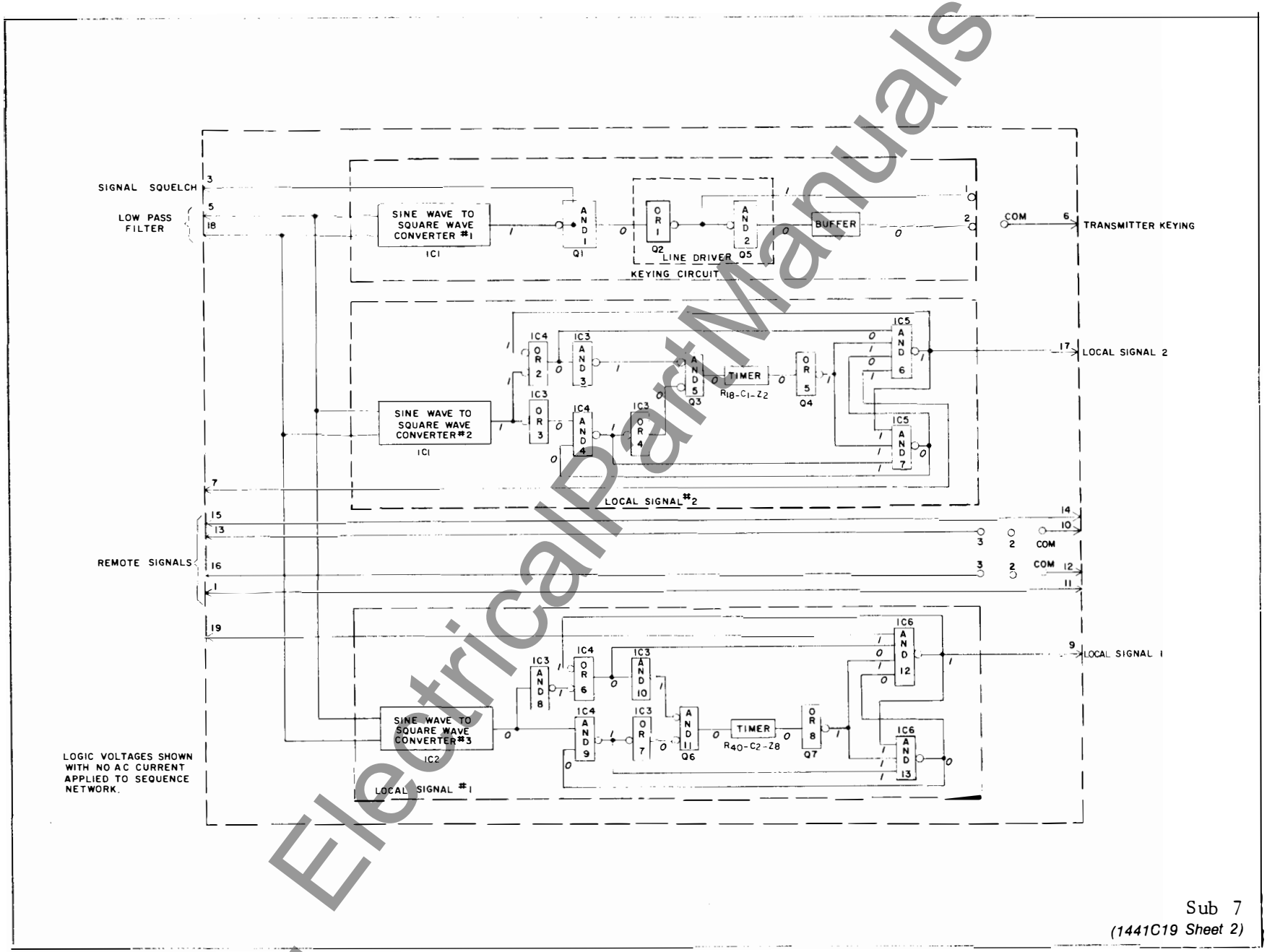


Fig. 9. Logic Drawing of Amplifier and Keying Board

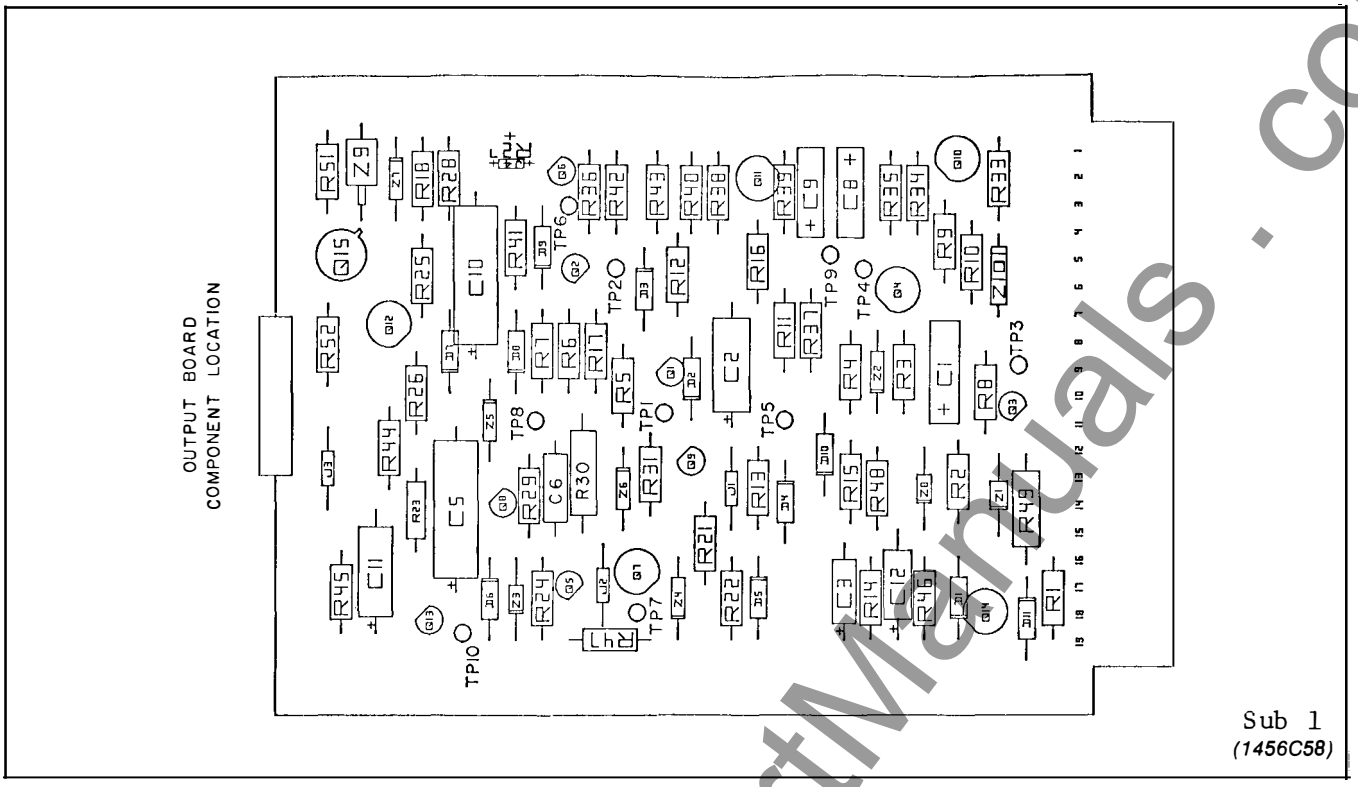


Fig. 10. Location of Components on Output Board

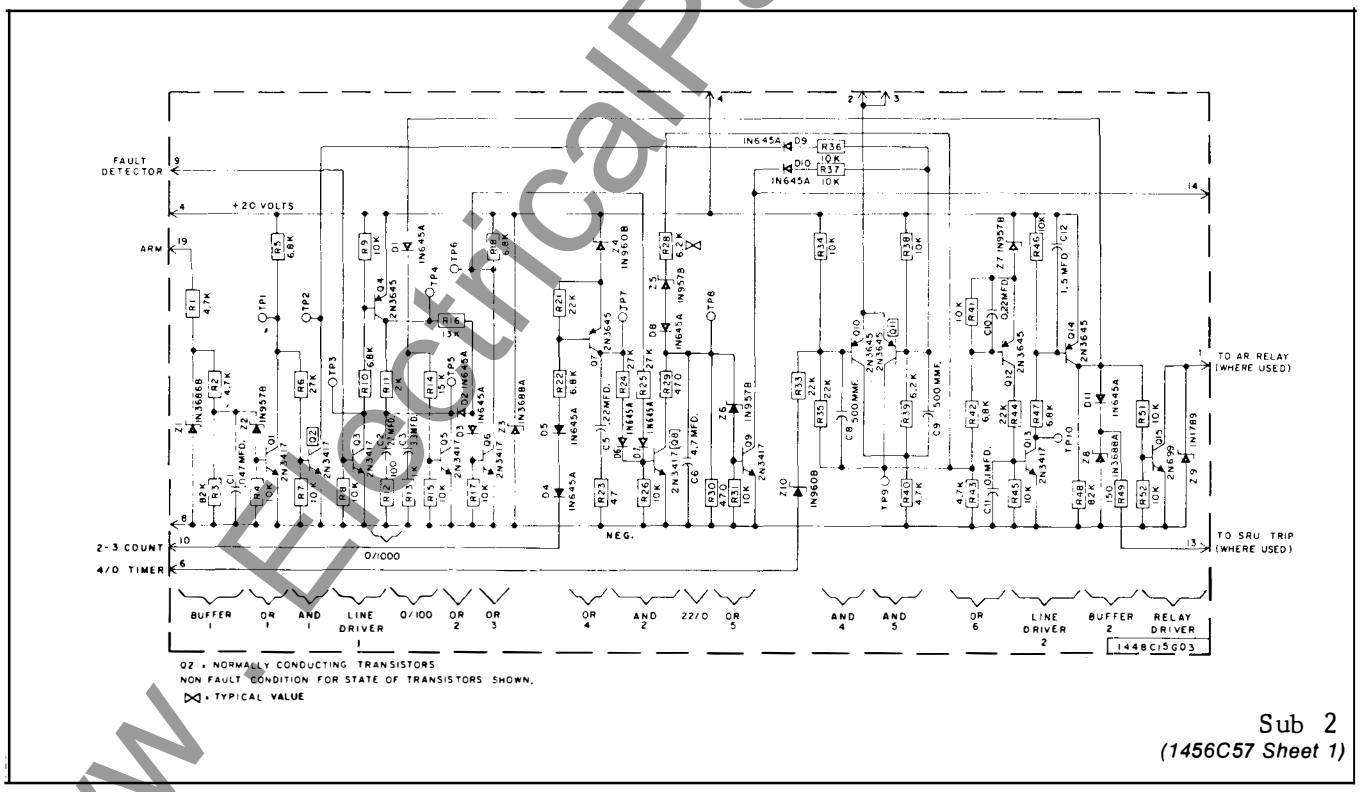


Fig. 11. Schematic of Output Board

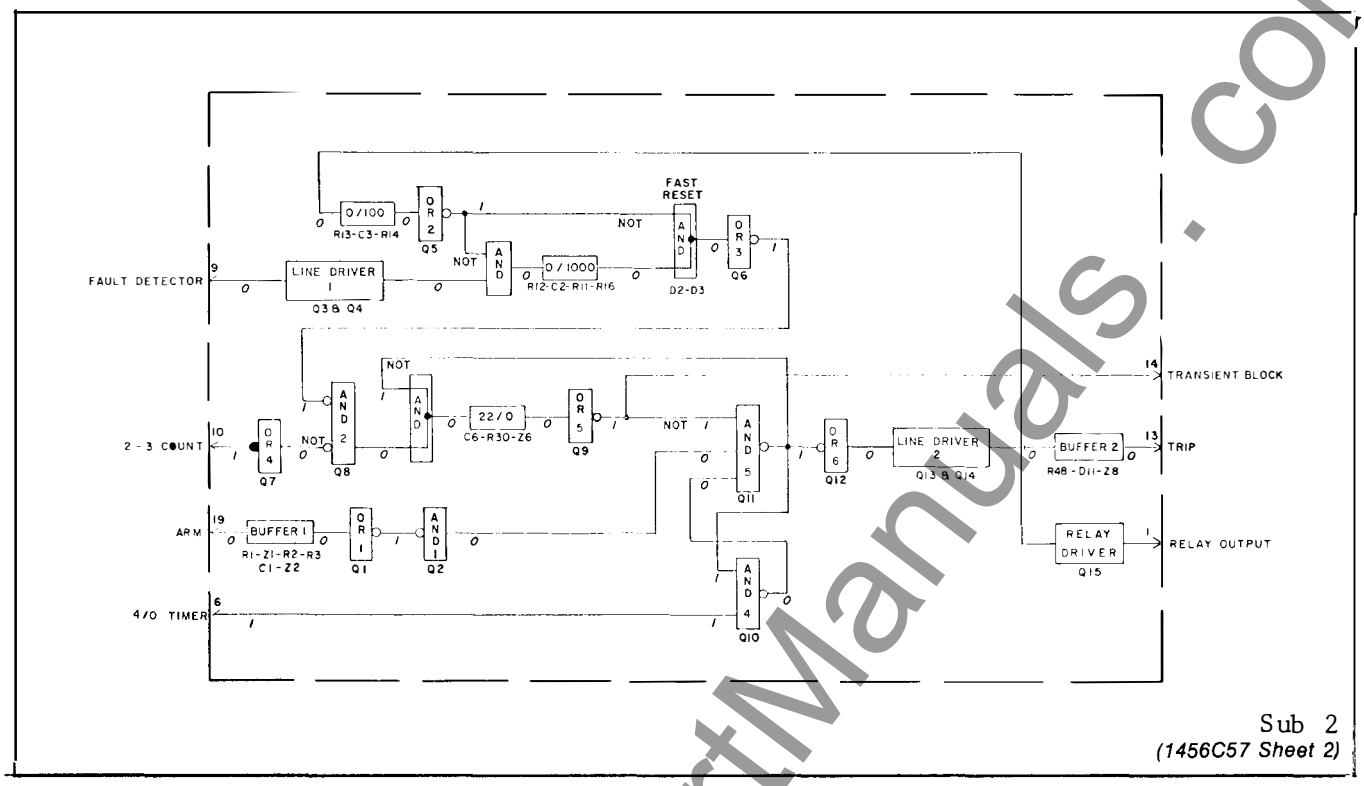


Fig. 12. Logic Drawing of Output Board

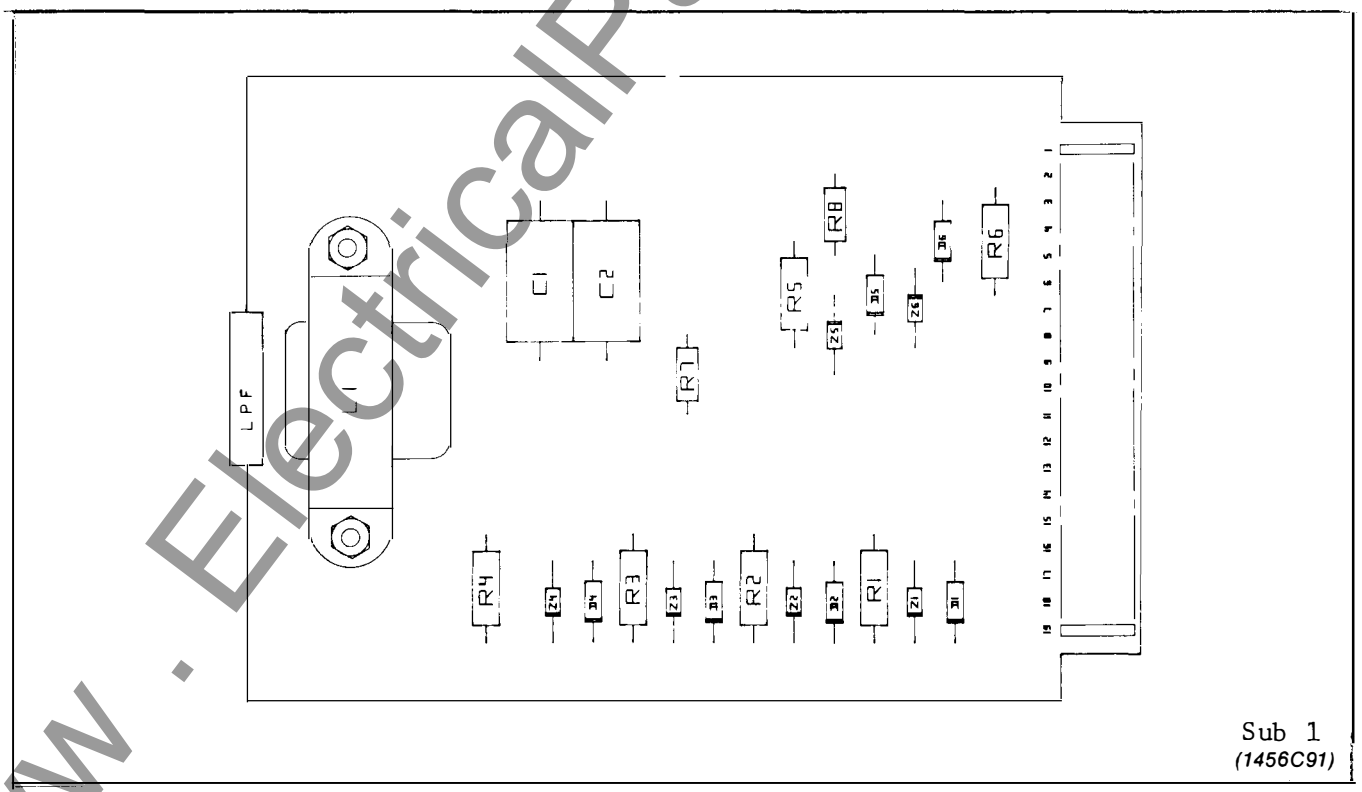
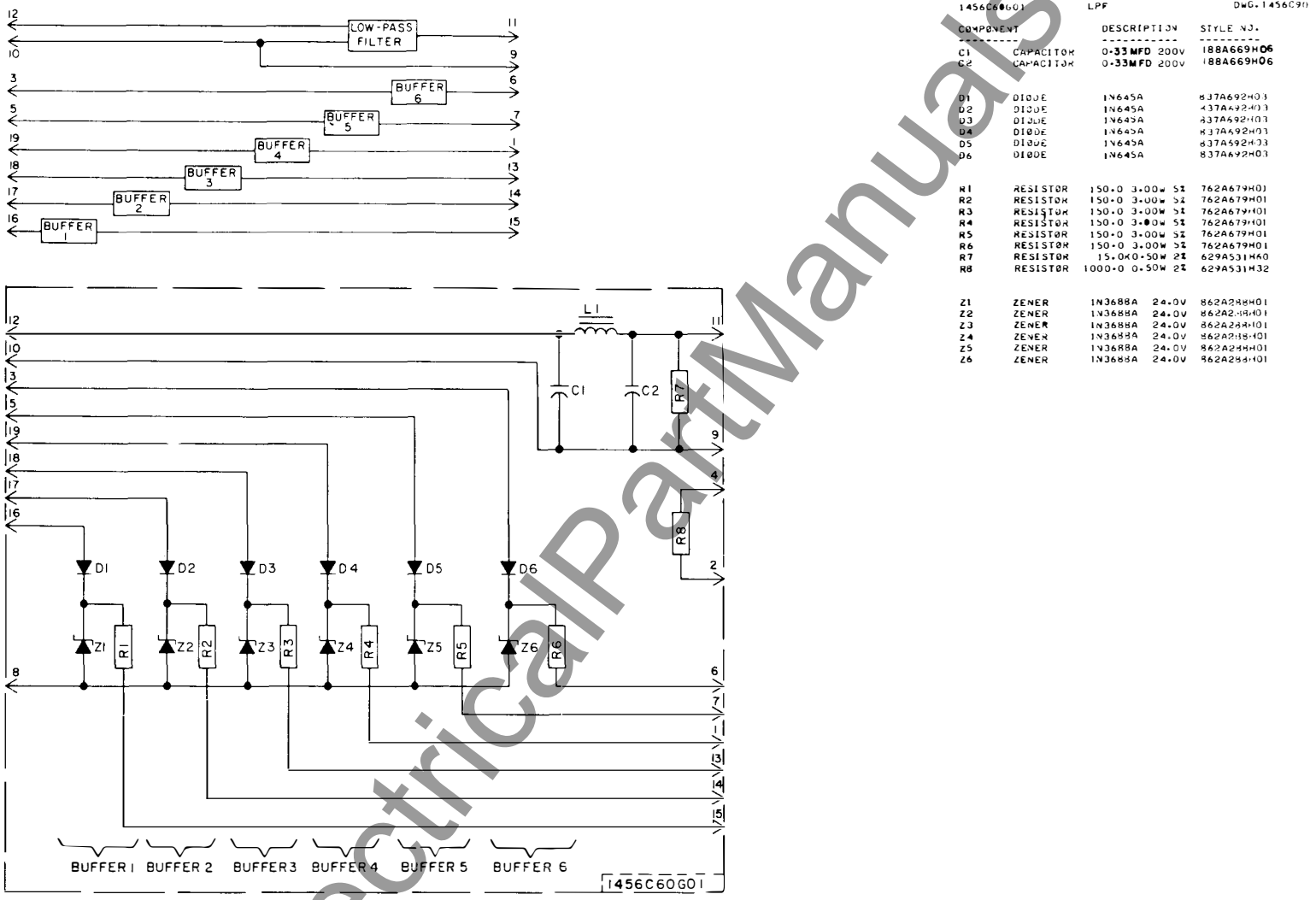


Fig. 13. Location of Components on Low Pass Filter Board



1456C60G01 LPF DWG. 1456C90

COMPONENT		DESCRIPTION	STYLE NO.
C1	CAPACITOR	0.33 MFD 200V	188A669H06
C2	CAPACITOR	0.33 MFD 200V	188A669H06
D1	DIODE	1N645A	837A692H03
D2	DIODE	1N645A	837A692H03
D3	DIODE	1N645A	837A692H03
D4	DIODE	1N645A	837A692H03
D5	DIODE	1N645A	837A692H03
D6	DIODE	1N645A	837A692H03
R1	RESISTOR	150.0 3.00W 5%	762A679H01
R2	RESISTOR	150.0 3.00W 5%	762A679H01
R3	RESISTOR	150.0 3.00W 5%	762A679H01
R4	RESISTOR	150.0 3.00W 5%	762A679H01
R5	RESISTOR	150.0 3.00W 5%	762A679H01
R6	RESISTOR	150.0 3.00W 5%	762A679H01
R7	RESISTOR	15.0K 0.50W 2%	629A531H40
R8	RESISTOR	1000.0 0.50W 2%	629A531H32
Z1	ZENER	1N3688A 24.0V	862A288H01
Z2	ZENER	1N3688A 24.0V	862A288H01
Z3	ZENER	1N3688A 24.0V	862A288H01
Z4	ZENER	1N3688A 24.0V	862A288H01
Z5	ZENER	1N3688A 24.0V	862A288H01
Z6	ZENER	1N3688A 24.0V	862A288H01

Sub 3
(1456C90)

Fig. 14. Schematic and Logic Drawing of Low Pass Filter Board

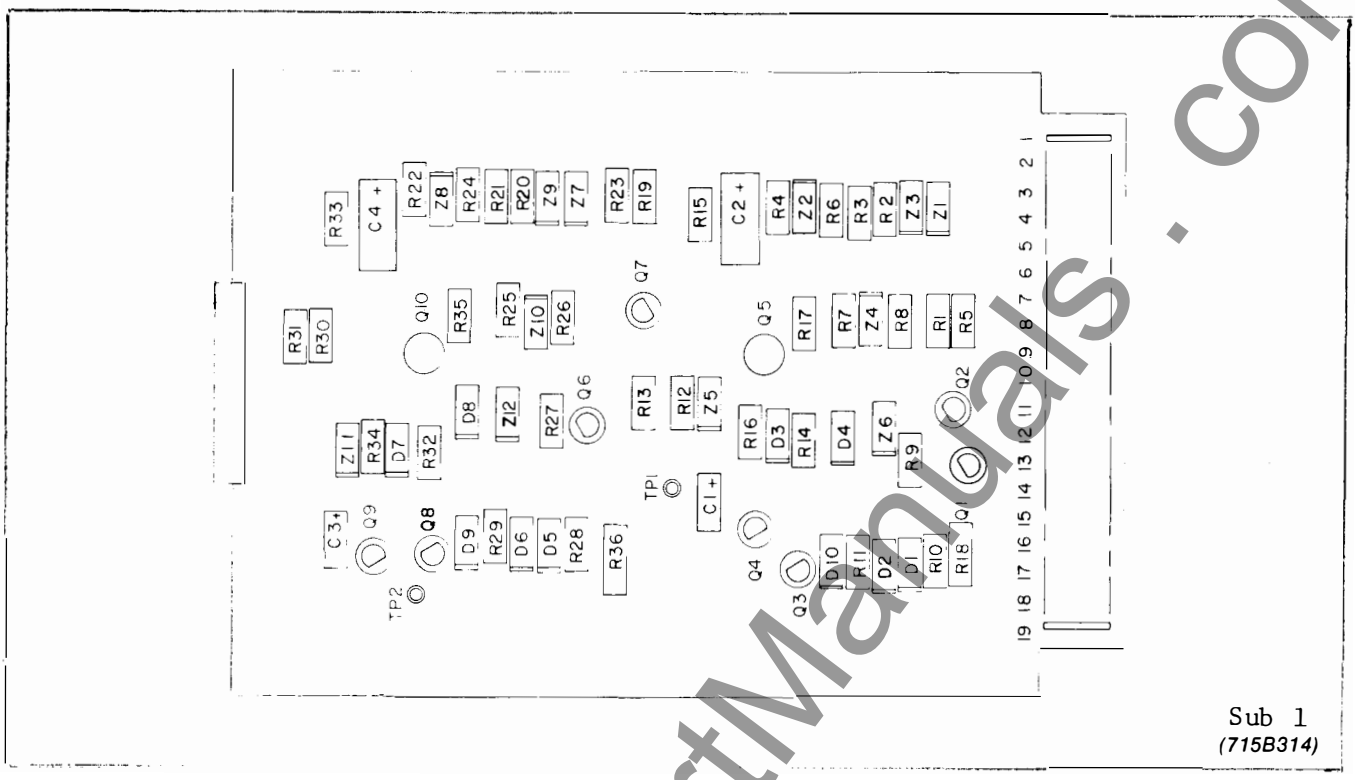


Fig. 15. Location of Components on Supervision Board

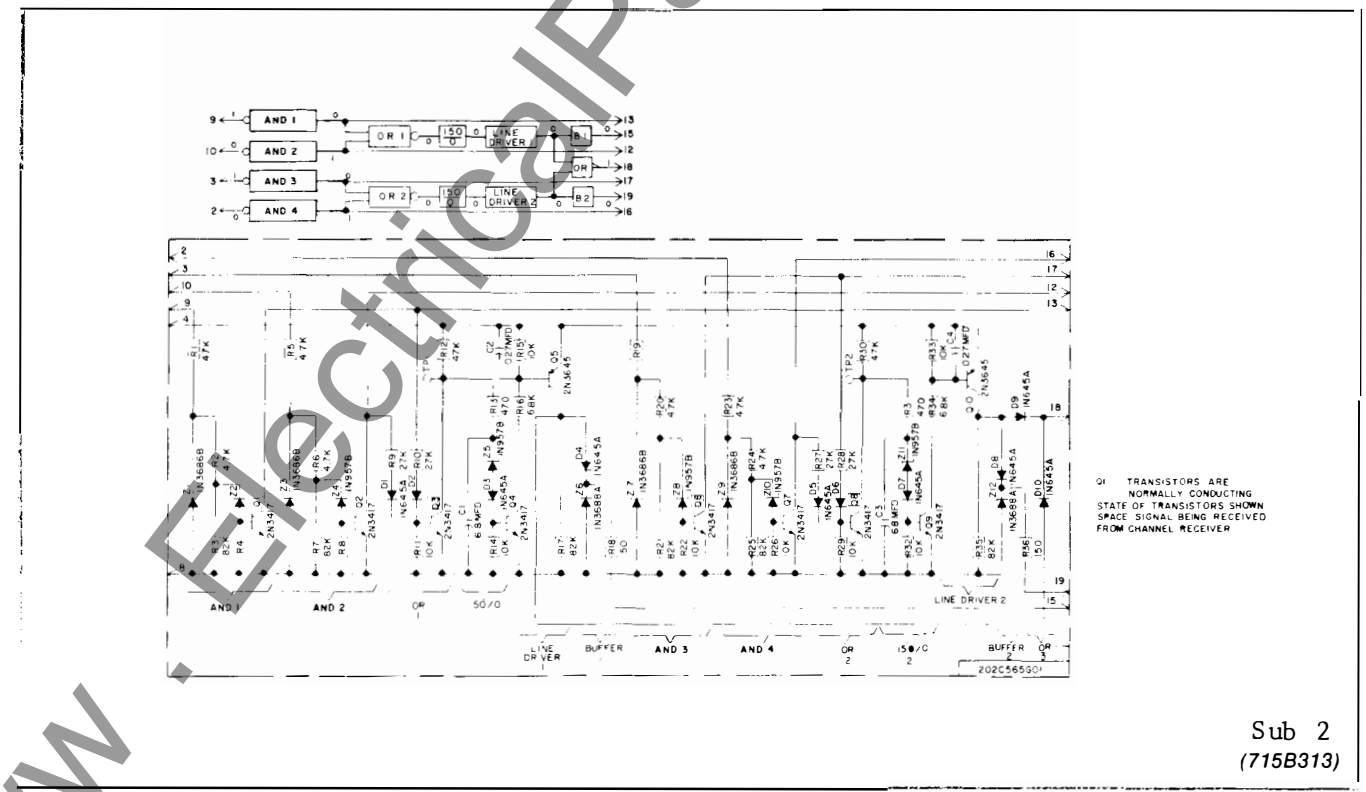


Fig. 16. Schematic and Logic Drawing of Supervision Board

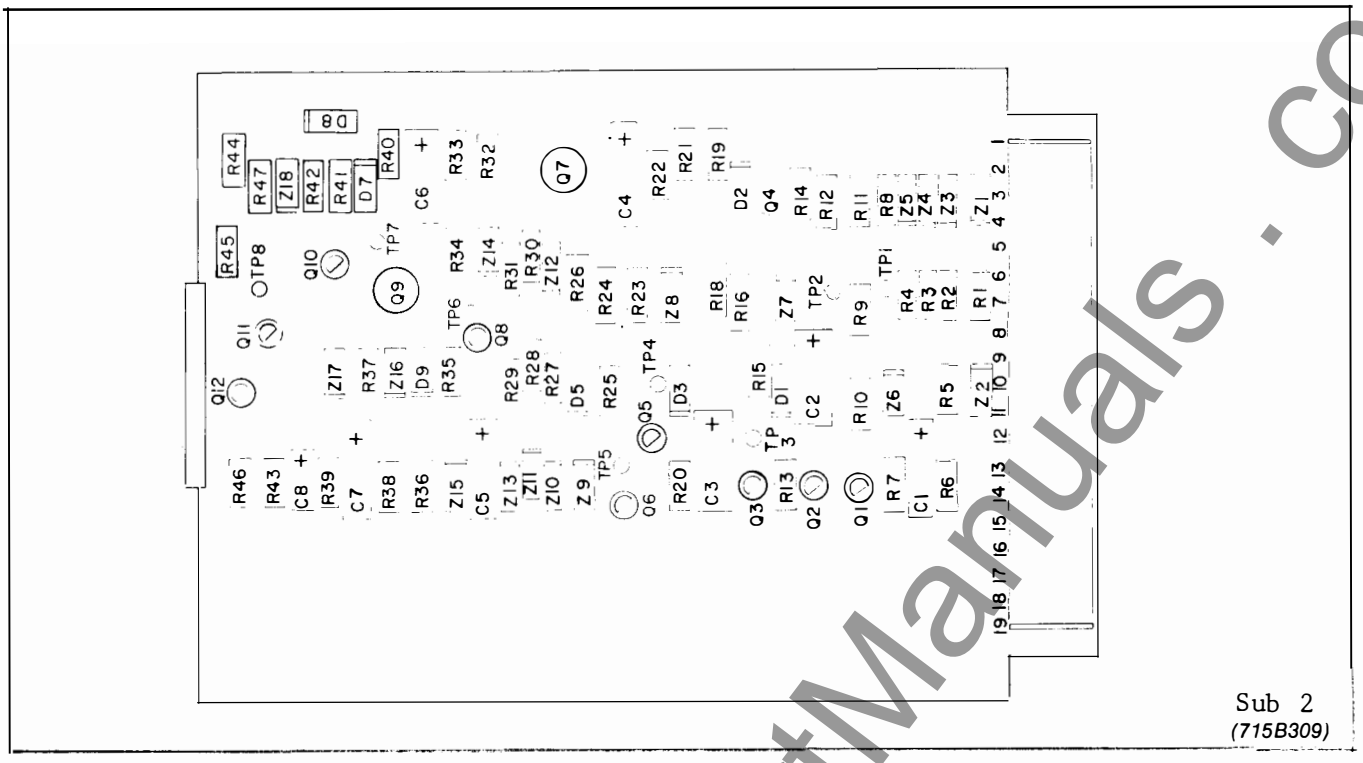


Fig. 17. Location of Components on Protective Relay Board

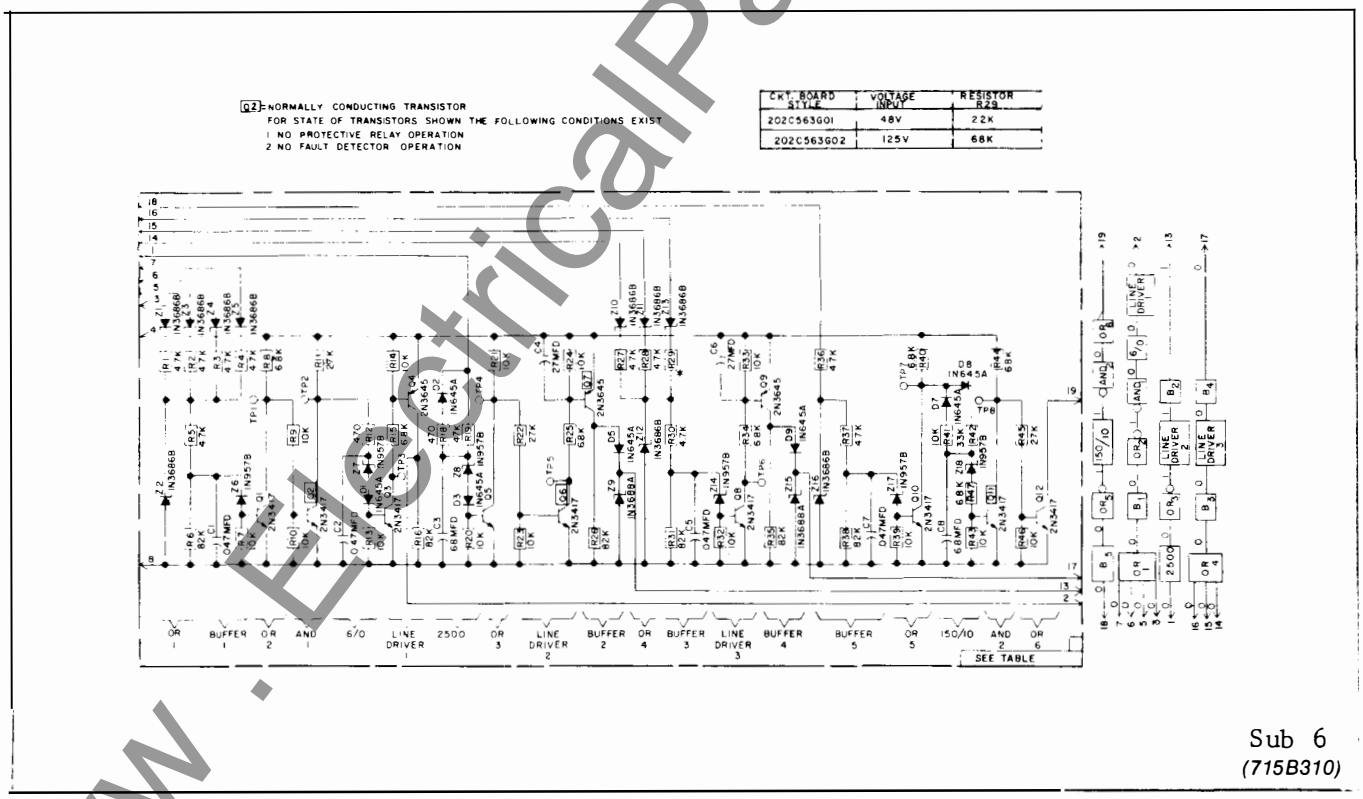
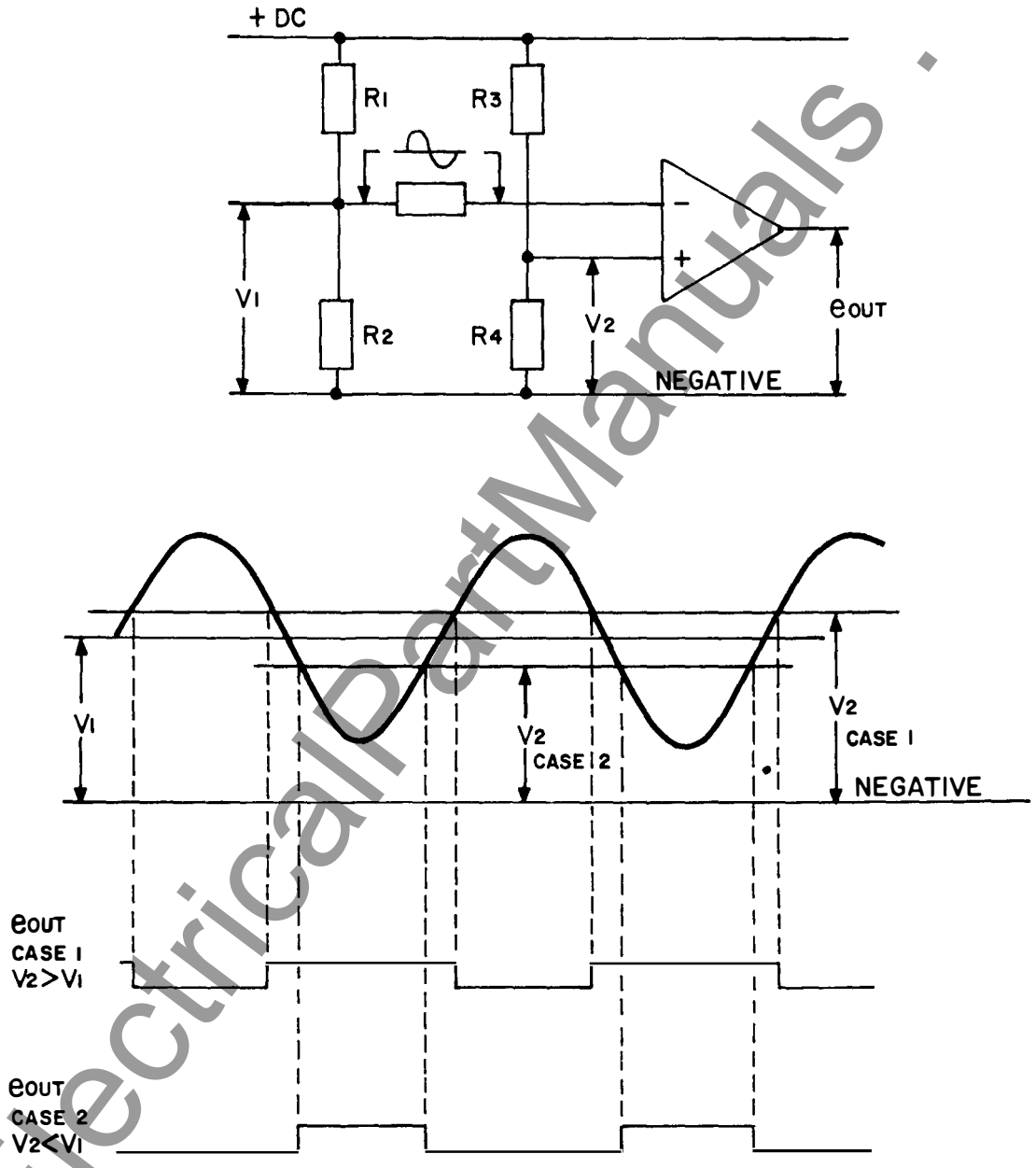
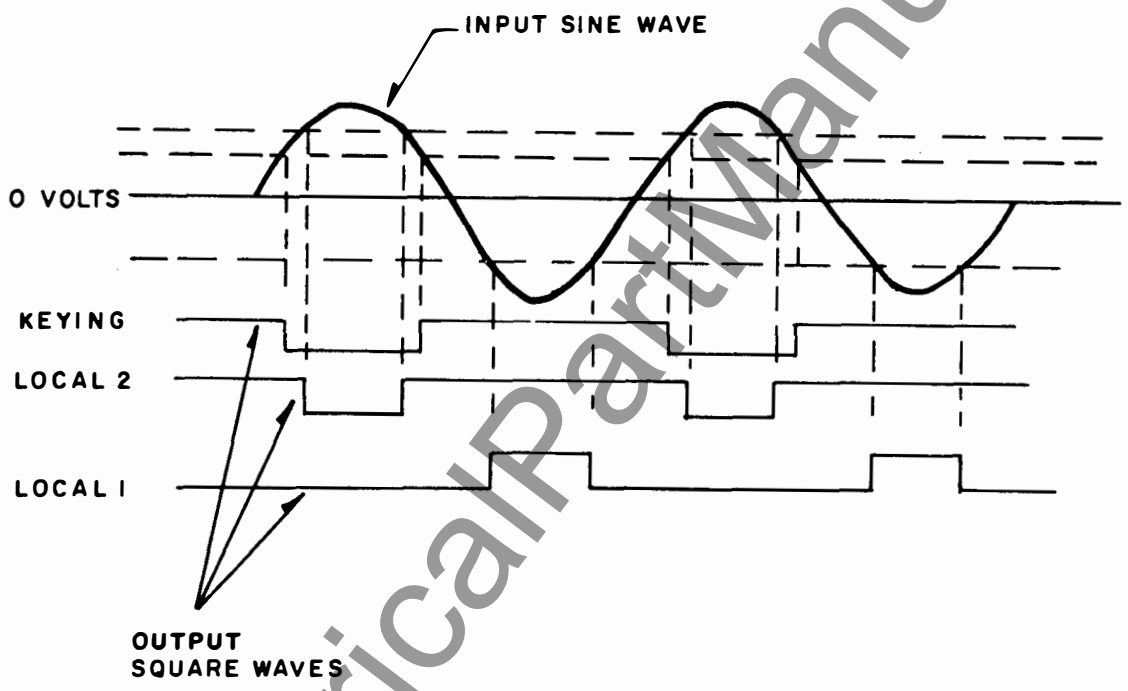


Fig. 18. Schematic and Logic Drawing of Protective Relay Board



Sub 1
(3510A6

Fig. 20. Sine Wave to Square Wave Convertor



Sub 1
(3520A52)

Fig. 21. Polarity Relationship of Sine Wave to Square Wave Convertor

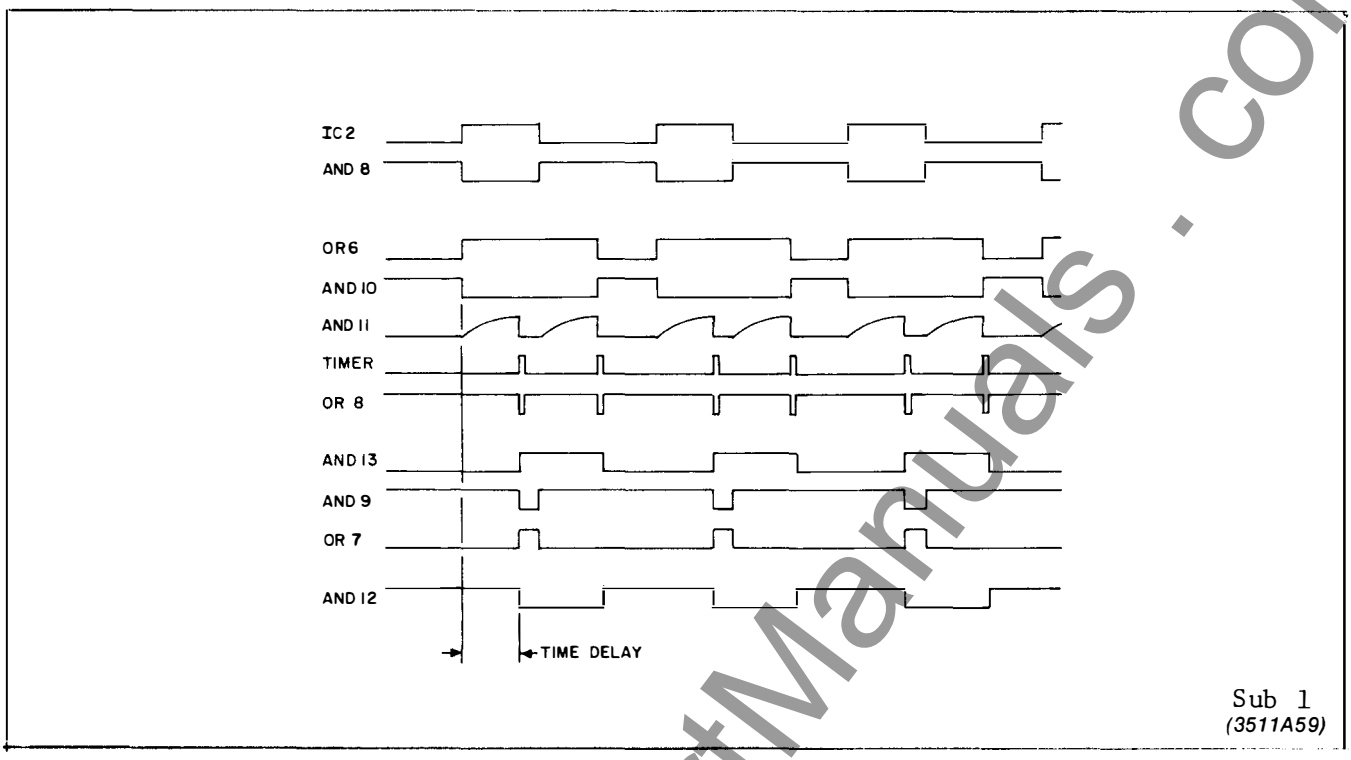


Fig. 22. Timing Waves of Phase Delay Circuit Number 1 of Amplifier and Keying Board

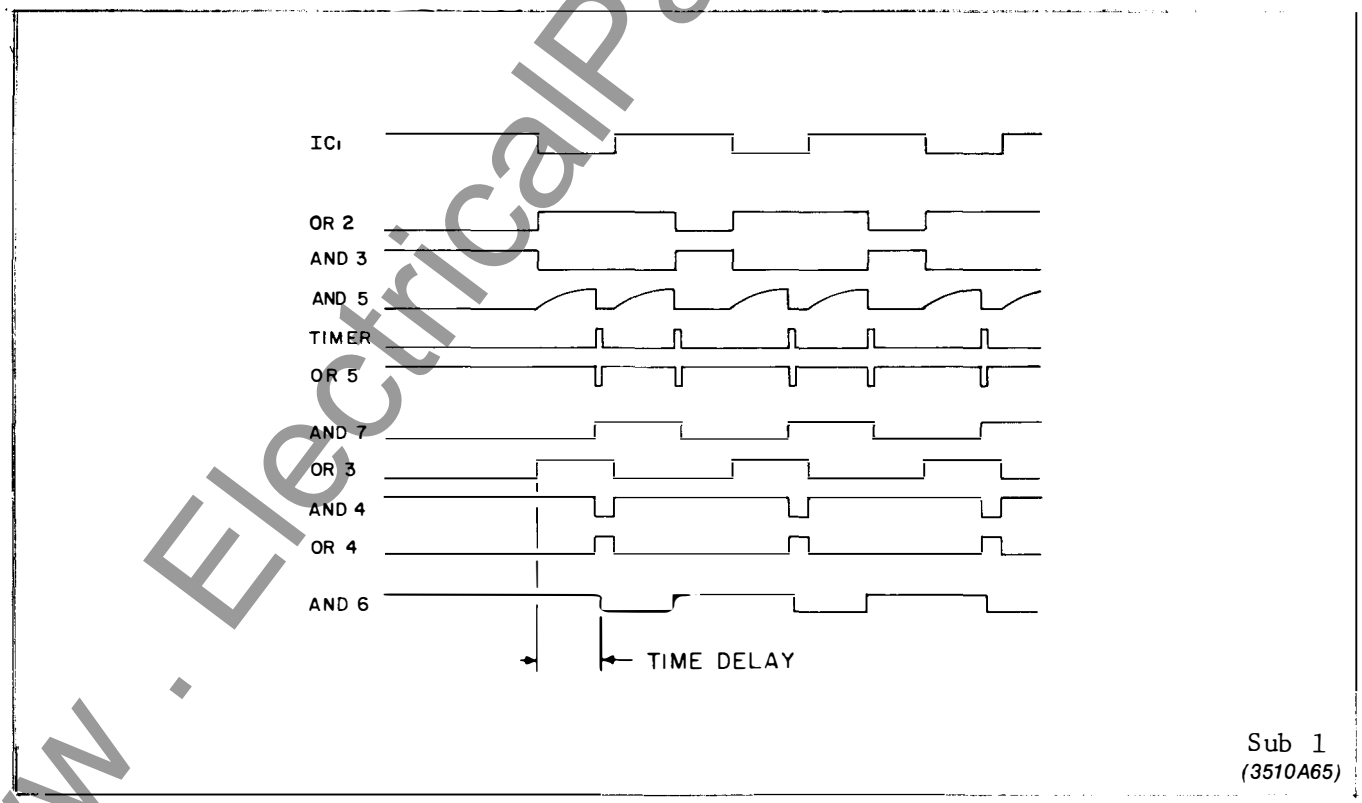
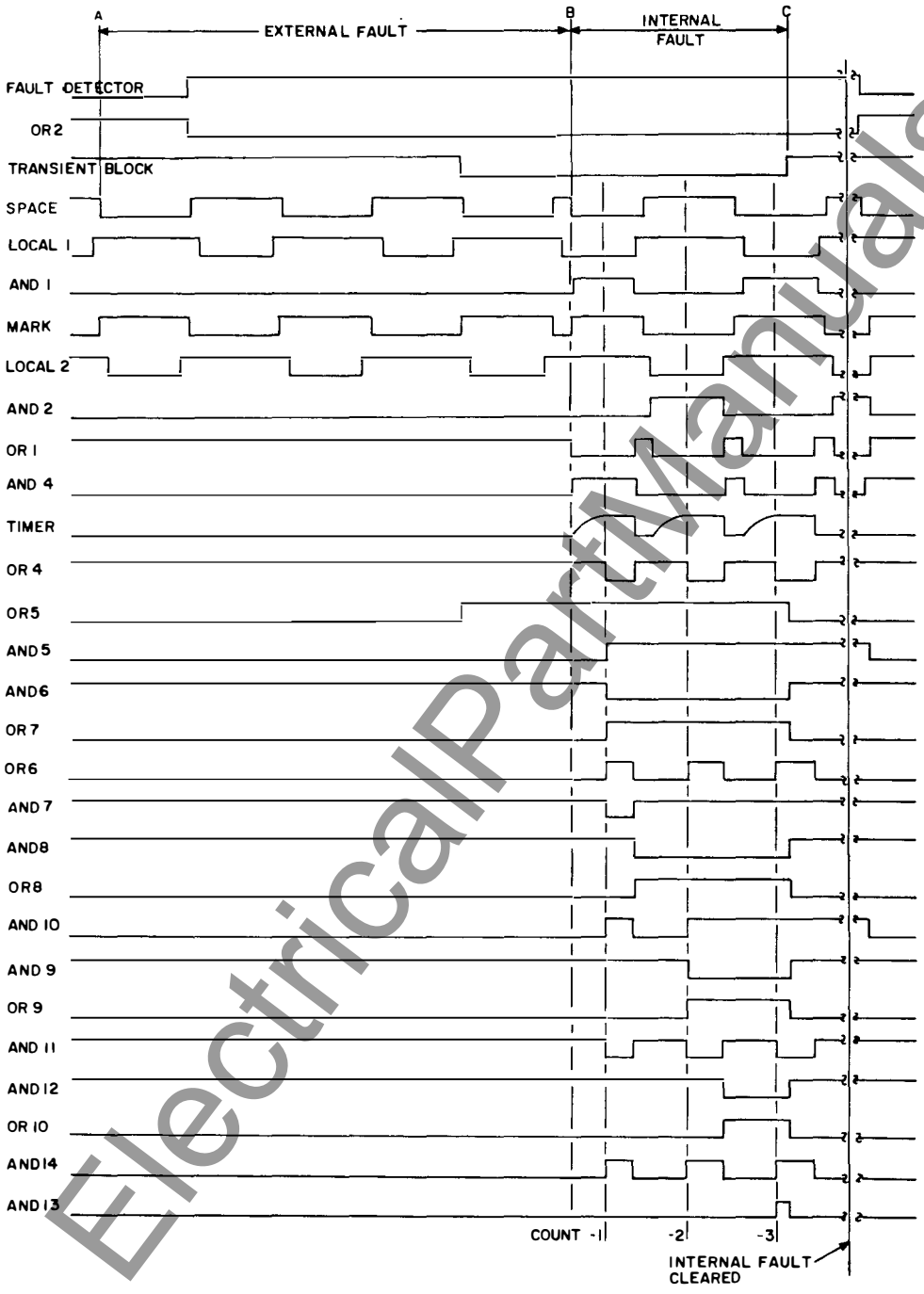


Fig. 23. Timing Waves of Phase Delay Circuit Number 2 of Amplifier and Keying Board



Sub 1
(775B220)

Fig. 24. Typical Timing Waves for Arming Board Circuits

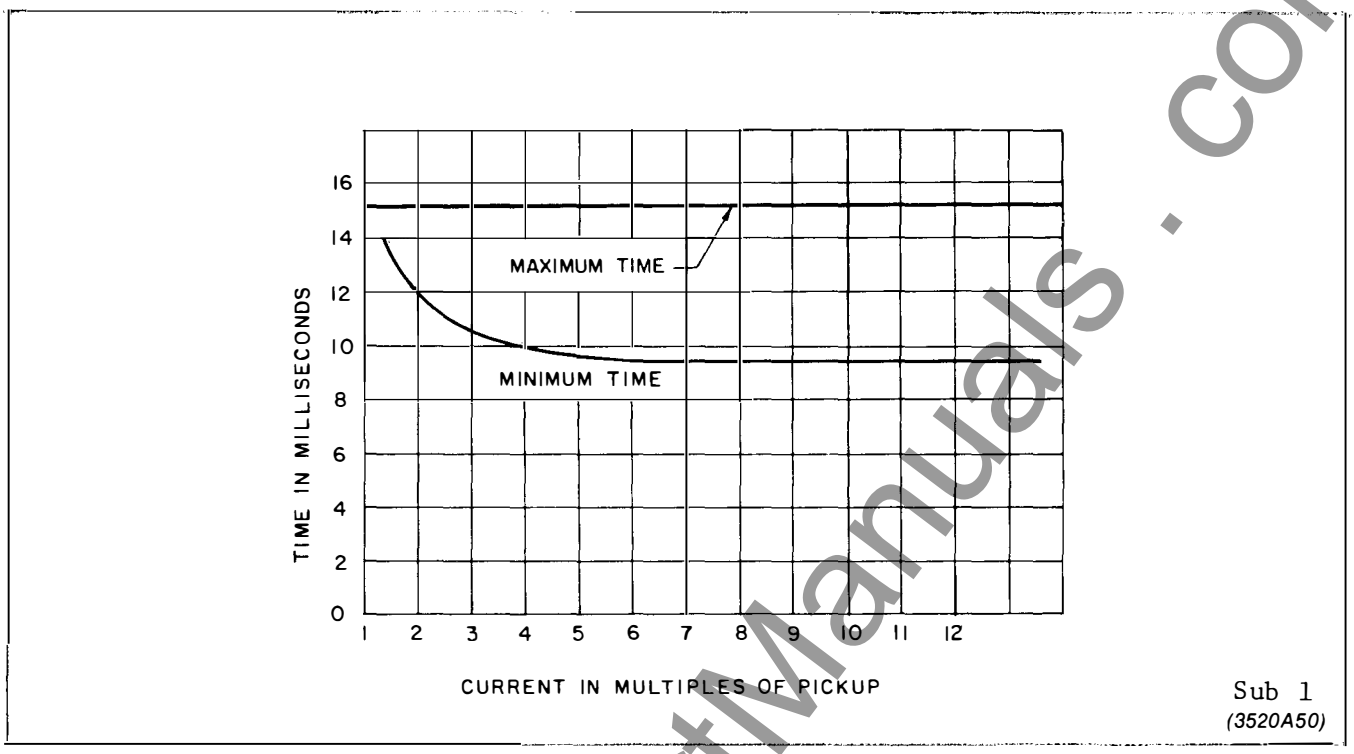


Fig. 25. Operating Times of the Fault Detector of SKBU-2A

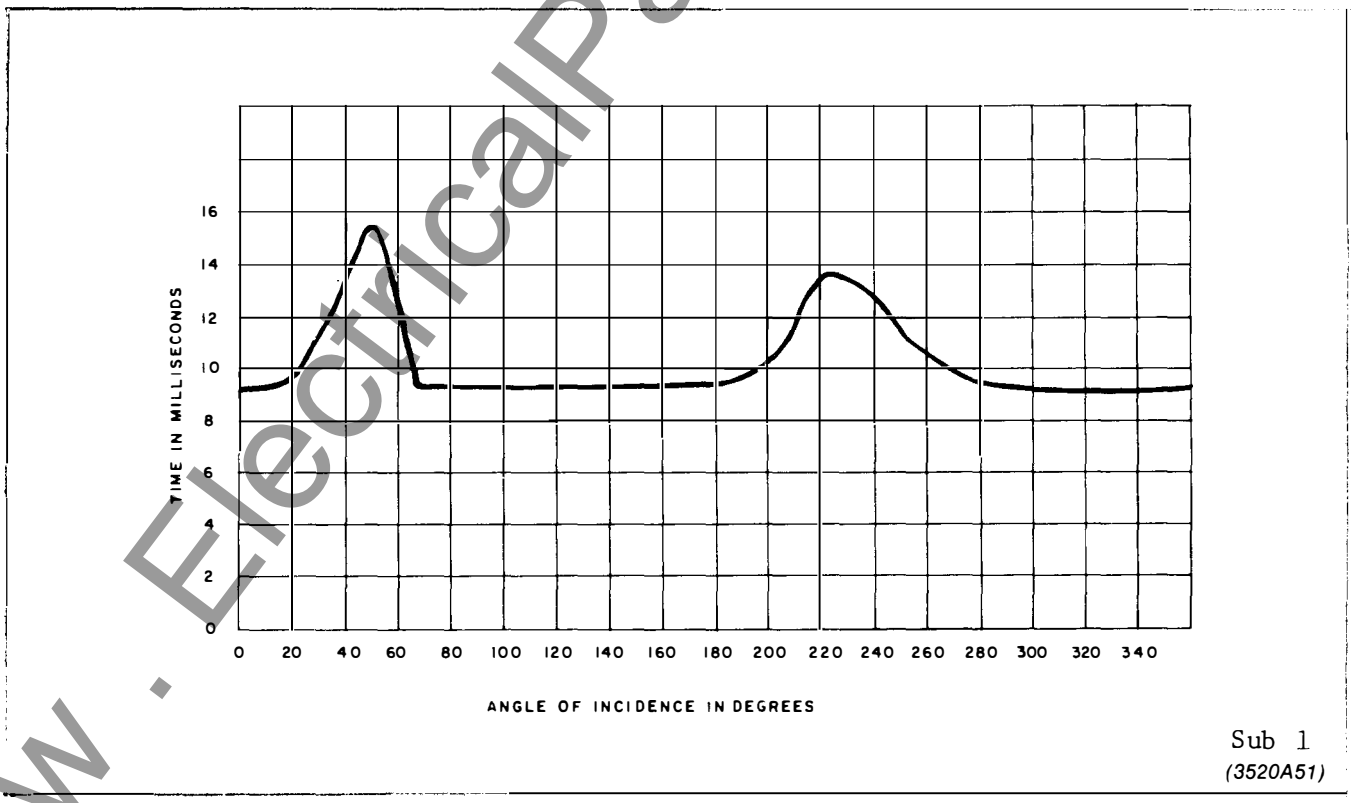
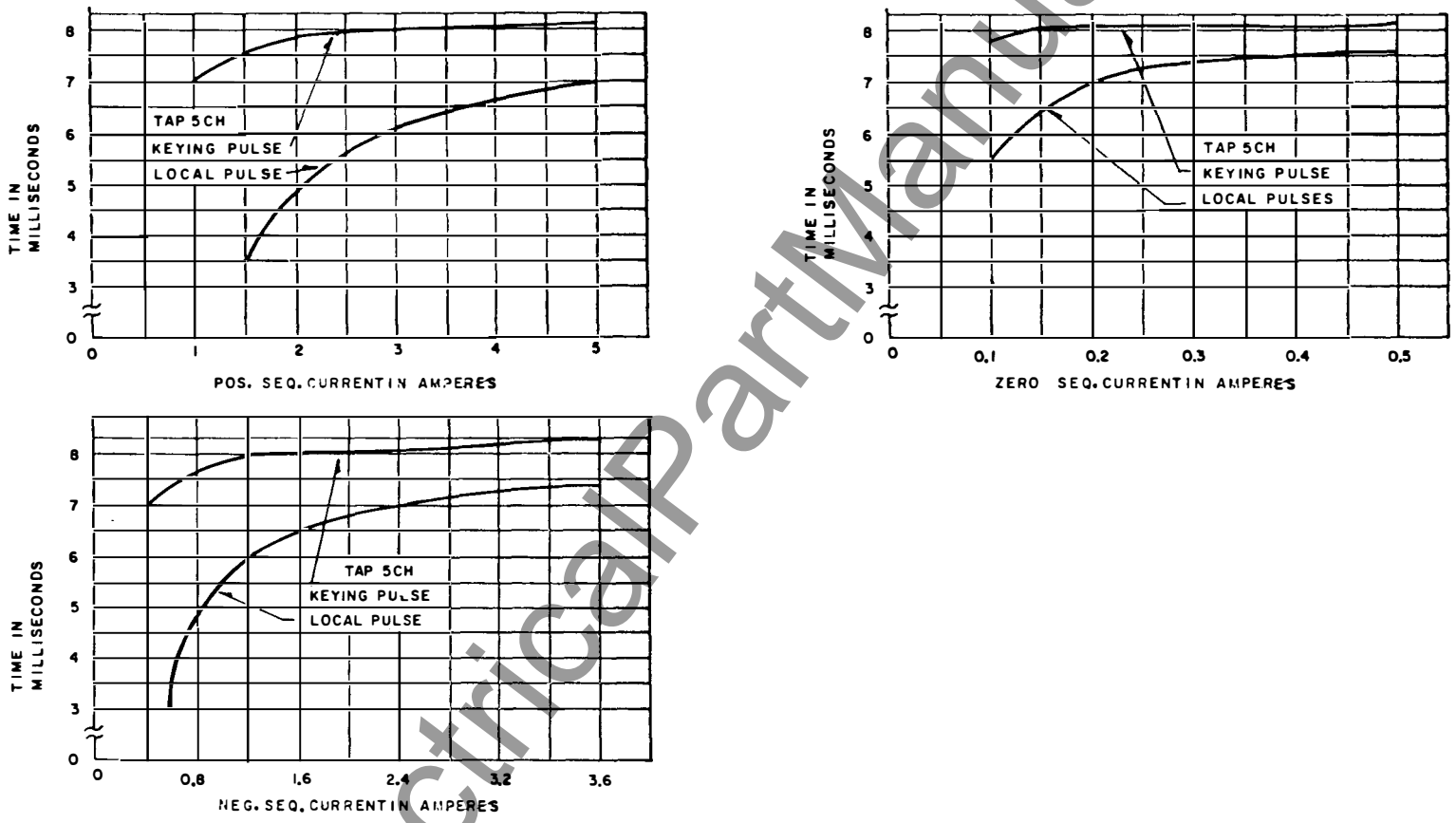


Fig. 26. Operating Times for Fault Detector of SKBU-2A Relay as a Function of Fault Incidence Angle



Sub 2
(775B945)

Fig. 27. Width of Keying and Local Pulses at Different Current Levels of SKBU-2A

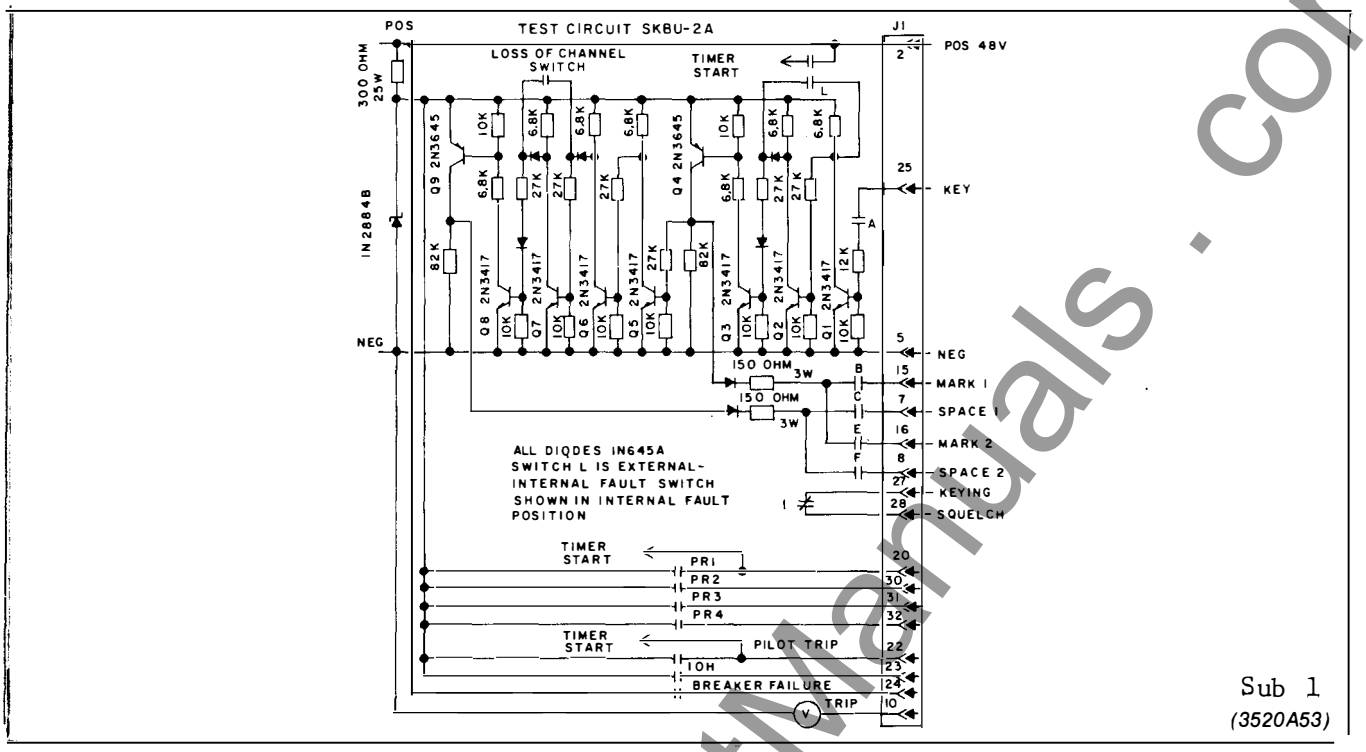


Fig. 28. Test Circuit of SKBU-2A

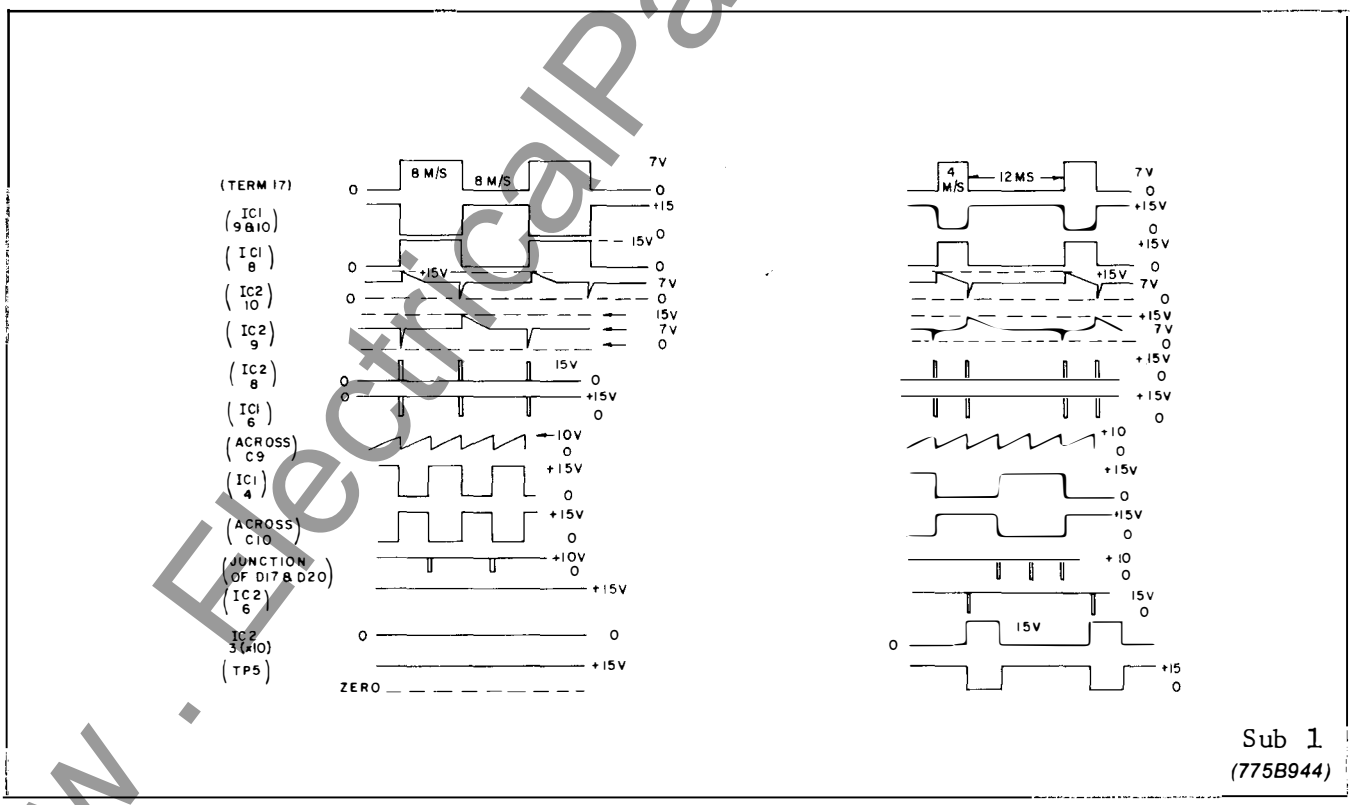


Fig. 29. Waveform of Pulse Width Detector

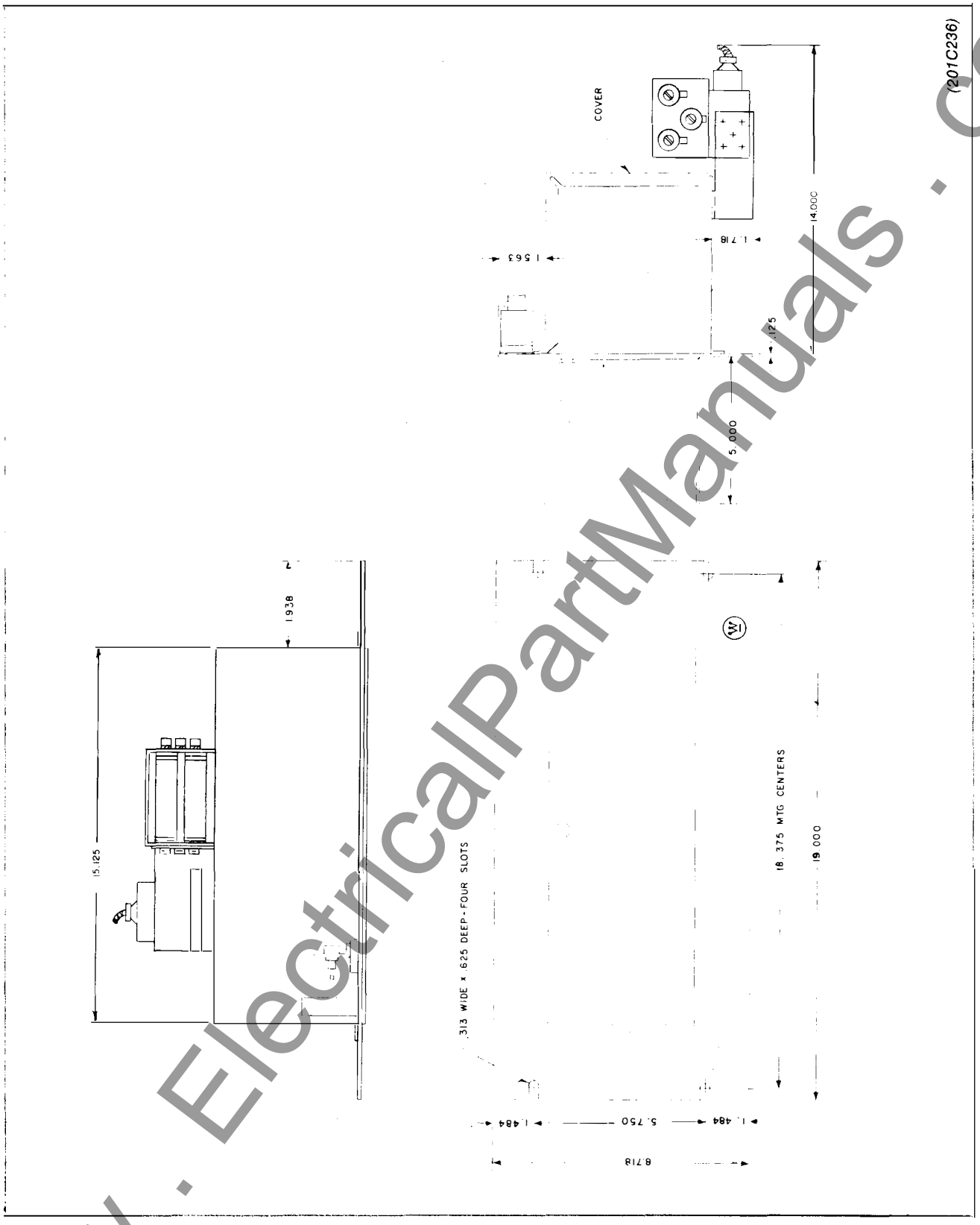


Fig. 30. Outline for the Type SKBU-2A Relay

WESTINGHOUSE ELECTRIC CORPORATION

RELAY-INSTRUMENT DIVISION **NEWARK, N. J.**

Printed in U.S.A

INSTALLATION • OPERATION • MAINTENANCE

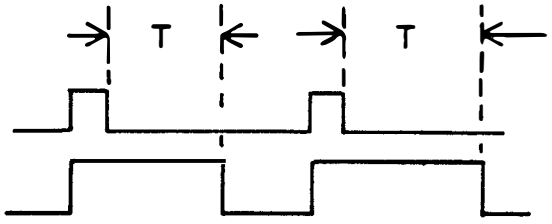
INSTRUCTIONS

TYPE SKBU-2A
DUAL, PHASE COMPARISON RELAY

This addendum to Instruction Leaflet 41-954.6 dated January 1978, relates to a change in the SKBU-2A Relay to improve its security for three-terminal line applications. Modifications have been made to the arming board such that a timer can be set for either 4 milliseconds for two-terminal lines or 5 milliseconds for three-terminal lines.

1. With reference to the schematic drawing of the arming board (figure 5, page 35), the modification consists of changing R37 from a resistor to a 50K trimpot S#880A826H06. Adjustment of this trimpot for proper time delays can be made by means of the 4/0 timer adjustment described on page 17 of I.L. 41-954.6. The same setup and procedures of the instruction leaflet should be followed except "step f".
   Step f should read:

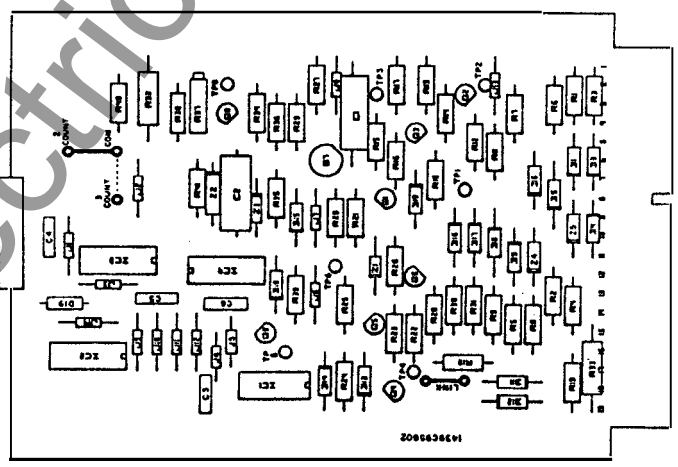
   Adjust trimpot R37 such that the difference in transition time between TP3 and terminal 6 going negative will be as illustrated in the following sketch.



T = 4 MILLISECONDS FOR 2 TERMINAL LINE

T = 5 MILLISECONDS FOR 3 TERMINAL LINE

2. Fig. 4 (page 34) is to be replaced by Fig. 4 below.
3. Fig. 5 (page 35) is to be replaced by Fig. 5 on other side of this sheet.

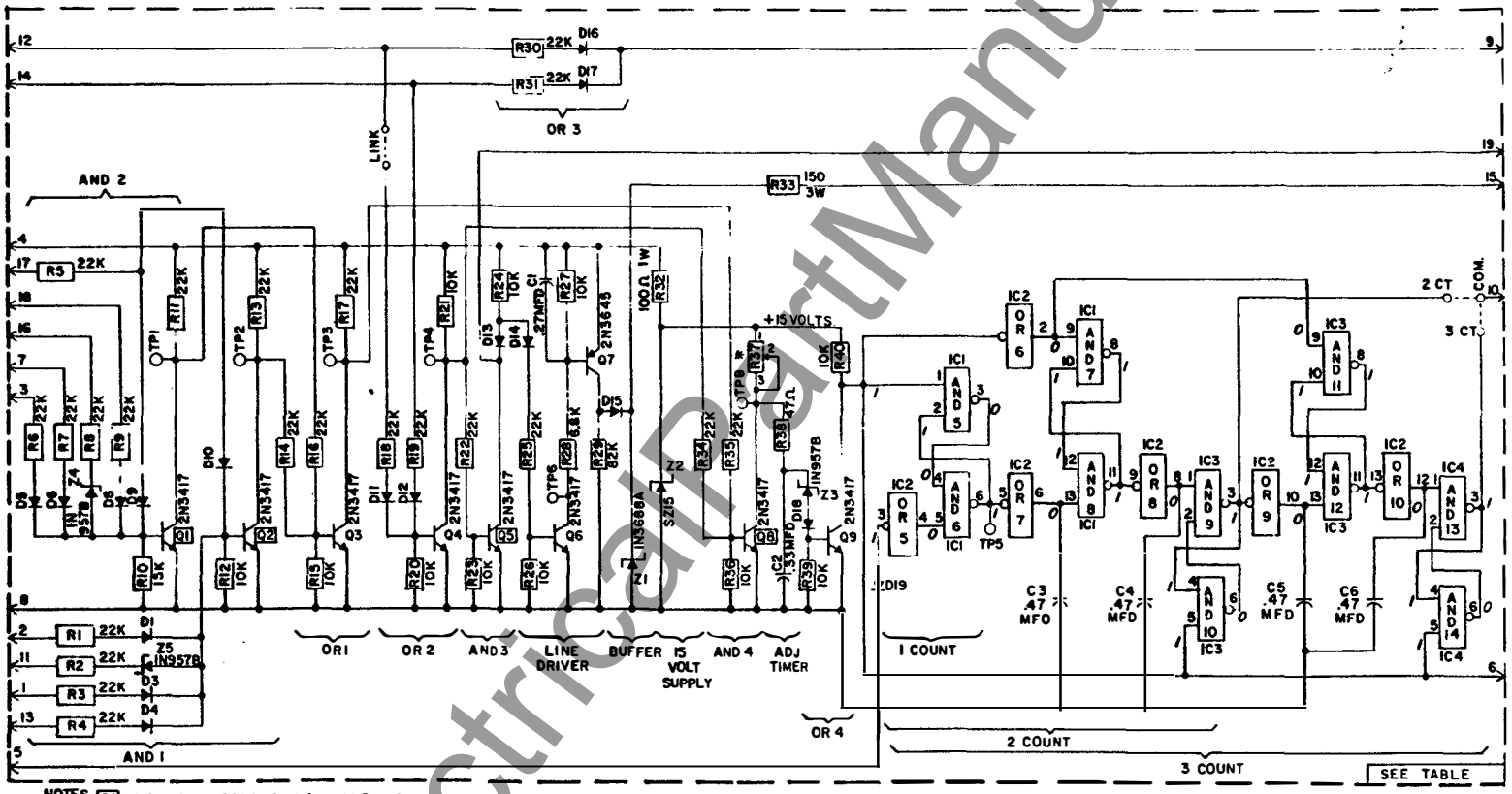


(Sub. 2 1441C70)

Fig. 4 Location of Components on Arming Board.

All possible contingencies which may arise during installation, operation, or maintenance, and all details and variations of this equipment do not purport to be covered by these instructions. If further information is desired by purchaser regarding his particular installation, operation or maintenance of his equipment, the local Westinghouse Electric Corporation representative should be contacted.

STYLE	COMP. R37	TIME DELAY	APPAR
1439C95G01	* 18K (RES)	4 MS	2 TERMINAL LINE
1439C95G02	* 50K (POT)	ADJ.	2 OR 3 TERMINAL LINE



NOTES Q1 = NORMALLY CONDUCTING TRANSISTORS

ALL DIODES IN645A

ONE RESISTOR (R41 NOT SHOWN) CONNECTED TO 4 UNUSED INPUTS ON IC4-9,-10,-12,8-13. WITH OTHER END OF RESISTOR CONNECTED TO +15 VOLTS.

LOGIC STATES SHOWN FOR CONDITIONS OF NO A.C. CURRENT APPLIED TO SEQUENCE NETWORK.

(Sub. 4 1440C26 Sheet 1)

Fig. 5. Schematic of Arming Board.

INSTALLATION • OPERATION • MAINTENANCE

INSTRUCTIONS

TYPE SKBU-2 AND TYPE SKBU-21 DUAL PHASE COMPARISON RELAYS

CAUTION: It is recommended that the user of this equipment become acquainted with the information in this instruction leaflet and on the system instruction leaflet before energizing the system.

Printed circuit modules should not be removed or inserted where the relay is energized. Failure to observe this precaution can result in an undesired tripping output and can cause component damage.

APPLICATION

The type SKBU-2 and SKBU-21 are high-speed relays used in conjunction with frequency shift type channels. Simultaneous tripping of the relays at each line terminal is obtained in less than 32 milliseconds for all internal faults within the limits of the relay settings.

The system is applicable to a voice-grade pilot-wire, micro-wave, or carrier channel.

In contrast to the carrier blocking scheme, this is a transfer trip system; accordingly, the blocking-start function is not required.

* The SKBU-2 and SKBU-21 relays may be applied to two-terminal or three-terminal lines. Two-terminal applications require one transmitter and one receiver per terminal. Three-terminal applications require one transmitter and two receivers per terminal.

All-distance supervision (distance relays provide the arming function for all internal faults) may be applied with both the SKBU-2 and SKBU-21 relays. For these applications, the link in the arming board must be open.

The overcurrent fault detector in the SKBU-2 relay responds to all fault types. Therefore, distance relays are not required to be used with the SKBU-2, although they may be added to improve arming sensitivity. The overcurrent fault detector in the SKBU-21 relay is not responsive to three-phase faults. Therefore, a distance relay, type SKDU-3, is required to supplement the fault detector for SKBU-21 applications.

TABLE OF CONTENTS

These instructions apply to SKBU-21 and SKBU-2 phase comparison relays for application to the following types of pilot channels.

1. TA-2 Tone Channel.
2. TA-2.1 Tone Channel.
3. TCF Carrier Channel.
* 4. TA-2.2 Tone Channel.
* 5. MC-22 Microwave Channel.

CONSTRUCTION

The phase comparison relays consist of a composite positive and negative sequence current network, a saturating transformer, three isolating transformers, a 20-volt power supply, and printed circuit boards mounted on a standard 19-inch wide panel, 8¾ inches high (5 rack units). The SKBU-21 relay has a second saturating transformer in addition to these components. Edge slots are provided for mounting the rack on a standard relay rack.

Sequence Network

a. SKBU-21

The sequence filter consists of a three-legged iron core reactor and a resistor. The reactor is a four-winding reactor with two primary windings and two secondary windings. The secondary windings are connected to the resistor which consists of three tube resistors and a small formed resistor: One secondary winding and the resistor is a negative sequence current filter while the other secondary winding and the resistor is a positive sequence filter.

b. SKBU-2 Relay

The sequence filter consists of a three-legged iron core reactor and a set of resistors, R_1 and

All possible contingencies which may arise during installation, operation, or maintenance, and all details and variations of this equipment do not purport to be covered by these instructions. If further information is desired by purchaser regarding his particular installation, operation or maintenance of his equipment, the local Westinghouse Electric Corporation representative should be contacted.

SUPERSEDES I.L. 41-954.5C, dated August 1972
* Denotes change from superseded issue.

EFFECTIVE JANUARY 1976

R_0. The reactor has three windings: two primary and a tapped secondary winding, wound on the center leg of an "F" type of lamination. The secondary taps are wired to the A, B and C tap connections in the front of the relay (R_1 taps). Ro consists of three tube resistors with taps wired to F, G and H tap connections in the front of the relay. The R_0 resistor is a formed resistor associated with the tapped secondary of the reactor.

Saturating Transformer

a. SKBU-21 Relay

The voltage from the sequence network is fed into two saturating or mixing transformers. One transformer supplies a fault detector circuit and the other transformer supplies a keying circuit. Zero sequence current windings are included on the transformer.

b. SKBU-2 Relay

The voltage from the sequence network is fed into the tapped primary of a saturating transformer which has two secondary windings. One winding supplies the fault detector and the other winding supplies a keying circuit.

Isolating Transformer

Three isolating transformers are provided in the relay to isolate the dc voltages from the ac voltages. Two of the transformers are also used to energize solid-state circuit on alternate half-cycle of the power system frequency.

Power Supply

The solid-state circuits of the relays are regulated from a 20-volt supply on the relay panel. This voltage is taken from a Zener diode mounted on a heat sink. A voltage dropping resistor is provided between the source dc supply and the 20 volt regulated supply.

Printed Circuit Boards

Seven printed circuit boards are used in these relays: A fault detector board, protective relay interface board, supervision board, amplifier and keying board, output board and a relay board. The circuits of the supervision board, and the amplifier and keying boards vary with the frequency shift equipment used as a pilot channel.

All of the circuitry that is suitable for mounting on printed boards is contained in an enclosure that projects from the rear of the front panel and is accessible by opening a hinged door on the front of the panel. The printed circuit boards slide in position in slotted guides at the top and bottom of each compartment and the board terminals engage a terminal block at the rear of the compartment. Each board and terminal block is keyed so that if a board is placed in the wrong compartment, it cannot be inserted into the terminal block. A handle on the front of each board is labeled to identify its function in the relay.

1. FD Board (Fault Detector Board)

The fault detector board contains a resistor-Zener diode combination, a phase splitting network, a solid-state fault detector, and a frequency verifier circuit. The controls for setting pickup (S_1) and dropout (S_2) of the fault detector are mounted on a plate in the front of the relay. This unit operates when the fault current exceeds a definite value.

The location of components on the board is shown in Fig. 3 and the schematic of the board is shown in Fig. 4.

2. Arming Board

The arming board contains AND circuits that compares pulses produced by the circuits of the amplifier and keying board. An output is obtained that is proportional to the time difference in the phase. This board contains other logic circuits that will arm the trip output, set up the time delay of the trip output, and start transient blocking on external faults. A link is provided on this board such that the relay is armed by either solid state distance fault detectors or the SKBU fault detector. The link must be open for arming by the solid state distance fault detector only.

The location of components on the board is shown in Fig. 5 and the schematic of the board is shown in Fig. 6.

3. Ampl. and Key Board (Amplifier and Keying Board)

The amplifier and keying board contains two local squaring amplifiers, a transmitter keying circuit, and four remote squaring amplifiers. These These circuits produce the pulses that are compared by the AND circuits of the arming board to determine if the fault is external or internal. Links are provided on this board to connect the relay for two or three terminal operation. For two terminal applications, link 1 and link 2 on the Amplifier and Keyer Board must be connected C to 2. For three terminal applications, these links must be connected C to 3.

Because of the different keying requirements of the various pilot channels, this board varies with the different types of channels to which it is connected. The following table is with reference to the different figures that apply for the amplifier and keying board for the various type channels.

TYPE CHANNEL	LOCATION OF COMPONENTS	SCHEMATIC OF BOARD
TA-2	Fig. 7	Fig. 8
* TCF, TA2.2, MC-22	Fig. 9	Fig. 10

4. Output Board

The output board contains a 4-millisecond pickup and instantaneous dropout timer circuit, trip AND circuit, trip amplifier, transient blocking and unblocking circuits and two timer circuits. The trip AND operates when all the inputs to the arming board are of the correct polarity and the fault detector has operated. The transient blocking circuit operates after a time delay on external faults, and the transient unblock circuit operates after a time delay on a sequential fault (external fault followed by an internal fault).

The following figures apply to this board: Fig. 11 Component Location; Fig. 12 Schematic of the Board.

5. Relay Board

The relay board contains the phase delay circuit for shifting the local signals with reference to the remote signals. It also contains a low-pass filter. For the SKBU-21 relay, a Zener clipper-resistor combination is provided for protection of the solid-state circuits.

The following figures apply to this board: Fig. 13 Component Location; and Fig. 14 for the Schematic of the Board.

6. Supervis. Board (Supervision Board)

The number of circuits on this board varies with the application. However, for all applications interface circuits to the channel receivers and a 150 millisecond pickup and 0 millisecond dropout alarm timer circuit is provided on this board. The interface circuits connects the SKBU relay to the channel receiver, and the timer circuit locks out the relay for failure of the channel equipment. For tone channels a noise circuit is also provided to lockout the relay from information supplied by the tone equipment.

Because the board varies with the channel equipment, the following figures apply to the board.

TYPE CHANNEL	LOCATION OF COMPONENTS	SCHEMATIC OF BOARD
TA-2	Fig. 15	Fig. 16
TA-2.1	Fig. 15	Fig. 35
TCF, TA2.2, MC-22	Fig. 17	Fig. 18

7. Pr. Inter. Board (Protective Relay Interface Board)

The protective relay board contains logic circuits to connect the distance fault detectors, and squelch relays into the phase comparison relaying system. This board contains buffer circuits, and OR circuits to connect the relays into the system. A 6/0 timer circuit, 10/150 signal squelch circuit, and 2.5 second alarm circuit for sustained fault detector operation are also provided on this board.

Card Extender

A card extender (style no. 644B315G02) is available for facilitating circuit voltage measurements or major adjustments. After withdrawing anyone of the circuit boards, the extender is inserted into the terminal block on the front of the extender. This restores all components and test points on the boards are readily accessible.

Test Points

Test points are located on each printed circuit board for the major components on the board. Complete circuit test points are wired to the front panel of the relay for convenience in adjusting and testing the relay.

OPERATION

A. System

In a phase comparison relaying, the phase position of fault currents at the ends of a transmission line are compared over a pilot channel to determine if the fault is internal or external to the line section. When a frequency shift channel is used as the pilot channel, a dual comparison system can be utilized. This means that the system can trip on either half-cycle or power system frequency as contrasted to a blocking scheme where tripping occurs on alternate half-cycles during the absence of a carrier signal.

a. SKBU-21 Relay

The three-phase line currents energize a sequence network in the SKBU-21 relay which produces two single-phase output voltages that are proportional to either the positive sequence current or the negative sequence current. The single-phase voltages are applied to two saturating or mixing transformers, one which energizes the fault detector circuit and the other energizes the keying circuit of the SKBU-21 relay through a low-pass filter. The keying circuit shifts the frequency of the transmitter from a space frequency to a mark frequency. These frequencies are transmitted over the pilot channel to the receiver which converts the mark and space frequencies to two dc output voltages, a space output that corresponds to the mark frequency. Thus, on each half-cycle of power system frequency either a space or mark output is obtained from the receiver and applied as pulses to the remote squaring amplifiers of the SKBU-21 relay. Each of these half-cycle pulses are compared with the phase positions of each half-cycle of the voltage from the sequence network of the SKBU-21 relay at the receiver terminal. The space pulse is compared to one half-cycle of the voltage and the mark pulse to the other half-cycle. If the local and remote pulses are in an internal fault relationship and the fault detector has operated, tripping will occur 5 milliseconds later through operation of the trip AND and trip amplifier circuits on the output board of the relay.

b. SKBU-2 Relay

The three-phase line currents energize a sequence network in the SKBU-2 relay which produce a single-phase output voltage proportional to a combination of sequence components of the line current. This single-phase voltage energizes the primary of a saturating transformer with two secondary winding. One secondary winding energizes the fault detector circuit and the second secondary winding energizes the keying circuit of the relay through the low pass filter. The keying circuit shifts the frequency of the transmitter from a space frequency to a mark frequency. These frequencies are transmitted over the pilot channel to the tone receiver which converts the mark and space frequencies to two dc output voltage, a space output that corresponds to the space frequency and a mark output that corresponds to the mark frequency. Thus, on each half cycle of power system frequency either a space or mark output is obtained from the tone receiver and applied as pulses to the remote squaring amplifiers to the SKBU-2 relay. Each of these half-cycle pulses are compared with the phase positions of each half-cycle of the voltage from the sequence network of the SKBU-2 relay at the tone receiver terminal. The space pulse is compared to one half cycle of the voltage and the mark pulse to the other half-cycle. If the local and remote pulses are in an internal fault relationship and the fault detector has operated, tripping will occur 5 milliseconds later through operation of the trip AND and trip amplifier circuits on the output board.

Current transformer connections to the sequence networks at the two line terminals are such that the space and mark pulses are in phase with their respective local pulses during an internal fault to allow tripping. However, if the fault is external to the protected line section, the space and mark pulses are out-of-phase with their respective local pulses and tripping does not occur.

The four-millisecond delay previously mentioned is added to allow for differences in current transformer performance at opposite line terminals and relay coordination.

B. Relay

With reference to the logic diagram that applies to the particular relay, the three-phase line currents energize a sequence filter that varies with the type of relay.

a. SKBU-21 Relay

In the SKBU-21 relay, the sequence filter produces two single phase voltages: One voltage proportional to the positive sequence current, and the other voltage proportional to negative sequence current. These voltages are applied to primary windings of two saturating transformer where they are mixed to produce two separate secondary voltages proportional to a combination of sequence components. Zero sequence windings are included on the two transformers.

b. SKBU-2 Relay

In the SKBU-2 relay, the sequence filter pro-

duces a single phase voltage proportional to a combination of sequence components. This voltage is applied to the primary winding of a saturating transformer which produces two secondary voltages.

The secondary voltages are applied to two separate boards:

1. Fault Detector Board
2. Relay Board

1. Fault Detector Board

With reference to the schematic dwg. of Fig. 4, the ac voltage is applied to terminals 6, 5 and 3 of the fault detector board. This voltage is then applied to a phase-splitting network (C52, R52, R53) and a polyphase rectifier (diodes D51 to D56). The dc voltages obtained from the rectifier are applied to the fault detector circuit (Q51, Q52, Q53, Q54) which operates when the dc input "signal" exceeds a predetermined value.

Fault Detector (FD)

Under normal conditions, transistor Q51 has no base "signal" and is turned off. The collector of Q51 is at positive potential and provides base drive to transistor Q52, driving it to conduction. With Q52 conducting there is no base drive to transistor Q53 and Q53 is turned off. This condition keeps transistor Q54 in a non-conducting state, equivalent to an open-circuit.

When a fault causes the dc input voltage from the polyphase rectifier (across S_1 and R54) to exceed the 6.8 volt rating of Zener diode Z52, a positive input is applied to the base of Q51 causing it to conduct. In turn, Q52 stops conducting, and capacitor C54 charges, giving a few milliseconds time delay before Q53 and Q54 are switched to full conduction, thus "closing" the fault detector. When the fault detector operates, a positive input is applied to the arming board at terminal 12. The feedback path of resistors R66 and S2 increase the voltage to Z52 after the fault detector operates. This seals in the fault detector and allows the fault detector to drop at a high drop-out ratio when the ac current is reduced.

Frequency Verifier (FV)

During certain switching conditions, such as energization of a transmission line, residual currents and voltages may exist of higher frequencies than 60 hertz. The frequency verifier prevents fault detector operation when frequencies 120 hertz or higher are encountered during the switching conditions. The frequency verifier circuit consists of two functional parts: Zero-crossing and commutator circuits. With reference to Fig. 4, the zero-crossing circuit consists of Q55, Q56, Q57 and Q58. The commutator circuit consists of Q59, Q60, C58, C59, Z54 and Q61.

During either the positive or negative half-cycles of the output voltage from the mixing transformer, Q55 or Q57 transistors are driven into saturation by the output of the FV transformer (T3). Transistors Q56 or Q57 conduct until capacitors C56 or C57 respectively are fully charged. While either capacitor charges, a voltage output in the form of very narrow pulse is developed across R76 and R78 resistors. This pulse triggers Q59 control switch. When transistors Q55 or Q57 are not conducting, C56 and C57 capacitors discharge respectively through D66 or D62 and the parallel combination of R73 and R74 or R69 and R70.

While Q59 is "on" its anode (TP-60) is only about 0.7 volts above negative, thus turning off transistor Q62 to allow capacitor C60 to start charging. However, a shorter time delay (consisting of R84, the capacitor C59 and the reference Zener diode Z54) of 4.3 milliseconds is also started. After 4.3 milliseconds of delay, the control switch Q60 fires applying the voltage of capacitor C58 across C59 turning it off. This raises the potential of the Q59 anode to turn on Q62 to discharge C60 before the charge reaches a value to break down Z55 to turn on Q63. After the next zero-crossing pulse Q59 switch is turned on again, and the Q60 switch is turned off by capacitor C58. Transistor Q61, when turned on and off by the same voltage that fires the gate of Q59, discharges timing capacitor C59, when on. This starts the timing cycle with close to zero charge on the capacitor. If the zero crossing period of the FV voltage is less than 4.3 milliseconds, the Q61 transistor discharges the timing capacitor to prevent Q60 from turning on. This keeps Q59 switch on to allow C60 to charge to a value to break down Zener diode Z55 to turn on Q63. Turning on Q63 prevents Q53 of the fault detector from turning on, thereby preventing Q54 from turning on and this prevents an output from the fault detector.

2. Relay Board

With reference to Fig. 14, the ac voltage from either the second saturating transformer (SKBU-21) or the second winding of the single transformer (SKBU-2) is applied to terminals 10 and 12 of the

relay board. This voltage is applied to the phase delay circuit through a low pass filter. The low pass filter (C201, L201, C202) removes the harmonics from this voltage and applies a voltage that is essentially sinusoidal in waveform to R202 and R203 of the phase delay circuit. The phase delay circuit consists of R202, R203, C203 and S5 mounted on the front panel of the relay. By means of capacitor C203 and variable resistor S5, the voltage across terminal 4 and 2 can be made to lag the voltage across terminal 10 and 11 by a definite amount depending on the setting of S5. Each of these two voltages are applied to separate isolating transformers.

1. Undelayed voltages (terminals 10 and 11) to keying transformer (T1).
2. Delayed voltage (terminals 4 and 2) to local transformer (T2).

a. Keying Circuit

With no ac output (Ref. Fig. 8 or 10) voltage from the sequence network, transistor Q1 has no base current from terminals 2 and 8 of the amplifier and keying circuit. The collector of Q1 is at positive potential which allows base current to flow from positive 20 volts dc to the base of Q2 through R2 and R3. This applies negative potential to the collector of Q3 to prevent base current from flowing to Q3. Since Q2 is conducting, transistor Q3 does not conduct and the collector of Q3 is held at positive potential. As a result, transistor Q4 does not conduct.

When a sinusoidal voltage is applied to the keying transformer (T_1), the transformer steps up the voltage applied to terminals 2 and 8 of the amplifier and keying board. On the positive half-cycle of this voltage, terminal 8 is more positive than terminal 2 and transistor Q1 does not conduct.

In turn Q2 remains conducting and Q3 does not turn on. On the negative half-cycle of sine wave voltage from the keying transformer (T_1), terminal 2 is more positive than terminal 8 and base current flows in Q1. This turns Q1 on which applies negative potential to the collector of Q1. Base current to transistor Q2 is stopped and Q2 stops conducting, and its collector goes to positive potential. Positive potential is thus applied to the base of Q3 through R6 to turn on Q3. When Q3 conducts, its collector is connected to negative potential and Q4 will conduct. Thus an alternate half-cycles of the 60-hertz voltage from the low pass filter, Q4 turns on. By connecting Q4 through the proper interface to the channel transmitter, turning on Q4 keys the transmitter to a mark condition.

Q3 can be prevented from turning on and off by a negative signal applied to terminal 3 of the board. This is the input terminal from the signal squelch circuit of the protective relay board. With a negative input into terminal 3, Q3 will not turn on even though Q1 and Q2 are being turned on and off from the ac voltage applied to terminals 2 and 8.

b. Local Squaring Amplifiers (1 and 2)

There are two identical local squaring amplifiers in the SKBU-21 and SKBU-2 relays. (Number 1 Q5, Q6, Q7 and number 2 Q12, Q13 and Q14.) One is turned on and off by the positive half-cycle of voltage from the local transformer (T2) while the other one is turned on and off by the negative half-cycle of voltage from the transformer (T2). The square wave output voltages are, therefore, functions of the ac voltage input to the amplifiers. The polarity of the outputs of the two amplifiers are such that one amplifier has an output and the other one does not when ac voltage is applied to the local transformer. With no ac signal applied to the local transformer, both local amplifiers have a positive output. (This is a blocking signal to the AND circuits of the arming board.)

With reference to amplifier number 1 of either Fig. 8 or 10, with no ac input voltage, Q5 is not conducting and the collector of Q5 is at positive potential. This applies base current to transistor Q6 through R14 and R15 such that Q6 is turned on. This allows base current to flow in Q7. Q7 turns on to apply positive potential across R19 (blocking condition).

With the application of a sine wave voltage to terminals 5 and 18 of the amplifier and keying board, on the positive half-cycle of the voltage, the base of transistor Q5 is more positive than the emitter and Q5 (amplifier 1) conducts, and Q12 (amplifier 2) is turned off. On the negative half-cycle of the ac voltage, Q5 is turned off and Q12 is turned on. Therefore, Q5 is conducting on the positive half-cycle of ac voltage and Q12 is conducting on the negative half-cycle of ac voltage. Turning Q5 on, turns off transistor Q6. Transistor Q6 stops conducting

and its collector goes to a positive potential which turns off Q7. Thus the output of the squaring amplifier is a square wave voltage ranging from 0 volts dc to 20 volts dc depending upon the polarity of the voltage from the phase delay circuit.

Amplifier 2 is the same as amplifier number 1 except it is supplied by the opposite polarity of sine wave voltage from the local transformer (T2) at terminals 5 and 18 of the amplifier and keying board. The output voltage from this amplifier appears across R42. By applying the same analysis of amplifier 1 to amplifier 2, the output voltage across R42 is a square wave voltage of the reversed polarity than that across R19.

c. Remote Squaring Amplifiers

As shown in Fig. 7, there are four remote squaring amplifiers in both the SKBU-2 and SKBU-21 relays (number 3 Q8, Q9, number 5 Q10, Q11, number 4 Q15, Q16 and number 6 Q17 and Q18). Two amplifiers connect the space outputs of two receivers to the relay while the other two amplifiers connect the mark outputs of the two receivers to the relay. For a TA-2 tone channel, space squaring amplifier 3 consists of transistors Q8 and Q9 on the amplifier and keying board in conjunction with an interface circuit of Q13 and Q1 on the supervision board. Mark remote squaring amplifier 4 consists of Q15 and Q16 on the amplifier and keying board and interface transistor Q14 and Q2 on the supervision board (see Fig. 37). For a TCF carrier channel, space squaring amplifier 3 consists of Q1 on the supervision board and Q8 and Q9 on the amplifier 4 consists of Q2 on the supervision board and Q15 and Q16 on the amplifier and keying board. (See Fig. 38)

The remote squaring amplifiers are in one of three states:

1. Loss-of-channel state.
2. Receiving space frequency only.
3. Receiving alternate half-cycles of space and mark frequency.

a. TA2.1 Tone Channel (See Fig. 37)

For loss of a tone channel, the receiver clamps its output to a mark condition. The space output from the receiver is zero with respect to the positive source. This means that transistor Q13 and Q1 (on the supervision board) are not conducting. On the amplifier and keying board, base drive to transistor Q9 is provided from positive 20 volts dc through R26 and R27 to negative. Q8 is turned on to provide a positive 20 volts across R23. When the channel is in service and the receiver is in a space condition, transistors Q13 and Q1 (on the supervision board) turn on. This applies negative potential to R27 on the amplifier and keying board. Hence, Q9 can not conduct and Q8 stops conducting. The voltage across R23 is −20 volts (with ref. to +20 volts). For the condition where the receiver is receiving pulses, transistors Q13 and Q1 (on supervision board) turns on and off and the voltage across R23 of the amplifier and keying board is a square wave voltage varying from zero volts to a −20 volts dc (with ref. to +20 volts). The output of the mark remote squaring amplifier is the same as the space remote amplifier except that it operates off of the mark output of the receiver. The voltage is across R43.

b. TCF Channel (See Fig. 38)

For loss of a TCF carrier channel, the carrier receiver clamps its output into both a space and a mark condition. Transistor Q1 and Q2 on the supervision board turn on. This removes base current to Q9 and Q16 (on amplifier and keying board) respectively. Transistors Q9 and Q16 turn off which turns off Q8 and Q15. Negative 20 volts (with ref. to +20 volts) appears across both F23 and R24.

This voltage enables AND 1 and AND 2 to allow tripping until the AND circuits are disabled by the 150/0 timer of the supervision board.

For the condition where the receiver is receiving pulses, transistor Q1 (on supervision board) turns on and off for alternate half cycles and the voltage across R23 (on amplifier and keying board) is a square wave voltage varying from zero volts to a −20 volts dc (with ref. to +20 volts).

c. TA2.2 Tone Channel and MC-22 Microwave Channel (See Fig. 38)

In applying the relay to the TA2.2 tone channel or MC-22 microwave channel, the channel receivers clamp their outputs into neither a space nor mark condition for a loss of channel.

Transistors Q1 and Q2 on the supervision board turn off. This allows base current to flow into Q9 and Q16 on amplifier and keying board). Transistors Q9 and Q16 turn on which turns on Q8 and Q15. Positive 20 volts (ref. to negative) appears across both R23 and R24. This positive voltage inhibits AND 1 and AND 2 of the arming board to prevent tripping during the loss of channel.

For either internal or external fault conditions the outputs of both remote squaring amplifiers are square wave voltages. Both voltages vary from zero volts to approximately −20 volts dc and are out of phase with each other: i.e., when one voltage is at zero volts the other voltage is at −20 volts.

Links are provided on the board to connect the relay for either two or three terminal lines. The connection of C to 3 on link 1 connects remote squaring amplifier 5 to AND 1 of the arming board, and link 2 (C to 3) connects remote squaring amplifier 6 to AND 2 of the arming board for three terminal operation. For two terminal operation the connection of C to 2 on the links removes the inputs of remote amplifier 5 and 6 from the AND circuits of the arming board.

3. Arming Board

The phase relationship of the outputs of the local and remote squaring amplifiers are compared by the two AND circuits of the Arming Board. One AND circuit (number 1) compares the space signal with the output from local amplifier number 1. The second AND circuit (number 2) compares the mark signal with the outputs of local amplifier number 2. Since the local signals are always 180 degrees out-of-phase with each other, and the remote signals are always 180 degrees out-of-phase with each other, a change in phase angle of one signal with respect to the other will provide one input to AND 3 through OR 1 which will activate the 4/0 timer.

A link is provided on this board for purposes of arming the relay with both distance fault detectors and the SKBU relay fault detector. Removal of the link allows arming by distance fault detector only.

a. Internal Fault Conditions

With reference tothe logic drawing that applies to the particular relay for internal fault fed from both line terminals, the output voltage of the sequence filter at one line terminal is 180 degrees out-of-phase with respect to its load current condition. This changes the polarity of local Amplifier 1 and local Amplifier 2 such that their outputs are in phase with the remote signals. This means that AND 1 has a half-cycle of negative voltage and that AND 2 has a half-cycle of negative voltage (not the same half-cycle). The period of each negative voltage will be 180 degrees out-of-phase with reference to each other and a negative voltage will be produced out of OR1 of the arming board. The negative voltage is applied to AND 3 of the arming board to set-up one condition (negative voltage from OR 1 circuit) for activating the AND. The second condition to activate this AND is provided by arming the relay.

In either Fig. 21, 22, 23 or 24, with the link connected on the arming board, arming occurs through OR 2 by either the operation of the distance fault detectors or the relay fault detector will apply a voltage to OR 2 of the arming board. The output voltage from OR 2 applies a positive input to the trip AND of the output board through OR 3 and a negative input into AND 3 of the arming board. AND 3 is activated and starts the 4/0 timer. Four milliseconds later, a negative input is applied to the trip AND of the output board. Since the three conditions of trip (a negative input from the 4/0 timer, a positive input from the arm lead, and a positive signal from the 22/0 timer) is fulfilled, a trip output is obtained from the relay.

For arming by the distance fault detector only, the link on the arming board must be opened. This removes the input of the SKBU relay's fault detector from OR 2 of the arming board.

b. External Faults

Under external fault conditions, the square wave voltages from the remote squaring amplifiers and the square wave voltages from the local squaring amplifiers are out-of-phase such that zero output is obtained from the AND

circuits of the arming board. The output from local 1 and remote 3 are out-of-phase to prevent an output on AND 1 and the outputs from local 2 and remote 4 are out-of-phase to prevent an output on AND 2. As a result, the outputs of the AND circuits are zero, and AND 3 cannot be activated. This blocks AND 3 and the 4/0 timer cannot be energized.

With a fault detector operation, an input is applied to OR 2 and OR 4 of the arming board. OR 2 will provide a positive input to the trip AND of the output board. Tripping will not occur since the 4/0 timer does not provide a negative input to the Trip AND. The fault detector input to OR 4 will provide an input to a 0/1000 timer on the Output Board. The timer negates the signal to provide a negative input to the transient block AND. With the application of the negative input from the 0/1000 timer the three conditions of transient block are fulfilled – not a negative voltage from the Trip AND, not a positive voltage from the Transient Unblock Circuit; and a negative input from the 0/1000 timer. Twenty-Two milliseconds later the 22/0 timer of the transient block circuit times out to provide a negative input to the Trip AND. The Trip AND is thus de-sensitized on the external fault to prevent undesirable operation during transients associated with power reversals on the protective line or at the clearing of an external fault.

c. Sequential Faults

If the above external fault is followed by an internal fault before the external fault is cleared, the transient unblock circuit is set up to remove the transient blocking input to the Trip AND. For the internal fault, the square wave pulses on AND 1 and AND 2 of the arming board will reverse such that an output is obtained from these AND circuits. This output energizes OR1 which negates the signal to a negative signal. The negative signal provides the second input to AND 3 which:

1. Provides an input to the 4/0 timer which times out to apply a negative input to the Trip AND.
2. Applies a negative input to the AND of the transient unblock circuit to fulfill the requirements to obtain an output from the transient unblock circuit.

As a result, an input is applied to the unblock timer. Twenty-five milliseconds later, the unlock timer will operate to apply a positive voltage to the transient block AND circuit. This resets the 22/0 block timer and removes the input to the AND of the unblock timer to reset the unblock circuit. The required three inputs are thus applied to the trip AND and a trip output is obtained from the relay. Upon operation of the relay, the 0/100 millisecond timer resets the 0-1000 transient block timer.

d. Protective Relay Operation

The phase comparison relay is armed by the distance fault detector through a 6/0 timer on the protective relay board. The operation of the distance fault detectors applies positive potential to the board at either terminal 3, 5, 5 or 7. This turns Q1 on and turns Q2 off to allow C2 to charge. Six milliseconds later the voltage on C2 reaches the breakdown of Zener diode, Z7 and base current flows into transistor Q3 to turn Q3 on. This turns on Q4 to apply a positive potential to terminal 14 of the arming board.

4. Supervision Board

The circuits on the supervision board include the interface to the channel receiver and they vary with the type of equipment used as a pilot channel. In general, though, this board contains a low signal clamp timer.

a. Low Signal Clamp (.5/150 Timer)

1. Tone Channel (See Fig. 37)

With a serviceable channel either a space frequency or an alternate space-mark frequency is received from the channel equipment. With reference to a TA-2 tone channel, Q14 and Q2 of the supervision board of Fig. 16 are either turned off or turned on and off. With Q2 turned off, base current is supplied to transistor Q3 and Q3 conduct. The collector of Q3 is thus at negative potential and capacitor C1 cannot charge.

If the channel is not serviceable, the tone receiver is clamped into a mark condition and the space output is zero. Transistor Q14 conducts and transistor Q2 is turned on. Negative potential is applied to Q3 and stops conducting. Positive potential is then applied to capacitor C1 through resistor R7 and R8. After a 150 millisecond time delay,

capacitor C1 charges sufficiently to break down Zener diode Z1. When Z1 conducts, base drive is supplied to transistor Q3 and Q4 turns on. This connects the collector of Q4 to negative potential which allows base current to flow in transistor Q5 through R11. This turns on transistor Q5 to apply positive voltage to R12. This voltage is then applied to AND 1 and AND 2 of the arming board and to an alarm output. Applying the voltage to the AND circuits blocks tripping.

Under the condition of alternate mark and space outputs from the tone receiver, transistor Q3 is turned on and off every 8.3 milliseconds (half cycle of power system frequency). Every half cycle, capacitor C1 starts to charge but on the next half-cycle Q3 turns on to discharge capacitor C1. Since the charging time is not sufficient to allow capacitor C1 to break down Z1, transistor Q5 will not turn on to block tripping.

2. TCF Carrier Channel (See Fig. 38)

With reference to the supervision board of Fig. 18 for a serviceable TCF channel Q1 and Q2 either alternately turned on and off or Q1 is turned on and Q2 is turned off. Under both conditions, base current is supplied to transistor Q3 and Q3 is turned on at all times. With Q3 turned on, C1 can not charge and Q4 is turned off.

If the channel is not serviceable, the carrier receiver is clamped into both a mark and space output. This turns on transistors Q1 and Q2 and shorts the base of Q3 to negative potential and Q3 turns off. Positive potential is applied to C1 through R12 and R13 and 150 milliseconds later, Zener diode Z5 breaks down to allow base current to flow to Q4. Q4 turns on which provides a path through R16 for base current of Q5 to flow to negative. Q5 turns on to apply positive voltage to R17. This voltage is then applied to AND 1 and AND 2 of the arming board to block tripping. The voltage is also applied to an external alarm circuit.

When this relay is used on either a TA2.2 tone channel or a MC-22 microwave channel, the low signal clamp is not utilized. If these channels are not serviceable, the channel receiver is clamped into neither a mark nor a space output. This instantaneously places a blocking signal on the AND circuits of the SKBU relay. Hence, the relays will not trip on a low signal clamp. The low signal timer is not activated and will not produce an alarm output to the next device. This alarm information is supplied directly to the next device by the channel receivers.

a. **Noise Supervision (Tone Channel Only)**

The noise supervision interface consists of transistors Q17, Q11, Q12 and associated components (See Fig. 16). Under normal conditions, the output from the noise circuit of the tone receiver is zero volts. As a result, transistor Q17 is not conducting and base current is not supplied to transistor Q11. Transistor Q11 is turned off and its collector is held at positive potential to prevent base current from flowing in transistor Q12. Negative voltage (across R31) is applied to AND 1 and AND 2 of the arming board.

Under noise conditions the noise circuit of the tone equipment provides a negative output with respect to positive 48 volts dc. This negative voltage allows transistor Q17 to turn on to provide base current to Q11 through resistor R27. Transistor Q11, turns on, and its collector is connected to negative potential. Base current then flows in transistor Q12 through resistor, R30, and Q12 turns on. Positive potential is applied to resistor, R31 and to terminal 5 and 11 of the supervision board. From terminal 5, the voltage is applied to AND 1 and AND 2 of the arming board to block tripping. The voltage on terminal 11 is applied to an external alarm.

4. **PR INTER Board** (Protective Relay Interface Board) Fig. 20

The protective relay board includes the interface to the protective relays as well as the auxiliary circuits associated with the protective relays. This board contains a 6/0 timer, 2500 sustained arming timer, and a 150/10 signal squelch timer.

a. **Signal Squelch Timer**

When an input is applied to terminal 18 of the protective relay board, positive potential is applied to base of Q10, Q10 turns on to provide a discharge path for C8 through R41. 10 milliseconds after the input to terminal 18, Q11 turns off to turn on Q12. Turning on Q12 applies a negative input to the keying circuit of the amplifier and keying board which keeps the keying transistor from turning on.

Upon removal of the input to terminal 18 of the protective relay board Q10 turns off to apply positive potential to C8. 150 milliseconds later Q11 turns on to turn off Q12 which removes negative potential to the keying circuit.

b. Sustained Arming Alarm (2500 Timer)

When arming occurs, positive potential is applied to terminal 1 and capacitor C3 of the PR INTER Board from terminal 19 of the arming board. Two-and-a-half seconds later, the potential on C3 breaks down the Zener diode Z8 to allow base current to flow into Q5. This turns on Q5 which turns off Q6. Turning Q6 off applies positive potential to the base of Q7 and Q7 turns off. This removes positive potential from R26 and an external alarm is energized.

c. Arming Delay by Distance Fault Detectors (6/0 Timer)

The distance supervision arming is delayed by 6 milliseconds to allow time for the circuits feeding AND 1 and AND 2 to respond at fault inception. Operation of the distance fault detectors will apply positive potential to the protective relay board. This turns on Q1 which removes the base current to transistor Q2. Q2 turns off and positive potential is applied to capacitor C2. Six milliseconds later the voltage on C2 reaches a value to break down Zener diode Z7. This turns on Q3, which connects the base of Q4 to negative through resistor, R15. Q4 turns on to apply positive potential to resistor, R16 and terminal 2. From terminal 2 the voltage is applied to the arming board.

CHARACTERISTICS

A. SKBU-21 Relay

The type SKBU-21 relay is available for frequency shift channels, either tone or carrier. Taps are available to set different sensitivities of the fault detector to zero and negative sequence currents. These taps are as follows:

Negative Sequence Taps (I_2)

TAP SETTING	NEGATIVE SEQUENCE SENSITIVITY
A	None
B	0.4 Amperes
C	0.25 Amperes

Zero Sequence Taps (I_0)

TAP SETTING	ZERO SEQUENCE SENSITIVITY
F	None
G	0.2 Amperes
H	0.1 Amperes

The positive sequence response of the fault detector is greater than 7 amperes.

B. SKBU-2 Relay

Taps are available in the relay to set the sensitivity to different combinations of positive, negative, and zero sequence components of the line current. The T taps on the left hand tap plate indicate the balanced three phase amperes which will operate the fault detector FD. These taps are as follows:

3, 4, 5, 6, 7, 8 and 10.

For distance fault detector applications, the user should reset the SKBU-2 fault detector for a pick-up of twice tap value by means of the S1 setting.

Positive and Negative Sequence Current-R1 Taps

The upper half of the right hand tap plate of R1 taps changes the number of turns on the third winding of the mutual reactor. This reproportions the components of the sequence filter which changes the positive and negative sequence sensitivity of the fault detector. Operation of the fault detector with the various taps is given in the following table:

TABLE I

COMB.	SEQUENCE COMPONENTS IN NETWORK OUTPUT	TAPS ON RIGHT HAND TAP BLOCK		FAULT DETECTOR PICK-UP †	
		R_1	R_0 #	3ϕ FAULT	$\phi\phi$ FAULT
1	Pos., Neg., Zero	C	G or H	Tap Value	86% Tap Value (53% on BC Fault)
2	Pos., Neg., Zero	B	G or H	2 x Tap Value	90% Tap Value (65% on BC Fault)
3	Neg., Zero	A	G or H	–	100% Tap Value

* – Taps F, G and H are zero-sequence taps for adjusting ground fault sensitivity. See section on zero-sequence current tap.

† – When taps A and 3, or B and 3 are used, the fault detector will pickup 10 to 15 percent higher than the above values because of the variation in self-impedance of the sequence network and the saturating transformer.

Zero Sequence Current – R_0 Taps

The lower half of the right-hand tap plate (R_0 taps) is for setting the response of the relay to ground faults. Taps G and H give the approximate ground fault sensitivities listed in Table II. Tap F is used in applications where no response to zero sequence current is required. When this tap is used, the voltage output of the network caused by zero-sequence current is eliminated.

NOTE: Because of inherent characteristics of the sequence network, there will be small variations (from the values listed in Tables I and II) in the pick-up current for various phase or ground fault combinations.

TABLE II

COMB.	R_1 TAP	GROUND FAULT PICK-UP	PERCENT OF T TAP SETTING
		TAP G	TAP H
1	C	25%	12%
2	B	20%	10%
3	A	20%	10%

C. SKBU-2 and SKBU-21 Relay

The operating time of the fault detector of both the SKBU-2 and SKBU-21 is shown in Fig. 25. As shown in the figure, the fault detector has a maximum and minimum value. This is due to the point on the current wave that fault current is applied. Fig. 26 shows the operating times for different points on the fault wave for fault current at five amperes.

The keying response of the SKBU-21 relay is independent of the tap setting. Fig. 27 shows typical lengths of keying pulses with reference to a 60-hertz base of the SKBU-21 relay for different values of positive, negative, and zero sequence current. Fig. 32 shows the response of the SKBU-2.

The keying voltage across X_5-X_6 of the SKBU-21 Relay with reference to phase A positive, negative, and zero sequence currents is given by

$$V = 2.7\ Ia1\ \angle -125^\circ + 11.8 Ia2\ \angle 120^\circ + 31\ Ia0\ \angle 105^\circ$$

This voltage is measured with currents into the odd number terminals. X_5 is polarity terminal. 25 volts is maximum voltage obtainable from X_5-X_6.

The keying voltage across X_5-X_6 of the SKBU-2 relay with reference to phase A positive, negative and zero sequence currents is given by

$$V = K_1 Ia_1 + K_2 Ia_2 + K_0 Ia_0$$

Where values of K_1, K_2, and K_0 are given in the following table

CONSTANT	TAP SETTING	VALUE
K_1	A – F G H	0 0
K_1	B – F G H	$\frac{1.24}{T} \angle -130^\circ$
K_1	C – F G H	$\frac{2.47}{T} \angle -155^\circ$
K_2	A – F G H	$\frac{4.35}{T} \angle 55^\circ$
K_2	B – F G H	$\frac{5.3}{T} \angle 40^\circ$
K_2	C – F G H	$\frac{5.9}{T} \angle 20^\circ$
K_0	A – H	$\frac{73}{T} \angle 50^\circ$
K_0	B – H	$\frac{73}{T} \angle 40^\circ$
K_0	C – H	$\frac{61.5}{T} \angle 25^\circ$
K_0	A – G	$\frac{41}{T} \angle 50^\circ$
K_0	B – G	$\frac{41}{T} \angle 40^\circ$
K_0	C – G	$\frac{34}{T} \angle 20^\circ$
K_0	A,B,C – F	0

This voltage is measured with currents into the odd number terminals. X_5 is polarity terminal.

Typical logic drawing for a tone channel is shown in Fig. 21 and 23 and for a TCF carrier channel in Fig. 22 and 24.

Operating Time . . . . . 15 to 32 Milliseconds
Alarm . . . . . 2.5 seconds for FD operation
150 Milliseconds Loss-of-Channel
Transient Block Time . . . . 22 to 25 Milliseconds
Transient Unblock Time . . . 23 to 27 Milliseconds
Ambient Temperature Range . . . . −20°C to 55°C
DC Drain . . . . . 0.14 Amps at 48 Volts DC
Reset Time of Transient Block
1. After Fault Detector has Operated . . . . . 1000 Milliseconds
2. When unblock time is utilized . . . . . Instantaneous

ENERGY REQUIREMENTS

A. SKBU-21 Relay

Burdens measured at a balanced three-phase current of five amperes. (Independent of tap setting).

PHASE A		PHASE B		PHASE C	
Va	Angle	Va	Angle	Va	Angle
8.3	106°	2.2	50°	46.	0°

Burden measured at a single-phase to neutral current of five amperes.

Relay Taps	PHASE A		PHASE B		PHASE C	
	Va	Angle	Va	Angle	Va	Angle
C-H	11.7	2.1°	9.7	1.8°	44.0	2.2°
B-H	11.4	2.0°	10.3	1.8°	46.0	2.2°
A-H	11.1	2.0°	11.2	1.8°	48.0	2.2°
C-G	8.8	2.0°	7.0	1.8°	42.0	2.2°
B-G	8.7	2.0°	7.5	1.8°	43.5	2.2°
A-G	7.8	2.0°	8.5	1.8°	45.0	2.2°
C-F	6.7	2.0°	7.5	1.8°	42.0	2.2°
B-F	6.5	2.0°	7.2	1.8°	42.0	2.2°
A-F	5.8	2.0°	6.6	1.8°	43.9	2.2°

The angles above are the degrees by which the current lags its respective voltage.

B. SKBU-2 Relay

Burdens measured at a balanced three-phase current of five amperes.

Relay Taps	PHASE A		PHASE B		PHASE C	
	Va	Angle	Va	Angle	Va	Angle
A-F-3	2.4	5°	0.6	0°	2.5	50°
A-H-10	3.25	0°	0.8	100°	1.28	55°
B-F-3	2.3	0°	0.63	0°	2.45	55°
B-H-10	4.95	0°	2.35	90°	0.3	60°
C-F-3	2.32	0°	0.78	0°	2.36	50°
C-H-10	6.35	342°	3.83	80°	1.98	185°

Burdens measured at a single-phase to neutral current of five amperes.

Relay Taps	PHASE A		PHASE B		PHASE C	
	Va	Angle	Va	Angle	Va	Angle
A-F-3	2.47	0°	2.1	10°	1.97	20°
A-H-10	7.3	60°	12.5	53°	6.7	26°
B-F-3	2.45	0°	2.09	15°	2.07	10°
B-H-10	16.8	55°	22.0	50°	12.3	38°
C-F-3	2.49	0°	1.99	15°	2.11	15°
C-H-10	31.2	41°	36.0	38°	23.6	35°

The angles above are the degrees by which the current lags its respective voltage.

Continuous Ratings:

The Continuous Rating of the SKBU-2 relay is 10 amperes and the Continuous Rating of the SKBU-21 is 7 amperes. The two second overload rating or the SKBU-2 is 150 amp. phase and 125 amp. ground while the two second rating of SKBU-21 is 125 amp. phase and ground.

SETTINGS

If settings in between taps are desired, the tap screw should set in the next lowest tap. S_1 should then be adjusted for the desired pickup value. S_2 should then be adjusted to proper dropout ratio.

A. SKBU-21

The SKBU-21 relay has separate tap plates for adjustment of the zero and negative sequence sensitivity of the fault detector. The fault-detector tap markings and pickup are:

Negative Sequence Sensitivity (I_2)

A. None
B. 0.4 Amperes
C. 0.25 Amperes

Zero Sequence Sensitivity (I_0)

F. None
G. 0.2 Amperes
H. 0.1 Amperes

Two tap plates are provided: one for I_2 and the other one for I_0.

Tap A should not be used in service since this would prevent fault detector operation for phase-to-phase faults. However, tap F may be used with either B or C since negative sequence current flows for both phase-to-phase and ground faults.

The recommended settings are tap B or C as needed for the required sensitivity, and tap F. Taps G and H have been provided for applications where the negative-sequence load flow due to series impedance unbalance may be high enough to operate FD with a tap C setting. In this case, set in tap B and in tap G or H. It is not intended that taps C and H be used simultaneously due to the possibility of cancellation of the negative- and zero-sequence effects on ground faults. With a tap B setting, a tap H setting is preferred.

To summarize, the recommended setting combinations in the order of preference are:

COMBINATION	I_2 TAP	I_0 TAP
1	C	F
2	B	F
3	B	H
4	B	G

B. SKBU-2 Relay

The SKBU-2 relay has separate tap plates for adjustment of the phase and ground fault sensitivities and the sequence components included in the network output. The method of determining the correct taps for a given installation is discussed in the following paragraphs.

Setting Principles

Tap C provides the best balance between 3 phase and phase-to-phase fault sensitivity. Always use this tap where distance fault detector supervision is used. Where only the SKBU-2 fault detector is used and where the full load current (maximum through any terminal) is approximately five amperes or more, tap B will provide increased phase-to-phase fault sensitivity with little or no sacrifice in 3 phase fault sensitivity. For example, if a left-hand tap (T) of 6 is needed with tap C (6C), then use a 3 B setting instead.

NOTE: From Table I, pickup will be 105% of Tap 3 on 3B and 90% of Tap 6 for ϕA to ϕB fault. 3ϕ pickup is 6 amp. both settings.

Use tap A only where satisfactory unbalanced fault sensitivity cannot otherwise be obtained and where other protection is available for 3 phase faults. Since with Tap A no 3 phase fault protection is available.

In all cases provide identical response at all stations to insure proper phase comparison and adequate keying for any fault detected by remote-end relays. To accomplish this, the letter taps (A, B, C, F, G, H) should be identical at all stations. Also, the taps should be identical with CT ratios, or inversely proportional to CT ratios where different.

After selecting tap C or B, pick the T tap to allow reset of the fault detector in the presence of load flow. That is, fault detector pick-up should be at least 111 percent of full load current (maximum through any terminal).

Now select tap G or H for desired ground-fault sensitivity.

For distance fault detector applications, set 3C to provide the maximum sequence-filter voltage for the squaring amplifiers. The SKBU-2 current fault detector is then independently desensitized (by adjustment of S1 and S2 settings) to permit reset in the presence of full-load current. Phase faults which do not operate the SKBU-2 fault detector will be detected by the supplementary distance fault detectors.

EXAMPLE SKBU-2:

Assume a two-terminal line with current transformers rated 400/5 at both terminals. Also assume that full load current is 300 amperes, and that on minimum internal phase-to-phase faults 2000 amperes is fed in from one end and 600 amperes from the other end. Further assume that on minimum internal ground faults, 400 amperes is fed in from one end, and 100 amperes from the other end. No distance fault detectors are employed.

POSITIVE-SEQUENCE CURRENT TAP

Secondary Values:

$$\text{Load Current} = 300 \times \frac{5}{400} = 3.75 \text{ amperes} \quad (1)$$

Minimum Phase-to-Phase Fault Currents:

$$600 \times \frac{5}{400} = 7.5 \text{ amperes} \quad (2)$$

Fault detector setting (three phase) must be at least:

$$\frac{3.75}{0.9} = 4.18 \text{ amperes (0.9 is dropout ratio of fault detector. Setting will insure that the fault detector will reset on load current.)} \quad (3)$$

In order to complete the trip circuit on a 7.5 ampere phase-to-phase fault, the fault detector pick-up from Table I must not be more than:
(based on a three phase fault)

$$7.5 \times \frac{1}{0.86} = 8.7 \text{ amperes} \quad (4)$$

ZERO SEQUENCE TAP

Secondary Value:

$100 \times \frac{5}{400} = 1.25$ amperes minimum ground fault current

With T, tap 6 and R1 Tap B in use, the fault detector pick-up currents for ground faults (See Table II) are as follows:

Tap G 0.2 x 6 = 1.2 amperes

Tap H 0.1 x 6 = 0.6 amperes

From the above, tap H would be used to trip for a minimum ground fault of 1.25 amperes.

SEQUENCE COMBINATION TAP

From a comparison of (3) and (4) above it is evident that the fault detector can be set to trip under minimum phase fault conditions and yet not operate under maximum load. From (3) we can select tap 5 (T). In this. case, also select tap C (R_1). Current tap (6) would be used in preference to tap 5 to allow for occurrence of higher load current. However, if more margin is desired over load current, instead of setting 6C, use 3B for improved phase-to-phase fault sensitivity.

INSTALLATION

The phase comparison relay is generally supplied in a cabinet or on a relay rack as part of a complete assembly. The location must be free from dust, excessive humidity, vibration, corrosive fumes, or heat. The maximum temperature around the chassis must not exceed 55°C.

ADJUSTMENTS AND MAINTENANCE

NOTE: The phase comparison relay is normally supplied as part of a relaying system, and its calibration should be checked after the system has been installed and interconnected. Details are given in the instructions of the assembly. The assembly instructions and not the following instruction should be followed when the relay is received as an integral part of the relaying system.

In those cases where the relay is not part of a relaying system, the following procedure will verify that the circuits of the relay are functioning properly.

TEST EQUIPMENT

1. Oscilloscope
2. AC Current Source
3. Electronic Timer
4. AC Voltmeter
5. DC Voltmeter

ACCEPTANCE TEST

Connect the relay to the test circuit of Fig. 28 which represents the tone channel for test purposes. Fig. 29 represents the TCF carrier channel for test purposes. Connect 2, 4, 6 and 8 together on terminal block.

If a test fixture is not available, the remote pulses can be obtained from the SKBU keying circuit. This is accomplished by jumpering various circuits of the relay together as follows: (NOTE: These instructions apply where no external connections are made to the J1 block.)

1. Apply 48 volts dc to J1-2 (pos. and J1-5 (neg.). An alternate connection is to X1 and X4.
2. Jumper J1-26 to J1-27. (This replaces the external squelch test switch.)
3. Connect terminal 9 of supervision board to X14. (This connects space interface circuit to keying circuit.) As an alternate connection, J1-7 can be connected to J1-25.
4. Connect one pole of a DPST switch across TP-1 and TP-2 of amplifier and keying board. This is switch L of the tests. External fault position is with the switch open. Internal fault position is with the switch closed.
5. On the SKBU for TCF channel, connect terminal 13 to terminal 10 on the supervision board.

   (This connects mark interface to output of space interface.)

6. On the SKBU for a TA-2 tone channel:

a. Connect terminal 10 and TP-1 of supervision board through a diode-resistor network to negative. (Connect TP-1 through the forward direction of a second diode to the junction of the first diode and resistor.)

b. Connect J1-3 to positive 48 volts dc.

With the jumpers added as per the above information, the transistor circuits are connected together as shown in Figure 33.

If the above connections are utilized to test the relay, the reference to closing switches A, B, C, D, E, F, G, H and I of the following test procedure should be ignored.

The following tests are with reference to the relay as received. If a recalibration of the circuits is desired, the recalibration can best be obtained by setting S1, S2 and S5 to counterclockwise limit, S6 and S7 to clockwise limit, and R27 on output board to the middle of its range.

1. FD Pickup and Dropout

a. Set relay on taps C and H. Set SKBU-2 T tap 5.

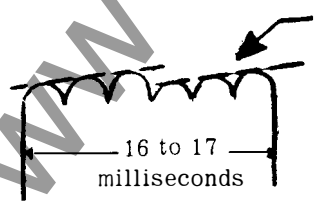
b. Connect a high resistance dc voltmeter across X_{22} and X_4 (neg.).

c. Apply 60 hertz current to terminal 1 and 3 of the relay. Gradually increase the current until the voltmeter changes reading from approximately zero volts to approximately 20 volts. This is the operating current of FD and should be 0.433±5% amperes for SKBU-21 relay and 4.33 ± 5% amperes for SKBU-2 relay.

d. Gradually lower ac test current until the dc voltmeter drops to approximately zero volts. This is the dropout current of FD and should occur at .389 to .395 amperes for SKBU-21 and 3.89 to 3.95 amperes for SKBU-2.

e. Adjustment of pickup and dropout is made by S_1, and S_2 respectively.

f. If the output of the fault detector is erratic at pickup, R53 on the fault detector should be adjusted such that the following waveform should appear across X_{21} to X_4.



peaks should be nearly equal or, if not, rising slightly to the right.

2. Check of Local Squaring Amplifiers

a. With all switches of test circuit open, apply 0.6 to 0.8 amperes ac to terminals 1 and 3 of the SKBU-21 relay, or 6 to 8 amperes ac to terminals 1 and 5 of the SKBU-2 relay.

b. Place scope probe across X12 and X4 (grd). A square wave of voltage should appear across X12 and X4 as shown in Fig. 30.

c. Place scope probe across X15 and X4 (grd). A square wave of voltage should appear across X15 and X4 as shown in Fig. 30.

d. If scope has two traces, connect one probe to X12 and second probe to X15. Connect grd. of scope to X4. The phase relationship of Fig. 30 should be observed.

3. Check of Keying Circuit

a. With all switches of test circuit open except A and 0.6 to 0.8 amperes ac applied to terminal 1 and 3 of the SKBU-21 relay, with scope check voltage across X14 and X4 (grd). (This voltage should be checked with 6 to 8 amperes into terminals 1 and 3 of SKBU-2 relay.)

b. Waveform shown in Fig. 30 should be observed.

4. Check of Remote Squaring Amplifiers

a. Close switches A, B and C of test fixture.

b. Apply 0.6 to 0.8 amperes ac to terminals 1 and 3 of the SKBU-21 relay, or 6 to 8 amperes ac to same terminals for SKBU-2 relay.

c. Using scope with grd. lead on X4, check waveshape of voltage across X9 and then X16. Waveforms of Fig. 30 should be observed. Also for three terminal application check waveform across X13 and X17.

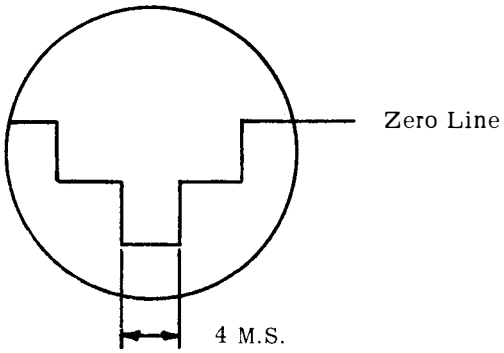
d. If scope has two traces, connect one probe to X9 and the other on X16. Connect grd. to X4. The phase relationship to Fig. 30 should be observed.

5. Setting of S6 (4/0 Timer)

a. With S5 set to minimum resistance (fully counter clockwise) and S6 to maximum resistance (fully clockwise) set switch L to external fault and close switches A, B and C, E and F. Open switch I. Apply 0.6 to 0.8 amperes ac to terminals 1 and 3 of the SKBU-21 relay or 6 to 8 amperes ac to same terminals of SKBU-2 relay.

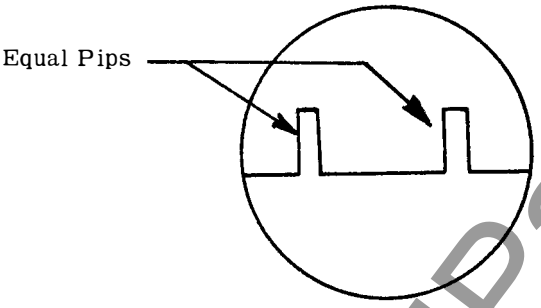
b. Place scope probe across X10 and X4 (grd).

Connect a second scope probe to X11. Adjust S5 until following waveform appears on scope.



c. Adjust S6 until the relay trips as indicated in a change in voltage on X11.

* d. Change S5 to obtain the following waveform. This will be with S5 at minimum resistance.

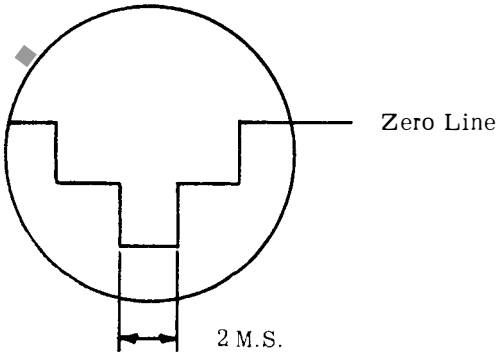


e. Close and open switch H, and slowly turn S5 until the relay operates. Waveform should be same as step b. If necessary, readjust S6 and repeat d and c.

* **6. Setting of S7 (Transient Unblock)**

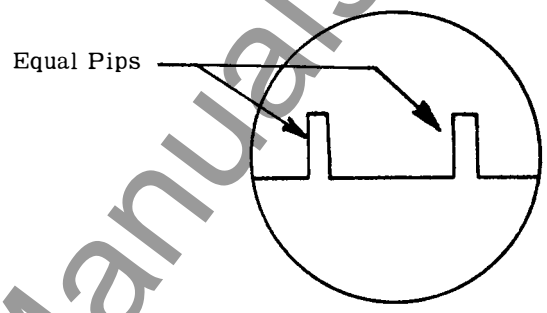
a. With S5 set to minimum resistance (fully counter clockwise) and S7 to maximum resistance (fully clockwise) set switch L to external fault and close switches A, B and C, E and F. Open switch I. Apply 0.6 to 0.8 amperes ac to terminals 1 and 3 of the SKBU-21 relay or 6 to 8 amperes ac to same terminals of SKBU-2 relay.

b. Place scope probe across X10 and X4 (grd). Connect a second probe to X7. Adjust S5 until following waveform appears on scope.



Slowly turn S7 until a voltage begins to show on X7. NOTE: This voltage is NOT a sudden charge but a small pulse of voltage that charges back to zero volts.

c. Change S5 to obtain the following waveform. This will be with S5 at minimum resistance. (NOTE: This will not be true if the relay is connected in a system.)



If relay is connected in a system, pips will change when remote terminal is adjusted. Readjust bottom terminals such that the pips remain equal.

7. Transient Blocking Delay (22/0 and 0/1000 Timer)

a. Connect electronic timer stop to X7 and X4 (grd). Set timer stop on negative going pulse. Relay not to be energized with ac current.

b. Connect timer start to X3. Set timer start to positive going pulse.

c. Close PR1 switch. (Represents 20 volts input to terminal 7 of PR board.) Timer should start and should stop between 22 and 25 milliseconds. If necessary, adjust R27 on output board to obtain timing.

d. Set timer start on a negative pulse and timer stop on a positive pulse.

e. Open PR1 switch. Timer should start and should stop after a time delay of 980 to 1020 milliseconds.

8. 6/0 Timer Distance Fault Detector

a. Connect timer start to timer start of PR1 switch. Set timer start on positive pulse. Connect timer stop to X3 and X4 (comm). Set timer stop on positive pulse.

b. Close PR1 switch (Represents 20 volts input to terminal 7 of PR board.) Timer should start and should stop after 6 to 8 milliseconds.

9. Sustained Arming Alarm

a. With electronic timer stop connected to X20 X20 and X4 (grd), set timer stop on negative going pulse.

b. Connect timer start to X3. Set timer start on positive pulse.

c. Close PR1 switch. (Represents 20 volts input to terminal 7 of PR board.) Timer will start and should stop after 2.2 to 2.8 seconds.

d. Open PR1 switch.

10. Recheck steps 5, 6 and 7. Readjust S6, R27 and S7 if necessary.

11. **Fast Reset Timer (0/100)**

a. Connect jumper from TP4 to terminal 4 on output board.

b. Connect start timer to X11. Set timer start on positive pulse. Connect timer stop to TP6 and terminal 8 (neg.) of output board. Set timer stop on positive pulse.

c. Apply 0.6 to 0.8 amperes ac into terminal 1 and out terminal 3 of SKBU-21 relay. (Apply 6 to 8 amperes ac to terminals 1 and 3 of SKBU-2 relay.) (Switches A, B, C, E, F closed, H and I open. Switch L on external fault position.)

d. Close switch L to internal fault position. Relay should trip and timer should start and stop in less than 2.5 milliseconds.

e. Set timer start on negative pulse and timer stop on negative pulse.

f. Close switch L to external fault position and de-energize relay. Timer should start and stop after 80 to 120 milliseconds.

g. Open all switches on test fixture, set L on external fault. Remove jumper from TP4 to terminal 4.

12. **150 Timer Low Signal Clamp 1 (TCF Channel Only)**

a. Connect timer stop to X19 and X4 (comm). Set timer stop to positive pulse.

b. Set switch L to internal fault position.

c. Connect timer start to timer start of switch L. Set timer start to positive pulse.

d. Close switches B, C and G. Close switch L to external fault position. Timer will start and should stop in 130 to 170 milliseconds.

e. Open switches B, C and G. Set L on internal fault position.

13. **150 Timer Low Signal Clamp 2 (TCF Channel Only)**

a. Connect timer stop to X19 and X4 (comm). Set timer stop to positive pulse.

b. Set switch L to internal fault position.

c. Connect timer start to timer start of switch L. Set timer start to positive pulse.

d. Close switches E, F and G. Close switch L to internal fault position. Timer will start and should stop in 130 to 170 milliseconds.

e. Open switches E, F and G and set L to internal fault position.

14. **150 Timer Low Signal Clamp 1 (TA-2 Tone Only)**

a. Connect timer stop to X19 and X4 (comm). Set timer stop to positive pulse.

b. Set switch L to internal fault position.

c. Connect timer start to timer start of switch L. Set timer start to negative pulse.

d. Close switches B and C. Close switch L to external fault position. Timer will start and should stop in 130 to 170 milliseconds.

e. Open switches B and C. Set L on internal fault position.

15. **150 Timer Low Signal Clamp 2 (TA-2 Tone Only)**

a. Connect timer stop X19 and X4 (comm). Set timer stop to positive pulse.

b. Set switch L to internal fault position.

c. Connect timer start to timer start of switch L. Set timer start to negative pulse.

d. Close switches E and F. Close switch L to external fault position. Timer will start and should stop in 130 to 170 milliseconds.

e. Open switches E and F and set switch L on internal fault position.

16. **Signal Squelch Time (10/150)**

a. Connect timer stop to X14 and X4 (comm). Set timer stop on negative pulse. Close switch A. Connect a jumper from TP1 to terminal 8 of the amplifier and keying board. This turns off Q2 to turn on Q3.

b. Connect timer start to pilot trip switch. Set timer start on positive pulse. Close switch I.

c. Close pilot trip switch. (Represent 20 volt input to terminal 14 of PR board.) Timer will start and will stop after an 8 to 12 millisecond delay.

d. Set timer stop on negative pulse, and timer start to negative pulse.

e. Open pilot trip switch. Timer should start and stop after a time delay of 125 to 185 milliseconds.

f. Remove jumper from TP to terminal 8.

17. Check of Noise Circuit (Where Used)

a. Connect dc voltmeter to X18 and X4 (grd). Voltage must read zero.

b. Close switch D. (Connects terminal 7 of supervision board to negative for TA-2 tone channel, and represents a 20 volt input to terminal 7 of supervision board for TA-2.1 tone channel. Switch D can be connected to +20 volts instead of −12 volts.) Voltage must rise to 20 volts. Open switch D. Voltage must change to zero volts. Close switch G. Voltage must rise to 20 volts. Open switch G.

18. Check of Frequency Verifier

a. Open all switches of test circuit.

b. Connect scope across TP60 and terminal 8 of the FD board.

c. Apply 0.5 amperes to terminal 1 and 3 of SKBU-21 relay. (Apply 5 amperes to terminal 1 and 3 on SKBU-2 relay).

d. Waveform of Fig. 31 should be observed.

TROUBLE SHOOTING PROCEDURE

To trouble shoot the equipment, the logic diagram voltage of Table III (Fig. 30) should be used to isolate the circuit that is not performing correctly. The schematic of the individual board, and the voltages of Table IV should then be used to isolate the faulty component.

RENEWAL PARTS

Repair work can be done most satisfactorily at the factory. However, interchangeable parts can be furnished to the customers who are equipped for doing the repair work. When ordering parts, always give the complete nameplate data. For components mounted on the printed circuit board, give circuit symbol and the electrical value (ohms, mfd., etc.) and component style number.

TABLE IV

VOLTAGE MEASUREMENTS ON PRINTED CIRCUIT BOARDS

1. Fault Detector Board Style 5312D13G01

Test Point	I_{ac} = 0	I_{ac} = Pickup of FD	Test Point	I_{ac} = 0	I_{ac} = Pickup of FD
54	6.5 V. DC	less than 1	Term. 5-6	0	14.5 volts ac (Approx.)
55	less than 1	4.5 V. DC	TP 57	18 volts)	
56	less than 1	18 to 22 V.DC	TP 58	18 volts)	
Term.2	less than 1	8.6 V. DC	TP 59	less than 1)	Pulses see Fig. 31 for Waveform
51-52	0	7.4 volts ac (Approx.)	TP 60	20 volts)	
52-53	0	7.5 volts ac (Approx.)	TP 61	18 volts)	
53-51	0	7.4 volts ac (Approx.)	TP 62	less than 1)	

2. Supervision Board, 202C564G01, TA-2 Tones

TEST POINT	NORMAL CONDITION	ABNORMAL CONDITION	TEST POINT	NORMAL CONDITION	ABNORMAL CONDITION
TP1	*48 V. DC	less than 1 with loss of channel 1	Term. 17	**less than 1	16 V. with loss of channel 2
Term. 13	*less than 1	16 V. with loss of channel 1	TP5	*less than 1	48 V. with loss of channel 2
TP2	*less than 1	48 V. with loss of channel 1	Term. 16	*13.5 V DC	less than 1 with loss of channel 2
Term. 12	*13.5 V. DC	less than 1 with loss of channel 1	TP 6	*less than 1	7 V. with loss of channel 2
TP 3	*less than 1	7 V. with loss of channel 1	Term. 19	less than 1	20 V. with loss of channel 2
Term. 18	less than 1	20 V. with loss of channel 1	TP7	less than 1	48 V. with noise clamp
Term. 15	less than 1	20 V. with loss of channel 1	Term. 5	less than 1	20 V. with noise clamp
TP4	**48 V. DC	less than 1 with loss of channel 2	Term. 11	less than 1	20 V. with noise clamp

*Normal condition could be square wave pulses.

**Normal condition could be square wave pulses. On two terminal line application normal condition of TP4 — less than 1 and term 17 — 16 volt dc.

3. Supervision Board, 202C565G01, TCF Channel

TEST POINT	NORMAL CONDITION	ABNORMAL CONDITION	TEST POINT	NORMAL CONDITION	ABNORMAL CONDITION
Term. 13	*less than 1	less than 1 with loss of channel 1	Term. 17	**less than 1	less than 1 with loss of channel 2
Term. 12	*13.5 volts dc	less than 1 with loss of channel 1	Term. 16	*13.5 volts DC	less than 1 with loss of channel 2
TP1	*less than 1	7 V. DC with loss of channel 1	TP 2	*less than 1	7 V. DC with loss of channel 2
Term. 18	less than 1	20 V. DC with loss of channel 1	Term. 19	less than 1	20 V. DC with loss of channel 2
Term. 15	less than 1	20 V. DC with loss of channel 1			

*Normal condition could be square wave pulses.

**Normal condition could be square wave pulses. On two terminal line applications normal condition of terminal 17 is 13.5 volts dc.

TABLE IV (Con't.)

VOLTAGE MEASUREMENTS ON PRINTED CIRCUIT BOARDS

TEST POINT	NORMAL (I_{AC} = 0)	ABNORMAL ON I_{AC} = PICKUP OF FD
4. Amplifier and Keying Style, 202C551G01 for TA-2 Tones and Style 202C540G01 for TCF		
TP1	4.5 volts	4.5 volt pulses at FD pickup
TP2	less than 1	5.5 volt pulses at FD pickup less than 1 with squelch
Term.6 (TA-2 Tones)	48 volts	-12 volt pulses at FD pickup 48 V DC with squelch
Term.6 (TCF Carrier)	less than 1	20 volt pulses at FD pickup less than 1 with squelch
TP4	4.5 volts	4.5 volt pulses at FD pickup
Term.9	20 volts	20 volt pulses at FD pickup
Term.11	less than 1 or 20 volt pulses	20 volts with loss of TA-2 channel 1 less than 1 with loss of TCF channel 1
Term.1	less than 1 or 16 volt pulses TA-2, 13.5 volt pulses TCF	16 volts with loss of TA-2 channel 1
Term.12	**less than 1 or 20 volt pulses	20 volts loss of TA-2 channel 2 less than 1 with loss of TCF channel 2
Term.16	**less than 1 or 16 volt pulses TA-2, 13.5 volts TCF	16 volts with loss of TA-2 channel 2 less than 1 with loss of TCF channel 2
TP9	4.5 volts	4.5 volt pulses at FD pickup
Term.17	20 volts	20 volt pulses at FD pickup
Term.14	20 volts or 20 volt pulses	less than 1 with loss of channel 1
Term.15	13.5 volts or 13.5 volt pulses	less than 1 with loss of channel 1
Term.10	**20 volts or 20 volt pulses	less than 1 with loss of channel 2
Term.13	**13.5 volts or 13.5 volt pulses	less than 1 with loss of channel 2
5. Arming Board Style 202C509G01		
TP1	less than 1	10 volt pulses on internal fault *less than 1 on external fault less than 1 on loss of channel
TP2	less than 1	10 volt pulses on internal fault *less than 1 on external fault less than 1 on loss of channel
TP3	10 volts	*less than 1 on internal fault *10 volts on external fault 10 volts on loss of channel
TP4	13.5 volts	less than 1 at FD pickup
TP5	less than 1	13.5 volts at FD pickup
Term.15	less than 1	20 volts at FD pickup
TP8	20 volts	*less than 1 on internal faults *20 volts on external fault 20 volts on loss of channel
6. Output Board Style 202C548G01		
TP1	16	less than 1 when armed
TP2	less than 1	20 volts when armed
TP3	20 volts	less than 1 when armed
TP4	less than 1	20 volts when armed
TP5		less than 1 at trip
TP6	20 volts	less than 1 when armed
TP7	less than 1	Applies to sequential fault and is a pulse of short duration
TP8	less than 1	7 volts 22 milliseconds after arming
TP9	18.5	7 volts at trip
Term.13	less than 1	20 volts at trip

*Very narrow pulses would be observed on scope

**Values for three terminal line applications. On two terminal line applications – Term 12 and 10 are zero volts, Term. 16 volts TA-2 Tones, 13.5 volts TCF and Term. 13 13.5 volts dc for TA-2 tones and TCF.

ELECTRICAL PARTS LIST (Cont'd.)

Circuit Symbol	Description	Westinghouse Style Number
Protective Relay Board Style 202C563G01		
	Capacitors	
C1-C5-C7	0.047 Mfd.	849A437H04
C2	0.47 Mfd.	188A669H01
C3	68 Mfd.	187A508H02
C4-C6	0.27 Mfd.	188A669H05
C8	6.8 Mfd.	184A661H10
	Diodes	
D1 to D8	1N645A	837A692H03
	Transistors	
Q1-Q2-Q3-Q5-Q6-Q8-Q10-Q11-Q12	2N3417	848A851H02
Q4-Q7-Q9	2N3645	849A441H01
	Resistors	
R1-R2-R3-R4-R5-R27-R28-R30-R36 R37	4.7 K Ohm	629A531H48
R6-R16-R26-R31 R35-R38	82 K Ohm	629A531H78
R8-R15-R25-R34-R40-R44	6.8 K Ohm	629A531H52
R7-R9-R10-R14-R20-R21-R23-R24-R32-R33-R39-R41-R43-R46	10 K Ohm	629A531H56
R11-R22-R45	27 K Ohm	629A531H66
R12-R18	470 Ohm	629A531H24
°R29 (48 Vdc)	22 K Ohm	629A531H64
°R29 (125 Vdc)	68 K Ohm	187A643H71
R42	33 K Ohm	629A531H68
	Zener Diodes	
Z1 to Z5-Z10 to Z13-Z16	1N3686B, 20 V	185A212H06
Z6-Z7-Z8-Z14-Z17-Z18	1N957B, 6.8 V	186A797H06
Z9-Z15	1N3688A	862A288H01
Output Board Style 202C548G01		
	Capacitors	
C1	0.047 Mfd.	849A437H04
C2	22 Mfd.	184A661H16
ΛC3	3.3 Mfd.	867A530H01
C4-C12	1.5 Mfd.	187A508H09
C5-C7-C10	0.22 Mfd.	763A219H21
C6	4.7 Mfd.	184A661H12
C8-C9	500 Mmfd.	187A694H03
C11	0.1 Mfd.	188A669H03
	Diodes	
D1 to D11	1N645A	837A692H03

Circuit Symbol	Description	Westinghouse Style Number
Output Board Style 202C548G01 (Cont'd.)		
	Transistors	
Q1-Q2-Q3-Q5-Q6-Q8-Q9-Q13	2N3417	848A851H02
Q4-Q7-Q10-Q11-Q12-Q14	2N3645	849A441H01
	Resistors	
R1-R2-R32-R40-R43	4.7 K Ohm	629A531H48
R3-R48	82 K Ohm	629A531H78
R4-R7-R8-R9-R15-R17-R19-R26-R31-R34-R36-R37-R38-R41-R45-R46	10 K Ohm	629A531H56
R5-R10-R18-R22-R42-R47	6.8 K Ohm	629A531H52
R6-R24-R25	27 K Ohm	629A531H66
R11-R13	1 K Ohm	629A531H32
R12	100 Ohm	629A531H08
R14-R16-R50	15 K Ohm	629A531H60
R20	220 K Ohm	187A641H83
R21-R33-R35-R39 R44	22 K Ohm	629A531H64
R23	47 Ohm	187A290H17
R27 (Pot)	15 K Ohm	629A430H08
R28-R29	470 Ohm	629A531H24
R30	470 K Ohm	184A763H91
R49	150 Ohm, 3 Watts	762A679H01
	Zener Diodes	
Z1	1N3686B, 20 V	185A212H06
Z2-Z4-Z5-Z6-Z7	1N957B, 6.8 V	186A797H06
Z3-Z8	1N3688A, 24 V	862A288H01
Relay Board Style 5312D80G01 – SKBU-2 5312D78G01 – SKBU-21		
	Capacitors	
C201-C202-C203	0.25 Mfd.	187A624H02
	Resistors	
R201	50 Ohms, 5W	185A209H06
* R202-R203 (SKBU-21)	3.3 K Ohms	629A531H44
* R202-R203 (SKBU-2)	2.2 K Ohms	187A641H35
	Filter Choke	
L201	8.5 H , 450 Ohms	188A460H01
	Zener Diodes	
Z201 (SKUB-21 only)	1N1828C, 43 V	629A798H14

ΛC3 – 2.2 MFD. on some board.

° – Breaker Failure Inputs.

* Typical Value

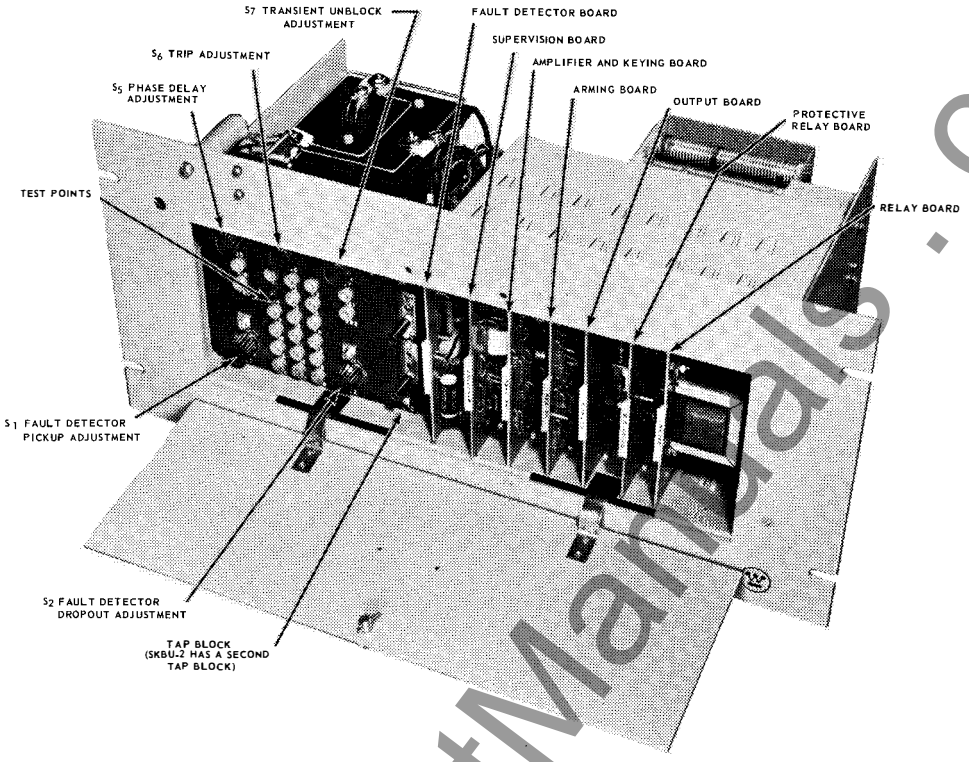


Fig. 1. Photograph (Front View).

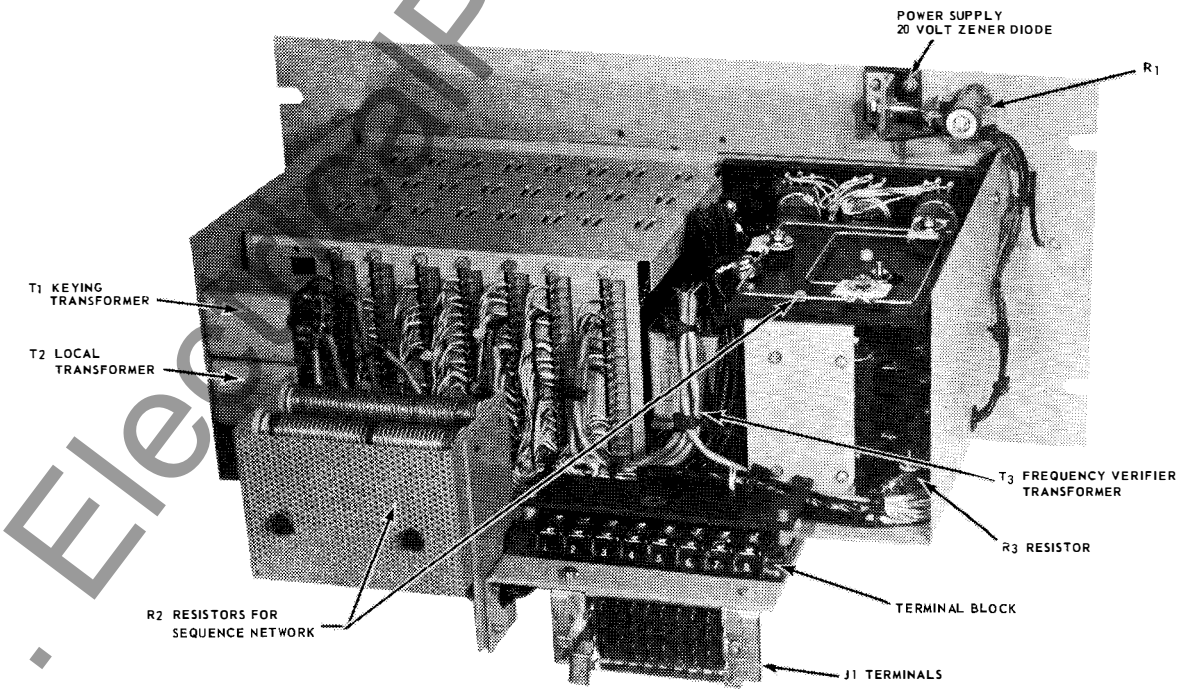


Fig. 2. Photograph (Rear View).

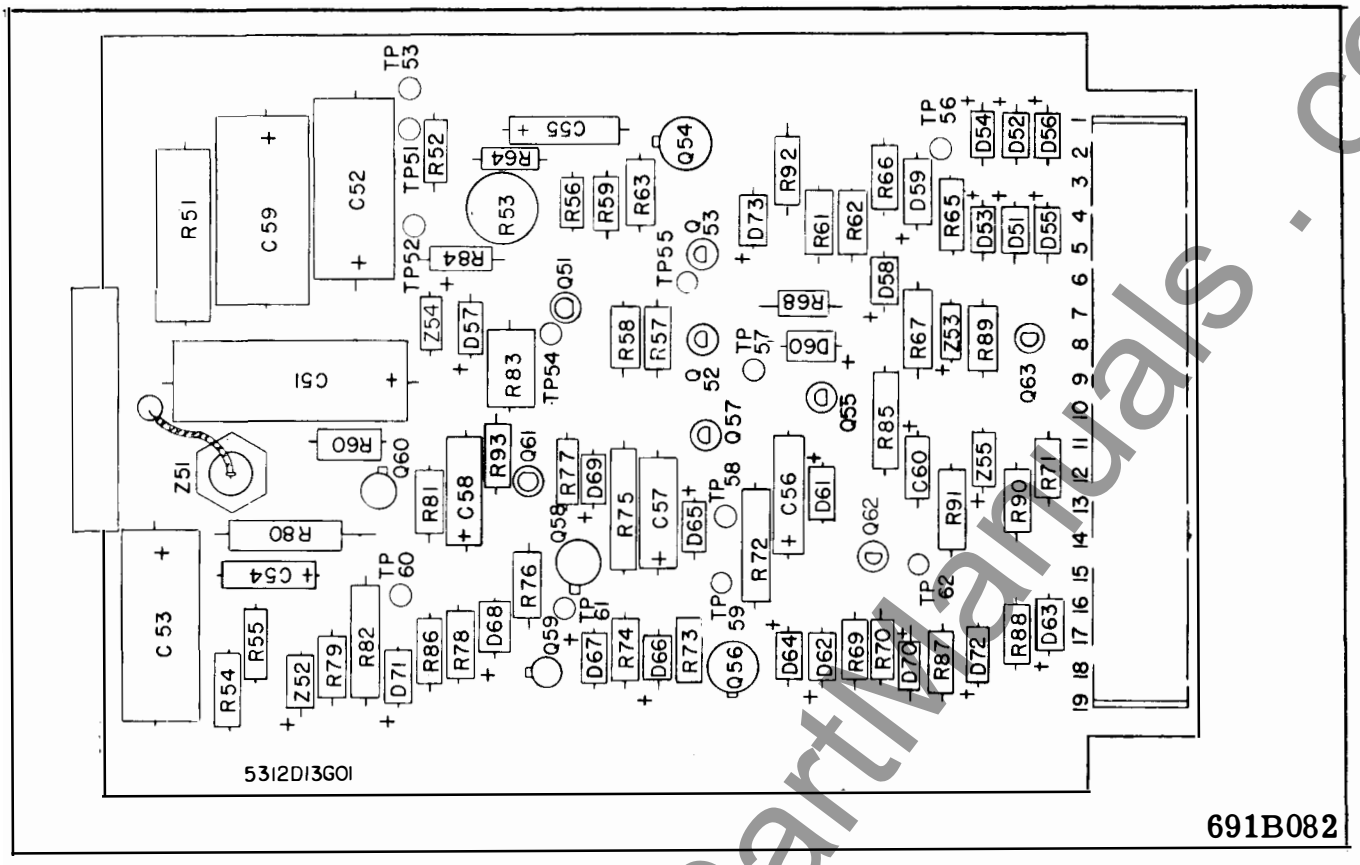


Fig. 3. Location of Components on Fault Detector Board.

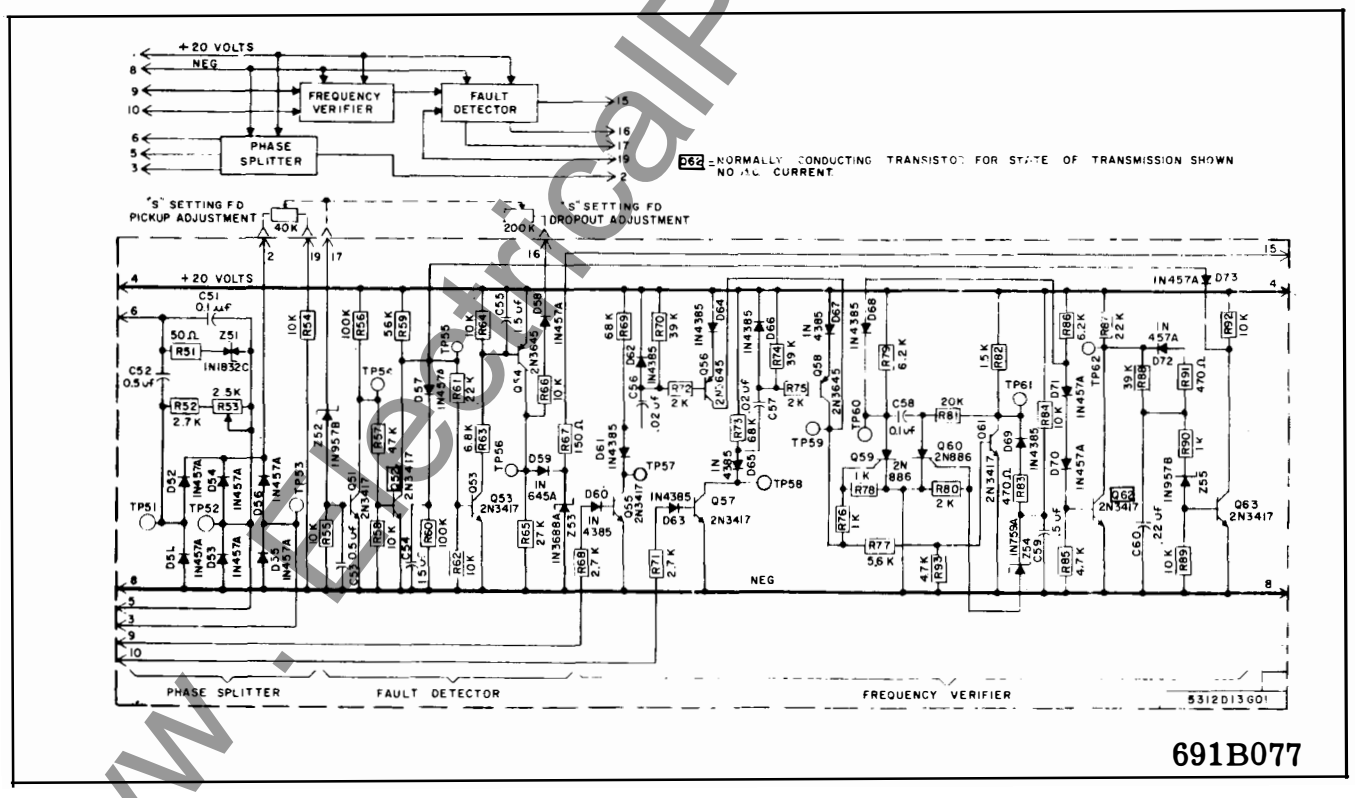


Fig. 4. Schematic of Fault Detector Board.

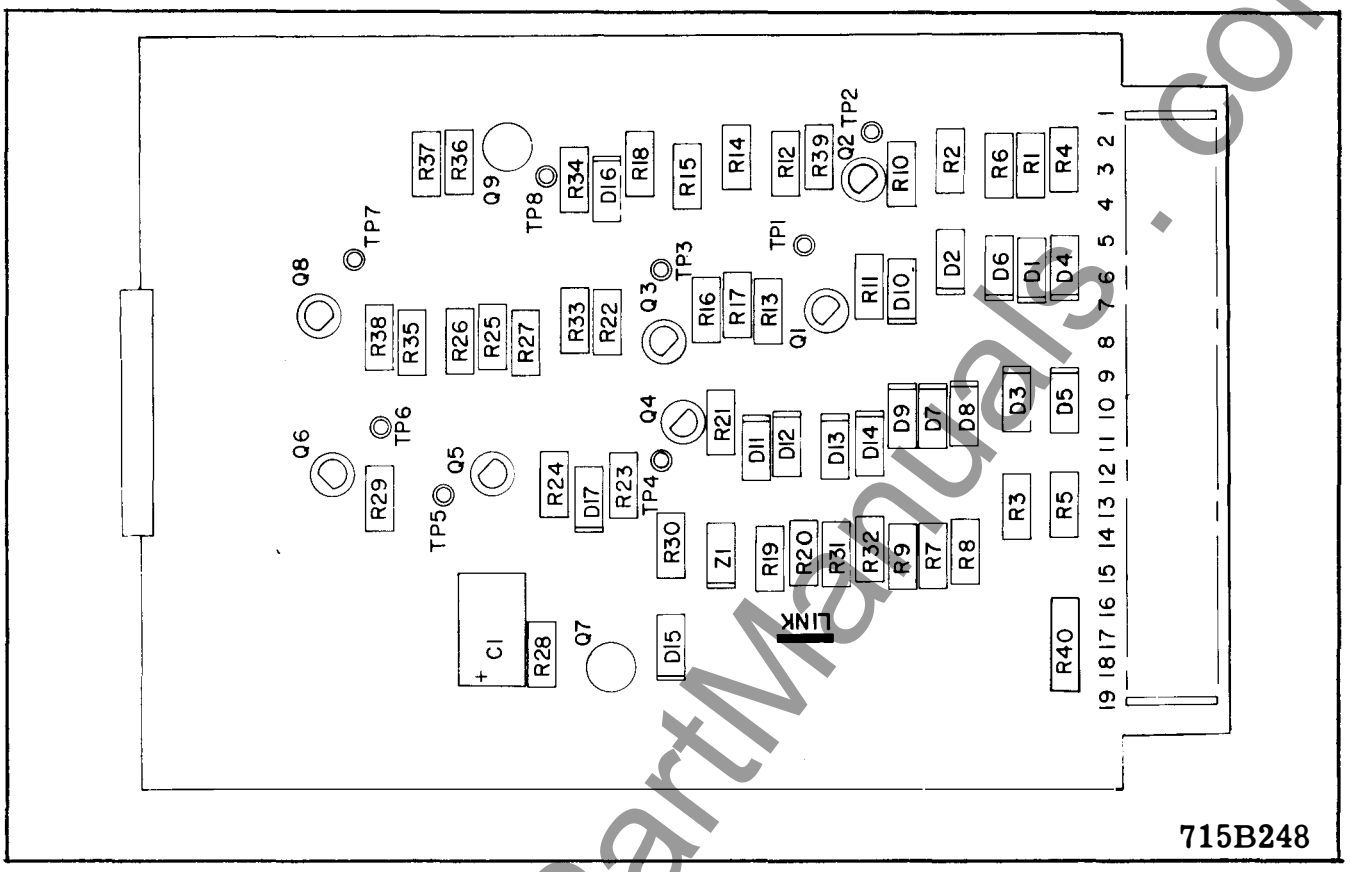


Fig. 5. Location of Components on Arming Board.

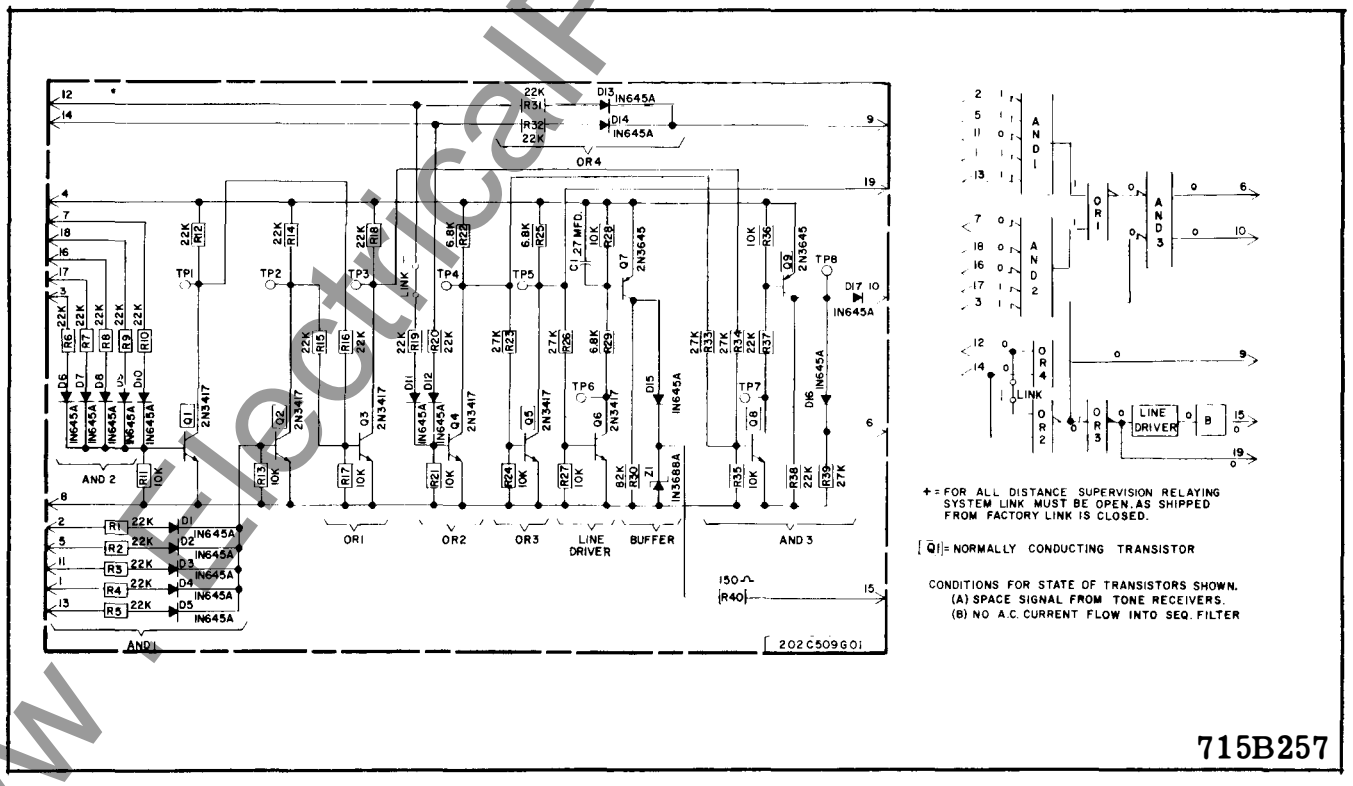


Fig. 6. Schematic of Arming Board.

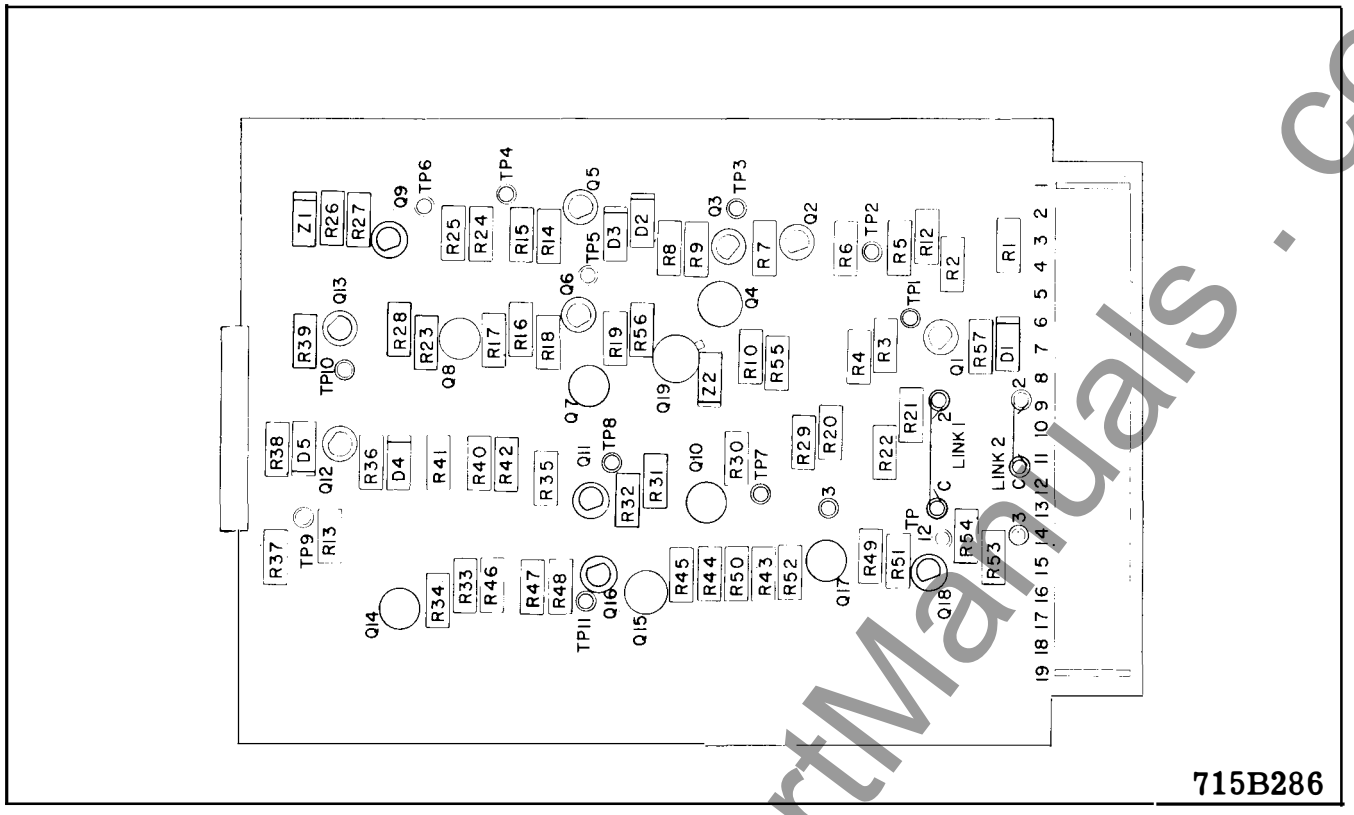


Fig. 7. Location of Components on Amplifier and Keying Board for TA-2 Tone Channel.

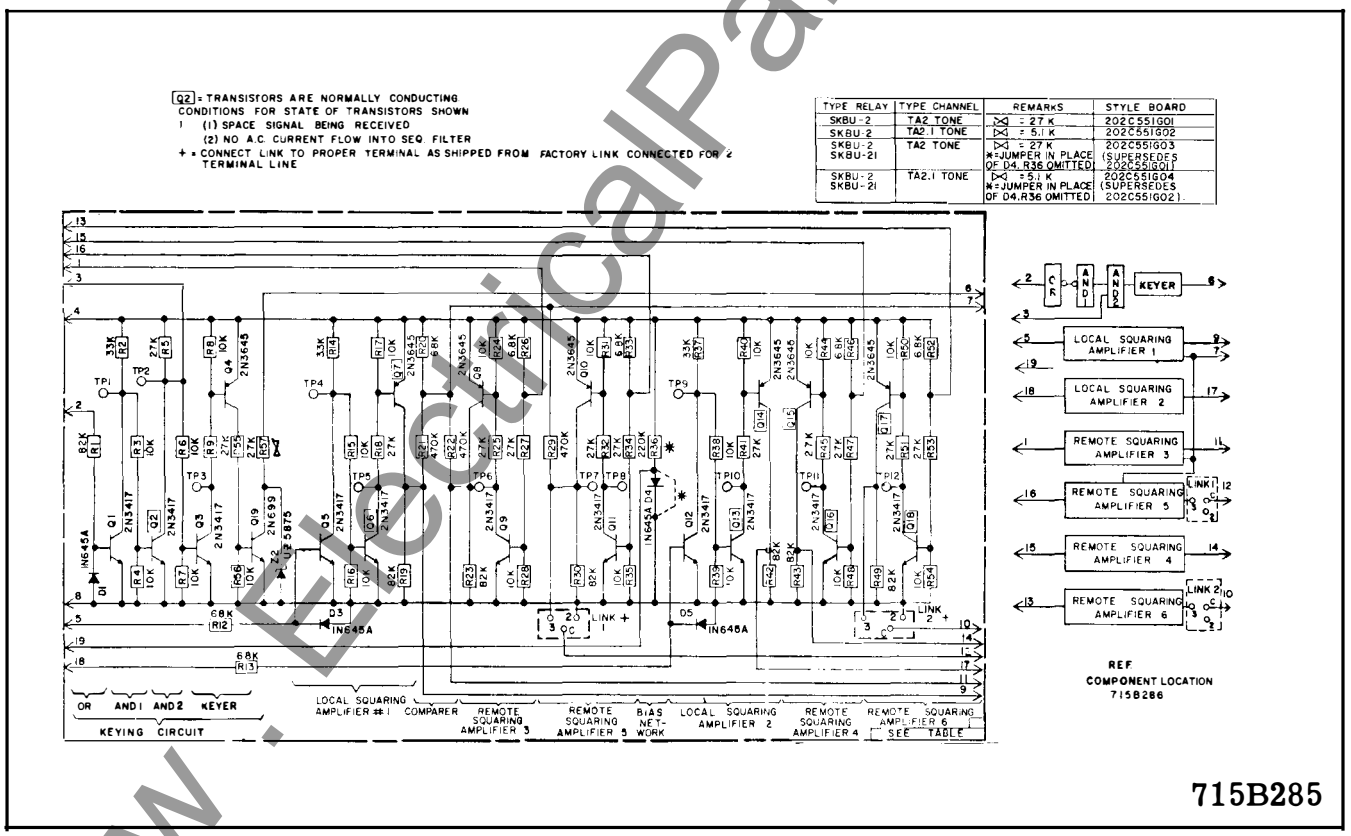


Fig. 8. Schematic of Amplifier and Keying Board for TA-2 Tone Channel.

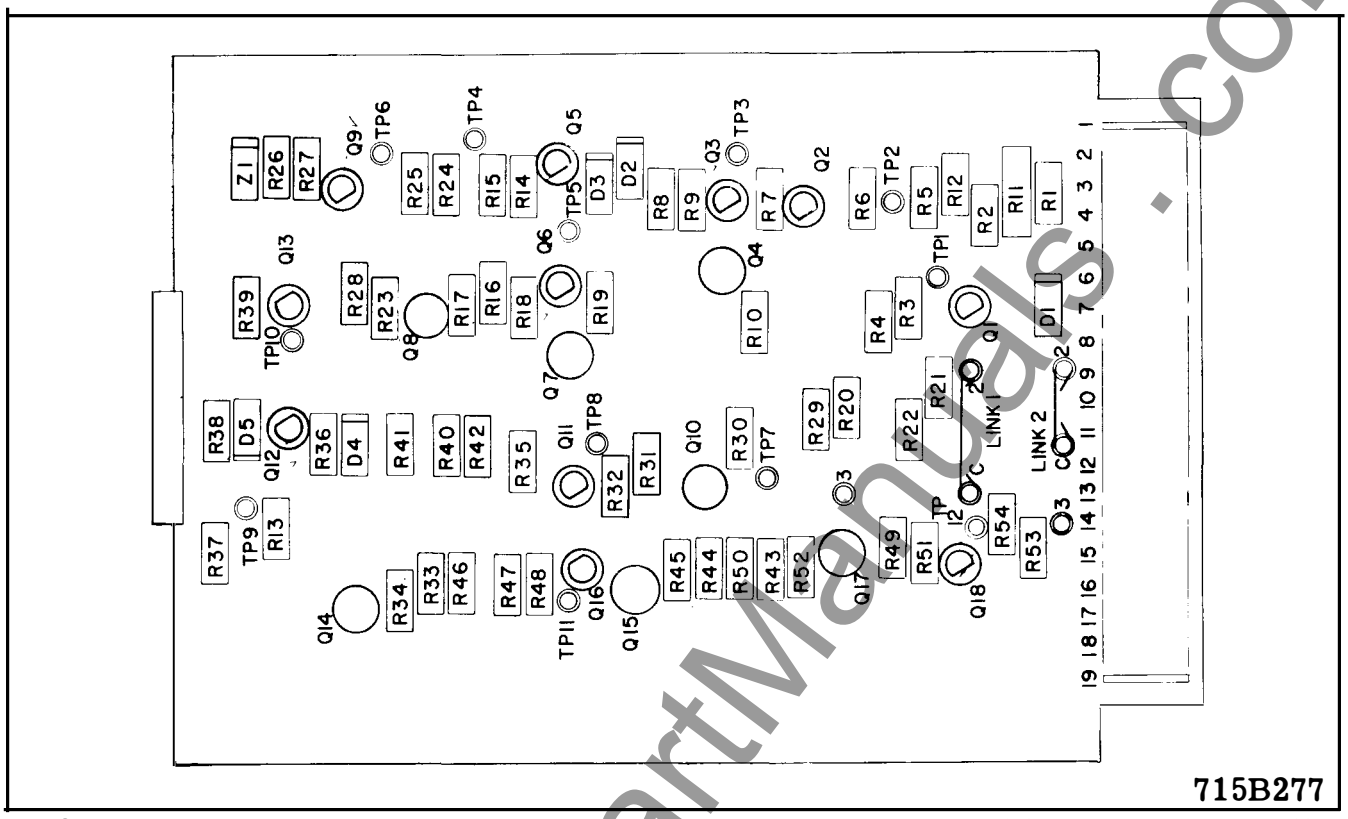


Fig. 9. Location of Components on Amplifier and Keying Board for TCF Carrier Channel, TA2.2 Tone Channel, and MC-22 Microwave Channel.

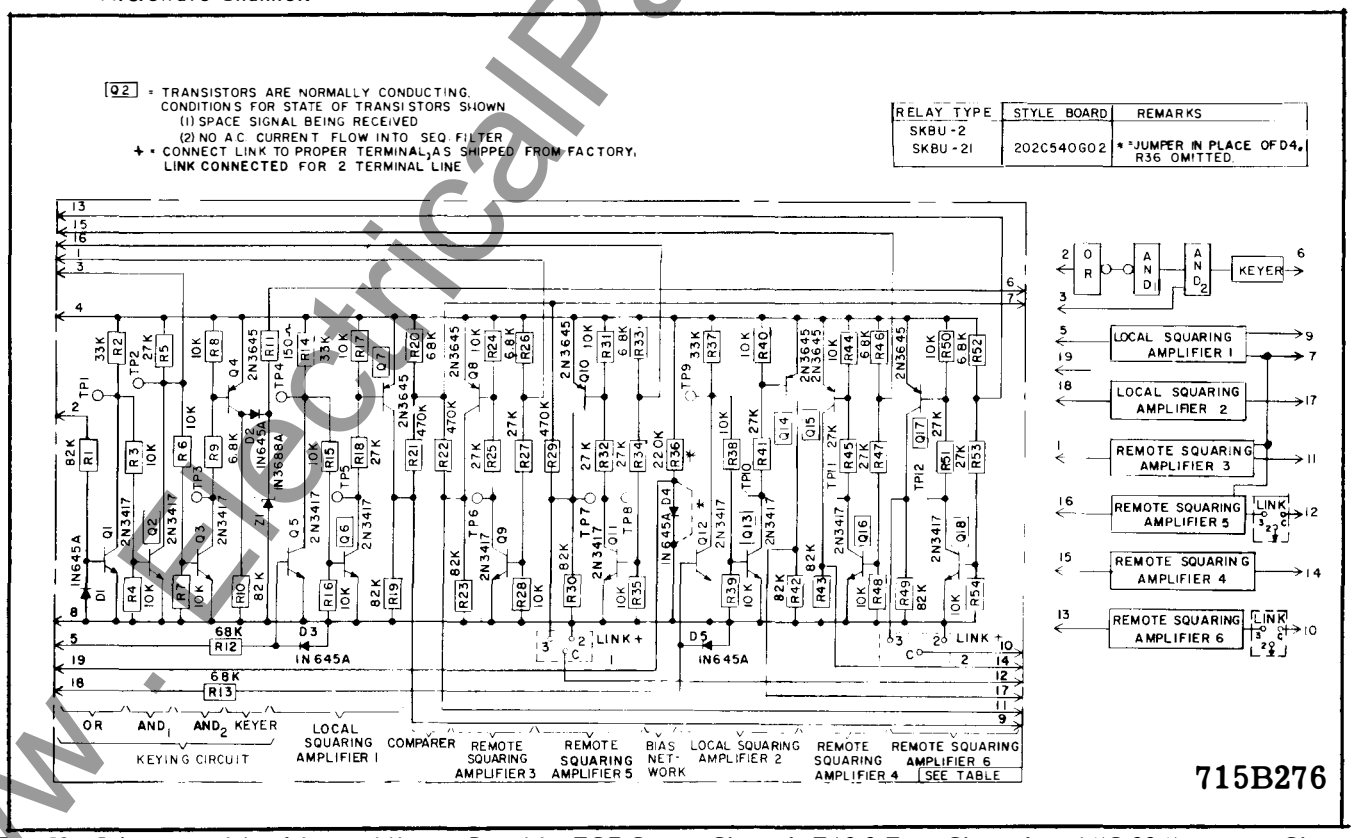


Fig. 10. Schematic of Amplifier and Keying Board for TCF Carrier Channel, TA2.2 Tone Channel, and MC-22 Microwave Channel.

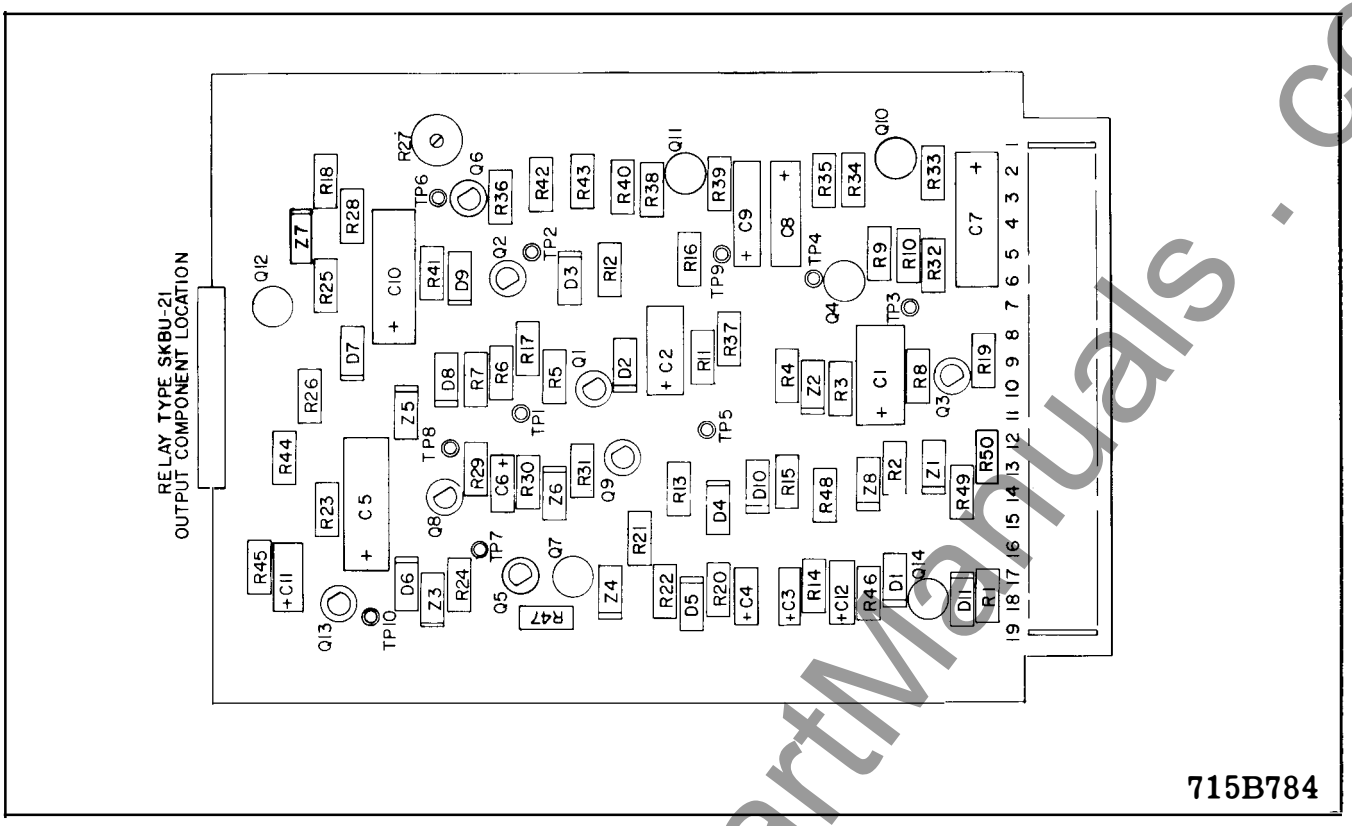


Fig. 11. Location of Components on Output Board.

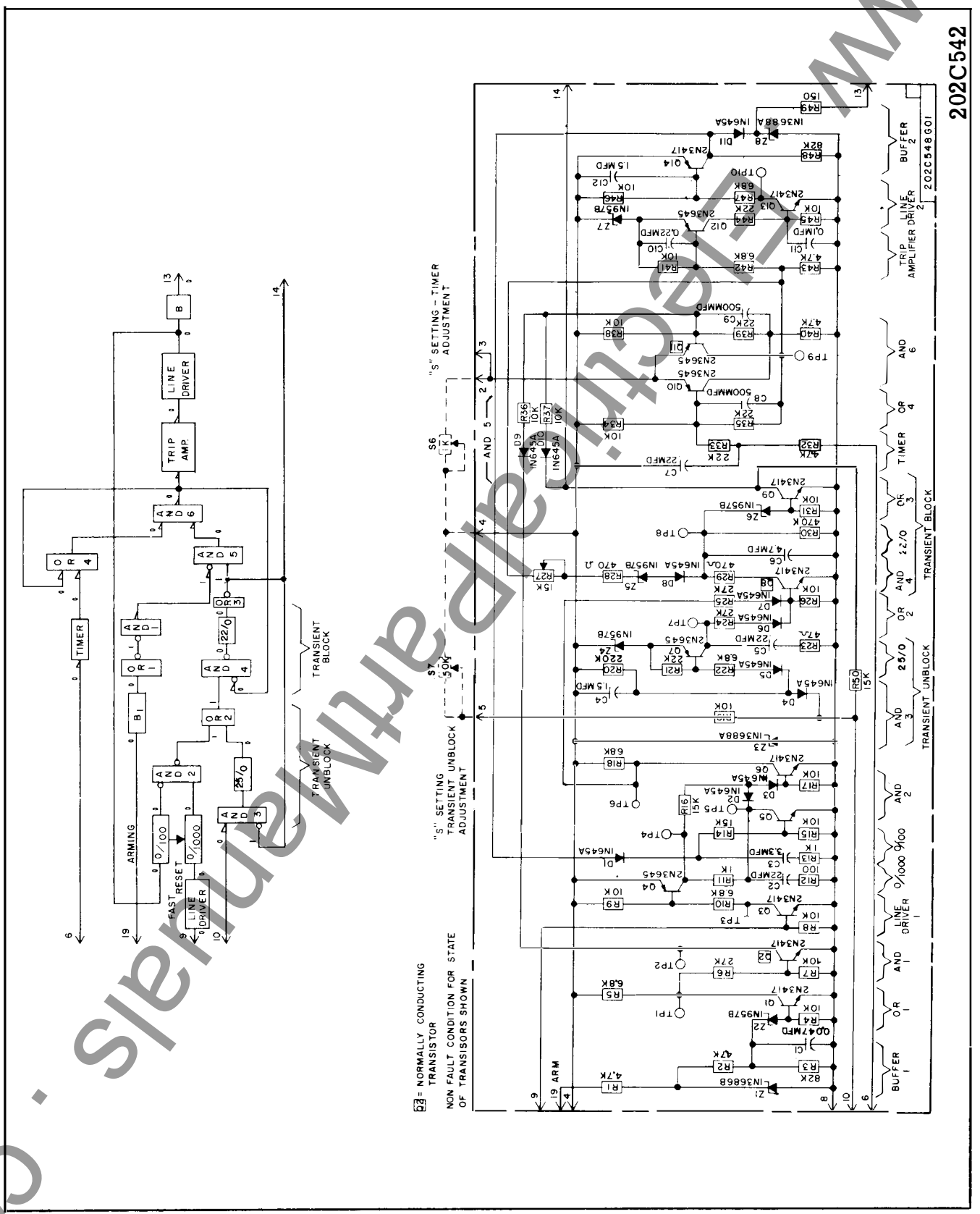


Fig. 12. Schematic of Output Board.

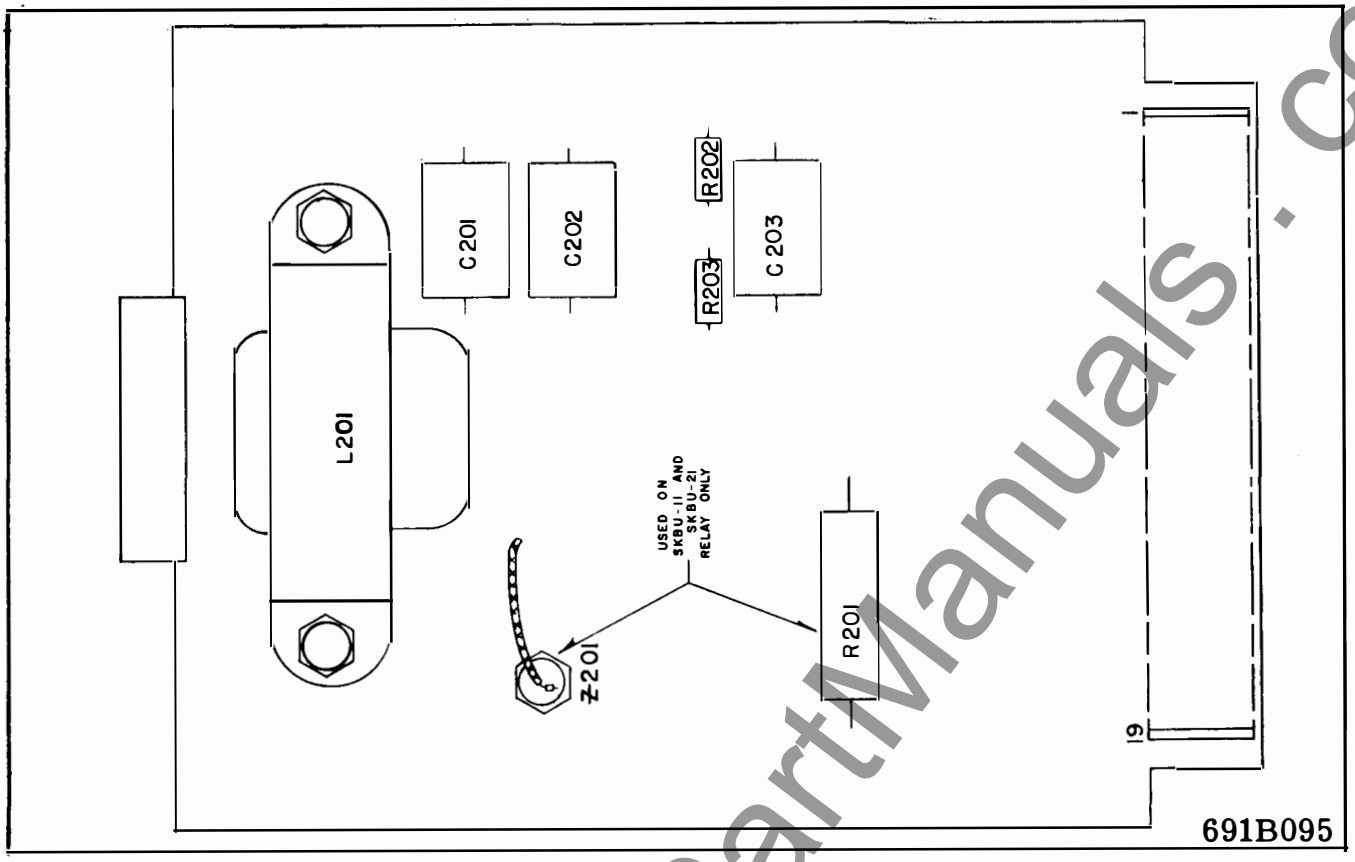
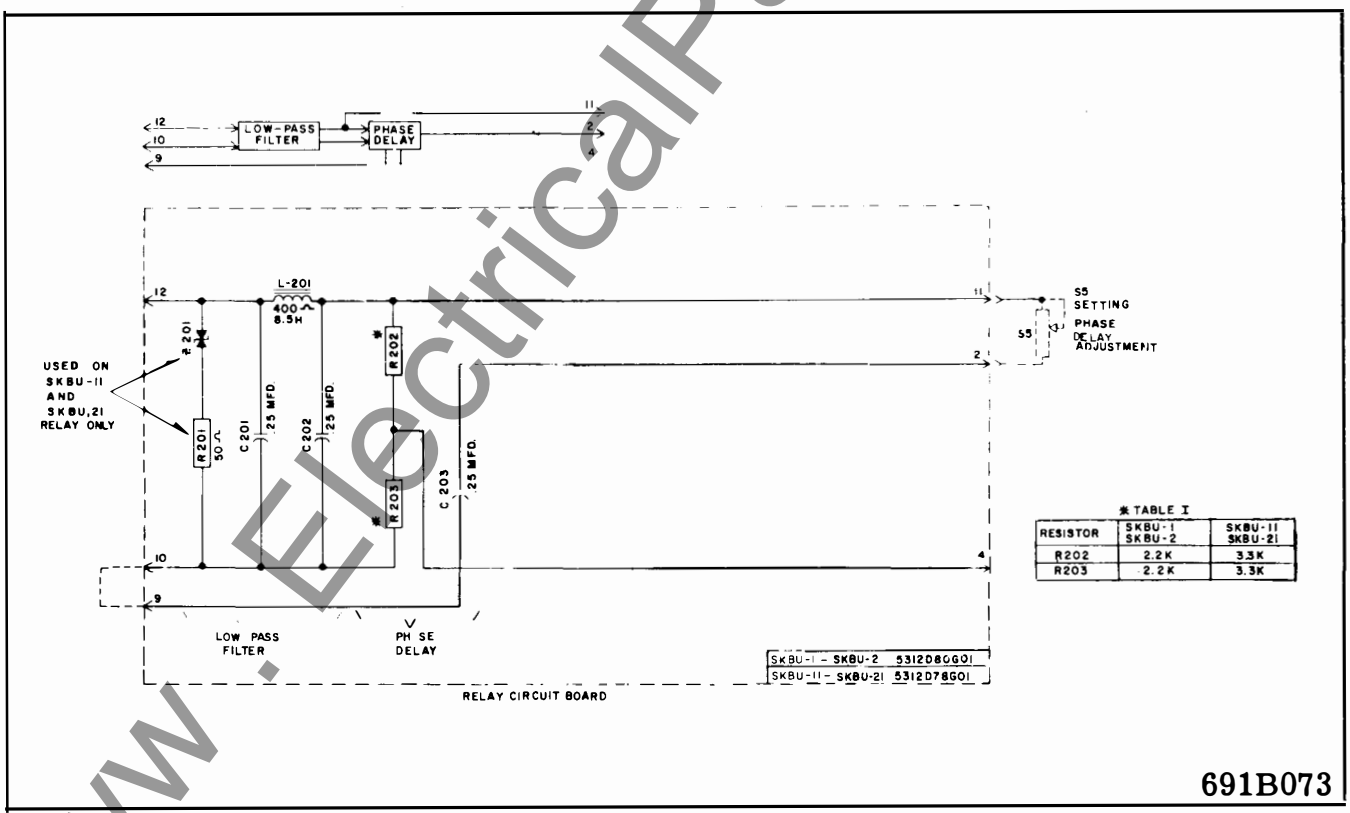


Fig. 13. Location of Components on Relay Board.



* TABLE I

RESISTOR	SKBU-1 SKBU-2	SKBU-11 SKBU-21
R202	2.2K	3.3K
R203	2.2K	3.3K

Fig. 14. Schematic of Relay Board.

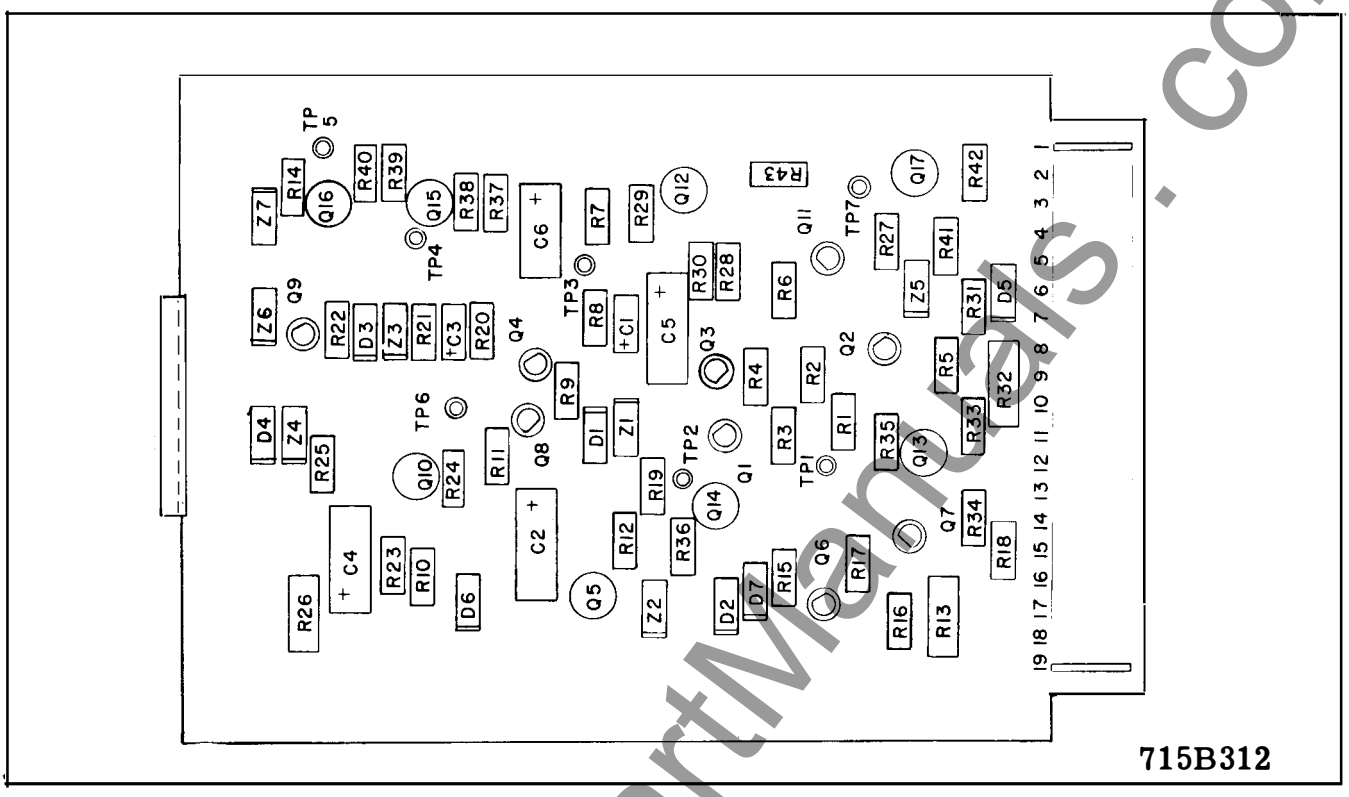


Fig. 15. Location of Components on Supervision Board for TA-2 Tone Channel.

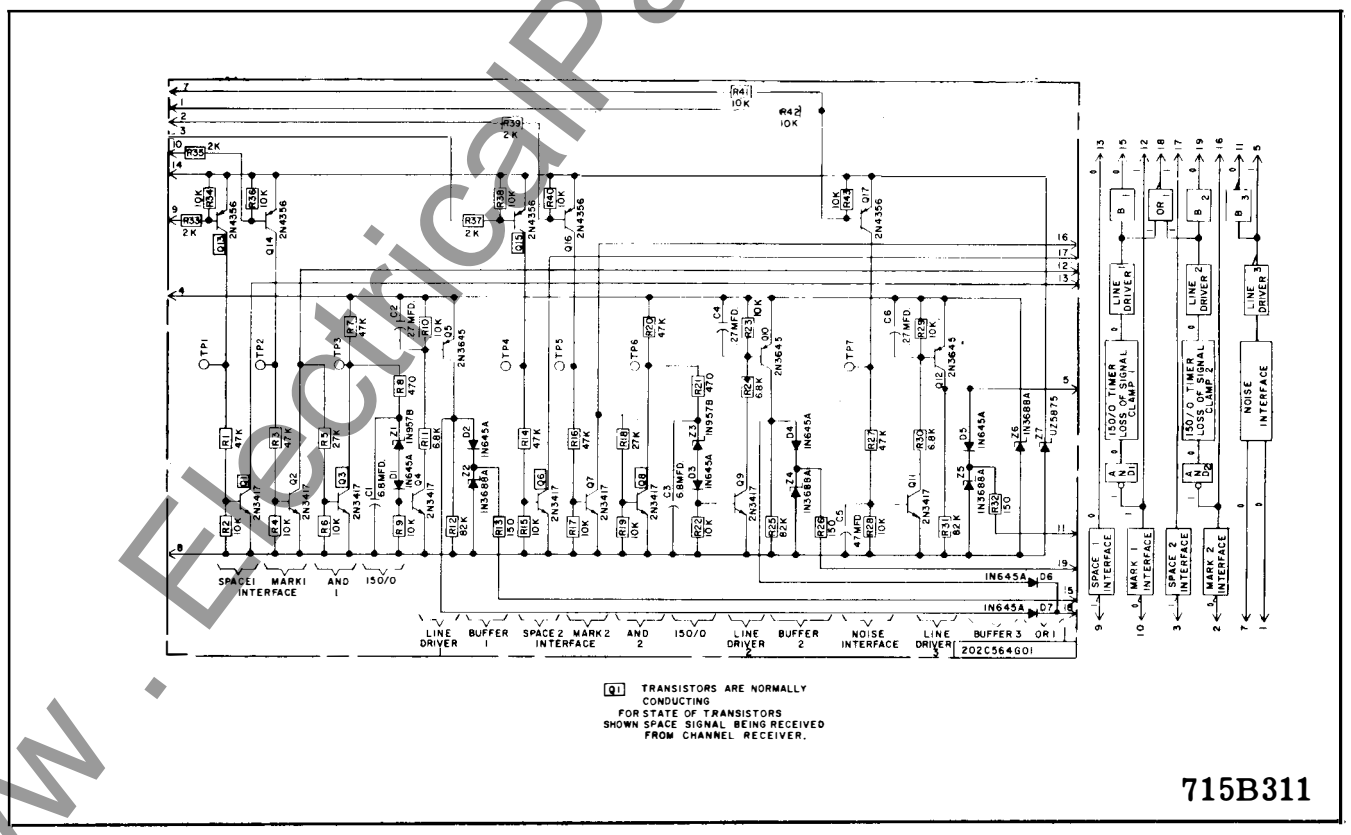


Fig. 16. Schematic of Supervision Board for TA-2 Tone Channel.

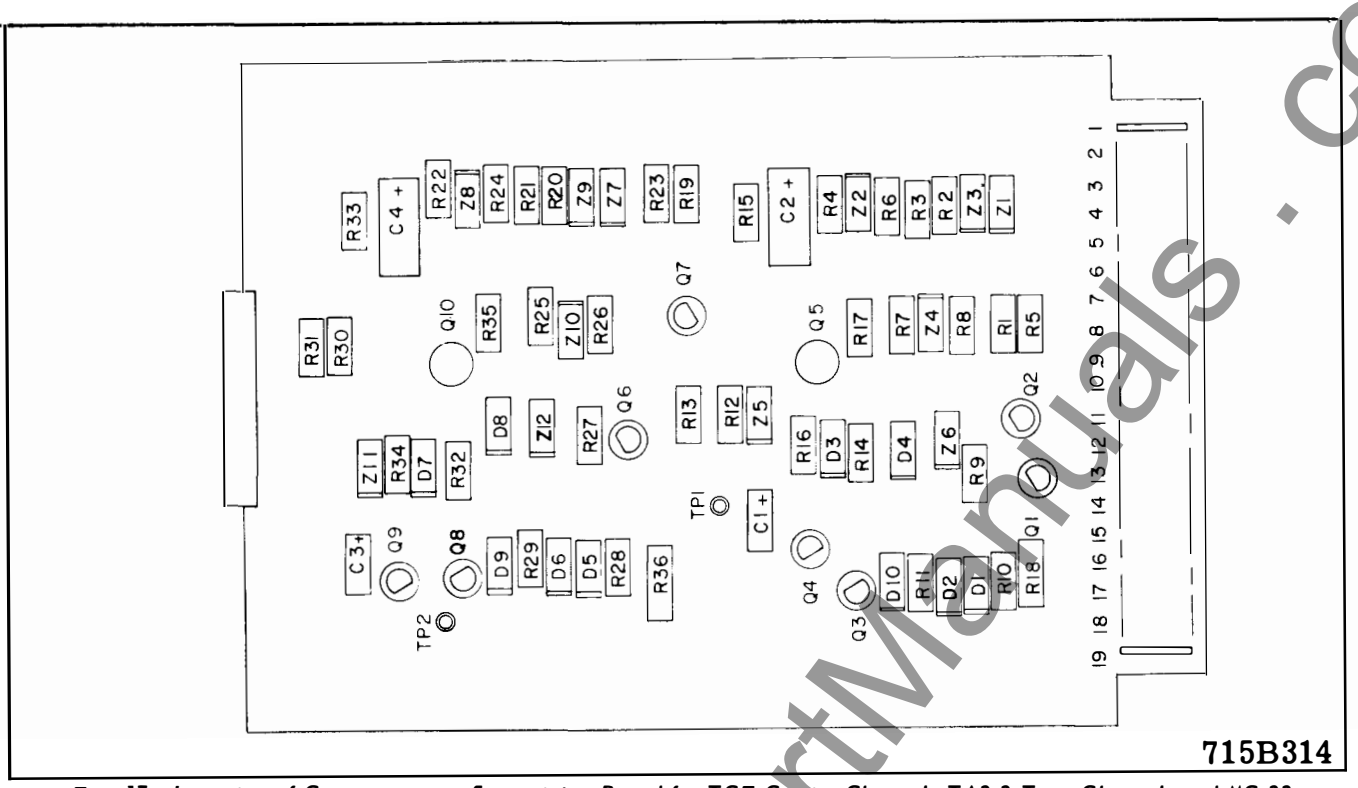


Fig. 17. Location of Components on Supervision Board for TCF Carrier Channel, TA2.2 Tone Channel, and MC-22 Microwave Channel.

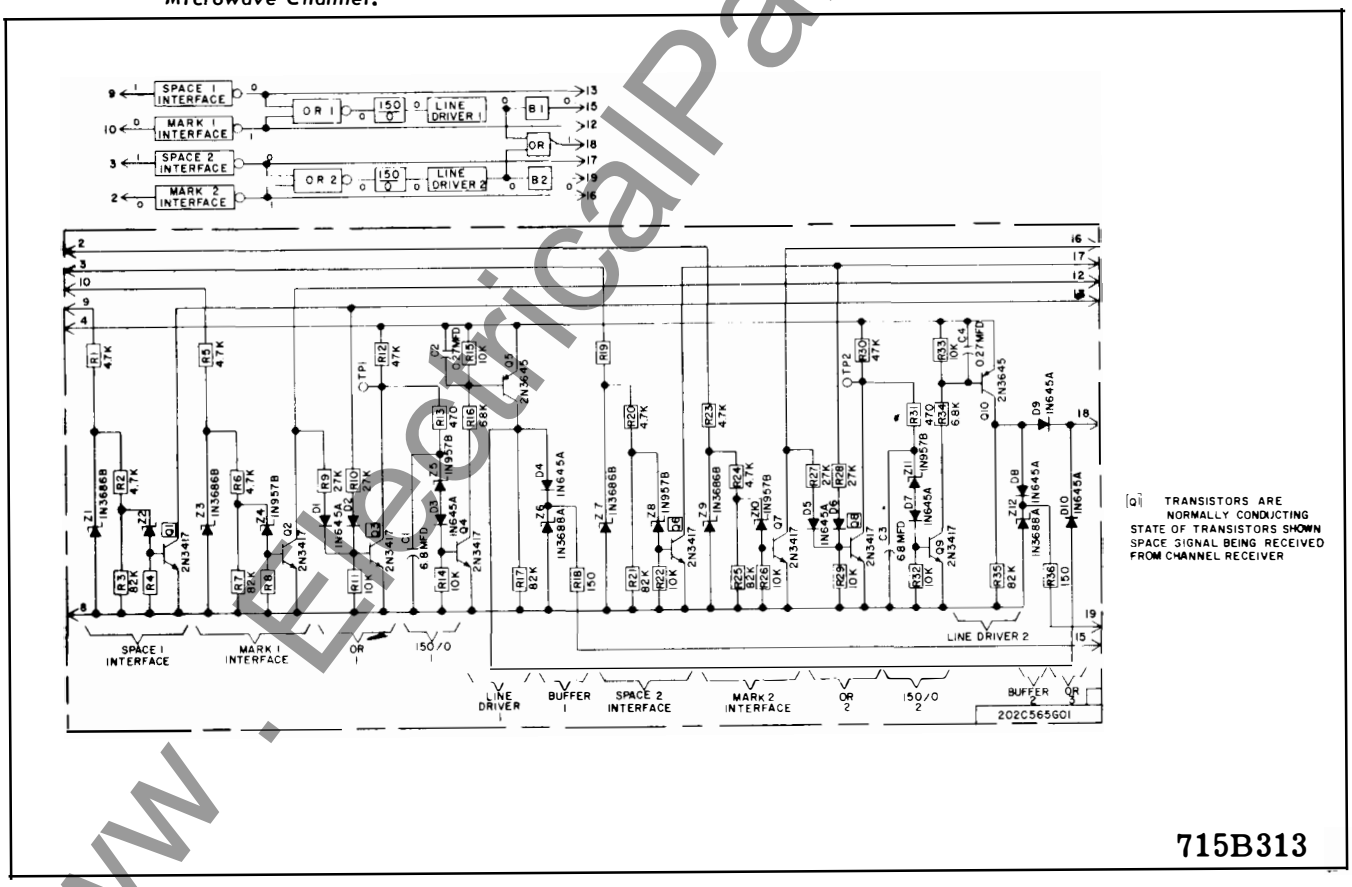


Fig. 18. Schematic of Supervision Board for TCF Carrier Channel, TA2.2 Tone Channel, and MC-22 Microwave Channel.

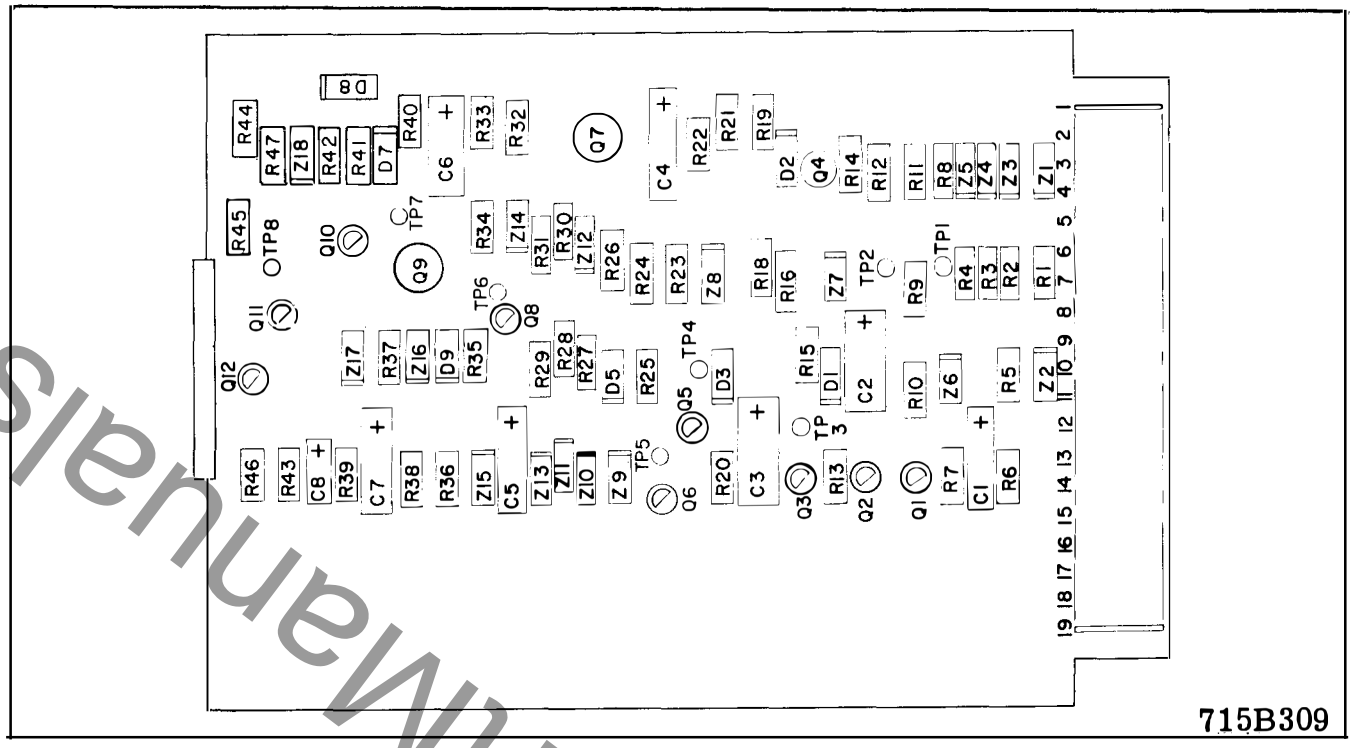


Fig. 19. Location of Components on Protective Relay Board.

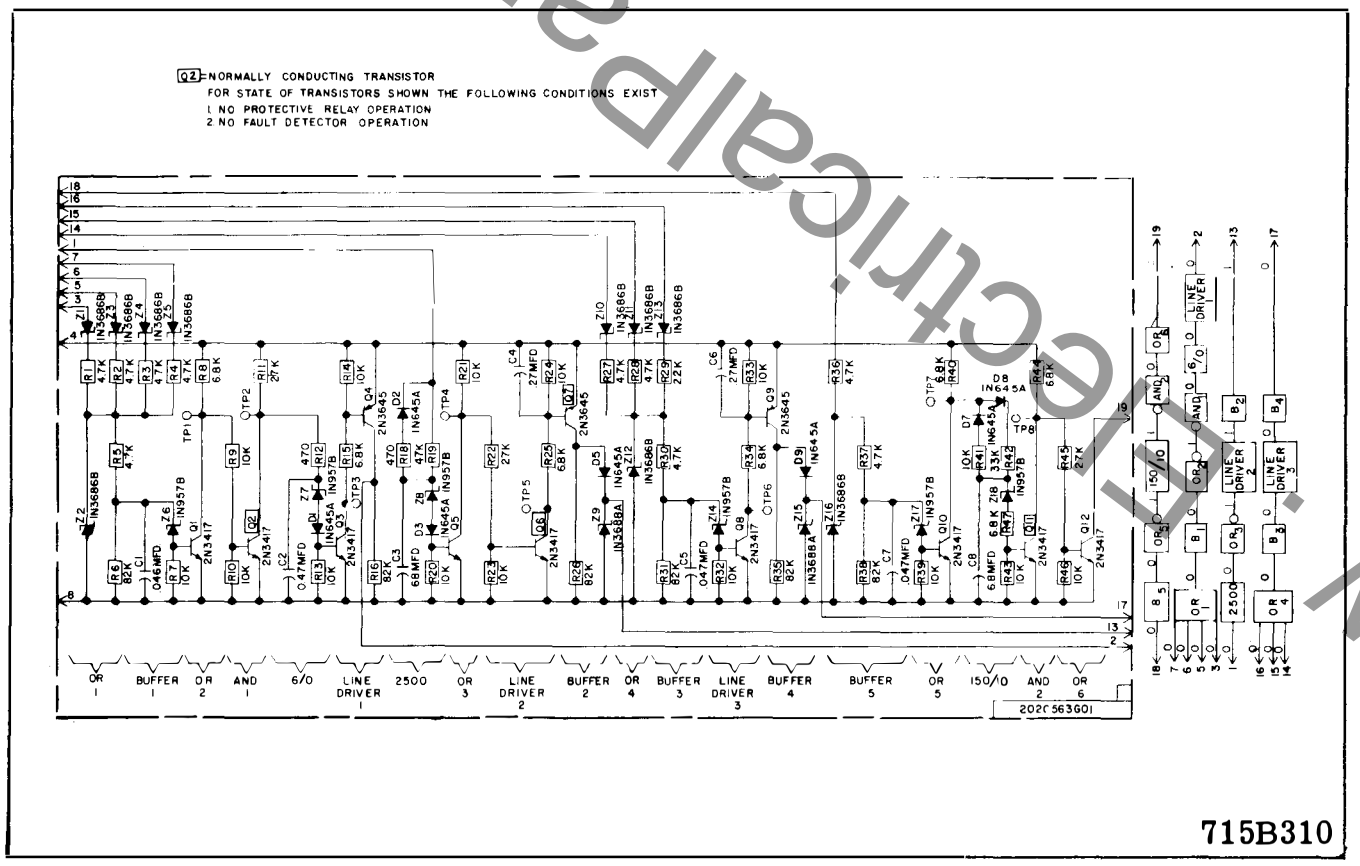


Fig. 20. Schematic of Protective Relay Board.

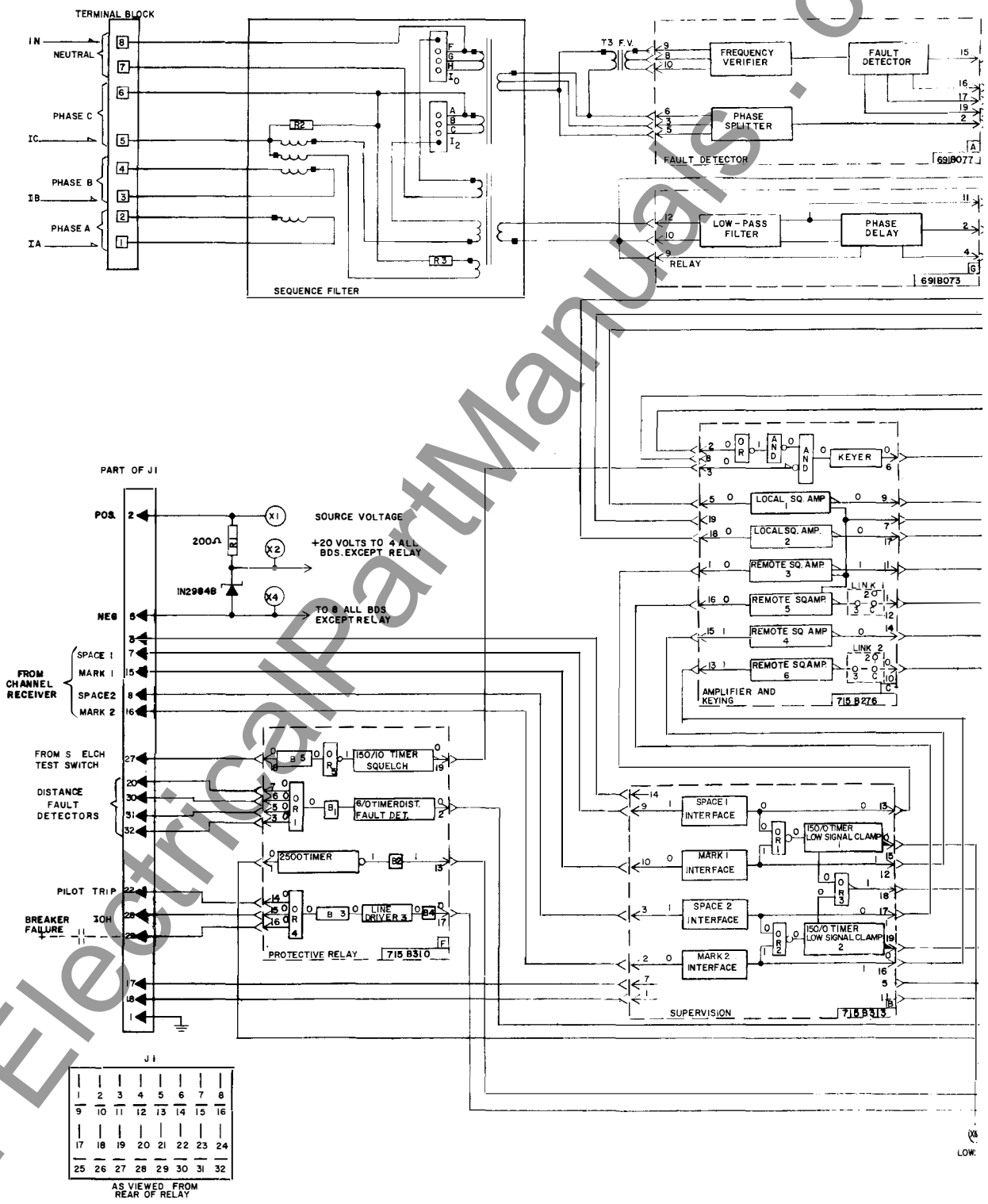
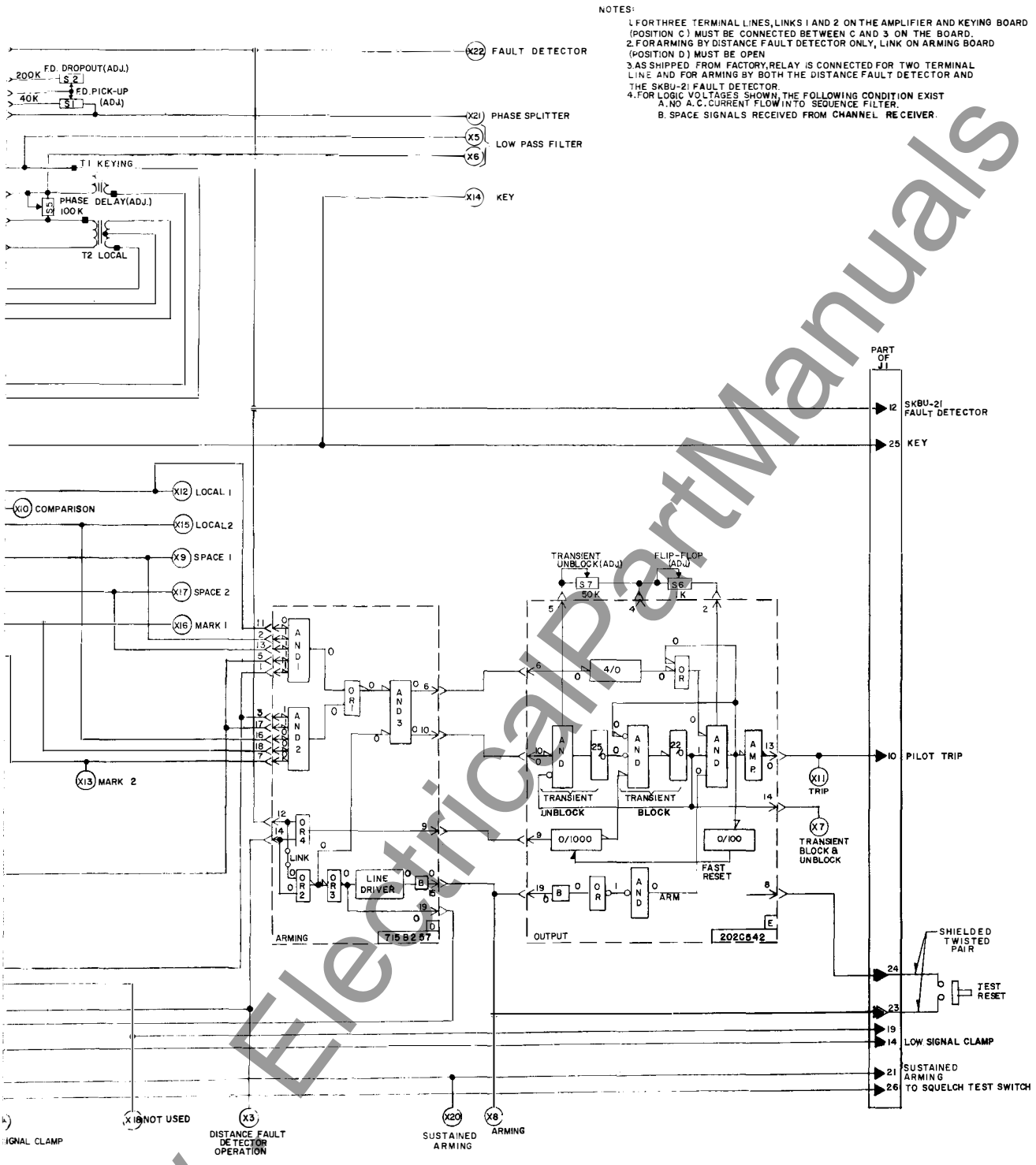


Fig. 22. Logic Diagram of SKBU-21 for TA2.2 C



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annel, MC-22 Microwave Channel and TCF Carrier Channel.

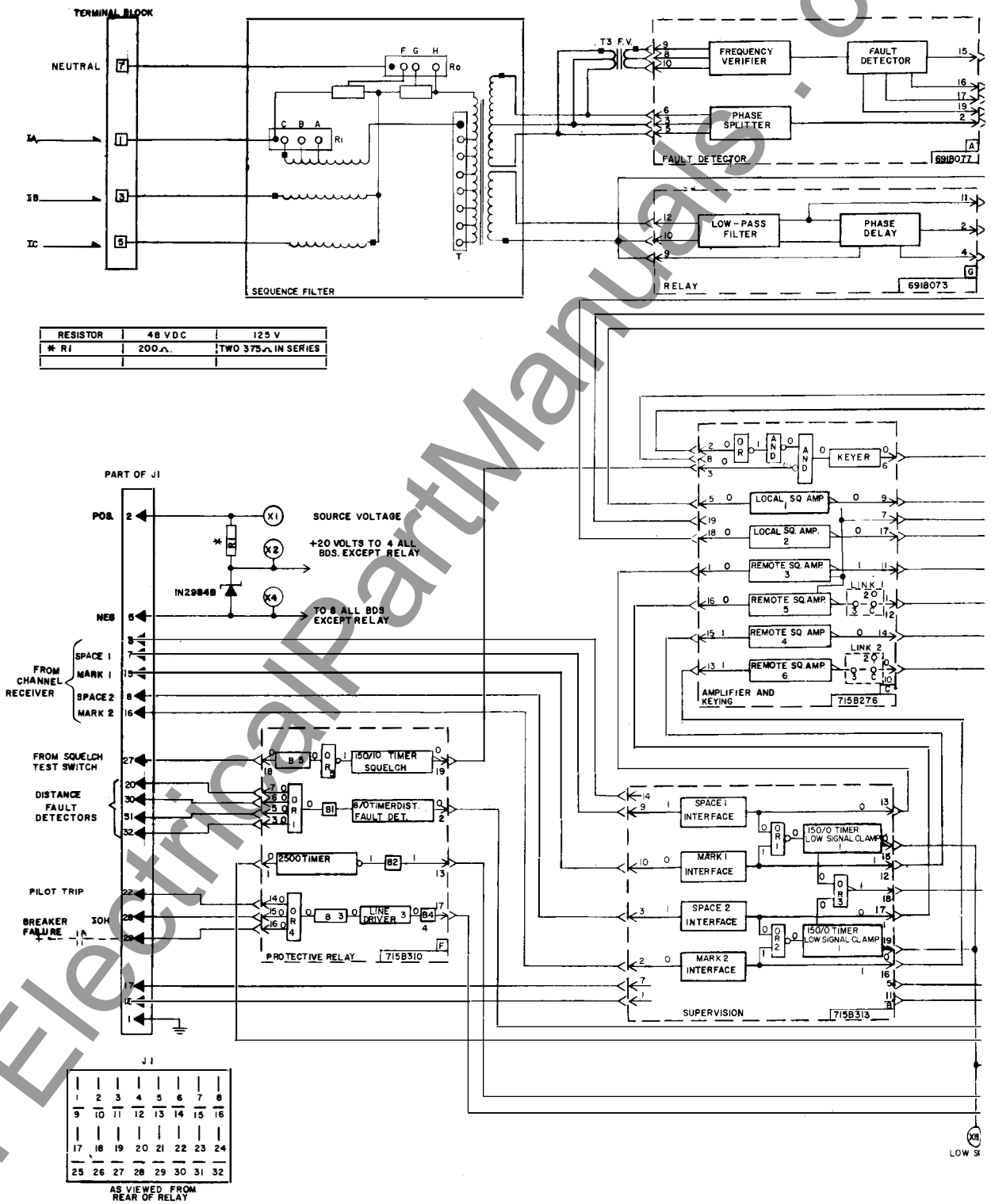
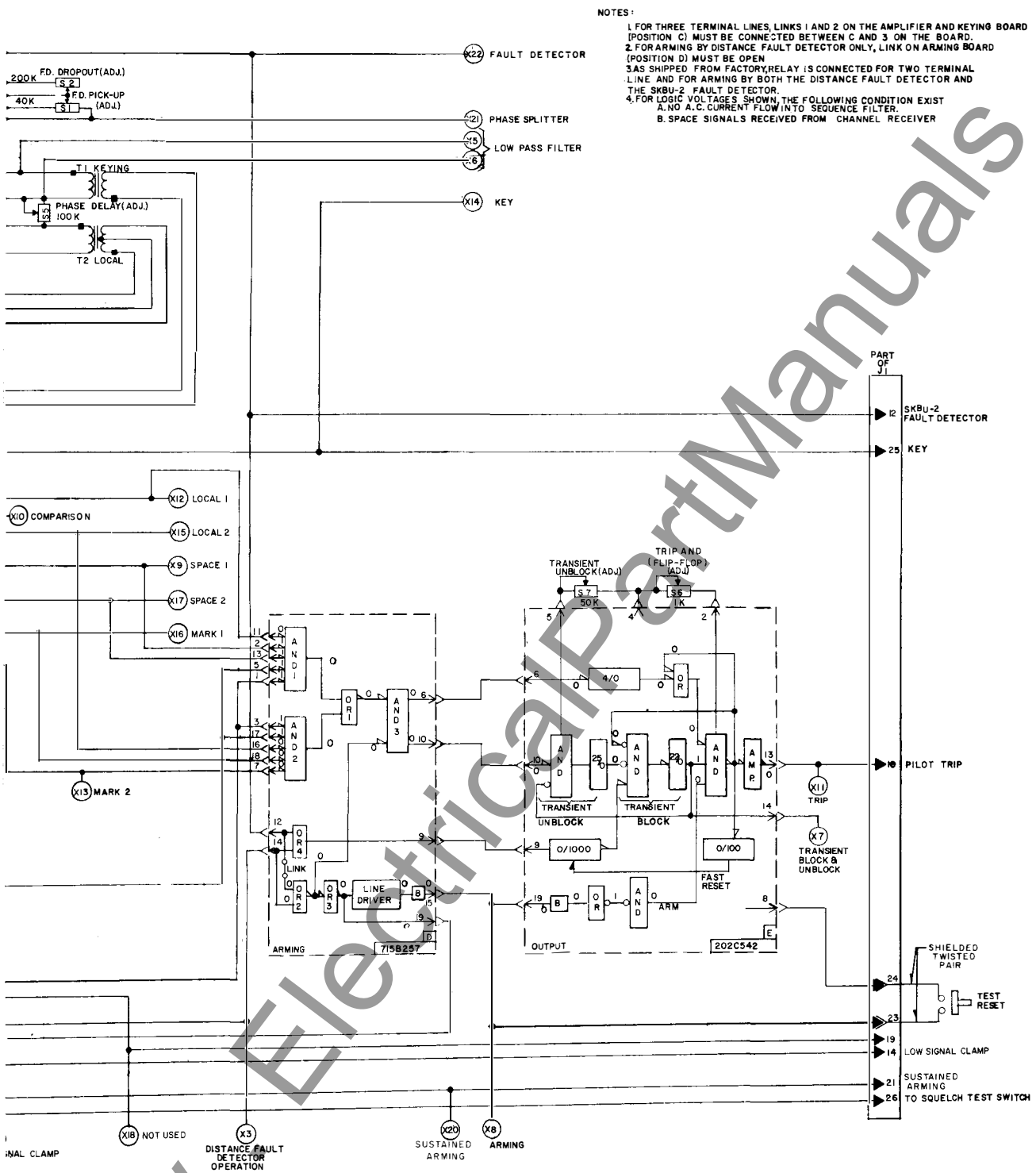


Fig. 24. Logic Diagram of SKBU-2 for TA2.2



5489D84

Tone Channel, MC-22 Microwave Channel and TCF Carrier Channel.

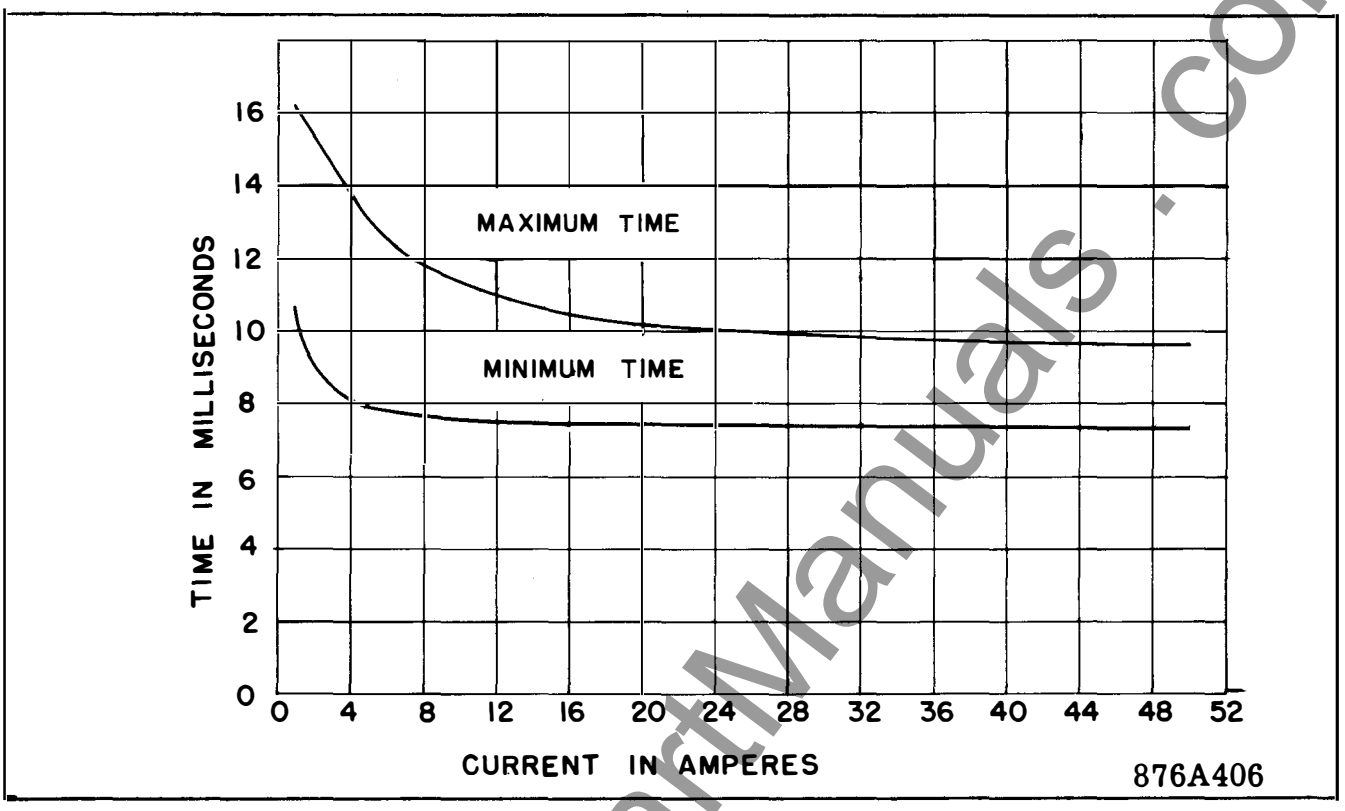


Fig. 25. Operating Times of Fault Detector of SKBU-21 Relay.

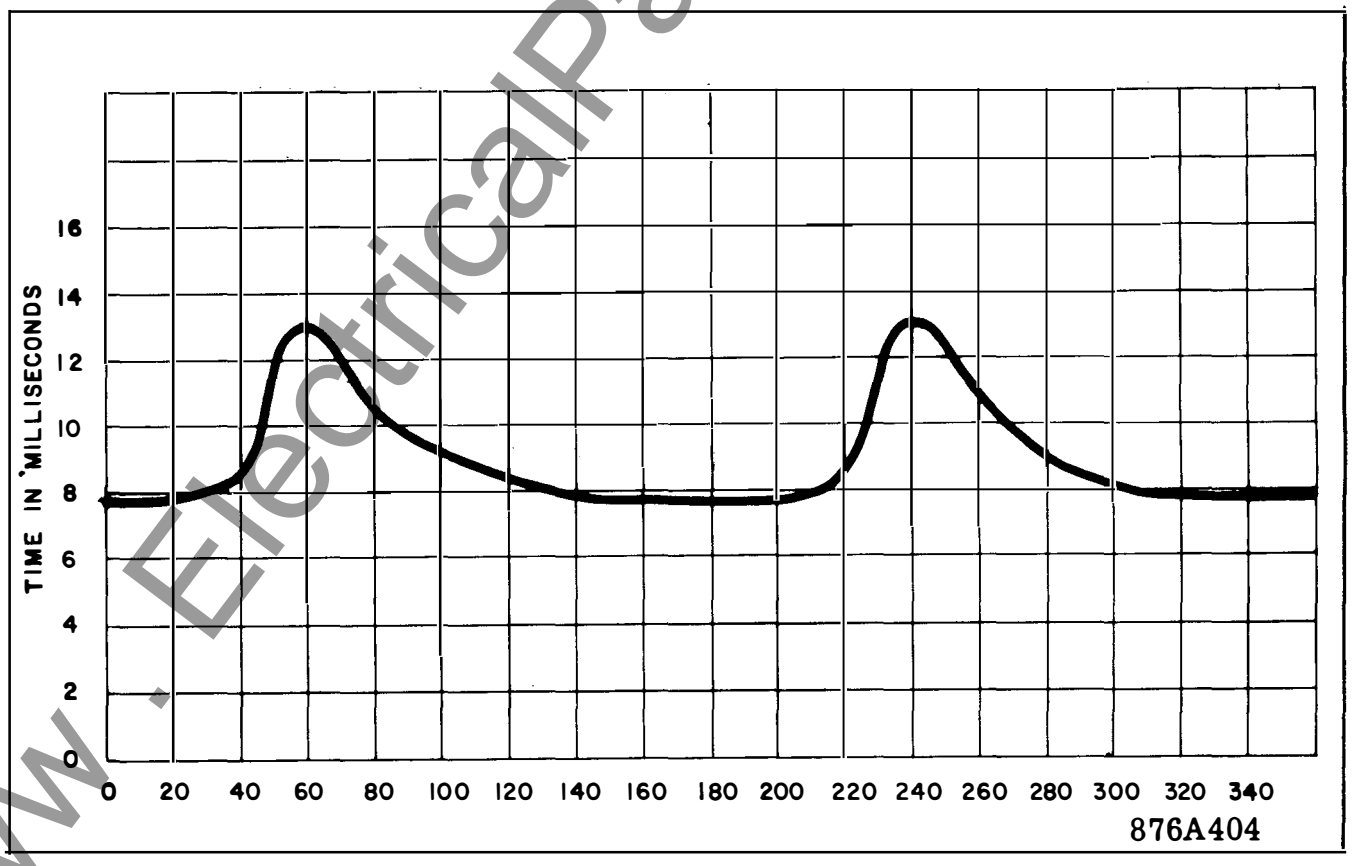


Fig. 26. Operating Times for Fault Detector of SKBU-21 Relay as a Function of Fault Incidence Angle at 5 amperes.

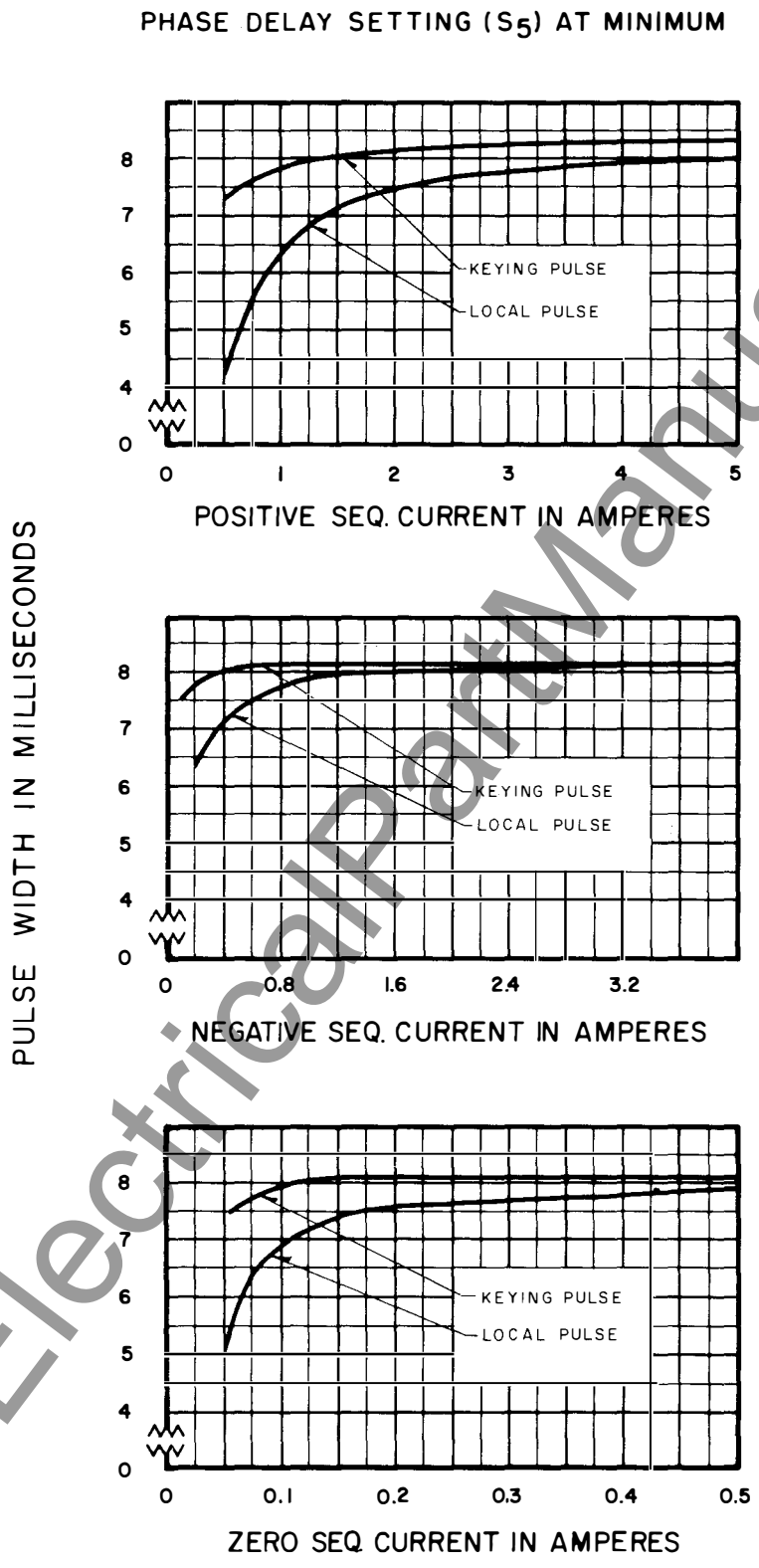


Fig. 27. Width of Keying Pulses at Different Current Levels of SKBU-21 Relay.

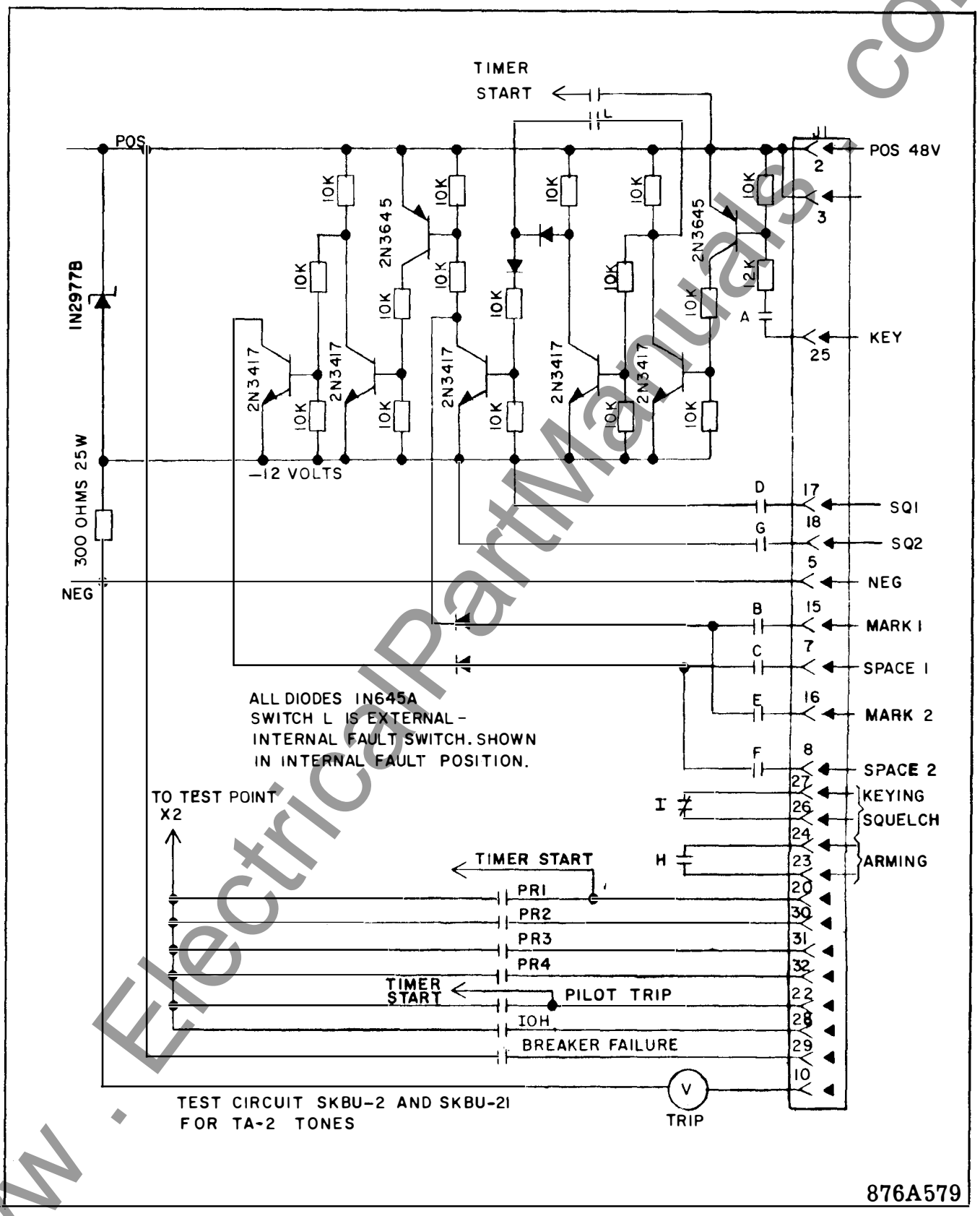


Fig. 28. Test Circuit of SKBU-21 Relay for TA-2 Tone Channel.

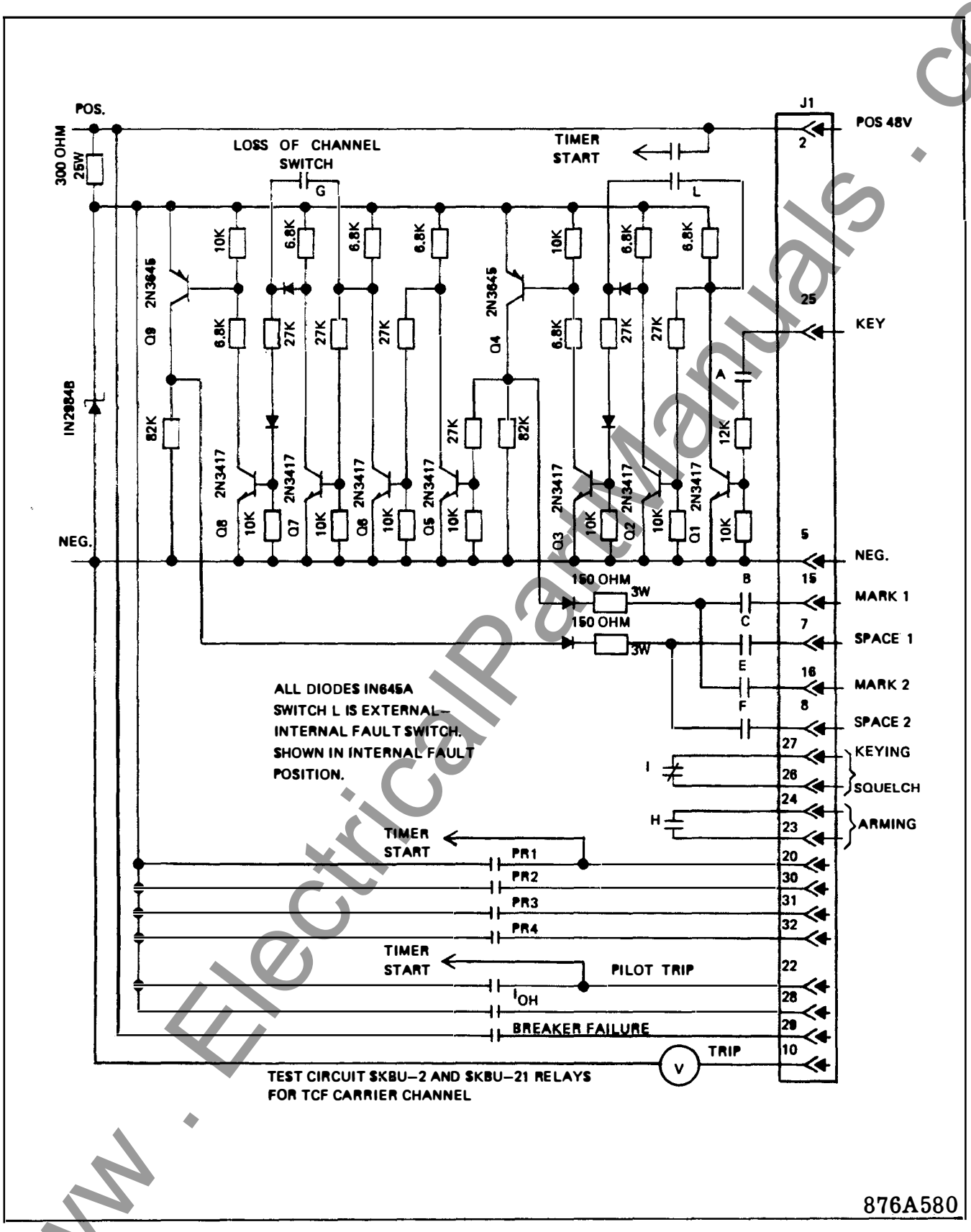
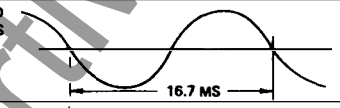
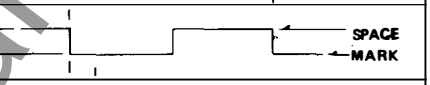
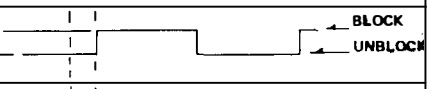
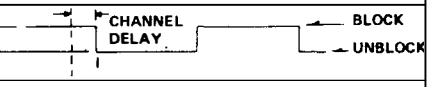
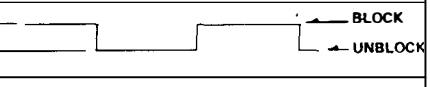
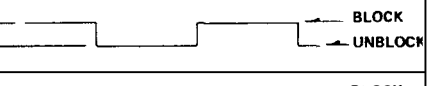
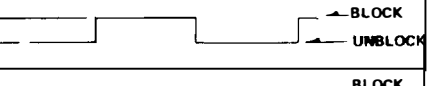
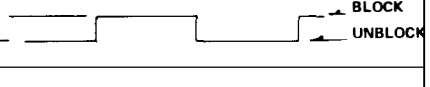
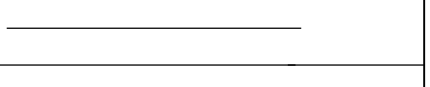
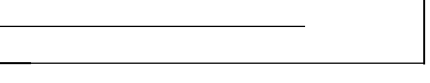


Fig. 29. Test Circuit of SKBU-21 Relay for TCF Carrier Channel, TA2.2 Tone Channel, and MC-22 Microwave Channel.

TEST POINT	CIRCUIT	VOLTAGE TO X4
X1	D.C. INPUT VOLTAGE	48 VOLTS D.C.
X2	REGULATED D.C.	20 VOLTS D.C.
X4	BATTERY NEGATIVE	
X7	TRANSIENT BLOCK	NORMAL 20 VOLTS OPERATE 0 VOLTS
X8	ARMING	NORMAL 20 VOLTS OPERATE 0 VOLTS
X11	PILOTTRIP	NORMAL 0 VOLTS OPERATE 20 VOLTS
X18	NOISE (TA–2 ONLY)	NORMAL 0 VOLTS OPERATE 20 VOLTS
X3	DISTANCE FAULT DETECTOR OPERATION	NORMAL 0 VOLTS OPERATE 20 VOLTS
X19	LOSS OF SIGNAL CLAMP	NORMAL 0 VOLTS OPERATE 20 VOLTS
X20	SUSTAINED ARMING	NORMAL 20 VOLTS OPERATE 0 VOLTS
X22	FAULT DETECTOR	NORMAL 0 VOLTS OPERATE 20 VOLTS
X5 TO X4(GND)	LOW PASS FILTER	I LOAD 5 AMPS 3 Ø  16.7 MS
X14	KEYING TONE CHANNEL ØØ	 X Y SPACE MARK
X14	KEYING TCF POWER LINE CARRIER CHANNEL	 20 0 MARK SPACE
X12	LOCAL SIGNAL 1	 20 0 BLOCK UNBLOCK
X9	SPACE SIGNAL 1 REMOTE 3	 20 0 CHANNEL DELAY BLOCK UNBLOCK
X17	SPACE SIGNAL 2 REMOTE 5 (3 TERMINAL LINE)	 20 0 BLOCK UNBLOCK
X15	LOCAL SIGNAL 2	 20 0 BLOCK UNBLOCK
X16	MARK SIGNAL 1 REMOTE 4	 20 0 BLOCK UNBLOCK
X13	MARK SIGNAL 2 REMOTE 6 (3 TERMINAL LINE)	 20 0 BLOCK UNBLOCK
X10	COMPARER	
X21	PHASE SPLITTER	

ØØ = TA 2 TONE CHANNEL X = 45 VOLTS Y = 36 VOLTS
TA2.1 TONE CHANNEL X = 18 VOLTS Y = 8 VOLTS

716B052

Fig. 30. Table III Test Point Voltage.

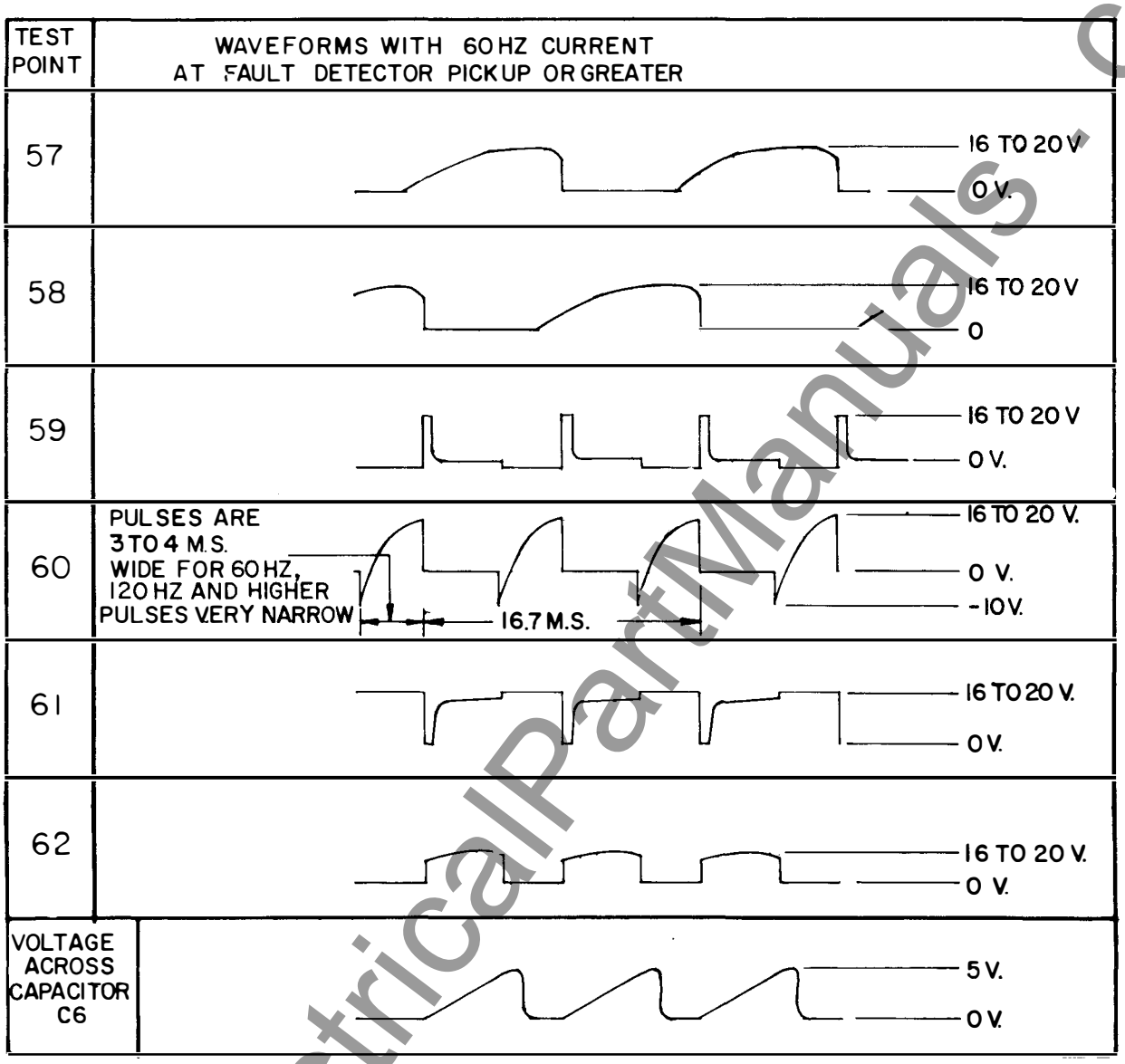


Fig. 31. Frequency Verifier Waveforms at 60 Hz.

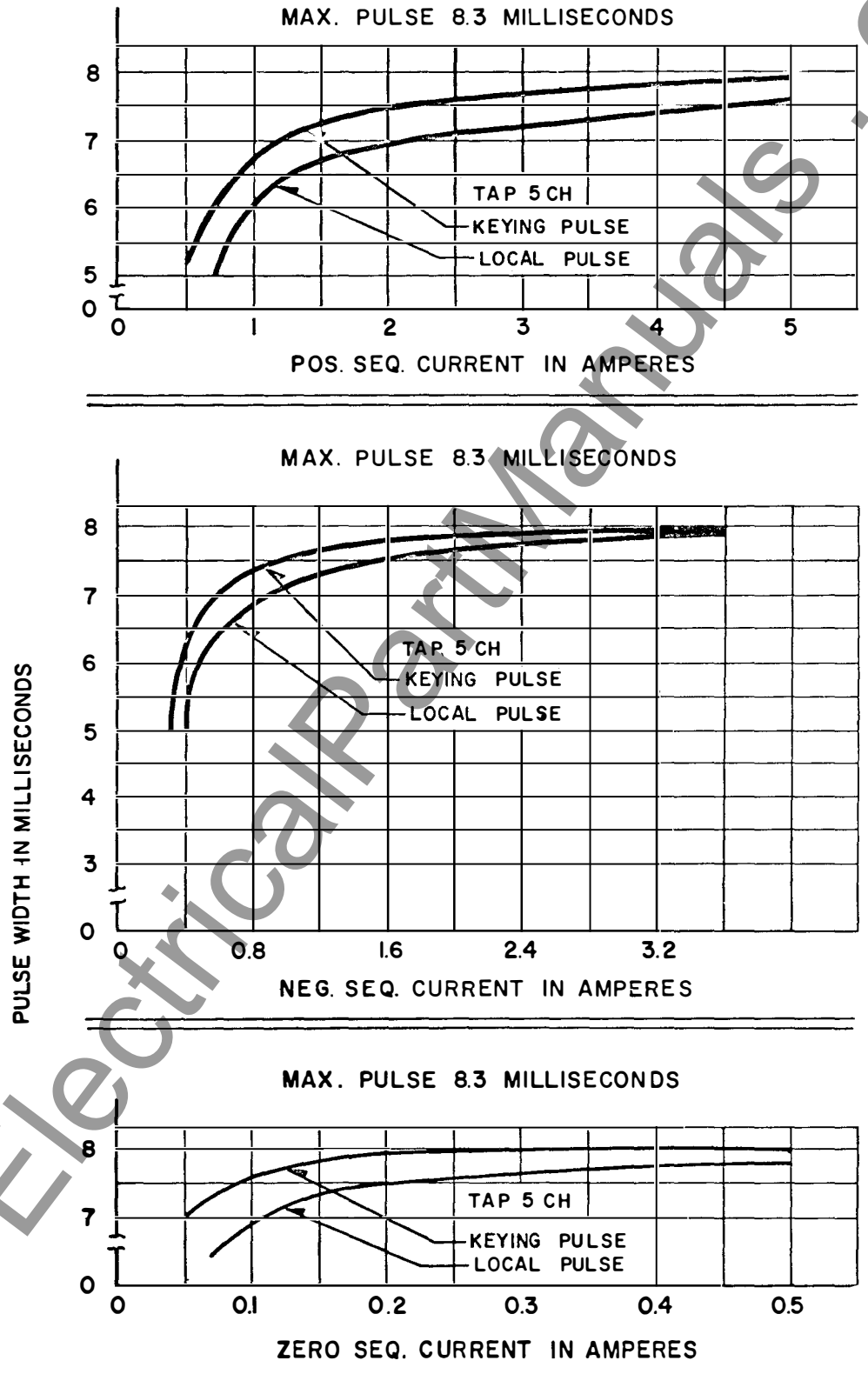


Fig. 32. Width of Keying Pulses at different current levels of SKBU-2 Relay.

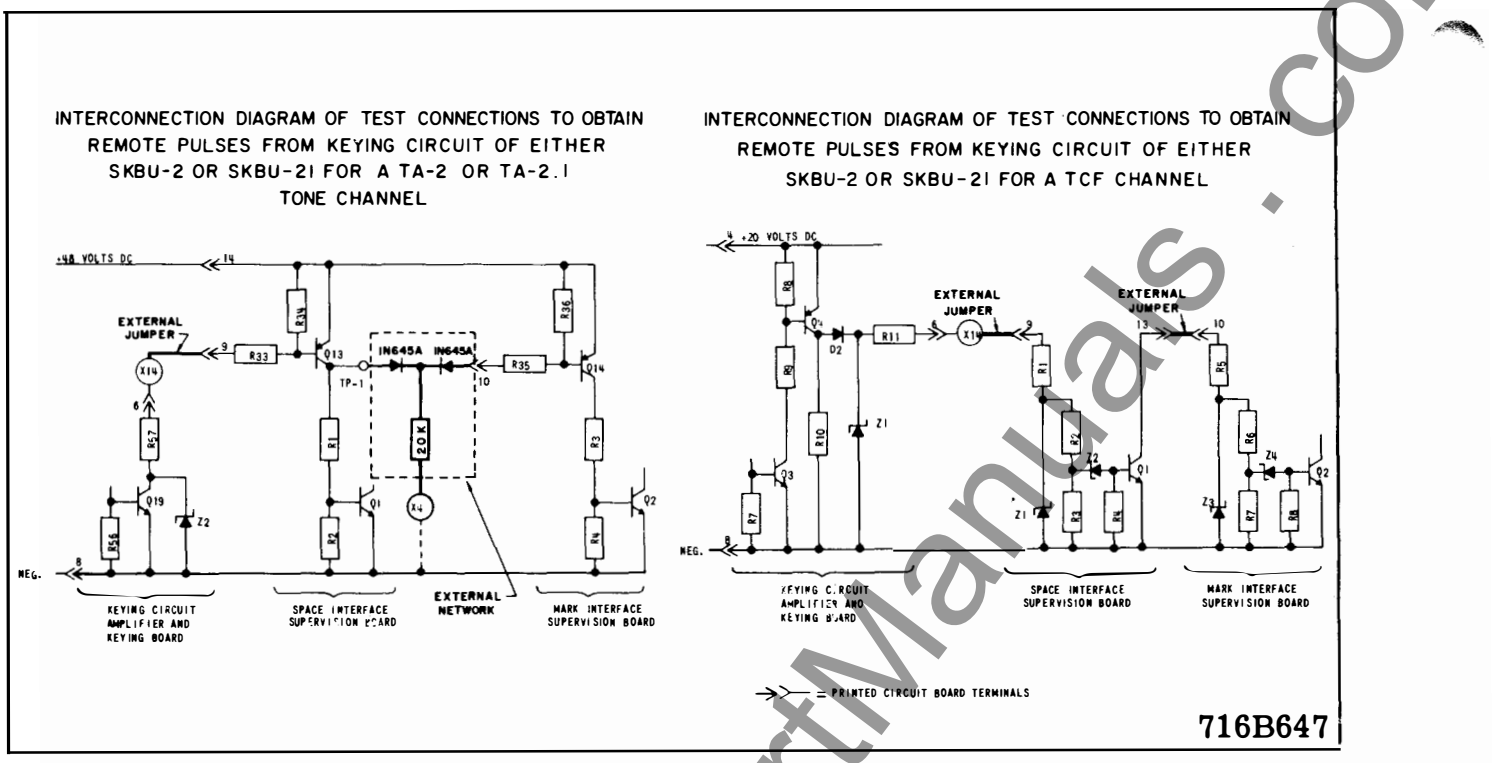


Fig. 33. Inter Connection Diagram of Test Connections to Obtain Remote Pulses from Keying Circuit.

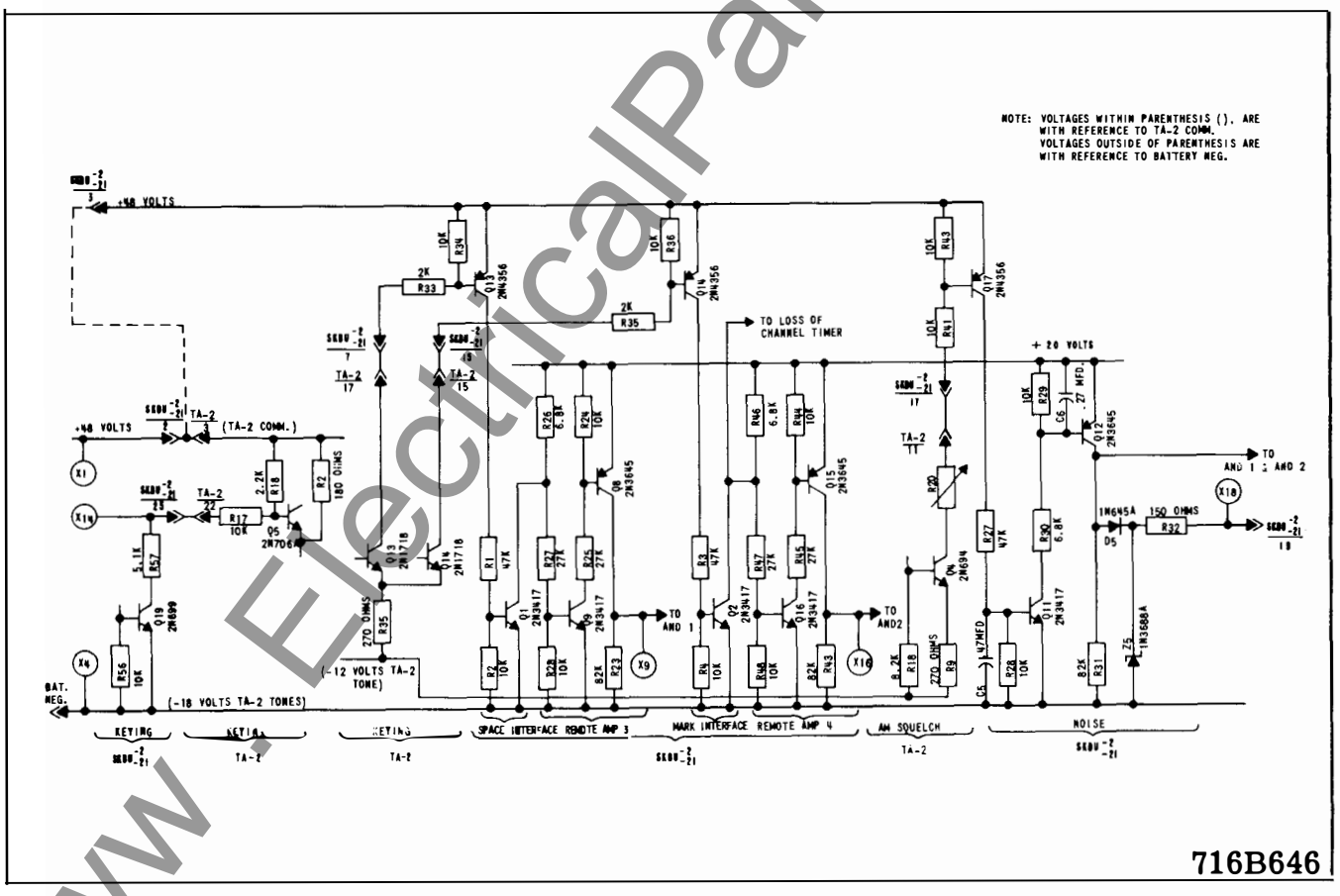


Fig. 34. Elementary Connections of SKBU to TA-2 Tone Channel.

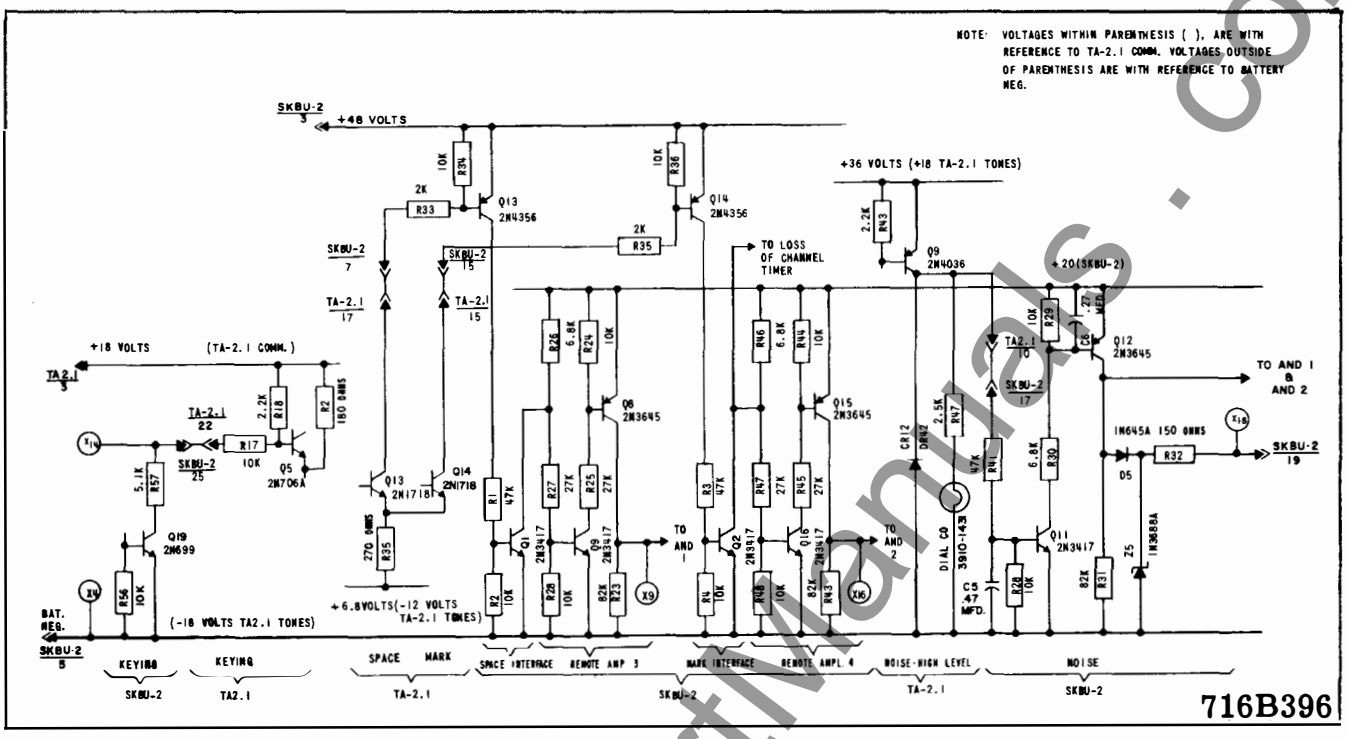


Fig. 35. Elementary Connections of SKBU to TA-2.1 Tone Channel.

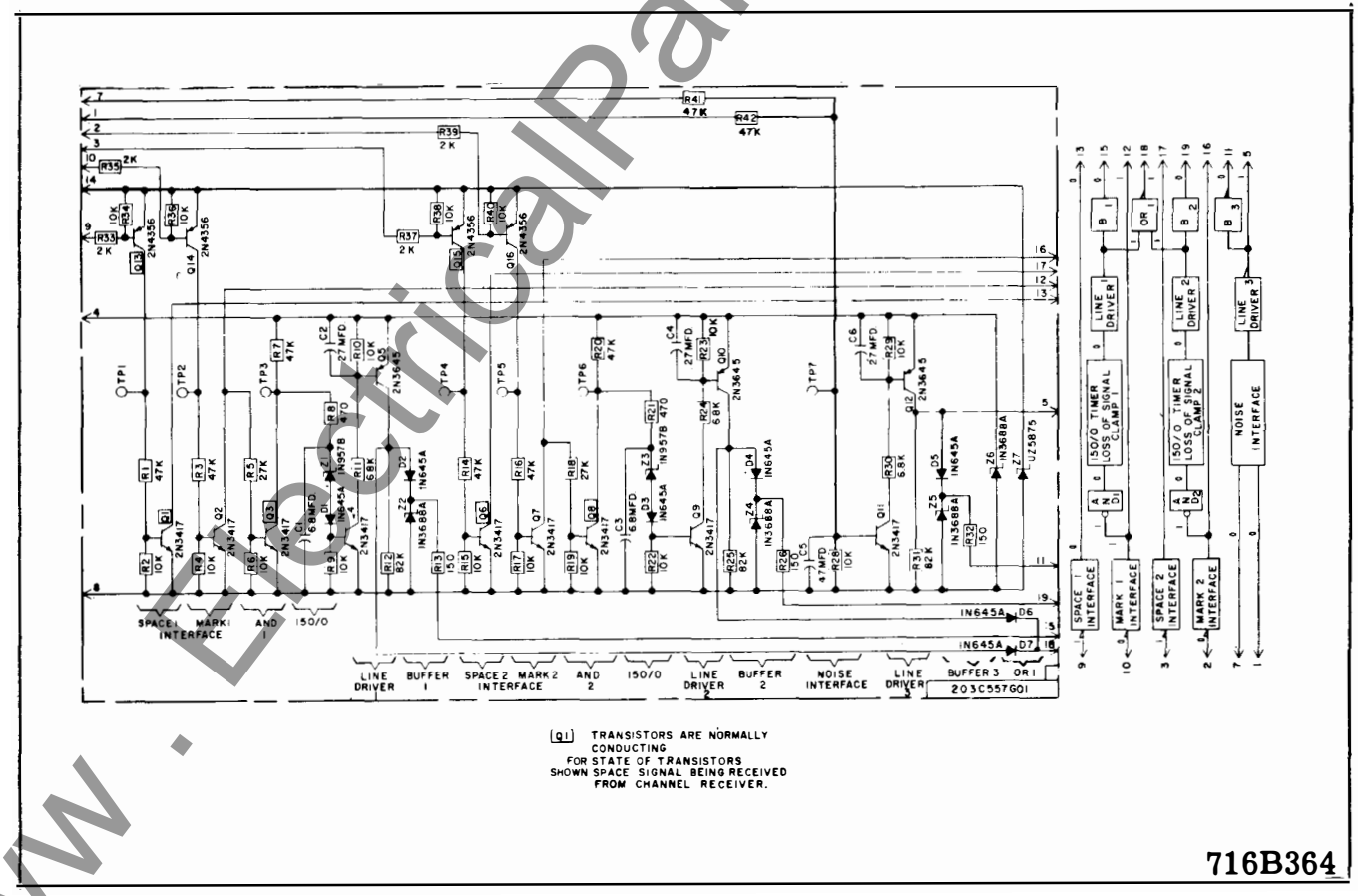


Fig. 36. Schematic of Supervision Board for TA-2.1 Tone Channel.

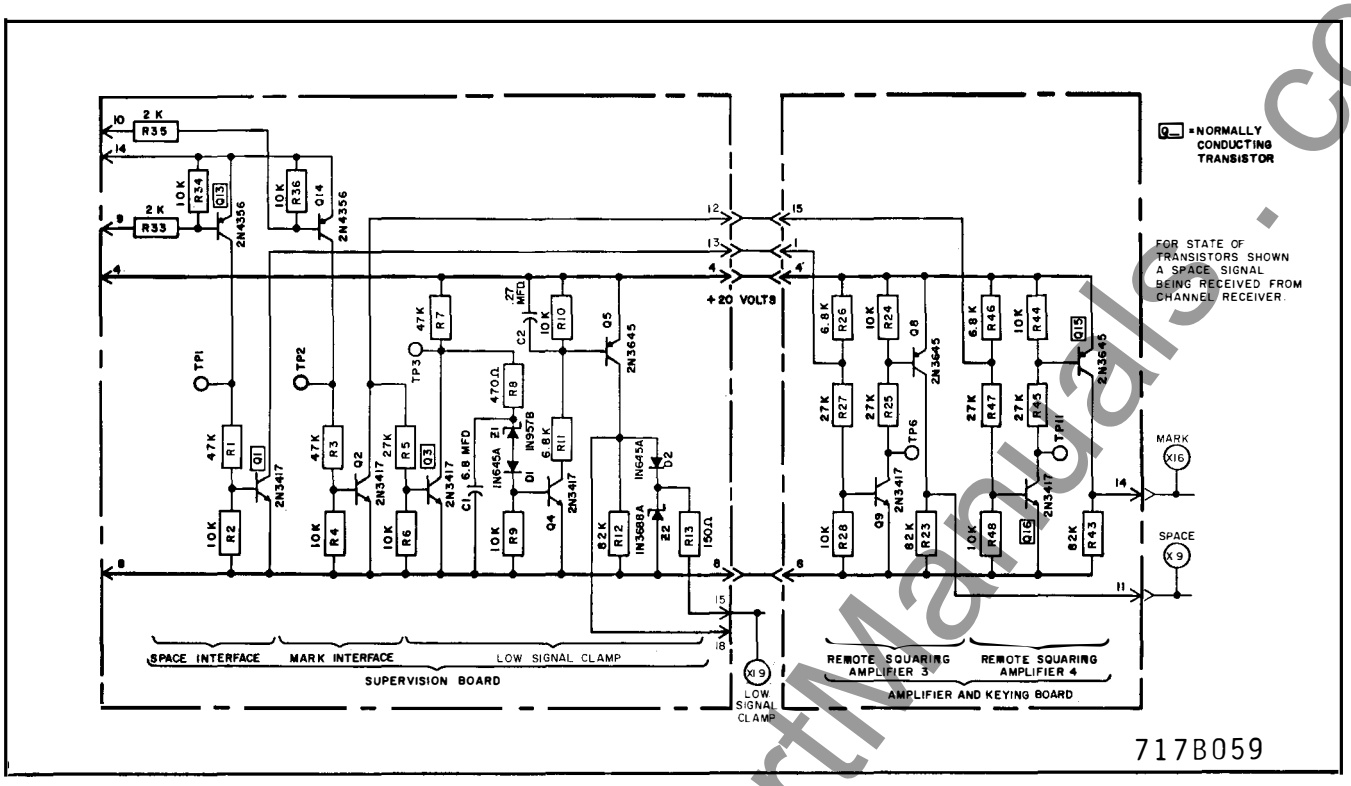


Fig. 37. Connection Diagram of Remqte Squaring Amplifiers of SKBU-2 and SKBU-21 Relays for TA-2 Tone Channel.

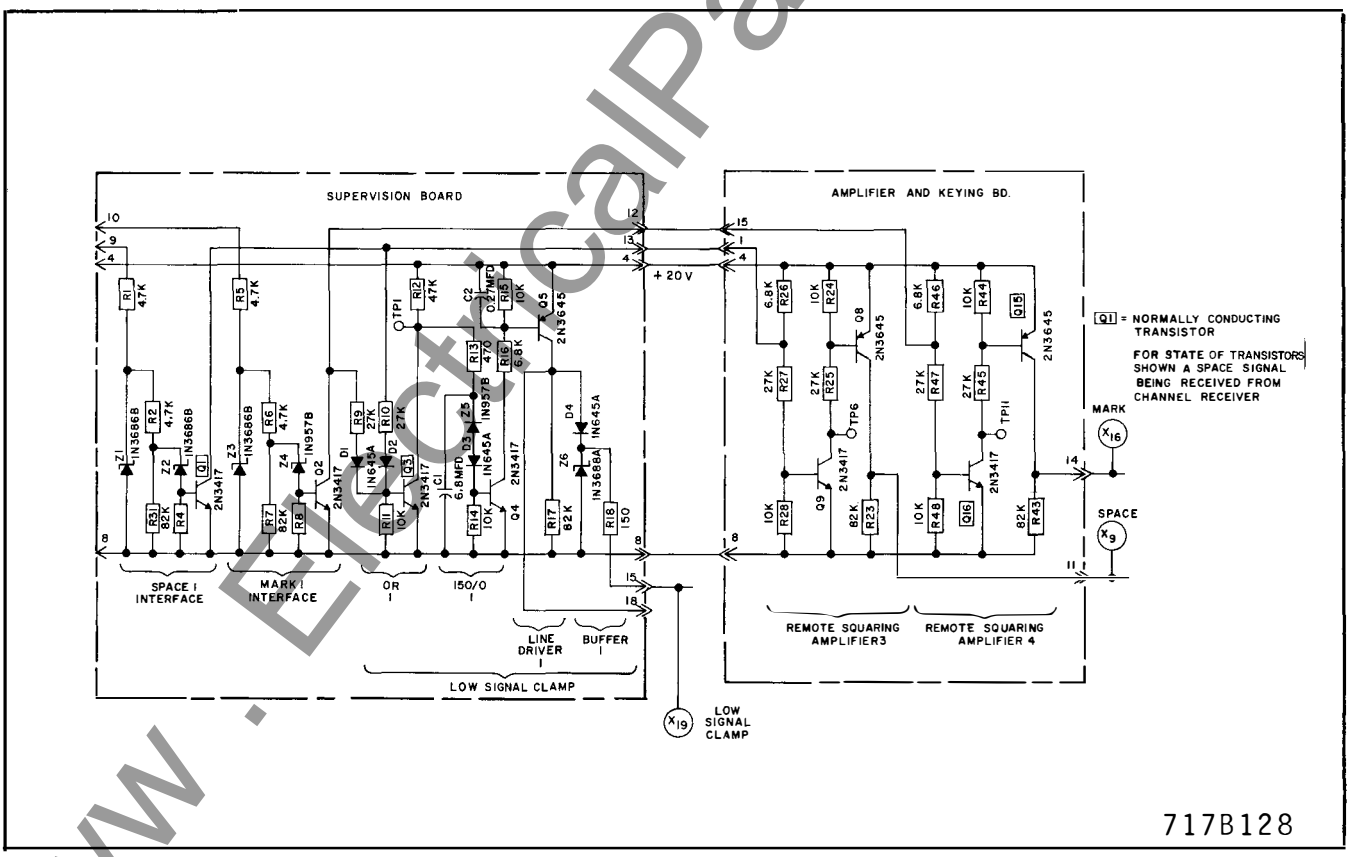


Fig. 38. Connection Diagram of Remote Squaring Amplifiers of SKBU-2 and SKBU-21 Relays for TCF Carrier Channel, TA2.2 Tone Channel and MC-22 Microwave Channel.

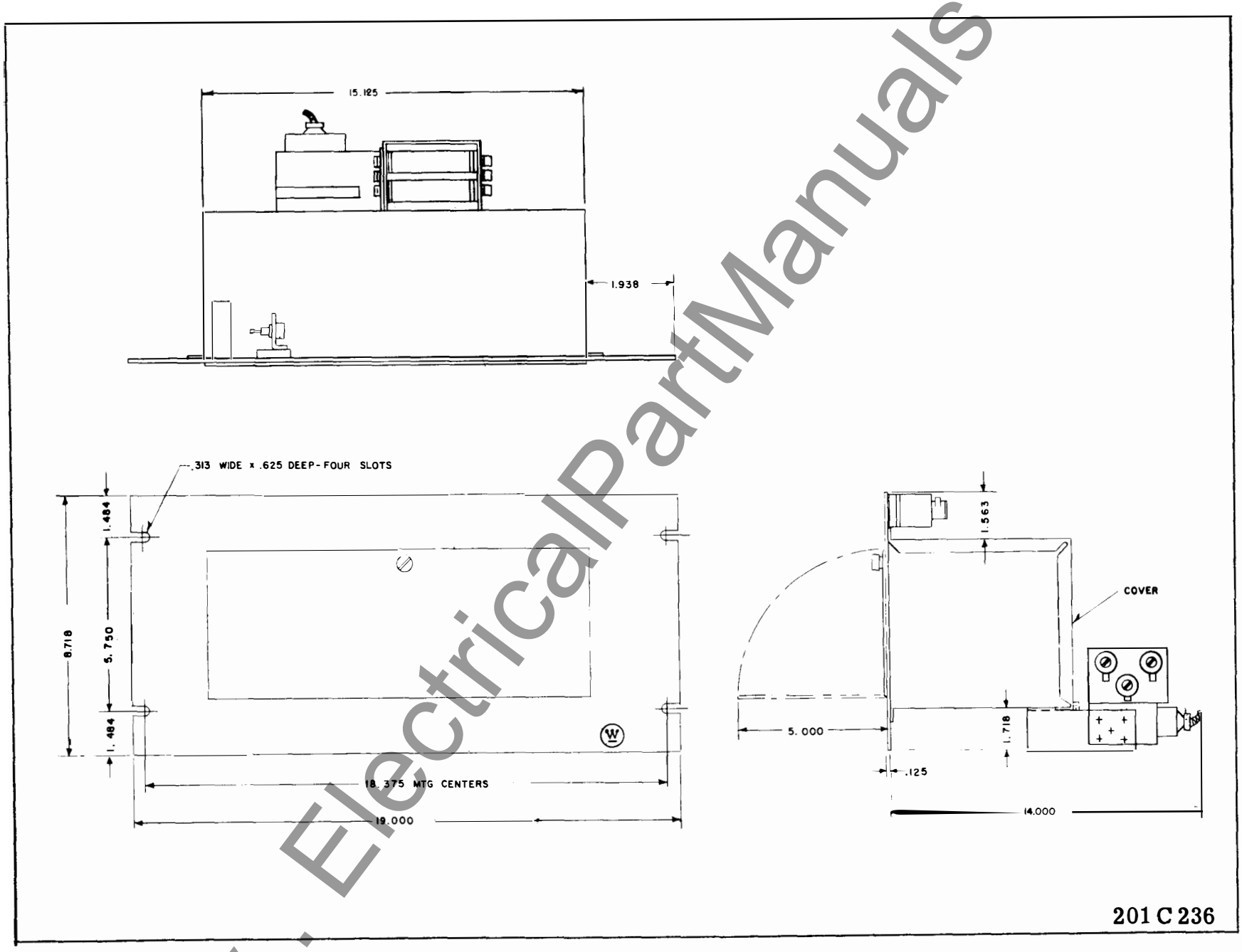


Fig. 39 Outline for the Type SKBU-21 Relay

WESTINGHOUSE ELECTRIC CORPORATION
RELAY-INSTRUMENT DIVISION **NEWARK, N. J.**
Printed in U.S.A.

INSTALLATION • OPERATION • MAINTENANCE

INSTRUCTIONS

TYPE SKBU-1 AND TYPE SKBU-11 PHASE COMPARISON RELAY FOR TC CARRIER CHANNEL

CAUTION: It is recommended that the user of this equipment become acquainted with the information ✪ in this instruction leaflet and in the system instruction leaflet before energizing the system.

Printed circuit modules should not be removed or ✪ inserted when the relay is energized. Failure to observe this precaution can result in an undesired tripping output and can cause component damage.

APPLICATION

The type SKBU-1 relay and the type SKBU-11 relay are relays used in conjunction with a type TC power line ✪ carrier set to provide complete phase and ground fault protection of a two-terminal transmission line. Simultaneous tripping of the relay at each line terminal is obtained in less than twenty-five milliseconds for all internal faults within the limits of the relay settings. The phase-comparison system operates on line current only, and no source of ac line potential is required. The distance phase-comparison systems use distance relays to complement the fault detectors. Neither system will trip during a swing or out-of step conditions. The carrier equipment operates directly from the station battery.

CONSTRUCTION

The phase comparison relays consist of a com- ✪ posite positive, negative and zero sequence current network, a saturating transformer, three isolating transformers, a 20-volt power supply, and printed circuit boards mounted on a standard 19-inch wide panel, 8-3/4 inches high (5 rack units). The SKBU-11 relay has a second saturating transformer in addition to these components. Edge slots are provided for mounting the rack on a standard relay rack.

Sequence Network

a. SKBU-11

The sequence filter consists of a three-legged iron core reactor and a resistor. The reactor is a four-winding reactor with two primary windings and two secondary windings. The secondary windings are connected to the resistor which consists of three tube resistors and a small formed resistor. One secondary winding and the resistor is a negative sequence current filter while the other secondary winding and the resistor is a positive sequence filter.

b. SKBU-1 Relay

The sequence filter consists of a three-legged iron core reactor and a set of resistors, R_1 and R_0. The reactor has three windings: two primary and a tapped secondary winding, wound on the center leg of a "F" type of lamination The secondary taps are wired to the A, B and C tap connections in the front of the relay (R_1 taps). Ro consists of a three tube resistors with taps wired to F, G and H tap connections in the front of the relay. The R_0 resistor is a formed resistor associated with the tapped secondary of the reactor.

Saturating Transformer

a. SKBU-11 Relay

The voltage from the sequence network is fed into two saturating or mixing transformers. One transformer supplies a fault detector circuit and the other transformer supplies a keying circuit. Zero sequence current windings are are included on the transformer.

b. SKBU-1 Relay

The voltage from the sequence network is fed into the tapped primary of a saturating transformer which has two secondary windings. One winding supplies the fault detector circuit and the other winding supplies a keying circuit.

All possible contingencies which may arise during installation, operation, or maintenance, and all details and variations of this equipment do not purport to be covered by these instructions. If further information is desired by purchaser regarding his particular installation, operation or maintenance of his equipment, the local Westinghouse Electric Corporation representative should be contacted.

SUPERSEDES I.L. 41-954.3D, DATED APRIL 1977
✪ DENOTES CHANGE FROM SUPERSEDED ISSUE. EFFECTIVE SEPTEMBER 1978

Isolating Transformer

Three isolating transformers are provided in the relay to isolate the dc voltages from the ac voltages. Two of the transformers are also used to energize solid-state circuit on alternate half-cycle of the power system frequency.

Power Supply

The solid-state circuits of the relays are regulated from a 20-volt supply on the relay panel. This voltage is taken from a Zener diode mounted on a heat sink. A voltage dropping resistor is provided betwe en the source dc supply and the 20 volt regulated supply.

Printed Circuit Boards

Seven printed circuit boards are used in these relays: A fault detector board, protective relay interface board, supervision board, amplifier and keying board, arming board, output board and a relay board. The circuits of the protective relay board vary with the relaying system.

All of the circuitry that is suitable for mounting on printed boards is contained in an enclosure that projects from the rear of the front panel and is accessible by opening a hinged door on the front of the panel. The printed circuit boards slide in position in slotted guides at the top and bottom of each compartment and the board terminals engage a terminal block at the rear of the compartment. Each board and terminal block is keyed so that if a board is placed in the wrong compartment, it cannot be inserted into the terminal block. A handle on the front of each board is labeled to identify its function in the relay.

1. FD Board (Fault Detector Board)

The fault detector board contains a resistor-Zener diode combination, a phase splitting network, a solid-state fault detector, and a frequency verifier circuit. The controls for setting pickup (S_1) and dropout (S_2) of the fault detector are mounted on a plate in the front of the relay. This unit operates when the fault current exceeds a definite value.

The location of components on the board is shown in Fig. 3 and the schematic of the board is shown in Fig. 4.

2. Arming Board

The arming board connects the outputs of the supervision board and the fault detector board to the final output of the relay. This board contains logic circuits that will arm the trip output, set up the time delay of the trip output, and start transient blocking on external faults.

The location of components on the board is shown in Fig. 5 and the schematic of the board is shown in Fig. 6.

3. Amplifier and Keying Board

The amplifier and keying board contains a local squaring amplifier, a transmitter keying circuit, a remote squaring amplifier, and a signal squelch circuit for each line terminal. The amplifier circuits produce the pulses that are compared by AND circuit of the arming board to determine if the fault is external or internal.

The location of components on the board is shown in figure 7, and the schematic of the board is shown in Fig. 8.

4. Output Board

The output board contains a 4-millisecond pick-up instantaneous dropout timer circuit, trip "AND" (flip-flop circuit), trip amplifier, transient blocking and unblocking circuits. The trip AND operates when all the inputs to the AND inputs of the arming board are of the correct polarity and the fault detector has operated. The transient blocking circuit operates after a time delay on external faults, and the transient unblock circuit operates after a time delay on a sequential fault (external fault followed by an internal fault). The following figures apply to this board: Fig. 9 Component Location; Fig. 10 Schematic of the Board.

5. Relay Board

The relay board contains the phase delay circuit for shifting the local signals with reference to the remote signals. It also contains a low-pass filter. For the SKBU-11 relay, a Zener clipper-resistor combination is provided for protection of the solid-state circuits.

The following figures apply to this board: Fig. 11 Component Location, and Fig. 12 for the schematic of the board.

6. Supervision Board

The supervision board contains a 8/0 timer for distance fault detector operation, a 2.5 second

alarm circuit for sustained arming operation, a fault detector (FD1) and a carrier control circuit. The circuits on this board are utilized to start carrier, to alarm on an sustained arming operation, and to delay arming for distance fault detector operation.

Fig. 13 shows the component location for this board and Fig. 14 shows the schematic of the board.

7. Protective Relay Board

The protective relay board contains logic circuits to connect the distance fault detectors, and squelch relays into the phase comparison portion of the relaying system. This board contains AND circuits, buffer circuits, and OR circuits to connect the relays into the system.

Fig. 15 shows the component location for the board. Fig. 16 and 17 shows the schematic of the board.

Card Extender

A card extender (style no. 644B315G02) is available for facilitating circuit voltage measurements or major adjustments. After withdrawing anyone of the circuit boards, the extender is inserted in that compartment. The board then is inserted into the terminal block on the front of the extender. This restores all components and test points on the boards are readily accessible.

Test Points

Test points are located on each printed circuit board for the major components on the board. Complete circuit test points are wired to the front panel of the relay for convenience in adjusting and testing the relay.

OPERATION

A. System

The SKBU carrier relaying system compares the phase position of the currents at the ends of a line section over a carrier channel to determine whether an internal or external fault exists on the line section.

1. SKBU-11 Relay

The three-phase line currents energize a sequence network in the SKBU-11 relay which produces two single-phase output voltages that are proportional to either the positive sequence current or the negative sequence current. The single-phase voltages are applied to two saturating or mixing transformers, one which energizes the fault detector circuits (FD-1 and FD-2) and the other energizes the keying circuit of the SKBU-11 relay through a low-pass filter. This circuit allows the transmission of carrier on alternate half-cycles of the power line frequency. Carrier is transmitted from both line terminals and is received at the opposite ends where it is compared with the phase position of the local sequence network output. If the local and remote pulses are in an internal fault relationship and the fault detector has operated, tripping will occur 5-milliseconds later through operation of the trip "AND" and trip amplifier circuits on the output board of the relay.

2. SKBU-1 Relay

The three-phase line currents energize a sequence network in the SKBU-1 relay which produce a single-phase output voltage proportional to a combination of sequence components of the line current. This single-phase voltage energizes the primary of a saturating transformer with two secondary windings. One secondary winding energizes the fault detector circuits (FD-1 and FD-2) and the second secondary winding energizes the keying circuit of the relay through the low pass filter. This circuit allows the transmission of carrier on alternate half-cycles of the power frequency current. cycles of the power line frequency. Carrier is transmitted from both line terminals it is compared with the phase position of the local sequence network output. If the local and remote pulses are in an internal fault relationship and the fault detector has operated, tripping will occur 5-milliseconds later through operation of the trip "AND" and trip amplifier circuits on the output board of the relay.

Current transformer connections to the sequence networks at the two line terminals are such that carrier is transmitted on the same half-cycles from both terminals during an internal fault to allow tripping during the half-cycle that carrier is not transmitted.

However, if the fault is external to the protected line section, carrier is transmitted on alternate half-cycles from opposite terminals. Thus each terminal blocks the opposite terminal during the half-cycle when it is attempting to trip.

The four-millisecond delay previously mentioned is added to allow for differences in current transformer performance at opposite line terminals, relay coordination, and momentary interruptions in carrier caused by arcing over of protective gaps in the tuning equipment.

Since this relaying system operates only during a fault, the carrier channel is available at all other times for the transmission of other functions.

B. Relay

With reference to the logic diagram that applies to the particular relay, the three-phase line currents energize a sequence filter that varies with the type relay.

1. SKBU-11 Relay

In the SKBU-11 relay, the sequence filter produces two single phase voltages: One voltage proportional to the positive sequence current, and the other voltage proportional to negative sequence current. These voltages are applied to primary windings of two saturating transformers where they are mixed to produce two separate secondary voltages proportional to a combination of sequence components. Zero sequence windings are included on the two transformers.

2. SKBU-1 Relay

In the SKBU-1 relay, the sequence filter produces a single phase voltage proportional to a combination of sequence components. This voltage is applied to the primary winding of a saturating transformer which produces two secondary voltages.

The secondary voltages are applied to two separate boards:

Voltage 1 to Fault Detector Board

Voltage 2 to Relay Board

1. Fault Detector Board

With reference to the schematic drawing of Fig. 4, the ac voltage is applied to terminals 6, 5, and 3 of the fault detector board. This voltage is then applied to a phase-splitting network (C52, R52, R53) and a polyphase rectifier (diodes D51 to D56). The dc voltages obtained from the rectifier are applied to the fault detector circuit (Q51, Q52, Q53, Q54) which operates when the dc input "signal" exceeds a predetermined value.

Fault Detector (FD-2)

Under normal conditions, transistor Q51, has no base "signal" and is turned off. The collector of Q51 is at positive potential and provides base drive to transistor Q52, driving it to conduction. With Q52 conducting there is no base drive to transistor Q53 and Q53 is turned off. This condition keeps transistor Q54 in a non-conducting state, equivalent to an open circuit.

When a fault causes the dc input voltage from the polyphase rectifier (across S_1 and R_{54}) to exceed the 6.8 volt rating of Zener diode Z52, a positive potential is applied to the base of Q51 causing it to conduct. In turn, Q52 stops conducting, and capacitor C54 charges, giving a few milliseconds time delay before Q53 and Q54 are switched to full conduction, thus "closing" the fault detector. When the fault detector operates, a positive input is applied to the arming board at terminal 12. The feedback path of resistors R66 and S2 increase the voltage to Z52 after the fault detector operates. This seals-in the fault detector and allows the fault detector to drop out at a high dropout ratio when the ac current is reduced.

Frequency Verifier (FV)

During certain switching conditions, such as energization of a transmission line, residual currents and voltages may exist of higher frequencies than 60 hertz. The frequency verifier prevents fault detector operation when frequencies 120 hertz or higher are encountered during the switching conditions. The frequency verifier circuit consists of two functional parts: Zero-crossing and commutator circuits. With reference to Fig. 4,

the zero-crossing circuit consists of Q55, Q56, Q57 and Q58. The commutator circuit consists of Q59, Q60, C58, C59, Z54 and Q61.

During either the positive or negative half-cycles of the output voltage from the mixing transformer, Q55 or Q57 transistors are driven into saturation by the output of the FV transformer (T3). Transistors Q56 or Q58 conduct until capacitors C56 or C57 respectively are fully charged. While either capacitor charges, a voltage output in the form of very narrow pulse is developed across R76 and R78 resistors. This pulse triggers Q59 control switch. When transistors Q55 or Q57 are not conducting, C56 and C57 capacitors discharge respectively through D66 or D62 and the parallel combination of R73 and R74 or R69 and R70.

While Q59 is "on" its anode (TP60) is only about 0.7 volts above negative, thus turning off transistor Q62 to allow capacitor C60 to start charging. However, a shorter time delay (consisting of R84, capacitor C59 and the reference Zener diode Z54) of 4.3 milliseconds is also started. After 4.3 milliseconds of delay, the control switch Q60 fires applying the voltage of capacitor C58 across Q59 turning it off. This raises the potential of the Q59 anode to turn on Q62 to discharge C60 before the charge reaches a value to to break down Z55 to turn on Q63. After the next zero-crossing pulse Q59 switch is turned on again, and the Q60 switch is turned off by capacitor C58. Transistor Q61 when turned on and off by the same pulse that fires the gate of Q59, discharges timing capacitor C59, when on. This starts the timing cycle with close to zero charge on the capacitor. If the zero crossing period of the FV voltage is less than 4.3 milliseconds, the Q61 transistor discharges the timing capacitor to prevent Q60 from turning on. This keeps Q59 switch on to allow C60 to charge to a value to break down Zener diode Z55 to turn on Q63. Turning on Q63 prevents Q53 of the fault detector from turning on thereby preventing Q54 from turning on and thus prevents an output from the fault detector.

2. Relay Board

With reference to Fig. 12, the ac voltage from either the second saturating transformer (SKBU-11) or the second winding of the single transformer (SKBU-1) is applied to terminals 10 and 12 of the relay board. This voltage is then applied to the phase delay circuit through a low pass filter. The low pass filter (C201, L201, C202) removes the harmonics from this voltage and applies a voltage that is essentially sinusoidal in waveform to R202 and R203 of the phase delay circuit. The phase delay circuit consists of R202, R203, C203, and S5 mounted on the front panel of the relay. By means of capacitor C203 and variable resistor S5, the voltage across terminal 4 and 2 can be made to lag the voltage across terminal 10 and 11 by a definite amount depending on the setting of S5. Each of these two voltages are applied to separate isolating transformers.

1. Undelayed voltage terminals 10 and 11 to a keying transformer (T1).
2. Delayed voltages (terminals 4 and 2) to local transformer (T2).

a. Keying Circuit

With no ac output (Ref. Fig. 8) voltage from the sequence network, base current does not flow into transistor Q103, from terminals 9 and 8 of the amplifier and keying board. The collector of Q103 is at positive potential which allows base current to flow from positive 20 volts dc to the base of Q104 through R111 and R112. This turns on Q104 to prevent base current from flowing to Q105. Since Q104 is conducting, transistor Q105 does not conduct and the collector of Q105 is held at positive potential. As a result, transistor Q105 does not conduct.

When a sinusoidal voltage is applied to the keying transformer (T1), the transformer steps up the voltage applied to terminals 9 and 8 of the amplifier and keying board. On the positive half-cycle of this voltage, terminal 8 is more positive than terminal 9 and transistor Q103 does not conduct. In turn Q104 remains conducting and Q105 does not turn on. On the negative half-cycle of sine wave voltage from the keying transformer, terminal 9 is more positive than terminal 8 and base current flows in Q103. This turns Q103 on which

removes base current to transistor Q104. Q104 stops conducting, and its collector goes to positive potential. Positive potential is thus applied to the base of Q105 through R114 and R115 to turn on Q105. Thus on alternate half-cycles of the 60-hertz voltage from the low pass filter, Q105 turns on. If the carrier control circuit operates, as seen in Fig. 18, turning Q105 on and off every half cycle, shorts the input to the TC carrier set every other half cycle so that carrier is transmitted on the half cycle when Q105 is not conducting.

b. Signal Squelch Circuit

When an input is removed from terminal 7 of the amplifier and keying board, positive potential is removed from the base of Q101. Q101 turns off and a discharge path from C101 is provided through R102 and transistor Q1 of the protective relay board. Q101 stops conducting and a positive potential is applied to capacitor C102 of the amplifier and keying board. Ten milliseconds after the input to terminal 7, C102 charges sufficiently to break down Zener diode, Z102. This turns on Q102, which shorts the input of the TC carrier set to negative to prevent the transmission of carrier.

Upon removal of the input to terminal 7 of the amplifier and keying board, positive potential is applied to capacitor, C101, 150 milliseconds later C101 charges sufficiently to break down Zener diode Z101. This turns on Q101 to provide a discharge path for C102 through R106 and Q101 to negative. In turn, Q102 stops conducting to remove the short from the input of the TC carrier set.

c. Local Squaring Amplifier

The delayed voltage from the local transformer (T2) is applied to the local squaring amplifier (Q106, Q107, Q108) and a loading circuit on the amplifier and keying board of the relay. With reference to the local squaring amplifier of Fig. 8, with no ac input voltage, Q106 is not conducting and the collector of Q106 is at positive potential. This applies base current to transistor Q107 through R120 and R121 such that Q107 is turned on. This allows base current to flow in Q108. Q108 turns on to apply positive potential across R125, (blocking condition).

With the application of a sine wave voltage to terminal 6 and 19 of the amplifier and keying board, on the negative half-cycle of the voltage, the base of transistor Q106 is more positive than the emitter and Q106 (amplifier 1) conducts. On the positive half-cycle of the ac voltage, Q106 is turned off and current flows into the loading circuit. Therefore, Q106 is conducting on the negative half-cycle of ac voltage. Turning Q106 on and turns off transistor Q107. Transistor Q107 stops conducting and its collector goes to a positive potential which turns off Q108. Thus the output of the squaring amplifier is a square wave voltage ranging from 0 volts dc to 20 volts dc depending upon the polarity of the voltage from the phase delay circuit.

D. Remote Squaring Amplifier

The remote squaring amplifier consists of transistors Q109 and Q113 of the amplifier and keying board, (Ref. Fig. 8).

Under non-fault conditions, carrier is not transmitted from the remote carrier set. As a result the base of Q113 is more negative than its emitter, and Q113 conducts. This applies positive 20 volts to the base of Q109 to prevent it from turning on. Hence, Q109 is not conducting and negative voltage (with ref. to +20 volts) appears across R129, (unblocking condition).

Under fault conditions, the remote TC carrier set is keyed on and off as described under the Keying Circuit. This signal is received at the local TC carrier receiver and is converted to a square wave voltage varying in magnitude from 45 volts to 0 volt. This voltage is applied to the base of Q113 through R141 and D110. Upon application of positive 45 volts d-c to the base of Q113, the potential of the base is greater than that of the emitter and Q113 stops conducting. This removes positive potential from R139 and allows the base of Q109 to become nega-

tive with respect to the emitter. Q109 turns on to apply positive voltage (with ref. to neg.) to R129. Hence, the voltage across R129 is a square wave voltage that is developed by the voltage received from the T_C receiver.

3. Arming Board (Ref. Fig. 6)

The phase relationship of the outputs of the local and remote squaring amplifiers are compared by AND 1 of the Arming Board. If the local and remote signals are out of phase with respect to each other, the AND circuit will provide one input to AND number 3 which will activate the 4/0 timer.

a. Internal Fault Conditions

With reference to the logic drawing that applies to the relay, the output voltages of the sequence filter of one relay are 180 degrees out-of-phase with respect to its load current condition. This changes the polarity of Amplifier #1 such that its output is in phase with the remote signal. This means that AND 1 has a half-cycle of negative voltage. This voltage is applied to AND 3 of the arming board to set-up one condition (negative voltage from OR-1) for activating the AND. The second condition to activate AND-3 is provided by arming the relay.

In either Fig. 19, 20, or 27, arming occurs through either the operation of the distance fault detectors or the operation of fault detector (FD2) of either the SKBU-11 or SKBU-1 relays. The operation of either fault detector will apply a voltage to OR 2 of the arming board. The output voltage from OR 2 applies a positive input to the trip AND of the output board through ARM and a negative signal into AND 3 of the arming board. AND 3 is activated and starts the 4/0 timer. Four milliseconds later, a negative input is applied to the trip AND of the output board. Since the three conditions of trip (a negative input from the 4/0 timer, not a negative input from the ARM logic, and a positive signal from the 22/0 timer) is fulfilled, a trip output is obtained from the relay.

b. External Fault

Under external fault conditions, the square wave voltage from the remote squaring amplifier and the square wave voltage from the local squaring amplifier are out-of-phase such that zero output is being obtained from AND 1 of the arming board. As a result, the output of AND 1 is zero, and AND 3 cannot be activated. This blocks AND 3 and the 4/0 timer is not energized.

With fault detector operation, an input is applied to OR-2 and OR-3 of the arming board. OR-2 will provide a positive input (not a negative input) to the trip AND but tripping will not occur since the 4/0 timer is not providing a negative input to the Trip AND. The fault detector input to OR-3 will provide an input to a 1/100 timer on the Output Board. The timer negates the signal to provide a negative input to the transient block AND. With the application of the input from the 0/100 timer the three conditions of transient block are fulfilled — not an input from the Transient UNBLOCK circuit, not a negative input from the Trip AND, and a negative input from the 0/100 timer. Twenty two milliseconds later the 22/0 timer of the transient block circuit times out to remove the positive input to the TRIP AND. The TRIP AND is thus desensitized to prevent undesirable operation during transients associated with power reversals on the protective line or at the clearing of an external fault.

c. Sequential Faults

If the above external fault is followed by an internal fault before the external fault is cleared, the transient unblock circuit is set up to remove the transient blocking input to the TRIP AND. For the internal fault, the square wave pulses on AND-1 of the arming board will reverse such that a square-wave output is obtained from AND-1. This output energizes OR-1. The negative signal provides the second input to AND-3 which:

1. Provides an input to the 4/0 timer which times out to apply a negative input to the TRIP AND.

2. Applies a square wave input every other half cycle to the AND of the transient unblock circuit to fulfill the requirements to obtain an output from the transient unblock circuit.

As a result, an input is applied to the unblock timer every other half cycle. Twenty-five milliseconds later, capacitor C301 (Ref.Fig.10) will charge such that the unblock timer will operate to apply a voltage to the block AND circuit. This resets the 22/0 block timer, and removes the input to the AND of the unblock timer to reset the unblock circuit. The required three inputs are thus applied to the Trip AND and a trip output is obtained from the relay.

4. Supervision Board (Ref. Fig. 14)

The circuits on the supervision board include the auxiliary functions of the relay, and they include a fault detector (FD-1), carrier control circuit and timer circuit.

a. Fault Detector 1 (FD-1) (Q161, Q162)

Under normal conditions, transistor Q161, has no base "signal" and is turned off. The collector of Q161 is at positive potential and no collector current flows. This keeps transistor Q162 in a non-conducting state, equivalent to an open circuit.

When a fault causes the dc input voltage from the polyphase rectifier (of the FD Board) across S3 and R185 to exceed the 6.8 volt rating of Zener diode Z156, a positive input is applied to the base of Q161 base causing it to conduct. In turn, Q162 is switched to conduction, thus "closing" the fault detector. When the fault detector operates, a positive input is applied to the carrier control circuit. The feedback path of resistors R191 and S4 increase the voltage to Z156 after the fault detector operates. This seals in the fault detector and allows the fault detector to drop out at a high dropout ratio when the ac is reduced.

B. Carrier Control Circuit (Q163, Q164)

Under normal conditions Q163 is not conducting and base drive is supplied to Q164. As shown in Fig. 18, the emitter of Q164 is connected to negative dc. The collector of Q164 is connected to positive 45 volts dc of the TC set through R142 of the amplifier and keying board. Normally Q164 is conducting. When either FD1 or the distance carrier start relay operate, base drive is supplied to Q163. Q163 turns on and shorts the base of Q164 to negative. Q164 turns off to raise the potential of point A of Fig. 18. This starts the transmission of carrier.

c. Arming Delay By Distance Fault Detectors (8/0 Timer) (Q151, C151, Z151, Q152, Q153)

The distance supervision arming is delayed by 8 milliseconds to allow time for the AND of the arming board to respond at fault inception. Operation of the distance fault detectors will remove base current to transistor Q151. Q151 turns off, and positive potential is applied to capacitor C151. Eight milliseconds later the voltage on C151 reaches a value to break down Zener diode Z151. This turns on Q152, which connects the base of Q153 to negative through resistor, R158. Q153 turns on to apply positive potential to resistor R160 and terminal 13. From terminal 13 the voltage is applied to the arming board.

d. Sustained Arming Alarm (2500 Timer) (C152, Z152, Q154 to Q156)

When arming occurs, positive potential is applied to terminal 18 and capacitor C152 from terminal 15 of the arming board. Two-and-one-half seconds later, the potential on C152 breaks down the Zener diode Z152 to allow base current to flow into Q154. This turns on Q154 which turns off Q155. Turning Q154 off applies positive potential to the base of Q156 and Q156 turns off. This removes positive potential from R170 and an external alarm is energized.

CHARACTERISTICS

A. SKBU-11 Relay

Taps are available in the SKBU-11 relay to set different sensitivities of the fault detector (FD-1) to zero and negative sequence currents. These taps are as follows:

NEGATIVE SEQUENCE TAPS (I_2)

TAP SETTING	NEGATIVE SEQUENCE SENSITIVITY
A	None
B	0.4 Amperes
C	0.25 Amperes

Zero Sequence Taps (I_0)

TAP SETTING	ZERO SEQUENCE SENSITIVITY
F	None
G	0.2 Amperes
H	0.1 Amperes

The second fault detector unit (FD-2) which supervises arming is adjusted to pick up at a current 125 per cent greater than FD-1. By means of the S_1 adjustment, the pick up of FD-2 can be increased to 250 per cent greater than FD-1.

The positive sequence response of the fault detector is greater than 7 amperes.

B. SKBU-1 Relay

Taps are available in the relay to set the sensitivity of FD-1 to different combinations of positive, negative and zero sequence components of the line current. The T taps on the left hand tap plate indicate the balanced three phase amperes which will operate the fault detector FD-1. These taps are as follows:

3, 4, 5, 6, 7, 8 and 10

The second fault detector unit (FD-2) which supervises arming is adjusted to pickup at a current 125 percent greater than FD-1. By means of the S_1 adjustment, the pickup of FD-2 can be increased to 250 percent greater than FD-1.

For distance fault detector applications, the user should reset the SKBU-1 fault detector for a pick-up of twice the tap value by means of the S_3 setting.

Positive and Negative Sequence Current - R1 Taps

The upper half of the right hand tap plate or R1 taps changes the number of turns on the third winding of the mutual reactor. This reproportions the components of the sequence filter which changes the positive and negative sequence sensitivity of the fault detector. Operation of the fault detector (FD-1) with the various taps is given in the following table:

TABLE I

COMB.	SEQUENCE COMPONENTS IN NETWORK OUTPUT	TAPS ON RIGHT HAND TAP BLOCK		FAULT DETECTOR (FD-1) PICK-UP †	
		R_1	R_0*	3¢ FAULT	¢¢ FAULT θ
1	Pos., Neg., Zero	C	G or H	Tap Value	86% Tap Value (53% on BC Fault)
2	Pos., Neg., Zero	B	G or H	2 x Tap Value	90% Tap Value (65% on BC Fault
3	Neg., Zero	A	G or H	—	100% Tap Value

— Taps F, G and H are zero-sequence taps for adjusting ground fault sensitivity, See section on zero-sequence current tap.

† — When taps A and 3, or B and 3 are used, FD-1 will pickup 10 to 15 per cent higher than the above values because of the variation in self-impedance of the sequence network and the saturating transformer.

θ — Fault detector FD-2 is set to pick-up at 125 per cent of FD-1 for a two terminal line, or 250 per cent of FD-1 for a three terminal line.

Zero Sequence Current – R_0 Taps

The lower half of the right-hand tap plate (R_0 taps) is for setting the response of the relay to

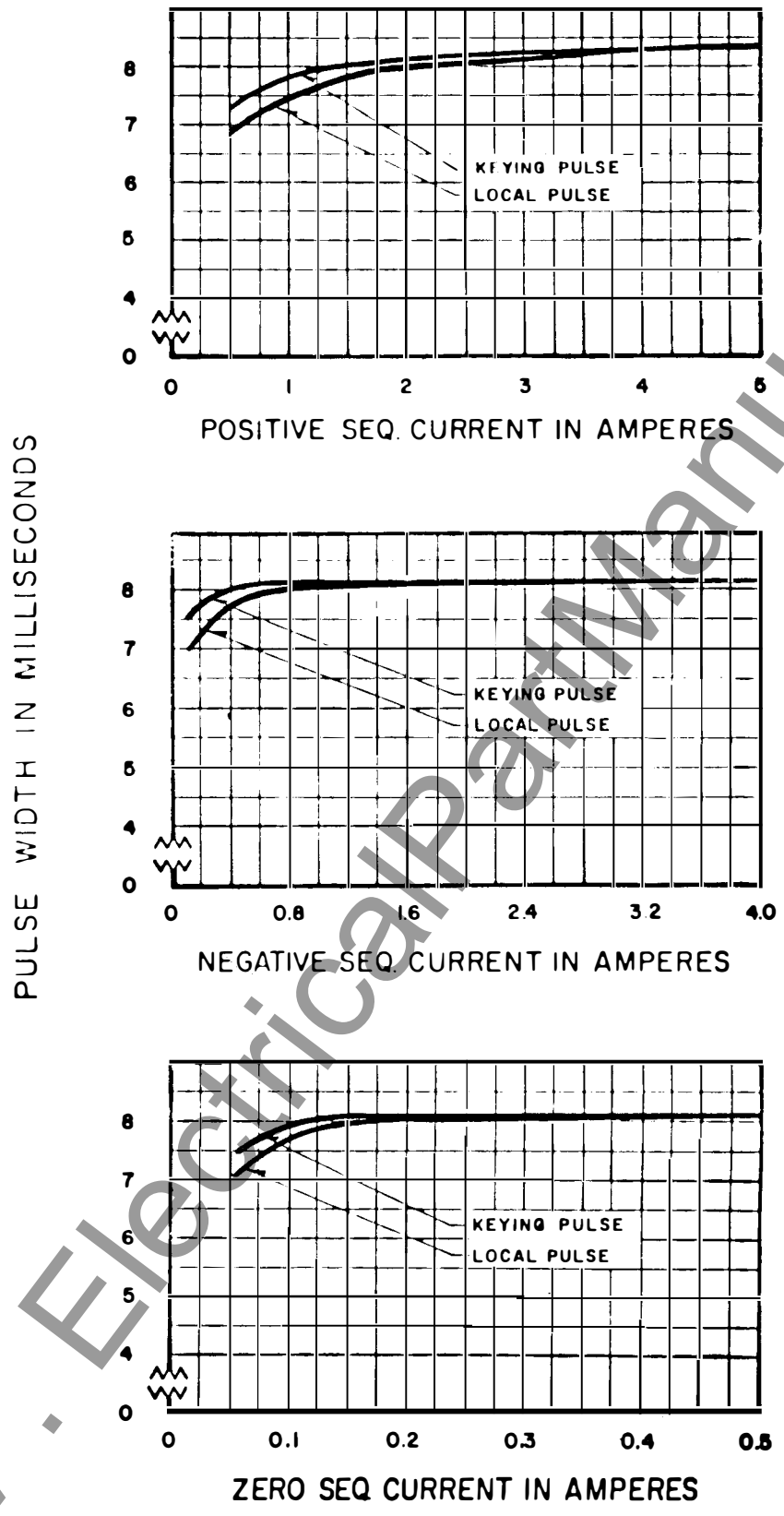


Fig. 23. Width of Keying Pulses at Different Current Levels of SKBU-11 Relay. (Phase Delay Setting S5 at minimum.)

ENERGY REQUIREMENTS

A. SKBU-11 Relay

Burdens measured at a balanced three-phase current of five amperes. (Independent of tap setting).

PHASE A		PHASE B		PHASE C	
VA	ANGLE	VA	ANGLE	VA	ANGLE
8.3	106°	2.2	50°	46	0°

Burden measured at a single-phase to neutral current of five amperes.

RELAY TAPS	PHASE A		PHASE B		PHASE C	
	VA	ANGLE	VA	ANGLE	VA	ANGLE
C-H	11.7	2.0°	9.7	1.8°	44.0	2.2°
B-H	11.4	2.0°	10.3	1.8°	46.0	2.2°
A-H	11.1	2.0°	11.2	1.8°	48.0	2.2°
C-G	8.8	2.0°	7.0	1.8°	42.0	2.2°
B-G	8.7	2.0°	7.5	1.8°	43.5	2.2°
A-G	7.8	2.0°	8.5	1.8°	45.0	2.2°
C-F	6.7	2.0°	7.5	1.8°	42.0	2.2°
B-F	6.5	2.0°	7.2	1.8°	42.0	2.2°
A-F	5.8	2.0°	6.6	1.8°	43.0	2.2°

B. SKBU-1 Relay

Burdens measured at a balanced three-phase current of five amperes.

RELAY TAPS	PHASE A		PHASE B		PHASE C	
	VA	ANGLE	VA	ANGLE	VA	ANGLE
A-F-3	2.4	5°	0.6	0°	2.5	50°
A-H-10	3.25	0°	0.8	100°	1.28	55°
B-F-3	2.3	0°	0.63	0°	2.45	55°
B-H-10	4.95	0°	2.35	90°	0.3	60°
C-F-3	2.32	0°	0.78	0°	2.36	50°
C-H-10	6.35	342°	3.83	80°	1.98	185°

Burdens measured at a single-phase to neutral current of five amperes.

RELAY TAPS	PHASE A		PHASE B		PHASE C	
	VA	ANGLE	VA	ANGLE	VA	ANGLE
A-F-3	2.47	0°	2.1	10°	1.97	20°
A-H-10	7.3	60°	12.5	53°	6.7	26°
B-F-3	2.45	0°	2.09	15°	2.07	10°
B-H-10	16.8	55°	22.0	50°	12.3	38°
C-F-3	2.49	0°	1.99	15°	2.11	15°
C-H-10	31.2	41°	36.0	38°	23.6	35°

The angles above are the degrees by which the current lags its respective voltage.

CONTINUOUS RATINGS: The continuous rating of the SKBU-1 is 10 amperes and the continuous rating of the SKBU-11 is 7 amperes. The two second overload rating of the SKBU-1 is 150 amp. phase and 125 amp. ground while the two second rating of the SKBU-11 is 125 amp. phase and ground.

SETTINGS

If settings in between taps are desired, the tap screw should be set in the next lowest tap. S_1 and S_3 should then be adjusted for the desired pickup value. Dropout should be readjusted by means of S_2 and S_4.

A. SKBU-11

The SKBU-11 relay has separate tap plates for adjustment of the zero and negative sequence sensitivity of the fault detector (FD-1). The fault detector tap markings and pickup are:

Negative Sequence Sensitivity (I_2)

A. None

B 0.4 Amperes

C. 0.25 Amperes

Zero Sequence Sensitivity (I_0)

F. None

G. 0.2 Amperes

H. 0.1 Amperes

Two tap plates are provided: one for I_2 and the other one for I_0.

Tap A should not be used in service since this would prevent fault detector operation for phase-to-phase faults. However, tap F may be used with either B or C since negative sequence current flows for both phase-to-phase and ground faults.

The recommended settings are tap B or C as needed for the required sensitivity, and tap F. Taps G and H have been provided for applications where the negative-sequence load flow due to series impedance unbalance may be high enough to operate FD with a tap C setting. In this case, set in tap B and in tap G or H. It is not intended that taps C and H be used simultaneously due to the possibility of cancellation of the negative-and zero-sequence effects on ground faults. With a tap B setting, a tap H setting is preferred.

To summarize, the recommended setting combinations in the order of preference are:

COMBINATION	I_2 TAP	I_0 TAP
1	C	F
2	B	F
3	B	H
4	B	G

For a long two-terminal line, FD2 should be set at 250 per cent of FD1. As shipped from the factory, FD2 is set to pickup at 125 per cent.

B. SKBU-1 Relay

The SKBU-1 relay has separate tap plates for adjustment of the phase and ground fault sensitivities and the sequence components included in the network output. The method of determining the correct taps for a given installation is discussed in the following paragraphs.

Setting Principles

Tap C provides the best balance between three phase and phase-to-phase fault sensitivity. Always use this tap where distance fault detector supervision is used. Where only the SKBU-1 fault detector is used and where the full load current (maximum through any terminal) is approximately five amperes or more, tap B will provide increased phase-to-phase fault sensitivity with little or no sacrifice in three phase fault sensitivity. For example, if a left-hand tap (T) of 6 is needed with tap C (6C), then use a 3B setting instead.

NOTE: From Table I, pickup will be 4.15 amp. for tap 3B and 5.40 amp. for tap 6C for ϕa to ϕb fault, 3ϕ pickup is 6 amperes on tap 6C and 6.1 amp. on 3B.

Use tap A only where satisfactory unbalanced fault sensitivity cannot otherwise be obtained and where other protection is available for three phase faults, since with Tap A no three phase fault protection is available.

In all cases provide identical response at all stations to insure proper phase comparison and adequate keying for any fault detected by remote-end relays. To accomplish this, the letter taps (A, B, C, F, G, H) should be identical at all stations. Also, the taps should be identical with identical CT ratios, or inversely proportional to CT ratios where different.

After selecting tap C or B, pick the T tap to allow reset of the fault detector in the presence of load flow. That is, fault detector pick-up should be at least 111 per cent of full load current (maximum through any terminal).

Now select tap G or H for desired ground-fault sensitivity.

For distance fault detector applications, set 3C to provide the maximum sequence-filter voltage for the squaring amplifiers. The SKBU-1 current fault detector FD-2 is then independently desensitized (by adjustment of S1 and S2 settings) to permit reset in the presence of full-load current. Phase faults which do not operate the SKBU-1 fault detector will be detected by the supplementary distance fault detectors.

Examples of SKBU-1, Relay Settings

CASE I

Assume a two-terminal line with current transformers rated at 400/5 at both terminals. Also assume that full load current is 300 amperes, and that on minimum internal phase-to-phase faults, 2000 amperes is fed in from one end and 600 amperes from the other end. Further assume that on minimum internal ground faults, 400 amperes is fed in from one end, and 100 amperes from the other end.

a. Positive Sequence Current Tap

Secondary Values:

Load Current $= 300 \times \frac{5}{400} = 3.75$ amperes (1)

Minimum Phase-to-Phase Fault Currents:

$600 \times \frac{5}{400} = 7.5$ amperes (2)

Fault detector FD-1 setting (three phase) must be at least:

$\frac{3.75}{0.90} = 4.18$ amperes (0.90 is dropout ratio of FD-1. Setting will insure that the fault detector will reset on load current) (3)

In order to complete the trip circuit on a 7.5 ampere phase-to-phase fault, the fault detector FD-1 setting from Table I must not be more than: (based on a three phase fault:

$7.5 \times \frac{1}{0.86} \times \frac{1}{1.25} = 6.93$ amperes (4)

$1.25 = \frac{\text{FD-2 Pickup}}{\text{FD-1 Pickup}}$

Sequence Combination Tap

From a comparison of (3) and (4) above, it is evident that the fault detector can be set to trip under minimum phase fault condition yet not operate under maximum load. In this case, tap C would be used (see Table I, Comb. 1) as there is sufficient difference between maximum load and minimum fault to use the full three-phase sensitivity. Current tap 6 would be used in preference to tap 5 to allow for occurrence of higher load current.

Zero Sequence Tap

Secondary Value:

$100 \times \frac{5}{400} = 1.25$ amperes minimum ground fault current.

With T tap 6 and R1 tap, the fault detector pickup currents for ground faults (See Table II) are as follows:

Tap G $.25 \times 6 = 1.5$ ampere (FD-1)
Minimum Trip $= 1.25 \times 1.5$ ampere $= 1.8$ amp. (FD-2)

Tap H $.12 \times 6 = 0.72$ ampere (FD-1)
Minimum Trip $= 1.25 \times 0.75 = 0.90$ ampere (FD-2)

From the above, tap H would be used to trip for a minimum ground fault of 1.25 amperes.

CASE II

Assume the same fault currents as in Case I, but a maximum load current of 550 amperes. In this example, with the same sequence combination as in Case I, the fault detectors cannot be set to trip on the minimum internal three-phase fault, yet remain inoperative on load current. (Compare equations (5) and (6).) However, by connecting the network per combination 2 on Table I, the relay can be set to trip on minimum phase-to-phase fault, although it will have only half the sensitivity to three-phase faults. This will allow operation at maximum load without picking up the fault detector, and provide high speed relaying of all except light three-phase faults.

In order to complete the trip circuit on a 7.5 ampere phase-to-phase fault, the fault detector tap must now be not more than:

$7.5 \times \frac{1}{1.25} \times \frac{1}{.90} = 6.67$ amperes (5)

To be sure the fault detector FD-1 will reset after a fault, the minimum tap setting is determined as follows:

Load Current $= 550 \times \frac{5}{400} = 6.9$ amperes (6)

$\frac{6.9}{0.90} = 7.7$ amps. (.90 is dropout ratio of FD-1) (7)

Since from Table I, Comb. 2, the fault detector pickup current for three-phase faults is twice tap value, half the above value (Eq. 7) should be used in determining the minimum three-phase tap.

$\frac{7.7}{2} = 3.86$ (8)

From a comparison of (5) and (8) above, tap 5 or 6 could be used. (Continuous load current rating of relay is 10 amperes).

With the three-phase tap 5 in use, the fault detector pickup current for ground faults will be as follows:

Tap G $= .2 \times 5 = 1.0$ ampere (FD-1)
Minimum Trip $= 1.0 \times 1.25 = 1.25$ ampere (FD-2)

Tap H = .1 × 5 = 0.5 ampere (FD-1)
Minimum Trip = 1.25 × 0.5a. = 0.63 ampere (FD-2)

Therefore, tap H would be used to trip the minimum ground fault of 1.25 ampere with a margin of safety.

INSTALLATION

The relays should be mounted on switchboard panels or their equivalent in a location free from dirt, moisture, excessive vibration and heat. The maximum ambient temperature around the chassis must not exceed 55°C. Mount the relay by means of the four slotted holes on the front of the case. Additional support should be provided toward the rear of the relay in addition to the front panel mounting. This will protect against warping of the front panel due to the extended weight within the relay case. Ground relay chassis with No. 12 AWG copper wire to grounding post.

ADJUSTMENTS AND MAINTENANCE

NOTE: The phase comparison relay is normally supplied as part of a relaying system, and its calibration should be checked after the system has been installed and interconnected. Details are given in the instructions of the assembly. The assembly instructions and not the following instruction should be followed when the relay is received as an integral part of the relaying system.

In those cases where the relay is not part of a relaying system, the following procedure can be followed to verify that the circuits of the relay are functioning properly.

TEST EQUIPMENT

1. Oscilloscope
2. AC Current Source
3. Electronic Timer
4. AC Voltmeter
5. DC Voltmeter

ACCEPTANCE TEST

Connect the relay to the test circuit of Fig. 24 which represents the TC carrier channel for test purposes. On SKBU-11 relays, jumper terminals 2 to 4 to 6 to 8.

If the test fixture is not available, the remote pulses can be obtained from the SKBU keying circuit. This is accomplished by jumpering various circuits of the relay together as follows: (Note: These instructions apply where no external connections are made to the J101 block).

1. Apply either 48 volts dc or 45 volts dc to J101-2 (pos.) and J101-5 (neg.). An alternate connection is to X_1 and X_4. Also connect positive 45 volts dc to either X_3 or J101-3.
2. Jumper J101-5 to J101-6. An alternate connection is terminal 3 to terminal 8 on the supervision board. This connects the carrier control to negative.
3. Jumper J101-13 to J101-14. An alternate connection is terminal 6 of the supervision board to terminal 15 of the amplifier and keying board. This connects the carrier control circuit to positive 45 volts dc through R142 of the amplifier and keying board.
4. Jumper J101-25 to J101-7. An alternate connection is terminal 12 to terminal 17 of the amplifier and keying board. This connects the keying circuit to the remote squaring amplifier.
5. Short resistor R141 on the amplifier and keying board. This is necessary to allow the remote squaring amplifier to work from a lower voltage input than normal. Normally 45 volts dc is applied to J101-17. In this test circuit, approximately 24 volts dc is applied to J101-17.
6. Connect one pole of a DPST switch as shown in Fig. 29. Add diodes as shown. This is switch L of the following tests and enables internal-external fault tests to be performed on the relay. External fault position is with the switch closed. Internal fault position is with the switch open. This switch removes a stage from the remote squaring amplifier to reverse the polarity of the remote pulses.

With the jumpers added as per the above information, the transistor circuits are connected together as shown in figure 29.

If the above connections are utilized to test the relay, the reference to closing switches A, B, C, and D should be ignored.

The following tests are with reference to the relay as received. If a recalibration of the circuits is desired, the recalibration can best be obtained by setting S1, S2, S4 and S5 to counterclockwise limit, S6, S3 and S7 to clockwise limit, and R316 on output board to the middle of its range.

1. FD-1 Pickup and Dropout

a. Set relay on taps C and H. Set SKBU-1 T tap 5.

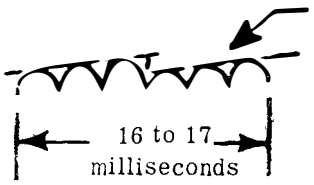
b. Connect a high resistance dc voltmeter across X_{16} and X_4 (neg.).

c. Apply 60 hertz current to terminal 1 and 3 of the relay. Gradually increase the current until the voltmeter changes reading from approximately zero volts to approximately 20 volts. This is the operating current of FD-1 and should be 0.433 ±5% amperes for SKBU-11 relay and 4.33 ±5% amperes for SKBU-1 relay.

d. Gradually lower ac test current until the dc voltmeter drops to approximately zero volts. This is the dropout current of FD-1 and should occur at .389 to .395 amperes for SKBU-11 and 3.89 to 3.95 amperes for SKBU-1.

e. Adjustment of pickup and dropout is made by S3 and S4 respectively.

f. If the output of the fault detector is erratic at pickup, R35 on the fault detector should be adjusted such that the following waveform should appear across X_{15} to X_4.



peaks should be nearly equal or, if not, rising slightly to the right.

2. FD-2 Pickup and Dropout

a. With relay set on taps I_2 = C, I_0 = H, connect a high resistance voltmeter to X_{13} and X_4 (neg.).

b. With a 60 hertz test current connected to terminal 1 and 3 of the relay, gradually increase the current until the voltmeter charges reading from approximately zero volts to approximately 20 volts. This is the operating current of FD-2 and should be between 0.514 to 0.568 amperes for SKBU-11 and 5.14 to 5.68 amperes for SKBU-1.

c. Gradually lower the ac test current until the dc voltmeter drops to approximately zero volts. This is the dropout current of FD-2 and should occur at between 0.461 to 0.509 amperes for SKBU-11 and 4.61 to 5.09 amperes for SKBU-1.

3. Check of Local Squaring Amplifiers

a. With all switches of test circuit open, apply 0.6 to 0.8 amperes ac to terminals 1 and 3 of the SKBU-11 relay, or 6 to 8 amperes ac to terminals 1 and 3 of the SKBU-1 relay.

b. Place scope probe across X12 and X4 (grd). A square wave of voltage should appear across X12 and X4 as shown in Fig. 25.

4. Check of Keying Circuit

a. With all switches of test circuit open and 0.6 to 0.8 amperes ac applied to terminal 1 and 3 of the SKBU-11 relay, with scope check voltage across X14 and X4 (grd). (This voltage should be checked with 6.0 to 8.0 amperes into terminals 1 and 3 of SKBU-1 relay).

b. Waveform shown in Fig. 25 should be observed.

5. Check of Remote Squaring Amplifiers

a. Close switches A, B and C of test fixture.

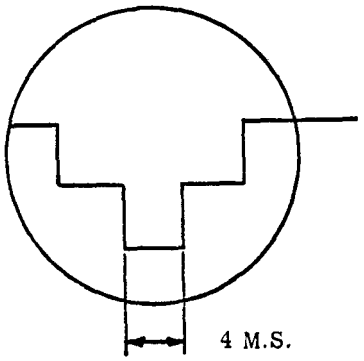
b. Apply 0.6 to 0.8 amperes ac to terminals 1 and 3 of the SKBU-11 relay, or 6 to 8 amperes ac to same terminals for SKBU-1 relay.

c. Using scope with grd. lead on X4, check waveshape of voltage across X9. Waveforms of Fig. 25 should be observed.

6. Setting of S5 and S6

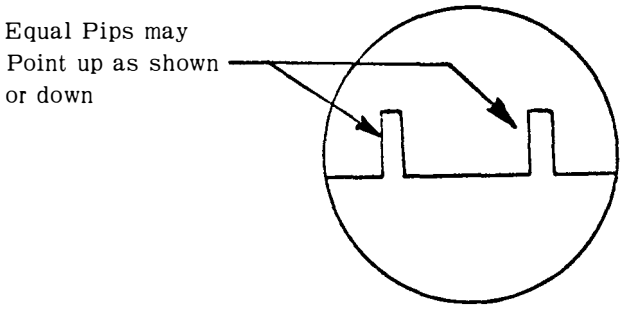
a. With S5 set to minimum resistance (fully counter-clockwise) and S6 to maximum resistance (fully clockwise), (set L on external fault) close switches A, B and C of the test circuit. Apply 0.6 to 0.8 amperes ac to terminals 1 and 3 of the SKBU-11 relay or 6 to 8 amperes ac to same terminals of SKBU-1 relay. Open and close switch D.

b. Place scope across X10 and X4 (grd). Adjust S5 until following waveform appears on scope.



c. Adjust S6 until the relay trips. This sets the triggering of the Trip AND after a 4 millisecond delay.

d. Slowly change S5 to obtain the following waveform. This will be with S5 at or near minimum resistance.



e. Close and open switch D, and slowly turn S5 until the relay operates. Waveform should be the same as in step 6. If necessary, readjust S6 and repeat step d and e.

7. Transient Blocking Delay (22/0 and 0/100 Timer)

a. Connect electronic timer stop to X7 and X4 (grd). Set timer stop on negative going pulse. Relay not to be energized with ac current.

b. Connect timer start to X18. Set timer start to positive going pulse.

c. Close switch A and switch 31. Close switch 32. (Represents 20 volt input to terminals 3 and 19 of protective relay board). Timer should start and should stop between 22 and 25 milliseconds. If necessary, adjust R316 on output board to obtain timing.

d. Set timer start on a negative pulse and timer stop on a positive pulse.

e. Open switch 32. (Represents removal of 20 volt input to terminal 5 of the protective relay board) Timer should start, and should stop after a time delay of 80 to 135 milliseconds.

8. 8/0 Timer Distance Fault Detector

a. Connect timer start to terminal 16 of supervision board. Set timer start on positive pulse. Connect timer stop to X18 and X4 (comm). Set timer stop on positive pulse.

b. Close switch 31. Close switch 32. (represents 20 volt input to terminals 3 and 19 of protective relay board). Timer should start and should stop after 6 to 8 milliseconds.

9. Sustained Arming Alarm (2.5 Seconds)

a. With electronic timer stop connected to X17 and X4 (grd), set timer stop on negative going pulse.

b. Connect timer start to X18, Set timer start on positive pulse.

c. Close switch 31 and then switch 32. (Represents 20 volt input to terminals 3 and 19 of Protective relay board). Timer will start and should stop after 2.3 to 2.7 seconds.

d. Open switch 31 and 32.

10. Check of Transient Unblocking Circuit

a. With electronic timer stop connected to X7 and X4 (grd), set timer stop on positive going pulse.

b. Connect timer start to timer start contacts of switch A. Set timer start on negative pulse. If DPST switch "L" of test circuit of Fig. 29 is used, connect second pole of switch to +20 volts to trigger timer.

c. Close switch A and apply 0.6 to 0.8 amperes ac into terminal 1 and 3 of the SKBU-11 relay. (6 to 8 amperes into 1 and 3 of SKBU-1)

d. Open switch A, timer should start and should stop after a time delay. Time should be 22 to 28 milliseconds. Recheck approximately 10 times in order to take an average of 10 readings. To recheck time, it will be necessary to close SW-A and reset relay with SW-D If test circuit of Fig. 29 is used, close switch "L" to internal fault position. Timer should start and stop after a time delay of 22 to 28 milliseconds. Take average of 10 readings.

11. Recheck steps 6, 7 and 10. Readjust S6, R316, and S7 if necessary.

12. Signal Squelch Time (10/150)

a. Connect timer stop to X14 and X4 (grd). Open switch C.

b. Connect timer start to switch 28. Set timer start on positive pulse. Connect timer stop on positive pulse.

c. Close switch 28. Timer will start and will stop after a 8 to 12 millisecond delay.

d. Set timer stop on negative pulse, and timer start to negative pulse.

e. Open switch 28. Timer should start and stop after a time delay of 125 to 185 milliseconds.

13. Check of Frequency Verifier

a. Open all switches of test circuit.

b. Connect scope across TP60 and terminal 8 of the FD board.

c. Apply 0.6 to 0.8 amperes to terminal 1 and 3 of SKBU-11 relay. (Apply 6.0 to 8.0 amperes to terminal 1 and 3 of SKBU-1 relay)

d. Waveform of Fig. 26 should be observed.

TROUBLE SHOOTING PROCEDURE

To trouble shoot the equipment, the logic diagram voltages of Fig. 25 should be used to isolate the circuit that is not performing correctly. The schematic of the individual board, and the voltages of Table III should then be used to isolate the faulty component.

RENEWAL PARTS

Repair work can be done most satisfactorily at the factory. However, interchangeable parts can be furnished to the customers who are equipped for doing the repair work. When ordering parts, always give the complete nameplate data. For components mounted on the printed circuit board, give circuit symbol and the electrical value (ohms, mfd., etc.) and component style number.

TABLE III

VOLTAGE MEASUREMENTS ON PRINTED CIRCUIT BOARDS

FAULT DETECTOR BOARD

Test Point	$I_{a.c.}$ = 0	$I_{a.c.}$ = Pickup of FD
TP54	6.5 V. d.c.	less than 1
TP55	less than 1	4.5 V. d.c.
TP56	less than 1	18 to 20 V. d.c.
Term. 2	less than 1	8.6 V. d.c.
51-52	0	7.4 volts a.c. (Approx.)
52-53	0	7.5 volts a.c. (Approx.)
53-51	0	7.4 volts a.c. (Approx.)
Term. 5-6	0	15 volts a.c. (Approx.)
TP 57	18 volts	
TP 58	18 volts	
TP 59	less than 1	Pulses See Fig. 26 for
TP 60	20 volts	Waveform
TP 61	18 volts	
TP 62	less than 1	

SUPERVISION BOARD

Test Point	Normal Condition	Abnormal Condition
Term. 16	12	less than 1 with DFD ▲ Operation
TP151	less than 1	7 with DFD Operation
TP152	20	less than 1 with DFD Operation
Term. 13	less than 1	20
Term. 18	less than 1	15 with sustained arming
TP153	15	less than 1 with sustained arming
TP154	less than 1	20 with sustained arming
Term. 19	20	less than 1 with sustained arming
Term. 10	less than 1	6.8 volts d.c.
TP158	20	less than 1
Term. 1	less than 1	20
Term. 15	6	20 ▲DFD = distance fault
Term. 6	less than 1	20 detector

AMPLIFIER AND KEYING

Test Point	Normal ($I_{a.c.}$ = 0)	Serviceable Channel ● ▲ Abnormal or I_{AC} = Pickup of FD
Term. 7	18	● less than 1 breaker failure or trip
TP101	less than 1	● 8.5 breaker failure or trip
Term. 10	less than 1	● less than 1 breaker failure or trip
TP102	5 Vdc	▲ 4.3 V pulses
Term. 13	less than 1	▲ ≠ 6 volt pulses
Term. 12	less than 1	▲ ≠ 20 volt pulses

AMPLIFIER AND KEYING (Continued)

Test Point	Normal ($I_{a.c.}$ = 0)	Serviceable Channel Abnormal or I_{AC} = Pickup of FD
TP103	5 Vdc	▲ 5 volt pulses
TP104	less than 1	▲ 16 volt pulses
Term. 11	20 Vdc	▲ 20 volt pulses
Term. 2	0 V	▲ 20 volt pulses
Term. 18	20 V	▲ 6 volt pulses (Ref. +20V)
Term. 17	0 Volts	▲ 45 volt pulses

≠ Non-squelch condition
● Abnormal
▲ I_{ac} = FD pickup
⋈ Terminal 10 and 12 connected together.

ARMING BOARD

Test Point	External Fault	Internal Fault
TP252	≠ less than 1	10 V pulses
Term. 3	≠ 10 volts	10 V pulses
TP254	≠ less than 1	20 V pulses
TP255	≠ 20 volts	20 V pulses
# TP256	less than 1	less than 1
# Term. 19	18 volts	18 volts

≠ Very narrow pulses would be observed on scope.
With I_{ac} = 0 (Unarmed condition)
TP256 – 6 volts, Term. 19 – 0 volts.

OUTPUT BOARD

Test Point	Normal	Trip	Blocking
301	20	Applies to Sequential Fault	
302	0	Applies to Sequential Fault	
303	2.2	12.5	less than 1
304	less than 1	less than 10	7
Board 14	20	20	less than 1
305	18.5	7	18.5
306	0	13.5	0
307	20	less than 1	20
308	0	20	0

ELECTRICAL PARTS LIST

CIRCUIT SYMBOL	DESCRIPTION	WESTINGHOUSE STYLE NUMBER
FAULT DETECTOR BOARD Style 5312D13G01		
Capacitors		
C51	0.1 Mfd	1544920
C52-C53-C59	0.5 Mfd	187A624A11
C54-C55	1.5 Mfd	187A508H09
C56-C57	0.02 Mfd	187A624H09
C58	0.1 Mfd	187A624H01
C60	0.22 Mfd	762A703H01
Diodes		
D51 to D58-D70 to D73	1N457A	184A855H07
D59	1N645A	837A692H03
D60 to D69	1N4385	184A855H14
Transistors		
Q51-Q52-Q53-Q55-Q57-Q61-Q62-Q63	2N3417	848A851H02
Q54-Q56-Q58	2N3645	849A441H01
Switches		
Q59-Q60	2N886	185A517H03
Resistors		
R51	50 Ohms, 5W	185A209H06
R52-R68-R71	2.7K Ohms ½W	629A531H42
R53 (POT)	2.5K Ohms ½W	629A430H03
R54-R55-R58-R62-R64-R66-R84-R89-R92	10K Ohms ½W	629A531H56
R56-R60	100K Ohms ½W	184A763H75
R57	47K Ohms ½W	629A531H72
R59	56K Ohms ½W	184A763H69
R61-R87	22K Ohms ½W	629A531H64
R63	6.8K Ohms ½W	629A531H52
R65	27K Ohms ½W	629A531H66
R67	150 Ohms 3W	762A679H01
R69-R73	68K Ohms ½W	629A531H76
R70-R74-R88	39K Ohms ½W	629A531H70
R72-R75-R80	2K Ohms ½W	836A503H33
R76-R78-R90	1K Ohms ½W	629A531H32
R77	5.6K Ohms ½W	629A531H50
R79-R80	6.2K Ohms ½W	629A531H51
R81	20K Ohms ½W	629A531H63
R82	1.5K Ohms ½W	836A503H30
R83-R91	470 Ohms ½W	629A531H24
R85-R93	4.7K Ohms ½W	629A531H48

CIRCUIT SYMBOL	DESCRIPTION	WESTINGHOUSE STYLE NUMBER
FAULT DETECTOR BOARD (Continued)		
Zener Diodes		
Z51	1N1832C, 62V	184A617H06
Z52-Z55	1N957B, 6.8V	186A797H06
Z53	1N3688A, 24V	862A288H01
Z54	1N759A, 12V	837A693H01
SUPERVISION BOARD Style 5315D34G01		
Capacitor		
C151-C153-C157	0.47 Mfd	188A669H01
C152	68 Mfd	187A508H02
C154-C158	1.5 Mfd	187A508H09
Diodes		
D151-D157-D162	1N457A	184A855H07
D152-D155-D156	1N645A	837A692H03
Transistors		
Q151-Q152-Q154-Q155-Q161-Q163-Q164	2N3417	848A851H02
Q153-Q156-Q162	2N3645	849A441H01
Resistors		
R151-R158-R168-R188-R194	6.8K Ohms ½W	629A531H52
R152-R153-R157-R159-R164-R165-R167-R169-R186-R189-R191-R193-R196	10K Ohms ½W	629A531H56
R154	470 Ohms ½W	184A763H19
R166-R192	22K Ohms ½W	184A763H59
R156-R161	1K Ohms ½W	184A763H27
R160-R170-R190	82K Ohms ½W	629A531H78
R155-R162	33K Ohms ½W	184A763H63
R163	56K Ohms ½W	184A763H69
R171	150 Ohms 3W	762A679H01
R195	2.7K Ohms ½W	184A763H37
R185	47K Ohms ½W	184A763H67
Zener Diode		
Z151-Z152-Z156	1N957B, 6.8V	186A797H06
Z153	1N3688A, 24V	862A288H01
Z158	UZ5875, 75V	837A693H04

ELECTRICAL PARTS LIST (Continued)

CIRCUIT SYMBOL	DESCRIPTION	WESTINGHOUSE STYLE NUMBER
AMPLIFIER & KEYING BOARD Style 5314D77G01		
Capacitor		
C101	6.8 Mfd	184A661H21
C102	1.5 Mfd	187A509H09
Diodes		
D101-D110 to D113	1N457A	184A855H07
D102 to D105-D107 to D109	1N645A	837A692H03
Transistors		
Q101 to Q107	2N3417	848A851H02
Q108-Q109-Q113	2N3645	849A441H01
Resistors		
R101	6.8K Ohms ½W	629A531H52
R102-R106	470 Ohms ½W	184A763H19
R103	39K Ohms ½W	184A763H65
R104-R108	1K Ohms ½W	184A763H27
R105-R109-R112 to R116-R121-R122-R124-R130	10K Ohms ½W	184A763H51
R107	15K Ohms ½W	629A531H60
R110	82K Ohms ½W	629A531H78
R111-R120	33K Ohms ½W	184A763H63
R118	220K Ohms ½W	184A763H83
R119-R132	68K Ohms ½W	629A531H76
R123-R139	22K Ohms ½W	184A763H59
R125-R129	4.7K Ohms ½W	184A763H43
R126-R128	470K Ohms ½W	184A763H91
R127-R141	47K Ohms ½W	184A763H67
R140	56K Ohms ½W	184A763H69
R142	1K Ohms 5W	763A129H07
Zener Diodes		
Z101-Z102	1N957B, 6.8V	186A797H06
Z103	1N3688A, 24 V	862A288H01
Z104	1N748A 3.9V	186A797H13

CIRCUIT SYMBOL	DESCRIPTION	WESTINGHOUSE STYLE NUMBER
ARMING BOARD Style 201C170G01		
Diodes		
D255-D257-D260-D261-to D265-D267	1N457A	184A855H07
Transistors		
Q252-Q253-Q256-Q258-Q259	2N3417	848A851H02
Q257	2N3645	849A441H01
Resistors		
R255-R257-R261-R262-R265-R274-R277-R278-R280-R281-R287-R288	22K Ohms ½W	184A763H59
R260-R264-R275-R276-R282-R284-R285	10K Ohms ½W	184A763H51
R279	27K Ohms ½W	629A531H66
R283-R290	12K Ohms ½W	629A531H58
Zener Diodes		
Z251	1N3688A, 24V	862A288H01
PROTECTIVE RELAY BOARD Style 201C165G01 – 201C476G01		
Capacitors		
C1 to C4	.047 Mfd	849A437H04
Diodes		
D1 to D5-D9	1N645A	837A692H03
Transistors		
Q1 to Q6-Q9	2N3417	848A851H02
Resistors		
R1 (125 volt input)	68K 1W	187A643H71
R1 (48 volt input)	22K ½W	184A763H59

ELECTRICAL PARTS LIST (Continued)

CIRCUIT SYMBOL	DESCRIPTION	WESTINGHOUSE STYLE NUMBER
PROTECTIVE RELAY BOARD (Continued)		
Resistors (Continued)		
R2-R3-R4-R8-R9-R13-R14-R122-R23	4.7K ½W	629A531H48
R5-R10-R15-R24-R34	82K	629A531H78
R6-R21-R30-R39	27K ½W	184A763H01
R7-R11-R16-R20-R25-R29-R40	10K ½W	629A531H56
R12-R17-R26	6.8K ½W	629A531H52
R18-R19-R27-R28	22K ½W	184A763H59
Zener Diode		
Z1-Z3-Z5-Z7	1N3686B, 20V	185A212H06
Z2-Z4-Z6-Z8	1N957B, 6.8V	186A797H06
OUTPUT BOARD Style 201C025G02		
Capacitors		
C301	1.0 Mfd	837A241H15
C302-C303-C306-C309	0.22 Mfd	762A703H01
C304-C305	4.7 Mfd	184A661H12
C307-C308	500 Mmfd	187A694H03
C310	0.10 Mfd	188A669H03
C311	1.5 Mfd	187A508H09
Diodes		
D301 to D306-D308	1N457A	184A855H07
D307	1N645A	837A692H03
Transistors		
Q301-Q305-Q306-Q307-Q309	2N3645	849A441H01
Q302-Q303-Q304-Q308	2N3417	848A851H02
Resistors		
R301-R303-R304-R306-R310-R311-R314-R315-R320-R323-R324-R326-R330-R335	10K Ohms ½W	184A763H51

CIRCUIT SYMBOL	DESCRIPTION	WESTINGHOUSE STYLE NUMBER
OUTPUT BOARD (Continued)		
Resistors (Continued)		
R302	220K Ohms ½W	187A641H83
R305	47 Ohms ½W	187A290H17
R307	47K Ohms ½W	184A763H67
R308 – R312	470 Ohms ½W	184A763H19
R309 – R317	1K Ohms ½W	184A763H27
R313	470K Ohms ½W	184A763H91
R316 (Pot.)	15K Ohms ½W	629A430H08
R318 – R322 – R323	4.7K Ohms ½W	184A763H43
R319 – R321 – R325	22K Ohms ½W	184A763H59
R327	6.8K Ohms ½W	184A763H47
R329	18K Ohms ½W	184A763H57
R331	10K Ohms ½W	629A531H56
R332	6.8K Ohms ½W	629A531H52
R333	27K Ohms ½W	629A531H66
R334	150 Ohms 3 W	762A679H01
Zener Diode		
Z301 to Z305	1N957B, 6.8V	186A797H06
Z306 - Z307	1N3688A, 24 V	862A288H01
RELAY BOARD Style 5312D78G01 – SKBU-11 Style 5312D80G01 – SKBU-1		
Capacitors		
C201-C202-C203	0.25 Mfd	187A624H02
Resistors		
R201▲	50 Ohms 5W	185A209H06
R202-R203 (SKBU-11)	3.3K Ohms ½W	629A531H44
R202-R203 (SKBU-1)●	2.2K Ohms ½W	187A641H35
Filter Choke		
L201	8.5Hy 450 Ohms	188A460H01
Zener Diodes		
Z201▲	1N1828C 43V	629A798H14

▲SKBU-11 only ●Typical Value – Resistors selected for proper loading of low pass filter.

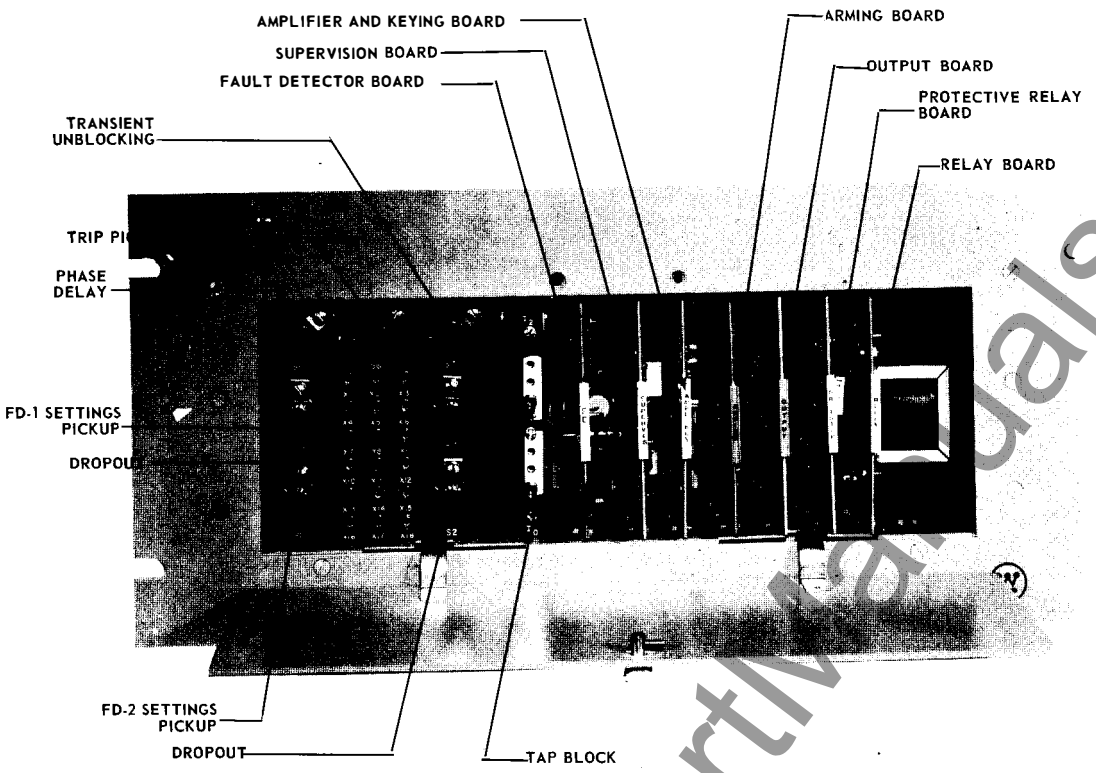


Fig. 1. Photograph (Front View) SKBU-11 Relay SKBU-1 Has a Second Tap Block "T".

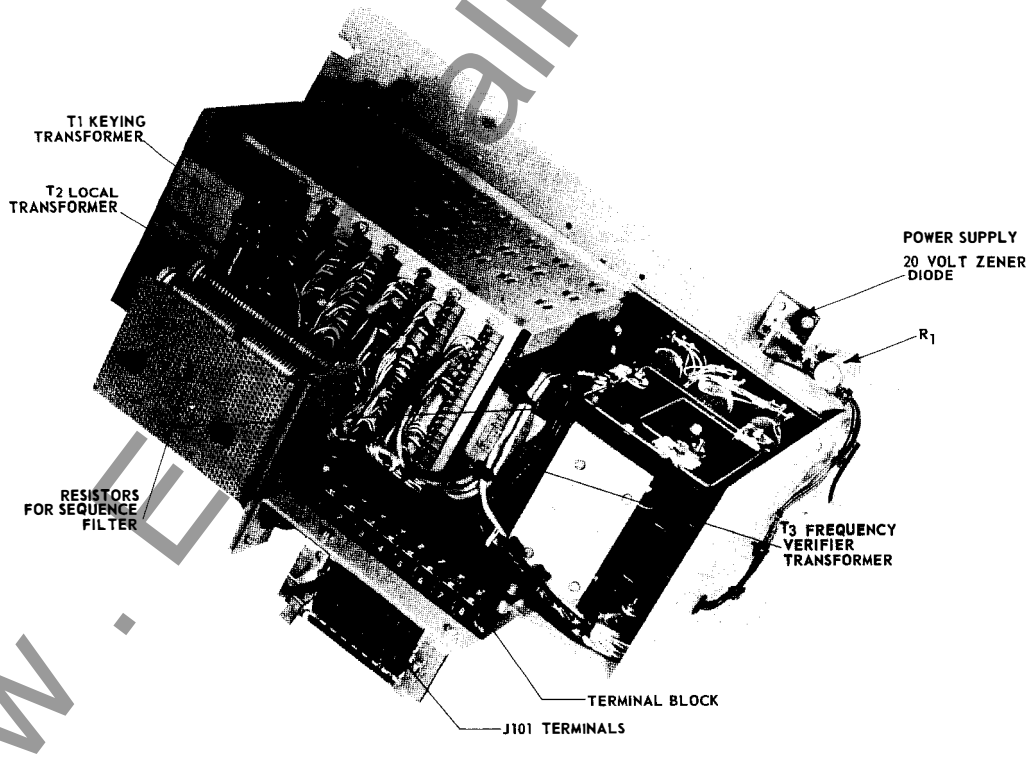


Fig. 2. Photograph (Rear View) SKBU-11 Relay

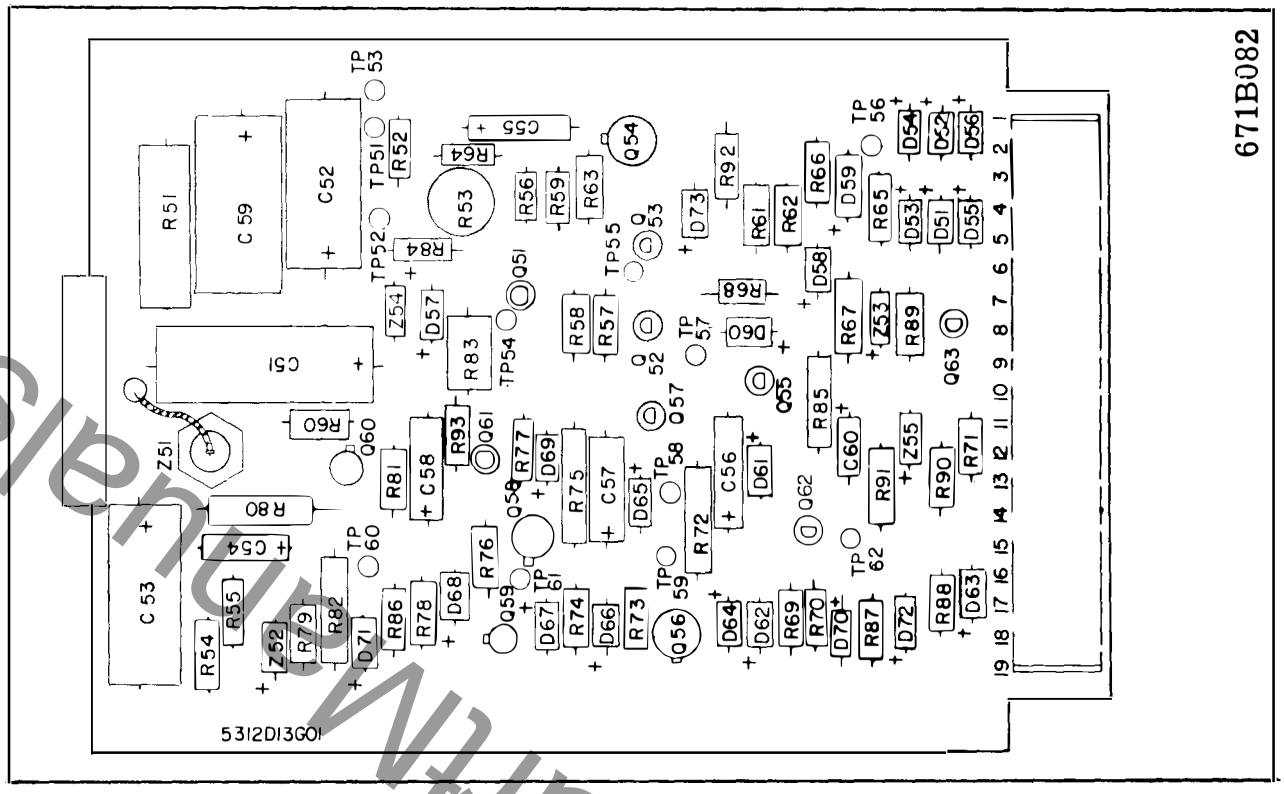


Fig. 3. Location of Components on Fault Detector Board.

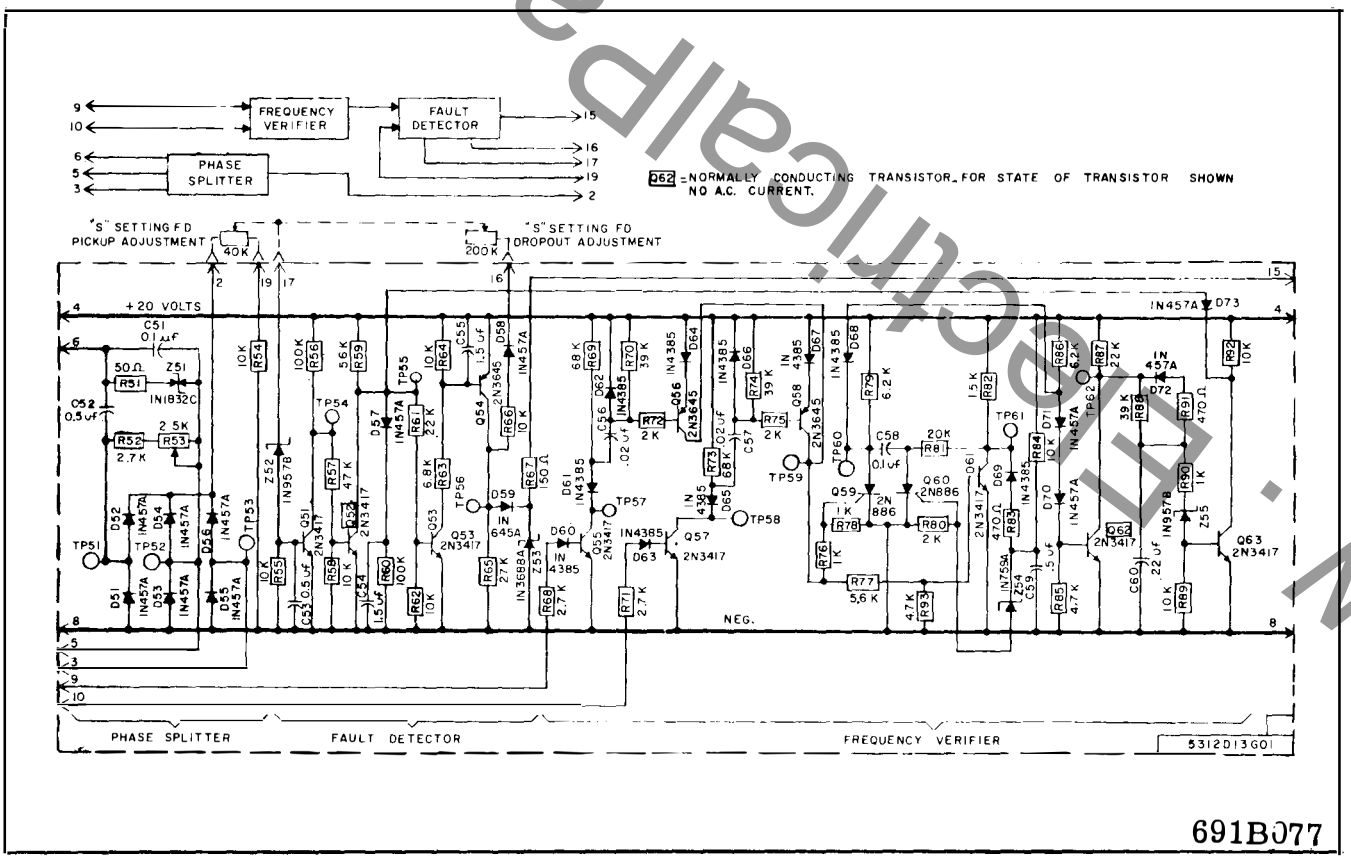


Fig. 4. Schematic of Fault Detector Board.

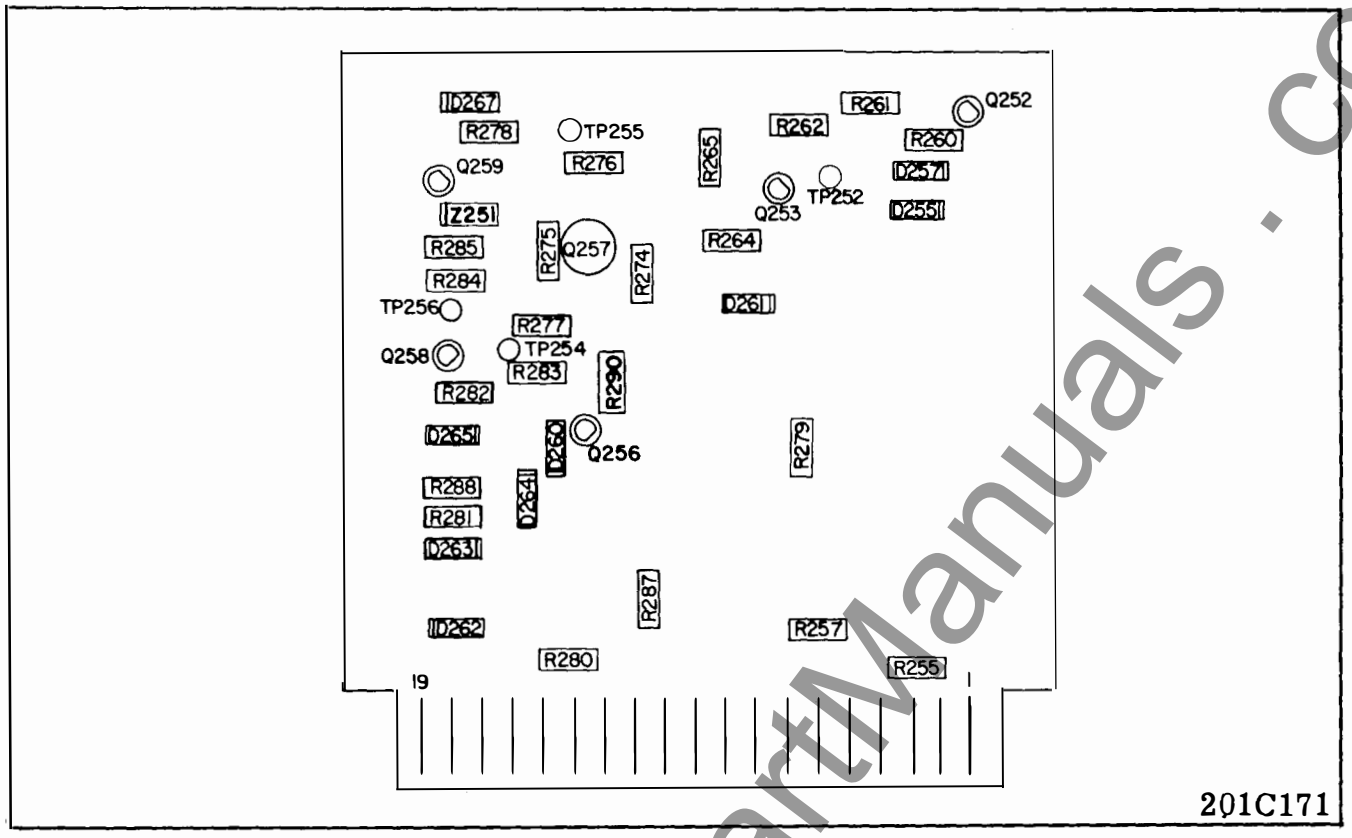


Fig. 5. Location of Components on Arming Board

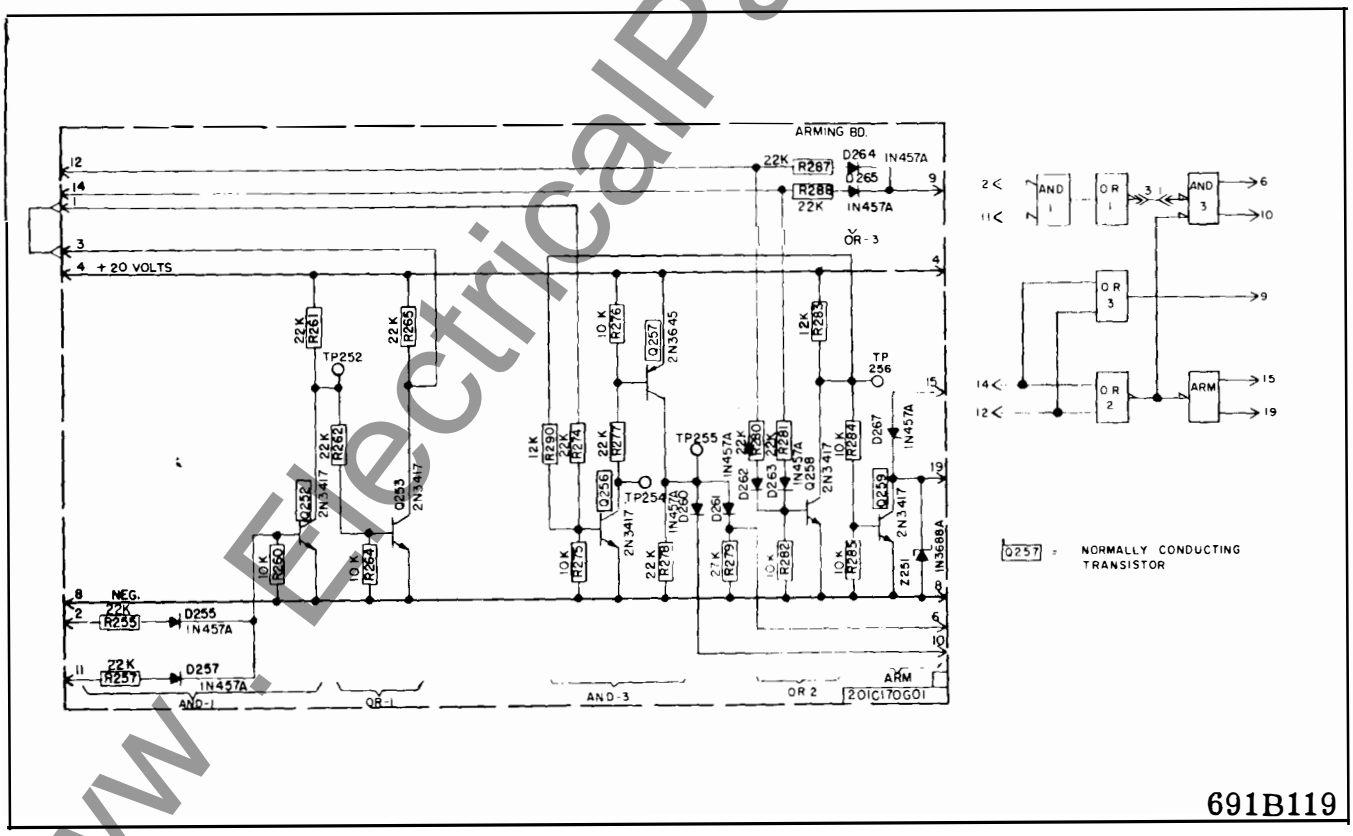


Fig. 6. Schematic of Arming Board

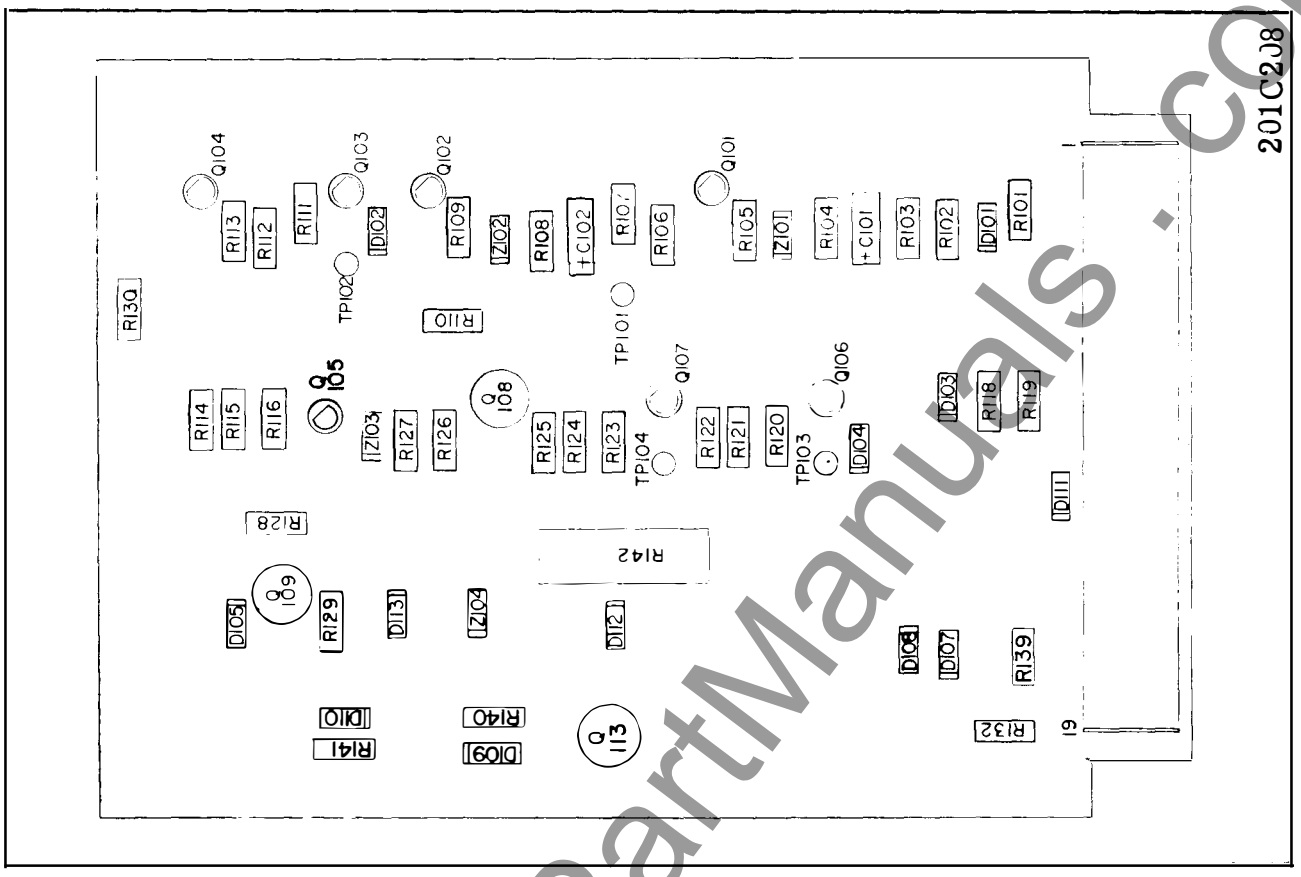


Fig. 7. Location of Components on Amplifier and Keying Board.

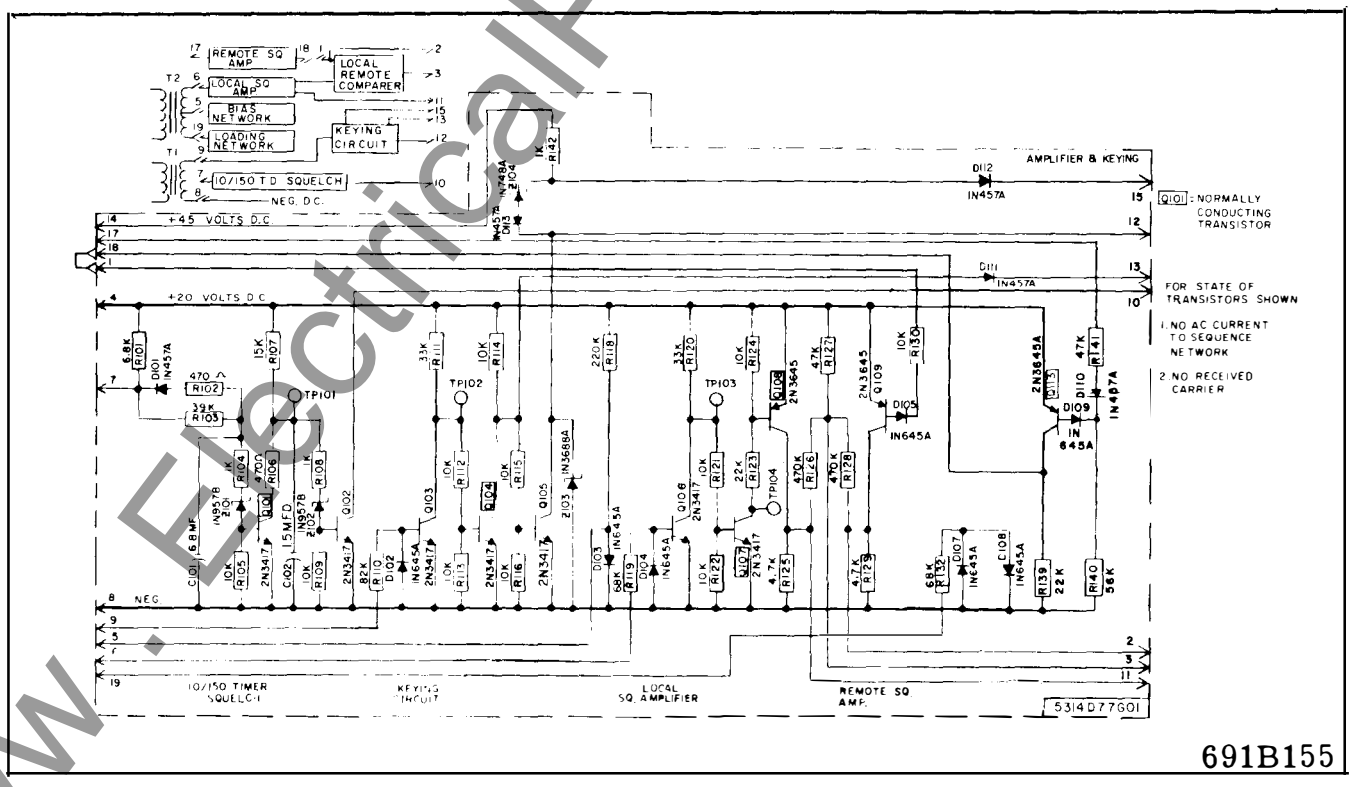


Fig. 8. Schematic of Amplifier and Keying Board.

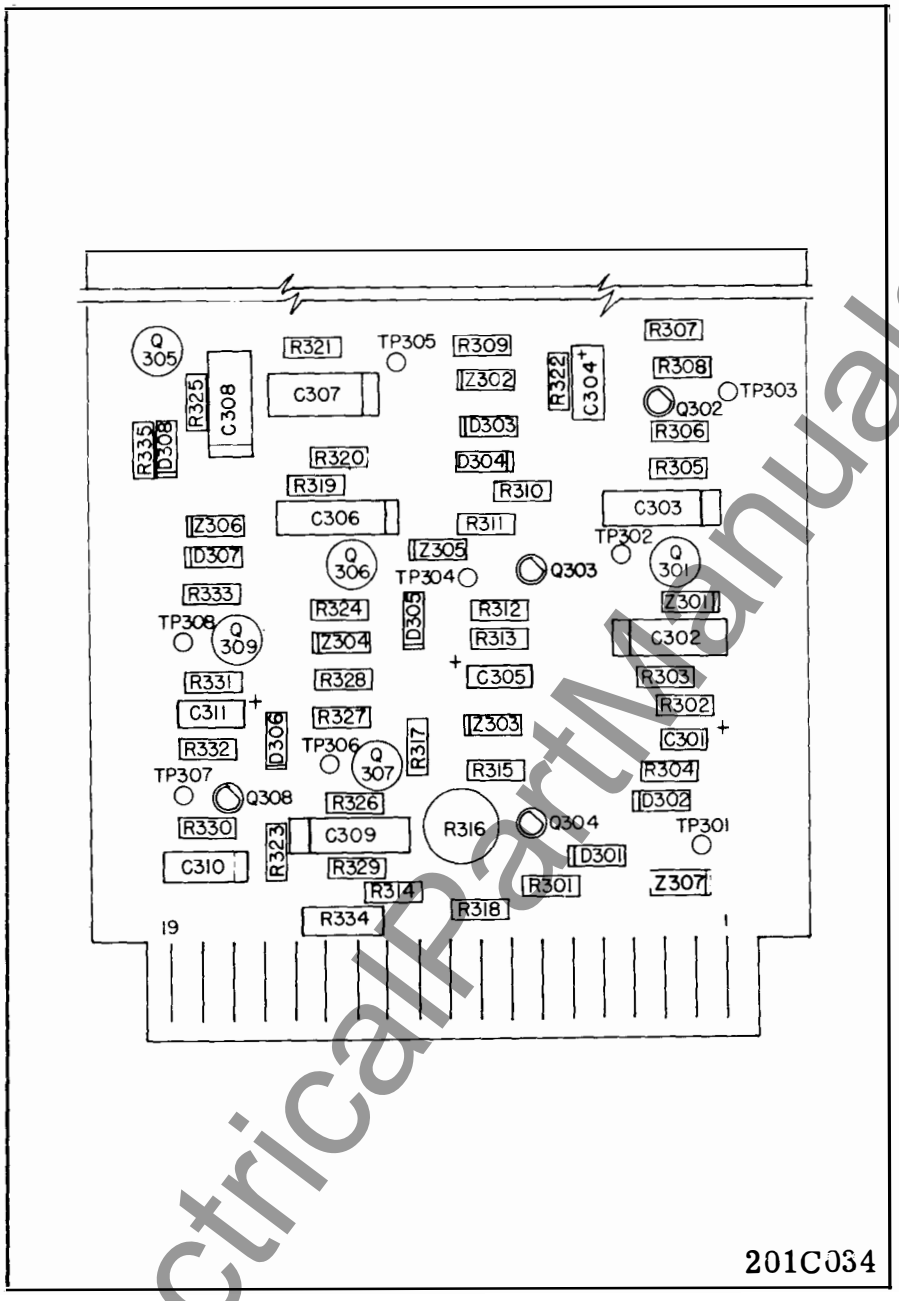
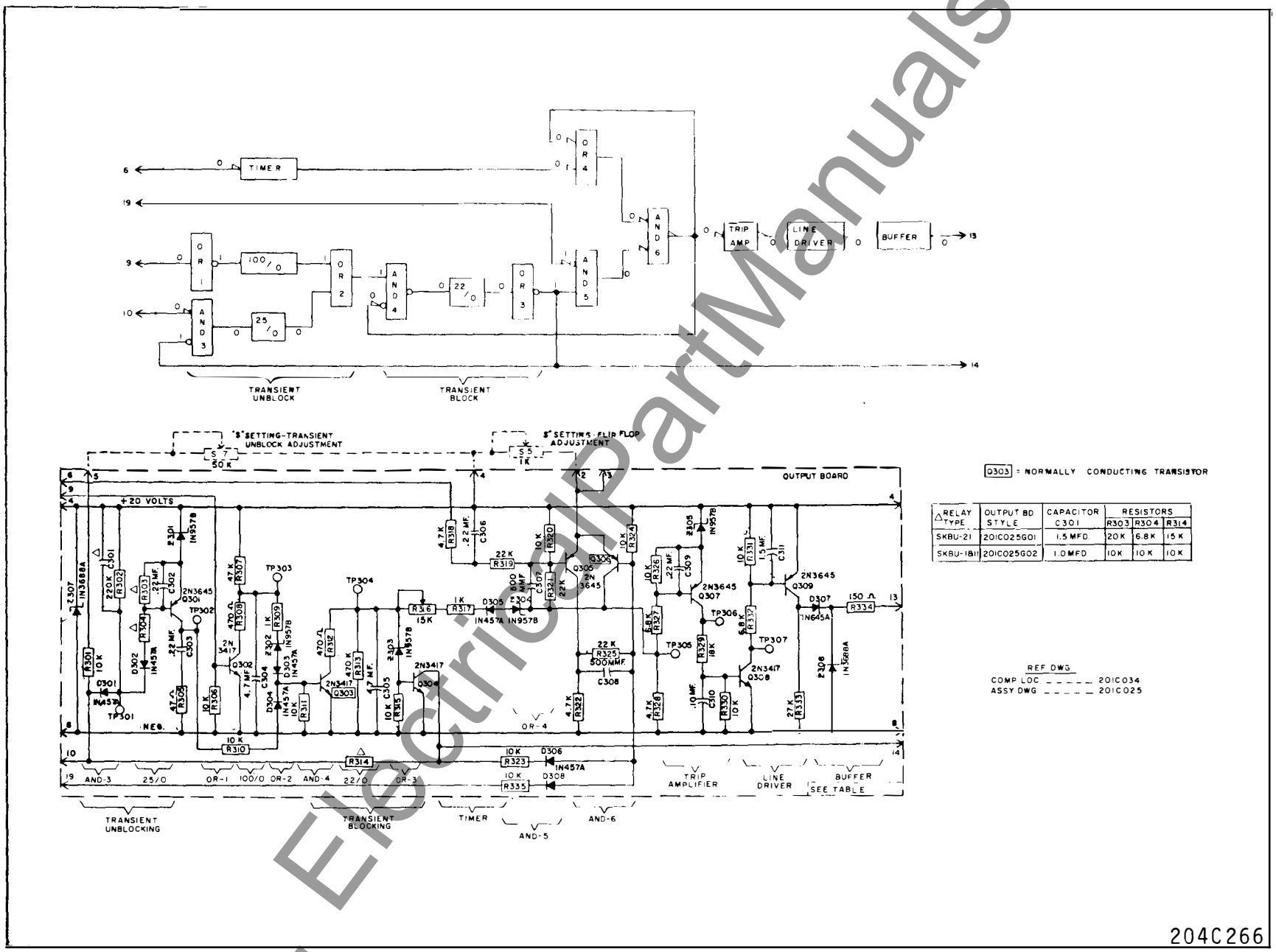


Fig. 9. Location of Components on Output Board.



△RELAY TYPE	OUTPUT BD STYLE	CAPACITOR C301	RESISTORS R303	R304	R314
SKBU-21	20IC025G01	1.5 MFD.	20K	6.8K	15K
SKBU-1811	20IC025G02	1.0 MFD.	10K	10K	10K

Fig. 10. Schematic of Output Board.

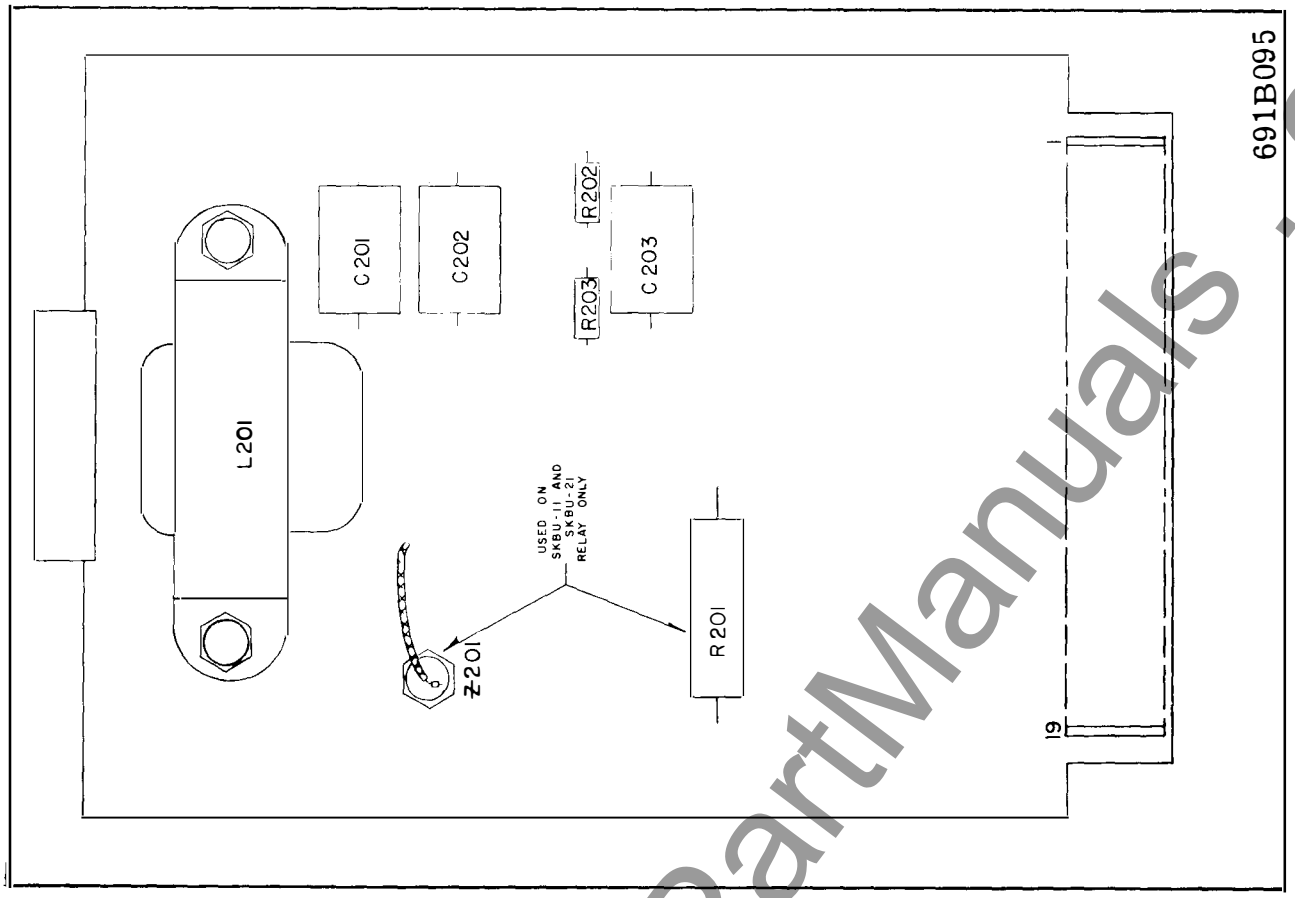


Fig. 11. Location of Components on Relay Board.

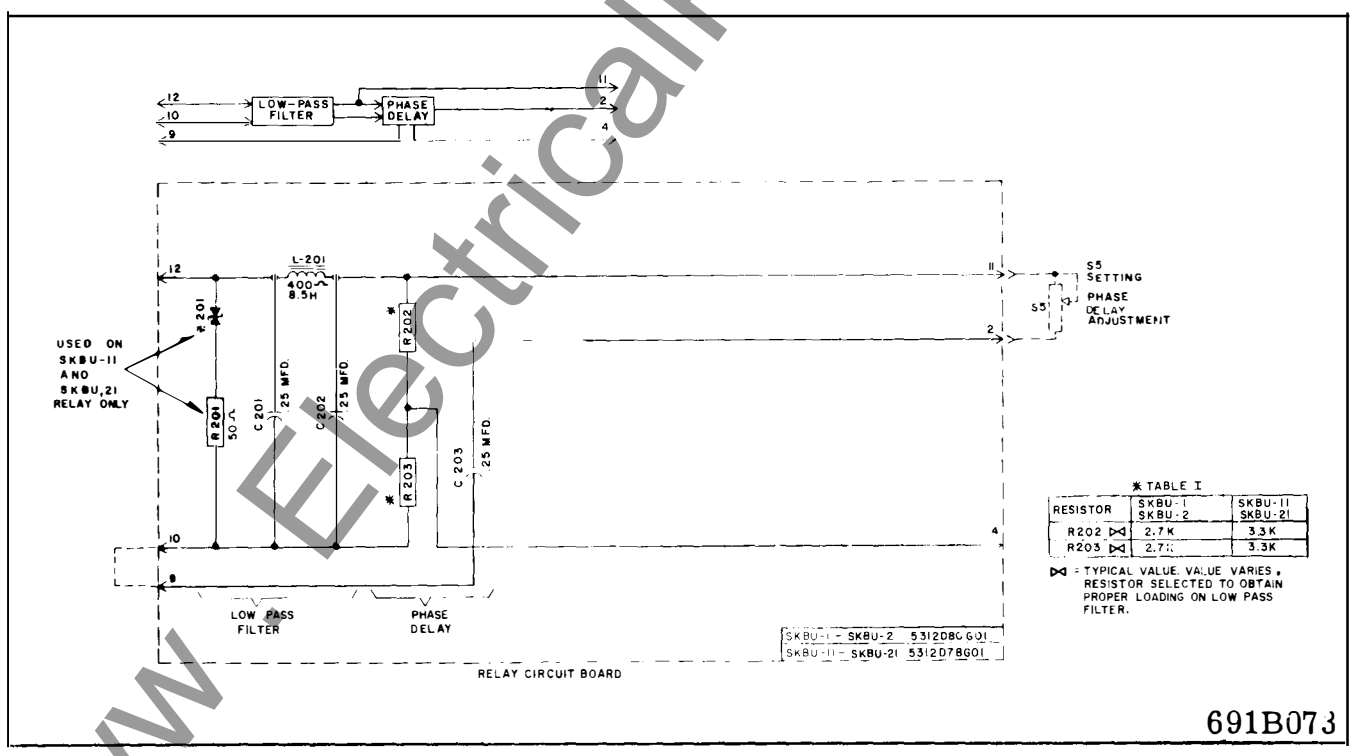


Fig. 12. Schematic of Relay Board.

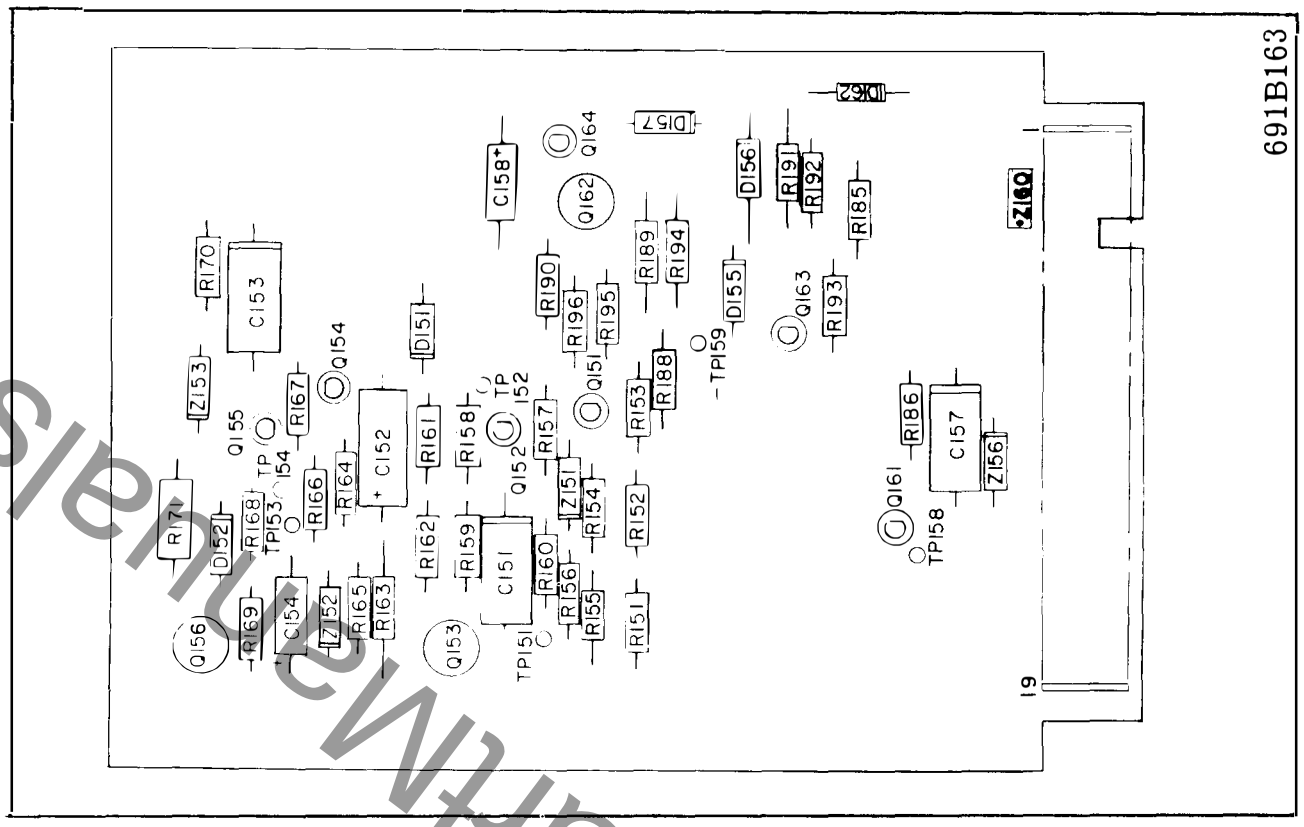


Fig. 13. Location of Components on Supervision Board.

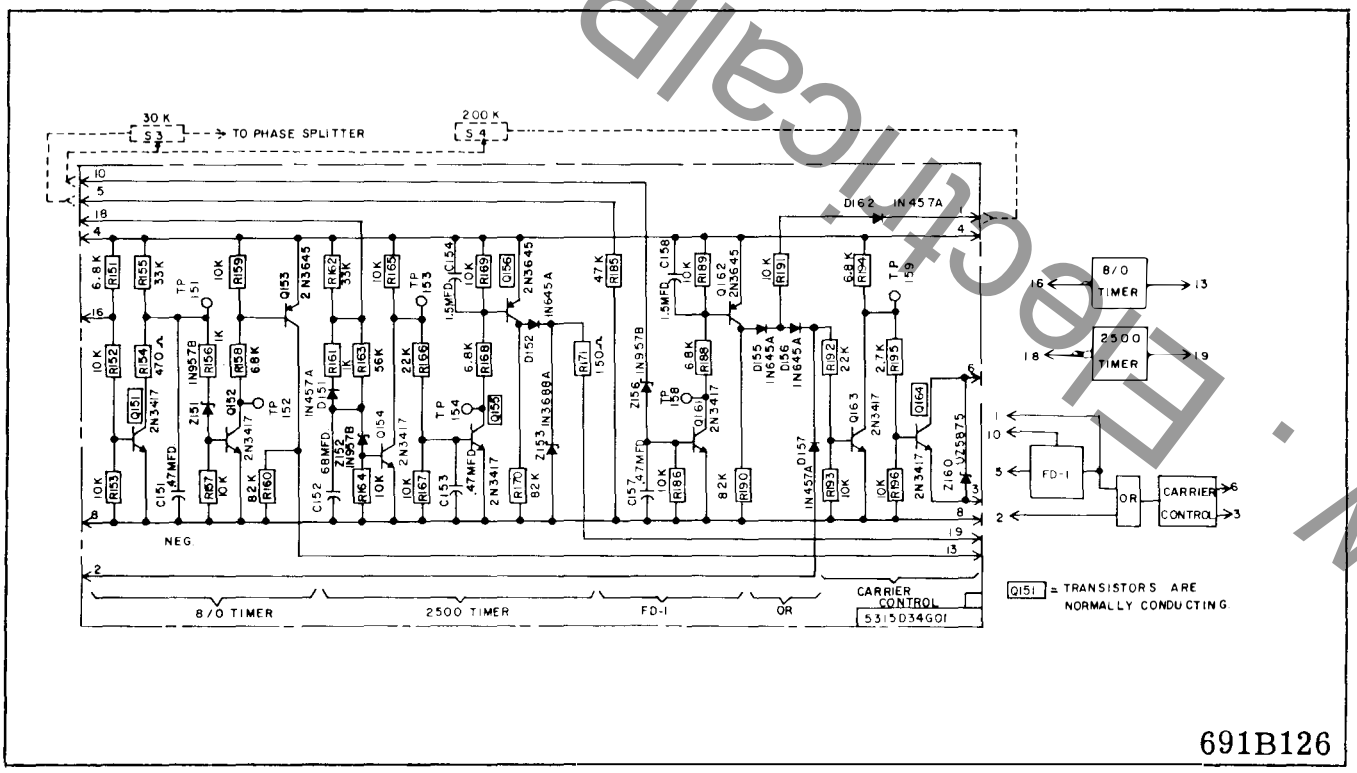


Fig. 14. Schematic of Supervision Board.

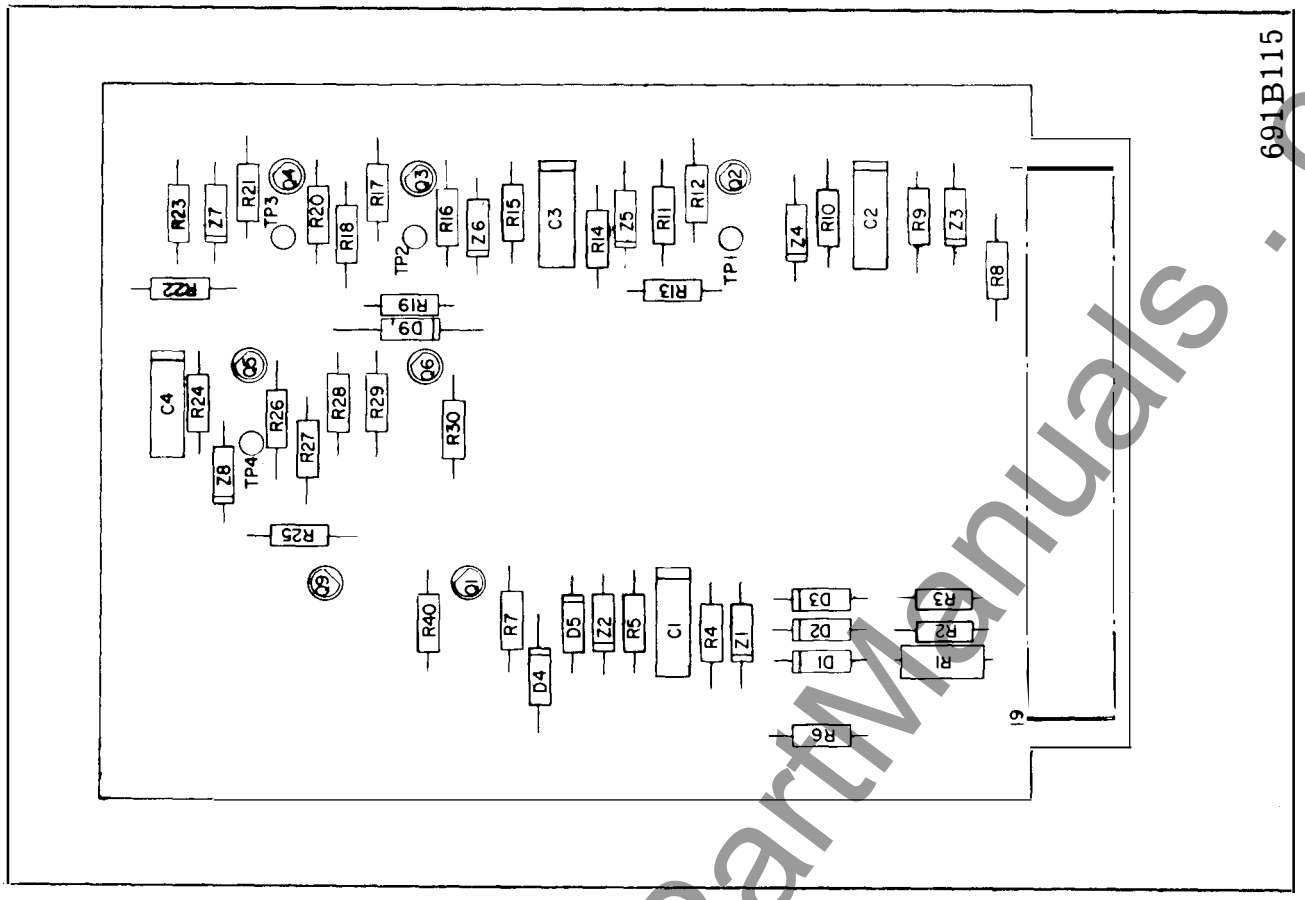


Fig. 15. Component Location on Protective Relay Board.

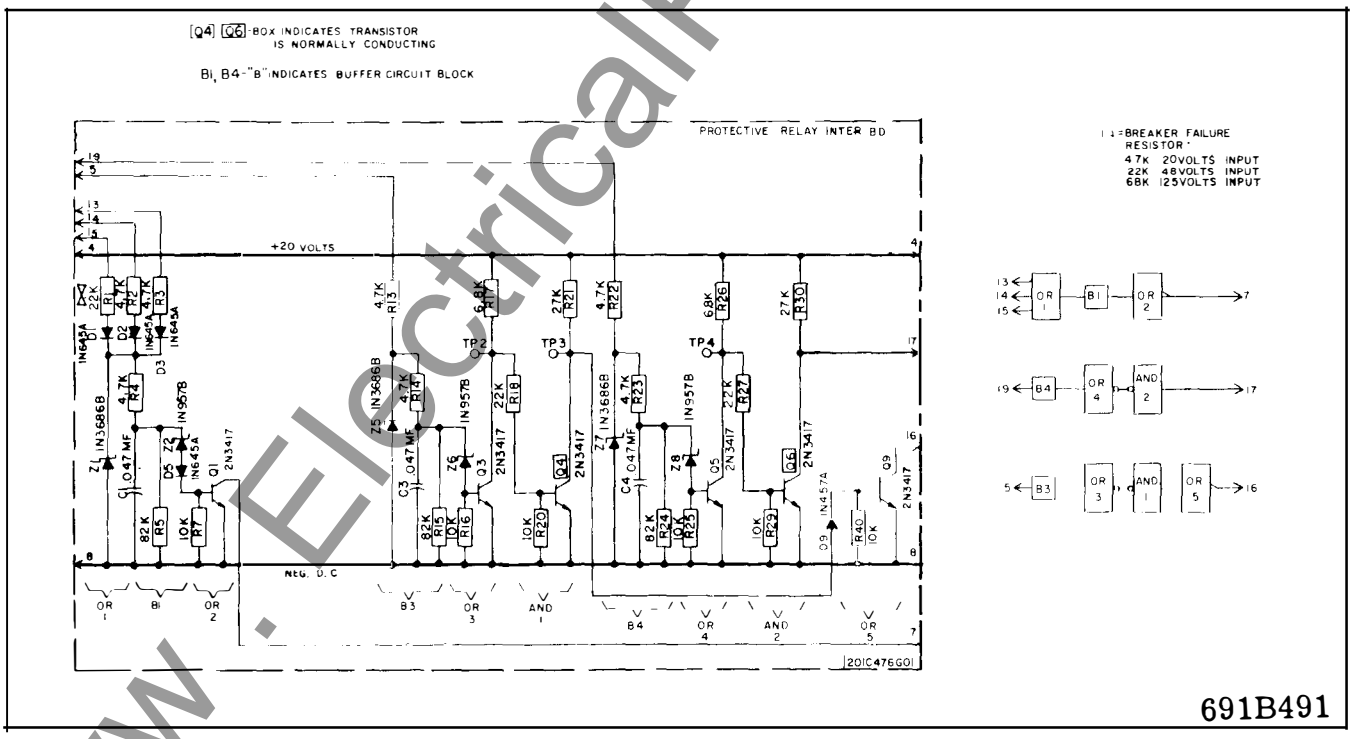


Fig. 16. Schematic of Protective Relay Board for Distance Phase Comparison System.

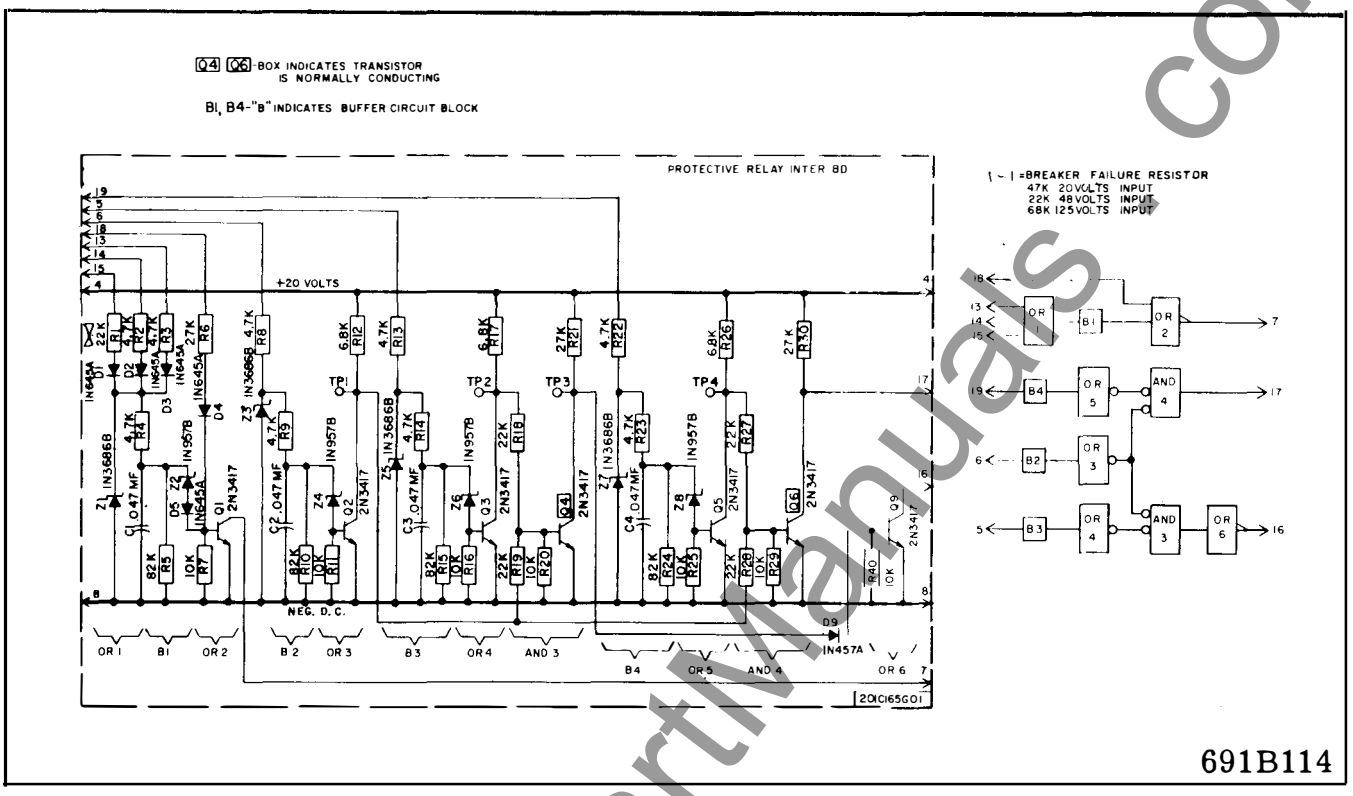


Fig. 17. Schematic of Protective Relay Board for Distance Phase Comparison System with Blinder Control.

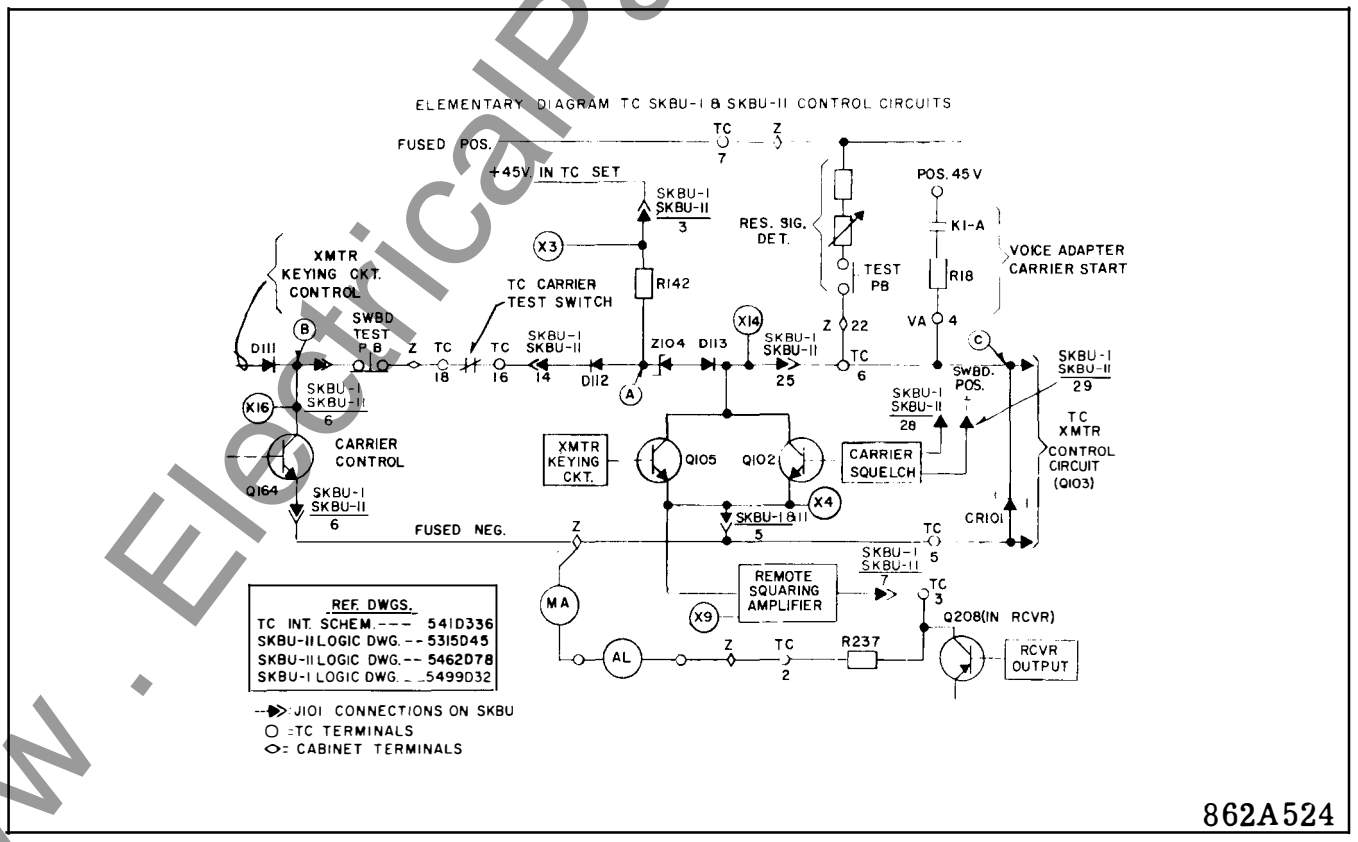


Fig. 18. Elementary Connection of TC SKBU-11.

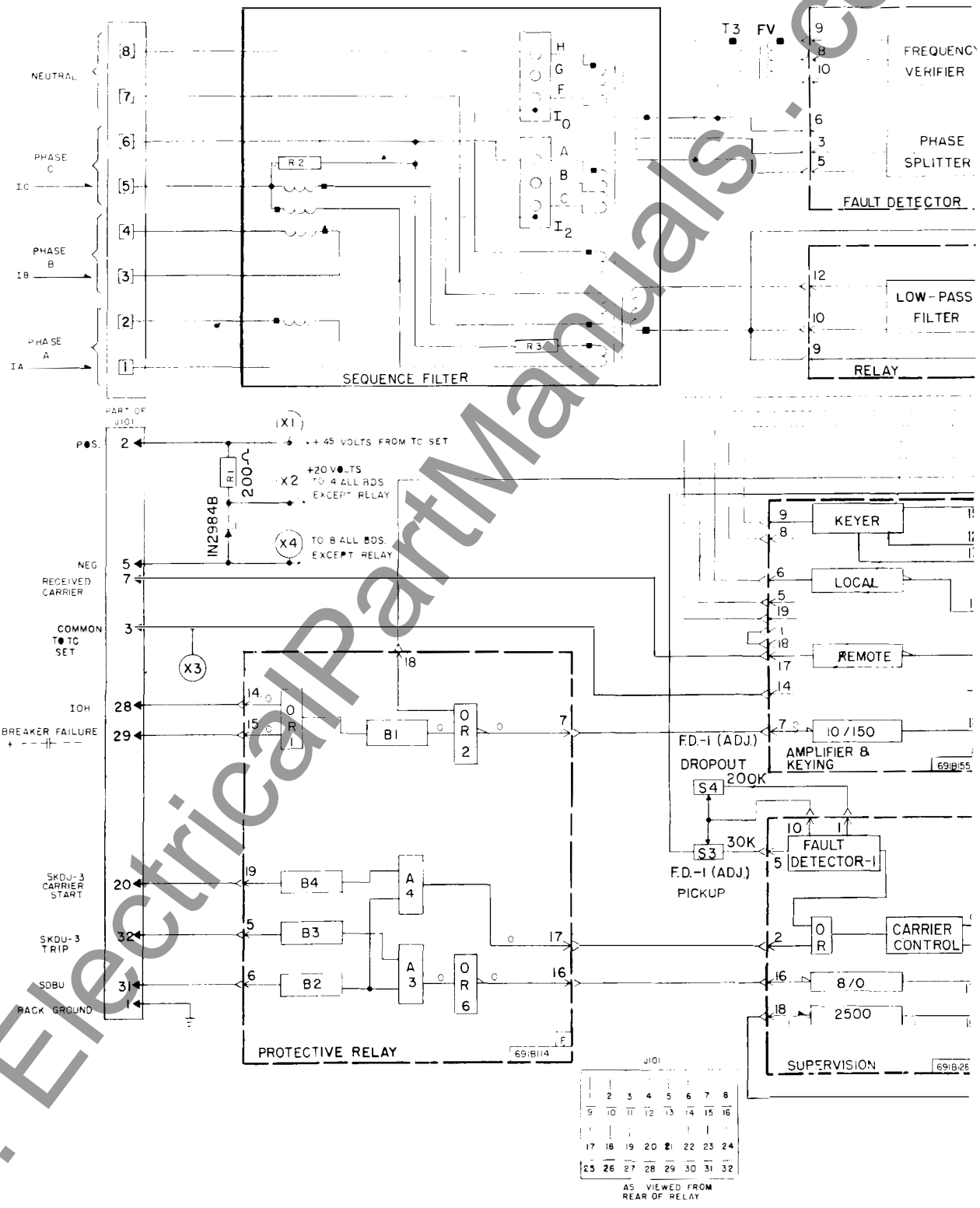
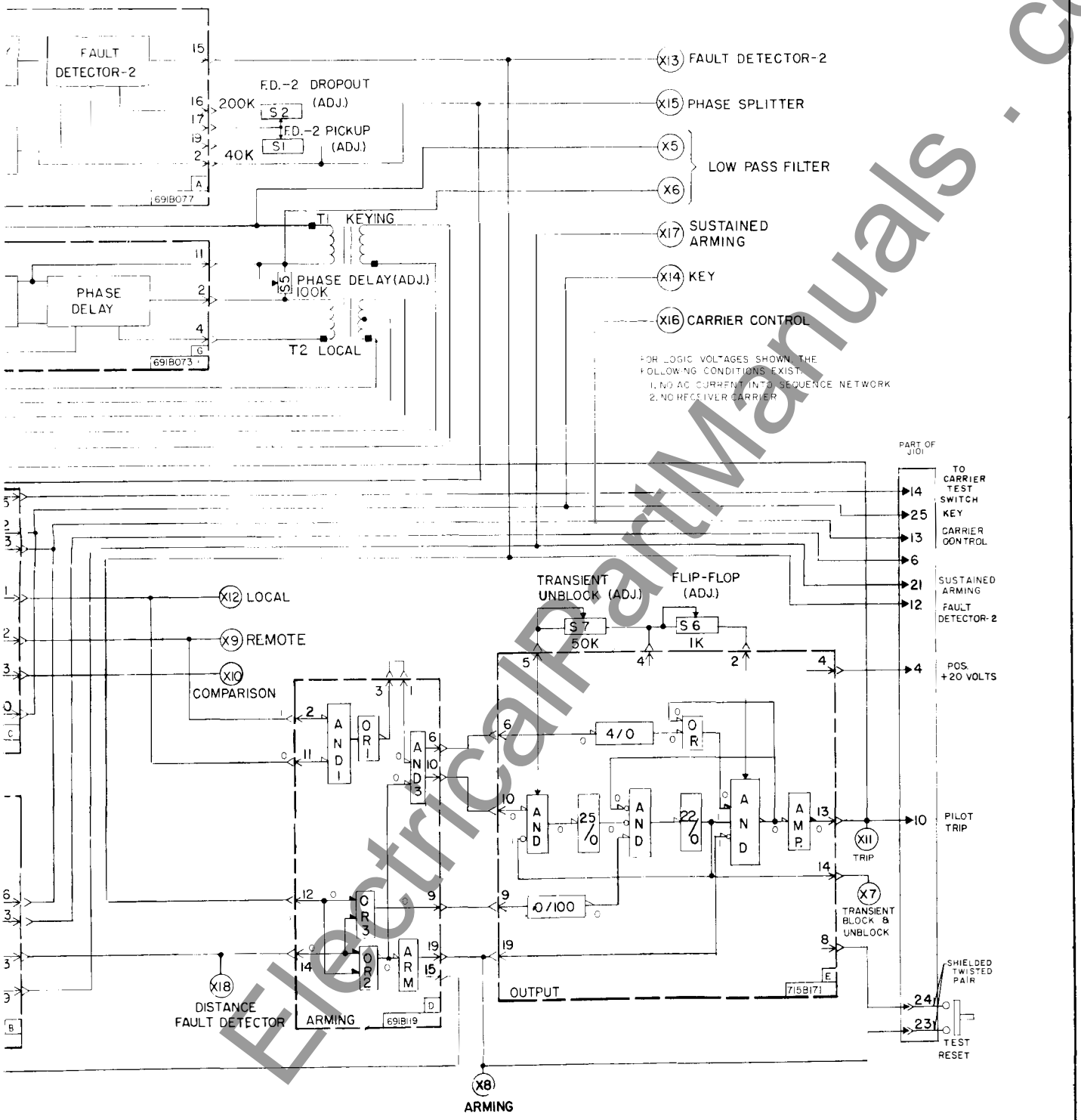


Fig. 20. Logic Diagram of SKBU-11 Relay



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or Distance Phase Comparison System with Blinder Control.

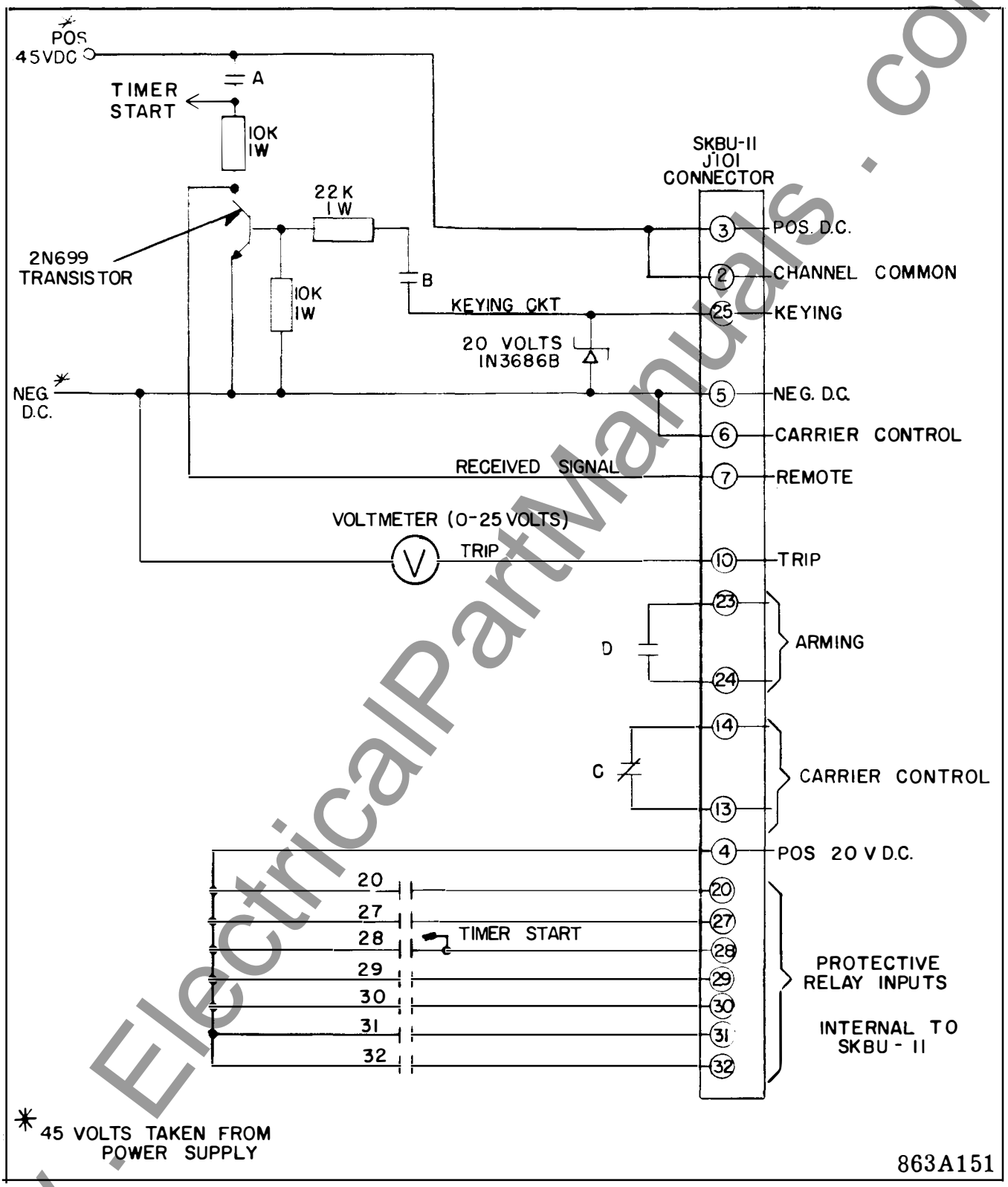


Fig. 24. Test Circuit of SKBU-1 and SKBU-11 Relays.

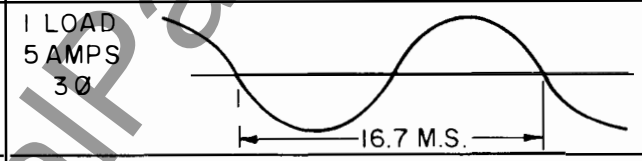
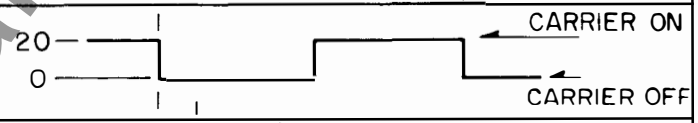
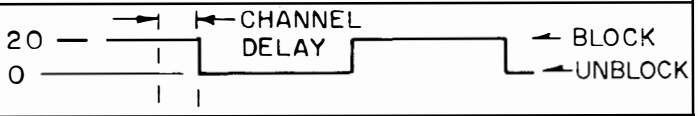
TEST POINT	CIRCUIT	VOLTAGE TO X4
X1	D.C. INPUT VOLTAGE	48 VOLTS D.C.
X2	REGULATED D.C.	20 VOLTS D.C.
X3	COMMON T.C.	45 VOLTS D.C.
X4	BATTERY NEGATIVE	———
X7	TRANSIENT BLOCK	NORMAL 20 VOLTS OPERATE 0 VOLTS
X8	ARMING	NORMAL 20 VOLTS OPERATE 0 VOLTS
X11	PILOT TRIP	NORMAL 0 VOLTS OPERATE 20 VOLTS
X13	FAULT DETECTOR	NORMAL 0 VOLTS OPERATE 20 VOLTS
X17	SUSTAINED ARMING	NORMAL 20 VOLTS OPERATE 0 VOLTS
X18	DISTANCE FAULT DETECTOR OPERATION	NORMAL 0 VOLTS OPERATE 20 VOLTS
X5 TO X6(GND)	LOW PASS FILTER	
X14	KEYING	
X12	LOCAL	
X9	REMOTE	
X16	CARRIER CONTROL	

Fig. 25. Test Point Voltages.

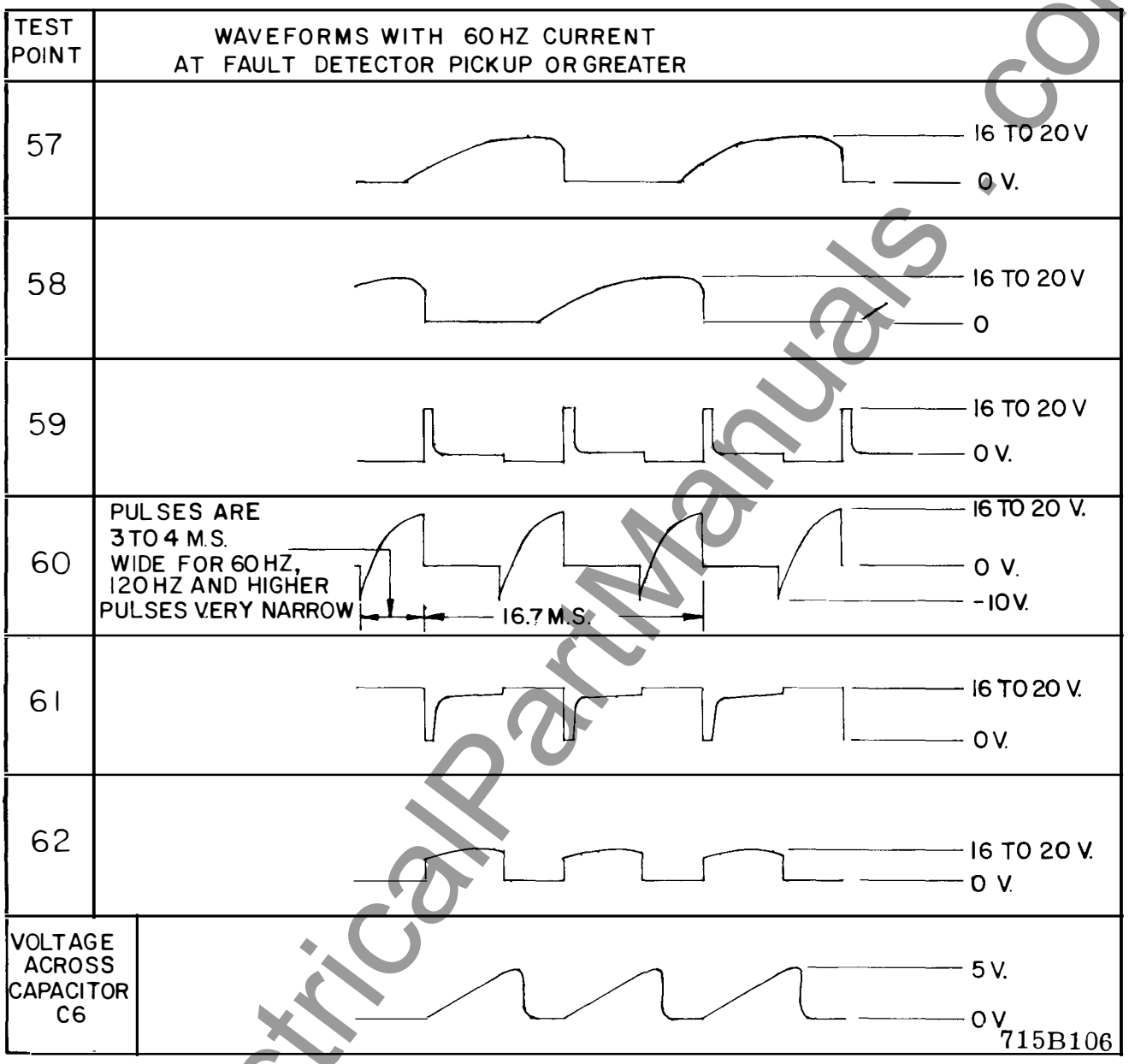


Fig. 26. Frequency Verifier Waveforms at 60 Hz.

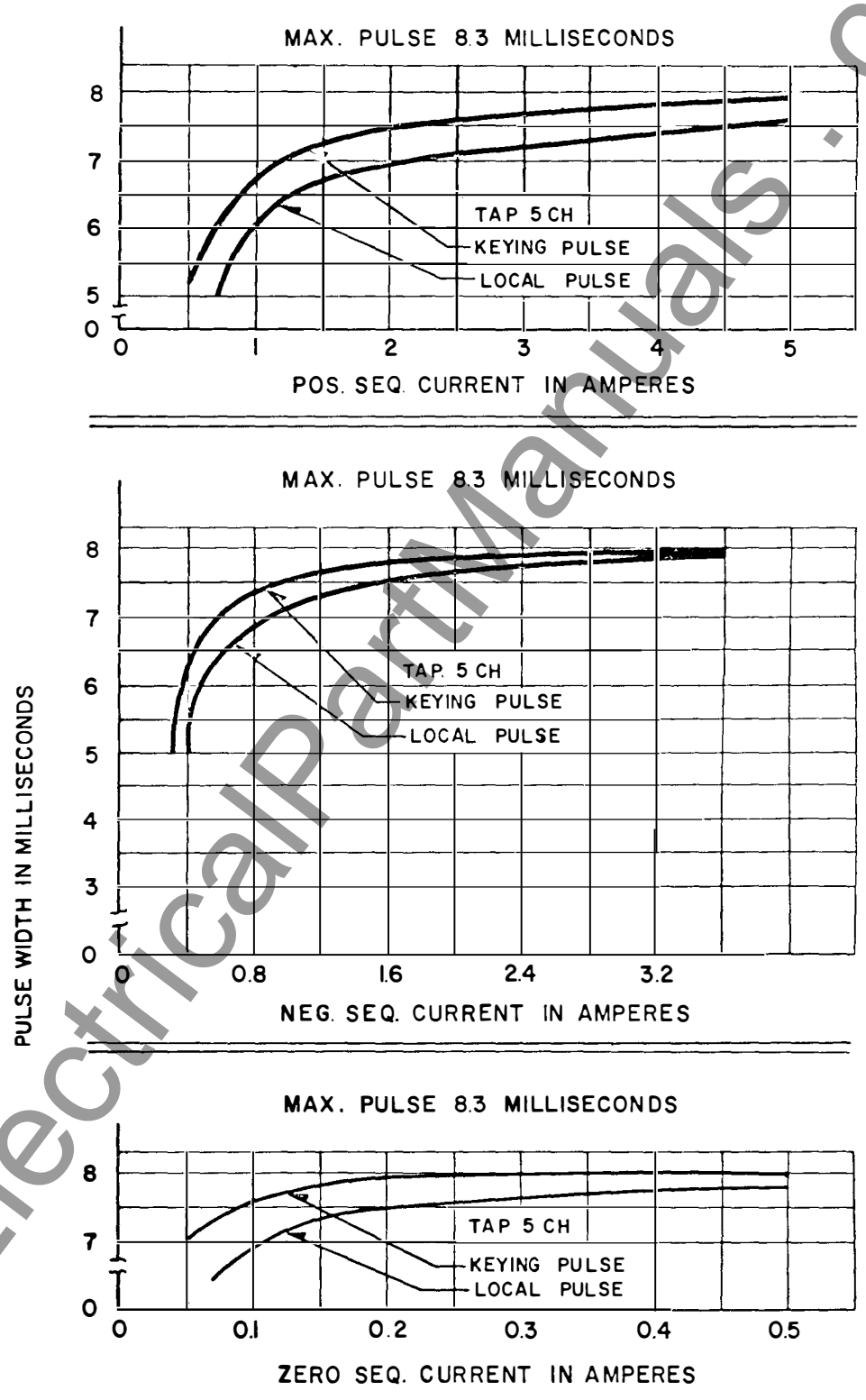


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Fig. 28. Width of Keying Pulses at Different Current Levels of SKBU-1 Relay

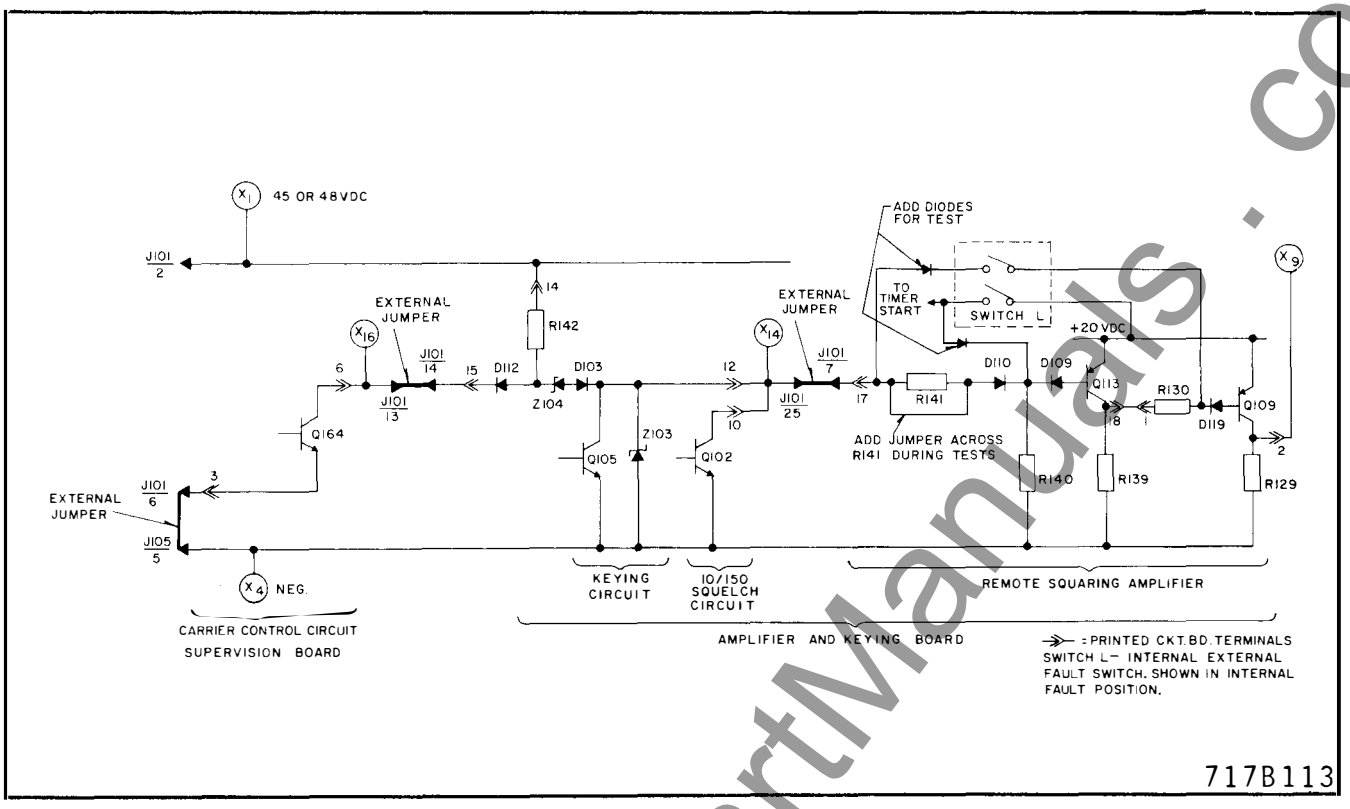


Fig. 29. Inter Connection Diagram of Test Connections to Obtain Remote Pulses from Keying Circuit

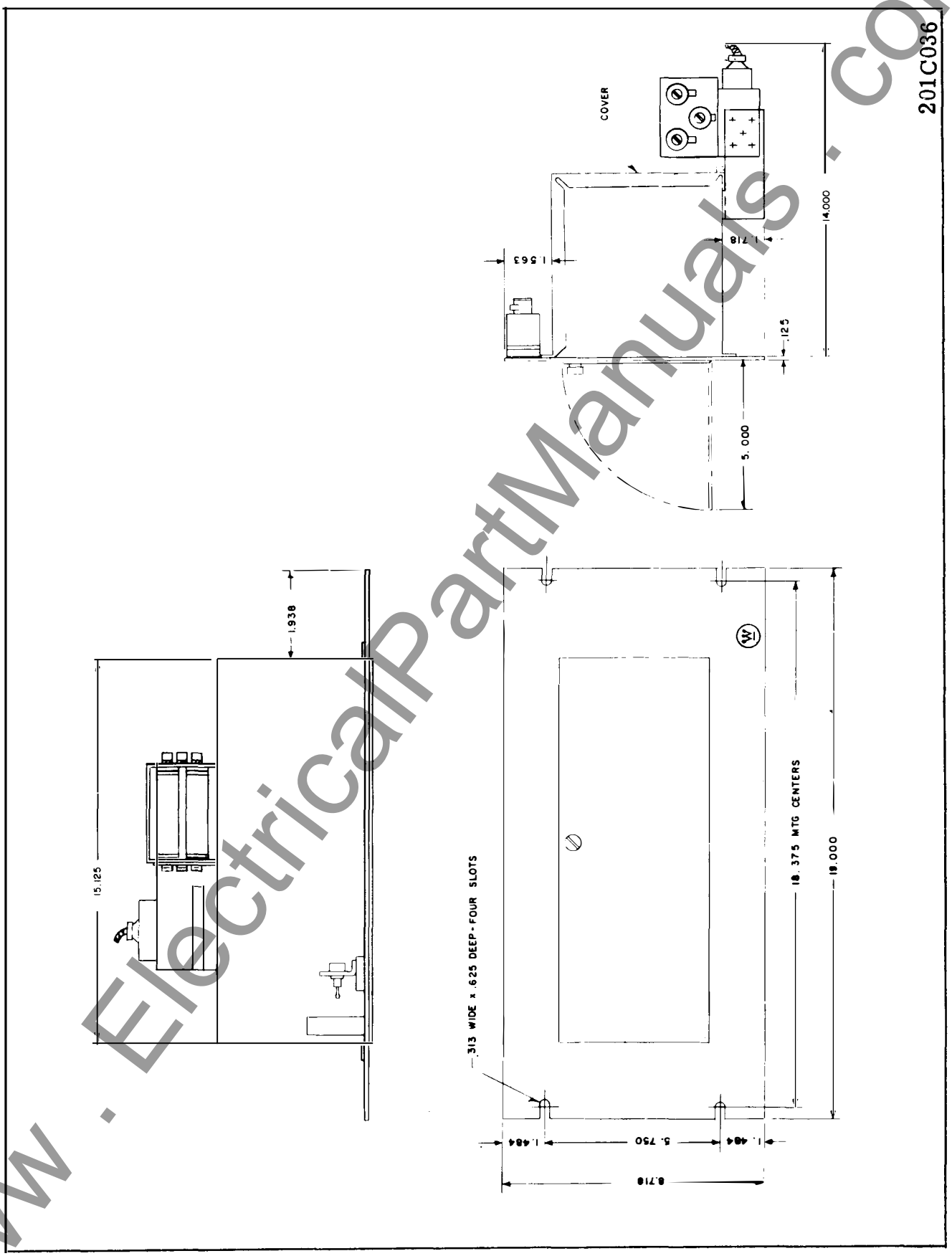


Fig. 30. Outline for Type SKBU-11 Relay

WESTINGHOUSE ELECTRIC CORPORATION

RELAY-INSTRUMENT DIVISION **CORAL SPRINGS, FL.**

Printed in U.S.A.

INSTALLATION • OPERATION • MAINTENANCE

INSTRUCTIONS

TYPE SKBU PHASE COMPARISON RELAY FOR TYPE TC CARRIER CHANNEL

CAUTION: It is recommended that the user of this equipment become acquainted with the information in this instruction leaflet and in the system instruction leaflet before energizing the system.

Printed circuit modules should not be removed or inserted when the relay is energized. Failure to observe this precaution can result in an undesired tripping output and cause component damage.

APPLICATION

The type SKBU relay is a high speed carrier relay used in conjunction with a type TC power line carrier set to provide complete phase and ground fault protection of a two terminal or three terminal transmission line. Simultaneous tripping of the relays at each line terminal is obtained in less than twenty-five milliseconds for all internal faults within the limits of the relay settings. The relay operates on line current only, and no source of a-c line potential is required. Consequently, the relays will not trip during a swing or out-of-step conditions. The carrier equipment operates directly from the station battery.

CONSTRUCTION

The type SKBU relay consists of a combination positive, negative and zero sequence current network, a saturating transformer, a 20-volt power supply, and printed circuit boards mounted on a standard 19-inch wide panel, 8-3/4 inches high (5 rack units). Edge slots are provided for mounting the rack on a standard relay rack. The location of these components is shown in Figures 1 and 2. The components are connected as shown in the internal schematics of Figures 3 and 4.

Sequence Network

The sequence filter consists of a three-legged iron core reactor and a set of resistors, R1 and R0. The reactor has three windings: two primary and a tapped secondary winding, would on the center leg of a "F" type of lamination. The secondary taps are wired to the A, B and C tap connections in the front of the relay (R1 taps). R0 consists of three tube resistors with taps wired to F, G and H tap connections in the front of the relay. The R1 resistor is a formed resistor associated with the tapped secondary of the reactor.

Saturating Transformers

The voltage from the network is fed into the tapped primary of a small saturating transformer. This transformer and a Zener clipper (on a printed circuit board) connected across its secondary are used to limit the voltage impressed on the solid state circuits, thus providing a small range of voltage for a large variation of maximum to minimum fault currents. This provides high operating energy for light faults, and limits the operating energy for heavy faults to a reasonable value.

Printed Circuit Boards

The number of boards varies with the application of the SKBU relay but in general consists of four printed circuit boards mounted in the order given (left to right-front view); a fault detector board, an amplifier and keying board, an output board, and a trip board. All of the circuitry that is suitable for mounting on printed circuit boards is contained in an enclosure that projects from the rear of the front panel and is accessible by opening a hinged door on the front of the panel. The printed circuit boards slide into position in slotted guides at the top and bottom of each compartment and the board terminals engage a terminal block at the rear of the compartment. Each board and terminal block is keyed so that if a board is placed in the wrong compartment it cannot be inserted into the terminal block. A handle on the front of each board is labeled to identify its function in the relay.

All possible contingencies which may arise during installation, operation, or maintenance, and all details and variations of this equipment do not purport to be covered by these instructions. If further information is desired by purchaser regarding his particular installation, operation or maintenance of his equipment, the local Westinghouse Electric Corporation representative should be contacted.

SUPERSEDES I.L. 41-954.1D, dated July 1974
✪ Denotes change from superseded issue.

EFFECTIVE NOVEMBER 1977

(1) Fault Detector Board

The fault detector board contains a resistor-Zener diode combination, a phase splitting network, and two solid state fault detectors (FD-1 and FD-2). The controls for setting pickup (S1 for FD-2, S3 for FD-1) and dropout (S2 for FD-2, S4 for FD-1) of the fault detectors are mounted on the plate in the front of the assembly.

(2) Amplifier and Keying Board

The amplifier and keying board contain a local squaring amplifier, a remote squaring amplifier, an "AND" circuit, and a transmitter keying circuit. A carrier squelch circuit is also located on the board.

(3) Output Board

The output board contains a 4 millisecond pickup and instantaneous dropout, timer circuit, flip-flop circuit, trip amplifier, transient blocking and unblocking circuit.

(4) Trip Board

The trip board contains the phase delay circuit for shifting the local signal with reference to the remote signal. This board also contains the final tripping output of the SKBU.

(5) Card Extender

A card extender (Style No. 644B315G02) is available for facilitating circuit voltage measurements or major adjustments. After withdrawing any one of the circuit boards, the extender is inserted in that compartment. The board then is inserted into the terminal block on the front of the extender. This restores all circuit connections, and all components and test points on the boards are readily accessible.

Test Points

Test points are located on each printed circuit board for the major components on the board. Complete circuit test points are wired to the front panel of the relay for convenience in adjusting and testing the relay.

OPERATION

A. System

The SKBU carrier relaying system compares the phase position of the currents at the ends of a line section over a carrier channel to determine whether an internal or external fault exists on the line section. The three-phase line currents energize a sequence network which produces a single-phase output voltage proportional to a combination of sequence components of the line current. During a fault, this single-phase voltage energizes the keying circuit to allow the transmission of carrier on alternate half-cycles of the power frequency current. Carrier is transmitted from both line terminals in this manner, and is received at the opposite ends where it is compared with the phase position of the local sequence network output. If the local and remote half-cycle pulses are of the correct phase position for an internal fault, after a 4 millisecond delay during the half cycle in which carrier is not transmitted, tripping will be initiated through operation of the flip-flop and trip amplifier circuits. Current transformer connections to the sequence networks at the two terminals are such that carrier is transmitted on the same half cycles from both terminals during a internal fault to allow tripping during the half cycle that carrier is not transmitted. However, if the fault is external to the protected line section, carrier is transmitted on alternate half cycles from opposite terminals. Thus each terminal blocks the opposite terminal during the half cycle when it is attempting to trip.

The four-millisecond delay previously mentioned is added to allow for differences in current transformer performance at opposite line terminals, relay coordination, and momentary interruptions in carrier caused by arcing over of protective gaps in the tuning equipment.

Since this relaying system operates only during a fault, the carrier channel is available at all other times for the transmission of other functions.

B. Relay

With reference to either Figs. 3 or 4, the three phase line currents energize a sequence network which gives a single phase output voltage proportional to a combination of sequence components of the line current. This single phase output voltage is applied as inputs to two boards from the secondary of the saturating transformer.

1. Fault Detector Board (Phase Splitter Circuit).
2. Relay Board (Phase Delay Circuit).

1. Fault Detector

The a-c voltage is applied to a phase splitting network (C52, R54, R53) and a polyphase rectifier (diodes D51 to D56). The d-c voltage so obtained requires a minimum of filtering

(C53) and responds rapidly to a change in magnitude of the a-c output. This d-c voltage is applied to two fault detector circuits which operate when the d-c input "signal" exceeds a predetermined value.

a. Fault Detector 1 (FD-1)

Under normal line conditions (no fault), current flows from positive 45 volts d-c through resistor R72 and Zener diode Z54 to negative, holding Q55 emitter at 6.8 volts positive. In transistor Q55, current flows from emitter to base, then through S3 and R71 to negative, thus turning on Q55. The collector current of Q55 provides base drive to transistors Q56 and Q57, turning them on also. The voltage drops across Q56 and Q57 are very low (about 0.5 volts), thus providing the equivalent of a closed contact. When a fault occurs, the d-c voltage from the polyphase rectifier is applied to S3 and R71. When this voltage exceeds the 6.8 volt drop across Zener diode Z54, transistor Q55 stops conducting. This removes the base current from Q56 and Q57, causing them to stop conducting, and providing the equivalent of an open circuit. With reference to Figure 7, this open circuit removes negative potential at point A and allows the potential at point C to become 20 volts. This increase in voltage at point C starts transmission of carrier.

When Q56 is cut off, its collector potential rises to about 20 volts. This also further raises the potential of Q55 base through feedback resistors R75 and S4, thus holding Q55 in a non-conducting state. When the input voltage (from the polyphase rectifier) is reduced, FD1 "resets" to allow transistors Q55, Q56 and Q57 to conduct. Resistor S3 is for setting the FD1 pickup current (calibration adjustment), and the setting of S4 determines the 80 percent dropout value.

b. Fault Detector 2 (FD-2)

Under normal conditions, transistor Q51 has no base "signal" and is turned off. The collector of Q51 is at a high enough positive potential to provide base drive for transistor Q52, driving it to conduction. With Q52 conducting there is no base drive to transistor Q53 and Q53 is turned off. This condition keeps transistor Q54 in a non-conducting state, equivalent to an open circuit. Zener diode Z3 is to protect transistor Q54 from external surge voltages.

When a fault causes the d-c input voltage from the polyphase rectifier to exceed the 6.8 volt rating of Zener diode Z52, (through R55, and S1) a positive bias is applied to Q51 base causing it to conduct. In turn, Q52 stops conducting, and capacitor C55 charges up, giving a few milliseconds time delay before Q53 and Q54 are switched to full conduction, thus "closing" FD2. The feedback resistors R60 and S2 provide a 90 percent FD2 dropout ratio with "toggle" action at the dropout point.

When FD-2 operates, positive 45 volts d-c is applied to the output board at terminal 18. This 45 volts is applied to the flip-flop circuit at terminal 19 and to the transient blocking circuit through Zener diode Z302. Thus, FD2 will "arm" the flip-flop and energize transient blocking of the SKBU relay.

2. Relay Board

The a-c voltage from the saturating transformer is also applied to the phase delay circuit through a low-pass filter of the relay board. The low-pass filter (C251, L251, C252) removes the harmonics from this voltage and applies a voltage that is essentially sinusoidal in waveform to R251 and R252 of the phase delay circuit. By means of capacitor C253 and variable resistor S5, the voltage across terminals 4 and 9 can be made to lag the voltage across terminal 10 and 11 by a definite amount depending on the setting of S5. These two voltages are applied to the amplifier and keying board of the SKBU relay.

a. Undelayed Voltage to the Keying Circuit.
b. Delayed Voltage to the Local Squaring Amplifier.

a. Keying Circuit

Under normal conditions transistor Q102 is turned off. The collector of Q102 is at negative potential which allows base current to flow from

positive 20 volts d-c through the base of transistor Q103, through R104 and R102 to negative. Transistor Q103 conducts and positive 20 volts is applied to the collector of Q103 to prevent base current from flowing in Q104, Since Q104 is not conducting, transistor Q105 does not conduct and the collector of Q105 is held at positive potential.

When a fault occurs, sinusoidal voltage is applied to transistor Q102 from terminals 4 and 10 of the relay board. On the positive half cycle, terminal 12 is more positive than terminal 4 of the amplifier and keying board, and Q102 does not conduct. However, on the negative half cycle of sine wave voltage, terminal 12 is more negative than terminal 4 and base current flows in Q102. This turns Q102 on and applies positive 20 volts to R102. This turns Q103 off which in turn puts negative potential on R106. Q104 then conducts to allow base current to flow into Q105. When Q105 conducts, its collector is connected to negative potential. Thus, the collector of Q105 is connected to negative on alternate half cycles of the 60-hertz voltage from the low pass filter. If FD-1 is not conducting, as seen from Fig. 7, turning Q105 on and off every half cycle, shorts the input to the TC carrier set every other half cycle so that carrier is transmitted on the half cycle when Q105 is not conducting.

b. Local Squaring Amplifier

The shifted voltage from the phase delay circuit is applied to the local squaring amplifier of the SKBU relay. Under non-fault conditions, Q108 is not conducting and R115 is at negative potential. As a result, the base of Q109 is at a lower potential than the emitter of the transistors. Base current for both transistors flows from positive 20 volts through R116 and R115 to negative and both transistors conduct. With Q111 turned on, positive 20 volts is applied to R119 which is applied to R129 and R130 through D111 and D109 respectively. This voltage is the input to the AND circuit from the local signal and is the quantity to be compared with the signal from the remote terminal to determine if a fault is internal or external.

Under fault conditions, a sine wave of voltage is applied from emitter to base of transistor Q108. On the positive half cycle the base of transistor Q108 is more positive than the emitter and Q108 does not conduct. On the negative half cycle of sine wave voltage, the base is more negative than the emitter and Q108 conducts. Turning Q108 on applies positive 20 volts to R115 to cause Q109 to turn off. This causes Q111 to turn off such that negative potential is applied to R119. Hence, on alternate half cycles of sine wave voltage, negative voltage appears across R119 to apply negative voltage to R129 and R130 through D111 and D109 respectively. The voltage across the resistor is thus a square wave voltage varying from 20 volts d-c to 0 volt d-c dependent upon the polarity of the voltage from the phase delay circuit.

3. Remote Squaring Amplifier

Under non-fault conditions, carrier is not transmitted from the remote carrier set. As a result the base of Q113 is more negative that its emitter, and Q113 conducts. This applies positive 20 volts to the base of Q112 to prevent it from turning on. Hence, Q112 is not conducting and negative voltage appears across R123. This voltage is applied to R129 and R130 through D112 and D110 respectively, and allows the voltage across these resistors to remain at negative potential.

Under fault conditions, the remote TC carrier set is keyed on and off as described under the Keying Circuit. This signal is received at the local TC carrier receiver and is converted to a square wave voltage varying in magnitude from 45 volts to 0 volt. This voltage is applied to the base of Q113 through D108 and R128. Upon application of

positive 45 volts d-c to the base of Q113, the potential of the base is greater than that of the emitter and Q113 stops conducting. This removes positive potential from R124 and allows the base of Q112 to become negative with respect to the emitter. Q112 turns on to apply positive voltage to R123. Hence, the voltage across R123 is a square wave voltage that is developed by the voltage received from the TC receiver. This voltage is applied to R129 and R130 through D112 and D110.

4. 4/0 Milliseconds Time Delay

The 4/0 time delay consists of R315, C305, R316, R317. R318 and R319. Under non-fault conditions, a continuous positive 20 volts is received from the local squaring amplifier at terminal 6 of the output board. This prevents capacitor C305 from charging and keeps the base of Q305 of the flip-flop at positive potential.

Under external fault conditions, the square wave voltage from the remote squaring amplifier and the square wave voltages from the local squaring amplifier are out of phase, such that a continuous 20 volts is received at terminal 6 of the output board. C305 does not charge, and transistor Q305 cannot turn on.

Under internal fault conditions, the square wave voltages from the squaring amplifiers are in phase. Hence, for one-half cycle, negative voltage appears at terminal 6 of the Output board. This allows C305 to charge through resistors R315 and R129 to negative. After a calibrated time delay of 4 milliseconds, the voltage across C305, which is applied to the base-emitter circuit of transistor Q305 in the flip-flop circuit is sufficient to allow Q305 to conduct.

5. Flip-Flop

The flip-flop circuit consists of transistors Q305 and Q306 and associated components. Under normal conditions, transistor Q305 is in a non-conducting state, and transistor Q306 is fully conducting. The base of transistor Q306 is held well below its emitter potential by means of the voltage divider consisting of resistors R325, R326, D305 and R327. With this bias, transistor Q306 is held in saturation and the flip-flop is desensitized so that even if transistor Q305 turns on, transistor Q306 does not turn off. This desensitizing circuit is an arrangement to prevent inadvertent operation of the flip-flop in the presence of surges on the d-c system. As long as Q306 is conducting, its collector is at a high enough positive potential such that transistor Q307 in the tripping amplifier cannot turn on.

Upon the occurrence of an internal fault, positive 45 volts d-c is applied from Q54 (FD-2) to terminal 18 of the Output board. This removes the desensitizing bias from transistor Q306 by making the potential of the junction of resistor R327 and diode D305 greater than the 20 volt supply for the flip-flop circuit. When this occurs, there is no current flow through resistor R326 and diode D305 and the flip-flop is now "armed" or in a ready condition for a tripping operation. Since the pulses from the "AND" circuit are in phase, after a 4 millisecond delay, the potential across capacitor C305 is sufficient to cause Q305 to conduct. This immediately causes operation of the flip-flop, turning off transistor Q306. When Q306 is no longer conducting, the potential of the junction of R329 and R328 drops to a relatively low value. When this occurs, there is sufficient voltage across the base-emitter circuit of transistor Q307 in the trip amplifier to cause it to turn on.

6. Trip Amplifier

When transistor Q307 is turned on by operation of the flip-flop, base current flows from positive 20 volts through Z305, the emitter-base junction of Q307, and the resistors R328 and R329 to negative. The collector current of transistor Q307 flows through R330 and the base-emitter junction of output transistor Q308. The collector of Q308 is connected to positive 45 volts d-c through R253 and the AR coil of the relay board. Collector current thus flows from positive 45 volts d-c through the AR coil, R253 to transistor Q308, hence, the AR operates to trip the breaker. In case of a voltage output from the SKBU relay, transistor Q252 turns on to provide 20 volts output of the next device.

7. Carrier Squelch

When the SKBU relay operates as a result of an internal fault, positive potential is applied to the squelch circuit of the amplifier and keying board. Ten milliseconds after positive potential is applied, capacitor C101 charges sufficiently to allow base current to flow to transistor Q106. Transistor Q106 turns on to short the carrier start lead to negative (ref. Fig. 7). Carrier is then turned off and will remain off for approximately 150 milliseconds after the SDBU resets to prevent delayed tripping of the remote breaker due to a short burst of carrier at the instant of the local breaker opening.

8. Transient Blocking

When Q54 (FD-2) turns on, positive 45 volts is applied to terminal 18 of the output board, and energizes the transient blocking circuit. Base current is supplied to transistor Q302 through resistor, R305 and Zener diode, C302. Transistor, Q302, turns on to connect the base of transistor, Q303, to negative. Q303 stops conducting and capacitor C303 starts to charge. When the charge on capacitor C303 is sufficient to cause the breakdown of Zener diode Z303, it turns on transistor Q304. This provides a conducting path from the base circuit of transistor Q306 in the flip-flop, diode D304, the resistor R324, and the collector emitter circuit of transistor Q304 to negative. This occurs after a time delay of 20 to 30 milliseconds and provides a path to apply a "desensitizing" bias to transistor Q306 in the flip-flop. Thus, the transient blocking circuit allows 20 to 30 milliseconds after the operation of FD-2 for the flip-flop to operate and energize the output of the relay. If tripping does not occur in this time, as during an external fault, the operation of the transient blocking circuit desensitizes the flip-flop to prevent undesirable operation during transients associated with power reversals on the protective line or at the clearing of an external fault.

The transient blocking circuit is cancelled either by FD-2 resetting or by the operation of the transient unblocking circuit.

9. Transient Unblocking

If an internal fault occurs before an external fault is cleared, high speed tripping is obtained. The square wave output from the local and remote squaring amplifier changes from an out-of-phase condition to an in-phase condition. As a result, negative potential is applied to the transient unblocking circuit at terminal 9 of the Output board. Zener diode Z301 breaks down and base current flows through Z301, emitter-base of Q301, resistor R303, Diode D302, and D301, resistor R130 and through the conducting transistor, Q304, to negative. Transistor Q301 turns on to apply positive potential to resistor, R309. Base current then flows through resistor R309, to turn on transistor Q303. Capacitor, C303, will be rapidly discharged to remove the potential from the base of transistor, Q304. Transistor Q304 turns off to interrupt the desensitizing circuit from the base of transistor Q306. When this happens, the flip-flop will then be able to operate to provide an input to the trip amplifier.

CHARACTERISTICS

The sequence network in the relay is arranged for several possible combinations of sequence components. For most applications, the output of the network will contain the positive, negative and zero sequence components of the line current. In this case, the T taps on the left-hand tap place indicate the balanced three phase amperes which will operate the carrier-start fault detector (FD-1). The taps available are 3, 4, 5, 6, 7, 8 and 10 and are on the primary of the saturating transformer. The second fault-detector unit (FD-2), which supervises operation of tripping, is adjusted to pick up at a current 25 percent above tap value.

For phase-to-phase faults AB and CA, enough negative sequence current has been introduced to allow the fault detector FD-1 to pick up at 86 percent of the tap setting. For BC faults, the fault detector will pick up at approximately 50 percent of the tap setting. This difference in pickup current for different phase-to-phase faults if fundamental, and occurs because of the angles at which the positive and negative sequence components of current add together.

With the sequence network arranged for positive, negative and zero sequence output, there are some applications where the maximum load current and minimum fault current are too close together to set the relay to pickup under a minimum fault current, yet not operate under load. For these cases, a tap is available on the SKBU relay which cuts the three-phase sensitivity in half, while the phase-to-phase setting is substantially unchanged. The relay then trips at 90 percent of tap value for AB and CA faults, and at twice tap value for three-phase faults. The setting for BC faults is 65 percent of tap value. In some cases, it may be desirable to eliminate response to positive-sequence current entirely, and operate the SKBU relay on negative-plus-zero sequence current. A tap is available to operate in this manner. The fault detector picks up at tap value for all phase-to-phase faults, but is unaffected by balanced load current or three-phase faults.

For ground faults, separate taps (Ro) are available for adjustment of the ground fault sensitivity to about 1/4 or 1/8 of the left-hand tap plate setting. See Table II. For example, if the SKBU relay is set at T, tap 4, the fault detector (FD-1) pickup current for ground faults can be either 1 or 1/2 ampere.

In special applications, it may be desirable to eliminate response to zero sequence current. The relay is provided with a tap to allow such operation.

Taps . . . . . 3,4,5,6,7,8,10 (pos. seq.)
A,B,C, (mixture pos.seq.)
F,G,H (zero seq.)

Operating Time . . . . . 12 to 35 milliseconds

Transient Blocking Time . . . . . 20 to 30 milliseconds

Transient Unblocking Time . . . 20 to 30 milliseconds

Squelch Time . . . . . 150 milliseconds

Ambient Temperature Range . . . . . -20°C to 55°C

Output Voltage (where used)
. . . . . 10 milliamperes at 20 volts d-c

Drain on 45 volt Power Supply of TC Set:

Non-Trip Condition . . . . . 60 MA

Trip Condition (with AR output) . . . . . 100 MA

Trip Condition (with voltage output) . . . . . 80 MA

ENERGY REQUIREMENTS

Burdens measured at a balanced three-phase current of five amperes

Relay Taps	Phase A		Phase B		Phase C	
	VA	Angle	VA	Angle	VA	Angle
A-F-3	2.4	5°	0.6	0°	2.5	50°
A-H-10	3.25	0°	0.8	100°	1.28	55°
B-F-3	2.3	0°	0.63	0°	2.45	55°
B-H-10	4.95	0°	2.35	90°	0.3	60°
C-F-3	2.32	0°	0.78	0°	2.36	50°
C-H-10	6.35	342°	3.83	80°	1.98	185°

Burdens measured at a single-phase to neutral current of five amperes.

Relay Taps	Phase A		Phase B		Phase C	
	VA	Angle	VA	Angle	VA	Angle
A-F-3	2.47	0°	2.1	10°	1.97	20°
A-H-10	7.3	60°	12.5	53°	6.7	26°
B-F-3	2.45	0°	2.09	15°	2.07	10°
B-H-10	16.8	55°	22.0	50°	12.3	38°
C-F-3	2.49	0°	1.99	15°	2.11	15°
C-H-10	31.2	41°	36.0	38°	23.6	35°

The angles above are the degrees by which the current lags its respective voltage.

Continuous Rating:

The continuous rating of the relay is 10 amperes. The two second overload rating of the relay is 150 amp. phase and 125 amp. ground.

SETTINGS

The SKBU relay has separate tap plates for adjustment of the phase and ground fault sensitivities and the sequence components included in the network output. The range of the available taps is sufficient to cover a wide range of applications. The method of determining the correct taps for a given installation is discussed in the following paragraphs.

In all cases, the similar fault detectors on the relays at both terminals of a line section must be set to pickup at the same value of line current. This is necessary for correct blocking during faults external to the protected line section.

Sequence Combination Taps

The two halves of the right-hand tap plate are for connecting the sequence network to provide any of

the combinations described in the previous section. The upper half of the tap plate or R1 taps changes the tap on the third winding of the mutual reactor and thus changes the relative amounts of positive and negative sequence sensitivity. Operation of the relay with the various taps is given in the table below.

TABLE I

COMB.	SEQUENCE COMPONENTS IN NETWORK OUTPUT	TAPS ON RIGHT HAND TAP BLOCK		FAULT DETECTOR FD-1 PICKUP	
		R1	Ro	3ϕ Fault	$\phi-\phi$ Fault θ
1	Pos., Neg., Zero	C	G or H#	Tap Value	86% Tap Value (53% on BC Fault)
2	Pos., Neg., Zero	B†	G or H	2 x Tap Value	90% Tap Value (65% on BC Fault)
3	Neg., Zero	A†	G or H	------	100% Tap Value

– Taps F, G and H are zero-sequence taps for adjusting ground fault sensitivity.

See section on zero-sequence current tap.

θ – Fault detector FD-2 is set to pickup at 125% of FD-1 for a two-terminal line, or 250% for a three-terminal line.

† – When taps A and 3 or B and 3 are used, FD-1 will pickup 10 to 15 percent higher than the above values because of the variation in self-impedance of the sequence network and the saturating transformer.

Positive-Sequence Current Tap and FD-2 Tap

The left-hand tap plate, T, has taps of 3, 4, 5, 6, 7, 8 and 10 which represent the three-phase, fault detector FD-1 pickup currents, when the relay is connected for positive, negative and zero sequence output. The fault detector FD-2 closes its contact to allow tripping at current value 25 percent above the fault detector FD-1 setting. This 25 percent difference is necessary to insure that the carrier-start fault detectors (FD-1) at both ends of a 2-terminal transmission line section pickup to start carrier on an external fault before operating energy is applied through FD-2.

For a 3-terminal line, there is a provision on the printed circuit board for changing the temperature compensation when calibrating FD-2 to pickup at 250% of FD-1 setting. This is necessary to allow proper blocking on 3-terminal lines when approximately equal currents are fed in two terminals, and their sum flows out the third terminal of the line. The relay is shipped connected for 2 terminal line service. For a 3-terminal line, the jumper on the FD board must be changed to c-3, and FD-2 must be recalibrated for 250% of FD-1.

The T, Ro, and R1 taps should be selected to assure operation on minimum internal line-to-line faults, and yet not operate on normal load current, particularly if the carrier channel is to be used for auxiliary functions. The dropout current of the FD-1 fault detector is 80 percent of the pickup current, and this factor must also be considered in selecting the positive-sequence current tap and sequence component combination. The margin between load current and fault detector pickup should be sufficient to allow the fault detector to dropout after an external fault, when load current continues to flow.

Zero-Sequence Current Tap – Ro Taps

The lower half of the right-hand tap plate (Ro taps) is for adjusting the ground fault response of the relay. Taps G and H give the approximate ground fault sensitivities as listed in Table II. Tap F is used in applications where increased sensitivity to ground faults is not required. When this tap is used, the voltage output of the network caused by zero-sequence current is eliminated.

NOTE: Because of inherent characteristics of the sequence network, there will be small variations (from the values listed in Tables I and II) in the pickup current for various phase or ground fault combinations.

TABLE II

COMB.	R1 TAP	GROUND FAULT PICKUP PERCENT OF T TAP SETTING	
		TAP G	TAP H
1	C	25%	12%
2	B	20%	10%
3	A	20%	10%

Examples of SKBU Relay Settings

CASE I

Assume a two-terminal line with current transformers rated 400/5 at both terminals. Also assume that full load current is 300 amperes, and that on minimum internal phase-to-phase faults 2000 amperes is fed in from one end and 600 amperes from the other end. Further assume that on miminum internal ground faults, 400 amperes is fed in from one end, and 100 amperes from the other end.

Positive Sequence Current Tap

Secondary Values:

$$\text{Load Current} = 300 \times \frac{5}{400} = 3.75 \text{ amperes} \quad (1)$$

Minimum Phase-to-phase Fault Currents:

$$600 \times \frac{5}{400} = 7.5 \text{ amperes} \quad (2)$$

Fault detector FD-1 setting (three phase) must be at least:

$$\frac{3.75}{0.80} = 4.7 \text{ amperes} \quad (3)$$

(0.80 is dropout ratio of FD-1. Setting will insure that the fault detector will reset on load current)

In order to complete the trip circuit on a 7.5 ampere phase-to-phase fault, the fault detector FD-1 setting must not be more than:

From Table I (based on a three phase fault)

$$7.5 \times \frac{1}{0.8} \times \frac{1}{1.25} = 6.93 \text{ amperes}$$

$$1.25 = \frac{\text{FD-2 Pickup}}{\text{FD-1 Pickup}} \quad (4)$$

Sequence Combination Tap

From a comparison of (3) and (4) above, it is evident that the fault detector can be set to trip under minimum phase fault condition yet not operate under maximum load. In this case, tap C would be used (see Table I, Comb. 1) as there is sufficient difference between maximum load and minimum fault to use the full three-phase sensitivity. Current tap 6 would be used in preference to tap 5 to allow for occurrence of higher load current.

Zero Sequence Tap

Secondary Value:

$$100 \times \frac{5}{400} = 1.25 \text{ amperes minimum ground fault current}$$

With T tap 6 and R1, tap C in use, the fault detector FD-1 pickup currents for ground faults are as follows:

Tap G 1/4 x 6 = 1.5 ampere
Minimum Trip = 1.25 x 1.5 = 1.88 ampere

Tap H 1/8 x 6 = 0.75 ampere
Minimum Trip = 1.25 x 0.75 = 0.94 ampere

From the above, tap H would be used to trip for a minimum ground fault of 1.25 amperes.

CASE II

Assume the same fault currents as in Case I, but a maximum load current of 550 amperes. In this example, with the same sequence combination as in Case I, the fault detectors cannot be set to trip on the minimum internal three-phase fault, yet remain inoperative on load current. Compare equations (5) and (6). However, by connecting the network per combination 2 on Table I, the relay can be set to trip on minimum phase-to-phase fault, although it will have only half the sensitivity to three-phase faults. This will allow operation at maximum load without picking up the fault detector, and provide high speed relaying of all except light three-phase faults.

In order to complete the trip circuit on a 7.5 ampere phase-to-phase fault, the fault detector tap must now be not more than:

$$7.5 \times \frac{1}{1.25} \times \frac{1}{0.9} = 6.67 \text{ amperes} \quad (5)$$

To be sure the fault detector FD-1 will reset after a fault, the minimum tap setting is determined as follows.

$$\text{Load Current} = 550 \times \frac{5}{400} = 6.9 \text{ amperes} \quad (6)$$

$$\frac{6.9}{0.80} = 8.6 \quad (7)$$

Since from Table 1 comb. 2 the fault detector pickup current for three-phase faults is twice tap value, half the above value (Eq. 7) should be used in determining the minimum three-phase tap.

$$\frac{8.6}{2} = 4.3 \qquad (8)$$

From a comparison of (5) and (8) above, tap 5 or 6 could be used. (Continuous load current rating of relay is 10 amperes.)

With the three-phase tap 5 in use, the fault detector pickup current for ground faults will be as follows:

Tap G	1/5 x 5	= 1.0 ampere (FD-1)
Minimum Trip	= 1.0 x 1.25 a.	= 1.25 ampere (FD-2)

Tap H	1/10 x 5	= 0.5 ampere (FD-1)
Minimum Trip	= 1.25 x 0.5 a.	= 0.63 ampere (FD-2)

Therefore, tap H would be used to trip the minimum ground fault of 1.25 ampere with a margin of safety.

✪ INSTALLATION

The relays should be mounted on switchboard panels or their equivalent in a location free from dirt, moisture, excessive vibration and heat. The maximum ambient temperature around the chassis must not exceed 55°C. Mount the relay by means of the four slotted holes on the front of the case. Additional support should be provided toward the rear of the relay in addition to the front panel mounting. This will protect against warping of the front panel due to the extended weight within the relay case. Ground relay chassis is with No. 12 AWG copper wire to grounding post.

ADJUSTMENTS AND MAINTENANCE

NOTE: The SKBU relay is normally supplied as part of a carrier relaying system, and its calibration should be checked after the system has been installed and interconnected. Details are given in the instructions of the assembly. The assembly instructions and not the following instruction should be followed when the relay is received as an integral part of the relaying system.

In those cases where the SKBU relay is not a part of a relaying system, the following procedure can be followed to verify that the circuits of the SKBU relay are functioning properly.

Test Equipment:

1. Oscilloscope
2. A.C. Current Source
3. Electronic Timer
4. A.C. Voltmeter
5. D.C. Voltmeter

Acceptance Test

Connect the relay to the test circuit of Fig. 8 which represents the TC carrier channel for test purposes. Open all test switches of the test circuit and connect a 60 hertz test current between terminals 3 and 4 of the relay. Set relay taps on C and & and remove T tap screw.

1. Filter Output

a. Connect a high resistance a-c voltmeter across common of T tap block and the common of Ro tap block.

b. Pass with 3.44 amperes, 60 hertz into terminal 3 and out terminal 4 of relay. Voltmeter should read between 0.75 volts and 0.85 volts a-c.

2. FD-1 Pickup and Dropout

a. Set relay taps 5, C and H. Close all switches of test circuit.

b. Connect a high resistance d-c voltmeter across X14 and X3 (Neg.).

c. Apply 60 hertz current to terminals 3 and 4 of the relay. Gradually increase the current until the voltmeter changes reading from approximately zero volts to approximately 20 volts. This is the operating current of FD-1 and should be 4.33 ± 5% amperes.

d. Gradually lower a-c test current until the d-c voltmeter drops to approximately zero volts. This is the dropout current of FD-1 and should occur at 80% of the pickup current.

3. FD-2 Pickup and Dropout

a. With the current test leads connected as in the FD-1 test, connect the voltmeter across X13 and X3 (Neg.)

b. Gradually raise a-c current until voltmeter reads approximately 45 volts. This should be 5.41 ± 5% amperes.

c. Gradually lower a-c test current until the d-c voltage reading drops to zero volts. This is dropout of FD-2 and should occur at 90% of pickup current.

4. Check of Local Squaring Amplifier

a. Open switches A, B, C, D and E of test circuit.

b. Place scope across X10 and X3 (GRD). Apply 5 amperes a-c to terminals 3 and 4 of relay.

c. A square wave voltage should appear across X10 and X3 with the waveshape of Fig. 9.

5. Check of Keying Circuit

a. Open all switches of test circuit and apply 5 amperes a-c to terminals 3 and 4 of the relay.

b. With scope check voltage across X11 and X3 (GRD). Waveform should be a square wave as shown in Fig. 9.

c. Close switches A, B, C and D. No change should be noted in waveform across X11 and X3 (GRD).

6. Check of Remote Squaring Amplifier

a. Close switches A, B and C of the test circuit.

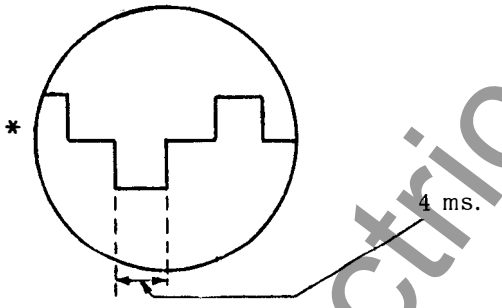
b. Apply 5 amperes a-c to terminals 3 and 4 of the SKBU relay.

c. Put scope across X9 and X3 (GRD). A square wave of voltage should be obtained (see Fig. 9.)

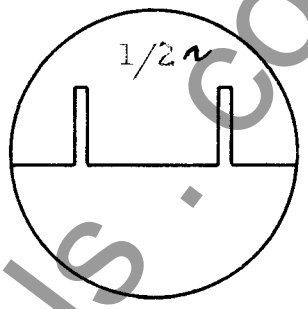
7. Setting of S5 and S6

a. Set S5 to minimum resistance and S6 to maximum resistance (fully clockwise).

b. With switches A, B and C of the test circuit closed, apply 6 amperes a-c to terminals 3 and 4 of the SKBU relay.



c. Place scope across X12 and X2 (GRD). Adjust S5 until following waveform is obtained.



Equal Pips may point up as shown or down

d. Close switch D and adjust S6 until the AR trips. In the case of a voltage output SKBU relay, place d-c voltmeter across X16 and X3. Tripping is indicated by a change in voltage from 0 to 20 volts. This sets the triggering of the flip-flop after a 4 millisecond delay. Recheck pickup by moving S5 minimum, opening and closing switch D and then adjusting S5 until AR operates. it may be necessary to re-adjust S6 to obtain AR tripping on waveform of step c.

e. Slowly increase S5 to obtain the following waveform. Adjust for minimum area of the pips. This will be with S5 near minimum resistance.

8. Check of Transient Blocking

a. Connect electronic timer stop to X7 and X3 (GRD). Set timer stop on negative going pulse.

b. Connect timer start to timer start contacts of switch D. Set timer start to make.

c. With switches A, B and C open, apply 6 amperes a-c to terminals 3 and 4 of the SKBU relay.

d. Close switch D and measure time for voltage to drop from 20 volts to approximately zero volts. This should be between 20 to 30 milliseconds. Take average of ten readings.

9. Check of Transient Unblocking Circuit

a. With electronic timer stop connected to X7 and X3 (GRD), set timer stop on positive going pulse. Also connect a-c voltmeter across X7 and X3 (NEG.).

b. Connect timer start to timer start contacts of switch A.

c. Apply 6 amperes a-c to terminal 4 and 3 of the SKBU relay, and close switches A, B, C and D of test circuit. Closing switch D sets up transient blocking as can be seen by a change in voltage from 20 volts d-c to 0 volt d-c.

d. Open switch A and measure time for voltage to change from approximately zero volt to 20 volts. Time should be 20 to 30 milliseconds. Measure average of 10 trials. For each trial it will be necessary to close switch A and then open switch D. Switch D should then be closed and A opened to measure the unblocking time.

10. Check of Carrier Squelch Circuit

a. Connect timer stop across X11 and X3 GRD. Set timer stop on negative pulse.

b. Connect timer start. Set timer start to make.

c. Open switch C. Approximately 20 volts should appear across X11 and X3.

d. Close switch E and measure time for voltage to disappear. This should be 8 to 12 milliseconds.

e. Set timer stop on positive pulse and timer start on break.

f. Measure time for voltage to reappear by opening switch E. Time should be 120 to 180 milliseconds.

ROUTINE MAINTENANCE

All contacts should be periodically cleaned. A contact burnisher S#182A836H01 is recommended. The use of abrasive material is not recommended because of the danger of embedding small particles in the face of the soft silver and thus impairing the contact.

CALIBRATION

Use the following procedure for calibrating the relay if the relay has been taken apart for repairs. The relay should be connected to the test circuit of Fig. 8.

1. Sequence Filter

To calibrate the sequence filter, the top cover must be removed and the following procedure used: Remove the T tap screw and insert the tap screws in tap C and H of the R1 and Ro taps. Pass a single-phase current of 10 amperes, rated frequency through the reactor coils in series from phase B to phase C (relay terminals 4 and 5). Accurately measure the a-c voltage from terminal 3 to the common of the T tap plate. This voltage should be between 3.7 and 4.1 volts. Now pass 10 amperes from terminal 3 to terminal 4 with tap screw C removed, and connect voltmeter from terminal 3 to the right-hand (front view) adjustable point of the formed resistor. Adjust this point to give a voltage equal to exactly one-third of the reactor drop. Note the above reading, and adjust the intermediate tap of formed resistor to give exactly 2/3 of the voltage obtained above for all of formed resistor. Measure this voltage from terminal 3 to the intermediate tap.

2. Phase Splitter

If replacement of the fault detector board or major component on the board necessitates a complete recalibration, proceed as follows:

a. Set relay taps 5-C-H.

b. Set S1 and S3 to full clockwise position.

c. Set S2 and S4 to mid-scale.

d. Pass 4.33 amperes through relay terminal 3 to terminal 4.

e. On fault detector board, check the a-c voltage from TP51 to TP52 and from TP52 to TP53 with a VTVM. Adjust the small pot. R53 on the fault detector board until these two voltages are equal.

f. Close all switches of test circuit and connect VTVM across X14 and X3 (Neg.)

g. Slowly turn S3 counterclockwise, with 4.33 amperes flowing, until FD-1 operates as indicated by a change in voltage reading from approximately zero volts to 20 volts d-c.

h. Reduce the a-c current to check FD-1 dropout. Adjust S4 to obtain 80 percent dropout (3.46 amperes). Dropout is indicated by a change in voltage reading from approximately 20 volts to 0 volt.

i. Recheck FD-1 pickup and dropout, and touch up S3 and S4 in that order for the correct calibration. Tighten the locking device.

j. Similarly recalibrate FD-2 using controls S1 (pickup) and S2 (dropout), repeating steps g, h and i, except for FD-2 pickup of 5.41 amperes and dropout of 4.85 amperes. Pickup is measured using X13 and X3 (negative) and is indicated by a change in voltage reading from a low voltage to 45 volts.

3. Tripping Relay (AR)

The type AR tripping relay unit has been properly adjusted at the factory to insure correct operation and should not be disturbed after receipt by the customer. If, however, the adjustments are disturbed in error, or it becomes necessary to replace some part in the field, use the following adjustment procedure. This procedure should not be used until it is apparent that the AR unit is not in proper working order, and then only if suitable tools are available for checking the adjustments.

a. Adjust the set screw at the rear of the top of the frame to obtain a 0.009 inch gap at the rear end of the armature air gap.

b. Adjust each contact spring to obtain 4 grams pressure at the very end of the spring. This pressure is measured when the spring moves away from the edge of the slot in the insulated crosspiece.

c. Adjust each stationary contact screw to obtain a contact gap of 0.020 inch. This will give 15-30 grams contact pressure.

4. Check of Solid-State Circuits

Perform tests listed under "Acceptance" tests to verify that the SKBU relay is functioning correctly.

TROUBLE SHOOTING PROCEDURE

To trouble shoot the equipment, the logic diagram of either Fig. 5 or 6, voltages of Fig. 9, should be used to isolate the circuit that is not performing correctly. The schematic of either Fig. 3 or 4, and the voltages of Table IV should then be used to isolate the faulty component.

TABLE IV
VOLTAGE MEASUREMENTS OF PRINTED CIRCUIT BOARD

1. Fault Detector Board

D–C Voltages – positive with respect to negative d-c (terminal 8 of board).

TEST POINT	I = 0	I = 2 x FD-2 p.u.
Terminal 14	45.0 VDC	45.0 VDC
TP 54	6.6	6.8
TP 55	6.6	less than 1
TP 56	14.5	less than 1
TP 57	less than 1	14.5
TP 58	45	less than 1
Terminal 13 FD-1	less than 1	20
Terminal 15 FD-2	less than 1	45
TP 52 – TP 51	less than 1	18 VAC Approximately
TP 52 – TP 53	less than 1	17.8 VAC Approximately

2. Amplifier and Keying

D–C Voltages – positive with respect to negative (terminal 8 of board).

TEST POINT	NORMAL	FAULT
Terminal 4	20	20
TP 101	20	10
TP 102	20.3	19.8
TP 103	less than 1	10
Terminal 3	less than 1	19.8

3. Output Board

D–C Voltages – positive with respect to negative (terminal 8 of board).

TEST POINT	NORMAL	FAULT
TP 302	19.5	19.0
TP 301	10	8.5
Terminal 14	20	19.0

RENEWAL PARTS

Repair work can be done most satisfactorily at the factory. However, interchangeable parts can be furnished to the customers who are equipped for doing the repair work. When ordering parts, always give the complete nameplate data. For components mounted on the printed circuit board, give the circuit symbol and the nameplate value (ohms, mfd, etc.).

ELECTRICAL PARTS LIST

CIRCUIT SYMBOL	DESCRIPTION	W STYLE NO.
FAULT DETECTOR BOARD STYLE 898C314G01		
Capacitor		
C51	0.10 MFD	1549220
C52	0.5	187A624H11
C53	0.25	187A624H02
C54	1.0	187A624H04
C55	1.5	187A508H09
Diodes		
D51 to D56 – D61	1N459A	184A855H08
D59 to D60 – D62	1N457A	184A855H07
Transistors		
Q51-Q52-Q56-Q57	2N697	184A638H18
Q53	2N699	184A638H19
Q54	2N4356	849A441H02
Q55	2N652A	184A638H16
Resistors		
R51	50 Ohm, 5W	185A209H06
R52	9.1K Ohm, ½W	187A763H50
R53	2.5K Ohm, Pot.	629A430H03
R54	2.7K Ohm, ½W	629A530H42
R55-R73-R78	10K Ohm, ½W	629A530H56
R56-R58	15K Ohm, ½W	187A641H55
R57	18K Ohm, ½W	184A763H57
R59	Thermistor 1D05N	185A211H05
R60-R65	68K Ohm, ½W	187A641H71
R61	.22 Meg. Ohm, ½W	184A763H83
R62-R64-R68-R74	10K Ohm, ½W	187A641H51
R63	.1 Meg. Ohm, ½W	187A641H75
R66	470K Ohm, ½W	184A763H91
R67	39K Ohm, ½W	187A641H65
R69	10K Ohm, ½W	187A641H51
R70	6.8 Ohm, ½W	187A641H47
R71	20K Ohm, ½W	629A530H63
R72	3.9K Ohm, 1W	187A643H41
R75	33K Ohm, ½W	187A641H63
R76	10K Ohm, 1W	187A643H51
R77	1K Ohm, ½W	629A530H43

CIRCUIT SYMBOL	DESCRIPTION	W STYLE NO.
FAULT DETECTOR BOARD (Con't.)		
Zener Diodes		
Z51	1N1832C	184A617H06
Z52-Z54	1N957B	186A797H06
Z53	1N1789	584C434H08
Z55	1N3686B	185A212H06
AMPLIFIER AND KEYING 898C399G01		
Capacitor		
C101	39 MFD	187A508H04
Diodes		
D101-D102-D104-D106 to D113	1N457A	184A855H07
D103	1N91	182A881H04
Transistors		
Q101-Q102-Q107-Q108	Matched Pair 2N652A	671B632G01
Q105-Q106	2N697	184A638H18
Q103-Q104-Q109-Q111	2N3645	849A441H01
Q112-Q113	2N652A	184A638H16
Resistors		
R101-R103-R114-R127	100K Ohm, ½W	187A641H75
R102	100K Ohm, ½W	184A763H75
R104-R131	33K Ohm, ½W	187A641H63
R105	68K Ohm, ½W	187A641H71
R106	27K Ohm, ½W	187A641H61
R107-R119-R123	4.7K Ohm, ½W	187A641H43
R108-R109-R126	10K Ohm, ½W	187A641H51
R110	3.3K Ohm, ½W	184A763H39
R111	5.6K Ohm, ½W	187A641H45
R112	1.2K Ohm, ½W	184A763H29
R113	330 Ohm, 2W	185A207H15
R115	100K Ohm, ½W	187A641H75
R116-R130	22K Ohm, ½W	187A641H59
R118-R121-R129	47K Ohm, ½W	187A641H67
R120-R122	470K Ohm, ½W	187A641H91
R124-R125	15K Ohm, ½W	187A641H55
R128-R117	39K Ohm, ½W	187A641H65
Zener Diode		
Z101	1N748A	186A797H13

ELECTRICAL PARTS LIST (Con't.)

CIRCUIT SYMBOL	DESCRIPTION	W STYLE NO.
OUTPUT BOARD 898C316G02		
Capacitors		
C301	1.0 MFD	187A624H04
C302	0.25 MFD	187A624H02
C303	3.0 MFD	188A293H06
C304-C306	0.05 MFD	187A624H08
C305	0.22	188A293H02
Diodes		
D301-D304-D305-D306	1N457A	184A855H07
D302-D303	1N91	182A881H04
Transistor		
Q301-Q305-Q306-Q307	2N652A	184A638H16
Q302-Q303-Q304	2N697	184A638H18
Q308	2N699	184A638H19
Resistors		
R301-R303-R309-R310-R313-R324-R325	10K Ohm, ½W	187A641H51
R302	120K Ohm, ½W	187A641H77
R304	47 Ohm, ½W	187A640H17
R305	8.2K Ohm, ½W	187A641H49
R306-R315-R322	4.7K Ohm, ½W	187A641H43
R307-R331	2.2K Ohm, ½W	187A641H35
R308-R320	6.8K Ohm, ½W	187A641H47
R311	470 Ohm, ½W	187A641H19
R312	470K Ohm, ½W	187A641H91
R316-R321-R323	22K Ohm, ½W	187A641H59
R317-R328-R332	5.6K Ohm, ½W	184A763H45
R318	15K Ohm, ½W	187A641H55
R319	Thermistor 1D101	185A211H04
R326-R329	4.7K Ohm, ½W	184A763H43
R327	6.8K Ohm, ½W	184A763H47
R330	1.5K Ohm, ½W	187A641H31

CIRCUIT SYMBOL	DESCRIPTION	W STYLE NO.
OUTPUT BOARD (Con't.)		
Zener Diodes		
Z301-Z303-Z305	1N957B	186A797H06
Z302	1N965B	186A797H08
Z304	1N960B	186A797H10
Z306	1N1789	584C434H08
RELAY BOARD 898C318G02		
Capacitors		
C251-C252-C253	0.25 MFD	187A624H02
C254	0.02	1544921
Resistors		
R251-R252	2.2K Ohm, ½W	187A641H35
R253	800 Ohm, 3W	184A859H06
R254	150 Ohm, 1W	1724641
Filter Choke		
L251	8.5HY, 400 Ohm	188A460H01
Trip		
AR		408C845G09
Where a voltage output is required, the AR relay, R253 and C254 are omitted and the following additional parts are located on the board. Style of board is 899C273G01.		
Capacitors		
C254	0.25 MFD	187A624H02
Diode		
D251-D252	1N459A	184A855H08
D253	CER-69	188A342H06
Transistors		
Q251-Q252	2N4356	849A441H02
Resistors		
R253-R256	10K Ohm, ½W	184A763H51
R254	2.2K Ohm, 3W	184A859H15
R255	330 Ohm, 5W	837A233H07
R257	10K Ohm, ½W	184A763H51
R259	2.25K Ohm, 3W	184A636H03
Zener Diode		
Z251	1N3686B	185A212H06

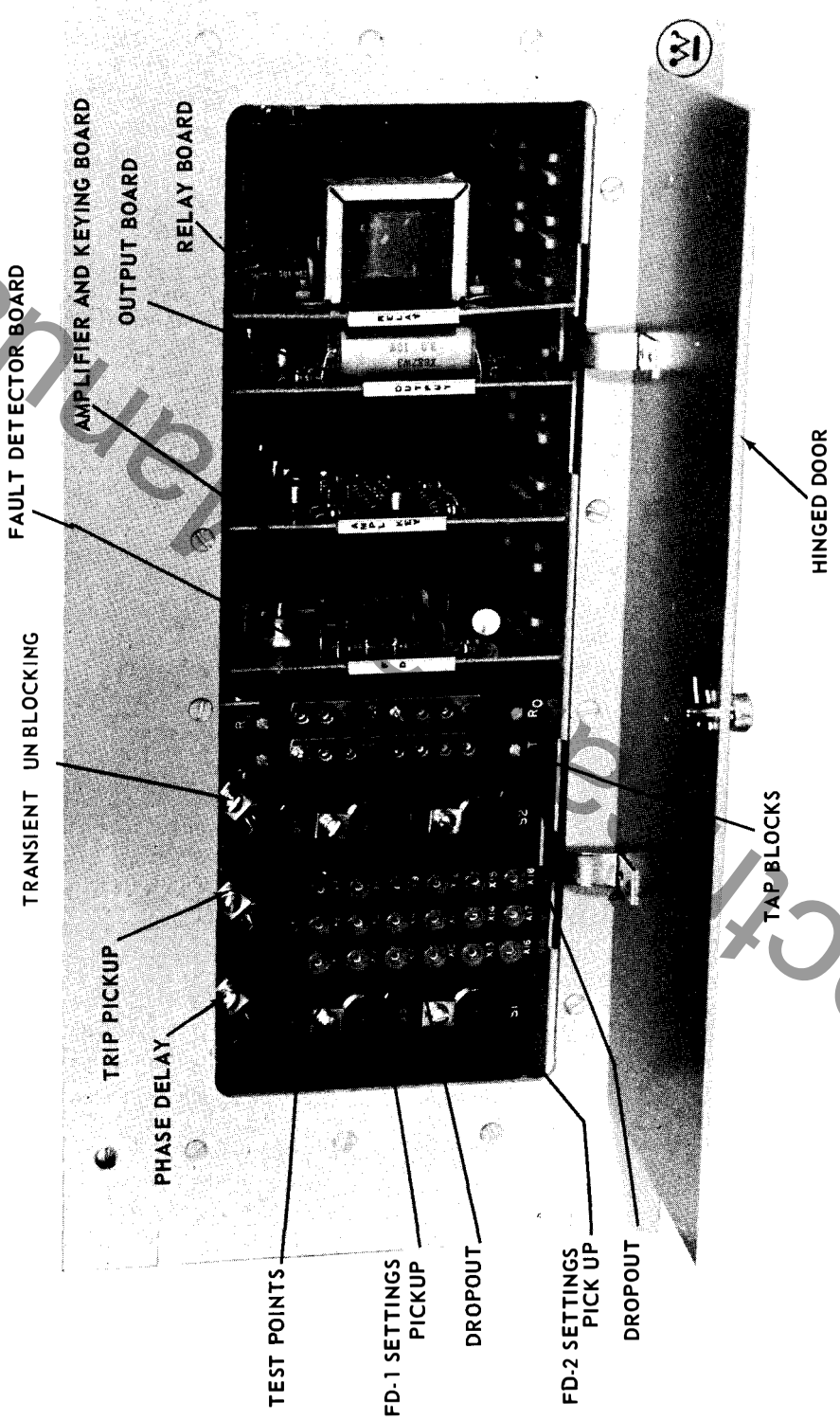


Fig. 1. Type SKBU Phase Comparison Relay (Front View). N365472

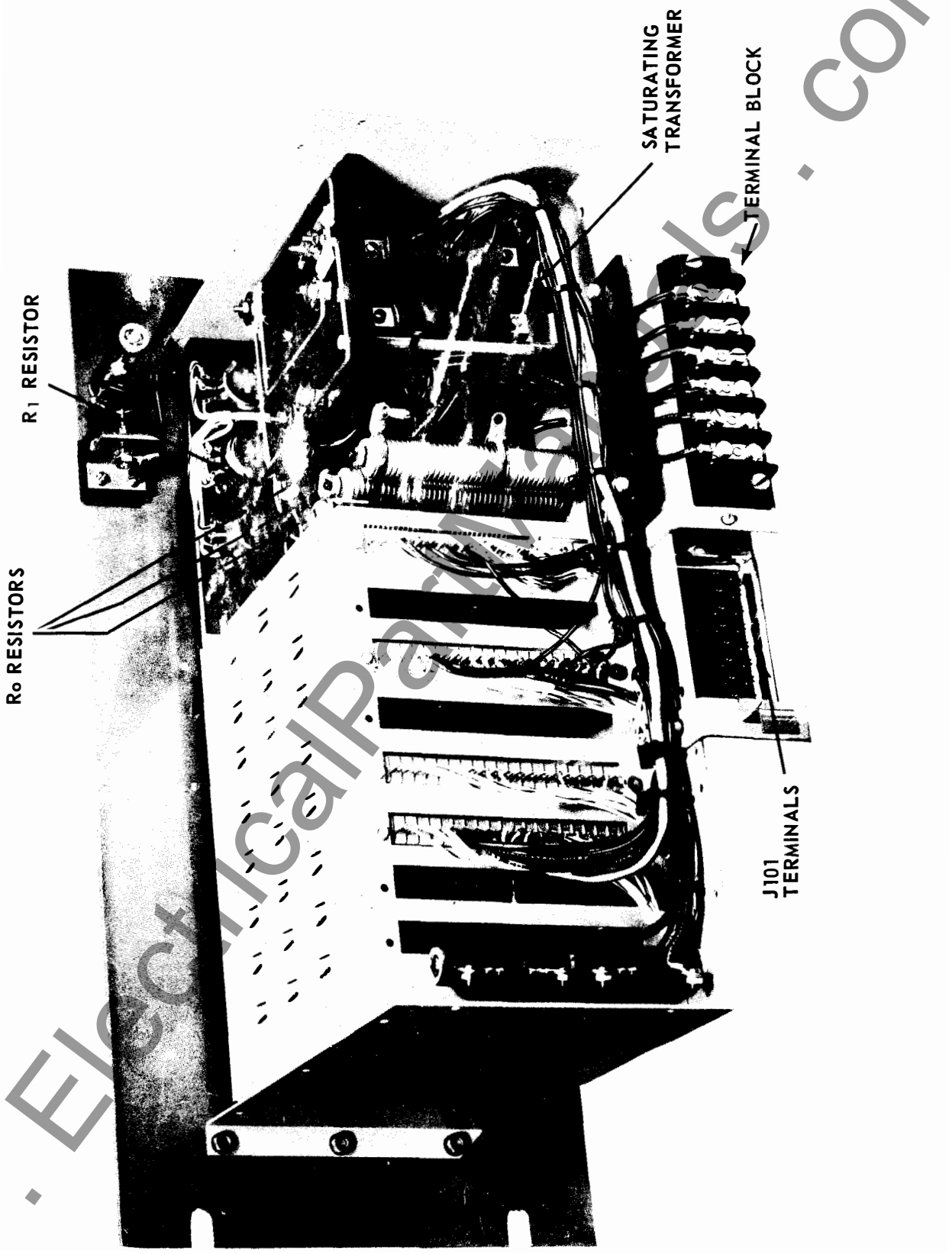
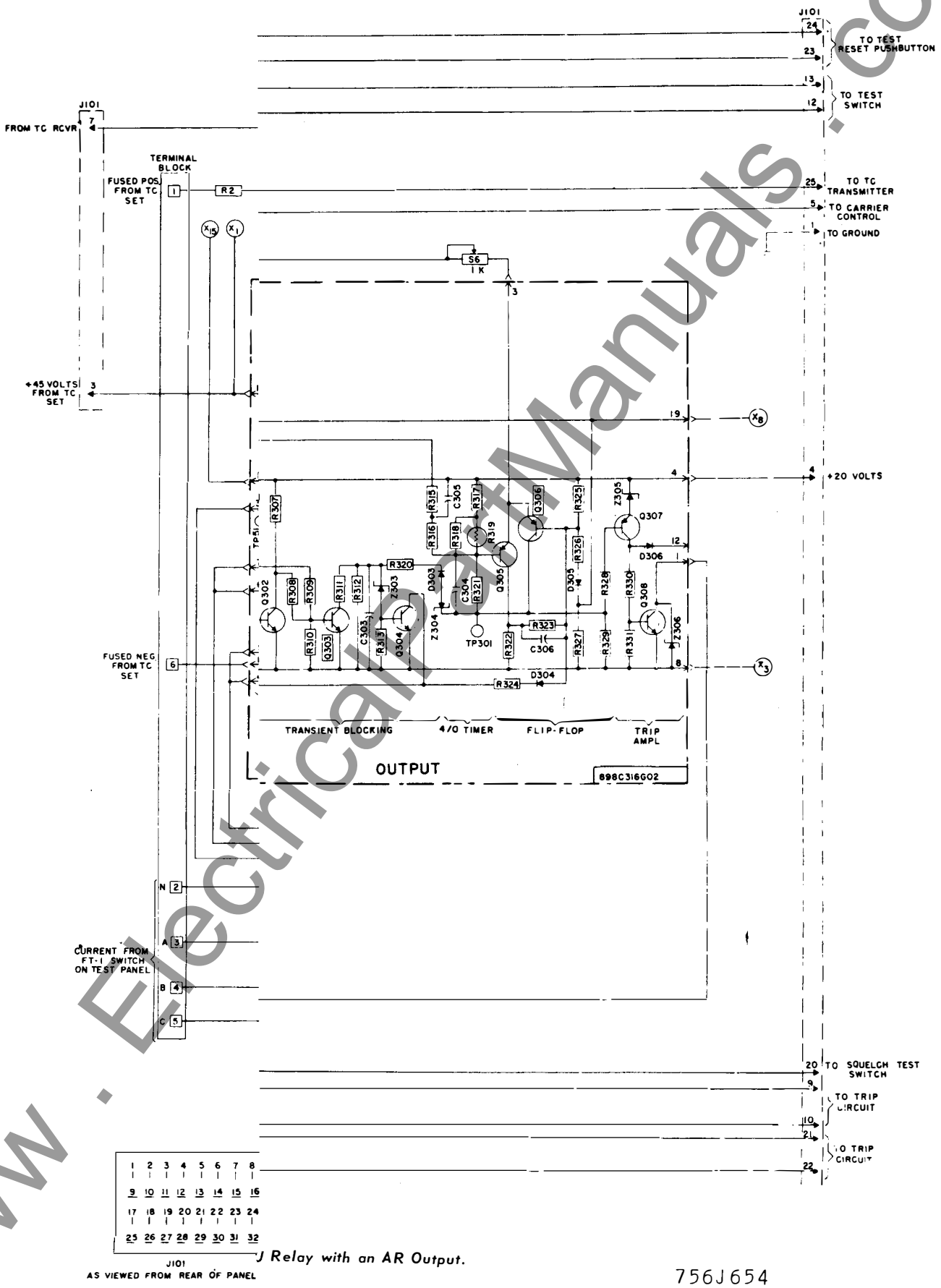
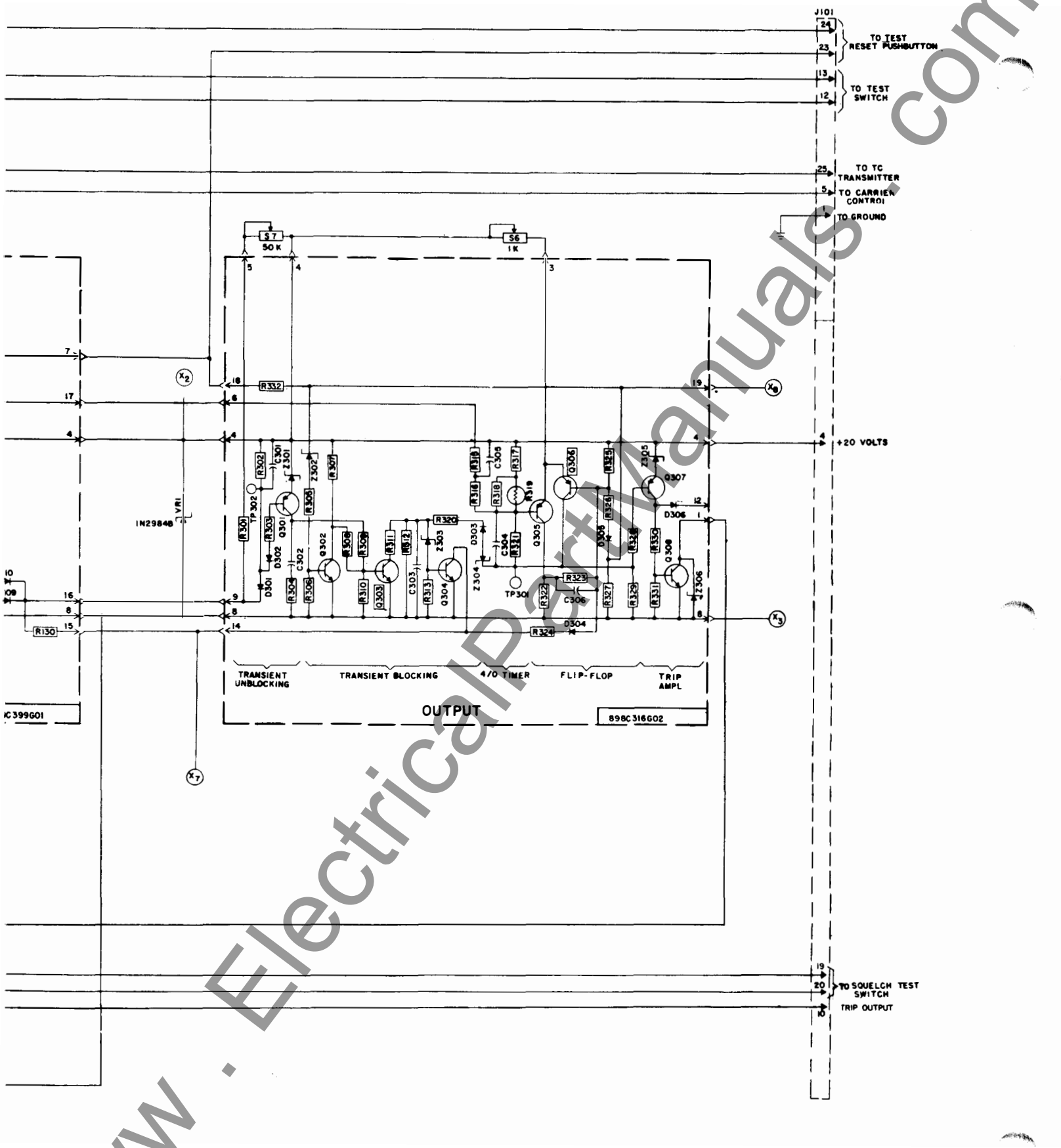


Fig. 2. Type SKBU Phase Comparison Relay (Rear View). N365471



J Relay with an AR Output.

756J654



Schematic of the Type SKBU Relay with Voltage Output.

756J704

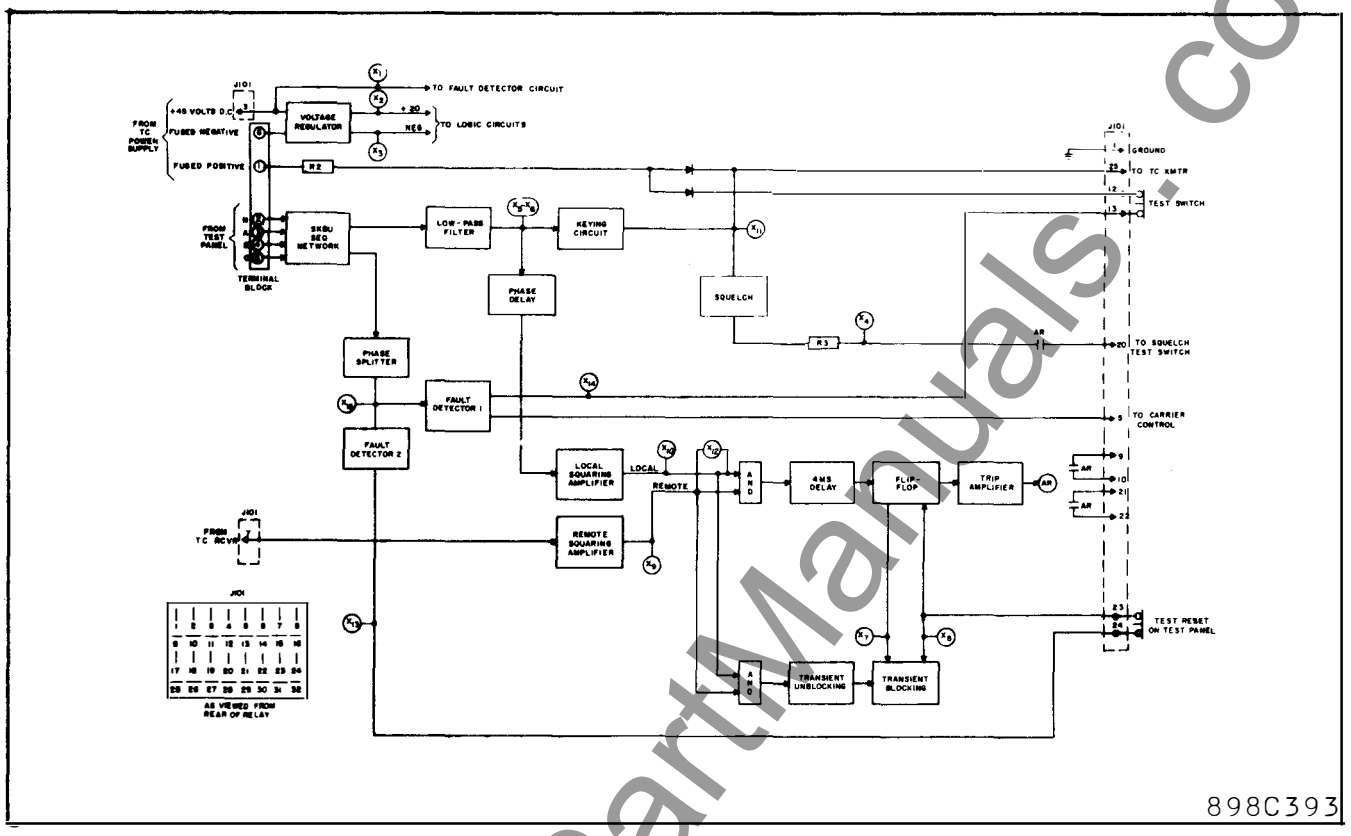


Fig. 5. Logic Diagram of the Type SKBU Relay with an AR Output.

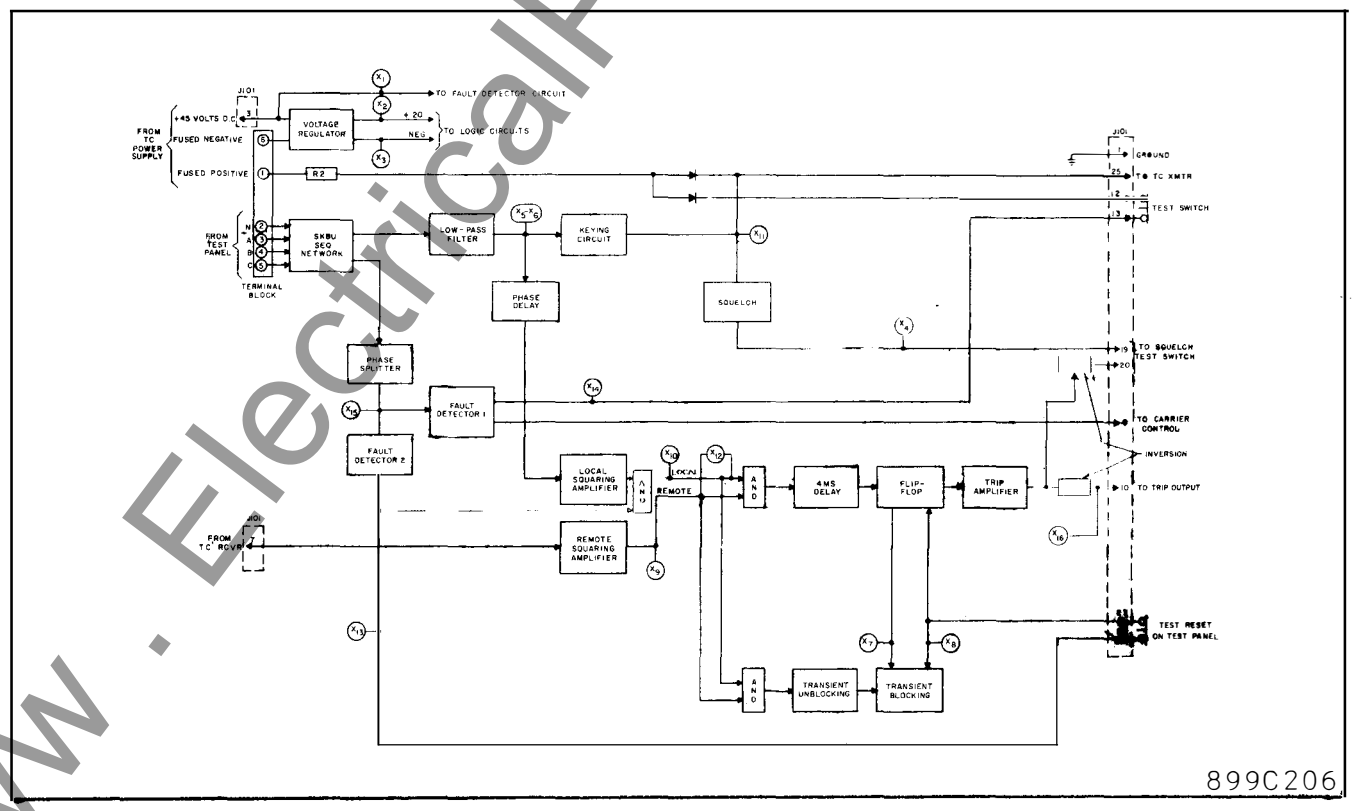


Fig. 6. Logic Diagram of the Type SKBU Relay with a Voltage Output.

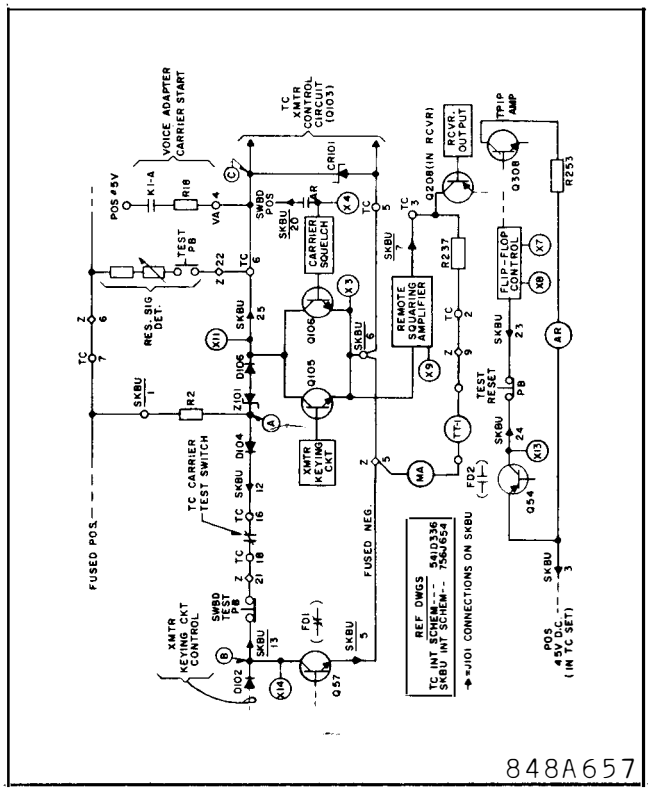


Fig. 7. Elementary Connections of TC SKBU Control Circuits.

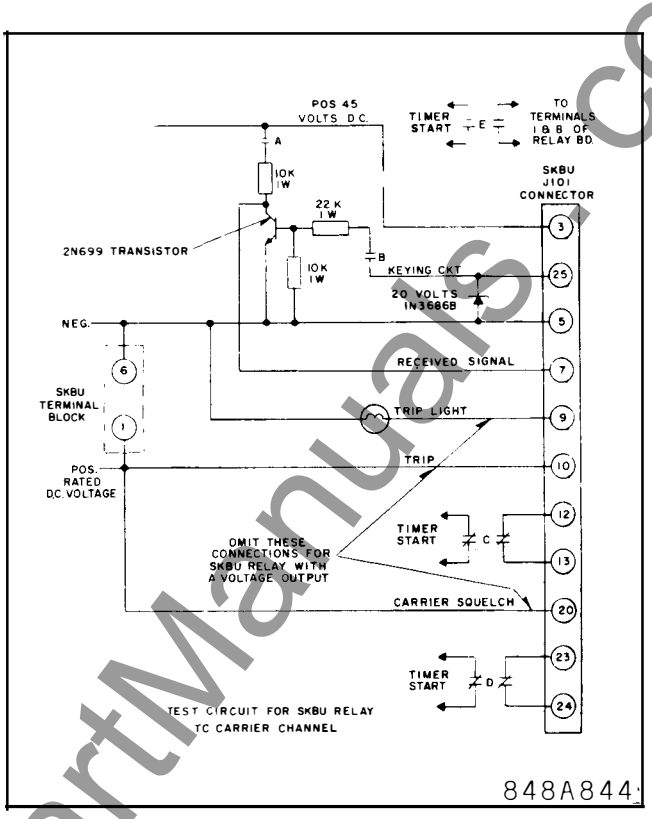


Fig. 8. Test Circuit of SKBU Relay.

TEST POINT	CIRCUIT	VOLTAGES TO X3 (EXCEPT WHERE SPECIFIED)		
		NORMAL**	EXTERNAL FAULT	INTERNAL FAULT
X1	POSITIVE 45 VOLTS FROM TC SET	+45	+45	+45
X2	REGULATED 20 VOLTS D.C.	+20	+20	+20
X3	NEGATIVE FROM TC SET	—	—	—
X4	CARRIER SQUELCH	0	0	RATED SUPPLY VOLTAGE
*X5 / *X6	LOW PASS FILTER VOLTAGE AT 2 TIMES PICKUP OF FD-1	0	4 TO 7 VOLTS RMS	4 TO 7 VOLTS RMS
X7	TRANSIENT BLOCKING	20	0	20
X8	ARMING	12	+20	+20
X9	REMOTE SQUARING AMPLIFIER	0	20 / 0	20 / 0
X10	LOCAL SQUARING AMPLIFIER	20	20 / 0	20 / 0
X11	KEYING	0	20 / 0	20 / 0
ΔX12	LOCAL REMOTE COMPARER	—	0 / 2	0 / 2
X13	FD-2	0ø	+45	+45
X14	FD-1	0	+20	+20
X15	PHASE SPLITTER AT 2 TIMES PICKUP OF FD-1	0	16V DC / 0	16V D.C. / 0
X16	TRIP OUTPUT-SKBU RELAY WITH VOLTAGE OUTPUT ONLY	0	0	20 VOLTS D.C.

* = VOLTS A.C. ACROSS X5 AND X6 ** NO LOAD CURRENT
Δ = VOLTS D.C. TO X2
ø = READING VARIES WITH VOLTMETER USED

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Fig. 9. Table III, Voltages of SKBU Relay.

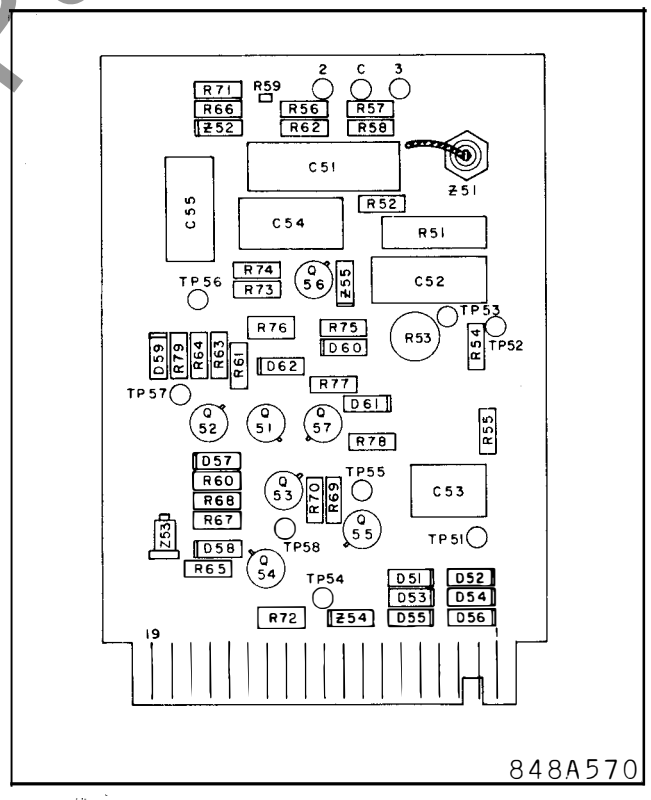

Fig. 10. Component Location on Fault Detector Printed Circuit Board for Type SKBU Relay.

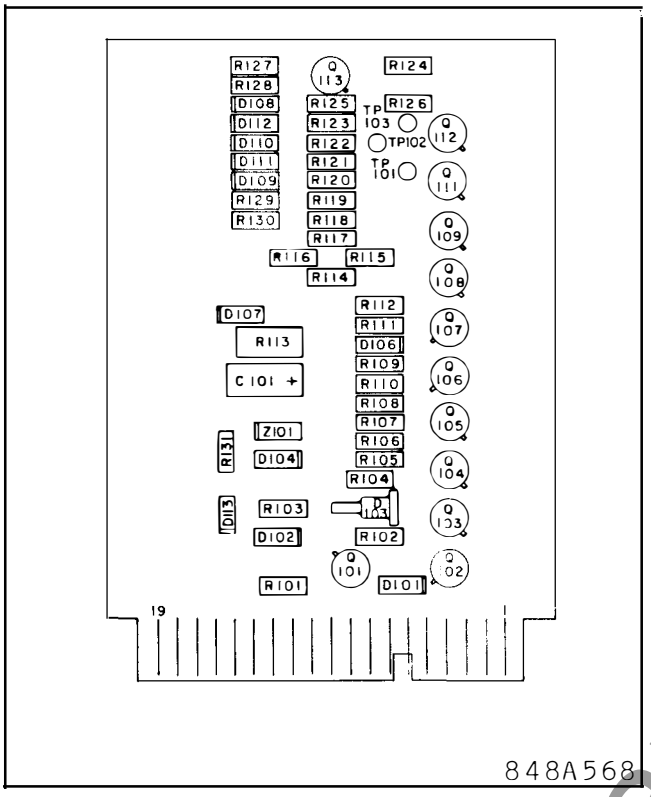

Fig. 11. Component Location on Amplifier and Keying Printed Circuit Board for Type SKBU Relay.

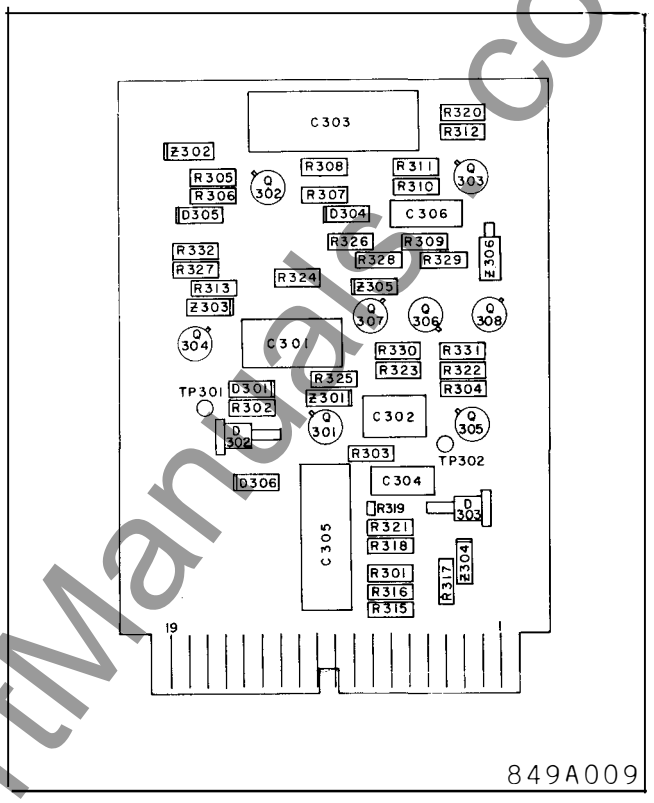

Fig. 12. Component Location on Output Printed Circuit Board for Type SKBU Relay.

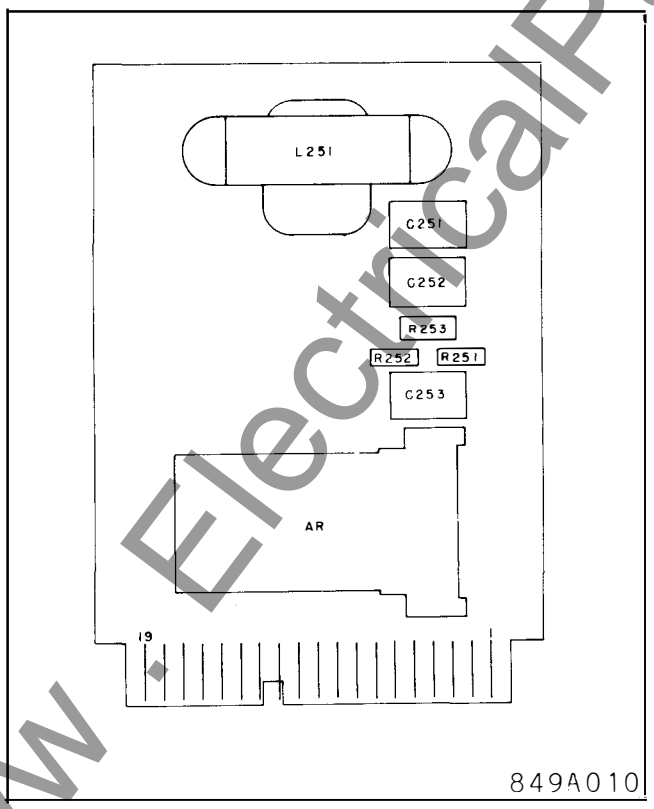

Fig. 13. Component Location on Relay Printed Circuit Board with an AR output for Type SKBU Relay.

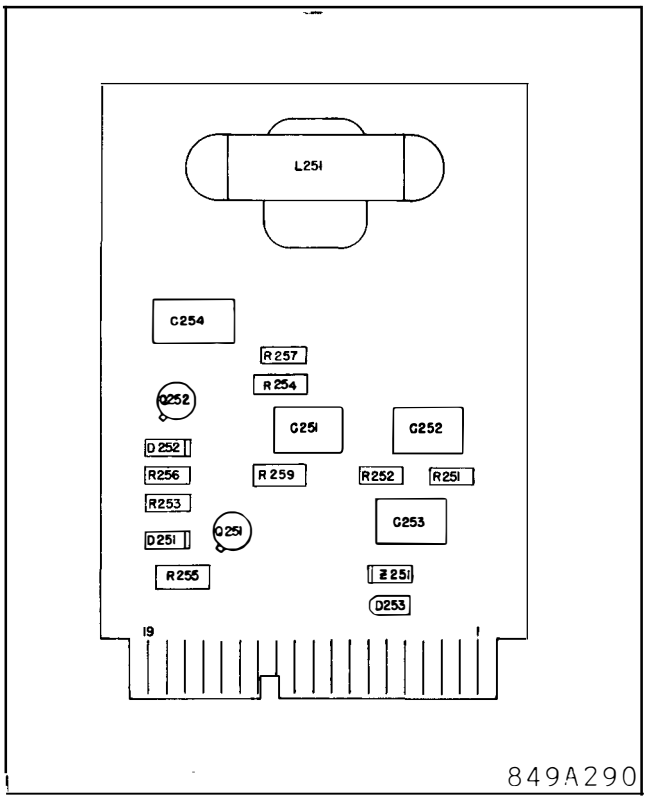

Fig. 14. Component Location on Relay Printed Circuit Board with a Voltage Output for Type SKBU Relay.

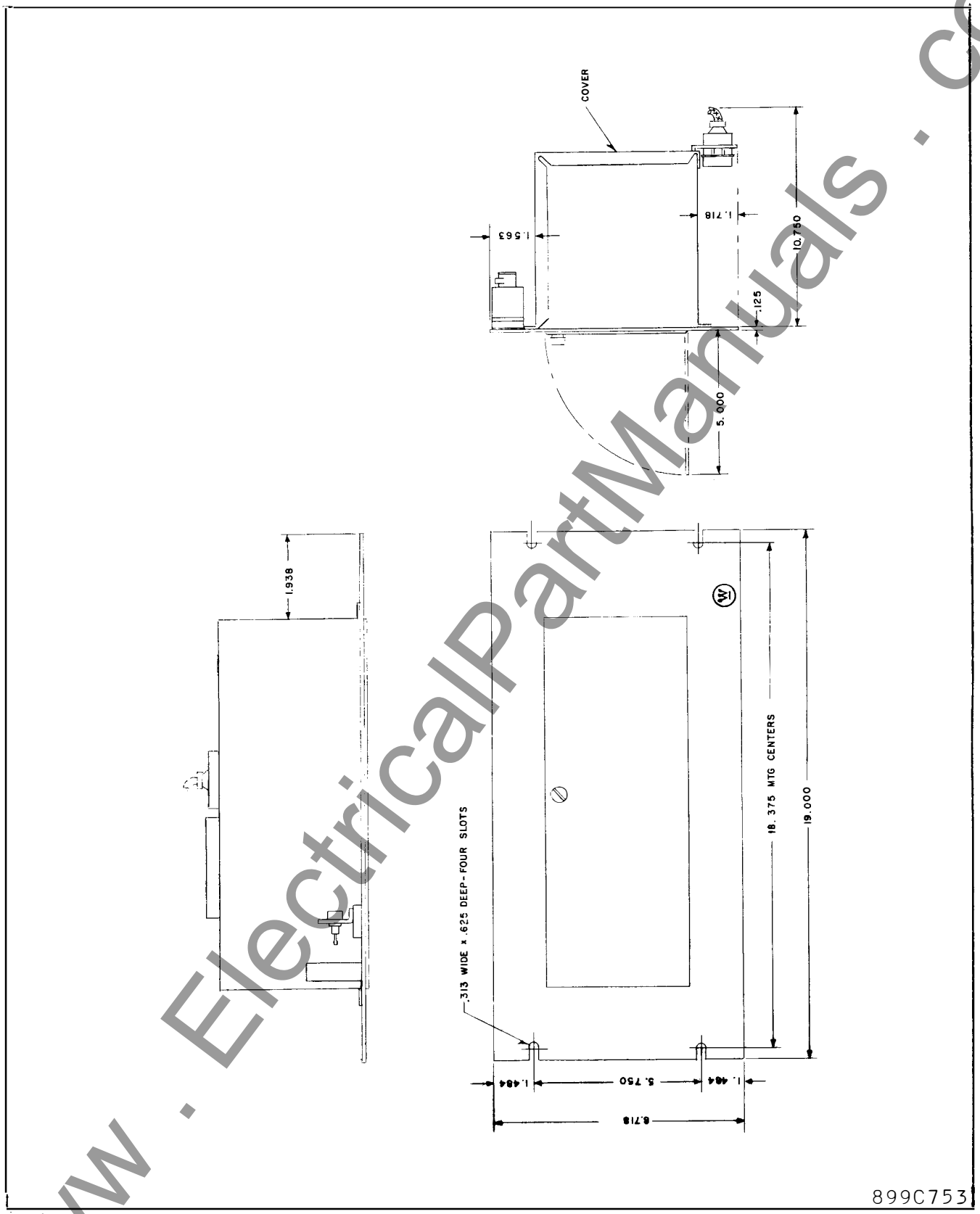

Fig. 15. Outline and Drilling Plan for Type SKBU Relay.

INSTALLATION • OPERATION • MAINTENANCE

INSTRUCTIONS

TYPE SKB AND SKB-1 RELAYS AND TEST EQUIPMENT FOR TYPE TC CARRIER

INSTRUCTIONS

CAUTION: Before putting relays into service, make sure that all moving parts operate freely, inspect the contacts to see that they are clean and close properly, and operate the relay to check the settings and electrical connections.

APPLICATION

The type SKB relay is a high-speed carrier relay with static fault detectors used in conjunction with power-line carrier equipment to provide complete phase and ground fault protection of a transmission line section. Simultaneous tripping of the relays at each line terminal is obtained in less than two cycles for all internal faults within the limits of the relay settings. The relay operates on line current only, and no source of a-c line potential is required. Consequently, the relays will not trip during a system swing or out-of-step conditions. The carrier equipment operates directly from the station battery.

The type SKB-1 relay is used in distance phase-comparison carrier relaying where separate distance-type fault detectors supplement the overcurrent fault detectors of the SKB-1 relay to give improved phase-fault sensitivity. Unless otherwise stated, the following sections of this instruction leaflet apply to both the types SKB and SKB-1 relays.

The SKB relay is available with indicating contactor switches with either a 1-ampere or a 0.2/2.0-ampere rating. The 0.2/2.0-ampere rating is recommended where a lockout relay is energized or where a high resistance auxiliary tripping relay is utilized. The SKB-1 relay has a low-current operation indicator, and the trip circuit energizes an external static tripping device.

PART I

TYPE SKB AND SKB-1 RELAYS

CONSTRUCTION

The relay consists of a combination positive, negative, and zero sequence current network, a saturating auxiliary transformer, Zener clipper, high-speed type AR tripping relay unit, indicating contactor switch plus the static fault-detector circuitry which is mounted on a printed-circuit board. These components are all mounted in an FT42 Flexitest relay case.

Sequence Network

The currents from the current-transformer secondaries are passed through a network consisting of a three-winding iron-core reactor and two resistors. The zero-sequence resistor, R_0, consists of three resistor tubes tapped to obtain settings for various ground fault conditions. The other resistor R_1 is a formed single wire mounted on the rear of the relay sub-base. The output of this network provides a voltage across the primary of the saturating transformer.

The lower tap block provides for adjustment of the relative amounts of the positive, negative, and zero sequence components of current in the network output. Thus, a single relay unit energized from the network can be used as a fault detector for all types of faults.

Saturating Auxiliary Transformer

The voltage from the network is fed into the tapped primary (upper tap plate) of a small saturating transformer. This transformer and a Zener clipper connected across its secondary are used to limit the voltage impressed on the static fault

All possible contingencies which may arise during installation, operation, or maintenance, and all details and variations of this equipment do not purport to be covered by these instructions. If further information is desired by purchaser regarding his particular installation, operation or maintenance of his equipment, the local Westinghouse Electric Corporation representative should be contacted.

SUPERSEDES I.L. 41-954D, dated Feb. 1973
* Denotes changes from superseded issue.

EFFECTIVE NOVEMBER 1977

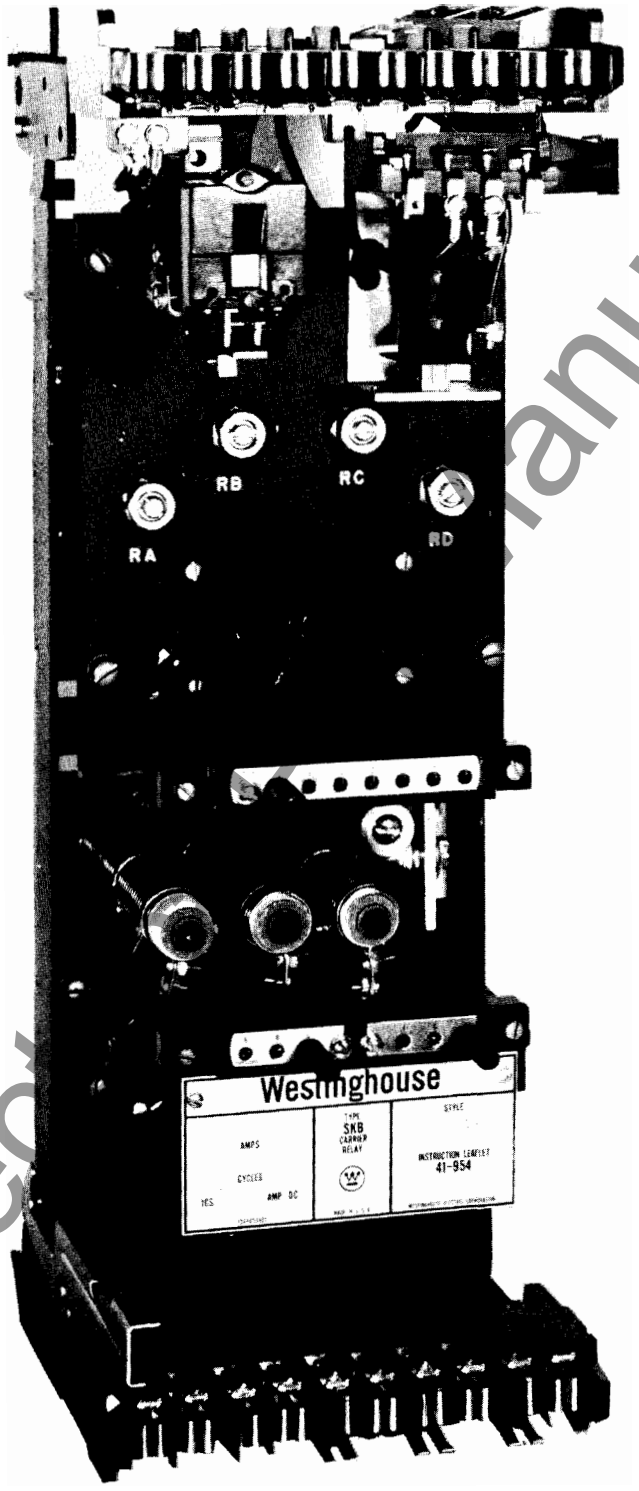

Fig. 1 Type SKB Relay – Front View

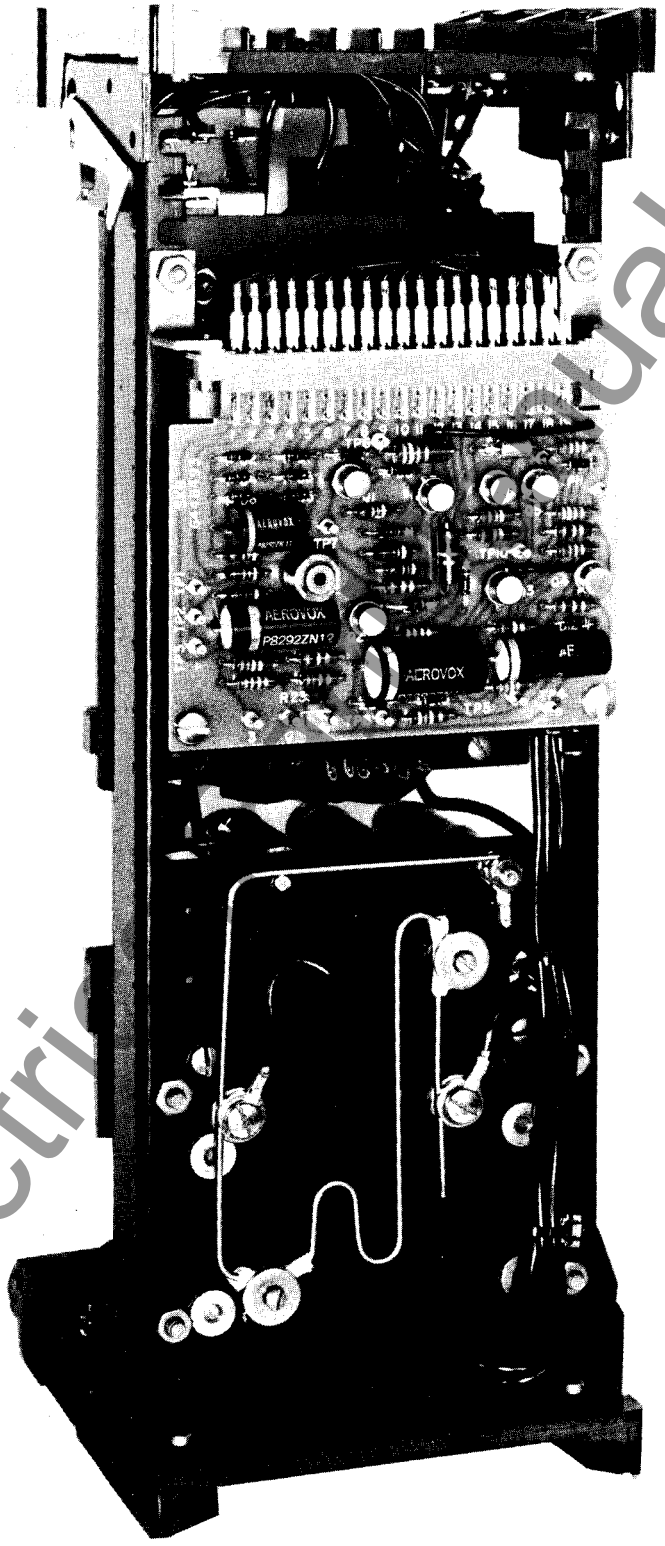

Fig. 2 Type SKB Relay – Rear View

detectors and the carrier control unit, thus providing a small range of voltage for a large variation of maximum to minimum fault currents. This provides high operating energy for light faults, and limits the operating energy for heavy faults to a reasonable value.

The upper tap plate changes the output of the saturating transformer, and is marked in amperes required to pick up the lower fault detector unit. For further discussion, see section entitled, SETTINGS.

Static Fault Detectors

The static circuitry for the two fault detectors FD1 and FD2 is mounted on a single printed circuit board on the rear of the relay chassis. Four controls for separately setting the pickup and dropout of FD1 and FD2 are mounted on a sub-panel in the chassis. The controls, with locking shafts, are adjustable from the front of the relay.

Tripping Relay

The AR tripping relay is a small high-speed attracted-armature type of unit. An insulated member, fastened to the free end of the armature, draws down four moving-contact springs to close the trip-circuit contacts when the relay coil is energized.

Indicating Contactor Switch Unit (ICS)

The d-c indicating contactor switch in the SKB relay is a small clapper type device. A magnetic armature, to which leaf-spring mounted contacts are attached, is attracted to the magnetic core upon energization of the switch. When the switch closes, the moving contacts bridge two stationary contacts, completing the trip circuit. Also during this operation, two fingers on the armature deflect a spring located on the front of the switch, which allows the the operation indicator target to drop. The target is reset from the outside of the case by a push rod located at the bottom of the cover.

The front spring, in addition to holding the target provides restraint for the armature and thus controls the pickup value of the switch. In the SKB-1 relay, the device has no contacts, and is used only as an operation indicator (OI).

OPERATION

The SKB or SKB-1 carrier relaying system compares the phase positions of the currents at the ends of a line-section over a carrier channel to determine whether an internal or external fault exists. The three-phase line currents energize a sequence network which gives a single-phase output voltage proportional to a combination of sequence components of the line current. During a fault, this single-phase voltage energizes a static control unit (TCU) which allows the transmission of carrier on alternate half-cycles of the power-frequency current. Carrier is transmitted from both line terminals in this manner, and is received at the opposite ends where it is compared with the phase position of the local sequence network output. If the local and remote half-cycle pulses are of the correct phase position for an internal fault, after a 4-millisecond delay during the half cycle in which carrier is not transmitted, tripping will be initiated through operation of the flip-flop and trip amplifier circuits in the TCU control unit. Current transformer connections to the sequence networks at the two terminals are such that carrier is transmitted on the same half cycles from both terminals during an internal fault, thus allowing tripping during the half cycles that carrier is not transmitted. However, if the fault is external to the protected line section, carrier is transmitted on alternate half cycles from opposite terminals. Thus each terminal blocks the opposite terminal during the half cycle when it is attempting to trip.

The four-millisecond delay previously mentioned is added to allow for differences in current transformer performance at opposite line terminals, relay co-ordination, and momentary interruptions in carrier caused by arcing over of protective gaps in the tuning equipment.

Since this relaying system operates only during a fault, the carrier channel is available at all other times for the transmission of other functions.

OPERATION
STATIC FAULT DETECTORS

The functional elements of the static fault detectors are shown in Fig. 3. The single-phase output of the sequence network (not shown) connects to the INPUT terminal shown at the left side of the drawing. This a-c voltage is applied to a phase-splitting network and polyphase rectifier. The resulting d-c voltage has relatively little ripple without much filtering which would slow down the fault detector operation. The d-c voltage is fed to two level detectors which determine the operating currents of FD1 and FD2. The output of FD1 level detector is amplified and provides a ''normally-closed'' FD1 static contact to start carrier.

The operation of FD2 is delayed about 5 milliseconds to insure coordination in setting up blocking for external faults where FD1 must operate to start carrier blocking a few milliseconds before FD2 energizes the comparison and flip-flop circuits. The output of FD2 fault detector circuit is equivalent to a ''normally-open'' contact.

The complete circuitry of the SKB relay is shown in Fig. 4. The sequence network, saturating transformer, phase-splitting network, and polyphase rectifier occupy the lower third of the diagram. The FD2 circuitry is in the middle portion, and the FD1 portion is in the upper part of the diagram. The type AR tripping relay is shown at the top. Fig. 5 is a simplified schematic of the SKB relay with the static fault detector circuitry omitted.

Figures 6 and 7 are the complete and simplified schematic diagrams, respectively, of the type SKB-1 relay. This relay differs from the SKB relay in the trip circuit wiring to terminals 1, 10, and 20, and in the connections from the saturating transformer tapped secondary to the input terminals 5 and 7 of the printed circuit board. The sequence network (R1, R0, and the mutual reactor) and the printed circuit board assembly for the static fault detectors for the SKB and SKB-1 relays are identical. Figure 8 shows the location of components on the printed circuit board for the static fault detectors for both the SKB and SKB-1 relays.

With reference to Fig. 4, the output voltage of the sequence network and saturating transformer is applied to a phase-splitting network (C1, R1, R2) and a polyphase rectifier (diodes D1 to D6). The d-c voltage so obtained requires a minimum of filtering (C2), and responds rapidly to a change in magnitude of the a-c output. This d-c voltage is applied to the FD1 and FD2 circuits which operate when the d-c input ''signal'' exceeds a predetermined value.

FD1 - Under normal line conditions (no fault), current flows from relay terminal 19 (pos. 45 v) through resistor R4 and Zener diode Z1 to negative, holding Q1 emitter at 6.8 volts positive. In transistor Q1, current flows from emitter to base, then through RA and R3 to negative, thus turning on Q1. The collector current of Q1 provides base drive to transistors Q2 and Q7, turning them on also. The voltage drop across Q7 is very low (less than 0.5 volt), thus providing the equivalent of a closed contact. When a fault occurs and the d-c input voltage to Q1 base (from the polyphase rectifier) exceeds the 6.8-volt drop across Zener diode Z1, transistor Q1 stops conducting. This removes the base current from Q2 and Q7, causing them to stop conducting, and providing the equivalent of an open contact at Q7 collector-emitter circuit.

When Q2 is cut off as just explained, its collector potential rises to about 20 volts. This further raises the potential of Q1 base through feedback resistors R6 and RB, thus holding Q1 in a non-conducting state. When the input voltage is sufficiently reduced to allow FD1 to ''reset,'' transistors Q1, Q2, and Q7 again conduct. Resistor RA is for setting the FD1 pickup current (calibration adjustment), and the setting of RB determines the 80 per cent dropout value.

FD-2 - Under normal conditions, transistor Q3 has no base ''signal'' and thus is turned off (not conducting). Thus Q3 collector is at a high enough positive potential to provide base drive for transistor Q4, driving it to full conduction. With Q4 fully conducting, there is no base drive to transistor Q5. With no Q5 collector current, the base of PNP-type transistor Q6 is supplied from the 45-volt source through the drop of diode D11. Thus the Q6 emitter is normally at a slightly lower potential than its base. This condition keeps transistor Q6 in a non-conducting state, equivalent to an open contact. Zener diode Z3 is to protect transistor Q6 from external surge voltages.

When a fault causes the d-c input voltage from the adjustable resistor RC to exceed the 6.8-volt rating of Zener diode Z2, a positive bias is applied to Q3 base, causing it to conduct. In turn, Q4 stops conducting, and capacitor C5 charges up, giving a few milliseconds' time delay before Q5 and Q6 are switched to full conduction, thus ''closing'' FD2. The feedback resistors R13 and RD provide a 90-percent FD2 dropout ratio with ''toggle'' action at the dropout point.

CHARACTERISTICS

The sequence network in the relays is arranged for several possible combinations of sequence components. For most applications, the output of the network will contain the positive, negative, and zero sequence components of the line current. In this case, the taps on the upper tap plate indicate the balanced three-phase amperes which will operate the carrier-start fault detector FD1. The second fault-detector unit FD2, which supervises operation of the AR tripping relay, is adjusted to pick up at a current 25 percent above tap value. The taps avail-

able are 3, 4, 5, 6, 7, 8, and 10, for the SKB relay, and 6, 8, 10, 12, 14, 16, and 20 for the SKB-1 relay. These taps are on the primary of the saturating transformer.

For phase-to-phase faults AB and CA, enough negative sequence current has been introduced to allow the fault detector FD1 to pick up at 86% of the tap setting. For BC faults, the fault detector will pick up at approximately 50% of the tap setting. This difference in pick-up current for different phase-to-phase faults is fundamental, and occurs because of the angles at which the positive and negative sequence components of current add together.

With the sequence network arranged for positive, negative, and zero sequence output, there are some applications where the maximum load current and minimum fault current are too close together to set the relay to pick up under minimum fault current, yet not operate under load. For these cases, a tap is available on both the SKB and SKB-1 relays which cuts the three-phase sensitivity in half, while the phase-to-phase setting is substantially unchanged. The relay then trips at 90% of tap value for AB and CA faults, and at twice tap value for three-phase faults. The setting for BC faults is 65 percent of tap value. In some cases, it may be desirable to eliminate response to positive-sequence current entirely, and operate the SKB relay on negative-plus-zero sequence current. A tap is available to operate in this manner. The fault detector FD1 picks up at about 95% of tap value for all phase-to-phase faults, but is unaffected by balanced load current or three-phase faults when using this tap.

For ground faults, separate taps are available for adjustment of the ground fault sensitivity to about 1/4 or 1/8 of the upper tap plate setting. See Table II. For example, if the upper tap plate of the SKB relay is set at tap 4, the fault detector (FD1) pick-up current for ground faults can be either 1 or ½ ampere. In special applications, it may be desirable to eliminate response to zero-sequence current. The relay is provided with a tap to allow such operation.

Trip Circuit

The main contacts of the SKB relay will safely close 30 amperes at 250 volts d-c and the seal-in contacts of the indicating contactor switch will safely carry this current long enough to trip a circuit breaker. The trip contacts of the SKB-1 relay have no seal-in device since they energize the low-current input of a static tripping relay.

Trip Circuit Constants - SKB Relay

Indicating Contactor Switch (ICS)
0.2-ampere tap, 6.5 ohms d-c resistance
2.0-ampere tap, 0.15 ohms d-c resistance
1.0-ampere tap, 0.1 ohms d-c resistance.

SETTINGS – SKB RELAY

The SKB relay has separate tap plates for adjustment of the phase and ground fault sensitivities and the sequence components included in the network output. The range of the available taps is sufficient to cover a wide range of application. The method of determining the correct taps for a given installation is discussed in the following paragraphs.

In all cases, the similar fault detectors on the relays at all terminals of a line section must be set to pick up at the same value of line current. This is necessary for correct blocking during faults external to the protected line section.

Positive-Sequence Current Tap and FD2 Tap

The upper tap plate has taps of 3, 4, 5, 6, 7, 8, and 10 for the SKB relay, or 6 to 20 for the SKB-1 relay. As mentioned before, these numbers represent the three-phase, fault detector FD1 pickup currents, when the relay is connected for positive, negative and zero sequence output. The fault detector FD2 operates to allow tripping at a current value 25 percent above the fault detector FD1 setting. This 25 percent difference is necessary to insure that the carrier-start fault detectors (FD1) at both ends of a 2-terminal transmission line section pick up to start carrier on an external fault before operating energy is applied through FD2.

For a 3-terminal line, FD2 settings must be readjusted for pickup at 250 percent of FD1 setting. This is necessary to allow proper blocking when approximately equal currents flow in two terminals, and their sum flows out the third line terminal. The relay is normally shipped calibrated for 2-terminal line operation.

When the SKB is to be used on a 3-terminal line, FD2 must be recalibrated as explained in the previous paragraph, and the FD2 temperature-compensating circuit must also be changed to accomodate the new Rc (FD2 pickup) setting. This is accomplished by changing the jumper near the lower left corner of the printed circuit board (see Fig. 8) from C-2 to C-3, as shown.

The taps on the upper and lower tap plates should be selected to assure operation on minimum internal line-to-line faults, and yet not operate on normal load current, particularly if the carrier channel is to be used for auxiliary functions. The drop-out current of the FD-1 fault detector is 80 percent of the pick up current, and this factor must also be considered in selecting the positive-sequence current tap and sequence component combination. The margin between load current and fault detector pick up should be sufficient to allow the fault detector to drop out after an external fault, when load current continues to flow.

Sequence Combination Taps

The two halves of the lower tap plate are for connecting the sequence network to provide any of the combinations described in the previous section. The left half of the tap plate changes the tap on the third winding of the mutual reactor and thus changes the relative amounts of positive and negative sequence sensitivity. Operation of the relay with the various taps is given in the table below.

TABLE I

COMB.	SEQUENCE COMPONENTS IN NETWORK OUTPUT	TAPS ON LOWER TAP BLOCK		FAULT DETECTOR FD1 PICK-UP △	
		LEFT HALF	RIGHT HALF	3 ϕ FAULT	ϕ - ϕ FAULT
1	Positive, Negative, Zero	C	G or H *	Tap Value	86% Tap Value (53% on BC Fault)
2	Positive, Negative, Zero	B +	G or H	2 x Tap Value	90% Tap Value (65% on BC Fault)
3	Negative, Zero	A +	G or H	——	95% Tap Value

* Taps F, G, and H are zero-sequence taps for adjusting ground fault sensitivity. See section on zero-sequence current tap.

△ Fault detector FD2 is set to pick up at 125% of FD1 for a two-terminal line, or 250% for a three-terminal line.

\+ When taps A and 3, or B and 3 are used, FD1 and FD2 will pickup 10 or 15 percent higher than the above values because of the variation in self-impedance of the sequence network and the saturating transformer.

Zero-Sequence Current Tap

The right half of the lower tap plate is for adjusting the ground fault response of the relay. Taps G and H give the approximate ground fault sensitivities as listed in Table II. Tap F is used in applications where increased sensitivity to ground faults is not required. When this tap is used, the voltage output of the network caused by zero-sequence current is eliminated.

NOTE: Because of inherent characteristics of the sequence network, there will be small variations (from the values listed in Tables I and II) in the pickup current for various phase or ground fault combinations. However, these variations will be the same from one relay to another.

TABLE II

COMB.	LOWER LEFT TAP	GROUND FAULT PICKUP	
		TAP G	TAP H
1	C	25%	12%
2	B	20%	10%
3	A	20%	10%

Examples of SKB Relay Settings

Case I

Assume a two-terminal line with current transformers rated 400/5 at both terminals. Also assume that full load current is 300 amperes, and that on minimum internal phase-to-phase faults 2000 amperes is fed in from one end and 600 amperes from the other end. Further assume that on minimum internal ground faults, 400 amperes is fed in from one end, and 100 amperes from the other end.

Positive-Sequence Current Tap

Secondary Values:

$$\text{Load Current} = 300 \times \frac{5}{400} = 3.75 \text{ amperes} \quad (1)$$

Minimum Phase-to-Phase Fault Currents:

$$600 \times \frac{5}{400} = 7.5 \text{ amperes} \quad (2)$$

Fault detector FD1 setting (three-phase) must be at least:

$$\frac{3.75}{0.80} = 4.7 \text{ amperes (0.80 is dropout ratio of FD-1 fault detector)} \quad (3)$$

so that the fault detector will reset on load current.

In order to complete the trip circuit on a 7.5 ampere phase-to-phase fault, the fault detector FD1 setting(three-phase) must be not more than:

$$7.5 \times \frac{1}{0.866} \times \frac{1}{1.25} = 6.98 \text{ amperes} \quad (4)$$

$$1.25 = \frac{\text{FD2 pickup}}{\text{FD1 pickup}}$$

Sequence Combination Tap

From a comparison of (3) and (4) above, it is evident that the fault detector can be set to trip under minimum phase fault condition yet not operate under maximum load. In this case, tap C on the lower left tap block would be used (see Table 1, Comb. 1) as there is sufficient difference between maximum load and minimum fault to use the full three-phase sensitivity. Current tap 6 would be used in preference to tap 5 to allow for occurrence of higher load current.

Zero Sequence Tap

Secondary Value:

$$100 \times \frac{5}{400} = 1.25 \text{ amperes minimum ground fault current.}$$

With the upper tap 6 and sequence tap C in use, the fault detector FD1 pickup currents for ground faults are as follows:

Lower right tap G–1/4 x 6 = 1.5 amp.
Minimum trip = 1.25 x 1.5 = 1.88 amp.
Lower right tap H–1/8 x 6 = 0.75 amp.
Minimum trip = 1.25 x 0.75 = 0.94 amp.

From the above, tap H would be used to trip the minimum ground fault of 1.25 amperes.

Case II

Assume the same fault currents as in Case I, but a maximum load current of 550 amperes. In this example, with the same sequence combination as in Case I, the fault detectors cannot be set to trip on the minimum internal three-phase fault, yet remain inoperative on load current. Compare equations (5) and (6). However, by connecting the network per Combination 2 on Table I, the relay can be set to trip on minimum phase-to-phase fault, although it will have only half the sensitivity to three-phase faults. This will allow operation at maximum load without picking up the fault detector, and provide high speed relaying of all except light three-phase faults.

In order to complete the trip circuit on a 7.5 ampere phase-to-phase fault, the fault detector tap must now be not more than:

$$7.5 \times \frac{1}{1.25} \times \frac{1}{0.9} = 6.6 \quad (5)$$

To be sure the fault detector FD1 will reset after a fault, the minimum tap setting is determined as follows:

$$\text{Load Current} = 550 \times \frac{5}{400} = 6.9 \text{ amps} \quad (6)$$

$$\frac{6.9}{0.80} = 8.6 \quad (7)$$

Since the fault detector pickup current for three-phase faults is twice tap value, half the above value (Eq. 7) should be used in determining the minimum three-phase tap.

$$\frac{8.6}{2} = 4.3 \quad (8)$$

From a comparison of (5) and (8) above, tap 5 or 6 could be used. (Continuous load current rating of relay is 10 amperes.)

With the three-phase tap 5 in use, the fault detector pickup current for ground faults will be as follows:

Tap G–1/5 x 5 = 1.0 a.
Minimum trip = 1.0 x 1.25 a. = 1.25 amp.

Tap H–1/10 x 5 = 0.5 a.
Minimum trip = 1.25 x 0.5 a. = 0.63 amp.

Therefore, tap H would be used to trip the minimum ground fault of 1.25 ampere with a margin of safety.

Indicating Contactor Switch (ICS) – SKB Relay

No setting is required for relays with a 1.0 ampere unit. For relays with a 0.2/2.0 ampere unit, connect the lead located in front of the tap block to the desired setting by means of the connecting screw. When the relay energizes a 125 or 250-volt d-c type WL relay switch, or equivalent, use the 0.2 ampere tap; for 48-volt d-c applications set the unit in tap 2 and use a type WL relay with a S# 304C209-G01 coil, or equivalent.

SETTINGS – SKB-1 RELAY

The SKB-1 relay tap settings are made from a consideration of just maximum load current and the resetting of FD1 fault detector. The SKB-1 current taps are 6, 8, 10, 12, 14, 16, and 20. On taps 6 and C, FD1 will operate at 6 amperes, 3-phase, and reset at 80% of pickup, or 4.8 amperes. This will be adequate in most cases where maximum load current is in the order of 3 to 4 amperes, secondary values. If maximum load current is 5 amperes or slightly higher, tap 8 should be used, which will give a dropout current for FD1 or 6.4 amperes.

For most SKB-1 relay applications, where static phase-distance relays are used as phase fault detectors, taps 6-C-H are recommended. This will give a minimum trip sensitivity for phase-to-ground faults of 6 x 1/8 x 1.25 or 0.94 ampere. Taps A or B are not recommended for SKB-1 relay application.

✪ INSTALLATION

The relays should be mounted on switchboard panels or their equivalent in a location free from dirt, moisture, excessive vibration and heat. Mount the relay vertically by means of the rear mounting stud or studs for the type FT projection case or by means of the four mounting holes on the flange for the semi-flush type FT case. Either the stud or the mounting screws may be utilized for grounding the relay. External toothed washers are provided for use in the locations shown on the outline and drilling plan to facilitate making a good electrical connection between the relay case, its mounting screws or studs, and the relay panel. Ground wires are affixed to the mounting screws or studs as required for poorly grounded or insulating panels. Other electrical connections may be made directly to the terminals by means of screws for steel panel mounting or to the terminal stud furnished with the relay for thick panel mounting. The terminal stud may be easily removed or inserted by locking two nuts on the stud and then turning the proper nut with a wrench.

For detail information on the FT case refer to I.L. 41-076.

ADJUSTMENT AND MAINTENANCE

CAUTION: When changing taps under load, the spare tap screw should be inserted in the new tap before removing the other tap screw.

Acceptance Tests

Since the static fault detector circuits obtain their d-c supply voltage from the associated type TC carrier set, the fault detector calibration can must easily be checked after the SKB relay and TC-TCU carrier assembly have been installed and interconnected.

NOTE: The relay current tap numbers and the FD1 and FD2 pickup and dropout current values in the Acceptance Tests and Calibration sections apply to the SKB relay. For the equivalent tap number and current value for the SKB-1 relay, double the figures given for the SKB relay.

The carrier trip circuit should be open for the following check: Set the SKB relay on taps 5, C, and H. Connect a 60-cycle test current circuit between phases A and B of the relay (terminals 5 and 7.). Connect a high-resistance d-c voltmeter between relay terminal (or test switch) 15 (pos.) and 18 (neg.). This will read approximately 20 volts when FD1 operates. Gradually increase the current. At 4.33 amperes, FD1 should operate, starting the transmission of half-cycle pulses of carrier, and the d-c voltmeter will read 20 volts.

Continue to increase the test current. At 5.41 amperes, FD2 should operate. If the R101 controls in the type TCU control unit have been set, the AR tripping unit in the SKB relay will operate. The operation of FD1 and FD2 can also be noted by observing the change in d-c voltage at the printed circuit board terminals 14 (FD1) and 15 (FD2) relative to TP4 (negative). See Table I for typical values for these voltages under standby and operating conditions.

Now back off the test current to check the dropout values. Fault detector FD2 should drop out at 90 per cent of pickup, or 4.85 amperes. The FD1 dropout is 80 per cent of pickup, or 3.46 amperes.

The fault detectors have been properly calibrated at the factory and normally will require no further adjustment. If it is found desirable to touch up the calibration, this can be done by loosening the locking nut and changing the adjustment of the appropriate control as listed at the beginning of this section. Turning RA or RC in a clockwise direction will increase the FD1 or FD2 pickup. Similarly, turning RB or RD in a clockwise direction will increase the dropout current.

The pickup and dropout calibration settings of FD1 and FD2 are made with the four controls on the SKB or SKB-1 relay subpanel, as follows:

Relay Unit	Pickup	Dropout
FD1	RA	RB
FD2	RC	RD

These four controls have slotted shafts (for screwdriver adjustment) and locking nuts which are tightened after proper adjustment.

Typical test point voltage values listed in Table I will be useful when checking the apparatus. The readings will remain fairly constant over an indefinite period unless a failure occurs. Voltages should be measured with a vacuum-tube voltmeter. To facilitate taking these voltages, a test cable is available. See Fig. 9. To use this cable, remove the SKB or SKB-1 chassis from its case. Remove the printed circuit board from the back of the relay, and insert the board end of the test cable in its place. Now plug the removed board into the receptacle at the other end of the cable. Replace the relay chassis in its case on the switchboard and close the test switches. The relay can now be energized and operated to obtain the readings in Table I. The test cable can also be used, if desired, with the printed circuit boards of the type TCU Control Unit. However, do not use these test cables in the TC transmitter where r.f. voltages are involved.

TABLE I

Note: All d-c voltages are positive with respect to negative d-c (TP4). All voltages are read with a vtvm, and in general will be within ± 10% of the values listed.

TEST POINT	$I_{SKB} = 0$	$I_{SKB} = 2 \times$ FD2 p.u. ϕ
TP5	45.0 vdc	45.0 vdc
TP6	6.5	6.8
TP7	6.5	< 0.5
TP8	14.0	< 0.5
TP9	< 0.5	14.0
TP10	45.0	< 0.5
TP11	45	45
*Term. 14	< 0.5	20.0
*Term. 15	—	44.5
*Term. 19	< 0.5	20.0
A-C TEST POINT VOLTAGES		
TP2 to TP1	18.0 vac approx.	
TP2 to TP3	17.5 vac approx.	

* On Printed Circuit Board

ϕ - Test current of twice FD2 pickup for the taps used.

< 0.5 - means less than 0.5

After the SKB or SKB-1 and associated relays and the carrier equipment have been installed and adjusted, the system can be checked following the procedure in Part II of this I.L. under the heading "OVERALL TEST OF COMPLETE INSTALLATION."

Routine Maintenance

All contacts should be periodically cleaned. A contact burnisher S# 182A836H01 is recommended. The use of abrasive material is not recommended because of the danger of embedding small particles in the face of the soft silver and thus impairing the contact.

The proper adjustments to insure correct operation of this relay have been made at the factory and should not be disturbed after receipt by the customer. If the adjustments have been changed, the relay taken apart for repairs, or if it is desired to check the adjustments at regular maintenance periods, the instructions below should be followed.

The performance of the phase comparison carrier relaying can be checked periodically as explained in Part III of this I.L. under the heading "TYPE SKB or SKB-1 TEST FACILITIES APPLICATION."

Calibration

Normally, there are no adjustments to be made in the sequence network. The taps on the three tubular R_0 resistors are brazed in place and cannot get out of adjustment. The two taps on the formed R1 resistor are factory settings, and should not require readjustment. However, if there is reason to suspect that the tap position has changed, the following procedure can be used to check the R1 tap settings for either the SKB or SKB-1 relay:

Remove the current tap screw (upper tap plate), and insert the tap screws in taps C and H on the lower tap plate.

Pass a single-phase current of ten amperes (SKB or SKB-1), rated frequency, through the reactor coils in series from phase B to phase C (relay terminals 7 and 9). Accurately measure the a-c voltage from phase A terminal to the upper tap plate. This voltage should be between 3.8 and 4.0 volts a-c. Now pass 10 amperes fromphase A to phase B with the lower tap screw C removed. Adjust the R1 tap further from the R1 mounting screw to give a voltage drop across R1 equal to exactly one-third of the reactor drop. This voltage can be measured directly across the terminals of the resistor R1 from the mounting screw to the last tap on R1.

Note the above reading, and adjust the intermediate tap on R1 to give exactly 1/3 of the voltage obtained above for all of R1. Measure the voltage from the R1 mounting screw to the intermediate tap.

If replacement of the printed circuit board or major components necessitates a complete recalibration, proceed as follows:

1. Set relay taps on 5-C-H. (10-C-H for SKB-1)
2. Use a phase A-B test current. (double the following current values for SKB-1 relay).
3. Set RA and RC to full clockwise position.
4. Set RB and RD to mid-scale.
5. Pass 4.33 amperes through the relay (phase A to B).
6. Check the a-c voltage from TP2 to TP1 and from TP2 to TP3 with a vtvm. Adjust the small pot. R2 on the printed circuit board until these two voltages are equal.
7. Now slowly turn RA counterclockwise, with 4.33 amperes flowing, until FD1 operates.
8. Reduce the phase A-B current to check FD1 dropout. Adjust RB to get 80 percent dropout (3.46 Amperes).
9. Recheck FD1 pickup and dropout, and touch up RA and RB in that order for the correct calibration. Tighten the locknuts.
10. Similarly recalibrate FD2 using controls RC (pickup) and RD (dropout), repeating steps 7, 8, and 9 except for FD2 pickup of 5.41 amp. and dropout of 4.85 amp. Do not readjust R2.
11. For 3-terminal lines, change the printed circuit board link from C2 to C3, then calibrate FD2 for 10.82 amp. pickup and 9.7 amp. dropout.

Tripping Relay (AR)

The type AR tripping relay unit has been properly adjusted at the factory to insure correct operation, and should not be disturbed after receipt by the customer. If, however, the adjustments are disturbed in error, or it becomes necessary to replace some part in the field, use the following adjustment procedure. This procedure should not be used until it is apparent that the relay is not in proper working order, and then only if suitable tools are available for checking the adjustments.

1. Adjust the set screw at the rear of the top of the frame to obtain a 0.009-inch gap at the rear end of the armature air gap.
2. Adjust each contact spring to obtain 4 grams pressure at the very end of the spring. This pressure is measured when the spring moves away from the edge of the slot in the insulated crosspiece.
3. Adjust each stationary contact screw to obtain a contact gap of 0.020 inch. This will give 15-30 grams contact pressure.

This completes the adjustment procedure for the AR relay unit. The resistance of the AR relay coil is 100 ohms.

Indicating Contactor Switch (ICS in SKB Relay)

Close the main relay contacts and pass suf-

ficient direct current through the trip circuit to close the contacts of the ICS. This value of current should not be greater than the particular ICS tap setting being used. The indicator target should drop freely.

Operation Indicator (OI in SKB-1 Relay)

Apply 80 percent of rated voltage across relay terminals or test switches 1 and 10. When the AR relay is operated, the orange target should drop. There are no seal-in contacts on the operation indicator, which is a voltage-operated device.

Replacement of Printed-Circuit Board Components

If a defective resistor, capacitor, or diode is found, cut it out of the circuit by first clipping off its leads on the component side of the printed circuit board. Then turn the board over, melt the solder holding the remaining lead to the printed pad, and remove the lead with tweezers.

NOTE: For such work, a 60-watt iron with a small, clean, well-tinned tip is recommended. Use a 60-40 (tin-lead) rosin-core solder. Do not hold the iron against the printed-circuit board any longer than necessary to remove and replace the component. If the terminal hole in the board closes up with solder, use the iron to melt it, then open up the hole with a fine awl or similar tool.

Where transistors are mounted on small plastic pads, the leads cannot be clipped off. In such a case, melt the solder on one connection at a time, while gently tilting back that section of the transistor. Because of the small flexible leads, the transistor will gradually separate from the board.

Wherever possible, use a heat-sink (such as an

ELECTRICAL PARTS LIST

Symbol	Description	Style
C1	0.5 mfd. 200V ± 10%	187A624H11
C2	0.25 mfd, 200V ± 20%	187A624H02
C4	1.0 mfd, 200V ± 20%	187A624H04
C5 ✪	1.5 mfd, 200V ± 10% ✪	187A508H09
CT	0.1 mfd, 400V.D.C.	1544920
D1-D7	IN459A Diode	184A855H08
D8-D9 D10-D12	IN457A Diode	184A855H07
Q1	2N652A	184A638H16
Q2-Q3	2N697	184A638H18
Q4	2N697	184A638H18
Q5	2N699	184A638H19
Q6	2N4356	849A441H02
Q7	2N697	184A638H18
R1	2.7K 1/2W ± 5%	629A530H42
R2	2.5K ± 20% 1/4W Pot	629A430H03
R3 ✪	20K 1/2W ± 5%	629A530H63
R4	3.9K 1W ± 5%	187A643H41
R6	33K 1/2W ± 10%	187A641H63
R7	10K 1/2W ± 5%	629A530H56
R8	10K 1/2W ± 10%	187A641H51
R9	10K 1/2W ± 5%	629A530H56
R10	0.22 MEG, 1/2W ± 5%	184A763H83
R11	10K 1/2W ± 10%	187A641H51
R12	15K 1/2W ± 10%	187A641H55
R13	33K 1/2W ± 10%	187A641H71
R14	0.1 MEG, 1/2W ± 10%	187A641H75
R15	10K 1/2W ± 10%	187A641H51

Symbol	Description	Style
R16	68K 1/2W ± 10%	187A641H71
R17	39K 1/2W ± 10%	187A641H65
R18	10K 1/2W ± 10%	187A641H51
R19	6.8K 1/2W ± 10%	187A641H47
R20 ✪	10K ✪ ✪	629A531H56
R21	18K 1/2W ± 5%	184A763H57
R22	15K 1/2W ± 10%	187A641H55
R23	Type 1DO51 Thermistor, 20K at 25°C.	185A211H05
R24	470K 1/2W ± 5%	184A763H91
R25	10K 1W ± 5%	187A643H51
R26	1K 1/2W ± 5%	629A530H32
R27 ✪	10K 1/2W ± 5%	629A530H56
RA	30K pot.	185A067H15
RB	200K pot.	185A067H14
RC	40K pot.	185A067H16
RD	200K pot.	185A067H14
RT	50 ohms, 2" tube	1340388
RL	9.1K, ½ watt, ±5%-SKB-1 only	
Z1	IN957B (6.8v, 0.4w) Zener Diode	186A797H06
Z2	IN957B (6.8v, 0.4w) Zener Diode	186A797H06
Z3	IN1789 (56v, 1.0w) Zener Diode	584C434H08
Z4	IN3686B (20v, 0.75w) Zener Diode	185A212H06
ZT	IN1832C (62v, 10w) Zener Clipper	184A617H06

alligator clip) on any transistor or diode being soldered. As an alternate, use a long-nosed pliers to hold the lead (being soldered) between the device and the point of soldering.

Test Equipment

1. A-C ammeter and load box (for fault-detector calibration).
2. Vacuum-tube voltmeter for a-c and d-c measurements.
3. Cathode-ray oscilloscope (to check carrier keying and 60-cycle square-wave voltages in TCU Control Unit).
4. Test Cable

RENEWAL PARTS

Repair work can be done most satisfactorily at the factory. However, interchangeable parts can be furnished to the customers who are equipped for doing repair work. When ordering parts, always give the complete nameplate data. For components mounted on the printed circuit board, give the circuit symbol, electrical value, and style number.

ENERGY REQUIREMENTS SKB OR SKB-1 RELAY

Burdens measured at a balanced three-phase current of five amperes:

Relay Taps	Phase A		Phase B		Phase C	
	VA	Angle	VA	Angle	VA	Angle
A-F- 3	2.47	5°	0.6	0°	2.5	20°
A-H-10	3.25	0°	0.8	100°	1.28	55°
B-F-33	2.3	0°	0.63	0°	2.45	55°
B-H-10	4.95	0°	2.35	90°	0.3	60°
C-F- 3	2.32	0°	0.78	0°	2.36	50°
C-H-10	6.35	342°	3.83	80°	1.98	185°

Burdens measured at a single-phase-to-neutral current of five amperes:

Relay Taps	Phase A		Phase B		Phase C	
	VA	Angle	VA	Angle	VA	Angle
A-F- 3	2.47	0°	2.1	10°	1.97	20°
A-H-10	7.3	60°	12.5	53°	6.7	26°
B-F- 3	2.45	0°	2.09	15°	2.07	10°
B-H-10	16.8	55°	22.0	50°	12.3	38°
C-F- 3	2.49	0°	1.99	15°	2.11	15°
C-H-10	31.2	41°	36.0	38°	23.6	35°

The angles above are the degrees by which the current lags its respective voltage.

PART II – TYPE TCU CONTROL UNIT

The construction, operation, and adjustment of the type TCU Control Unit used with the SKE or SKB-1 relays are covered in separate instructions identified as I.L. 41-944.5 plus supplements, when required. The Control Unit is a part of the Type TC carrier assembly.

OVERALL TEST OF COMPLETE INSTALLATION

After the complete equipment has been installed and adjusted, the following tests can be made which will provide an overall check on the relay and carrier equipment. The phase rotation of the three-phase currents can be checked by measuring the a-c voltage across relay terminals 2 and 3 with a high resistance a-c voltmeter of at least 1000 ohms per volt. The reading obtained should be approximately 0.9 volts per ampere of balanced three-phase load current (secondary value) with relay taps 4, C and H, or taps 8-C-H for the SKB-1 relay.

The following test requires that a balanced three-phase load current of at least 1.0 ampere (secondary) be flowing through the line-section protected by the SKB relays. At both terminals of the protected line section, remove the SKB or SKB-1 relay cover and open the trip circuit by pulling the test switch blade with the red handle. Put the tap screw on the upper tap plate in the 4 tap, and on the lower ones in the C and H taps. Be sure to insert the spare tap screw before removing the connected one. Now open test switches 4 and 5 on the relay at one end of the line section (station A) and insert a current test plug or strip of insulating material into the test jack on switch 5 to open the circuit through

that switch. The above operation shorts the phase A to neutral circuit ahead of the sequence filter and disconnects the phase A lead from the filter. This causes the phase B and C currents to return to the current tramsformers through the zero-sequence resistor in the filter, thus simulating a reversed phase A-to-ground fault fed from one end of the line only, As a result, both the fault detectors and tripping relay at Station A should operate. Completion of the trip circuit can be checked by connecting a small lamp (not over 10 watts) across the terminals of test switch 10. (SKB only.)

Now perform the above operations at the opposite end of the line section (station B) and momentarily open and reclose test switch 11 or momentarily depress the Test Reset push-button, if more convenient. This simulates a phase-to-ground fault external to the protected line section. The fault detectors, but not the operating unit should operate. Test switch 11 operation is required to make sure that "flip-flop" stage in the control unit is in reset position. Now open and reclose switch 11 at station A in order to reset "flip-flop" stage from previous "trip" condition. The operating unit at station A should stay open now. Restore test switches 4 and 5 at Station A to normal (closed). The line conditions now represent a phase-to-ground fault fed from Station B. only. The fault detectors at A should reset and the operating unit at B should pick up. Restore test switches 4 and 5 at Station B to normal, and all elements of the relay at Station B should reset.

The above tests have checked phase rotation, the polarity of the sequence filter output, the interconnections between the relay and the carrier set and the Phase A current connections to the relay at both stations. Phase B and C should be similarly checked by opening test switches 6 and 7 for phase B, and switches 8 and 9 for phase C. The same procedure described for Phase A is then followed.

If all the tests have been completed with satisfactory results, the test switches at both line terminals should be closed (close the trip-circuit test switch last) and the relay cover replaced. The equipment is now ready to protect the line-section to which it is connected.

PART III – TYPE SKB OR SKB-1 TEST FACILITIES APPLICATION

The test facilities provide a simple manually operated test procedure that will check the combined relay and carrier equipment. The test can be performed without the aid of instruments. The results give assurance that all equipment is in normal operating condition without resorting to more elaborate test procedures.

CONSTRUCTION

Test Switch

The type W-2 test switch is a four-position, multi-stage switch. The contact arrangement is shown in Fig. 10, and the outline and drilling plan in Fig. 11. The "on" contacts are used to complete the SKB trip circuit and the alarm circuit. These contacts are indicated in Fig. 10 by contacts C5-D5 and A1-B1. In the "Off" position, the SKB trip circuit is opened through contact C5-D5, but the alarm circuit remains closed through contact A1Z-B1Z. Two test positions to the left of the "Off" position. are provided. When the switch is moved to either of these positions, the relay trip and alarm circuits are interrupted and a red alarm light is turned on by switch contacts A6-B6 and A7-B7. Moving the switch to the "Test 1" position will connect the output of the auxiliary test transformer directly to the SKB terminals number 8 and 9. Moving the switch to the "Test 2" position will connect the test transformer with a reversed polarity to the SKB relay.

For the SKB-1 relay, refer to the overall diagram which applies to the particular order for actual connections.

Auxiliary Test Transformer

The auxiliary test transformer is designed to operate from a 120-volt, 60-cycle power source. Four secondary taps numbered 1, 2, 3, and 4 are provided to vary the magnitude of the phase-C-to-ground test current approximately as follows:

TRANS TAP	RELAY TAP	
	G	H
1	3 amp.	2 amp.
2	5 amp.	4 amp.
3	7.5 amp.	5.5 amp.
4	9.5 amp.	7 amp.

The outline and drilling plan of the transformer is shown in Fig. 12.

Indicating Lamps

The red and blue indicating lamps are standard rectangular Minalites. Outline and drilling dimensions are given in Fig. 11.

ADJUSTMENT

Choose a transformer tap that will provide approximately two times the phase-to-ground current setting of the FD-2 fault detector as previously determined.

OPERATION

A multi-contact switch is provided at each line terminal which serves the dual functions of a carrier on-off switch and a test switch. This switch is arranged to apply a single-phase current to the SKB or SKB-1 relay to simulate internal and through fault conditions. Relay operation is noted by observing a blue indicating lamp connected in the SKB relay trip circuit. During the test the SKB trip circuit to the line breaker is opened and a red warning light is energized through auxiliary contacts on the test switch.

Use of the auxiliary test equipment is to be limited to provide a simplified test after the initial installation tests have been performed as described in Part II of this instruction leaflet.

The test apparatus is to be connected as shown in Fig. 10 with the auxiliary test transformers energized from 120-volt, 60-cycle power sources, at each line terminal, that are in phase with each other. The following operation procedure assumes that the same polarity is used in connecting the test transformer at each line terminal.

1. Turn the carrier test switch at both line terminals to OFF.

2. Turn the carrier test switch to TEST 1 at station A. The "A" relay should operate to transmit half cycle impulses of carrier, and trip. Tripping will be indicated by the blue light.

3. Turn the SKB test switch at Station B to TEST 1. This will simulate an internal fault fed from both line terminals. The relay at Station B will trip, and the relay at Station A will remain tripped. Tripping will be indicated by the blue lights at each line terminal. Carrier will be transmitted in half cycle impulses simultaneously from each end of the line.

4. Reset the SKB test switch at Station A. The relay at Station A will reset and turn off the blue light. The relay at Station B will hold its trip contact closed, lighting the blue light.

5. Turn the SKB test switch at Station A to TEST 2. Depress Test Reset pushbutton momentarily to reset Flip-Flop stage that may have operated during switching the test switch to position 2. Operate Test Reset pushbutton at Station B to reset Flip-Flop stage from previous tripped position. Both blue lights should be off at this point, which represents an external fault.

6. Reset the test switches at both line terminals to OFF before returning to ON for normal service. Push in handle to turn in ON position.

This completes the test procedure.

Component Style Numbers

Test Transformer	S# 1338284
Type W-2 Test Switch	S# 505A742G01 for 1/8" panel mounting.
Type W-2 Test Switch	S# 505A742G02 for 1-½" panel mounting.

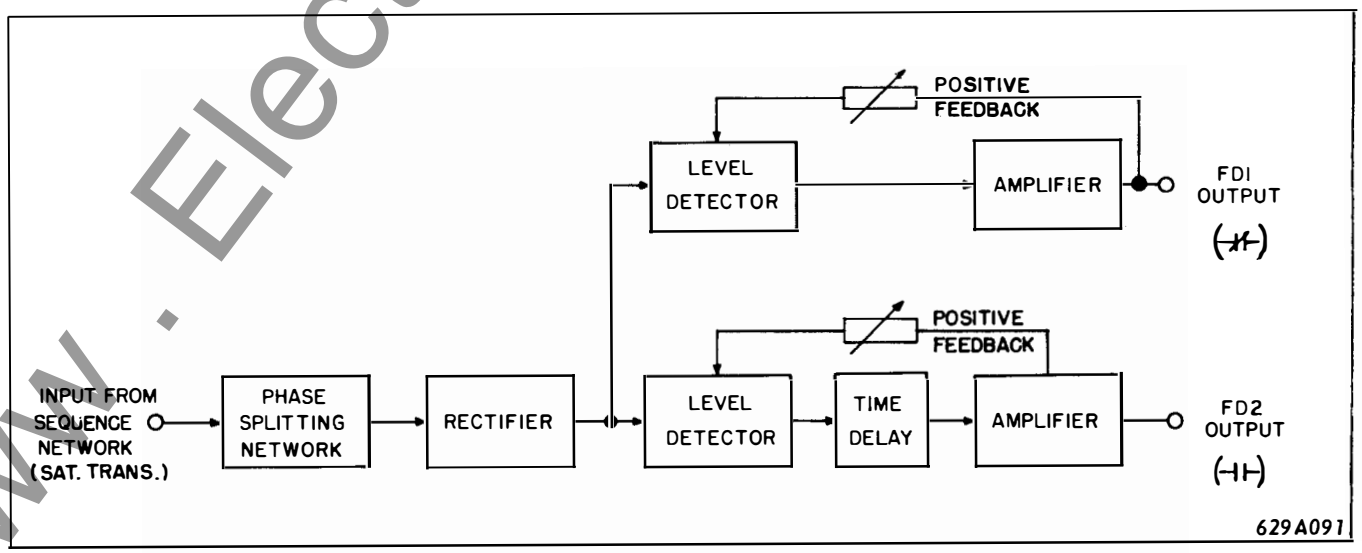

Fig. 3 Static Fault Detector Block Diagram

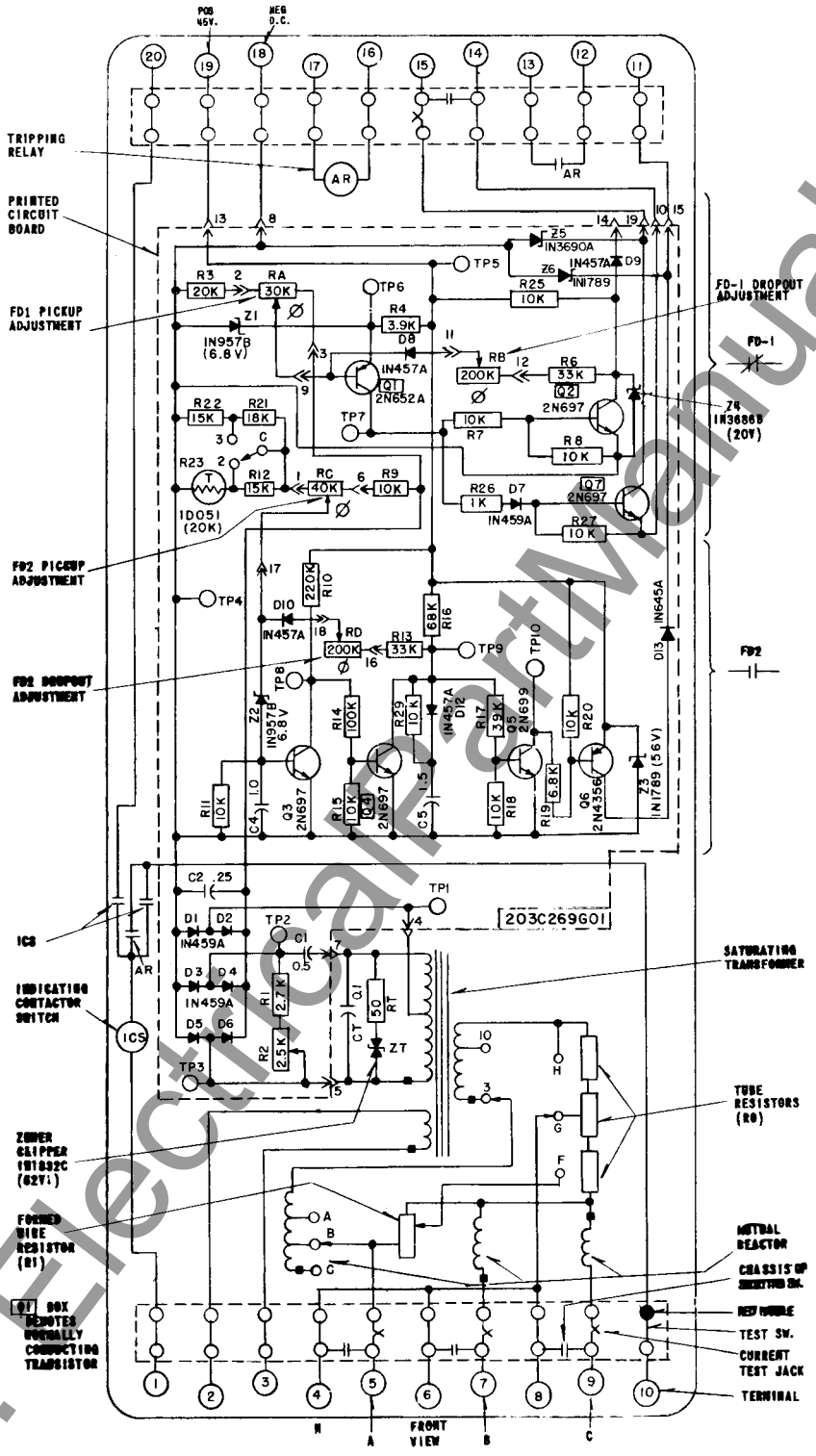

Fig. 4 Complete Internal Schematic of SKB Relay

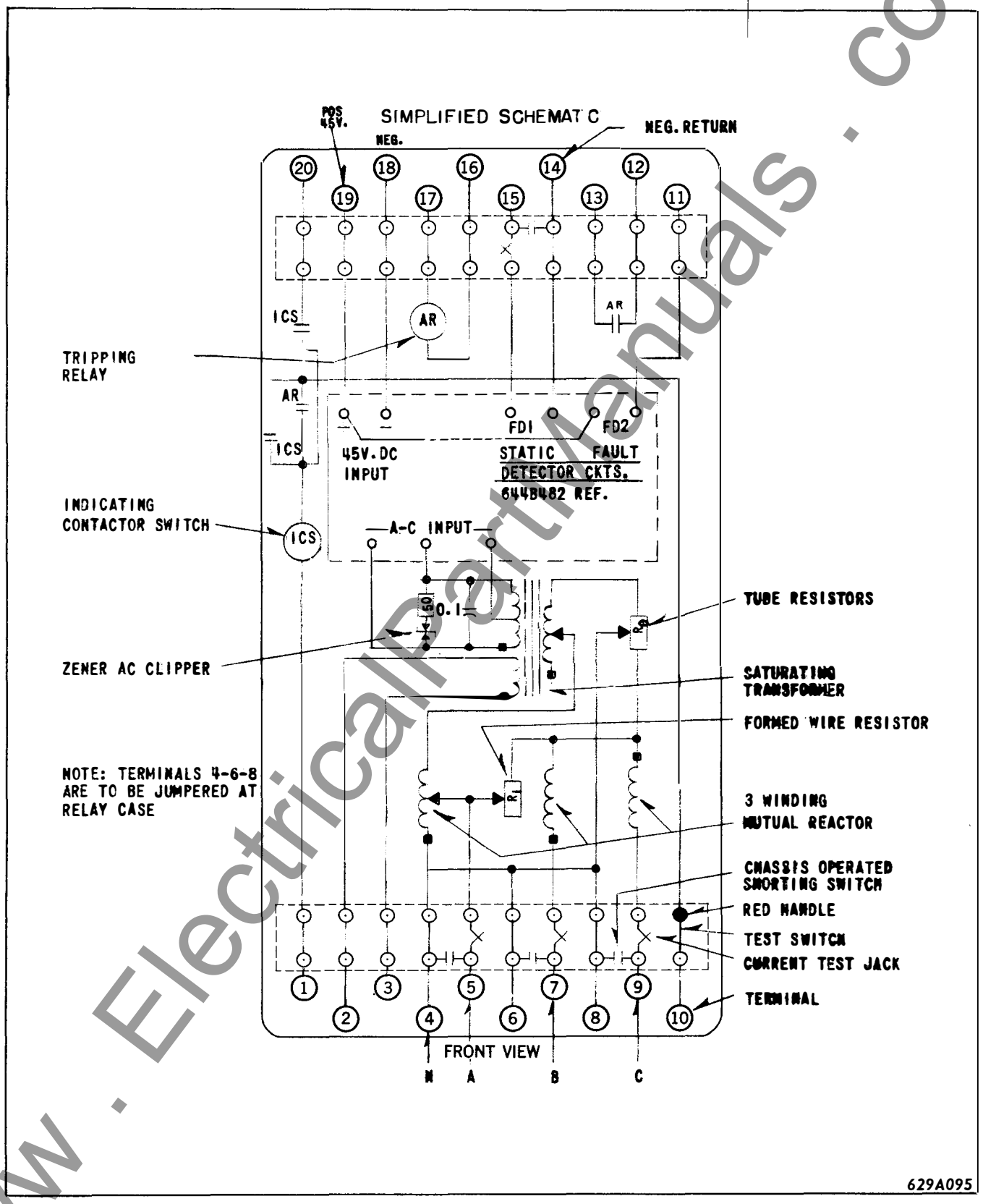

Fig. 5 Simplified Schematic — Type SKB Relay

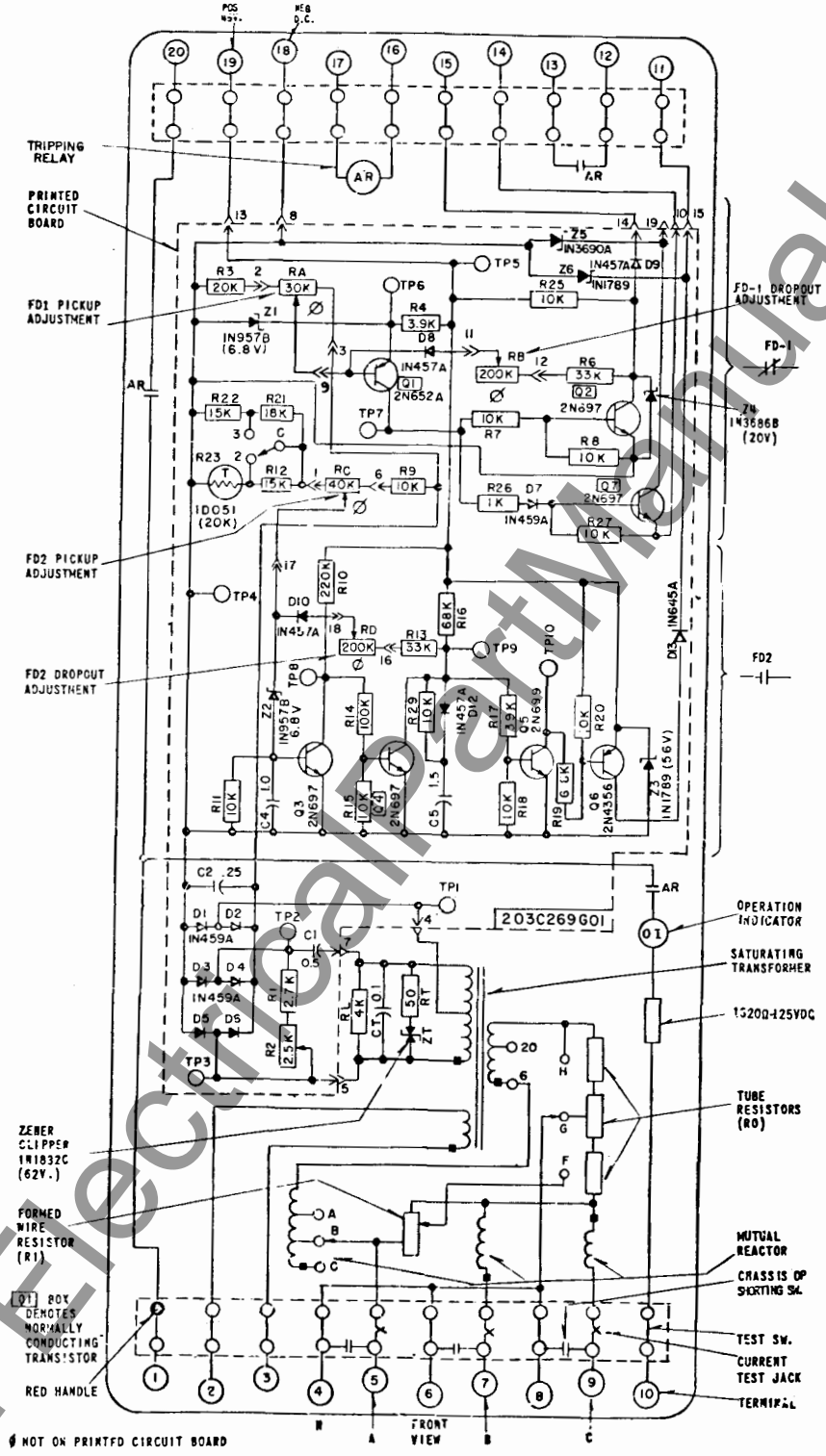

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Fig. 6 Complete Internal Schematic of SKB-1 Relay

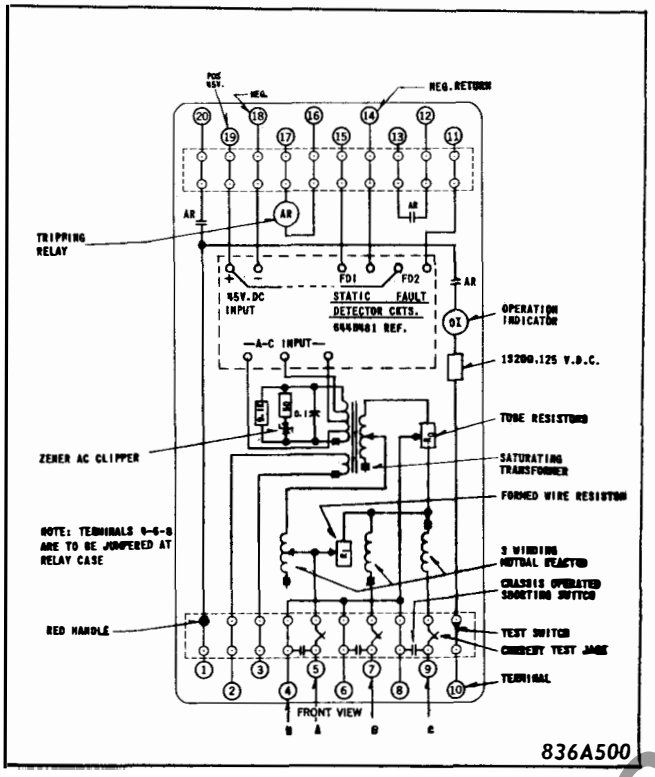


Fig. 7 Simplified Schematic – Type SKB-1 Relay

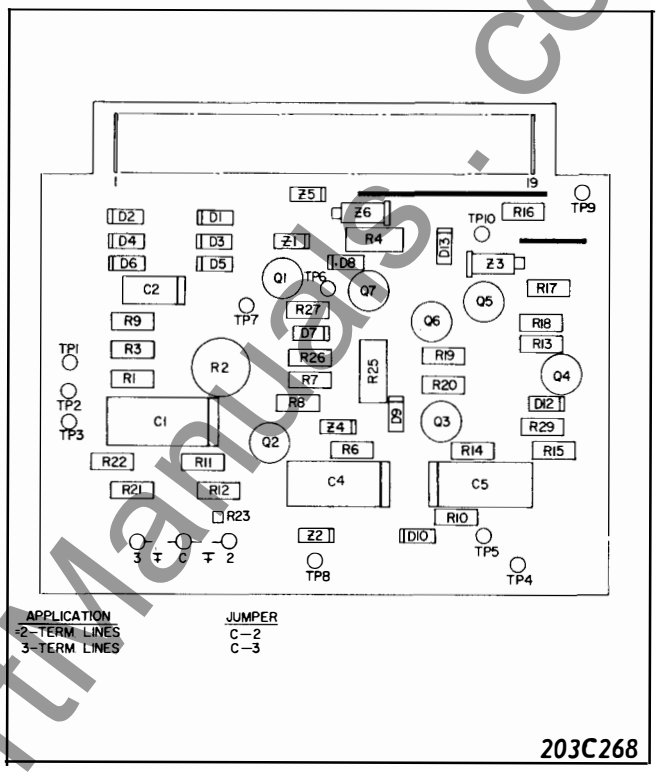


Fig. 8 Printed Circuit Board Component Location, SKB or SKB-1 Relay

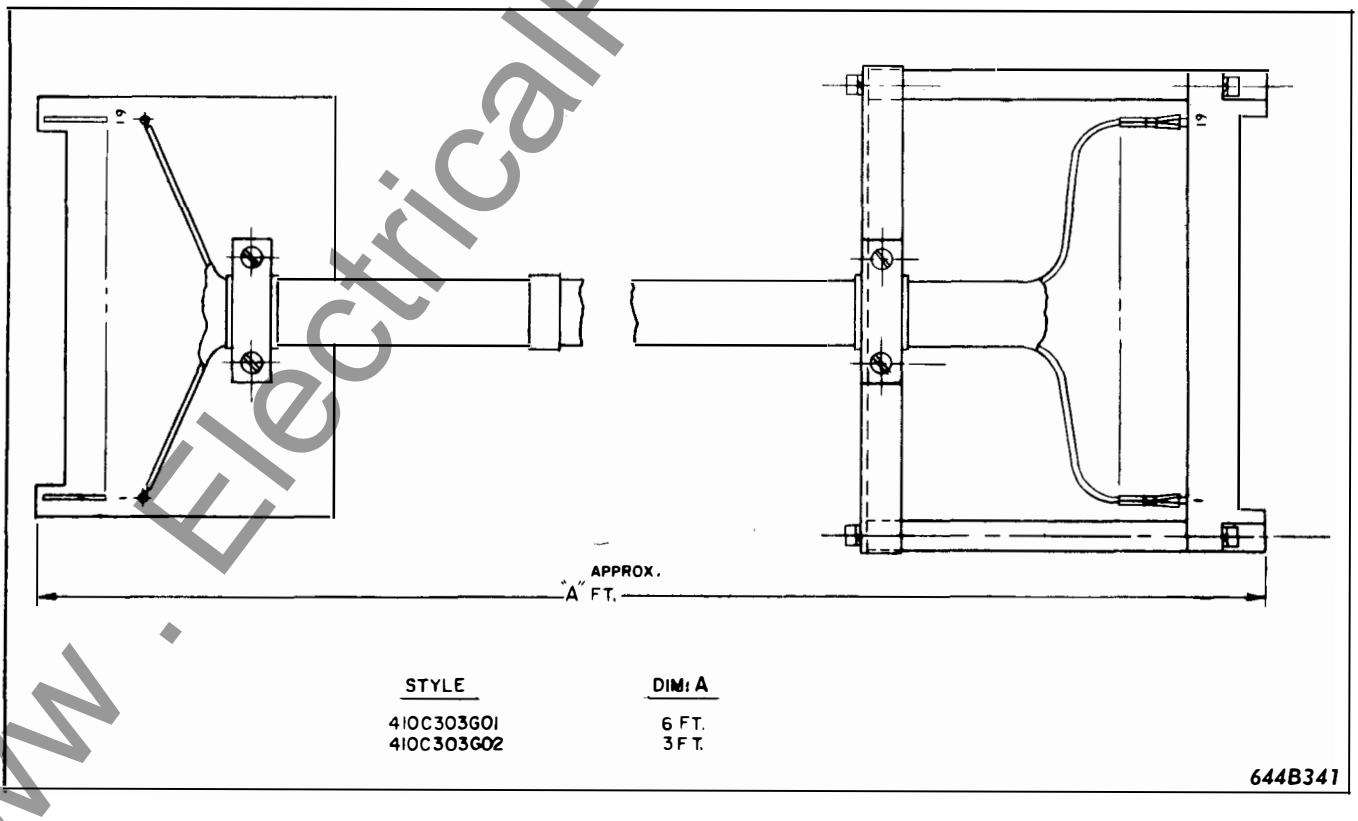


Fig. 9 Test Cable Assembly

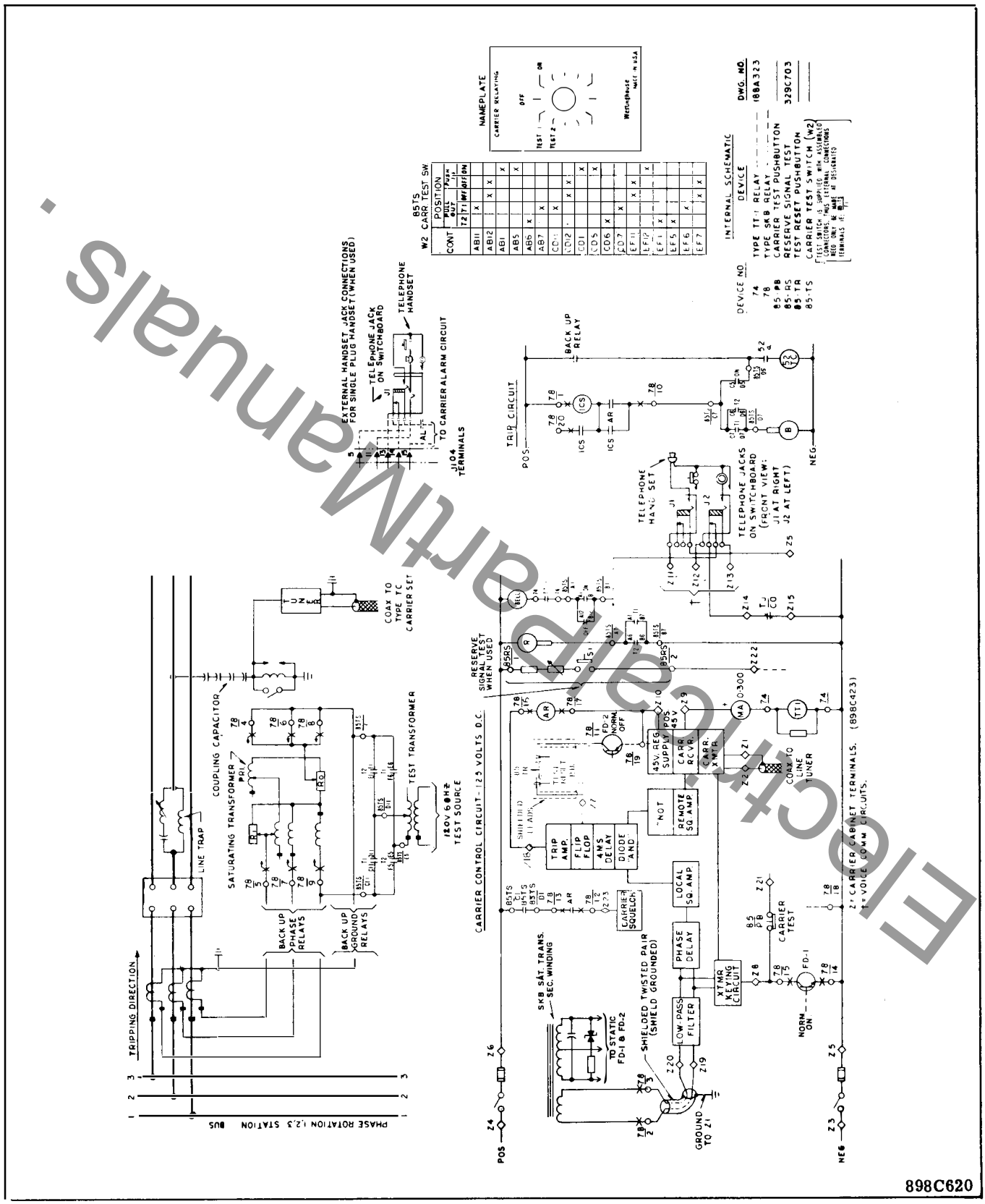


Fig. 10 *External Schematic of the SKB Relay and Test Facilities, with TT-1 Alarm Relay*

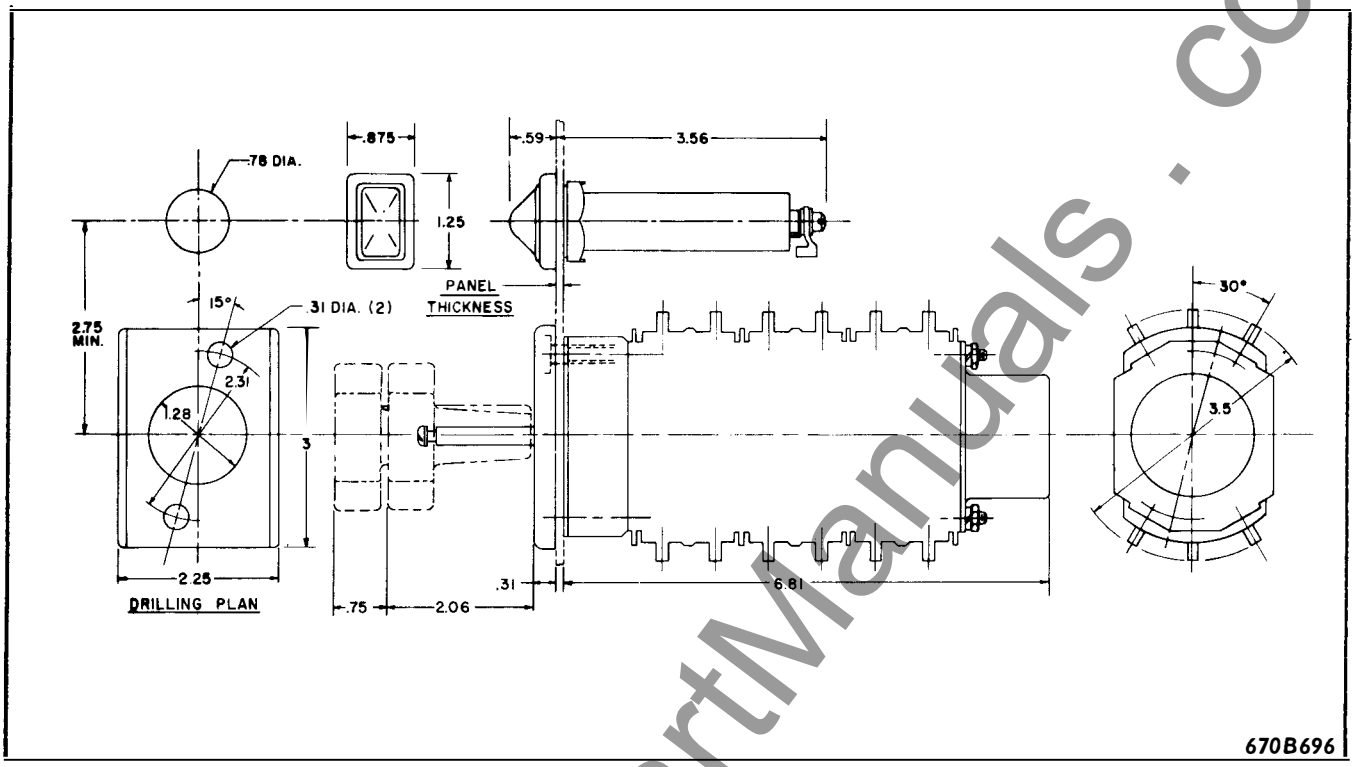


Fig. 11 Outline and Drilling Plan of the Type W-2 Test Switch and Indicating Lamps Used for SKB or SKB-1 Testing

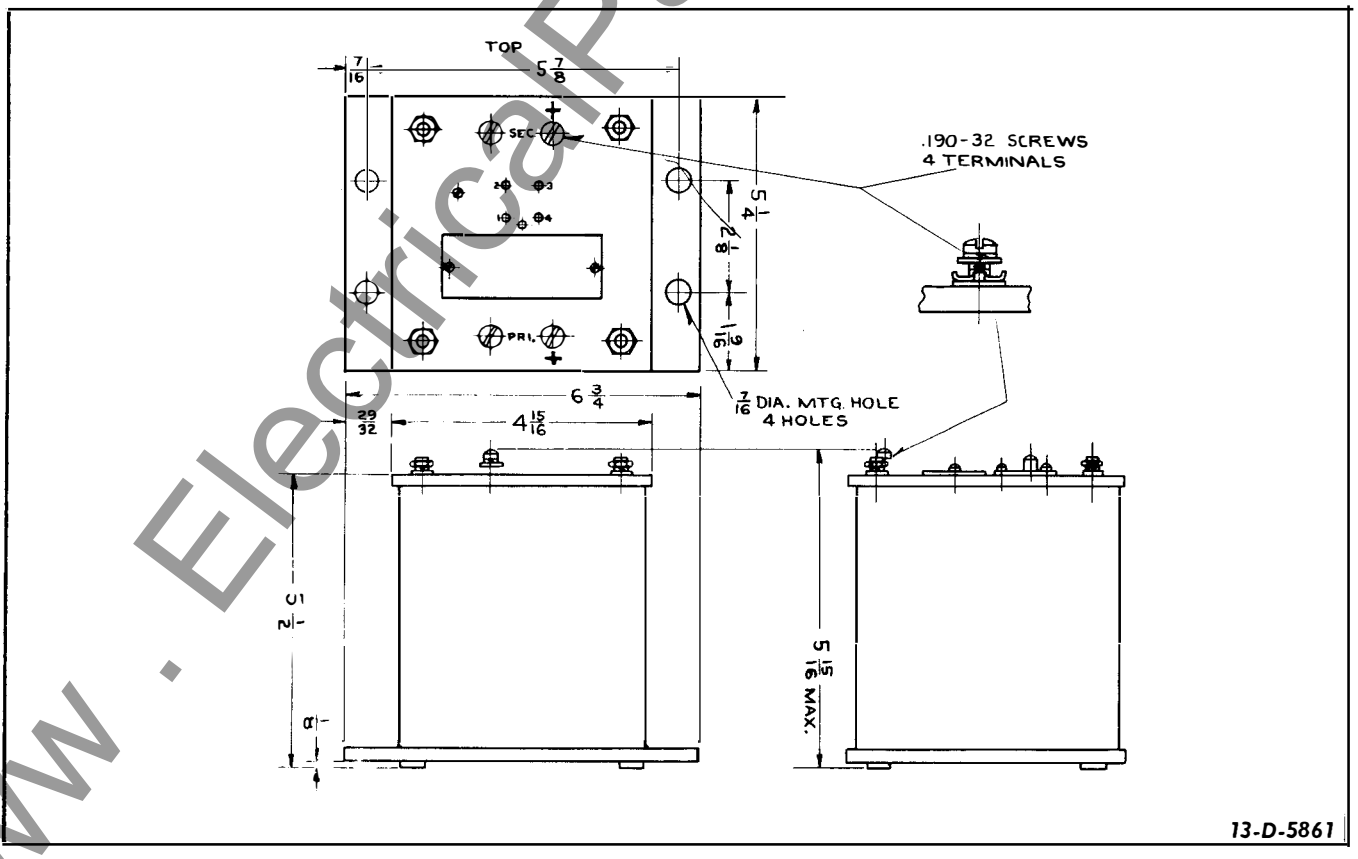
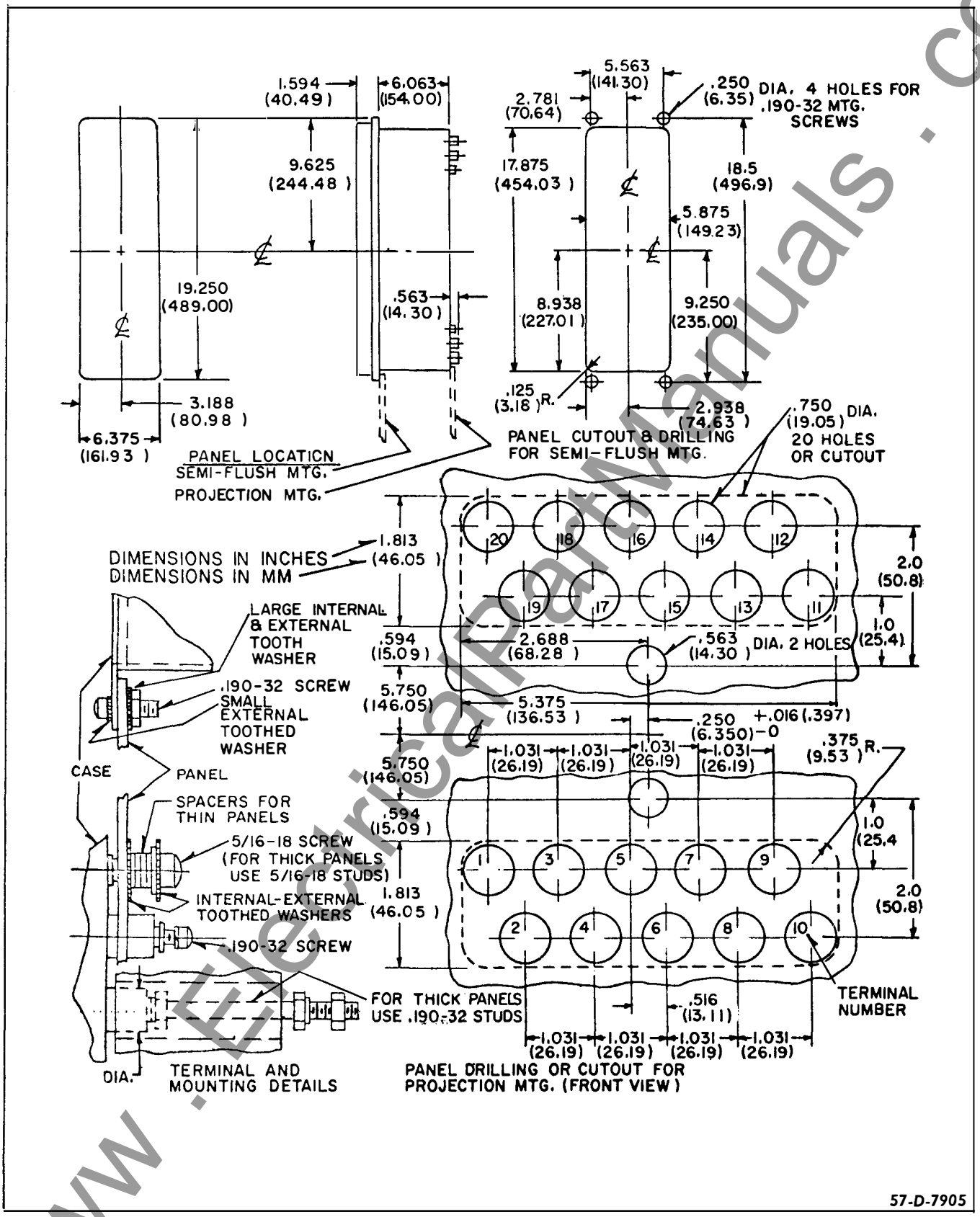
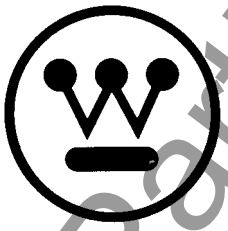


Fig. 12 Outline and Drilling Plan of the SKB Test Transformer



✪ *Fig. 13 Outline and Drilling Plan of the SKB or SKB-1 Relay in the FT-42 Case*



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