INSTALLATION • OPERATION • MAINTENANCE

INSTRUCTIONS

TYPE SRCU-2 MULTI-SHOT RECLOSING RELAY

CAUTION: It is recommended that the user of this equipment become acquainted with the information in this instruction leaflet before energizing the equipment. Failure to observe this precaution may result in damage to the equipment.
Printed circuit modules should not be removed or inserted while the relay is energized unless specific instructions elsewhere in this instruction leaflet state that such action is permissible. Failure to observe this precaution can result in an undesired output, and can cause component damage.

APPLICATION

The SRCU-2 static relay is intended for 3 shot reclosing applications where synchronism check, HLDB (hot-line-dead bus) and HBDL (hot bus-dead line) control is required. "Hot" and "dead" levels are independent of one-another and are adjustable from 3 to 120 volts.

The relay provides the following additional functions:

1. Intermediate lockout – delays the final reclosure until bus and line are hot and synchronism exists.
2. Supervisory close – allows external close control to be supervised by synchronism check, HLDB and HBDL. This control is designed for anti-pump operation.
3. Inhibit – all reclosing is restrained if the inhibit input is present. This input can be energized from such sources as a transfer trip system, indicating remote breaker failure, for example.
4. Indication – lights show the history of the reclosing relay action since last reset, including High Speed Reclose, Synchronism Check Reclose, HLDB or HBDL Reclose.
5. Initiated high speed reclosure – controlled by high speed trip from protective relays. An adjustable delay of 0-1 second is provided.
6. Reclose block input – predominates over reclose initiate input.
7. Independent timing control for each of the two time delayed reclosures.
8. Trip Output – responsive to dead line-dead bus, delayed 5 seconds.
9. Option for setting different times for HLDB and HBDL reclosures using the timers normally committed to second and third shot reclosures.
10. Selectable 1 to 3 shots to lockout.
11. Lockout relay.
12. Lockout on dc application.
13. 3 to 60 second adjustable reset time with calibrated dial.
14. Requires only a single 52b contact for breaker status indication.

CONSTRUCTION

The SRCU-2 relay is mounted on a 19 inch wide panel, 5¼ inches high (3 rack units) with edge slots for mounting on a standard relay rack or panel. For the outline and drilling plan, refer to Figure 28.

The photographs in Figures 1 and 2 show the front and rear view of the SRCU-2 relay with the front and rear door respectively open.

A hinged and removable door on the front of the chassis covers the printed circuit modules. Indicating lights are mounted on the left side of the front panel. A toggle switch is mounted above them to allow a check on the integrity of the lamps and to reset the seal-in indicators. A sealing post, located in the front top center of the relay, may be used to lock and seal the relay when in service.

The rear panel consists of a hinged door which may be opened to gain access to the relay harness wiring, power supply transistor and inductor, the close relay, the lockout relay, and the line and bus potential transformers. In addition, a 32 terminal connector for all SRCU-2 voltage inputs and outputs, and a terminal strip for the close relay current contacts are mounted at the rear right hand side of the chassis.

All of the circuitry suitable for mounting on printed circuit boards is contained in an enclosure behind the front door. The printed circuit modules slide into position in slotted guides at the top and bottom of the enclosure and engage a terminal block at the rear of the compartment. Each module and terminal block are keyed so that they cannot be accidentally inserted into the wrong slot location. The handle mounted on the front end of the module is used for identification, removal, and insertion of module, and acts as a bumper with the front door to prevent the module terminals from becoming disconnected from the terminal block. The modules may be removed for replacement purposes or for use in conjunction with a printed circuit board extender (style number 3494A90G01) which permits access to the module test points and terminals for making measurements while the relay is energized.

Location and title of the modules are shown on the relay component location drawing, Figure 5.

Printed Circuit Modules

Following is a description of all the printed circuit modules used in the SRCU-2 relay. Refer to the functional relay logic shown in Figure 3. The internal schematics associated with the printed modules contain a detailed logic diagram to simplify understanding of the circuitry, and a complete list and description of the components for renewal parts.

For those users not generally acquainted with logic circuit notation or with device symbols of those components used in the SRCU-2 drawings, it is recommended that a copy of Westinghouse instruction leaflet I.L. 41-000.1 entitled "Symbols for Solid state Protective Relaying" be consulted.

A. Power Supply Module ("POWER" - Position E)

Schematic diagram Figure 7

Component location Figure 6.

The power supply printed circuit module, in conjunction with the few parts mounted in the rear of chassis due to size or heat dissipation, provides the two regulated dc supply voltages required by the SRCU-2. The supply is of the switching regulator design giving high efficiency and relative insensitivity to input voltage. This allows the supply to operate over an input range of 42 to 140 volts dc without any power supply alterations, which is a distinctive feature.

The supply has two outputs; +20 volts for most relay functions, and +15 volts for the integrated circuits and most logic functions. The +20 volt supply is powered directly from the switching regulator, while the +15 volt supply is derived from the +20 volt supply and incorporates "snap turn-on" circuitry to insure the proper initial turn on states of the integrated circuits.

Built into both outputs to provide greater security are non-destructive overvoltage and overcurrent protection circuits, which, if activated (i.e. supply output is shorted) immediately shut the supply down.

A more detailed look at the power supply circuitry is as follows:

The switching regulator of the supply consists basically of chassis mounted switching transistor Q1 (c), and inductor L1 (c), and module components capacitor C6, diode D2, and voltage comparator and driver transistors Q5, Q6, Q2, Q1, Q3 and Q4.

Transistor Q1 (c) is used as a switch, either off or full on. When the voltage comparator and driver transistors switch Q1 (c) on, diode D2 is reversed biased and input voltage is applied

to inductor L1 (c). The current through L1 (c) increases at the rate

$$\frac{di}{dt} = \frac{(V \text{ input} - V \text{ capacitor C6})}{L1\ (c)}$$

When the voltage on capacitor C6 charges to 20 volts the voltage comparator, consisting of Q5 and Q6 in a differential amplifier arrangement, turns transistor Q1 (c) off through driver transistors Q2, Q1, Q3 and Q4.

At this point with Q1 (c) off, the current continues to flow through inductor L1 (c) and the voltage across L1 (c) reverses polarity, forward biasing diode D2.

During this time, the voltage across L1 (c) is clamped at the voltage $V_{C6} + V_{D2}$ (fwd.) and the current in the inductor decreases at the rate

$$\frac{di}{dt} = \frac{(V_{C6} + V_{D2}\ (\text{fwd.}))}{L1\ (c)}$$

When the current in L1 (c) falls below the load current required of the +20 volt supply, capacitor C6 starts discharging, decreasing V_{C6} until it falls below the 20 volt level set by the 20 turn potentiometer R_{22} in the voltage comparator. Transistor Q1 (c) is again turned on and the cycle is repeated. The circuit is designed such that Q1 (c) switches at a rate of about 22kHz. to 35kHz. to keep the ripple relatively small and capacitor C6 relatively fully charged.

The +15 volt supply is of the zener regulator type design and is derived from the +20 volt supply. It consists mainly of zener diode Z7, series dropdown resistors R23 and R35, filter capacitor C8, and the "snap turn on" circuitry of R24, C9, Z9, Q9, and Q10.

This "snap turn on" circuitry, which insures the proper turn on states of the integrated circuits, operates by sensing the voltage on the 20 volt supply through Z9 and Q9. It is slightly delayed by the RC combination of R24 and C9 and insures that the 20 volt supply is fully present before turning on series transistor Q10, and thereby the +15 volt supply.

Overcurrent protection is provided on the 20 volt output by the circuit consisting of R30, Q8, D11 and R28. This circuit operates when the current passing through R30 is sufficiently large enough (approx. 1 amp.) to cause an IR drop of enough voltage. (.7 volt) to turn on Q8, and thereby charge up capacitor C10. The combination of C10, R39, and D12 form the common discriminator circuit for all overcurrent and overvoltage inputs. When an input is sufficiently large to overcome the effects of shunting resistor R39, and charge capacitor C10 to approximately 1.4 volts to provide base drive to Q7, the switching supply is immediately shut down. This is accomplished by Q7 shorting the reference side of the voltage comparator differential amplifier to zero, thereby causing switching transistor Q1 (c) to turn off, allowing all outputs to drop to "0" volts.

Overcurrent protection (.5 amp.) is provided in the +15 volt output in a similar manner through the combination of R32, Q11 and D16.

Overvoltage protection in the +20 volt output is accomplished by Z6 and D21. If the 20 volt output exceeds the breakdown voltage of Z6 and D21, capacitor G10 in the common discriminator circuit charges and causes the supply to shut down as previously described.

Overvoltage protection of the +15 volt output is accomplished in a similar manner through Z8, D13, D14 and D15.

Restart of the switching supply requires the dc input voltage to be removed and reapplied. This is to allow start up circuitry capacitor C3 to discharge through R3 (approx. 0.8 second.) Upon reapplication of the input voltage, the charging R4 and C3 combination applies a voltage pulse, limited by Z1 to 20 volts, through diode D1 to the voltage comparator. This is sufficient to power the comparator and drive circuitry until the 20V. supply comes on and takes over through diode D10.

Reverse voltage protection to the power supply from accidental reverse application of the input voltage (station battery) to the SRCU-2 is provided by zener diode Z11. This zener, in series with the input to the module, blocks any

reverse voltage and only allows the supply to be energized if voltage polarity is applied to forward bias zener Z11.

Also contained on this module is the buffer resistor-capacitor combination for the 8/0 millisecond anti-bounce timer for the 52b contact input. A "48V" link is provided on this module for 48 volt operation of the relay, and should be removed for 125 volt operation. The function of this 48V link is to bypass the 125V series resistor R1 in the 8/0 millisecond timer buffer to allow the appropriate RC combination for 48 or 125 volt operation.

B. Synchronism Module ("SYNCHRONISM" – Position F)

Schematic Diagram Figure 8

Component location Figure 9

The synchronism printed circuit module contains the adjustable synchronism detector circuitry which responds to the phasing voltage between the bus and line potential transformers. A voltage difference signal between the transformers is full wave rectified by diodes D11 through D14, and applied to the base of transistor Q1 through a voltage divider network of resistor R7, R10, and R11. If this signal is greater than the voltage set on the emitter of Q1 by the voltage divider consisting of resistor R13 and 20 turn potentiometer R12, Q1 will turn on (phasing voltage is outside the set circle). The nonlinear attenuator on the input divider consisting of R8 and Z3, (and R9, TH-3, D15 and D16 for temperature stability) allow the 5 to 120 volt phasing voltage setting on the 20 turn potentiometer R12, to be uniformly sensitive over the complete range of 5 to 120 volts. This trimpot is located on the front of the module for ease of adjustment.

While the turn on of Q1, transistor Q2 turns on and applies a relative signal from the 20V dc supply into the level discriminator consisting of C4, R16, R17, D18, C5, and the circuitry associated with programmable unijunction transistor Q3. If this signal from Q2 is large enough (voltage/time) to charge capacitor C5 up to the firing voltage of Q3, Q3 fires and shorts the base drive from transistor Q4 turning it off to give a logic "1" SYN signal on module terminal 2. PUT Q3 remains latched on as long as the input signal remains sufficiently large. Once the signal drops below the setting, Q3 resets itself, allowing Q4 to turn on for a logic "0" SYN signal (phasing voltage is inside the set circle).

Typical phase-voltage curves for the SRCU-2 are shown in Figure 26.

This module also contains the rectifier and attenuator circuitry for the bus and line detectors where the respective signals from the bus and line potential transformers are full wave rectified and attenuated through respective nonlinear attenuators in the manner previously described. These signals are then sent to the HB, DB, HL and DL voltage detectors on the Line-Bus module.

C. Line-Bus Module ("LINE-BUS" – Position G)

Schematic diagram Figure 11.

Component location Figure 10.

The line-bus printed circuit module contains the 3 to 120 volt adjustable line and bus detectors circuitry. The attenuated line and bus signals from the synchronism module are compared to the corresponding settings on the four 20-turn potentiometers located at the front of the module for ease of adjustment. The four signals are then each treated in the same manner previously described for the circuitry on the synchronism module to arrive at the four output HB, DB, HL and DL. Each of the four levels can be individually set from 3 to 120 volts on its corresponding potentiometer. Individual test points are provided at the front of the module with a logic "0" reading indicating an input signal below the set point. These signals are then set to the Logic I module.

D. Logic I Module (LOGIC I" – Position H)

Schematic diagram Figure 12.

Component location Figure 13.

The logic I printed circuit module contains the corresponding logic circuitry to generate the

reclose supervisory functions SYN, HBDL, and HLDB, from synchronism, line and bus signals. Both time delayed reclosures are supervised by these three functions: that is, one of these functions must be present (within its setting) for the time delayed reclosures to take effect. Optional deletion of supervision of any of these functions can be accomplished by removal of corresponding programmable link on this module.

E. Counter Module ("COUNTER" – Position I)

Schematic diagram Figure 15.

Component location Figure 14.

The counter printed circuit module contains an 8/0 millisecond anti-bounce timer for the 52b contact input, and a NAND gate integrated circuit 4 step sequential counter. This counter responds to signals from the 52b contact, the HS reclose module, and the reset module, and sequences the SRCU-2 through its present functions. An operation to lockout selector link and the intermediate lockout selector link are located on the front panel of this module. By moving the adjustable link to the desired tap on the operations to lockout selector the SRCU-2 relay can be set to lockout the breaker after 1, 2, or 3 reclosing operations. The intermediate lockout option (lockout of SRCU-2 relay at one time delay reclosure less than the operations to lockout setting, 2nd or 3rd, depending upon tap setting) allows the last reclosure to occur for a synchronism condition only. This may be set by moving the link to the ON tap on the intermediate lockout selector.

F. Reset Module ("RESET" – Position J)

Schematic diagram Figure 16.

Component location Figure 17.

The reset printed circuit module contains the reset timer and circuitry which resets all elements, except the indicating lights, in the adjustable time of 3 to 60 seconds after the breaker remains closed. A calibrated dial is provided on the front panel of the module for ease of adjustment. The reset timer utilizes a programmable unjunction transistor circuit for range and accuracy. When the AND circuit associated with transistor Q1 is satisfied with both the breaker being closed (52b) and the counter having sequenced from the [1] position, the timer capacitors C7 and C10 are allowed to charge through potentiometer R10 and resistor R12. When the voltage on these capacitors reaches the firing level of Q2 (which is set by the voltage division on R15, R16 and R17), Q2 fires shorting the base drive to Q3, thereby causing it to turn off. This in turn allows the gate of IC6 to change state generating a logic "0" reset signal from module terminal 9.

This module also contains the sequence check circuitry which checks for any discrepancy of breaker operations (through the 52b contact) versus relay operation settings. This prevents pumping of the breaker by the SRCU-2 by blocking all reclosing in the relay if any discrepancy occurs. This locks the relay out upon the opening of the breaker.

The lockout circuitry is also contained on this module. It locks the SRCU-2 out, preventing further reclose operations after all desired set operations have occurred. In this lockout state the lockout relay is energized and a signal is sent to the indicator module to energize the lockout indicator.

G. High Speed Reclose Module ("HS RECL" – Position K)

Schematic diagram Figure 19.

Component location Figure 18.

The high speed reclose printed circuit module contains the control and adjustment circuitry for the high speed reclose timer. A 0-1 second calibrated dial is provided on the front panel of the module for ease of adjustment.

The high speed timer is controlled by a buffered H.S. initiate (permit) signal and a buffered H.S. block signal. The H.S. initiate signal from dc positive seals in after 8 milliseconds; the block signal prevents high speed reclosure, predominates over the initiate signal, and has a 60 millisecond override dropout timer for security.

The high speed reclosure is also supervised by the counter module in that it allows only the first reclosure to be a high speed reclosure. Optional supervision by a hot bus-dead line condition can be provided through the HBDL RECL programmable link on the circuit module. Removal of this link removes this option.

H. Time Delay Reclose Module ("TD RECL" – Position L)

Schematic diagram Figure 20.

Component location Figure 21.

The time delay reclose printed circuit module contains the dual 2-120 second adjustable reclose delay timers. A separate TD-1 calibrated dial and a TD-2 calibrated dial are provided on the front panel of the module for ease in adjustment of setting. The TD timers are controlled by signals from the counter and the logic I modules. The timer circuitry utilizes a programmable unijunction transistor (Q5) circuit for range and accuracy, which functions in a manner similar to that of the reset timer previously described. Both TD timers utilize the same timing capacitors and P.U.T. circuitry for scheme simplicity. The different time settings for TD-1 and TD-2 are achieved by switching a different calibrated potentiometer (R7 and R9) into the circuit for the two delays. This allows the TD-1 and TD-2 timers to be utilized to time the first and second time-delayed reclosures based on breaker operation or to be utilized to time a HLDB reclosure on the TD-1 timer and a HBDL reclosure on the TD-2 timer. This is accomplished by setting the three programmable links located on this module. When these links are set in the "A" position the TD timers follow breaker operation. When set in the "B" position the TD timers respond to bus and line conditions. These reclosures may be all HBDL, or all HLDB, or a selection of both, depending upon line and bus status.

I. Indicator Module ("INDICATOR" Position M)

Schematic diagram Figure 23.

Component location Figure 22.

The indicator printed circuit module contains the integrated circuit logic and driver circuitry for the functional indicators mounted on the front panel of the relay. The logic allows the indicator to show a history of relay operations. The indicators are reset through the logic by the test-reset switch on the front panel of the relay. When operated from the center position to either the test or the reset position this switch generates a logic "0" to cause the indicator logic to function, respectively checking on the integrity of the lamps or resetting of the seal-in indicators.

J. Logic II Module ("LOGIC II" Position N) – Optional

Schematic diagram Figure 24.

Component location Figure 25.

The Logic II printed circuit module contains a supervisory close function which overrides lockout to provide one additional reclosure. This buffered input activates logic circuitry to directly operate the close relay if either synchronism or either of the two line-bus conditions have been satisfied for greater than two seconds. This function is anti-pump and provides only one additional reclosure. It is released by removal of the supervisory close input. This function can be optionally deleted by removal of the SUPV. RECL. programmable link on this printed circuit module.

Also contained on this module is an inhibit function which will block all reclosing in the relay. There are four buffered inputs, two for channel trip and two for loss of channel, which activate the logic circuitry contained for this function.

Inhibit, which is delayed by 10 milliseconds and released 3 seconds after removal of the transfer trip signal, prevents reclosing during transfer trip even if both channels are lost. Inhibit will not occur if loss of channel is not preceded by a channel trip signal. This function can be optionally deleted by removal of the INHIBIT programmable link on this module.

The circuitry for a dead-line, dead-bus voltage output is also contained on this module. It provides a 20 volt dc signal after a DLDB condition has existed for a 5 second duration. This buffered output will then remain until reset by loss of the DLDB condition.

Line and Bus Potential Transformers

The line and bus potential transformers, which provide dc isolation, are located in the rear section of the chassis. Each is a 2:1:1 stepdown voltage transformer with a grounded static shield. One secondary from each transformer supplies information to the line and bus associated circuitry, and the other supplies information to the synchronism circuitry.

Close Relay

The operation of the close relay is controlled by the reclose circuitry on the T.D. Reclose module and the supervisory close circuitry on the Logic II module. Two normally open CR contacts are available.

Lockout Relay

The operation of the lockout relay is controlled by the operations to lockout and intermediate lockout circuitry on the Counter module and the sequence check and lockout circuitry on the Reset module. Two "form C" LR contacts are available. The lockout relay is energized when the SRCU-2 is in the lockout state (after sequencing with no successful reclosures), in the intermediate lockout state, and if the counter should fail to sequence in response to the 52b contact as detected by the sequence check circuitry.

Indicating Lights

The indicating lights are mounted on the front panel of the SRCU-2 relay and consist of one red power indicator and five amber functional indicators. The power indicator indicates the presence of the 20 volt d.c. regulated supply which powers the relay (15 volt d.c. integrated circuit supply is derived from the 20 volt supply). The functional indicators (High Speed Reclose, Hot-Line, Dead-Bus Reclose, Hot-Bus, Dead-Line Reclose, Synchronism Reclose, and Lockout) seal in, and can be tested and reset by the Test-Reset toggle switch.

Test-Reset Switch

The test-reset switch, mounted on the front panel of the SRCU-2 relay, is used to reset and test the functional indicators without disrupting any relay functions.

Internal Reclose Lockout Switch

The internal reclose lockout switch, mounted on an internal panel accessible with the door open, has a contact in series with each of the close relay contacts. When in the OFF position the contacts are open and the close relay contacts are prevented from performing the close function.

Bus-Line Potential Transformer Test Jacks

The bus-line potential transformer test jacks are wired directly to the bus and line potential transformer inputs. Polarity is shown by the use of red and black test jacks. These are accessible from the front of the relay with the door open, which facilitates monitoring and testing.

Theory Of Operation

The basic operation of the SRCU-2 relay will be described with the aid of Figure 3 internal logic schematic 645F607, Figure 4 external logic drawing, the individual module schematics, and Table I.

With three reclosures to lockout selected by the adjustable link on the front panel of the counter module, one high speed reclosure followed by up to two time delayed reclosures will be provided. With the breaker initially open and normal voltage applied to the SRCU-2 the lockout state will be assumed. Under these conditions the amber lockout indicator and the lockout relay will be energized, the counter module output terminals 5, 13 and 11 will be at a "0" logic level and no reclosing can take place. It is important to note that upon dc application the SRCU-2 will always assume the lockout state.

Upon closure of the breaker and opening of the 52b contact, the reset timer is enabled through the circuitry of the 8/0 millisecond 52b anti-bounce timer (counter module terminal 9 – reset module terminal 6). The reset timer is a 3-60 second adjustable timer that is dial calibrated on the front of the reset printed circuit module. Reset of all elements except the indicating lights occurs after the breaker remains closed for the pre-adjusted reset time. The logic "0" reset signal applied to terminal 10 of the counter module resets the counter to its normal state. In this state counter terminal 5 has a logic "1" which, in turn, disables the reset module terminal 10.

The logic "1" from counter terminal 5 is also sent to the high speed reclose circuitry and the time delay reclose circuitry. Applied to terminal 2 of the high speed reclose module it enables the circuitry to allow the T.D. −1 timer to start upon closure of the 52b contact (breaker trip). This allows the TD-1 reclosure to take place if the high speed reclosure is not initiated, which would result in only the two T.D. reclosures to the lockout state.

If it is now assumed that a permanent fault occurs on the line and the breaker is tripped, a High Speed reclosure takes place with the receipt of a H.S. RECL. initiate signal (48/125VDC) on terminal 8 of the relay (term. 11 of the H.S. RECL. module). This initiate signal actuates the H.S. 0-1 second adjustable calibrated timer, which provides a settable range from no intentional delay (.05 second inherently built into the SRCU-2) to the appropriate dead time for EHV applications.

The H.S. RECL. input has an 8/0 millisecond seal-in circuit to provide additional security, and allow a momentary signal to activate the High Speed reclose circuitry. Upon completion of the H.S. time delay the close relay (CR) is energized to reclose the breaker. Note that the pickup time of the CR is included in the calibration of the time dial and contributes to the inherent 50 millisecond minimum time of the H.S. RECL.

With the reclosure of the breaker, the 52b contact opens and the "AND" circuit on the H.S. RECL. module is satisfied to allow a "0" output from terminal 5 of this module to activate the H.S. reclose indicator circuitry and energize the amber H.S. RECL. indicator. The opening of the 52b contact also advanced the counter to the second reclose state. In this state counter module terminal 5 is a "0", terminal 13 is a "1", and terminal 11 is a "0".

This change satisfies the sequence check circuitry which is designed to check for any discrepancy of breaker operations (through 52b contact) versus relay operation settings. If any discrepancy occurs, the lockout state is assumed by the relay, thus making the SRCU-2 anti-pump for failures.

With the relay in the second reclose state, the H.S. reclose circuitry can no longer be activated due to the change of the logic "1" to logic "0" of the first reclose state of the counter on H.S. reclose module terminal 2.

The logic "1" of the second reclose state applied to T.D. reclose module terminal 8 allows the first time delayed reclosure TD-1 to start upon receipt of indication of a second trip of the breaker (52b closure) and receipt of a legitimate signal from the Logic I module as to either a SYN, a HLDB, or a HBDL condition being satisfied. Optional deletion of supervision of any of these Logic I module functions can be accomplished by removal of the corresponding links on the Logic I module.

Likewise, the change to the second reclose state of the counter allows the reset timer to start, if the breaker is closed. This timer, if allowed to time out, resets the SRCU-2. However, since it is assumed that a permanent fault occurred on the line, the breaker is again tripped, which stops the reset timer and resets it.

Now, upon receipt of indication of a second trip of the breaker (52b closure) all requirements for a T.D. −1 reclosure are met and the T.D. −1 reclose timer circuitry is actuated. This timer has an adjustable range of 2 to 120 seconds. Upon completion of the TD-1 time delay the close relay (CR) is energized to reclose the breaker. The pickup time of the CR is included in the calibration of the T.D. −1 time dial.

At the same time that the close relay is energized, a signal indicating that the close relay is sent to the corresponding "AND" circuits which, when respectively satisfied, activate the indicator circuitry of the three TD indicators — SYN, HBDL and HLDB. The requirements for indication are the respective signal being present (SYN or HBDL or HLDB), the close relay being energized, and finally, indication of closure of the breaker by the opening of the 52b contact. Thus, with the reclosure of the breaker after the TD-1 time delay a respective "AND" circuit is satisfied, and one indicator circuit and its respective functional indicator are energized.

The opening of the 52b contact after the TD-1 reclosure also advances the counter to the third reclose state. In this state counter module terminal 5 is a logic "0", terminal 13 is a "0", and terminal 11 is a "1". This change satisfies the sequence check circuitry for anti-pump protection. With this closure of the breaker the reset timer once again starts timing. This timer, if allowed to time out, would reset the SRCU-2. However, since it is assumed that a permanent fault occured on the line, the breaker is again tripped, which stops the reset timer and resets it.

With the closure of the 52b contact upon this third trip, the TD-2 timer is activated and recloses the breaker in the time set on the TD-2 calibrated dial in a manner similar to that previously described for TD-1 reclosure. The TD-2 reclose functional indicator is also activated in a manner previously described to energize the respective SYN, HLDB, or HBDL indicator.

The opening of the 52b contact upon the TD-2 (3rd) reclosure now advances the counter to the state where counter module terminals 5, 13 and 11 all have a logic "0", output. This change once again satisfies the sequence check circuitry for anti-pump protection. Likewise, the reclosure of the breaker once again starts the reset timer. However, since a permanent fault on the line is assumed the breaker is again tripped stopping the reset timer and resetting it.

This trip of the breaker, with the counter module outputs to the reclose circuitry at logic "0",, caused the SRCU-2 to assume the lockout state. This is accomplished when the 52b control signal on reset module terminal 6 becomes a logic "1" upon trip of the breaker. This completes the "AND" circuit with the three logic "0" counter reclose outputs. In the lockout state the lockout relay and the lockout indicator are energized and no reclosing or resetting functions are permitted to take place. The SRCU-2 will remain in this lockout state until the breaker is manually or electrically reclosed.

If we now assume that the fault has been cleared and the breaker is closed the reset circuitry of the SRCU-2 will perform in the manner previously described to reset the relay to the state shown in Figure 3, ready to go through another full sequence in line with the settings made at the beginning of this description.

The high speed reclosure may also optionally be set for supervision by a hot bus, dead-line condition. The HBDL RECL programmable link on the H.S. RECL module, when in position, requires that a HBDL condition exists for H.S. reclosing. Removal of this link removes this option.

The two time delay reclosures may optionally be changed from reclosing based upon breaker operations to reclosing based upon line and bus conditions. This allows one reclosing time delay for a HLDB condition and a different reclosing time delay HBDL condition. The TD-1 timer is then utilized for a HLDB reclosure and the TD-2 timer is utilized for a HBDL reclosure. This can be accomplished by changing the basic "AND" requirements for the timers by switching the three programmable links located on the T.D. RECL module from the A position to the B position.

Another option incorporated into the SRCU-2 is the intermediate lockout function. This function brings the relay to the lockout position one reclosure prior to final lockout, allowing the final reclosure to occur under synchronism check supervision only. In the previous example with the SRCU-2 set for three reclosures to lockout, the SRCU-2 would attain the lockout state after the second reclosure (TD-1) and would allow the final or third reclosure (TD-2) when synchronism exists between the line and the bus. This intermediate lockout function can be optionally switched on or off by changing the programmable link on the counter module front panel.

The logic II module (an optional inclusion depending upon relay style) contains the supervisory close function which will allow one additional reclosure, after all the reclosing operations set on the operations to lockout control. This function overrides the lockout state of the SRCU-2 to provide the additional reclosure. The buffered input activates the appropriate logic circuitry to directly operate the close relay if synchronism or either of the two line-bus conditions have been satisfied for greater than 2 seconds. The logic features anti-pump protection for the additional reclosure. The function is released by removal of the supervisory close input. Optional deletion of this function can be accomplished by removal of the SUPV. RECL. programmable link on this printed circuit module.

Also contained on this optional module is the inhibit function which, when activated, will block all reclosing by the SRCU-2. There are four buffered inputs, two for channel trip and two for loss of channel, which activate the logic circuitry provided for this function. This inhibit function is delayed by a 10 millisecond timer and will release 3 seconds after removal of the transfer trip signal. Reclosing will be prevented during transfer trip even if both channels are lost. Inhibit will not occur if loss of channel is not preceded by a channel trip signal. This function can be optionally deleted by removal of the INHIBIT programmable link on this module.

The dead-line, dead-bus voltage output, another optional function contained on this module, supplies a voltage output for initiating trip on the basis of DLDB after 5 seconds. This buffered output is capable of driving an external ARS type relay for tripping.

TABLE I – LOGIC STATES OF COUNTER MODULE

SRCU-2 SET FOR 3 RECLOSING OPERATIONS TO LOCKOUT (HS, TD-1, AND TD-2)							
BREAKER POSITION	COUNTER MODULE 205C643G01 LOGIC STATES					RELAY FUNCTION	INDICATORS ENERGIZED
	TERMINAL 14 52B CONTACT INPUT	TERMINAL 9 BREAKER STATUS OUTPUT	TERMINAL 5 OUTPUT TO 1ST RECLOSE CIRCUITRY	TERMINAL 13 OUTPUT TO 2ND RECLOSE CIRCUITRY	TERMINAL 11 OUTPUT TO 3RD RECLOSE CIRCUITRY		
CLOSED Reset Position	1	0	1	0	0	RESET POSITION	POWER
OPEN First Trip	0	1	1	0	0	ENABLES FIRST ENCLOSURE	POWER
CLOSED First Reclosure (H.S. RECL)	1	0	0	1	0	ENABLES RESET	POWER H.S. RECL.
OPEN Second Trip	0	1	0	1	0	ENABLES SECOND RECLOSURE	POWER H.S. RECL.
CLOSED Second Reclosure (TD-1 RECL)	1	0	0	0	1	ENABLES RESET	POWER H.S. RECL (TD-1 RECL) { SYN or HBDL or HLDB
OPEN Third Trip	0	1	0	0	1	ENABLES THIRD RECLOSURE	POWER H.S. RECL (TD-1 RECL) { SYN or HBDL or HLDB
CLOSED Third Reclosure (TD-2 RECL)	1	0	0	0	0	ENABLES RESET	POWER H.S. RECL (TD-1 RECL) { SYN or HBDL or HLDB (TD-2 RECL) { SYN or HBDL or HLDB
OPEN Fourth Trip	0	1	0	0	0	LOCKOUT POSITION	POWER H.S. RECL. (TD-1 RECL) { SYN or HBDL or HLDB (TD-2 RECL) { SYN or HBDL or HLDB LOCKOUT

CHARACTERISTICS

DC Control Voltage

The SRCU-2 relay is designed to operate on either 48 or 125 volts dc with no settings or adjustments required other than the 52b contact 8/0 millisecond anti-bounce timer adjustment link located on the power module. The operating range of the SRCU-2 is 42 to 140 volts d.c.

Line-Bus Voltage

The SRCU-2 relay is designed with two single phase potential transformers rated at 132Vac (rms) continuous.

Energy Requirements

Dc Burden: 14 watts at 48Vdc control voltage
16 watts at 125Vdc control voltage

AC Burden:

Bus Potential Transformer:	7 Volt-Amperes max. at 120Vac 60Hz.
Line Potential Transformer:	7 Volt-Amperes max. at 120Vac 60Hz.

Logic Inputs:

52b contact	48/125Vdc control voltage 48V-12mA max. current output to negative 125V-10mA max. current output to negative
H.S. RECL. H.S. BLOCK SUPV. CLOSE	48/125Vdc control voltage burden 48V-1.5mA max. current 125V-2.5mA max. current
All other inputs	15 to 20Vdc buffered 2mA max. current

Logic Outputs:

DLDB	15 to 20Vdc buffered 10mA max. current

Time Delays

Reset	3-60/0 adjustable timer Pickup ±10% Dropout - less than 1msec.
H.S. Reclose	0-1/0 adjustable timer Pickup .05 - 1 second ±5% Dropout less than 1 msec.
TD-1 Reclose	2-120/0 adjustable timer Pickup ±5% Dropout less than 1 msec.
TD-2 Reclose	2-120/0 adjustable timer Pickup ±5% Dropout less than 1 msec.

Line-Bus Detectors

Hot Line	3-120 volts adjustable level-detector ±5%
Dead Line	3-120 volts adjustable level-detector ±5%
Hot Bus	3-120 volts adjustable level-detector ±5%
Dead Bus	3-120 volts adjustable level-detector ±5%
Synchronism	5-120 volts adjustable level-detector ±5%

Surge Withstand Capability

Withstands SWC test proposed by the IEEE Power System Relaying Committee IEEE C72-033-4.

Dimensions

Height	5.25 inches (3 rack units)
Width	19 inches
Depth	14 inches

Weight

Approximately 22 lbs.

Temperature Range

–20°C to +55°C chassis ambient without departure from stated tolerances.

–30°C to +70°C chassis ambient without failure.

SETTINGS

Control Voltage

The only control voltage setting required on the SRCU-2 is the 52b contact, 8/0 anti-bounce timer adjustment located on the power module. The programmable link (48V) should be in place for 48 volt control voltage operation, or removed for 125 volt operation.

Line-Bus Voltage Detectors

The four voltage level detectors on the line-bus module to indicate line and bus status should be

set to the desired setting between 3 to 120Vac by the trimpots HL, DL, HB and DB and their corresponding test points. A logic "0" reading on module test points HL, DL, HB and DB indicates an input signal below the set point.

Synchronism Detector

The synchronism detector on the synchronism module should be set to the desired setting by the SYN trimpot. Typical voltage-angle characteristics of the SRCU-2 for various voltage settings with rated voltage on one circuit is shown in Figure 26. With both the bus and the line voltages in phase the syn. detector can be set from a 5 to 120 Vac voltage difference. A logic "0" reading on the SYN. test point indicates an input signal below the set point. Note that synchronism requires that either Bus or Line or both be "hot".

Reclosing Operations to Lockout

The reclosing operations to lockout selector link located on the front panel of the counter module should be set to the desired number of reclosing operations. By moving the adjustable link to the desired tap on the operations to lockout selector, the SRCU-2 can be set to lockout the breaker after 1, 2 or 3 reclosing operations. When operating on less than 3 reclosing operations to lockout, the reclosing intervals will be dropped starting with the third interval first.

Intermediate Lockout

The intermediate lockout selector link located on the front panel of the counter module should be set to either allow or disallow the intermediate lockout option. The intermediate lockout function (lockout of the SRCU-2 relay at one time-delay reclosure less than the operations to lockout setting, 2nd or 3rd, depending upon link setting) allows the last reclosure to occur for a synchronism condition only. This may be set by moving the link to the ON tap on the intermediate lockout selector.

High Speed Reclose Timer

The high speed reclose time delay should be set to the desired delay with the calibrated potentiometer located on the front panel of the H.S. RECL. module. The knob may be set between the limits shown, 0 (.050) to 1.0 seconds. After making the timer setting, lock the knob by tightening the screw on the knob lock tab assembly.

Hot-Bus, Dead-Line High Speed Reclose Option

The high speed reclosure may also be optionally set to be supervised by a HBDL condition by the HBDL RECL. programmable link on the high speed reclose module. Removal of this link removes this option.

Time Delay Reclose Timers

The time delay reclose timers, TD-1 and TD-2, should be set to the desired time delays with the calibrated potentiometers located on the front panel of the TD RECL module. Both knobs may be set between the limits shown, 2 to 120 seconds. After making the timer settings, lock the knobs by tightening the screw on the knob lock tab assemblies.

Logic I Supervision of Time Delay Reclosures

The three programmable links on the logic I module, HLDB, HBDL, and SYN, should be set for the desired functions for supervision of the T.D. Recl. timers. Both time delayed reclosures are supervised by these three functions; that is, one of these functions must be present (within its setting) for the time delayed reclosures to take effect. Deletion of supervision of any of these functions can be set by removal of the corresponding programmable link on the Logic I module.

Separate Timing Option for HLDB and HBDL Time Delay Reclosing

The TD-1 and TD-2 timers may be optionally set to time a HLDB reclosure on the TD-1 timer and a HBDL reclosure on the TD-2 timer instead of timing the first and second time delayed reclosures based on breaker operation. This is accomplished by setting the three programmable links located on the TD Reclose module. When these links are set in the "A" position the TD timers follow breaker operation. When set in the "B" position the TD timers respond to the bus and line conditions. These reclosures may be all HBDL, or all HLDB, or a selection of both depending upon line and bus status.

Reset Timer

The reset time delay should be set to the desired delay with the calibrated potentiometer located on the front panel of the reset module. The know may be set between the limits shown, 3 to 60 seconds. After making the timer setting, lock the know by tightening the screw on the knob lock tab assembly.

Inhibit Function (Optional with Logic II Module)

The inhibit function is set to block all reclosing by the SRCU-2 relay during transfer trip, even if both channels are lost. Inhibit will occur if loss of channel is preceded by a channel trip signal. This function can be deleted by removal of the INHIBIT programmable link on the Logic II module.

Supervisory Close Function (Optional with Logic II Module)

The supervisory close function is set to override lockout and provide one additional reclosure, when activated, if either synchronism or either of the two line-bus conditions have been satisfied for greater than two seconds. This function can be deleted by removal of the SUPV. RECL. programmable link on the LOGIC II module.

INSTALLATION

The SRCU-2 relay is mounted on a 19 inch wide panel, 5¼ inches high (3 rack units) with edge slots for mounting on a standard relay rack or panel. For the outline and drilling plan, refer to Figure 28. The mounting location must be free from dust, excessive humidity, vibration, corrosive fumes or heat. The maximum temperature around the chassis should not exceed +55°C for normal operation (see CHARACTERISTICS for temperature range specifications).

ADJUSTMENTS & MAINTENANCE

The proper adjustments to insure correct operation of this relay have been made at the factory. Upon receipt of the relay, no customer adjustments other than those covered under "SETTINGS" should be required.

Acceptance Check

It is recommended that an acceptance check be applied to the SRCU-2 relay to verify that the circuits are functioning properly. The SRCU-2 test diagram shown in Figure 27 aids in test of the relay. Proper energization of the relay is also shown in this figure.

A. DC Regulated Supplies (POWER Module)

DC Voltages measured at the respective test points should ±5% for +20 volts and +15 volts over a dc input range of 42 to 140Vdc. Short circuit protection shuts the power supply off if either +20Vdc or +15Vdc are overloaded or short circuited to NEG.

B. Bus-Line Voltage Detectors (LINE-BUS Module)

The four voltage level detectors to indicate line and bus status should be adjustable from 3 to 120 VAC by the trimpots HL, DL, HB and DB. Corresponding module test points are provided, with a logic "0" reading on these test points indicating an input signal below the set point. The line and bus voltages may be applied to the relay terminals directly or to the corresponding test jacks on the front of the relay.

C. Synchronism Detector (SYNCHRONISM Module)

The synchronism detector should be adjustable from 5 to 120VAC (bus-line voltage difference with both in phase) by the Syn. trimpot. All characteristics of the voltage-angle curves shown in Figure 26 should be obtainable. Syn test point "0" reading indicates an input signal below the set point (within the circle).

D. Function Operation

1. Relay Energization

The SRCU-2 relay should come on in the lockout state (lockout relay and lockout indicator energized) upon energization of D.C. with breaker open. Relay should reset (after breaker is closed) in the reset time delay setting.

2. Link-Programmed Operation

The SRCU-2 relay should operate functionally in accordance with the printed circuit module link-settings per tests I through XVI of Table II. All settings and time delays should be within tolerance.

3. Test/Reset Switch

When pushed to test position all indicators should be energized. When pushed to reset position all indicators except the power indicator should turn off.

4. Internal Reclose Lockout Switch

The internal reclose lockout switch (wired with its two contacts in series with each of the close relay contacts) in the off position prevents reclosure of the breaker.

At completion of the acceptance test return all settings and links to desired position.

TABLE II

Functional Operation Note: Respective indicators should light when each controlling function recloses breaker. Λ = H.S. Reclose permit signal 48/125 VDC applied to relay term. 8 required for H.S. reclosure.	PRINTED CIRCUIT MODULE	Power 205C655G01	Logic II 205C645G01	TD Reclose 205C659G01	HS Reclose 205C647G01	Logic I 205C657G01	Counter 205C643G01	FUNCTIONAL TEST
	LINK	48V. 52b Input	Inhibit Supv. Close	A-B A-B A-B	HBDL H.S. Recl.	HBDL HLDB SYN.	Operations to Lockout Inter. Lockout	
3 Reclosing Operations to Lockout H.S.Λ, TD-1, and TD-2 (or 2 operations to Lockout -TD-1 and TD-2 without HS Permit Signal Λ). T.D. Reclosing Operations Supervised by SYN. or HBDL, or HLDB condition.	I	Off	Off Off	A A A	Off	On On On	3 Off	
2 Reclosing Operations to Lockout H.S. Λ, and TD-1 (or 1 operation to Lockout - TD-1, without HS Permit Signal Λ). T.D. -1 Reclosing Operation supervised by SYN. or HBDL or HLDB condition.	II	Off	Off Off	A A A	Off	On On On	2 Off	
1 Reclosing Operation to Lockout H.S. with Permit Signal Λ (or TD-1 without Permit Signal Λ). T.D.-1 Reclosing Operation supervised by SYN. or HBDL, or HLDB condition.	III	Off	Off Off	A A A	Off	On On On	1 Off	
2 Reclosing Operations to intermediate Lockout (H.S. Λ and TD-1). 3rd. reclosure (TD-2) to final lockout only when SYN. condition exists. T.D.-1 Reclosing Operation supervised by SYN. or HBDL or HLDB condition.	IV	Off	Off Off	A A A	Off	On On On	3 On	
H.S. Reclosing Operation Λ to intermediate lockout. 2nd Reclosure TD-1 to final lockout only when SYN. condition exists.	V	Off	Off Off	A A A	Off	On On On	2 On	
Same as III	VI	Off	Off Off	A A A	Off	On On On	1 On	
Same as I except TD reclosures controlled by HBDL and HLDB conditions (HBDL on TD-2 timer and HLDB on TD-1 Timer). TD reclosure may be all HBDL or all HLDB or one of each.	VII	Off	Off Off	B B B	Off	On On On	3 Off	
Same as II except TD reclosures controlled by HBDL and HLDB conditions (HBDL on TD-2 timer and HLDB on TD-1 Timer). TD reclosure may be HBDL or HLDB.	VIII	Off	Off Off	B B B	Off	On On On	2 Off	

TABLE II

Functional Operation Note: Respective indicators should light when each controlling function recloses breaker. Δ = H.S. Reclose permit signal 48/125 VDC applied to relay term. 8 required for H.S. reclosure.	PRINTED CIRCUIT BREAKER	LINK	FUNCTIONAL TEST							
			IX	X	XI	XII	XIII	XIV	XV	XVI
Same as III except T.D. reclosure controlled by HBDL or HLDB.	Power 205C655G01	48V. 52b Input	Off	Off	Off	Off	Off	Off	Off	On
	Logic II 205C645G01	Inhibit Supv. Close	Off Off	Off Off	Off Off	Off Off	Off Off	On Off	Off On	Off Off
	TD Reclose 205C659G01	A-B A-B A-B	B B B	A A A	A A A	A A A	A A A	A A A	A A A	A A A
	HS Reclose 205C647G01	HBDL H.S. Recl.	Off	On	Off	Off.	Off	Off	Off	Off
	Logic I 205C657G01	HBDL HLDB SYN.	On On On	On On On	Off On On	On Off On	On On Off	On On On	On On On	On On On
	Counter 205C643G01	Operations to Lockout Inter. Lockout	1 Off	3 Off	3 Off	3 Off	3 Off	3 Off	3 Off	3 Off
Same as I except T.D. reclose Δ also requires a HBDL condition.										
Same as I except T.D. reclosing supervision by HBDL is removed.										
Same as I except T.D. reclosing supervision by HLDB is removed.										
Same as I except T.D. Reclosing supervision by Syn. is removed.										
Same as I except all reclosing is inhibited when (1) a channel trip signal is applied to relay term. 21 or 22 (Inhibit is 10Msec. delayed with 3 sec. or more dropout after removal of trip signal) (2) A channel loss signal to relay term. 23 or 24 is preceded by a channel trip signal. No inhibit is to occur if channel loss is not preceded by channel trip										
Same as I except additional reclosure available after lockout by applying signal to relay term. 25 if either SYN. or HBDL or HLDB condition is satisfied for greater than 2 sec. One reclosure only if provided and can be released by removal of supv. close input (term. 25).										
52b input buffer 8/0 Msec. anti-bounce timer for 48 volt supply voltage.										

Routine Maintenance

All relays should be inspected periodically and all settings and times of operation should be checked at least once every year or at such other intervals as may be indicated by experience to be suitable to the particular application.

Calibration

The proper adjustments to insure correct operation of the relay have been made at the factory and should not be disturbed after receipt by the customer. However, if the adjustments or any components have been changed or modules interchanged, then that portion of the SRCU-2 relay changed should be recalibrated and acceptance checked.

The areas where recalibration is possible are as follows:

1. Power Supply Module

   Trimpot. R22 must be adjusted such that the +20Vdc test point is within 1% of +20Vdc.

2. No other calibration is necessary other than desired changes in settings.

Trouble Shooting

The components in the SRCU-2 relay are operated well within their ratings and normally will give long and trouble free service. However, if a relay has given indication of trouble in service or during routine checks, then using "0" and "1" logic notation, the faulty printed circuit module (s) can be identified using the relay logic schematic, Figure 3.

In turn, the faulty component, connection, or circuit can be found using the individual module schematics which show the detailed NOR/NAND logic.

Each NOR block, shown by an AND with negated inputs or an OR with negated output represents a transistor on the module schematic. Likewise, each NAND integrated circuit is represented by an AND with a negated output or an OR with negated inputs with the specific I.C. terminals described.

Voltage levels for "0" and "1" logic states shown on the Fig. 3 logic drawing are:

Logic "0" is equivalent to less than 1Vdc and a logic "1" is equivalent to 8 to 15Vdc, except for the negative logic outputs to the indicators, close relay, and lockout relay where "0" is 20Vdc and "1" is zero.

For voltage levels on modules not employing conventional logic, refer the particular module operation description.

A module extender, style no. 3494A90G01, is available for facilitating circuit voltage measurements. Do not remove or insert modules while the SRCU-2 relay is energized as damage may result.

RENEWAL PARTS

Repair work can be done most satisfactorily at the factory. However, interchangeable parts can be furnished to the customers who are equipped for doing repair work. When ordering parts, always give data and appropriate Westinghouse style numbers.

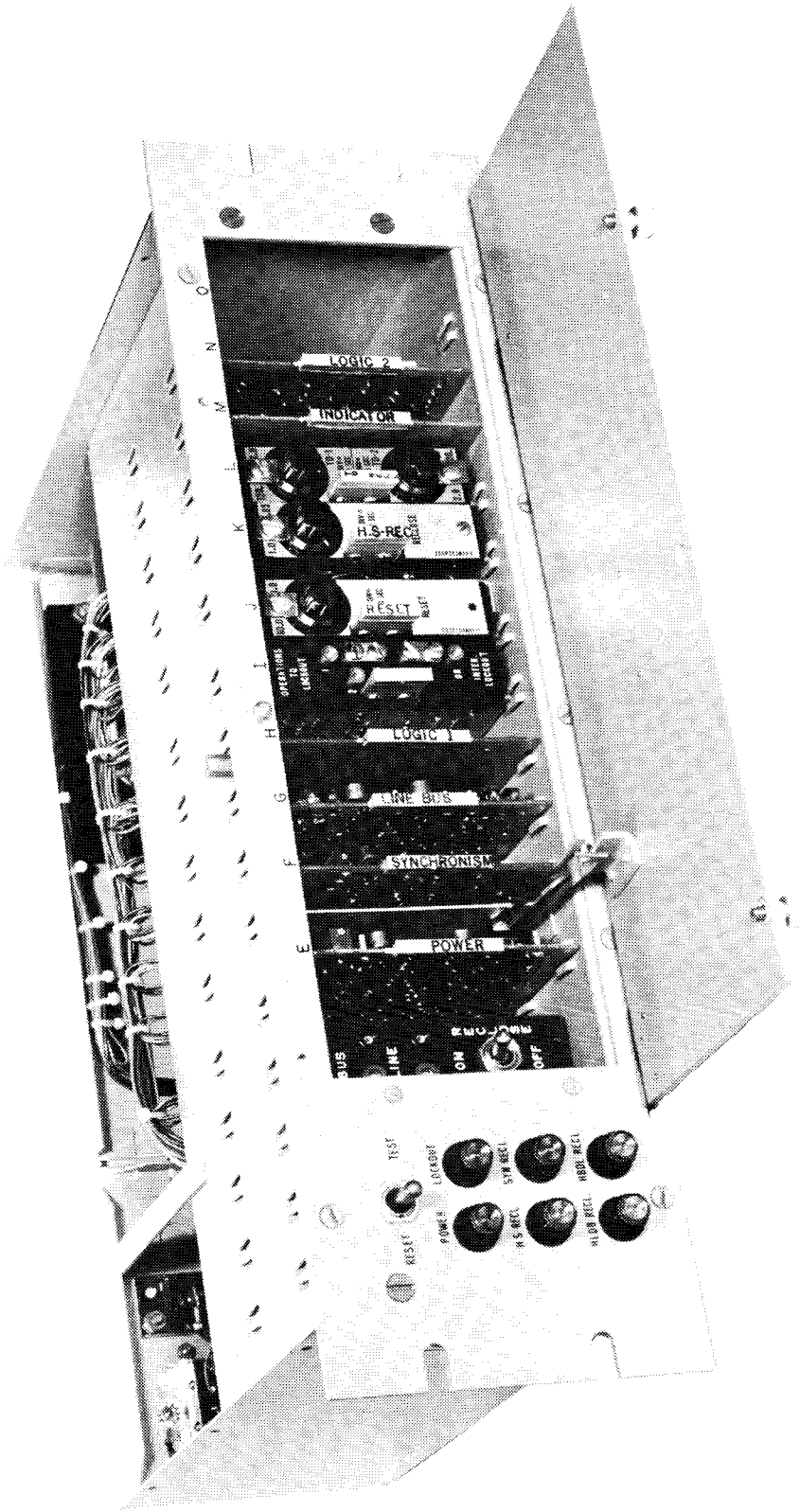


Fig. 1 Type SRCU-2 Relay – Front View

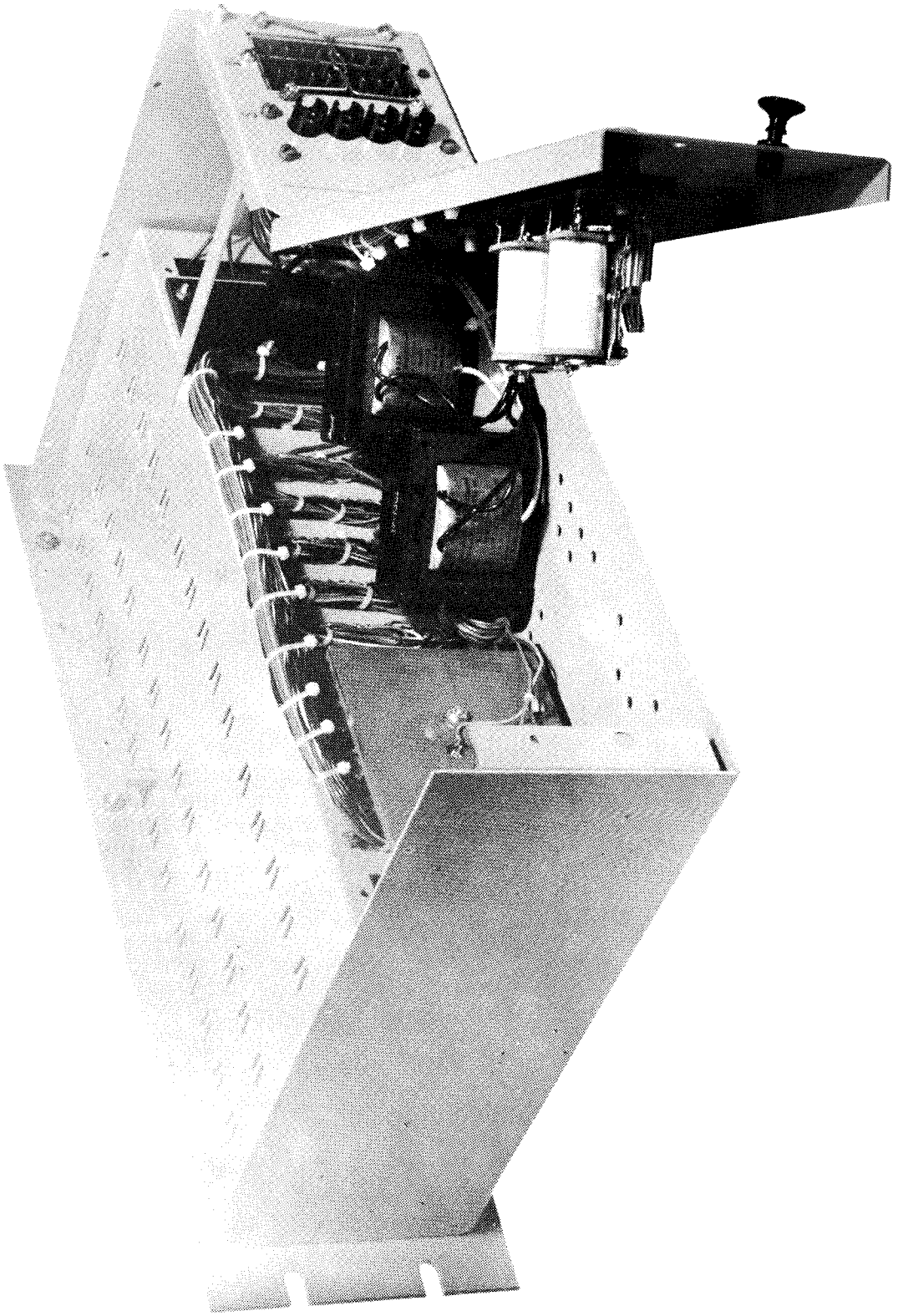
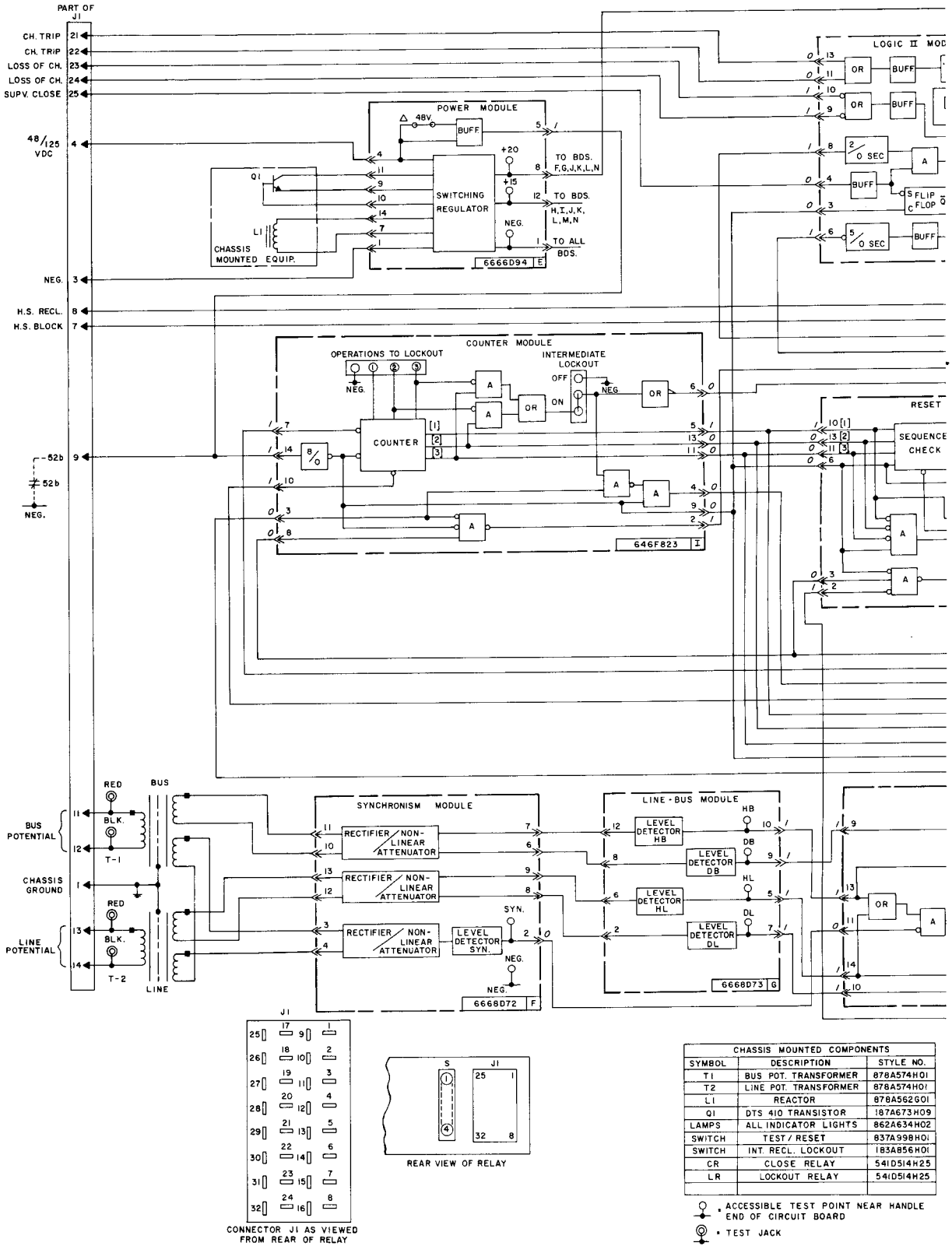


Fig. 2 Type SRCU-2 Relay – Rear View

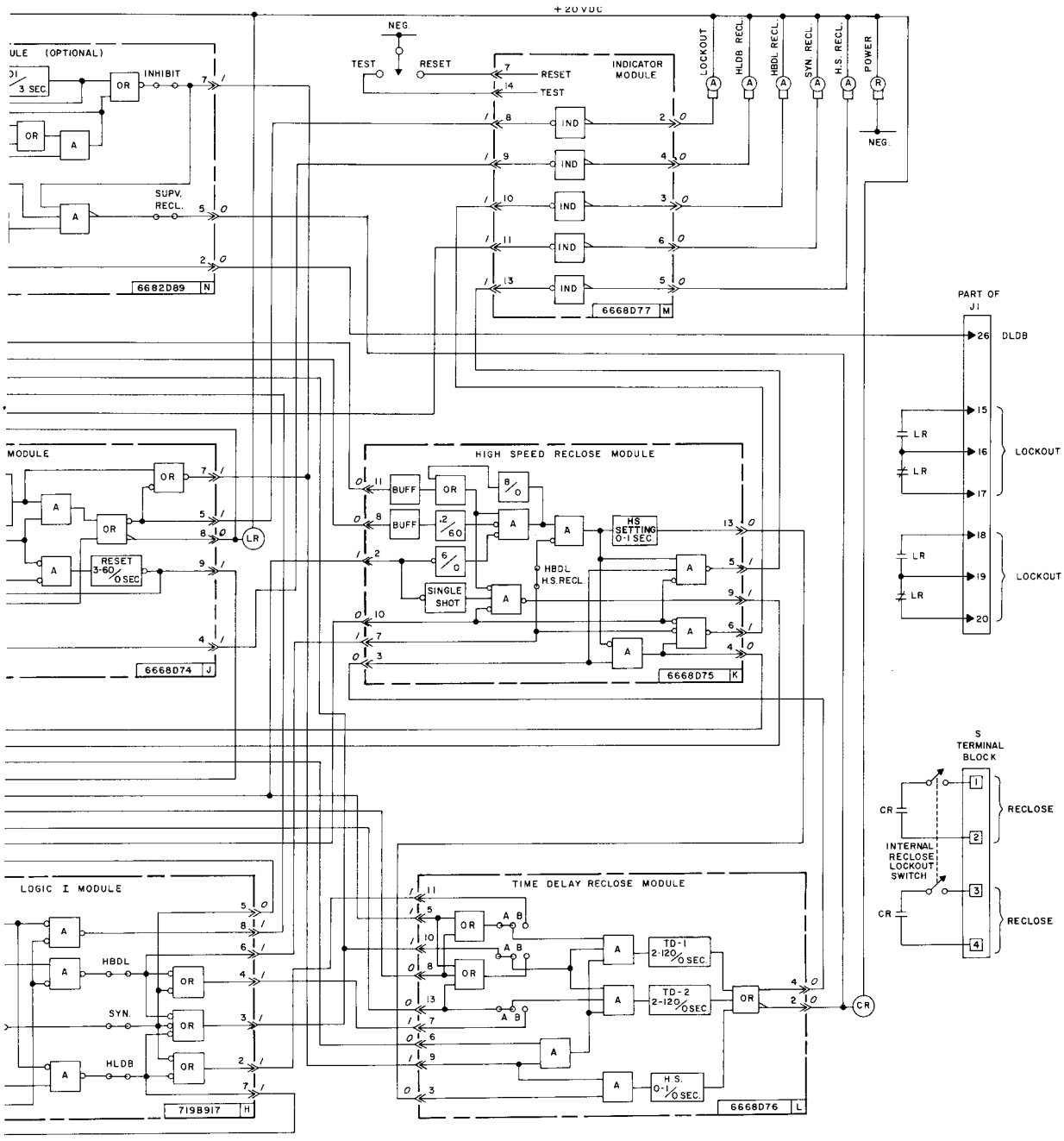


CHASSIS MOUNTED COMPONENTS		
SYMBOL	DESCRIPTION	STYLE NO.
T1	BUS POT. TRANSFORMER	878A574H01
T2	LINE POT. TRANSFORMER	878A574H01
L1	REACTOR	878A562G01
Q1	DTS 410 TRANSISTOR	187A673H09
LAMPS	ALL INDICATOR LIGHTS	862A634H02
SWITCH	TEST / RESET	837A998H01
SWITCH	INT. RECL. LOCKOUT	183A856H01
CR	CLOSE RELAY	541D514H25
LR	LOCKOUT RELAY	541D514H25

○ • ACCESSIBLE TEST POINT NEAR HANDLE END OF CIRCUIT BOARD

◎ • TEST JACK

Fig. 3 SRCU-2 Inter

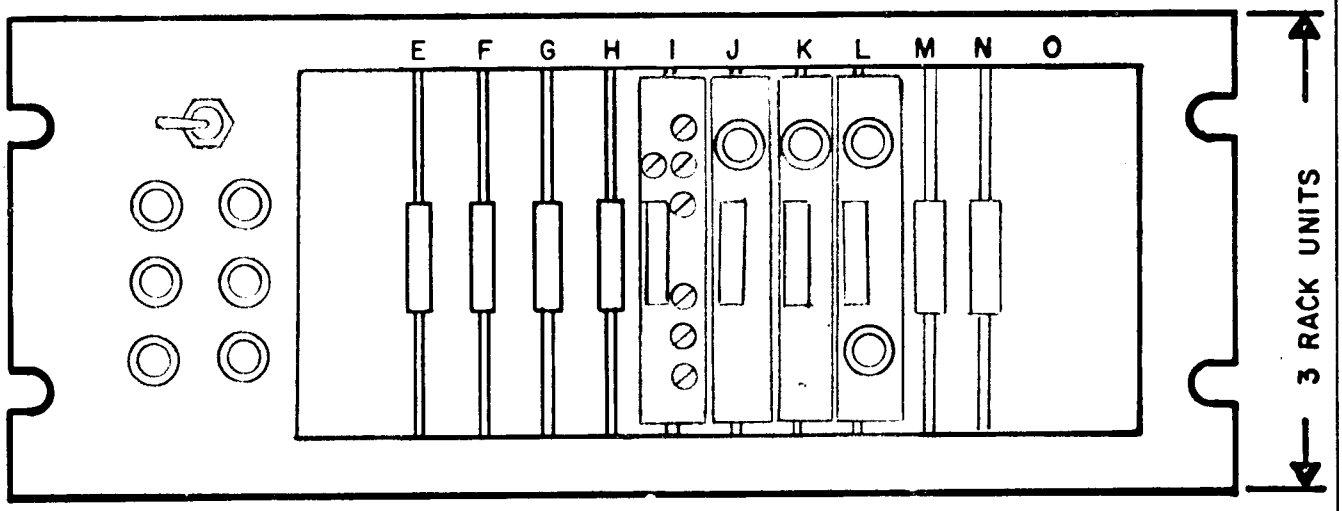


NOTES:

△ = REMOVE 48 VOLT LINK FOR 125 VDC OPERATION ON POWER MODULE LOCATION "E".

SIGNAL STATES "0" OR "/" ARE SHOWN FOR ALL NORMAL CONDITIONS WITH BREAKER CLOSED, 52b OPEN, SRCU-2 RESET, BOTH LINE AND BUS "HOT" AND IN SYNCHRONISM.

645F607

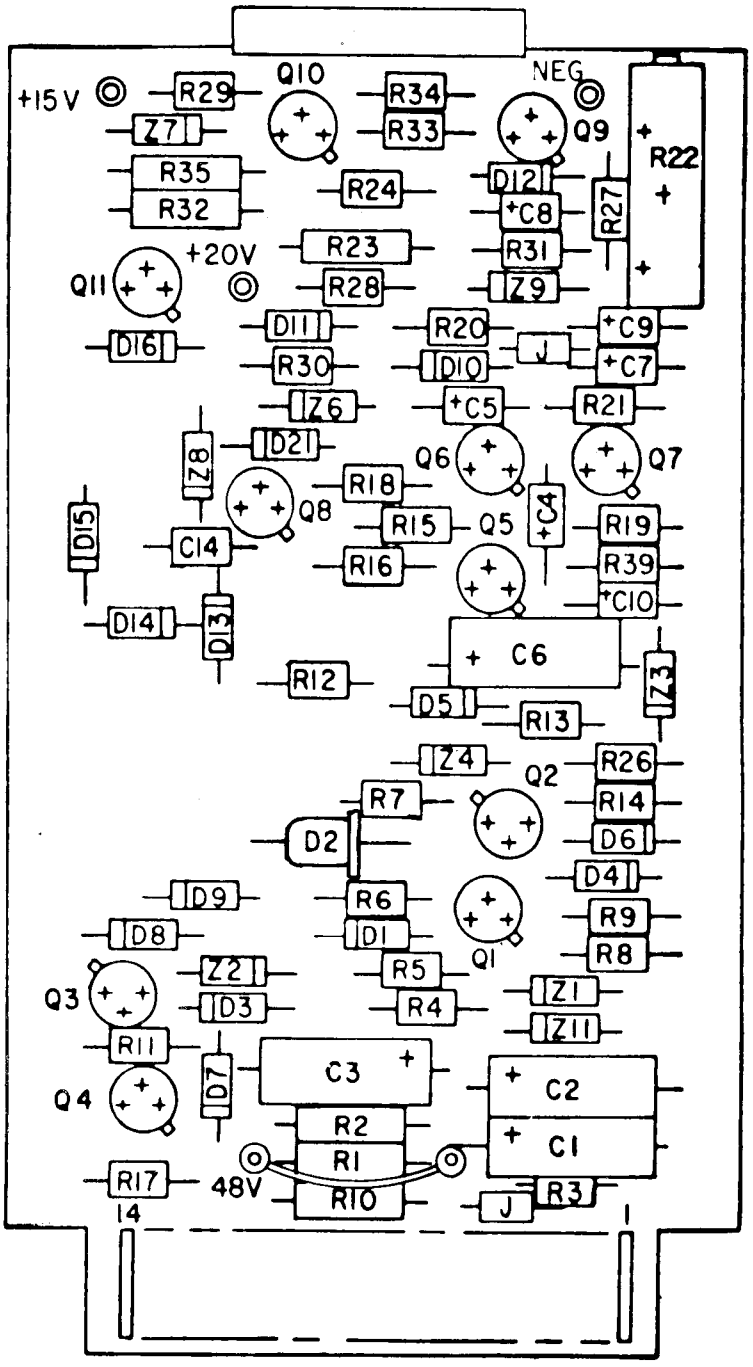


FRONT VIEW
(COVER REMOVED)

BOARD POSITION	BOARD DESCRIPTION
E	POWER SUPPLY
F	SYNCHRONISM
G	LINE BUS
H	LOGIC I
I	COUNTER
J	RESET
K	HS RECLOSE
L	TD RECLOSE
M	INDICATOR
N	LOGIC II
O	

3490A28

Fig. 5 Relay Type SRCU-2 Component Location



880A966

Fig. 6 Power Supply Module Component Location

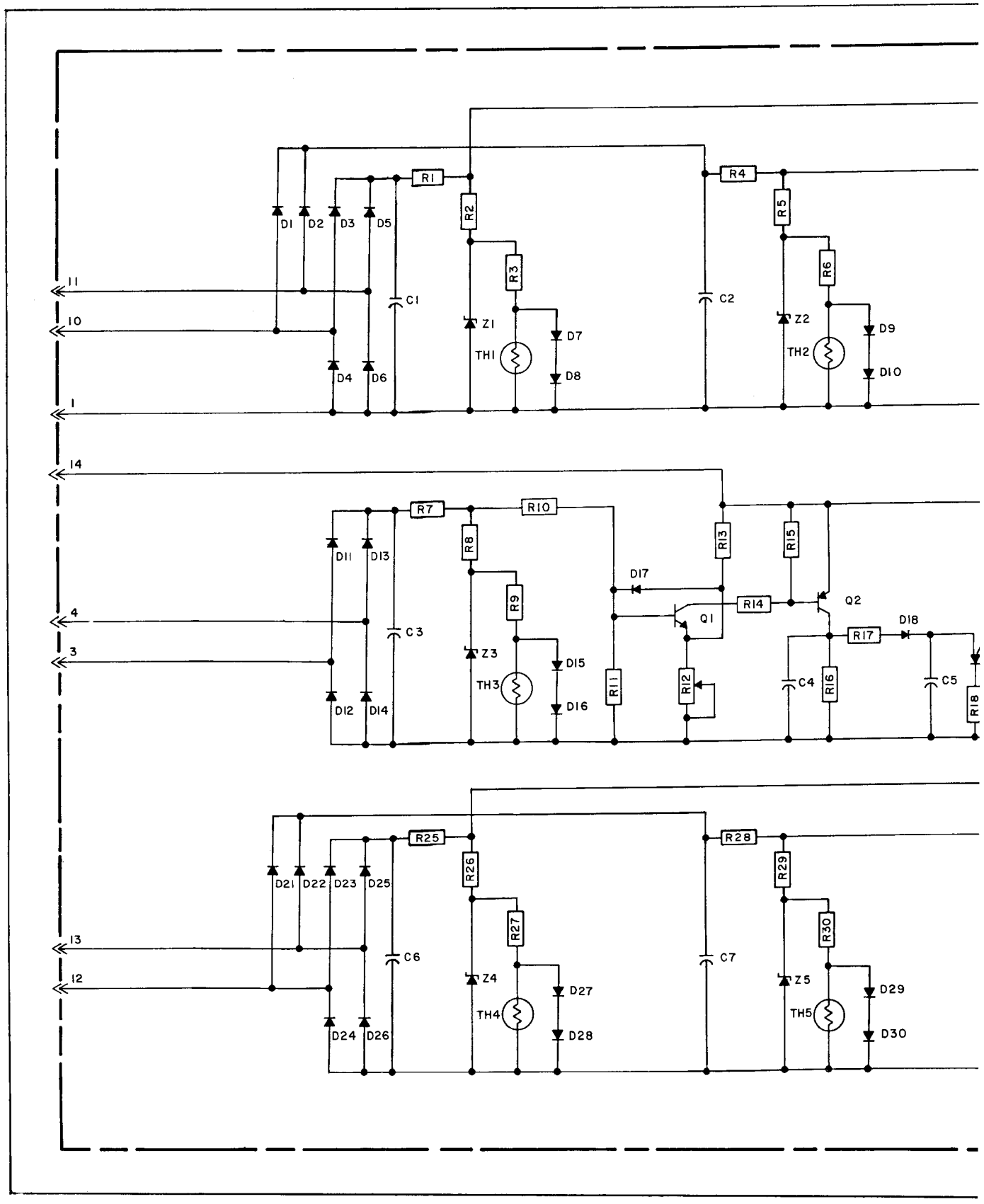
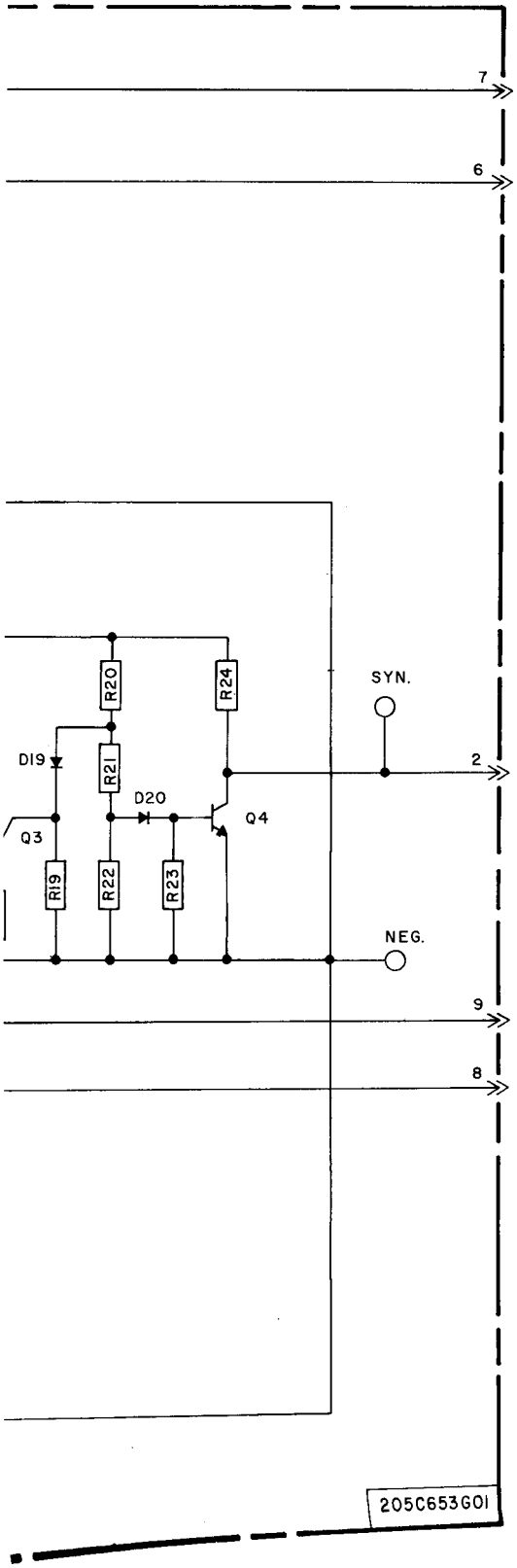


Fig. 8 Synchroni

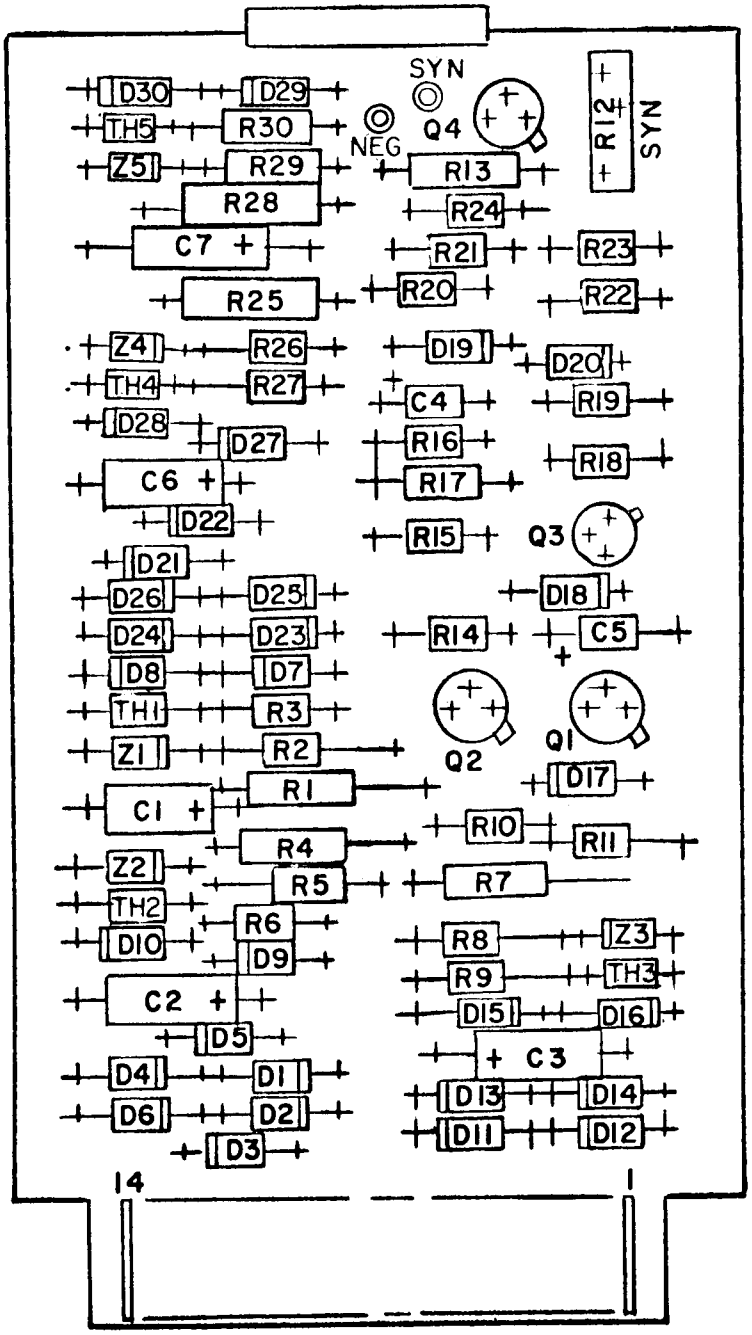


RESISTOR	DESCRIPTION	STYLE NO.
R1-R4-R25-R28	5K 3W ±1%	763A126H24
R2-R5-R8-R26-R29	1.1K 1/2W ±1%	862A376H05
R3-R6-R9-R27-R30	2.49K 1/2W ±1%	862A376H39
R7	5K 5W ±1%	763A130H19
R10	3.32K 1/2W±1%	862A376H51
R11	11K 1/2W ± 1%	848A820H49
R13	3.65K 1/2W ± 1%	862A376H55
R14-R17	5.49K 1/2W ±1%	848A820H20
R15-R23	10K 1/2W ± 2%	629A531H56
R16	12.1K 1/2W ± 1%	848A820H53
R18	100Ω 1/2W ± 2%	629A531H08
R19	1 MEG. 1/2W. ± 5%	184A763H99
R20	100K 1/2W ± 1%	848A821H42
R21-R22	49.9K 1/2W ± 1%	848A821H13
R24	.15 MEG. 1/2W ±2%	629A531H84
POT	DESCRIPTION	STYLE NO.
R12	20K 3/4W ±10%	880A826H01
CAPACITOR	DESCRIPTION	STYLE NO.
C1-C2-C3-C6-C7	.27 MFD. 200V.	188A669H05
C4	4.7 MFD. 35V.	184A661H12
C5	.1 MFD. 200V.	188A669H03
DIODE	DESCRIPTION	STYLE NO.
D1 TO D6-D21 TO D26	1N4818	188A342H06
D11 TO D14	1N4821	188A342H16
D7 TO D10-D15 TO D20-D27 TO D30	1N4148	836A928H06
TRANSISTOR	DESCRIPTION	STYLE NO.
Q1 - Q4	2N2219A	762A672H11
Q3	U13T1	878A289H01
Q2	2N2905A	762A672H10
ZENER DIODE	DESCRIPTION	STYLE NO.
Z1 TO Z5	1N957B	186A797H06
THERMISTOR	DESCRIPTION	STYLE NO.
TH1 TO TH5	10K	185A211H04

COMPONENT LOCATION_____880A997

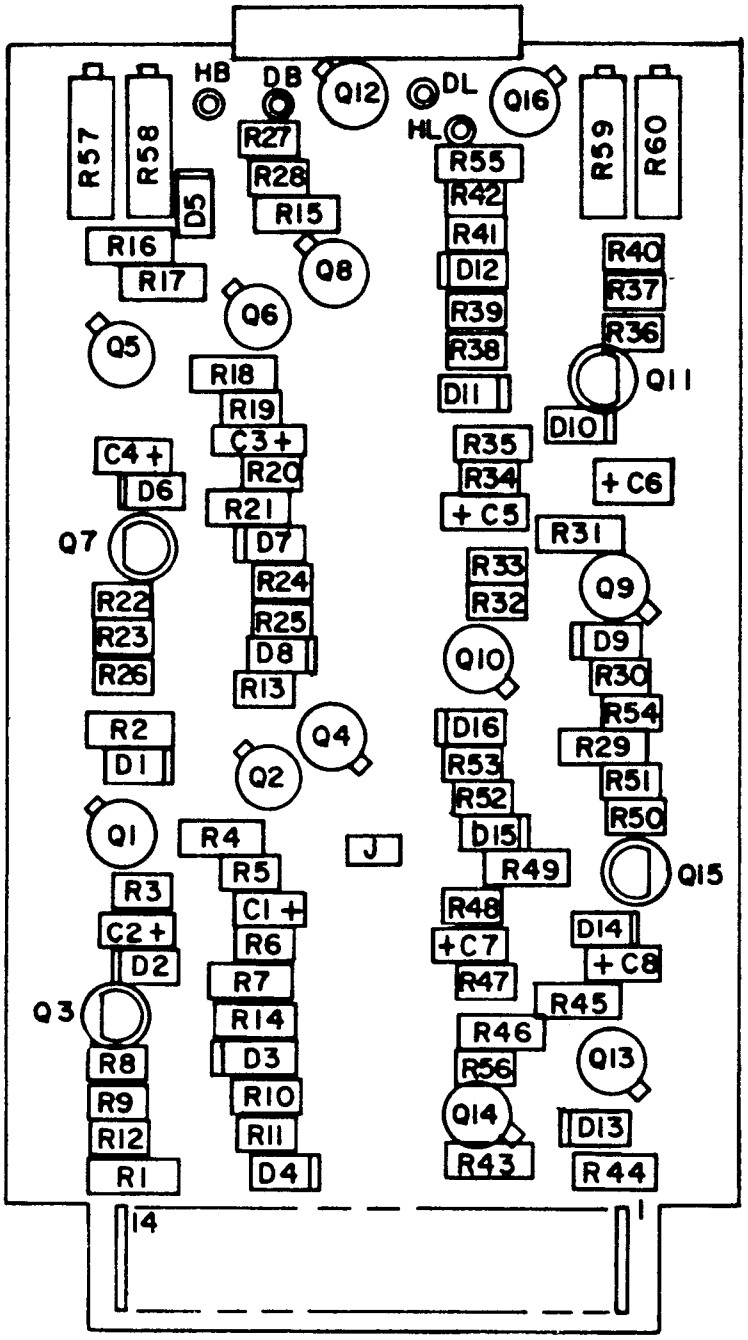
6668D72

:m Module Internal Schematic



880A997

Fig. 9 Synchronism Module Component Location



3501A01

Fig. 10 Line-Bus Module Component Location

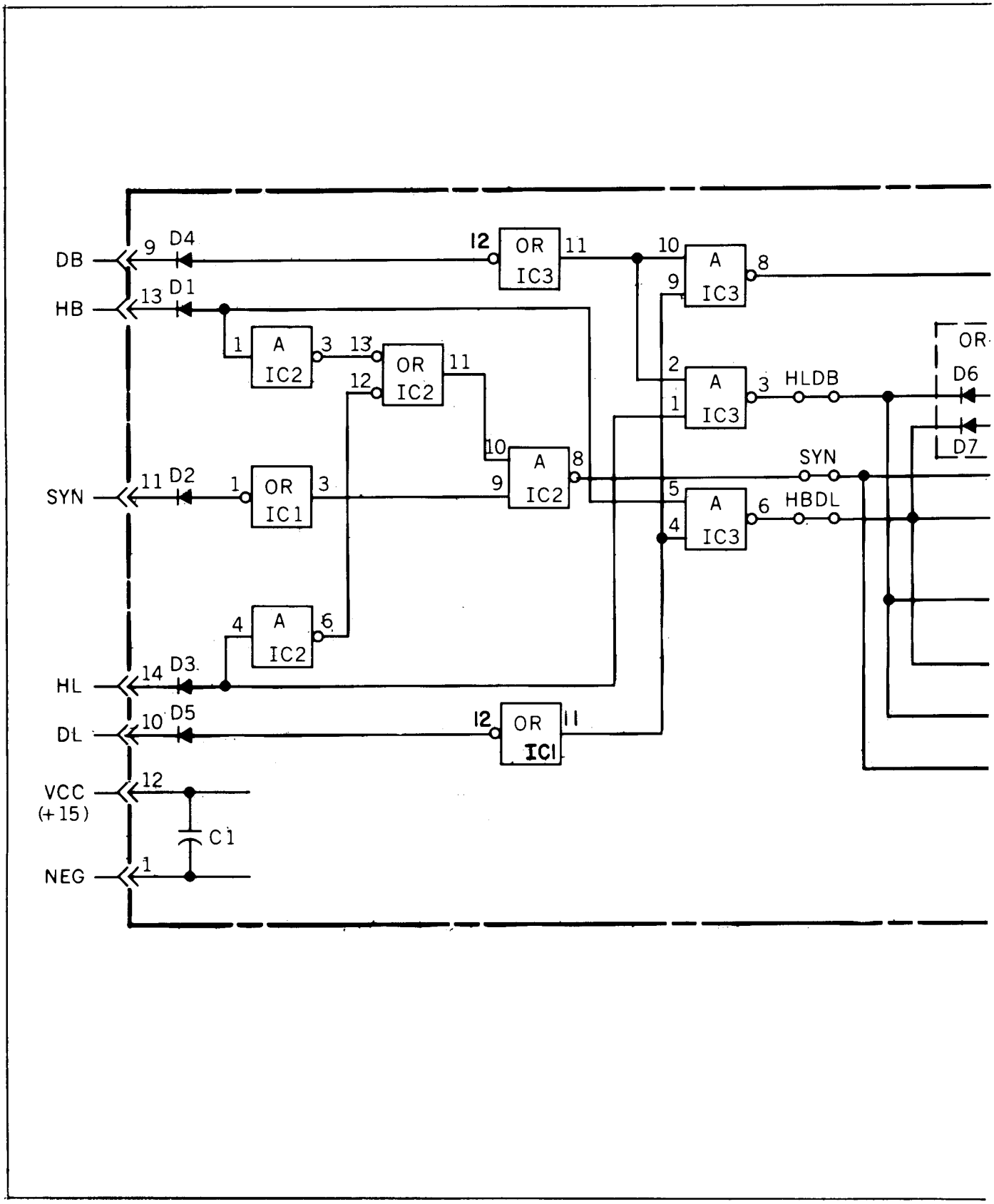
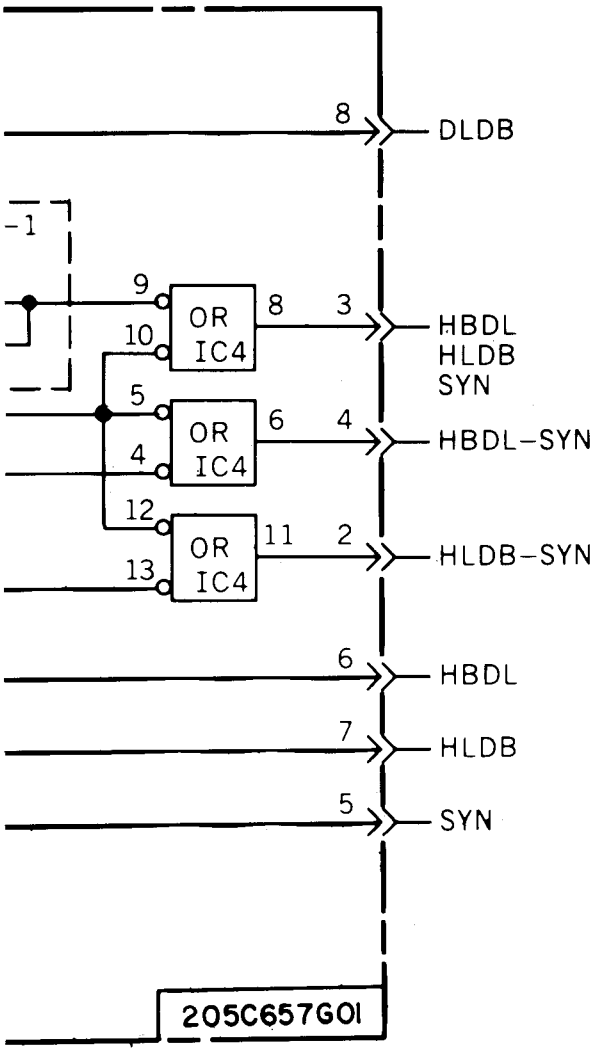


Fig. 12 Logic I



CAPACITOR	DESCRIPTION	STYLE NO.
C1	.47MFD 50V	762A680H04
DIODE	DESCRIPTION	STYLE NO.
D1 TO D7	1N4148	836A928H06
INT. CKT.	DESCRIPTION	STYLE NO.
IC1 TO IC4	MC672L	6296D58H01
JUMPER	**DESCRIPTION**	**STYLE NO.**
LINK	**HLDB-HBDL-SYN**	**3489A69G02**

COMPONENT LOCATION ____880A953

719B917

Module Internal Schematic

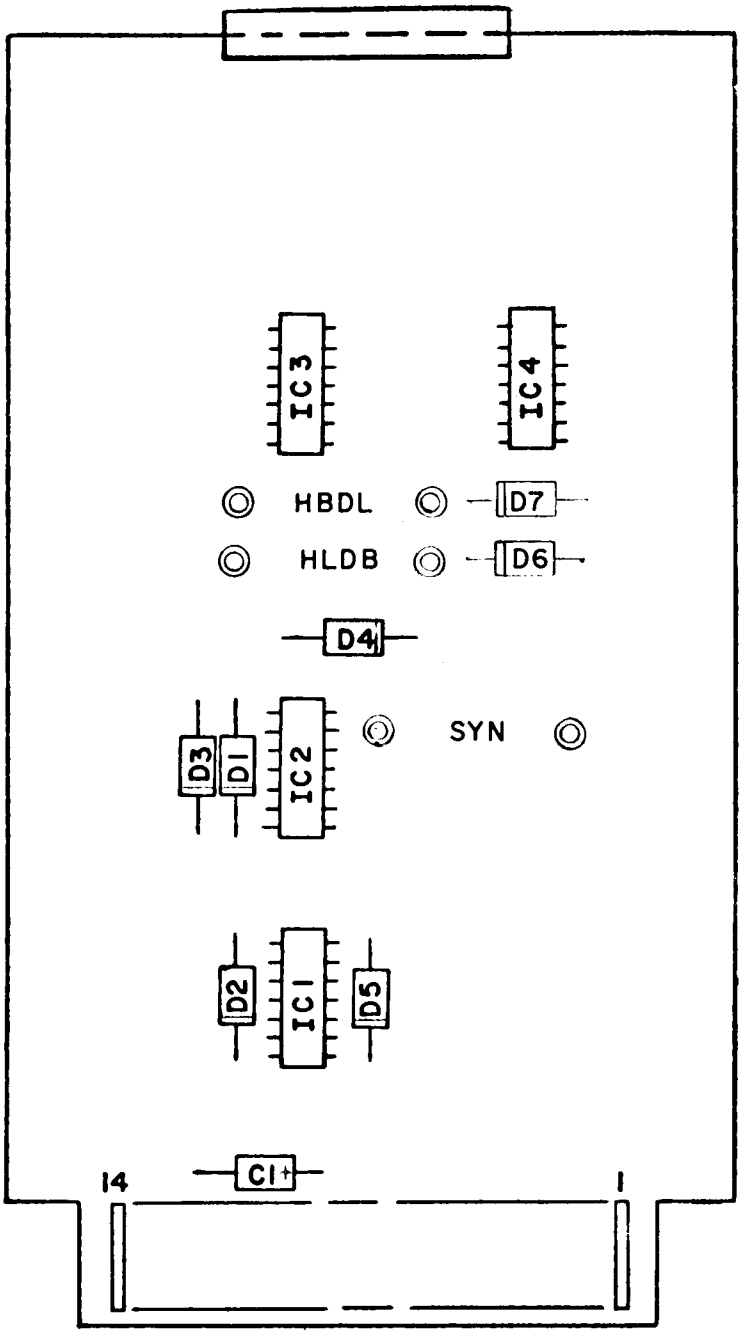


Fig. 13 Logic I Module Component Location

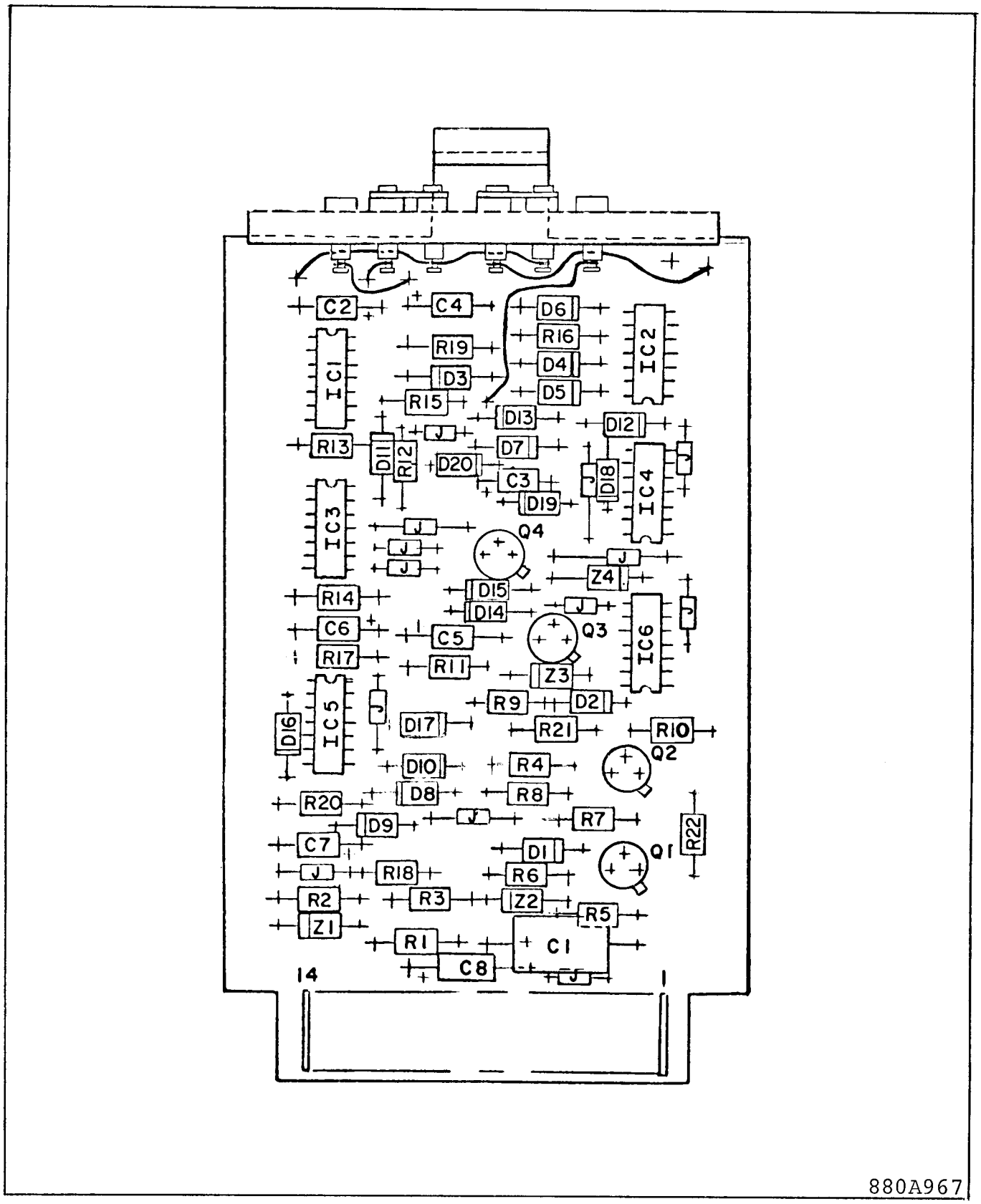


Fig. 14 Counter Module Component Location

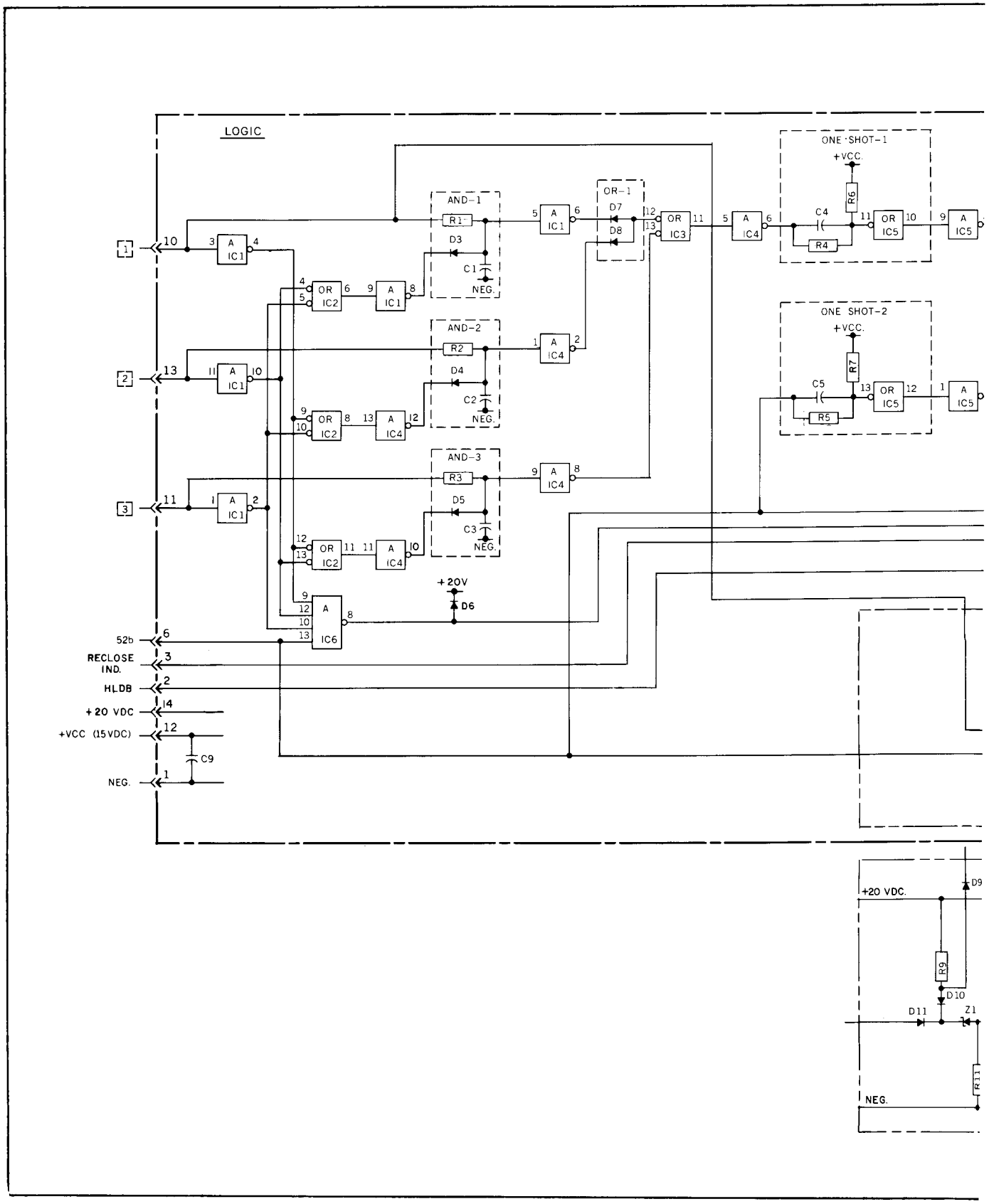
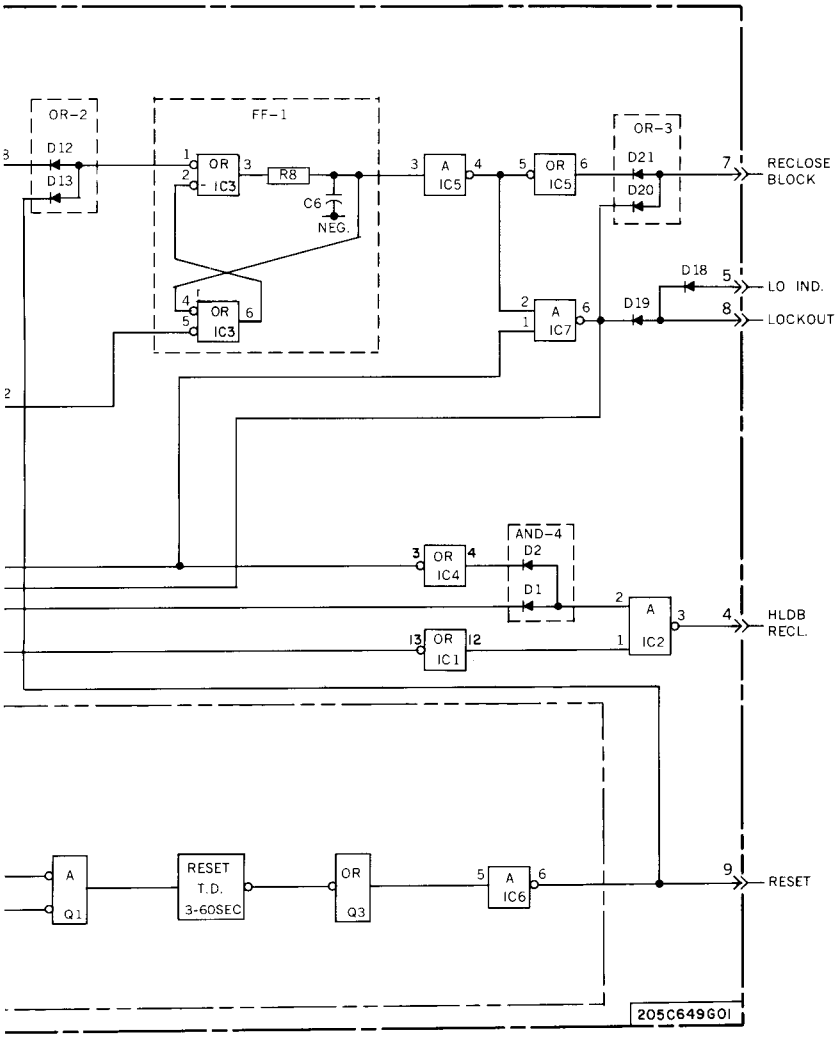
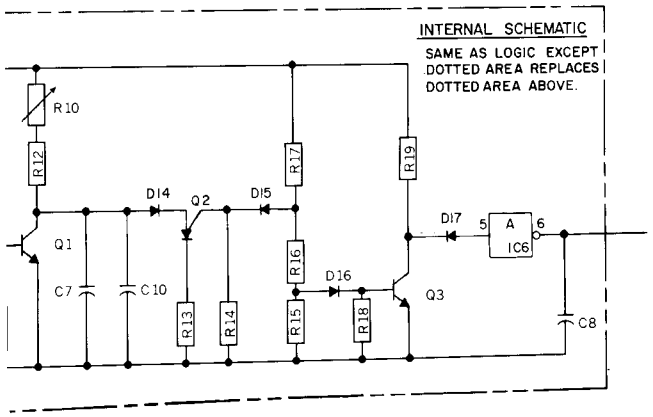


Fig. 16 Reset Mo





RESISTOR	DESCRIPTION	STYLE NO.
R1–R2–R3–R6 R7–R11–R18	10K 1/2W ±5%	184A763H51
R4–R5–R9	20K 1/2W ±5%	184A763H58
R8–R13	100Ω 1/2W ±5%	184A763H03
R12	8.2K 1/2W ±5%	184A763H49
R17	68.1K 1/2W ±1%	848A821H26
R16–R19	82K 1/2W ±2%	629A531H78
R15	100K 1/2W ±2%	629A531H80
R14	1 MEG 1/2W ±5%	184A763H99
R10	250K 1/2W ±10%	862A649H01

CAPACITOR	DESCRIPTION	STYLE NO.
C1–C2–C3	4.7MFD. 35V.	184A661H12
C4–C5	.27MFD. 200V.	849A437H02
C6	.22MFD. 60V.	187A508H22
C7–C10	150MFD. 30V.	849A007H01
C8	.01MFD. 200V.	764A278H10
C9	.47MFD. 50V.	762A680H04

DIODE	DESCRIPTION	STYLE NO.
D1 TO D21	1N4148	836A928H06

TRANSISTOR	DESCRIPTION	STYLE NO.
Q1–Q3	2N2219A	762A672H11
Q2	U13T1	878A289H01

ZENER DIO.	DESCRIPTION	STYLE NO.
Z1	IN960B	186A797H10

INT. CKT.	DESCRIPTION	STYLE NO.
IC2–IC3	MC672L	6296D58H01
IC6–IC7	MC679L	6296D58H02
IC1–IC4	MC680L	6296D58H03

COMPONENT LOCATION _ _ _ 880A969

6668D74

dule Internal Schematic

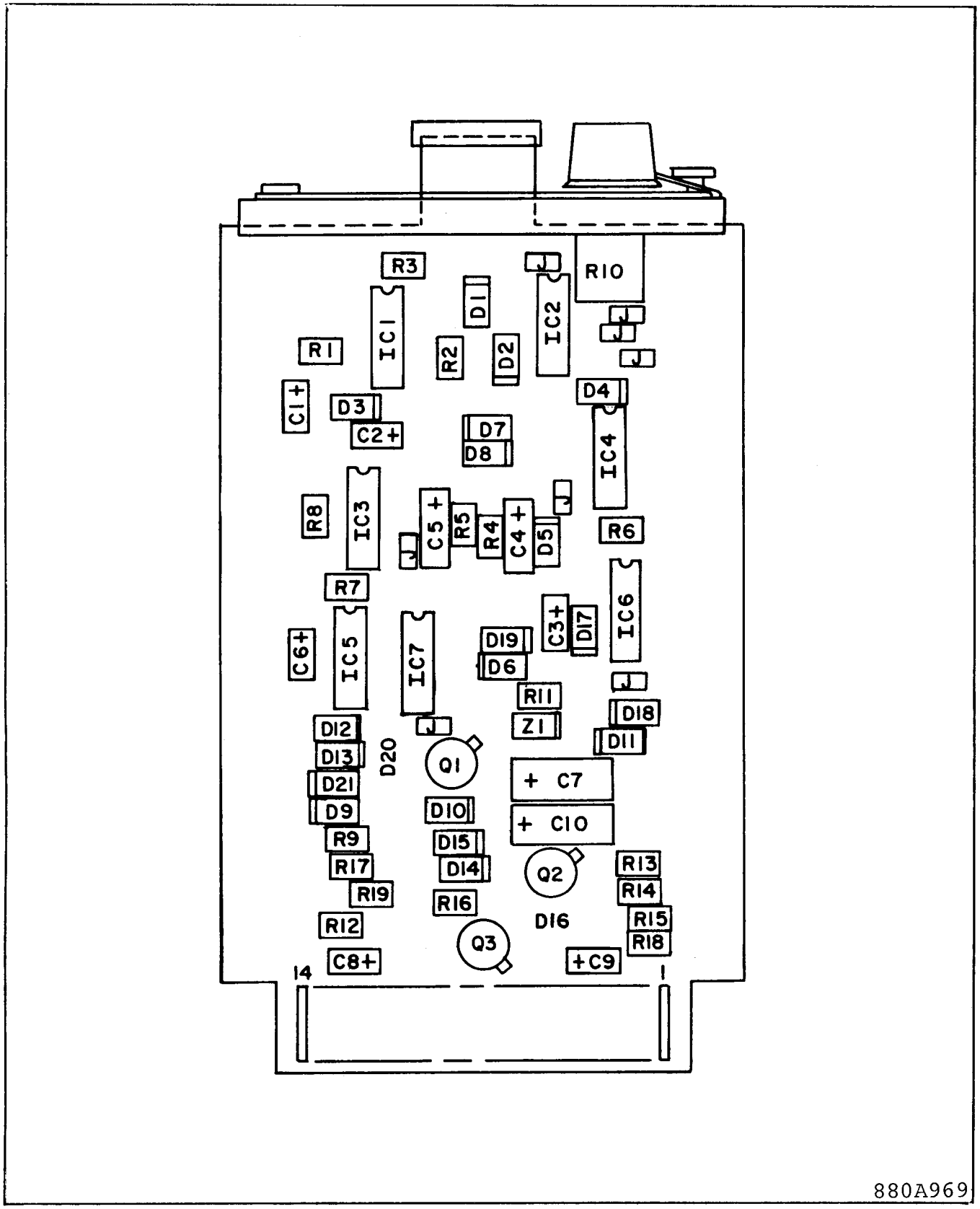
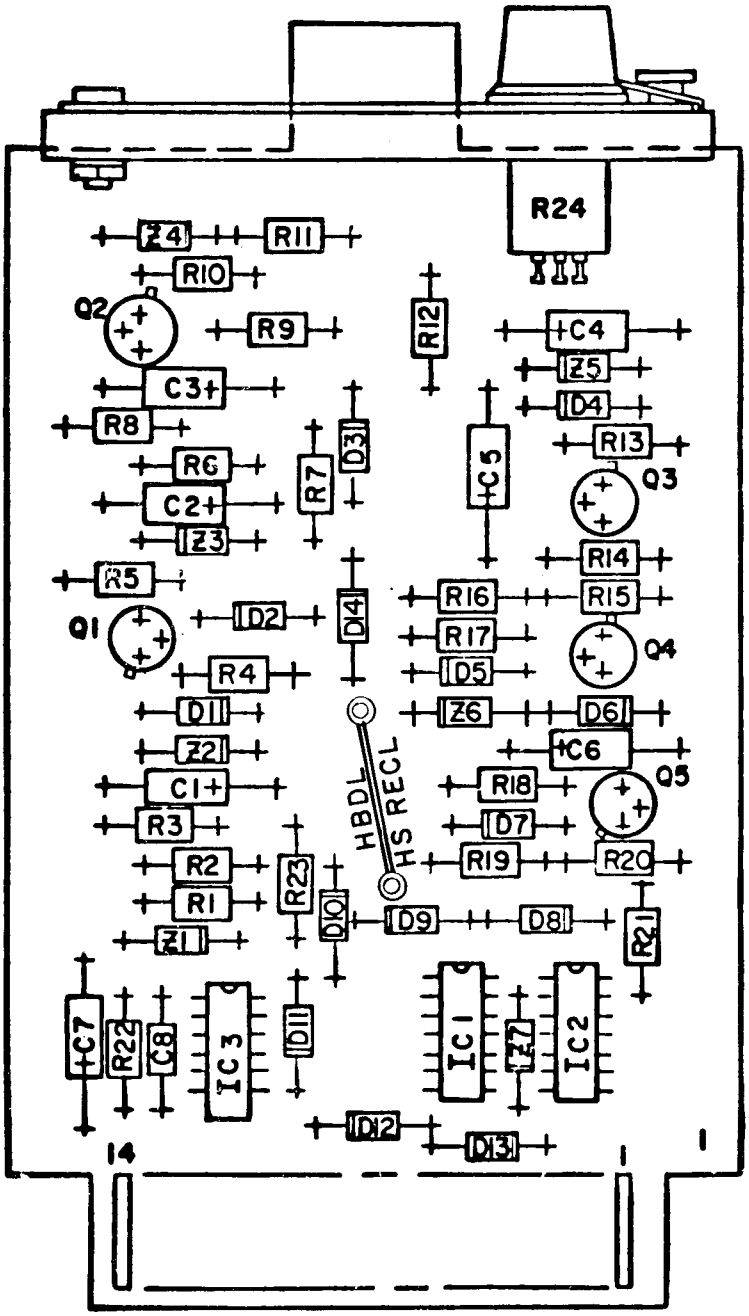
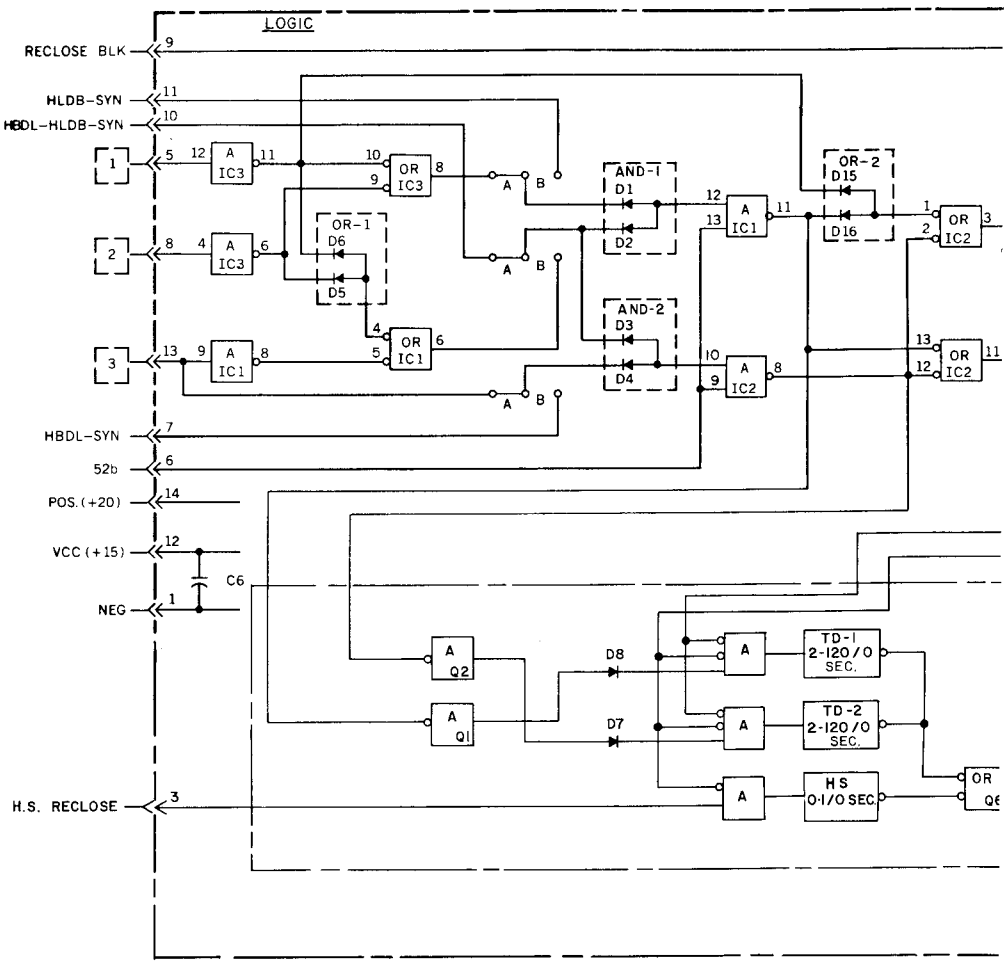


Fig. 17 Reset Module Component Location



3489A39

Fig. 18. High Speed Reclose Module Component Loc.



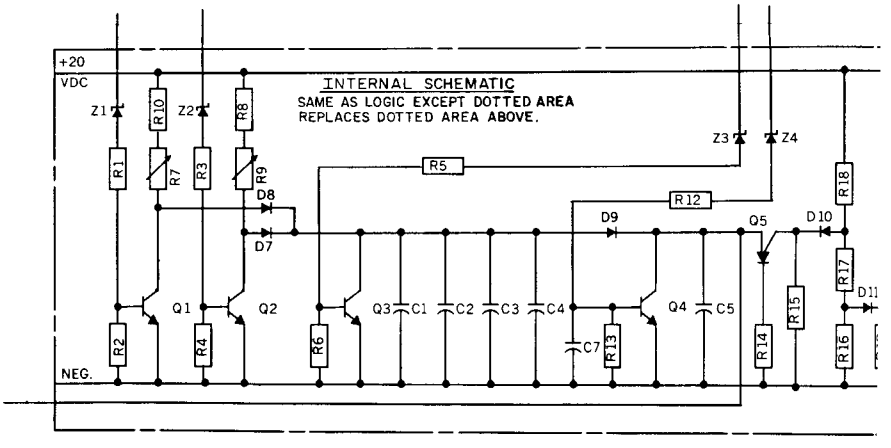
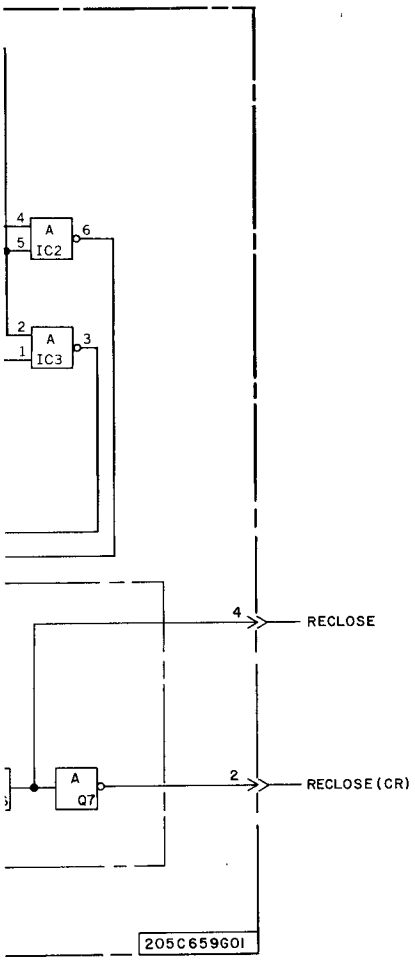
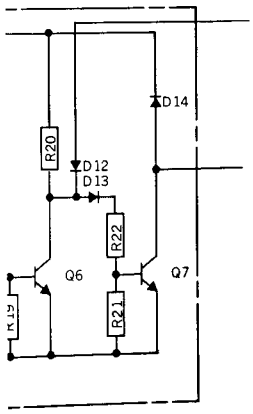


Fig. 20 Time Delay Re





RESISTOR	DESCRIPTION	STYLE NO.
R1-3-5-12	27K 1/2W±2%	629A531H66
R2-4-6-13,21	10K 1/2W±2%	629A531H56
R8-R10	3.3K 1/2W±2%	629A531H44
R14	100Ω 1/2W±2%	629A531H08
R15	1MEG 1/2W±1%	848A822H39
R16	100K 1/2W±2%	629A531H80
R17	90.9K 1/2W±1%	848A821H38
R18	68.1K 1/2W±1%	848A821H26
R19	20K 1/2W±2%	629A531H63
R20	15K 1/2W±2%	629A531H60
R22	30K 1/2W±2%	629A531H67

POT	DESCRIPTION	STYLE NO.
R7-R9	250K 1/2W±10%	862A649H01

CAPACITOR	DESCRIPTION	STYLE NO.
C1 TO C4	150MFD 30V	862A177H05
C5	6.8MFD. 35V	184A661H10
C7	.47MFD 35V	187A508H05
C6	.47MFD 50V	762A680H04

DIODE	DESCRIPTION	STYLE NO.
D1 TO D13 D15-D16	1N4148	836A928H06
D14	1N4818	188A342H06

TRANSISTOR	DESCRIPTION	STYLE NO.
Q1 TO Q4, Q6 Q7	2N2219A	762A672H11
Q5	U13T1	878A289H01

ZENER	DESCRIPTION	STYLE NO.
Z1 TO Z4	1N957B	186A797H06

INT CKT.	DESCRIPTION	STYLE NO.
IC1 TO IC3	MC672L	6296D58H01

JUMPER	DESCRIPTION	STYLE NO.
LINK	A-B	3489A69G01
COMPONENT	0Ω	862A478H01

COMPONENT LOCATION-- 880A940

6668D76

lose Module Internal Schematic

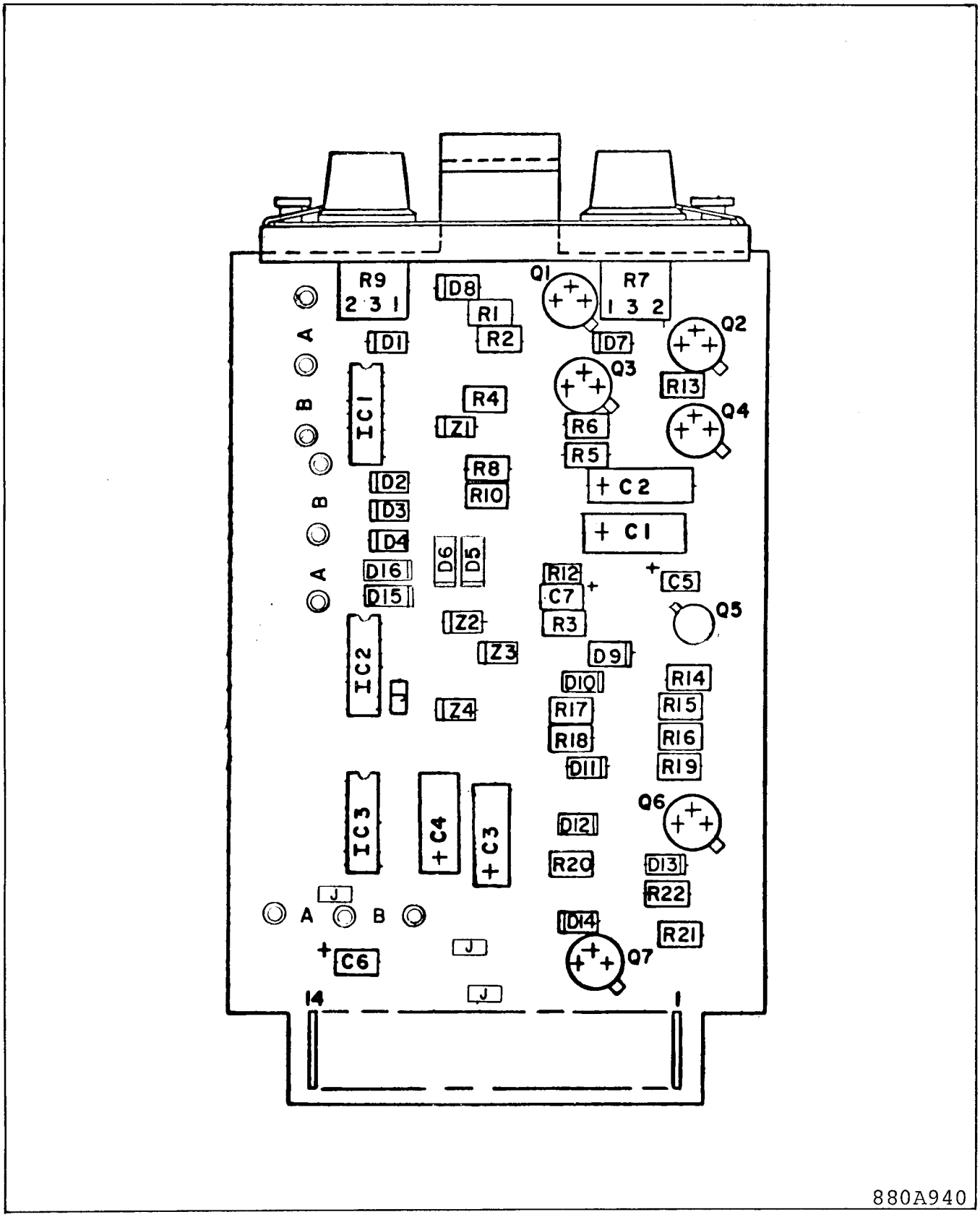
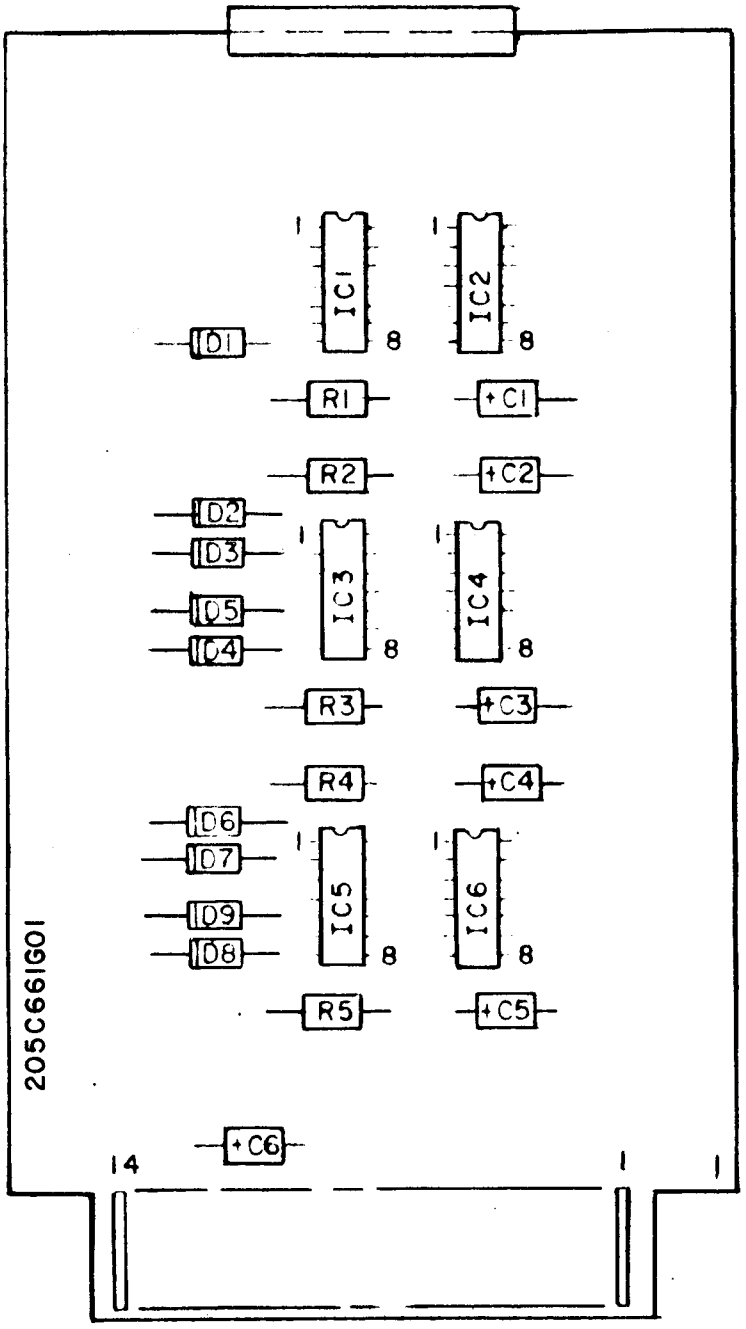


Fig. 21 Time Delay Reclose Module Component Location



880A822

Fig. 22 Indicator Module Component Location

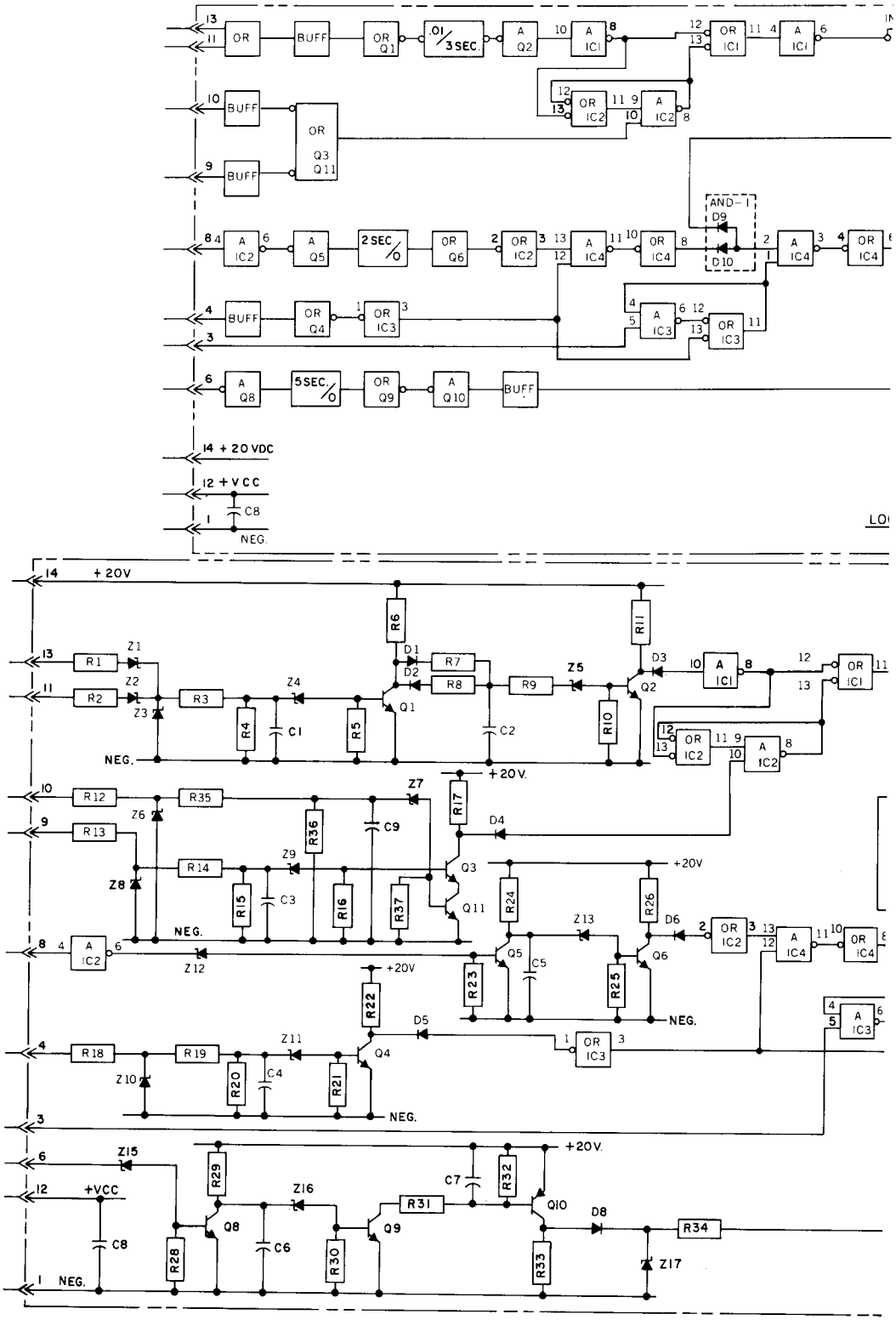
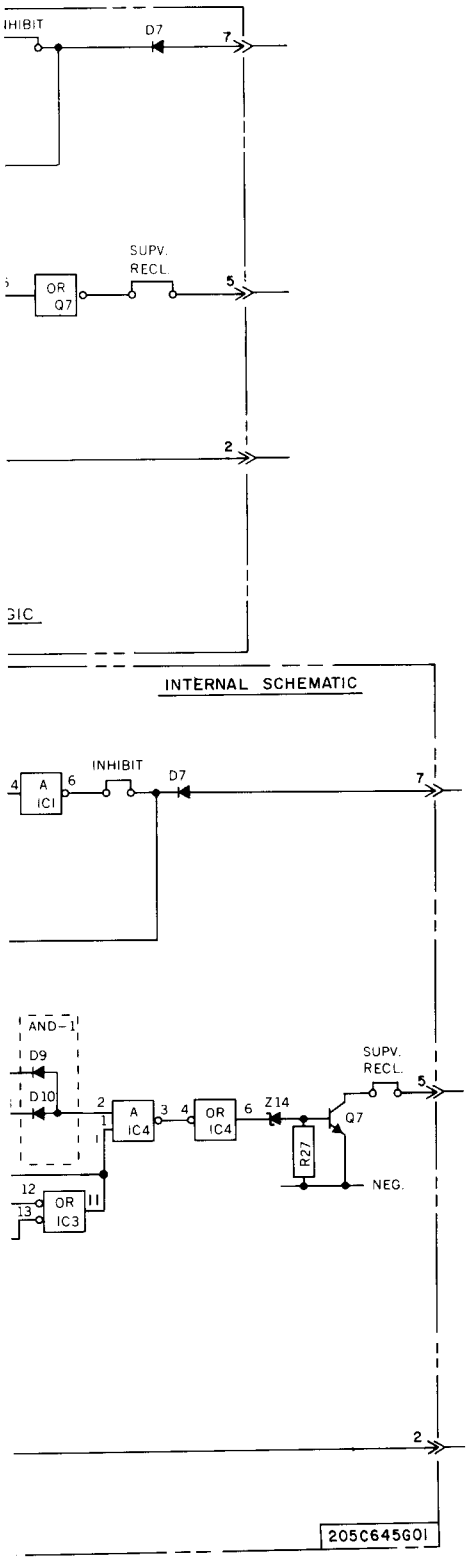


Fig. 24 Logic II Module

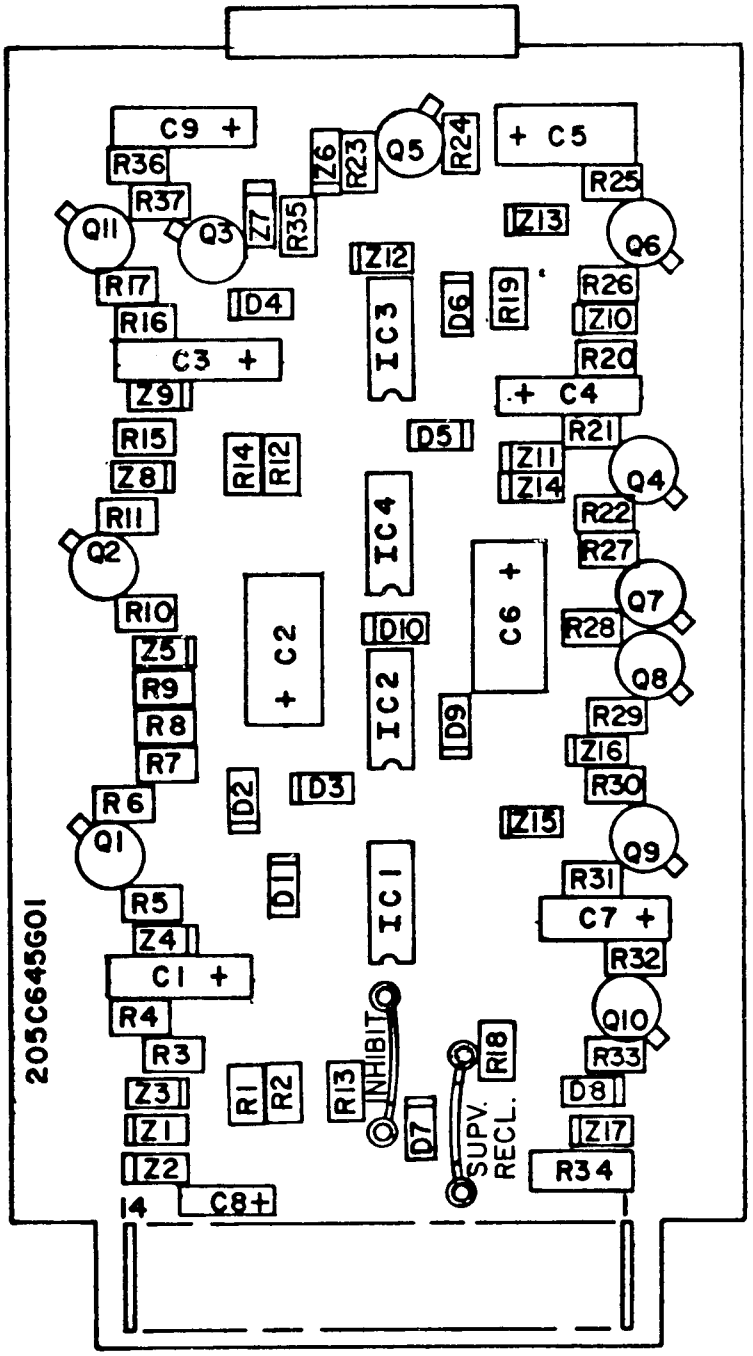


RESISTOR	DESCRIPTION	STYLE NO.
R1-R2-R3-R12-R13-R14-R18-R19-R35	4.7K 1/2W±2%	629A531H48
R4-R11-R15-R17 R20-R22-R26-R33 R36	82K 1/2W±2%	629A531H78
R5-R9-R16-R21 R23-R27-R28-R32 R37	10K 1/2W±2%	629A531H56
R6-R10-R25-R30	20K 1/2W±2%	629A531H63
R24	120K 1/2W±2%	629A531H82
R7	22K 1/2W±2%	629A531H64
R8	300Ω 1/2W±2%	629A531H19
R29	100K 1/2W±2%	629A531H80
R31	6.8K 1/2W±2%	629A531H52
R34	150Ω 3W	762A679H01
CAPACITOR	DESCRIPTION	STYLE NO.
C1-C3-C4-C9	.047MFD. 200V	849A437H04
C5	47MFD. 35V	837A241H22
C2-C6	150MFD. 30V	862A177H05
C7	.27MFD. 200V	188A669H05
C8	.47MFD. 50V	762A680H04
DIODE	DESCRIPTION	STYLE NO.
D1 TO D7-D9-D10	IN4148	836A928H06
D8	IN645A	837A692H03
TRANSISTOR	DESCRIPTION	STYLE NO.
Q1 TO Q9-Q11	2N2219A	762A672H11
Q10	2N2905A	762A672H10
ZENER DIODE	DESCRIPTION	STYLE NO.
Z1-Z2-Z17	IN3688A	862A288H01
Z3-Z6-Z8-Z10	IN3686B	185A212H06
Z4-Z5-Z7-Z9-Z11 TO Z16	IN957B	186A797H06
INT. CKT.	DESCRIPTION	STYLE NO.
IC1 TO IC4	MC672L	6296D58H01
JUMPER	DESCRIPTION	STYLE NO.
LINK	INHIBIT	3489A69G01
LINK	SUPV. RECL.	3489A69G01

COMPONENT LOCATION _____ 880A990

6682D89

(Optional) Internal Schematic



880A990

Fig. 25 Logic II Module (Optional) Component Location

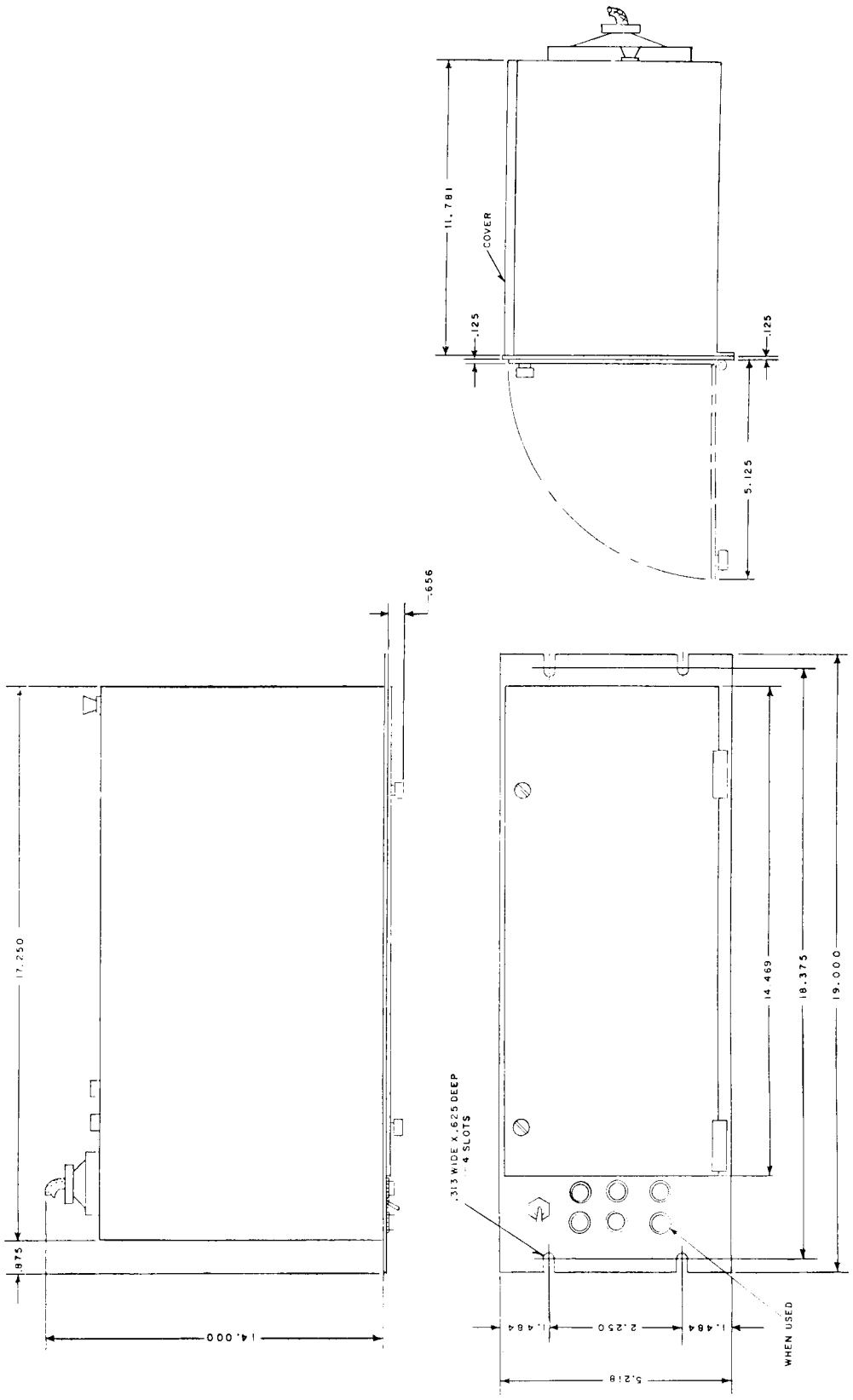


Fig. 28 Outline and Drilling Plan for Type SRCU-2 Relay

WESTINGHOUSE ELECTRIC CORPORATION
RELAY-INSTRUMENT DIVISION **NEWARK, N. J.**
Printed in U.S.A.

INSTALLATION • OPERATION • MAINTENANCE

INSTRUCTIONS

Type SRCU-2 MULTI-SHOT RECLOSING RELAY

CAUTION

It is recommended that the user of this equipment become acquainted with the information in this instruction leaflet before energizing the equipment. Failure to observe this precaution may result in damage to the equipment.

Printed circuit modules should not be removed or inserted while the relay is energized unless specific instructions elsewhere in this instruction leaflet state that such action is permissible. Failure to observe this precaution can result in an undesired output, and can cause component damage.

APPLICATION

The SRCU-2 static relay is intended for 3 shot reclosing applications where synchronism check, HLDB (hot-line-dead bus) and HBDL (hot bus-dead line) control is required. "Hot" and "dead" levels are independent of one another and are adjustable from 3 to 120 volts.

The relay provides the following additional functions:

1. Intermediate lockout – delays the final reclosure until bus and line are hot and synchronism exists.
2. Supervisory close – allows external close control to be supervised by synchronism check, HLDB and HBDL. This control is designed for anti-pump operation.
3. Inhibit – all reclosing is restrained if the inhibit input is present. This input can be energized from such sources as a transfer trip system, indicating remote breaker failure, for example.
4. Indication – lights show the history of the reclosing relay action since last reset, including High Speed Reclose, Synchronism Check Reclose, HLDB or HBDL Reclose.
5. Initiated high speed reclosure – controlled by high speed trip from protective relays. An adjustable delay of 0-1 second is provided.
6. Reclose block input – predominates over reclose initiate input.
7. Independent timing control for each of the two time delayed reclosures.
8. Trip Output – responsive to dead line-dead bus, delayed 5 seconds.
9. Option for setting different times for HLDB and HBDL reclosures using the timers normally committed to second and third shot reclosures.
10. Selectable 1 to 3 shots to lockout.
11. Lockout relay.
12. Lockout on dc application.
13. 3 to 60 second adjustable reset time with calibrated dial.
14. Requires only a single 52b contact for breaker status indication.

CONSTRUCTION

The SRCU-2 relay is mounted on a 19 inch wide panel, 5-1/4 inches high (3 rack units) with edge slots for mounting on a standard relay rack or panel. For the outline and drilling plan, refer to Figure 28.

The photographs in Figures 1 and 2 show the front and rear view of the SRCU-2 relay with the front and rear door respectively open.

All possible contingencies which may arise during installation, operation, or maintenance, and all details and variations of this equipment do not purport to be covered by these instructions. If further information is desired by purchaser regarding his particular installation, operation or maintenance of his equipment, the local Westinghouse Electric Corporation representative should be contacted.

A hinged and removable door on the front of the chassis covers the printed circuit modules. Indicating lights are mounted on the left side of the front panel. A toggle switch is mounted above them to allow a check on the integrity of the lamps and to reset the seal-in indicators. A sealing post, located in the front top center of the relay, may be used to lock and seal the relay when in service.

The rear panel consists of a hinged door which may be opened to gain access to the relay harness wiring, power supply transistor and inductor, the close relay, the lockout relay, and the line and bus potential transformers. In addition, a 32 terminal connector for all SRCU-2 voltage inputs and outputs, and a terminal strip for the close relay current contacts are mounted at the rear right hand side of the chassis.

All of the circuitry suitable for mounting on printed circuit boards is contained in an enclosure behind the front door. The printed circuit modules slide into position in slotted guides at the top and bottom of the enclosure and engage a terminal block at the rear of the compartment. Each module and terminal block are keyed so that they cannot be accidentally inserted into the wrong slot location. The handle mounted on the front end of the module is used for identification, removal, and insertion of module, and acts as a bumper with the front door to prevent the module terminals from becoming disconnected from the terminal block. The modules may be removed for replacement purposes or for use in conjunction with a printed circuit board extender (style number 3494A90G01) which permits access to the module test points and terminals for making measurements while the relay is energized.

Location and title of the modules are shown on the relay component location drawing, Figure 5.

Printed Circuit Modules

Following is a description of all the printed circuit modules used in the SRCU-2 relay. Refer to the functional relay logic shown in Figure 3. The internal schematics associated with the printed modules contain a detailed logic diagram to simplify understanding of the circuitry, and a complete list and description of the components for renewal parts.

For those users not generally acquainted with logic circuit notation or with device symbols of those components used in the SRCU-2 drawings, it is recommended that a copy of Westinghouse instruction leaflet I.L. 41-000.1 entitled "Symbols for Solid state Protective Relaying" be consulted.

A. Power Supply Module ("POWER" - Position E)

Schematic diagram Figure 7

Component location Figure 6.

The power supply printed circuit module, in conjunction with the few parts mounted in the rear of chassis due to size or heat dissipation, provides the two regulated dc supply voltages required by the SRCU-2. The supply is of the switching regulator design giving high efficiency and relative insensitivity to input voltage. This allows the supply to operate over an input range of 42 to 140 volts dc without any power supply alterations, which is a distinctive feature.

The supply has two outputs; +20 volts for most relay functions, and +15 volts for the integrated circuits and most logic functions. The +20 volt supply is powered directly from the switching regulator, while the +15 volt supply is derived from the +20 volt supply and incorporates "snap turn-on" circuitry to insure the proper initial turn on states of the integrated circuits.

Built into both outputs to provide greater security are non-destructive overvoltage and overcurrent protection circuits, which, if activated (i.e. supply output is shorted) immediately shut the supply down.

A more detailed look at the power supply circuitry is as follows:

The switching regulator of the supply consists basically of chassis mounted switching transistor Q1 (c), and inductor L1 (c), and module components capacitor C6, diode D2, and voltage comparator and driver transistors Q5, Q6, Q2, Q1, Q3 and Q4.

Transistor Q1 (c) is used as a switch, either off or full on. When the voltage comparator and driver transistors switch Q1 (c) on, diode D2 is reversed biased and input voltage is applied

to inductor L1 (c). The current through L1 (c) increases at the rate

$$\frac{di}{dt} = \frac{(\text{V input} - \text{V capacitor C6})}{\text{L1 (c)}}$$

When the voltage on capacitor C6 charges to 20 volts the voltage comparator, consisting of Q5 and Q6 in a differential amplifier arrangement, turns transistor Q1 (c) off through driver transistors Q2, Q1, Q3 and Q4.

At this point with Q1 (c) off, the current continues to flow through inductor L1 (c) and the voltage across L1 (c) reverses polarity, forward biasing diode D2.

During this time, the voltage across L1 (c) is clamped at the voltage $V_{C6} + V_{D2}$ (fwd.) and the current in the inductor decreases at the rate

$$\frac{di}{dt} = \frac{(V_{C6} + V_{D2}\ (\text{fwd.}))}{\text{L1 (c)}}$$

When the current in L1 (c) falls below the load current required of the +20 volt supply, capacitor C6 starts discharging, decreasing V_{C6} until it falls below the 20 volt level set by the 20 turn potentiometer R_{22} in the voltage comparator. Transistor Q1 (c) is again turned on and the cycle is repeated. The circuit is designed such that Q1 (c) switches at a rate of about 22kHz. to 35kHz. to keep the ripple relatively small and capacitor C6 relatively fully charged.

The +15 volt supply is of the zener regulator type design and is derived from the +20 volt supply. It consists mainly of zener diode Z7, series dropdown resistors R23 and R35, filter capacitor C8, and the "snap turn on" circuitry of R24, C9, Z9, Q9, and Q10.

This "snap turn on" circuitry, which insures the proper turn on states of the integrated circuits, operates by sensing the voltage on the 20 volt supply through Z9 and Q9. It is slightly delayed by the RC combination of R24 and C9 and insures that the 20 volt supply is fully present before turning on series transistor Q10, and thereby the +15 volt supply.

Overcurrent protection is provided on the 20 volt output by the circuit consisting of R30, Q8, D11 and R28. This circuit operates when the current passing through R30 is sufficiently large enough (approx. 1 amp.) to cause an IR drop of enough voltage. (.7 volt) to turn on Q8, and thereby charge up capacitor C10. The combination of C10, R39, and D12 form the common discriminator circuit for all overcurrent and overvoltage inputs. When an input is sufficiently large to overcome the effects of shunting resistor R39, and charge capacitor C10 to approximately 1.4 volts to provide base drive to Q7, the switching supply is immediately shut down. This is accomplished by Q7 shorting the reference side of the voltage comparator differential amplifier to zero, thereby causing switching transistor Q1 (c) to turn off, allowing all outputs to drop to "0" volts.

Overcurrent protection (.5 amp.) is provided in the +15 volt output in a similar manner through the combination of R32, Q11 and D16.

Overvoltage protection in the +20 volt output is accomplished by Z6 and D21. If the 20 volt output exceeds the breakdown voltage of Z6 and D21, capacitor G10 in the common discriminator circuit charges and causes the supply to shut down as previously described.

Overvoltage protection of the +15 volt output is accomplished in a similar manner through Z8, D13, D14 and D15.

Restart of the switching supply requires the dc input voltage to be removed and reapplied. This is to allow start up circuitry capacitor C3 to discharge through R3 (approx. 0.8 second.) Upon reapplication of the input voltage, the charging R4 and C3 combination applies a voltage pulse, limited by Z1 to 20 volts, through diode D1 to the voltage comparator. This is sufficient to power the comparator and drive circuitry until the 20V. supply comes on and takes over through diode D10.

Reverse voltage protection to the power supply from accidental reverse application of the input voltage (station battery) to the SRCU-2 is provided by zener diode Z11. This zener, in series with the input to the module, blocks any

reverse voltage and only allows the supply to be energized if voltage polarity is applied to forward bias zener Z11.

Also contained on this module is the buffer resistor-capacitor combination for the 8/0 millisecond anti-bounce timer for the 52b contact input. A "48V" link is provided on this module for 48 volt operation of the relay, and should be removed for 125 volt operation. The function of this 48V link is to bypass the 125V series resistor R1 in the 8/0 millisecond timer buffer to allow the appropriate RC combination for 48 or 125 volt operation.

B. Synchronism Module ("SYNCHRONISM" – Position F)

Schematic Diagram Figure 8

Component location Figure 9

The synchronism printed circuit module contains the adjustable synchronism detector circuitry which responds to the phasing voltage between the bus and line potential transformers. A voltage difference signal between the transformers is full wave rectified by diodes D11 through D14, and applied to the base of transistor Q1 through a voltage divider network of resistor R7, R10, and R11. If this signal is greater than the voltage set on the emitter of Q1 by the voltage divider consisting of resistor R13 and 20 turn potentiometer R12, Q1 will turn on (phasing voltage is outside the set circle). The nonlinear attenuator on the input divider consisting of R8 and Z3, (and R9, TH-3, D15 and D16 for temperature stability) allow the 5 to 120 volt phasing voltage setting on the 20 turn potentiometer R12, to be uniformly sensitive over the complete range of 5 to 120 volts. This trimpot is located on the front of the module for ease of adjustment.

While the turn on of Q1, transistor Q2 turns on and applies a relative signal from the 20V dc supply into the level discriminator consisting of C4, R16, R17, D18, C5, and the circuitry associated with programmable unijunction transistor Q3. If this signal from Q2 is large enough (voltage/time) to charge capacitor C5 up to the firing voltage of Q3, Q3 fires and shorts the base drive from transistor Q4 turning it off to give a logic "1" SYN signal on module terminal 2. PUT Q3 remains latched on as long as the input signal remains sufficiently large. Once the signal drops below the setting, Q3 resets itself, allowing Q4 to turn on for a logic "0" SYN signal (phasing voltage is inside the set circle).

Typical phase-voltage curves for the SRCU-2 are shown in Figure 26.

This module also contains the rectifier and attenuator circuitry for the bus and line detectors where the respective signals from the bus and line potential transformers are full wave rectified and attenuated through respective nonlinear attenuators in the manner previously described. These signals are then sent to the HB, DB, HL and DL voltage detectors on the Line-Bus module.

C. Line-Bus Module ("LINE-BUS" – Position G)

Schematic diagram Figure 11.

Component location Figure 10.

The line-bus printed circuit module contains the 3 to 120 volt adjustable line and bus detectors circuitry. The attenuated line and bus signals from the synchronism module are compared to the corresponding settings on the four 20-turn potentiometers located at the front of the module for ease of adjustment. The four signals are then each treated in the same manner previously described for the circuitry on the synchronism module to arrive at the four output HB, DB, HL and DL. Each of the four levels can be individually set from 3 to 120 volts on its corresponding potentiometer. Individual test points are provided at the front of the module with a logic "0" reading indicating an input signal below the set point. These signals are then set to the Logic I module.

D. Logic I Module (LOGIC I" – Position H)

Schematic diagram Figure 12.

Component location Figure 13.

The logic I printed circuit module contains the corresponding logic circuitry to generate the

reclose supervisory functions SYN, HBDL, and HLDB, from synchronism, line and bus signals. Both time delayed reclosures are supervised by these three functions: that is, one of these functions must be present (within its setting) for the time delayed reclosures to take effect. Optional deletion of supervision of any of these functions can be accomplished by removal of corresponding programmable link on this module.

E. Counter Module ("COUNTER" – Position I)

Schematic diagram Figure 15.

Component location Figure 14.

The counter printed circuit module contains an 8/0 millisecond anti-bounce timer for the 52b contact input, and a NAND gate integrated circuit 4 step sequential counter. This counter responds to signals from the 52b contact, the HS reclose module, and the reset module, and sequences the SRCU-2 through its present functions. An operation to lockout selector link and the intermediate lockout selector link are located on the front panel of this module. By moving the adjustable link to the desired tap on the operations to lockout selector the SRCU-2 relay can be set to lockout the breaker after 1, 2, or 3 reclosing operations. The intermediate lockout option (lockout of SRCU-2 relay at one time delay reclosure less than the operations to lockout setting, 2nd or 3rd, depending upon tap setting) allows the last reclosure to occur for a synchronism condition only. This may be set by moving the link to the ON tap on the intermediate lockout selector.

F. Reset Module ("RESET" – Position J)

Schematic diagram Figure 16.

Component location Figure 17.

The reset printed circuit module contains the reset timer and circuitry which resets all elements, except the indicating lights, in the adjustable time of 3 to 60 seconds after the breaker remains closed. A calibrated dial is provided on the front panel of the module for ease of adjustment. The reset timer utilizes a programmable unjunction transistor circuit for range and accuracy. When the AND circuit associated with transistor Q1 is satisfied with both the breaker being closed (52b) and the counter having sequenced from the [1] position, the timer capacitors C7 and C10 are allowed to charge through potentiometer R10 and resistor R12. When the voltage on these capacitors reaches the firing level of Q2 (which is set by the voltage division on R15, R16 and R17), Q2 fires shorting the base drive to Q3, thereby causing it to turn off. This in turn allows the gate of IC6 to change state generating a logic "0" reset signal from module terminal 9.

This module also contains the sequence check circuitry which checks for any discrepancy of breaker operations (through the 52b contact) versus relay operation settings. This prevents pumping of the breaker by the SRCU-2 by blocking all reclosing in the relay if any discrepancy occurs. This locks the relay out upon the opening of the breaker.

The lockout circuitry is also contained on this module. It locks the SRCU-2 out, preventing further reclose operations after all desired set operations have occurred. In this lockout state the lockout relay is energized and a signal is sent to the indicator module to energize the lockout indicator.

G. High Speed Reclose Module ("HS RECL" – Position K)

Schematic diagram Figure 19.

Component location Figure 18.

The high speed reclose printed circuit module contains the control and adjustment circuitry for the high speed reclose timer. A 0-1 second calibrated dial is provided on the front panel of the module for ease of adjustment.

The high speed timer is controlled by a buffered H.S. initiate (permit) signal and a buffered H.S. block signal. The H.S. initiate signal from dc positive seals in after 8 milliseconds; the block signal prevents high speed reclosure, predominates over the initiate signal, and has a 60 millisecond override dropout timer for security.

The high speed reclosure is also supervised by the counter module in that it allows only the first reclosure to be a high speed reclosure. Optional supervision by a hot bus-dead line condition can be provided through the HBDL RECL programmable link on the circuit module. Removal of this link removes this option.

H. Time Delay Reclose Module ("TD RECL" – Position L)

Schematic diagram Figure 20.

Component location Figure 21.

The time delay reclose printed circuit module contains the dual 2-120 second adjustable reclose delay timers. A separate TD-1 calibrated dial and a TD-2 calibrated dial are provided on the front panel of the module for ease in adjustment of setting. The TD timers are controlled by signals from the counter and the logic I modules. The timer circuitry utilizes a programmable unijunction transistor (Q5) circuit for range and accuracy, which functions in a manner similar to that of the reset timer previously described. Both TD timers utilize the same timing capacitors and P.U.T. circuitry for scheme simplicity. The different time settings for TD-1 and TD-2 are achieved by switching a different calibrated potentiometer (R7 and R9) into the circuit for the two delays. This allows the TD-1 and TD-2 timers to be utilized to time the first and second time-delayed reclosures based on breaker operation or to be utilized to time a HLDB reclosure on the TD-1 timer and a HBDL reclosure on the TD-2 timer. This is accomplished by setting the three programmable links located on this module. When these links are set in the "A" position the TD timers follow breaker operation. When set in the "B" position the TD timers respond to bus and line conditions. These reclosures may be all HBDL, or all HLDB, or a selection of both, depending upon line and bus status.

I. Indicator Module ("INDICATOR" - Position M)

Schematic diagram Figure 23.

Component location Figure 22.

The indicator printed circuit module contains the integrated circuit logic and driver circuitry for the functional indicators mounted on the front panel of the relay. The logic allows the indicator to show a history of relay operations. The indicators are reset through the logic by the test-reset switch on the front panel of the relay. When operated from the center position to either the test or the reset position this switch generates a logic "0" to cause the indicator logic to function, respectively checking on the integrity of the lamps or resetting of the seal-in indicators.

J. Logic II Module ("LOGIC II" Position N) – Optional

Schematic diagram Figure 24.

Component location Figure 25.

The Logic II printed circuit module contains a supervisory close function which overrides lockout to provide one additional reclosure. This buffered input activates logic circuitry to directly operate the close relay if either synchronism or either of the two line-bus conditions have been satisfied for greater than two seconds. This function is anti-pump and provides only one additional reclosure. It is released by removal of the supervisory close input. This function can be optionally deleted by removal of the SUPV. RECL. programmable link on this printed circuit module.

Also contained on this module is an inhibit function which will block all reclosing in the relay. There are four buffered inputs, two for channel trip and two for loss of channel, which activate the logic circuitry contained for this function.

Inhibit, which is delayed by 10 milliseconds and released 3 seconds after removal of the transfer trip signal, prevents reclosing during transfer trip even if both channels are lost. Inhibit will not occur if loss of channel is not preceded by a channel trip signal. This function can be optionally deleted by removal of the INHIBIT programmable link on this module.

The circuitry for a dead-line, dead-bus voltage output is also contained on this module. It provides a 20 volt dc signal after a DLDB condition has existed for a 5 second duration. This buffered output will then remain until reset by loss of the DLDB condition.

Line and Bus Potential Transformers

The line and bus potential transformers, which provide dc isolation, are located in the rear section of the chassis. Each is a 2:1:1 stepdown voltage transformer with a grounded static shield. One secondary from each transformer supplies information to the line and bus associated circuitry, and the other supplies information to the synchronism circuitry.

Close Relay

The operation of the close relay is controlled by the reclose circuitry on the T.D. Reclose module and the supervisory close circuitry on the Logic II module. Two normally open CR contacts are available.

Lockout Relay

The operation of the lockout relay is controlled by the operations to lockout and intermediate lockout circuitry on the Counter module and the sequence check and lockout circuitry on the Reset module. Two "form C" LR contacts are available. The lockout relay is energized when the SRCU-2 is in the lockout state (after sequencing with no successful reclosures), in the intermediate lockout state, and if the counter should fail to sequence in response to the 52b contact as detected by the sequence check circuitry.

Indicating Lights

The indicating lights are mounted on the front panel of the SRCU-2 relay and consist of one red power indicator and five amber functional indicators. The power indicator indicates the presence of the 20 volt d.c. regulated supply which powers the relay (15 volt d.c. integrated circuit supply is derived from the 20 volt supply). The functional indicators (High Speed Reclose, Hot-Line, Dead-Bus Reclose, Hot-Bus, Dead-Line Reclose, Synchronism Reclose, and Lockout) seal in, and can be tested and reset by the Test-Reset toggle switch.

Test-Reset Switch

The test-reset switch, mounted on the front panel of the SRCU-2 relay, is used to reset and test the functional indicators without disrupting any relay functions.

Internal Reclose Lockout Switch

The internal reclose lockout switch, mounted on an internal panel accessible with the door open, has a contact in series with each of the close relay contacts. When in the OFF position the contacts are open and the close relay contacts are prevented from performing the close function.

Bus-Line Potential Transformer Test Jacks

The bus-line potential transformer test jacks are wired directly to the bus and line potential transformer inputs. Polarity is shown by the use of red and black test jacks. These are accessible from the front of the relay with the door open, which facilitates monitoring and testing.

Theory Of Operation

The basic operation of the SRCU-2 relay will be described with the aid of Figure 3 internal logic schematic 645F607, Figure 4 external logic drawing, the individual module schematics, and Table I.

With three reclosures to lockout selected by the adjustable link on the front panel of the counter module, one high speed reclosure followed by up to two time delayed reclosures will be provided. With the breaker initially open and normal voltage applied to the SRCU-2 the lockout state will be assumed. Under these conditions the amber lockout indicator and the lockout relay will be energized, the counter module output terminals 5, 13 and 11 will be at a "0" logic level and no reclosing can take place. It is important to note that upon dc application the SRCU-2 will always assume the lockout state.

Upon closure of the breaker and opening of the 52b contact, the reset timer is enabled through the circuitry of the 8/0 millisecond 52b anti-bounce timer (counter module terminal 9 – reset module terminal 6). The reset timer is a 3-60 second adjustable timer that is dial calibrated on the front of the reset printed circuit module. Reset of all elements except the indicating lights occurs after the breaker remains closed for the pre-adjusted reset time. The logic "0" reset signal applied to terminal 10 of the counter module resets the counter to its normal state. In this state counter terminal 5 has a logic "1" which, in turn, disables the reset module terminal 10.

The logic "1" from counter terminal 5 is also sent to the high speed reclose circuitry and the time delay reclose circuitry. Applied to terminal 2 of the high speed reclose module it enables the circuitry to allow the T.D. −1 timer to start upon closure of the 52b contact (breaker trip). This allows the TD-1 reclosure to take place if the high speed reclosure is not initiated, which would result in only the two T.D. reclosures to the lockout state.

If it is now assumed that a permanent fault occurs on the line and the breaker is tripped, a High Speed reclosure takes place with the receipt of a H.S. RECL. initiate signal (48/125VDC) on terminal 8 of the relay (term. 11 of the H.S. RECL. module). This initiate signal actuates the H.S. 0-1 second adjustable calibrated timer, which provides a settable range from no intentional delay (.05 second inherently built into the SRCU-2) to the appropriate dead time for EHV applications.

The H.S. RECL. input has an 8/0 millisecond seal-in circuit to provide additional security, and allow a momentary signal to activate the High Speed reclose circuitry. Upon completion of the H.S. time delay the close relay (CR) is energized to reclose the breaker. Note that the pickup time of the CR is included in the calibration of the time dial and contributes to the inherent 50 millisecond minimum time of the H.S. RECL.

With the reclosure of the breaker, the 52b contact opens and the "AND" circuit on the H.S. RECL. module is satisfied to allow a "0" output from terminal 5 of this module to activate the H.S. reclose indicator circuitry and energize the amber H.S. RECL. indicator. The opening of the 52b contact also advanced the counter to the second reclose state. In this state counter module terminal 5 is a "0", terminal 13 is a "1", and terminal 11 is a "0".

This change satisfies the sequence check circuitry which is designed to check for any discrepancy of breaker operations (through 52b contact) versus relay operation settings. If any discrepancy occurs, the lockout state is assumed by the relay, thus making the SRCU-2 anti-pump for failures.

With the relay in the second reclose state, the H.S. reclose circuitry can no longer be activated due to the change of the logic "1" to logic "0" of the first reclose state of the counter on H.S. reclose module terminal 2.

The logic "1" of the second reclose state applied to T.D. reclose module terminal 8 allows the first time delayed reclosure TD-1 to start upon receipt of indication of a second trip of the breaker (52b closure) and receipt of a legitimate signal from the Logic I module as to either a SYN, a HLDB, or a HBDL condition being satisfied. Optional deletion of supervision of any of these Logic I module functions can be accomplished by removal of the corresponding links on the Logic I module.

Likewise, the change to the second reclose state of the counter allows the reset timer to start, if the breaker is closed. This timer, if allowed to time out, resets the SRCU-2. However, since it is assumed that a permanent fault occurred on the line, the breaker is again tripped, which stops the reset timer and resets it.

Now, upon receipt of indication of a second trip of the breaker (52b closure) all requirements for a T.D. −1 reclosure are met and the T.D. −1 reclose timer circuitry is actuated. This timer has an adjustable range of 2 to 120 seconds. Upon completion of the TD-1 time delay the close relay (CR) is energized to reclose the breaker. The pickup time of the CR is included in the calibration of the T.D. −1 time dial.

At the same time that the close relay is energized, a signal indicating that the close relay is sent to the corresponding "AND" circuits which, when respectively satisfied, activate the indicator circuitry of the three TD indicators — SYN, HBDL and HLDB. The requirements for indication are the respective signal being present (SYN or HBDL or HLDB), the close relay being energized, and finally, indication of closure of the breaker by the opening of the 52b contact. Thus, with the reclosure of the breaker after the TD-1 time delay a respective "AND" circuit is satisfied, and one indicator circuit and its respective functional indicator are energized.

The opening of the 52b contact after the TD-1 reclosure also advances the counter to the third reclose state. In this state counter module terminal 5 is a logic "0", terminal 13 is a "0", and terminal 11 is a "1". This change satisfies the sequence check circuitry for anti-pump protection. With this closure of the breaker the reset timer once again starts timing. This timer, if allowed to time out, would reset the SRCU-2. However, since it is assumed that a permanent fault occured on the line, the breaker is again tripped, which stops the reset timer and resets it.

With the closure of the 52b contact upon this third trip, the TD-2 timer is activated and recloses the breaker in the time set on the TD-2 calibrated dial in a manner similar to that previously described for TD-1 reclosure. The TD-2 reclose functional indicator is also activated in a manner previously described to energize the respective SYN, HLDB, or HBDL indicator.

The opening of the 52b contact upon the TD-2 (3rd) reclosure now advances the counter to the state where counter module terminals 5, 13 and 11 all have a logic "0", output. This change once again satisfies the sequence check circuitry for anti-pump protection. Likewise, the reclosure of the breaker once again starts the reset timer. However, since a permanent fault on the line is assumed the breaker is again tripped stopping the reset timer and resetting it.

This trip of the breaker, with the counter module outputs to the reclose circuitry at logic "0",, caused the SRCU-2 to assume the lockout state. This is accomplished when the 52b control signal on reset module terminal 6 becomes a logic "1" upon trip of the breaker. This completes the "AND" circuit with the three logic "0" counter reclose outputs. In the lockout state the lockout relay and the lockout indicator are energized and no reclosing or resetting functions are permitted to take place. The SRCU-2 will remain in this lockout state until the breaker is manually or electrically reclosed.

If we now assume that the fault has been cleared and the breaker is closed the reset circuitry of the SRCU-2 will perform in the manner previously described to reset the relay to the state shown in Figure 3, ready to go through another full sequence in line with the settings made at the beginning of this description.

The high speed reclosure may also optionally be set for supervision by a hot bus, dead-line condition. The HBDL RECL programmable link on the H.S. RECL module, when in position, requires that a HBDL condition exists for H.S. reclosing. Removal of this link removes this option.

The two time delay reclosures may optionally be changed from reclosing based upon breaker operations to reclosing based upon line and bus conditions. This allows one reclosing time delay for a HLDB condition and a different reclosing time delay HBDL condition. The TD-1 timer is then utilized for a HLDB reclosure and the TD-2 timer is utilized for a HBDL reclosure. This can be accomplished by changing the basic "AND" requirements for the timers by switching the three programmable links located on the T.D. RECL module from the A position to the B position.

Another option incorporated into the SRCU-2 is the intermediate lockout function. This function brings the relay to the lockout position one reclosure prior to final lockout, allowing the final reclosure to occur under synchronism check supervision only. In the previous example with the SRCU-2 set for three reclosures to lockout, the SRCU-2 would attain the lockout state after the second reclosure (TD-1) and would allow the final or third reclosure (TD-2) when synchronism exists between the line and the bus. This intermediate lockout function can be optionally switched on or off by changing the programmable link on the counter module front panel.

The logic II module (an optional inclusion depending upon relay style) contains the supervisory close function which will allow one additional reclosure, after all the reclosing operations set on the operations to lockout control. This function overrides the lockout state of the SRCU-2 to provide the additional reclosure. The buffered input activates the appropriate logic circuitry to directly operate the close relay if synchronism or either of the two line-bus conditions have been satisfied for greater than 2 seconds. The logic features anti-pump protection for the additional reclosure. The function is released by removal of the supervisory close input. Optional deletion of this function can be accomplished by removal of the SUPV. RECL. programmable link on this printed circuit module.

Also contained on this optional module is the inhibit function which, when activated, will block all reclosing by the SRCU-2. There are four buffered inputs, two for channel trip and two for loss of channel, which activate the logic circuitry provided for this function. This inhibit function is delayed by a 10 millisecond timer and will release 3 seconds after removal of the transfer trip signal. Reclosing will be prevented during transfer trip even if both channels are lost. Inhibit will not occur if loss of channel is not preceded by a channel trip signal. This function can be optionally deleted by removal of the INHIBIT programmable link on this module.

The dead-line, dead-bus voltage output, another optional function contained on this module, supplies a voltage output for initiating trip on the basis of DLDB after 5 seconds. This buffered output is capable of driving an external ARS type relay for tripping.

TABLE I – LOGIC STATES OF COUNTER MODULE

SRCU-2 SET FOR 3 RECLOSING OPERATIONS TO LOCKOUT (HS, TD-1, AND TD-2)							
BREAKER POSITION	COUNTER MODULE 205C643G01 LOGIC STATES					RELAY FUNCTION	INDICATORS ENERGIZED
	TERMINAL 14 52B CONTACT INPUT	TERMINAL 9 BREAKER STATUS OUTPUT	TERMINAL 5 OUTPUT TO 1ST RECLOSE CIRCUITRY	TERMINAL 13 OUTPUT TO 2ND RECLOSE CIRCUITRY	TERMINAL 11 OUTPUT TO 3RD RECLOSE CIRCUITRY		
CLOSED Reset Position	1	0	1	0	0	RESET POSITION	POWER
OPEN First Trip	0	1	1	0	0	ENABLES FIRST ENCLOSURE	POWER
CLOSED First Reclosure (H.S. RECL)	1	0	0	1	0	ENABLES RESET	POWER H.S. RECL.
OPEN Second Trip	0	1	0	1	0	ENABLES SECOND RECLOSURE	POWER H.S. RECL.
CLOSED Second Reclosure (TD-1 RECL)	1	0	0	0	1	ENABLES RESET	POWER H.S. RECL (TD-1 RECL) { SYN or HBDL or HLDB
OPEN Third Trip	0	1	0	0	1	ENABLES THIRD RECLOSURE	POWER H.S. RECL (TD-1 RECL) { SYN or HBDL or HLDB
CLOSED Third Reclosure (TD-2 RECL)	1	0	0	0	0	ENABLES RESET	POWER H.S. RECL (TD-1 RECL) { SYN or HBDL or HLDB (TD-2 RECL) { SYN or HBDL or HLDB
OPEN Fourth Trip	0	1	0	0	0	LOCKOUT POSITION	POWER H.S. RECL. (TD-1 RECL) { SYN or HBDL or HLDB (TD-2 RECL) { SYN or HBDL or HLDB LOCKOUT

CHARACTERISTICS

DC Control Voltage

The SRCU-2 relay is designed to operate on either 48 or 125 volts dc with no settings or adjustments required other than the 52b contact 8/0 millisecond anti-bounce timer adjustment link located on the power module. The operating range of the SRCU-2 is 42 to 140 volts d.c.

Line-Bus Voltage

The SRCU-2 relay is designed with two single phase potential transformers rated at 132Vac (rms) continuous.

Energy Requirements

Dc Burden: 14 watts at 48Vdc control voltage
16 watts at 125Vdc control voltage

AC Burden:

Bus Potential Transformer:	7 Volt-Amperes max. at 120Vac 60Hz.
Line Potential Transformer:	7 Volt-Amperes max. at 120Vac 60Hz.

Logic Inputs:

52b contact	48/125Vdc control voltage 48V-12mA max. current output to negative 125V-10mA max. current output to negative
H.S. RECL. H.S. BLOCK SUPV. CLOSE	48/125Vdc control voltage burden 48V-1.5mA max. current 125V-2.5mA max. current
All other inputs	15 to 20Vdc buffered 2mA max. current

Logic Outputs:

DLDB	15 to 20Vdc buffered 10mA max. current

Time Delays

Reset	3-60/0 adjustable timer Pickup ±10% Dropout - less than 1msec.
H.S. Reclose	0-1/0 adjustable timer Pickup .05 - 1 second ±5% Dropout less than 1 msec.
TD-1 Reclose	2-120/0 adjustable timer Pickup ±5% Dropout less than 1 msec.
TD-2 Reclose	2-120/0 adjustable timer Pickup ±5% Dropout less than 1 msec.

Line-Bus Detectors

Hot Line	3-120 volts adjustable level-detector ±5%
Dead Line	3-120 volts adjustable level-detector ±5%
Hot Bus	3-120 volts adjustable level-detector ±5%
Dead Bus	3-120 volts adjustable level-detector ±5%
Synchronism	5-120 volts adjustable level-detector ±5%

Surge Withstand Capability

Withstands SWC test proposed by the IEEE Power System Relaying Committee IEEE C72-033-4.

Dimensions

Height	5.25 inches (3 rack units)
Width	19 inches
Depth	14 inches

Weight

Approximately 22 lbs.

Temperature Range

–20°C to +55°C chassis ambient without departure from stated tolerances.

–30°C to +70°C chassis ambient without failure.

SETTINGS

Control Voltage

The only control voltage setting required on the SRCU-2 is the 52b contact, 8/0 anti-bounce timer adjustment located on the power module. The programmable link (48V) should be in place for 48 volt control voltage operation, or removed for 125 volt operation.

Line-Bus Voltage Detectors

The four voltage level detectors on the line-bus module to indicate line and bus status should be

set to the desired setting between 3 to 120Vac by the trimpots HL, DL, HB and DB and their corresponding test points. A logic "0" reading on module test points HL, DL, HB and DB indicates an input signal below the set point.

Synchronism Detector

The synchronism detector on the synchronism module should be set to the desired setting by the SYN trimpot. Typical voltage-angle characteristics of the SRCU-2 for various voltage settings with rated voltage on one circuit is shown in Figure 26. With both the bus and the line voltages in phase the syn. detector can be set from a 5 to 120 Vac voltage difference. A logic "0" reading on the SYN. test point indicates an input signal below the set point. Note that synchronism requires that either Bus or Line or both be "hot".

Reclosing Operations to Lockout

The reclosing operations to lockout selector link located on the front panel of the counter module should be set to the desired number of reclosing operations. By moving the adjustable link to the desired tap on the operations to lockout selector, the SRCU-2 can be set to lockout the breaker after 1, 2 or 3 reclosing operations. When operating on less than 3 reclosing operations to lockout, the reclosing intervals will be dropped starting with the third interval first.

Intermediate Lockout

The intermediate lockout selector link located on the front panel of the counter module should be set to either allow or disallow the intermediate lockout option. The intermediate lockout function (lockout of the SRCU-2 relay at one time-delay reclosure less than the operations to lockout setting, 2nd or 3rd, depending upon link setting) allows the last reclosure to occur for a synchronism condition only. This may be set by moving the link to the ON tap on the intermediate lockout selector.

High Speed Reclose Timer

The high speed reclose time delay should be set to the desired delay with the calibrated potentiometer located on the front panel of the H.S. RECL. module. The knob may be set between the limits shown, 0 (.050) to 1.0 seconds. After making the timer setting, lock the knob by tightening the screw on the knob lock tab assembly.

Hot-Bus, Dead-Line High Speed Reclose Option

The high speed reclosure may also be optionally set to be supervised by a HBDL condition by the HBDL RECL. programmable link on the high speed reclose module. Removal of this link removes this option.

Time Delay Reclose Timers

The time delay reclose timers, TD-1 and TD-2, should be set to the desired time delays with the calibrated potentiometers located on the front panel of the TD RECL module. Both knobs may be set between the limits shown, 2 to 120 seconds. After making the timer settings, lock the knobs by tightening the screw on the knob lock tab assemblies.

Logic I Supervision of Time Delay Reclosures

The three programmable links on the logic I module, HLDB, HBDL, and SYN, should be set for the desired functions for supervision of the T.D. Recl. timers. Both time delayed reclosures are supervised by these three functions; that is, one of these functions must be present (within its setting) for the time delayed reclosures to take effect. Deletion of supervision of any of these functions can be set by removal of the corresponding programmable link on the Logic I module.

Separate Timing Option for HLDB and HBDL Time Delay Reclosing

The TD-1 and TD-2 timers may be optionally set to time a HLDB reclosure on the TD-1 timer and a HBDL reclosure on the TD-2 timer instead of timing the first and second time delayed reclosures based on breaker operation. This is accomplished by setting the three programmable links located on the TD Reclose module. When these links are set in the "A" position the TD timers follow breaker operation. When set in the "B" position the TD timers respond to the bus and line conditions. These reclosures may be all HBDL, or all HLDB, or a selection of both depending upon line and bus status.

Reset Timer

The reset time delay should be set to the desired delay with the calibrated potentiometer located on the front panel of the reset module. The know may be set between the limits shown, 3 to 60 seconds. After making the timer setting, lock the know by tightening the screw on the knob lock tab assembly.

Inhibit Function (Optional with Logic II Module)

The inhibit function is set to block all reclosing by the SRCU-2 relay during transfer trip, even if both channels are lost. Inhibit will occur if loss of channel is preceded by a channel trip signal. This function can be deleted by removal of the INHIBIT programmable link on the Logic II module.

Supervisory Close Function (Optional with Logic II Module)

The supervisory close function is set to override lockout and provide one additional reclosure, when activated, if either synchronism or either of the two line-bus conditions have been satisfied for greater than two seconds. This function can be deleted by removal of the SUPV. RECL. programmable link on the LOGIC II module.

INSTALLATION

The SRCU-2 relay is mounted on a 19 inch wide panel, 5¼ inches high (3 rack units) with edge slots for mounting on a standard relay rack or panel. For the outline and drilling plan, refer to Figure 28. The mounting location must be free from dust, excessive humidity, vibration, corrosive fumes or heat. The maximum temperature around the chassis should not exceed +55°C for normal operation (see CHARACTERISTICS for temperature range specifications).

ADJUSTMENTS & MAINTENANCE

The proper adjustments to insure correct operation of this relay have been made at the factory. Upon receipt of the relay, no customer adjustments other than those covered under "SETTINGS" should be required.

Acceptance Check

It is recommended that an acceptance check be applied to the SRCU-2 relay to verify that the circuits are functioning properly. The SRCU-2 test diagram shown in Figure 27 aids in test of the relay. Proper energization of the relay is also shown in this figure.

A. DC Regulated Supplies (POWER Module)

DC Voltages measured at the respective test points should ±5% for +20 volts and +15 volts over a dc input range of 42 to 140Vdc. Short circuit protection shuts the power supply off if either +20Vdc or +15Vdc are overloaded or short circuited to NEG.

B. Bus-Line Voltage Detectors (LINE-BUS Module)

The four voltage level detectors to indicate line and bus status should be adjustable from 3 to 120 VAC by the trimpots HL, DL, HB and DB. Corresponding module test points are provided, with a logic "0" reading on these test points indicating an input signal below the set point. The line and bus voltages may be applied to the relay terminals directly or to the corresponding test jacks on the front of the relay.

C. Synchronism Detector (SYNCHRONISM Module)

The synchronism detector should be adjustable from 5 to 120VAC (bus-line voltage difference with both in phase) by the Syn. trimpot. All characteristics of the voltage-angle curves shown in Figure 26 should be obtainable. Syn test point "0" reading indicates an input signal below the set point (within the circle).

D. Function Operation

1. Relay Energization

   The SRCU-2 relay should come on in the lockout state (lockout relay and lockout indicator energized) upon energization of D.C. with breaker open. Relay should reset (after breaker is closed) in the reset time delay setting.

2. Link-Programmed Operation

   The SRCU-2 relay should operate functionally in accordance with the printed circuit module link-settings per tests I through XVI of Table II. All settings and time delays should be within tolerance.

3. Test/Reset Switch

   When pushed to test position all indicators should be energized. When pushed to reset position all indicators except the power indicator should turn off.

4. Internal Reclose Lockout Switch

   The internal reclose lockout switch (wired with its two contacts in series with each of the close relay contacts) in the off position prevents reclosure of the breaker.

At completion of the acceptance test return all settings and links to desired position.

TABLE II

Functional Operation Note: Respective indicators should light when each controlling function recloses breaker. Δ = H.S. Reclose permit signal 48/125 VDC applied to relay term. 8 required for H.S. reclosure.	Power 205C655G01	Logic II 205C645G01	TD Reclose 205C659G01	HS Reclose 205C647G01	Logic I 205C657G01	Counter 205C643G01	PRINTED CIRCUIT MODULE	FUNCTIONAL TEST
	48V. 52b Input	Inhibit Supv. Close	A-B A-B A-B	HBDL H.S. Recl.	HBDL HLDB SYN.	Operations to Lockout Inter. Lockout	LINK	
3 Reclosing Operations to Lockout H.S.Δ, TD-1, and TD-2 (or 2 operations to Lockout -TD-1 and TD-2 without HS Permit Signal Δ). T.D. Reclosing Operations Supervised by SYN. or HBDL, or HLDB condition.	Off	Off Off	A A A	Off	On On On	3 Off	I	
2 Reclosing Operations to Lockout H.S. Δ, and TD-1 (or 1 operation to Lockout - TD-1, without HS Permit Signal Δ). T.D. -1 Reclosing Operation supervised by SYN. or HBDL or HLDB condition.	Off	Off Off	A A A	Off	On On On	2 Off	II	
1 Reclosing Operation to Lockout H.S. with Permit Signal Δ (or TD-1 without Permit Signal Δ). T.D.-1 Reclosing Operation supervised by SYN. or HBDL, or HLDB condition.	Off	Off Off	A A A	Off	On On On	1 Off	III	
2 Reclosing Operations to intermediate Lockout (H.S. Δ and TD-1). 3rd. reclosure (TD-2) to final lockout only when SYN. condition exists. T.D.-1 Reclosing Operation supervised by SYN. or HBDL or HLDB condition.	Off	Off Off	A A A	Off	On On On	3 On	IV	
H.S. Reclosing Operation Δ to intermediate lockout. 2nd Reclosure TD-1 to final lockout only when SYN. condition exists.	Off	Off Off	A A A	Off	On On On	2 On	V	
Same as III	Off	Off Off	A A A	Off	On On On	1 On	VI	
Same as I except TD reclosures controlled by HBDL and HLDB conditions (HBDL on TD-2 timer and HLDB on TD-1 Timer). TD reclosure may be all HBDL or all HLDB or one of each.	Off	Off Off	B B B	Off	On On On	3 Off	VII	
Same as II except TD reclosures controlled by HBDL and HLDB conditions (HBDL on TD-2 timer and HLDB on TD-1 Timer). TD reclosure may be HBDL or HLDB.	Off	Off Off	B B B	Off	On On On	2 Off	VIII	

TABLE II

Functional Operation Note: Respective indicators should light when each controlling function recloses breaker. Δ = H.S. Reclose permit signal 48/125 VDC applied to relay term. 8 required for H.S. reclosure.	PRINTED CIRCUIT BREAKER	LINK												FUNCTIONAL TEST
		Power 205C655G01	Logic II 205C645G01	TD Reclose 205C659G01	HS Reclose 205C647G01	Logic I 205C657G01	Counter 205C643G01							
		48V. 52b Input	Inhibit Supv. Close	A-B A-B A-B	HBDL H.S. Recl.	HBDL HLDB SYN.	Operations to Lockout Inter. Lockout							
Same as III except T.D. reclosure controlled by HBDL or HLDB.		Off	Off Off	B B B	Off	On On On	1 Off	IX						
Same as I except T.D. reclose Δ also requires a HBDL condition.		Off	Off Off	A A A	On	On On On	3 Off	X						
Same as I except T.D. reclosing supervision by HBDL is removed.		Off	Off Off	A A A	Off	Off On On	3 Off	XI						
Same as I except T.D. reclosing supervision by HLDB is removed.		Off	Off Off	A A A	Off	On Off On	3 Off	XII						
Same as I except T.D. Reclosing supervision by Syn. is removed.		Off	Off Off	A A A	Off	On On Off	3 Off	XIII						
Same as I except all reclosing is inhibited when (1) a channel trip signal is applied to relay term. 21 or 22 (Inhibit is 10Msec. delayed with 3 sec. or more dropout after removal of trip signal) (2) A channel loss signal to relay term. 23 or 24 is preceded by a channel trip signal. No inhibit is to occur if channel loss is not preceded by channel trip		Off	On Off	A A A	Off	On On On	3 Off	XIV						
Same as I except additional reclosure available after lockout by applying signal to relay term. 25 if either SYN. or HBDL or HLDB condition is satisfied for greater than 2 sec. One reclosure only if provided and can be released by removal of supv. close input (term. 25).		Off	Off On	A A A	Off	On On On	3 Off	XV						
52b input buffer 8/0 Msec. anti-bounce timer for 48 volt supply voltage.		On	Off Off	A A A	Off	On On On	3 Off	XVI						

Routine Maintenance

All relays should be inspected periodically and all settings and times of operation should be checked at least once every year or at such other intervals as may be indicated by experience to be suitable to the particular application.

Calibration

The proper adjustments to insure correct operation of the relay have been made at the factory and should not be disturbed after receipt by the customer. However, if the adjustments or any components have been changed or modules interchanged, then that portion of the SRCU-2 relay changed should be recalibrated and acceptance checked.

The areas where recalibration is possible are as follows:

1. Power Supply Module

   Trimpot. R22 must be adjusted such that the +20Vdc test point is within 1% of +20Vdc.

2. No other calibration is necessary other than desired changes in settings.

Trouble Shooting

The components in the SRCU-2 relay are operated well within their ratings and normally will give long and trouble free service. However, if a relay has given indication of trouble in service or during routine checks, then using "0" and "1" logic notation, the faulty printed circuit module (s) can be identified using the relay logic schematic, Figure 3.

In turn, the faulty component, connection, or circuit can be found using the individual module schematics which show the detailed NOR/NAND logic.

Each NOR block, shown by an AND with negated inputs or an OR with negated output represents a transistor on the module schematic. Likewise, each NAND integrated circuit is represented by an AND with a negated output or an OR with negated inputs with the specific I.C. terminals described.

Voltage levels for "0" and "1" logic states shown on the Fig. 3 logic drawing are:

Logic "0" is equivalent to less than 1Vdc and a logic "1" is equivalent to 8 to 15Vdc, except for the negative logic outputs to the indicators, close relay, and lockout relay where "0" is 20Vdc and "1" is zero.

For voltage levels on modules not employing conventional logic, refer the particular module operation description.

A module extender, style no. 3494A90G01, is available for facilitating circuit voltage measurements. Do not remove or insert modules while the SRCU-2 relay is energized as damage may result.

RENEWAL PARTS

Repair work can be done most satisfactorily at the factory. However, interchangeable parts can be furnished to the customers who are equipped for doing repair work. When ordering parts, always give data and appropriate Westinghouse style numbers.

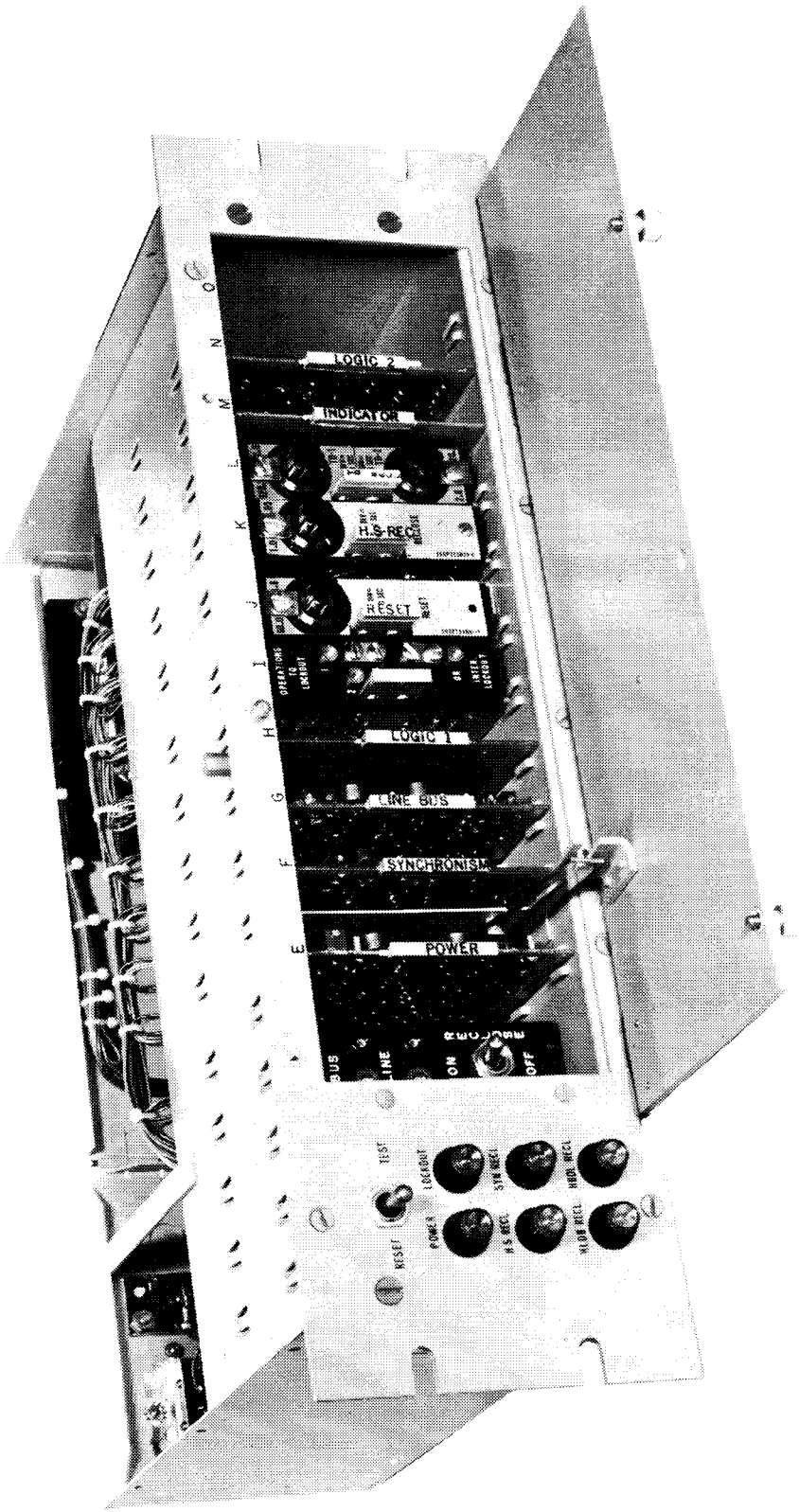


Fig. 1 Type SRCU-2 Relay – Front View

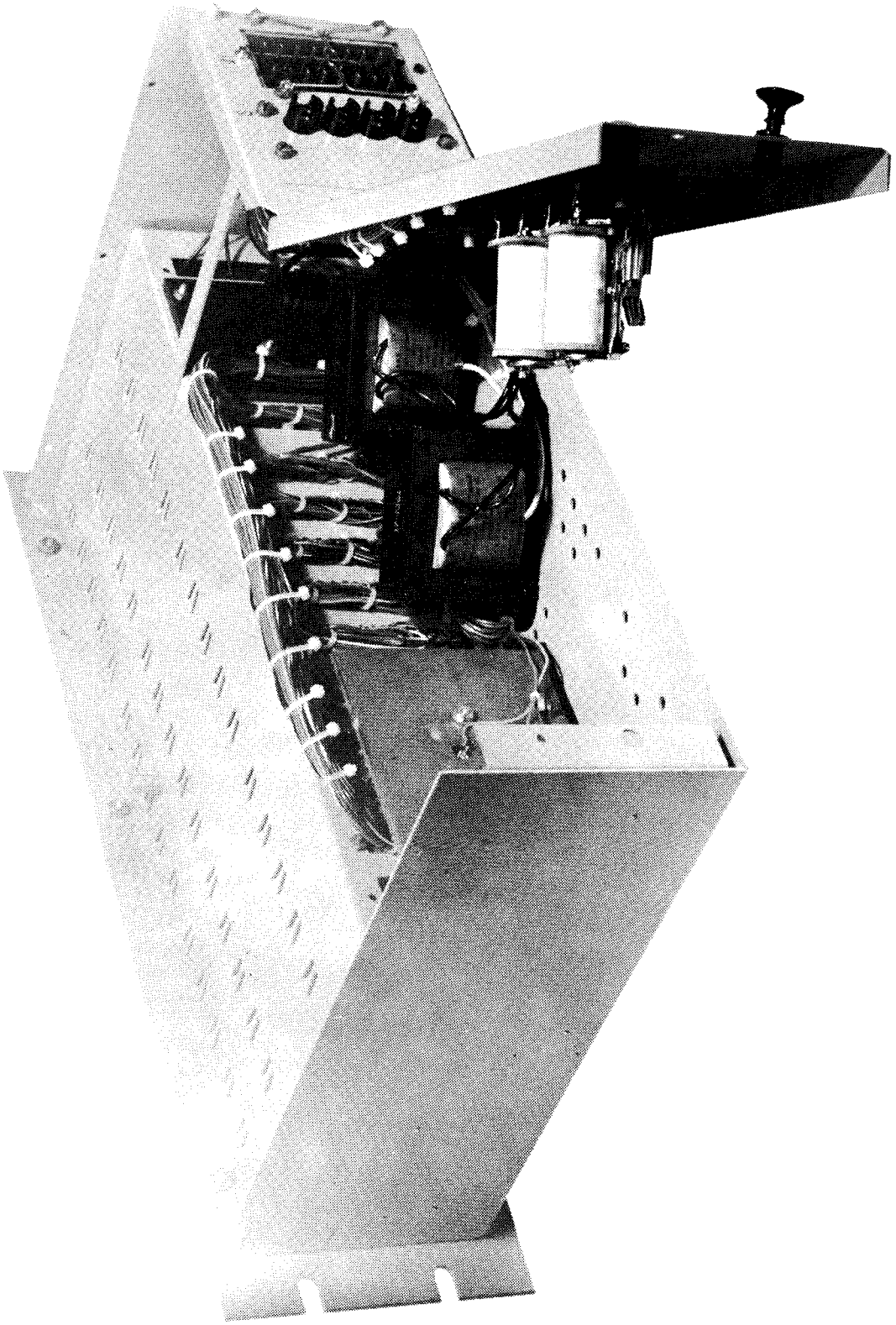
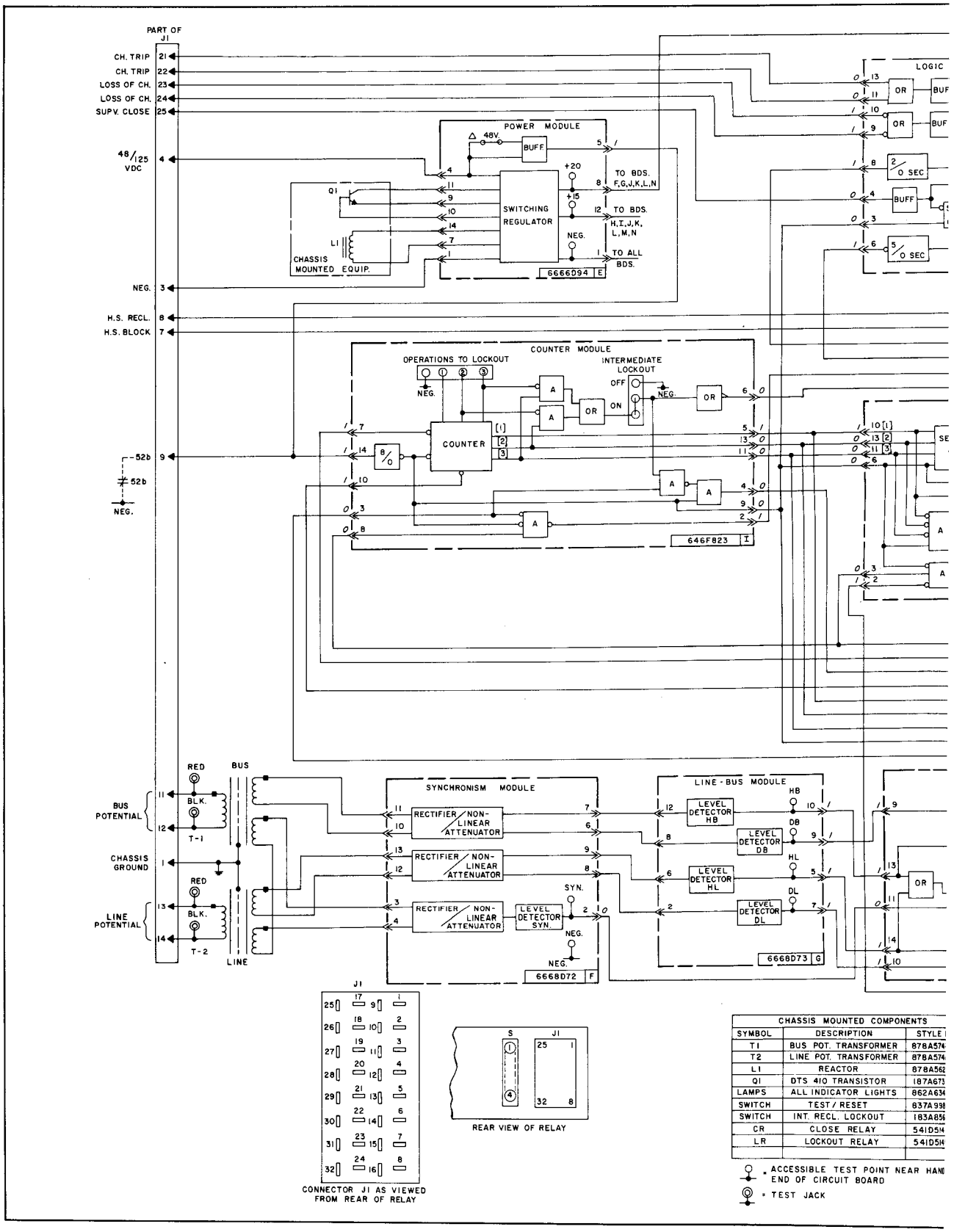


Fig. 2 Type SRCU-2 Relay – Rear View

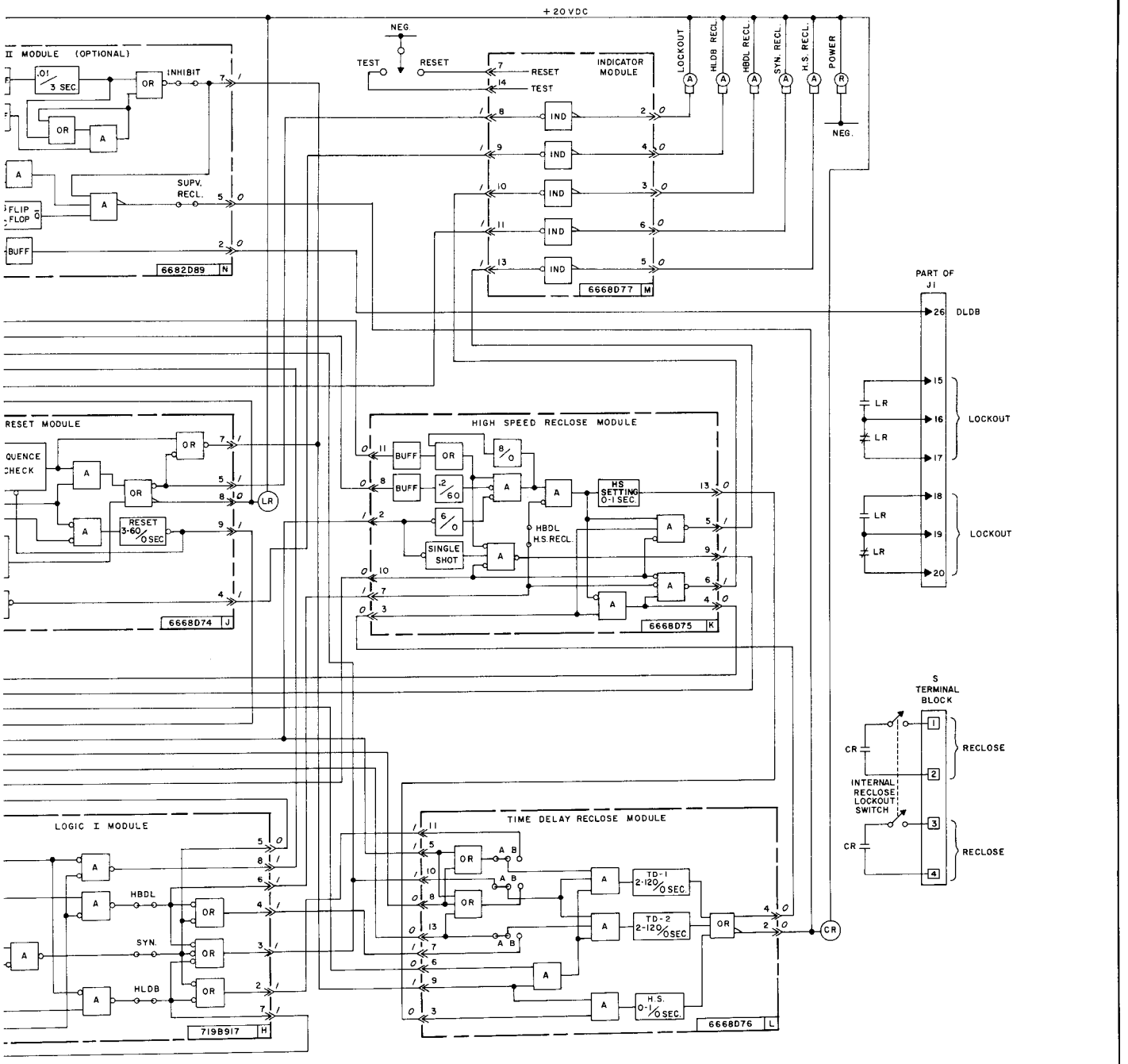


CHASSIS MOUNTED COMPONENTS		
SYMBOL	DESCRIPTION	STYLE
T1	BUS POT. TRANSFORMER	878A574
T2	LINE POT. TRANSFORMER	878A574
L1	REACTOR	878A562
Q1	DTS 410 TRANSISTOR	187A673
LAMPS	ALL INDICATOR LIGHTS	862A634
SWITCH	TEST / RESET	837A998
SWITCH	INT. RECL. LOCKOUT	183A856
CR	CLOSE RELAY	541D514
LR	LOCKOUT RELAY	541D514

= ACCESSIBLE TEST POINT NEAR HAND END OF CIRCUIT BOARD

= TEST JACK

Fig. 3.



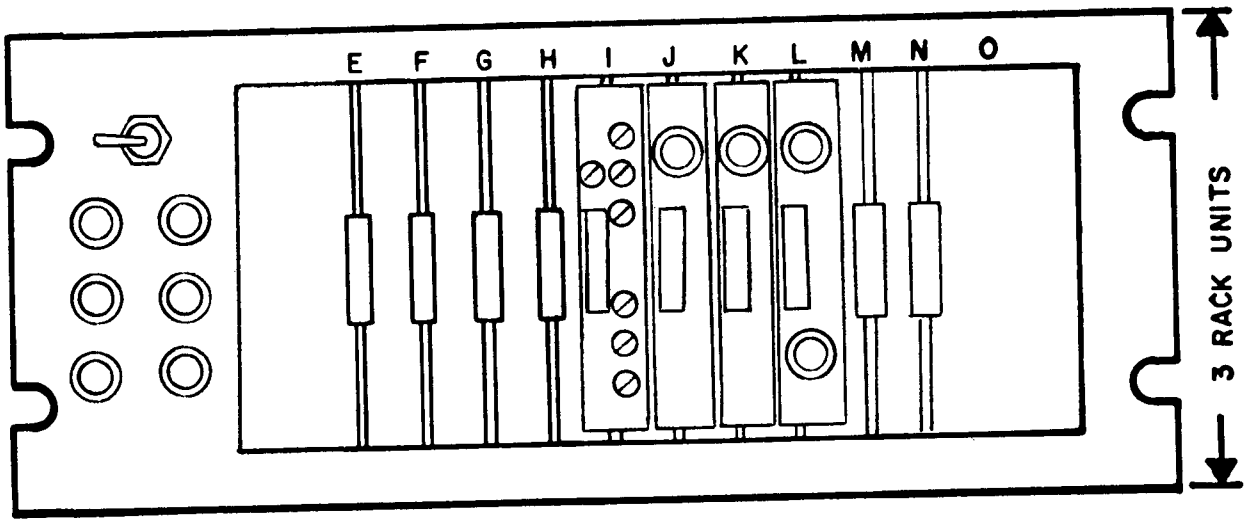
NOTES:

△ • REMOVE 48 VOLT LINK FOR 125 VDC OPERATION ON POWER MODULE LOCATION "E".

SIGNAL STATES "0" OR "/" ARE SHOWN FOR ALL NORMAL CONDITIONS WITH BREAKER CLOSED, 52b OPEN, SRCU-2 RESET, BOTH LINE AND BUS "HOT" AND IN SYNCHRONISM.

Sub. 4
645F607

SRCU-2 Internal Logic Schematic

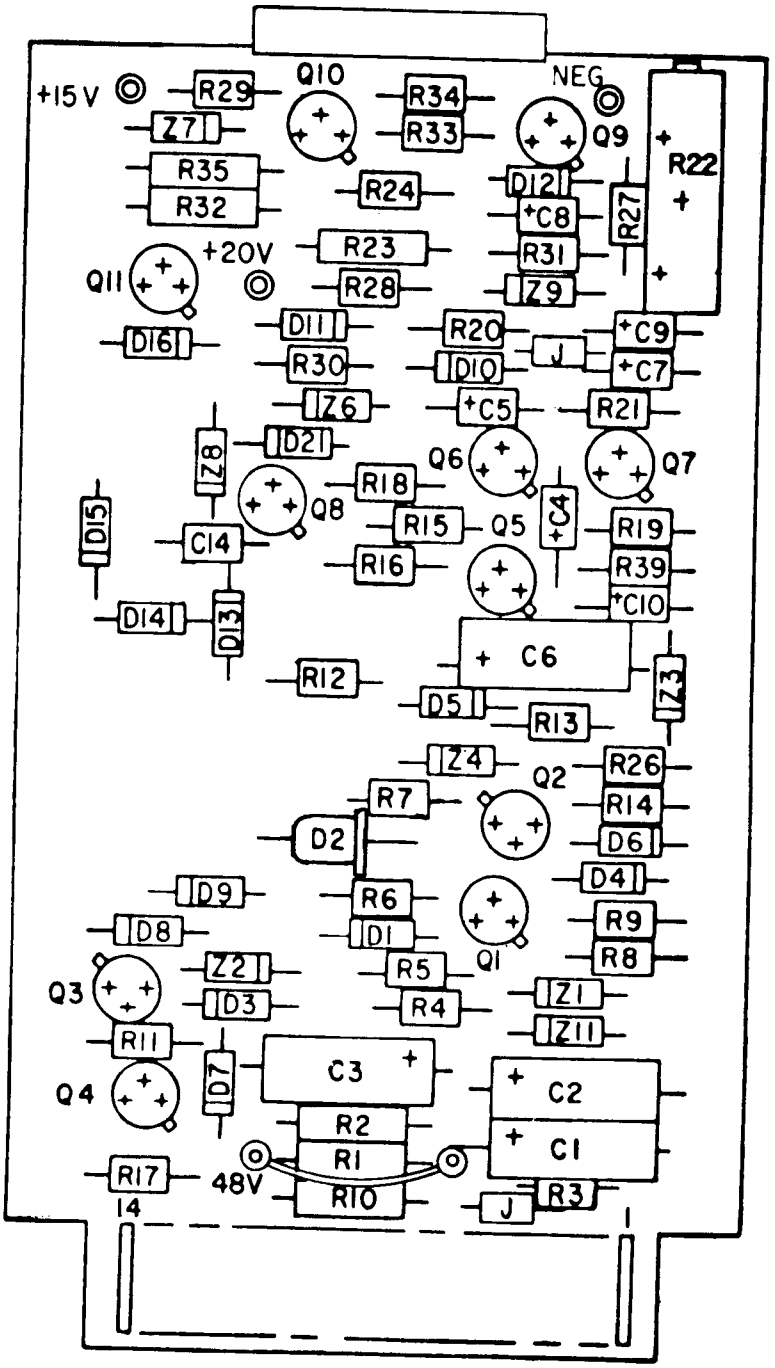


FRONT VIEW
(COVER REMOVED)

BOARD POSITION	BOARD DESCRIPTION
E	POWER SUPPLY
F	SYNCHRONISM
G	LINE BUS
H	LOGIC I
I	COUNTER
J	RESET
K	H S RECLOSE
L	T D RECLOSE
M	INDICATOR
N	LOGIC II
O	

3490A28

Fig. 5 Relay Type SRCU-2 Component Location



880A966

Fig. 6 Power Supply Module Component Location

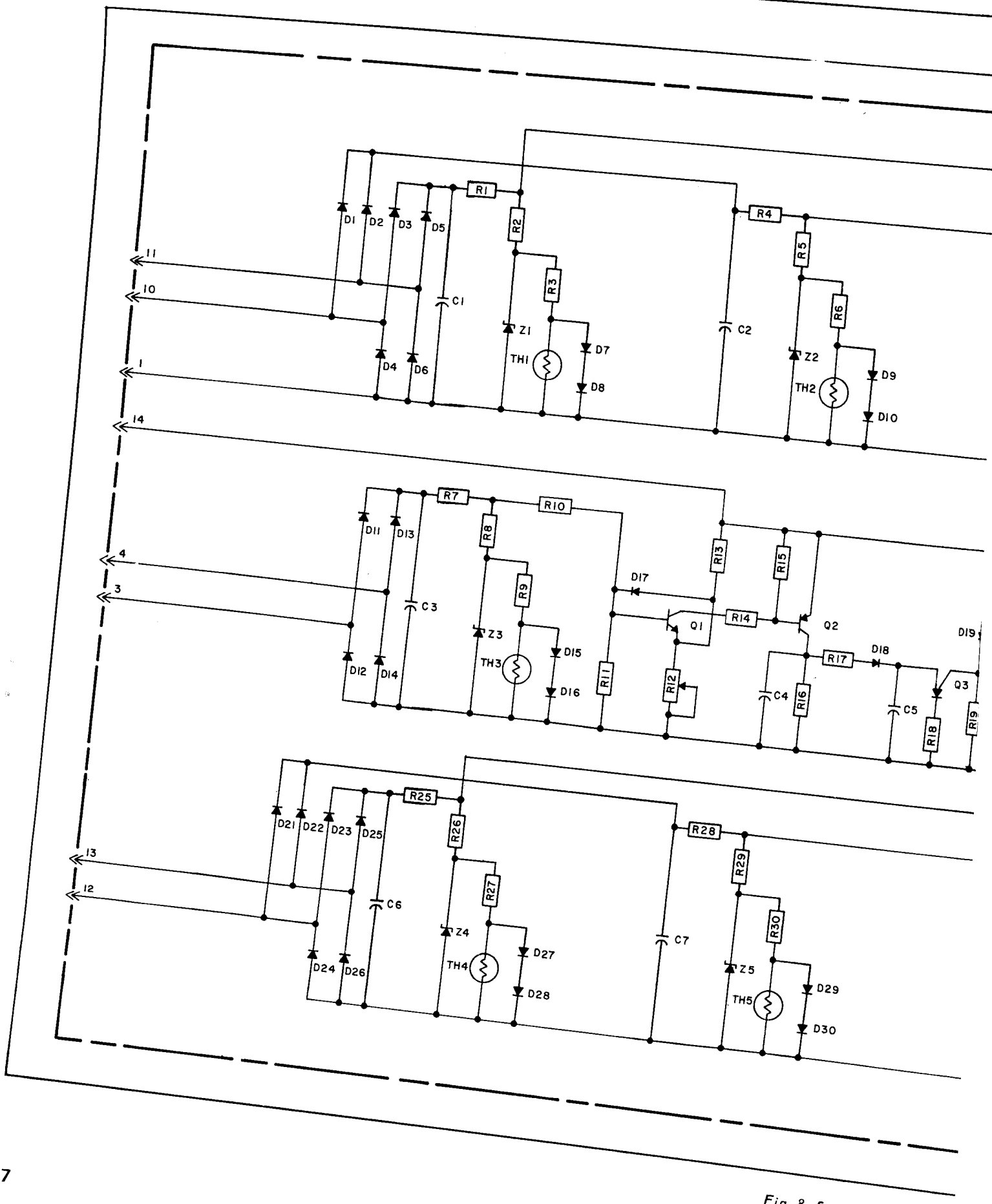
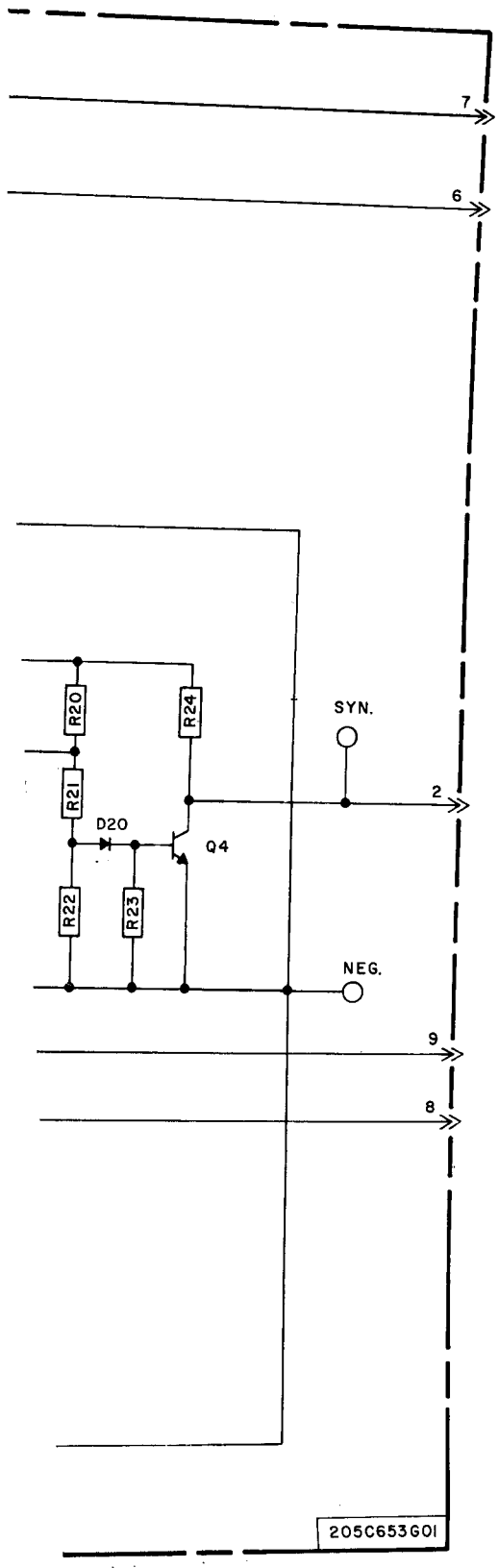


Fig. 8 Synchronism Module

I.L. 41-670A



RESISTOR	DESCRIPTION	STYLE NO.
R1-R4-R25-R28	5K 3W ±1%	763A126H24
R2-R5-R8-R26-R29	1.1K 1/2W ±1%	862A376H05
R3-R6-R9-R27-R30	2.49K 1/2W ±1%	862A376H39
R7	5K 5W ±1%	763A130H19
R10	3.32K 1/2W±1%	862A376H51
R11	11K 1/2W ± 1%	848A820H49
R13	3.65K 1/2W ± 1%	862A376H55
R14-R17	5.49K 1/2W ±1%	848A820H20
R15-R23	10K 1/2W ± 2%	629A531H56
R16	12.1K 1/2W ±1%	848A820H53
R18	100Ω 1/2W ± 2%	629A531H08
R19	1 MEG. 1/2W. ± 5%	184A763H99
R20	100K 1/2W ± 1%	848A821H42
R21-R22	49.9K 1/2W ± 1%	848A821H13
R24	.15 MEG. 1/2W ±2%	629A531H84

POT	DESCRIPTION	STYLE NO.
R12	20K 3/4W ±10%	880A826H01

CAPACITOR	DESCRIPTION	STYLE NO.
C1-C2-C3-C6-C7	.27MFD. 200V.	188A669H05
C4	4.7MFD. 35V.	184A661H12
C5	.1 MFD. 200V.	188A669H03

DIODE	DESCRIPTION	STYLE NO.
D1 TO D6-D21 TO D26	1N4818	188A342H06
D11 TO D14	1N4821	188A342H16
D7 TO D10-D15 TO D20-D27 TO D30	1N4148	836A928H06

TRANSISTOR	DESCRIPTION	STYLE NO.
Q1-Q4	2N2219A	762A672H11
Q3	U13T1	878A289H01
Q2	2N2905A	762A672H10

ZENER DIODE	DESCRIPTION	STYLE NO.
Z1 TO Z5	1N957B	186A797H06

THERMISTOR	DESCRIPTION	STYLE NO.
TH1 TO TH5	10K	185A211H04

COMPONENT LOCATION_____880A997

6668D72

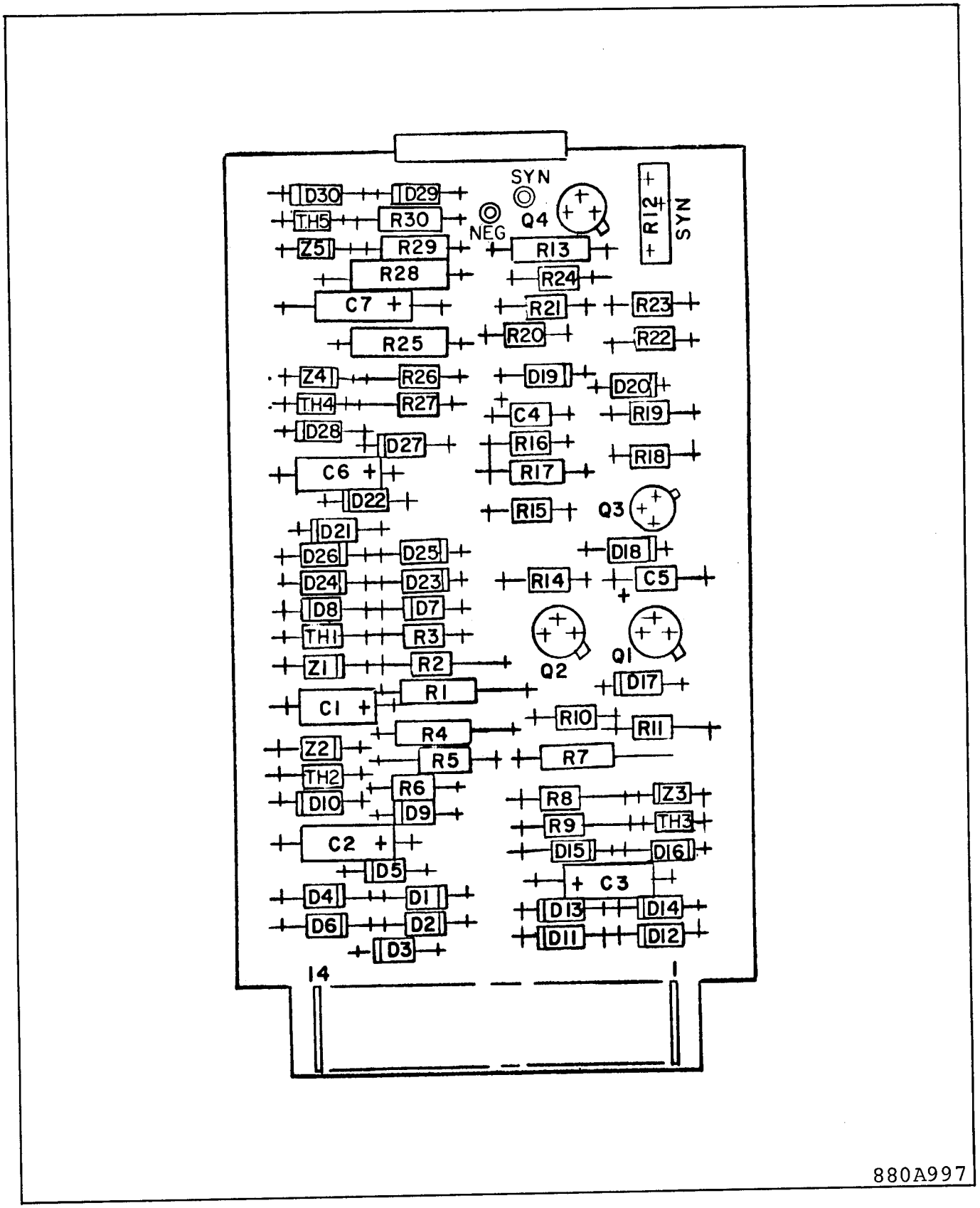


Fig. 9 Synchronism Module Component Location

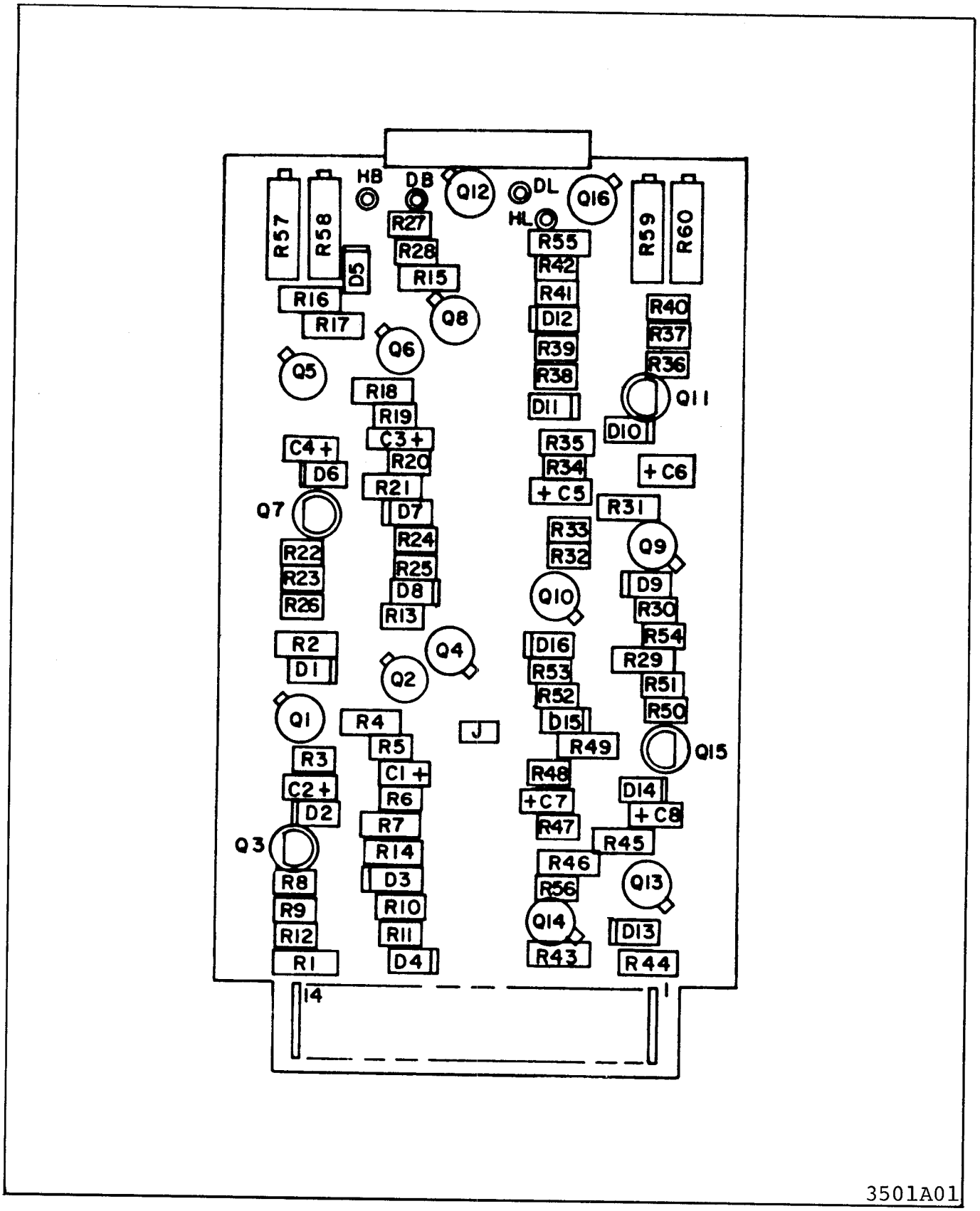


Fig. 10 Line-Bus Module Component Location

RESISTOR	DESCRIPTION	STYLE NO.
R1-R15-R29-R43	3.32K 1/2W ±1%	862A376H51
R2-R16-R30-R44	11K 1/2W ±1%	848A820H49
R3-R17-R31-R45	3.65K 1/2W ±1%	862A376H55
R4-R7-R18-R21-R32-R35-R46-R49	5.49K 1/2W ±1%	848A820H20
R5-R13-R19-R27-R33-R41-R47-R55	10K 1/2W ±1%	629A531H56
R6-R20-R34-R48	12.1K 1/2W ±1%	848A820H53
R8-R22-R36-R50	100Ω 1/2W ±1%	629A531H08
R9-R23-R37-R51	1MEG. 1/2W ±5%	184A763H99
R10-R24-R38-R52	100K 1/2W ±1%	848A821H42
R11-R12-R25-R26-R39-R40-R53-R54	49.9K 1/2W ±1%	848A821H13
R14-R28-R42-R56	15MEG. 1/2W ±1%	629A531H84

POT	DESCRIPTION	STYLE NO.
R57-R58-R59-R60	20K 3/4W ±10%	880A826H01

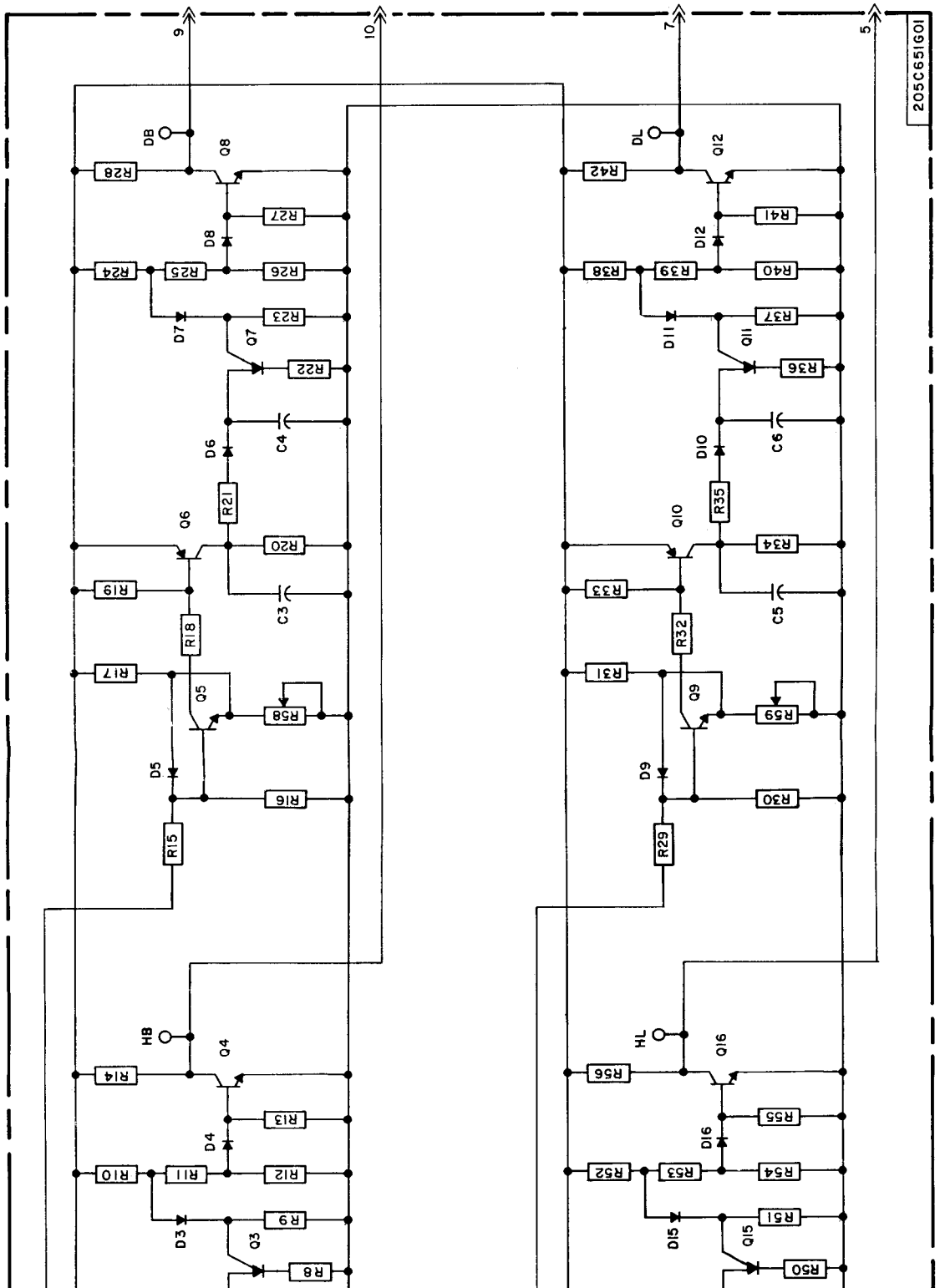
CAPACITOR	DESCRIPTION	STYLE NO.
C1-C3-C5-C7	4.7MFD. 35V	184A661H12
C2-C4-C6-C8	.1 MFD. 200V.	188A669H03

DIODE	DESCRIPTION	STYLE NO.
D1 TO D16	IN4148	878A649H01

TRANSISTOR	DESCRIPTION	STYLE NO.
Q1-Q4-Q5-Q8-Q9-Q12-Q13-Q16	2N2219A	762A672H11
Q2-Q6-Q10-Q14	2N2905A	762A672H10
Q3-Q7-Q11-Q15	U13T1	878A289H01

JUMPER	DESCRIPTION	STYLE NO.
COMPONENT	0 Ω	862A478H01

COMPONENT LOCATION-------- 3501A01



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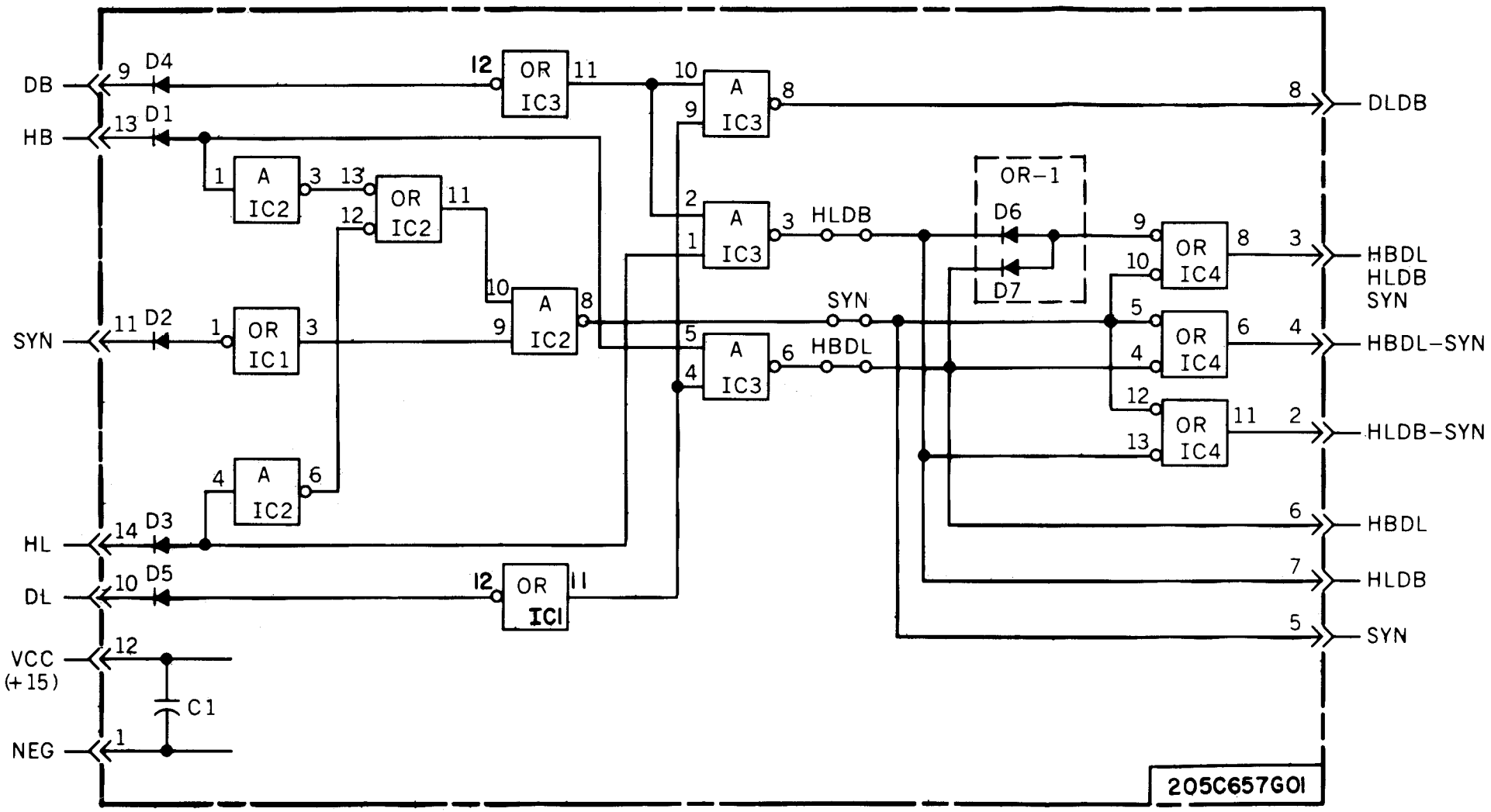
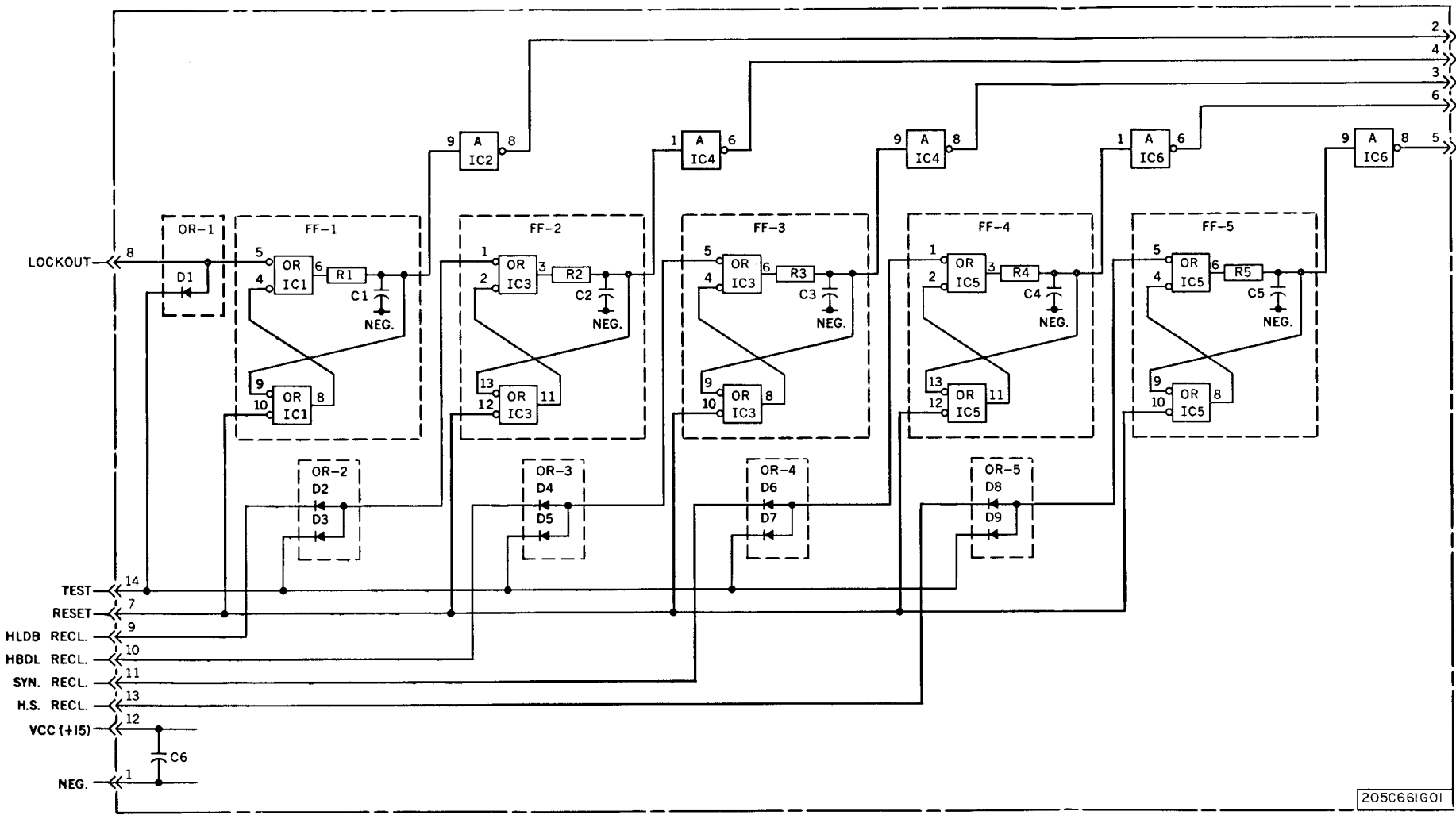
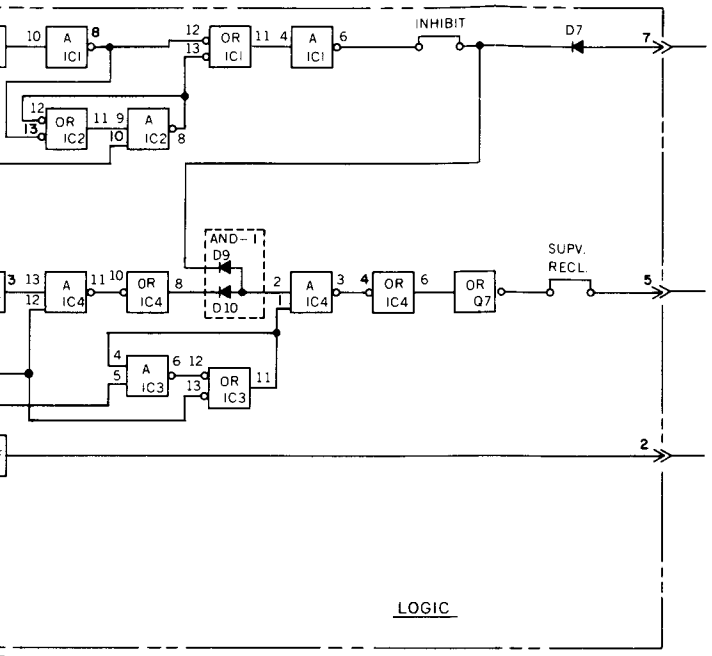
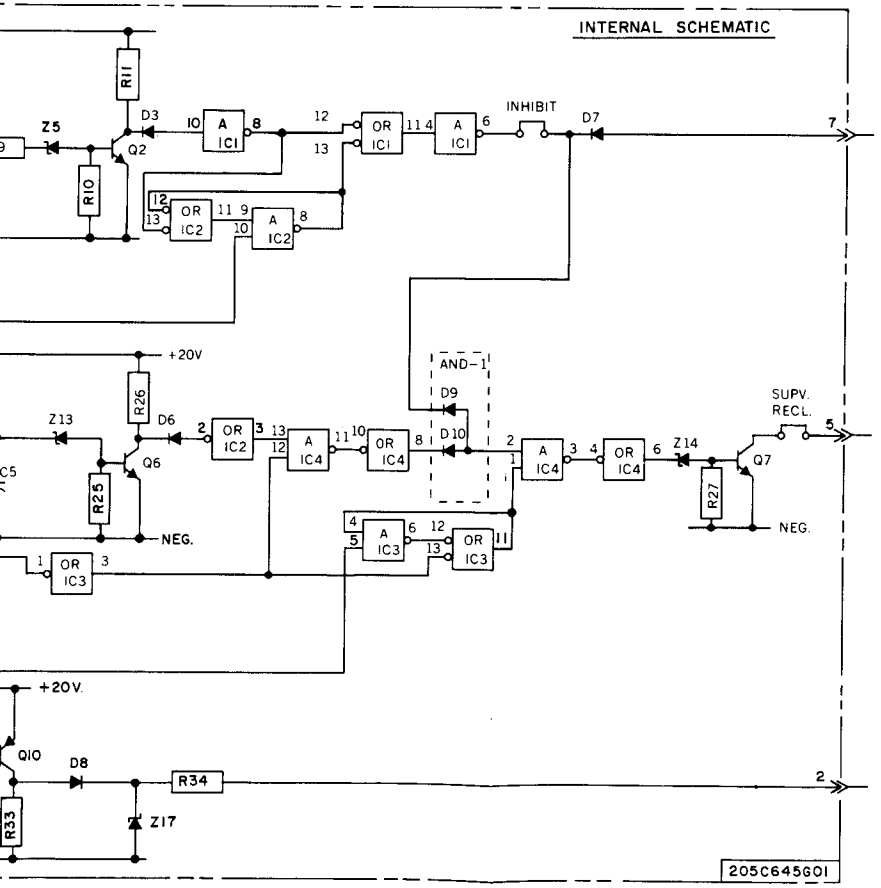

DB
HB
SYN
HL
DL
VCC (+15)
NEG
D1
D2
D3
D4
D5
C1
OR IC1
OR IC2
OR IC3
A IC2
A IC3
OR-1
D6
D7
HLDB
SYN
HBDL
OR IC4
DLDB
HBDL HLDB SYN
HBDL-SYN
HLDB-SYN
HBDL
HLDB
SYN
205C657G01


LOCKOUT
TEST
RESET
HLDB RECL.
HBDL RECL.
SYN. RECL.
H.S. RECL.
VCC (+15)
NEG.
OR-1
D1
FF-1
FF-2
FF-3
FF-4
FF-5
OR IC1
OR IC3
OR IC5
R1
R2
R3
R4
R5
C1
C2
C3
C4
C5
C6
NEG.
A IC2
A IC4
A IC6
OR-2
D2
D3
OR-3
D4
D5
OR-4
D6
D7
OR-5
D8
D9
205C661G01





RESISTOR	DESCRIPTION	STYLE NO.
R1-R2-R3-R12-R13-R14-R18-R19-R35	4,7K 1/2W±2%	629A531H48
R4-R11-R15-R17 R20-R22-R26-R33 R36	82K 1/2W±2%	629A531H78
R5-R9-R16-R21 R23-R27-R28-R32 R37	10K 1/2W±2%	629A531H56
R6-R10-R25-R30	20K 1/2W±2%	629A531H63
R24	120K 1/2W±2%	629A531H82
R7	22K 1/2W±2%	629A531H64
R8	300Ω 1/2W±2%	629A531H19
R29	100K 1/2W±2%	629A531H80
R31	6,8K 1/2W±2%	629A531H52
R34	150Ω 3W	762A679H01
CAPACITOR	DESCRIPTION	STYLE NO.
C1-C3-C4-C9	.047MFD. 200V	849A437H04
C5	47MFD. 35V	837A241H22
C2-C6	150MFD. 30V	862A177H05
C7	.27MFD. 200V	188A669H05
C8	.47MFD. 50V	762A680H04
DIODE	DESCRIPTION	STYLE NO.
D1 TO D7-D9-D10	IN4148	836A928H06
D8	IN645A	837A692H03
TRANSISTOR	DESCRIPTION	STYLE NO.
Q1 TO Q9-Q11	2N2219A	762A672H11
Q10	2N2905A	762A672H10
ZENER DIODE	DESCRIPTION	STYLE NO.
Z1-Z2-Z17	IN3688A	862A288H01
Z3-Z6-Z8-Z10	IN3686B	185A212H06
Z4-Z5-Z7-Z9-Z11 TO Z16	IN957B	186A797H06
INT. CKT.	DESCRIPTION	STYLE NO.
IC1 TO IC4	MC672L	6296D58H01
JUMPER	DESCRIPTION	STYLE NO.
LINK	INHIBIT	3489A69G01
LINK	SUPV. RECL.	3489A69G01

COMPONENT LOCATION _____ 880A990

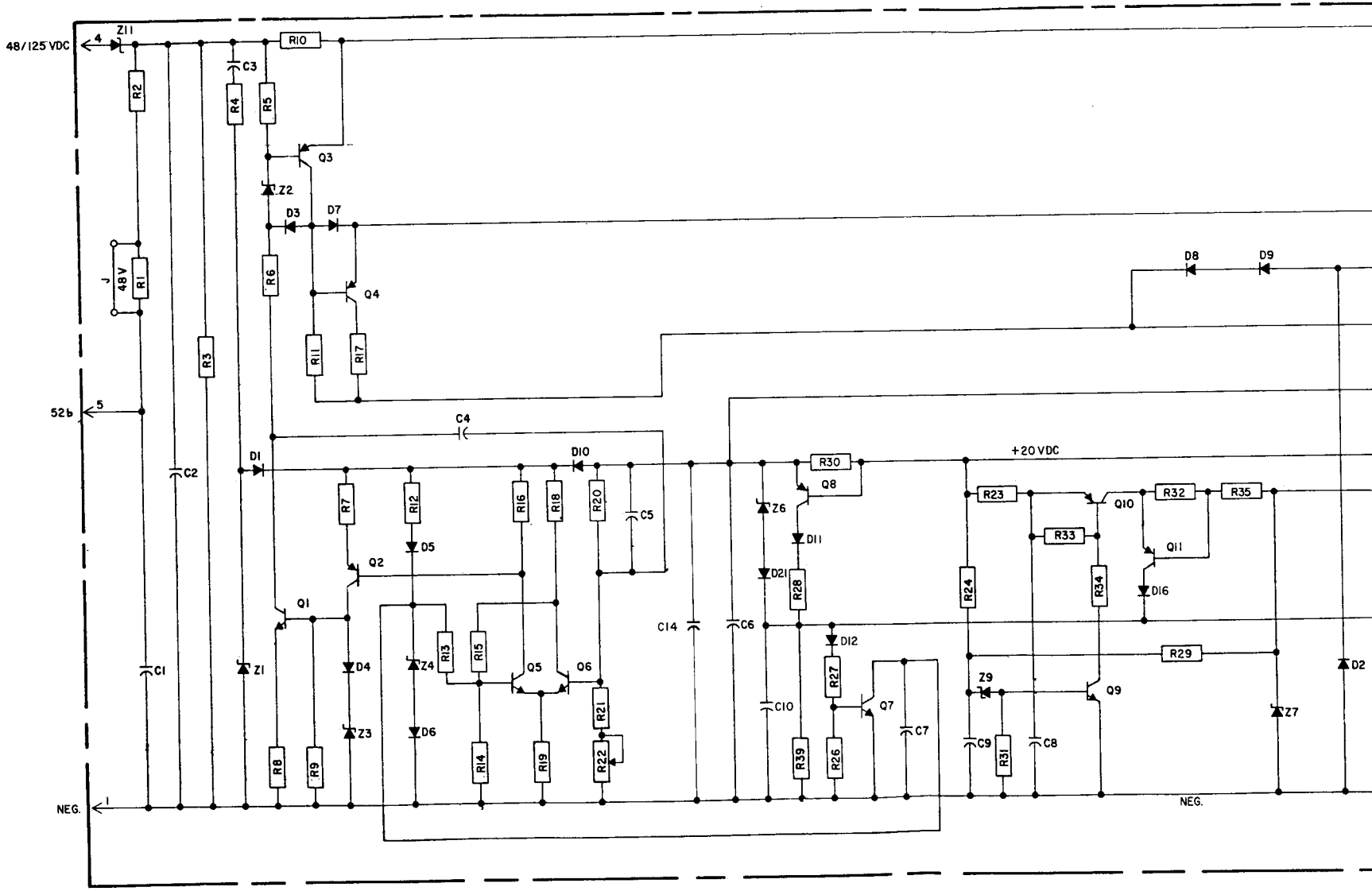
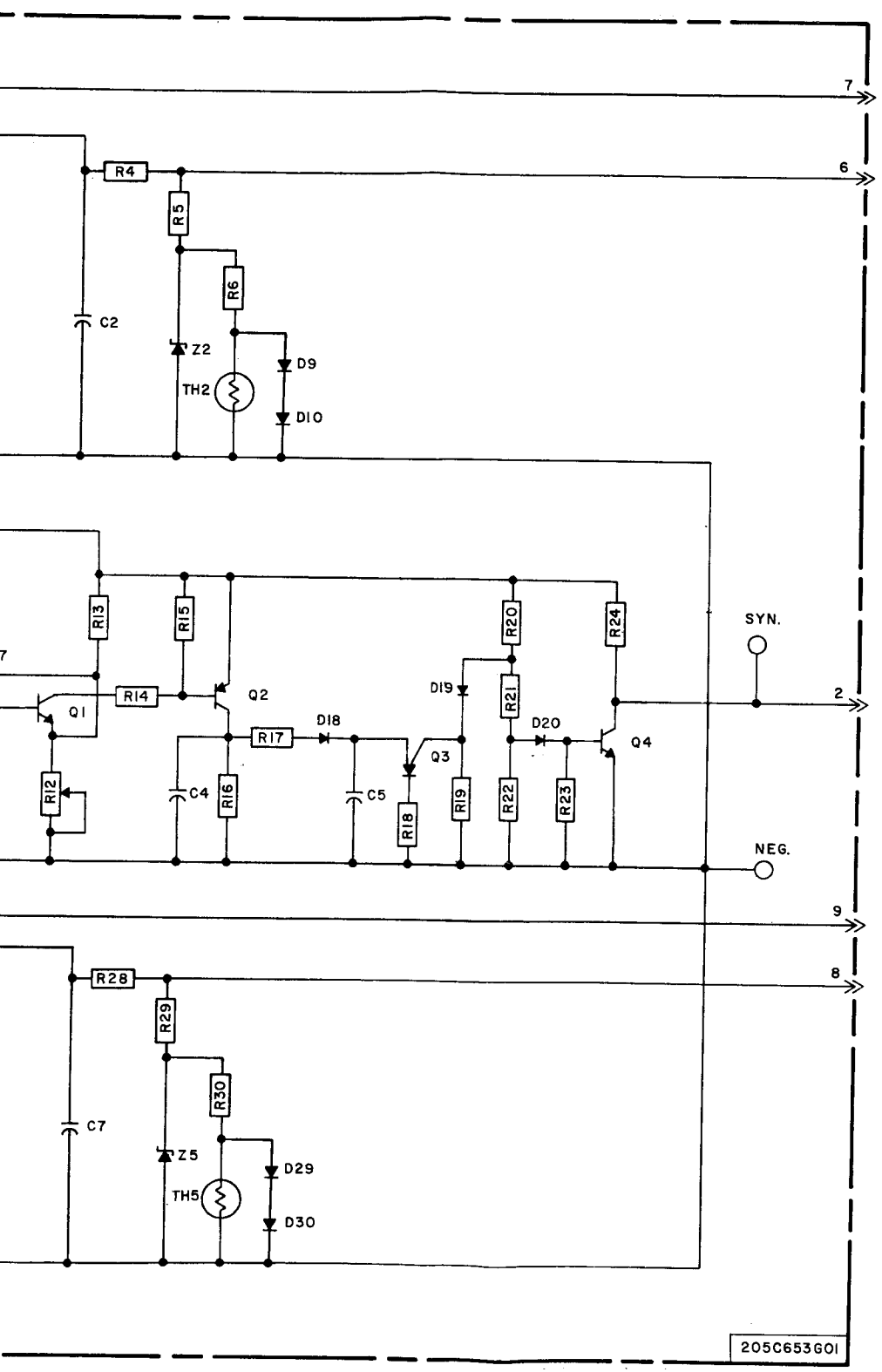


Fig. 7. Power Supply Module Internal Schematic



RESISTOR	DESCRIPTION	STYLE NO.
R1-R4-R25-R28	5K 3W ±1%	763A126H24
R2-R5-R8-R26-R29	1.1K 1/2W ±1%	862A376H05
R3-R6-R9-R27-R30	2.49K 1/2W ±1%	862A376H39
R7	5K 5W ±1%	763A130H19
R10	3.32K 1/2W±1%	862A376H51
R11	11K 1/2W ± 1%	848A820H49
R13	3.65K 1/2W ± 1%	862A376H55
R14-R17	5.49K 1/2W ±1%	848A820H20
R15-R23	10K 1/2W ±2%	629A531H56
R16	12.1K 1/2W ±1%	848A820H53
R18	100Ω 1/2W ±2%	629A531H08
R19	1 MEG. 1/2W. ± 5%	184A763H99
R20	100K 1/2W ± 1%	848A821H42
R21-R22	49.9K 1/2W ± 1%	848A821H13
R24	.15 MEG. 1/2W ±2%	629A531H84

POT	DESCRIPTION	STYLE NO.
R12	20K 3/4W ±10%	880A826H01

CAPACITOR	DESCRIPTION	STYLE NO.
C1-C2-C3-C6-C7	.27MFD. 200V.	188A669H05
C4	4.7 MFD. 35V.	184A661H12
C5	.1 MFD. 200V.	188A669H03

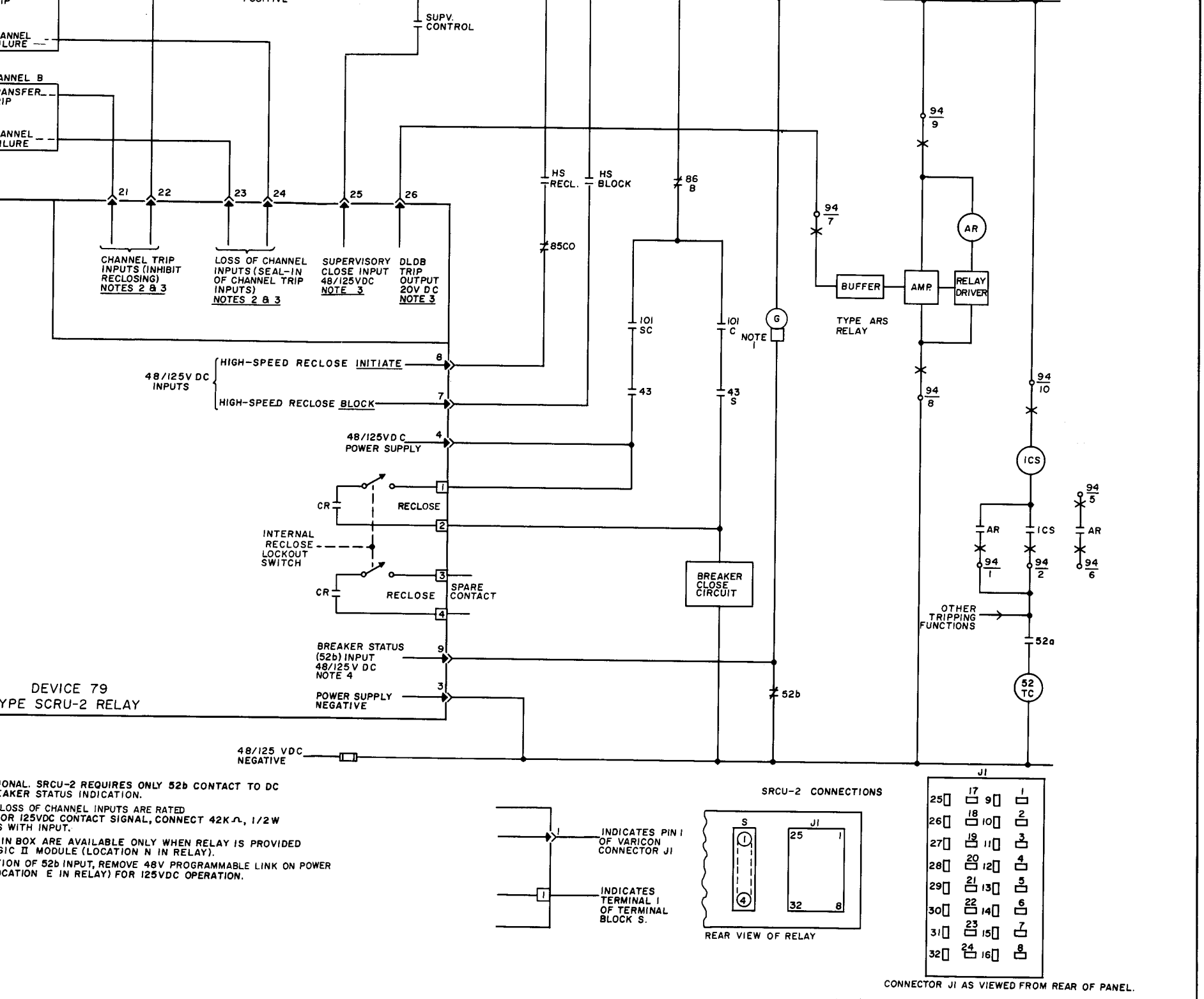
DIODE	DESCRIPTION	STYLE NO.
D1 TO D6-D21 TO D26	1N4818	188A342H06
D11 TO D14	1N4821	188A342H16
D7 TO D10-D15 TO D20-D27 TO D30	1N4148	836A928H06

TRANSISTOR	DESCRIPTION	STYLE NO.
Q1 - Q4	2N2219A	762A672HH
Q3	U13T1	878A289H01
Q2	2N2905A	762A672H10

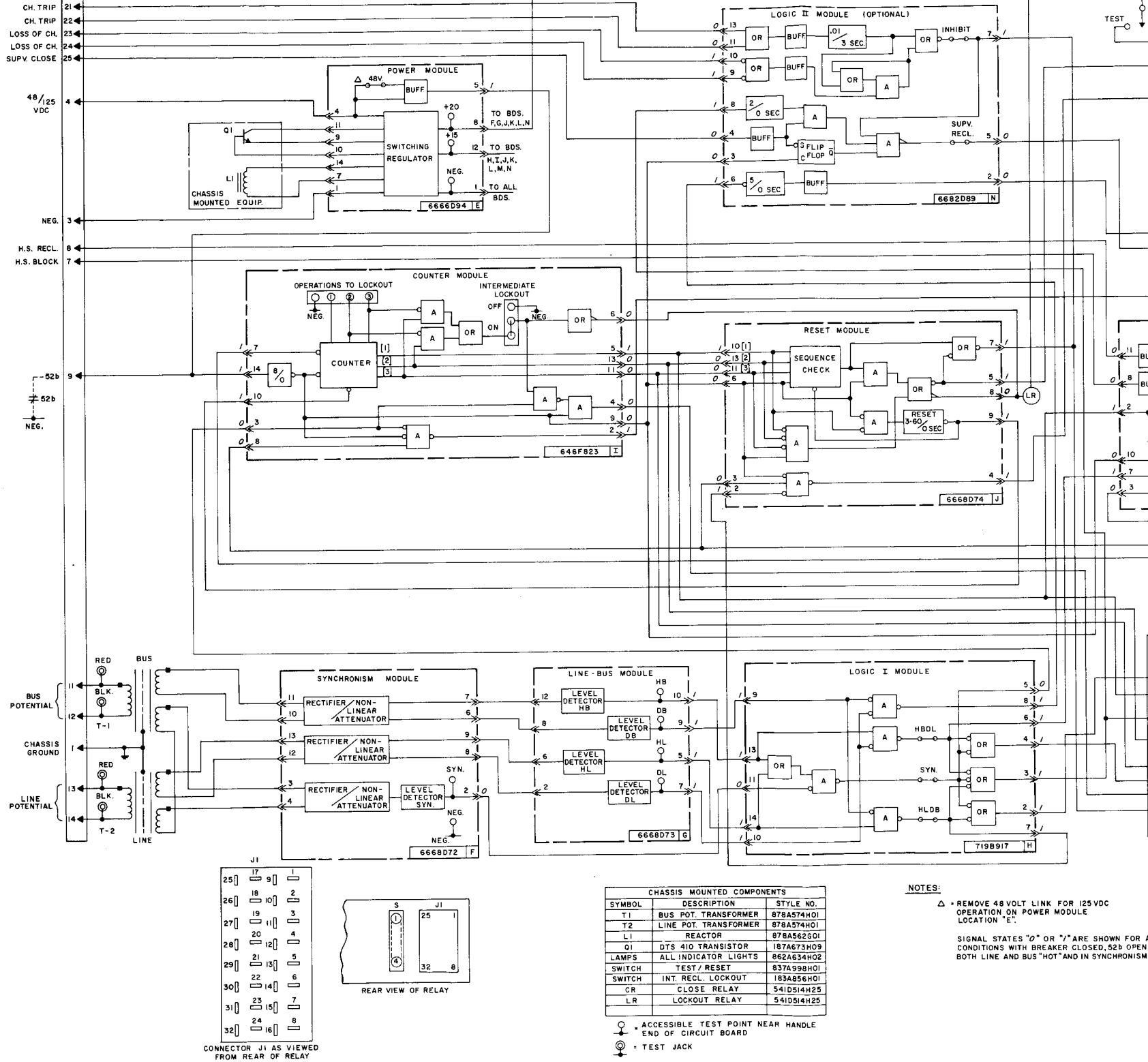
ZENER DIODE	DESCRIPTION	STYLE NO.
Z1 TO Z5	1N957B	186A797H06

THERMISTOR	DESCRIPTION	STYLE NO.
TH1 TO TH5	10K	185A211H04

COMPONENT LOCATION_____ 880A997


SUPV. CONTROL
21
22
23
24
25
26
CHANNEL TRIP INPUTS (INHIBIT RECLOSING) NOTES 2 & 3
LOSS OF CHANNEL INPUTS (SEAL-IN OF CHANNEL TRIP INPUTS) NOTES 2 & 3
SUPERVISORY CLOSE INPUT 48/125VDC NOTE 3
DLDB TRIP OUTPUT 20V DC NOTE 3
HS RECL.
HS BLOCK
86 B
85CO
101 SC
101 C
43
43 S
G
NOTE 1
94/7
94/9
94/8
94/10
BUFFER
AMP.
RELAY DRIVER
AR
TYPE ARS RELAY
ICS
94/5
94/1
94/2
94/6
OTHER TRIPPING FUNCTIONS
52a
52 TC
52b
48/125V DC INPUTS
HIGH-SPEED RECLOSE INITIATE
HIGH-SPEED RECLOSE BLOCK
48/125VDC POWER SUPPLY
CR
RECLOSE
INTERNAL RECLOSE LOCKOUT SWITCH
SPARE CONTACT
BREAKER CLOSE CIRCUIT
BREAKER STATUS (52b) INPUT 48/125 V DC NOTE 4
POWER SUPPLY NEGATIVE
48/125 VDC NEGATIVE
DEVICE 79
YPE SCRU-2 RELAY
ONAL. SRCU-2 REQUIRES ONLY 52b CONTACT TO DC
AKER STATUS INDICATION.
LOSS OF CHANNEL INPUTS ARE RATED
OR 125VDC CONTACT SIGNAL, CONNECT 42KΩ, 1/2W
S WITH INPUT.
IN BOX ARE AVAILABLE ONLY WHEN RELAY IS PROVIDED
SIC II MODULE (LOCATION N IN RELAY).
ION OF 52b INPUT, REMOVE 48V PROGRAMMABLE LINK ON POWER
CATION E IN RELAY) FOR 125VDC OPERATION.
INDICATES PIN 1 OF VARICON CONNECTOR J1
INDICATES TERMINAL 1 OF TERMINAL BLOCK S.
SRCU-2 CONNECTIONS
S
J1
REAR VIEW OF RELAY
CONNECTOR J1 AS VIEWED FROM REAR OF PANEL.

6688D23



CHASSIS MOUNTED COMPONENTS		
SYMBOL	DESCRIPTION	STYLE NO.
T1	BUS POT. TRANSFORMER	878A574H01
T2	LINE POT. TRANSFORMER	878A574H01
L1	REACTOR	878A562G01
Q1	DTS 410 TRANSISTOR	187A673H09
LAMPS	ALL INDICATOR LIGHTS	862A634H02
SWITCH	TEST / RESET	837A998H01
SWITCH	INT. RECL. LOCKOUT	183A856H01
CR	CLOSE RELAY	541D514H25
LR	LOCKOUT RELAY	541D514H25

= ACCESSIBLE TEST POINT NEAR HANDLE END OF CIRCUIT BOARD

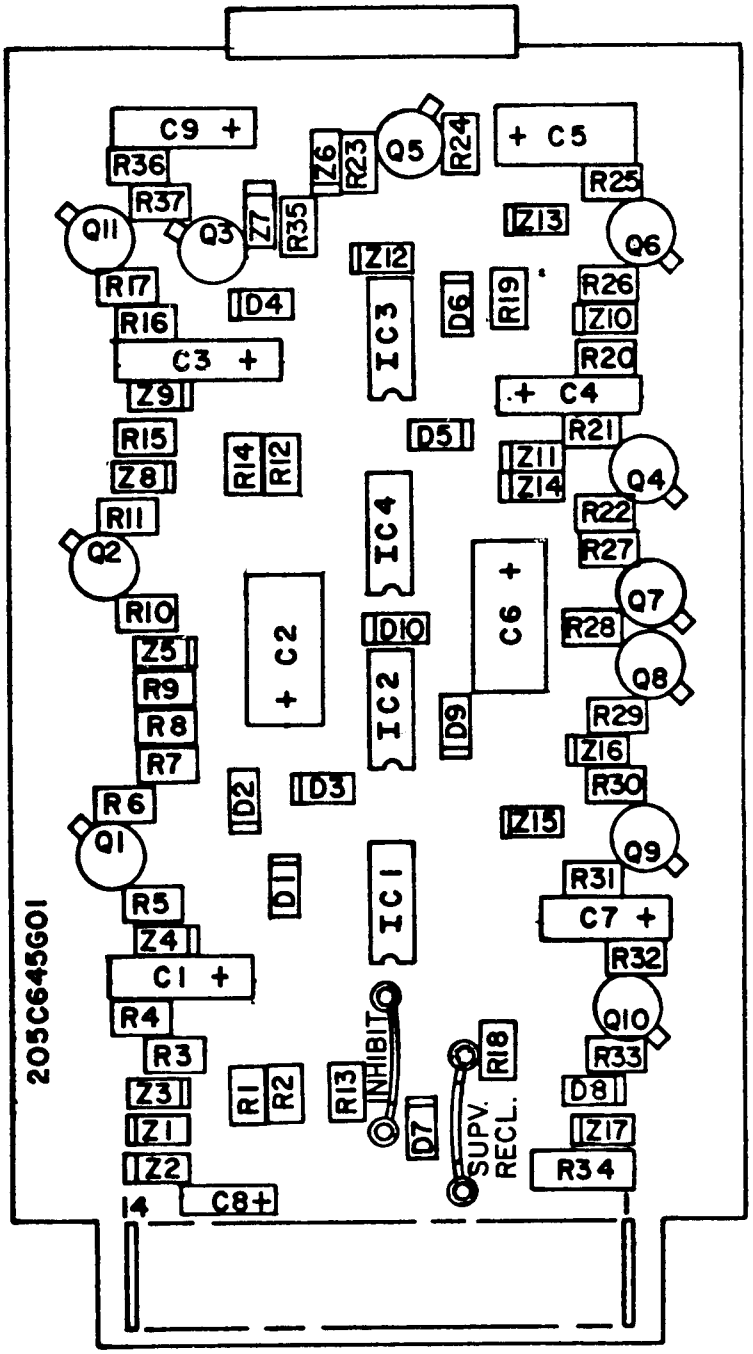
= TEST JACK

NOTES:

Δ = REMOVE 48 VOLT LINK FOR 125 VDC OPERATION ON POWER MODULE LOCATION "E".

SIGNAL STATES "0" OR "/" ARE SHOWN FOR A CONDITIONS WITH BREAKER CLOSED, 52b OPEN BOTH LINE AND BUS "HOT" AND IN SYNCHRONISM

Fig. 3. SRCU-2 Internal Logic Schematic



880A990

Fig. 25 Logic II Module (Optional) Component Location

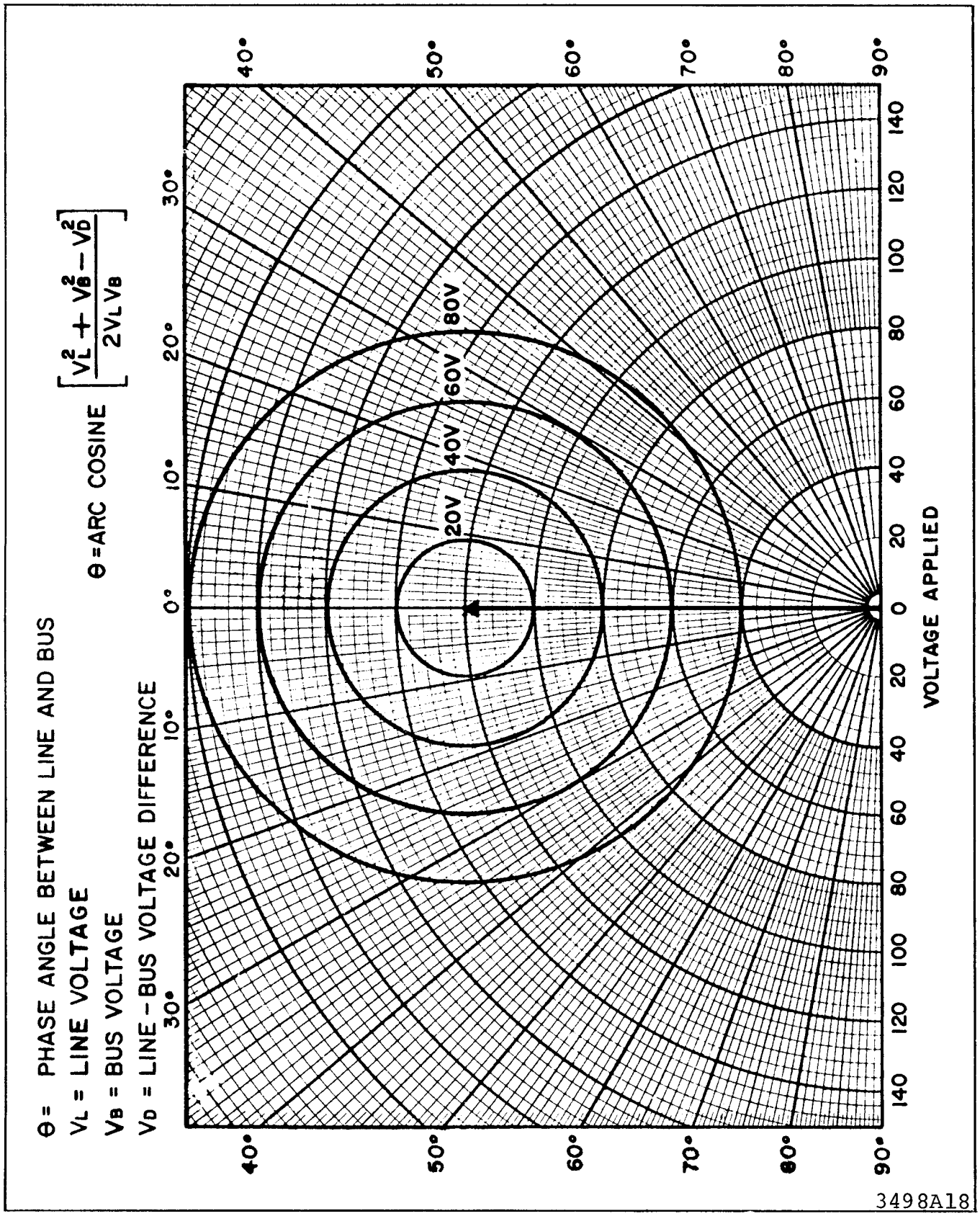


Fig. 26 Typical Voltage-Angle Characteristic of the SRCU-2 for Various Phasing Voltage Settings With Rated Voltage On One Circuit

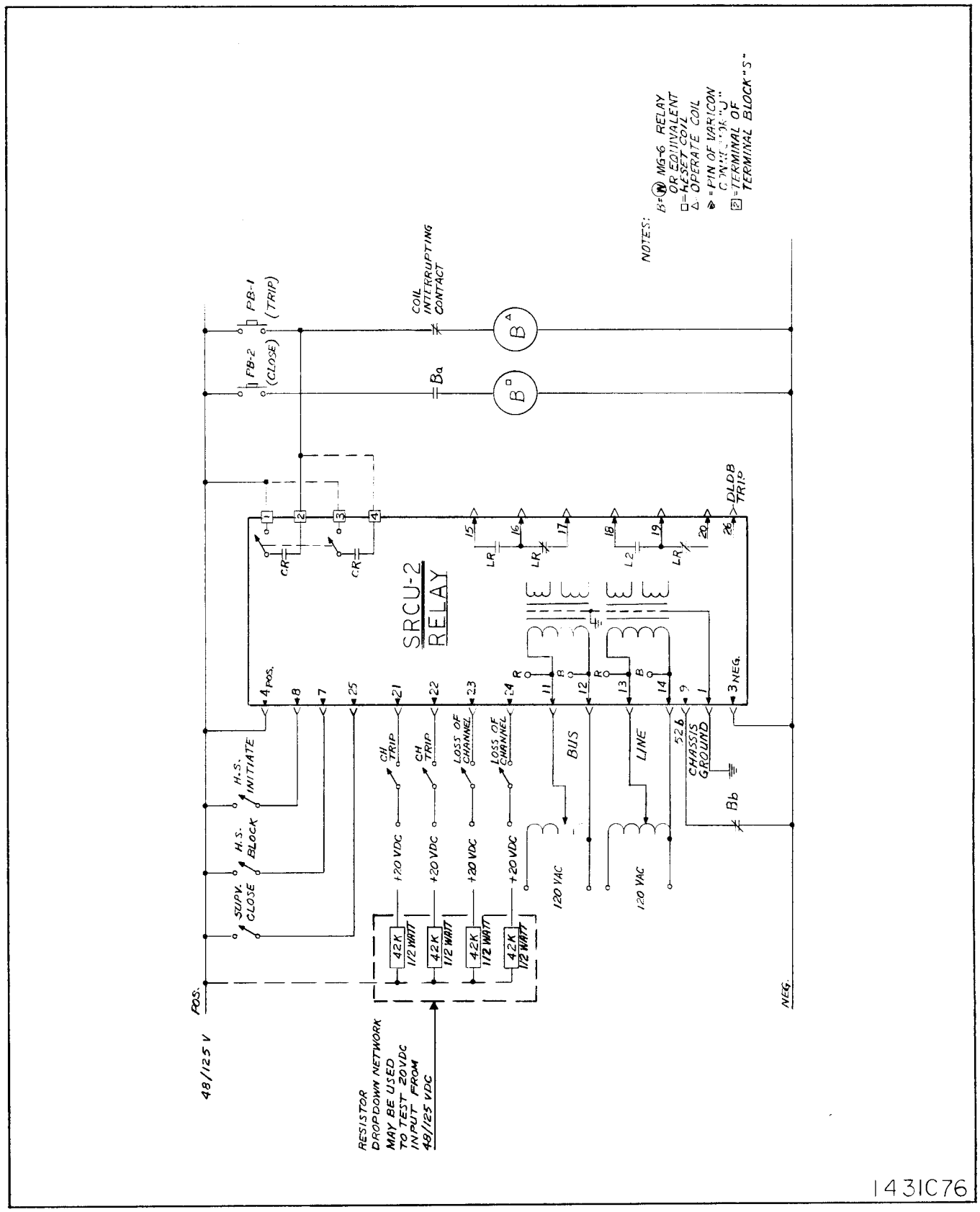


Fig. 27 Diagram of Test Connections for Type SRCU-2 Relay

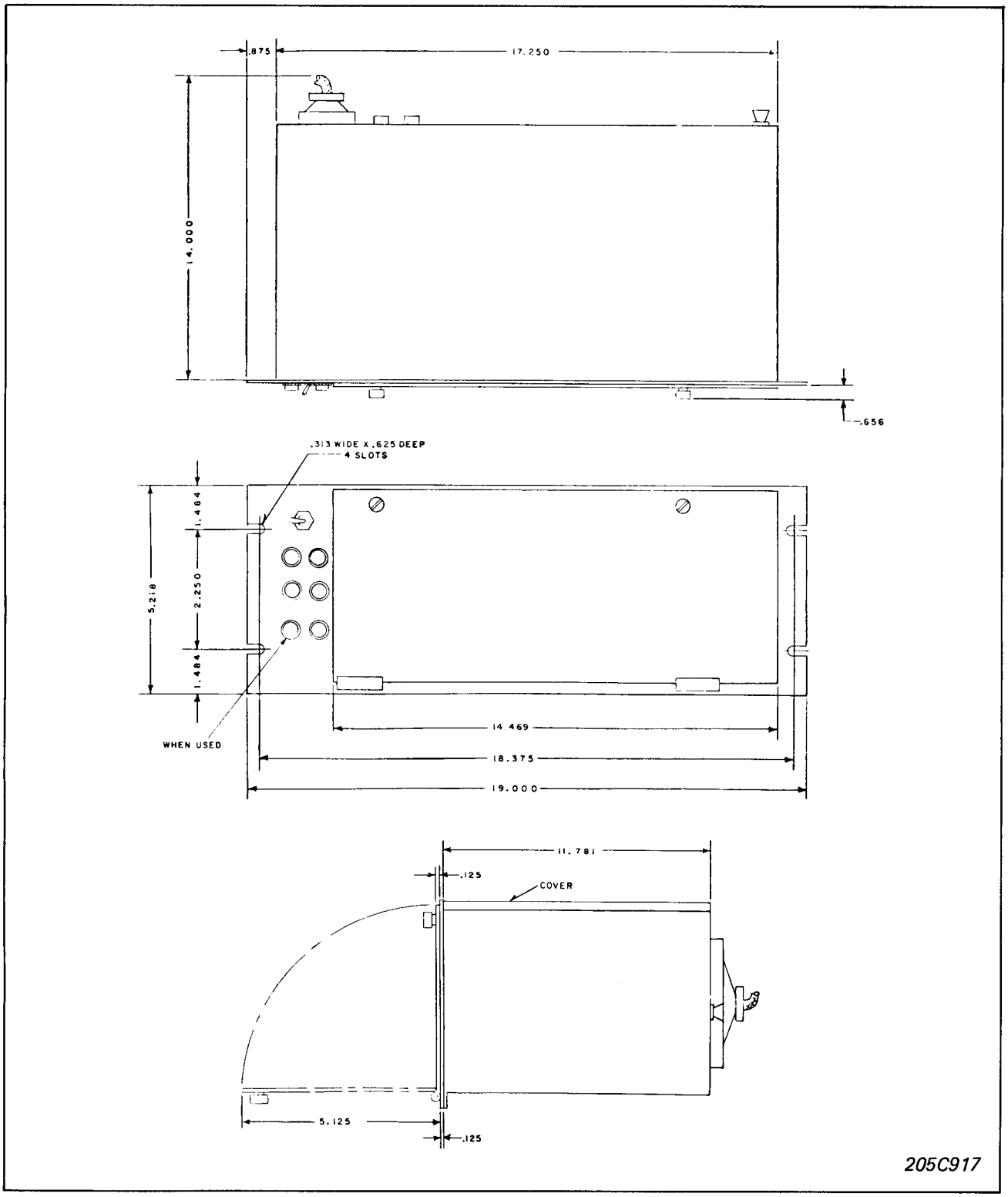


Fig. 28 Outline and Drilling Plan for Type SRCU-2 Relay

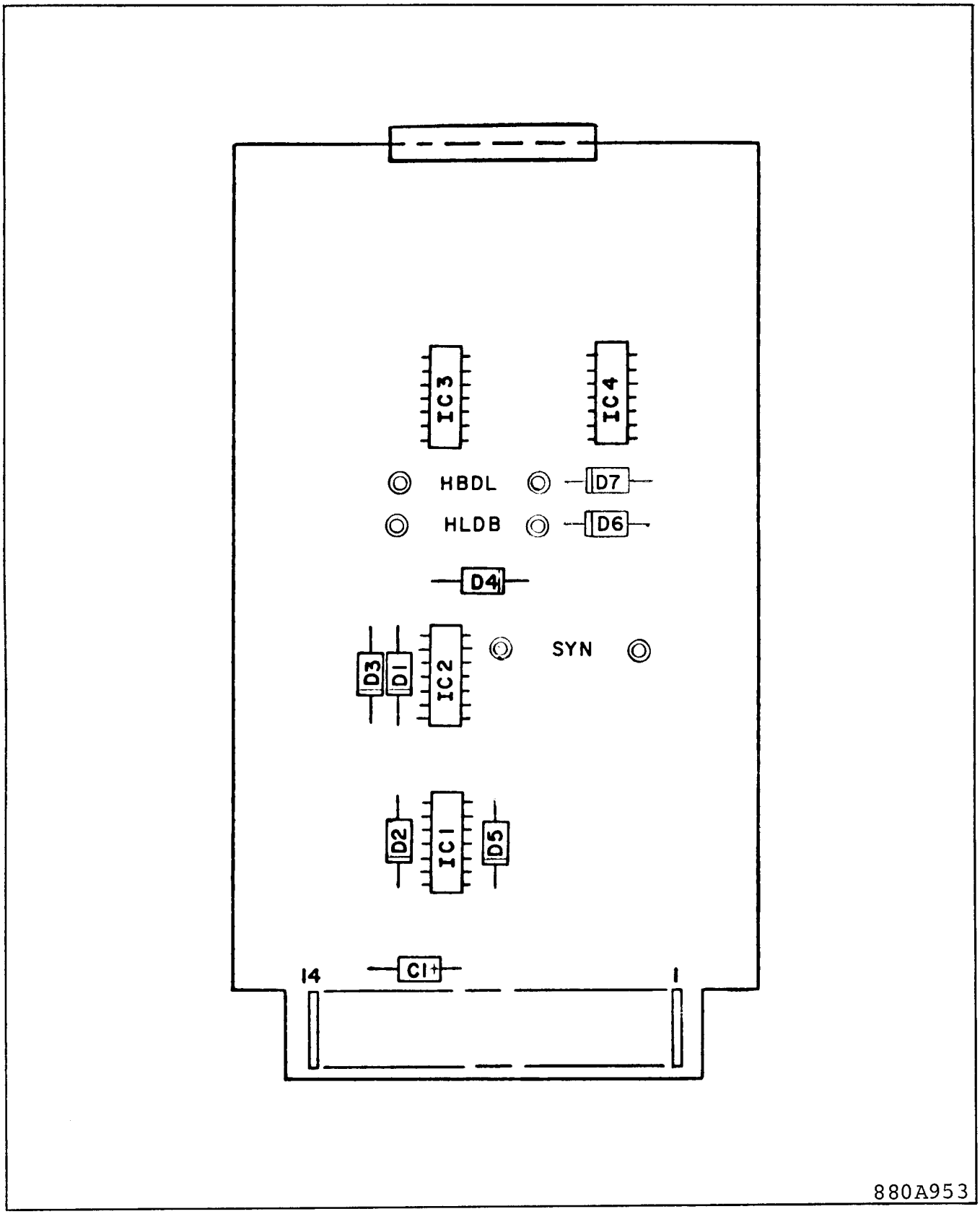


Fig. 13 Logic I Module Component Location

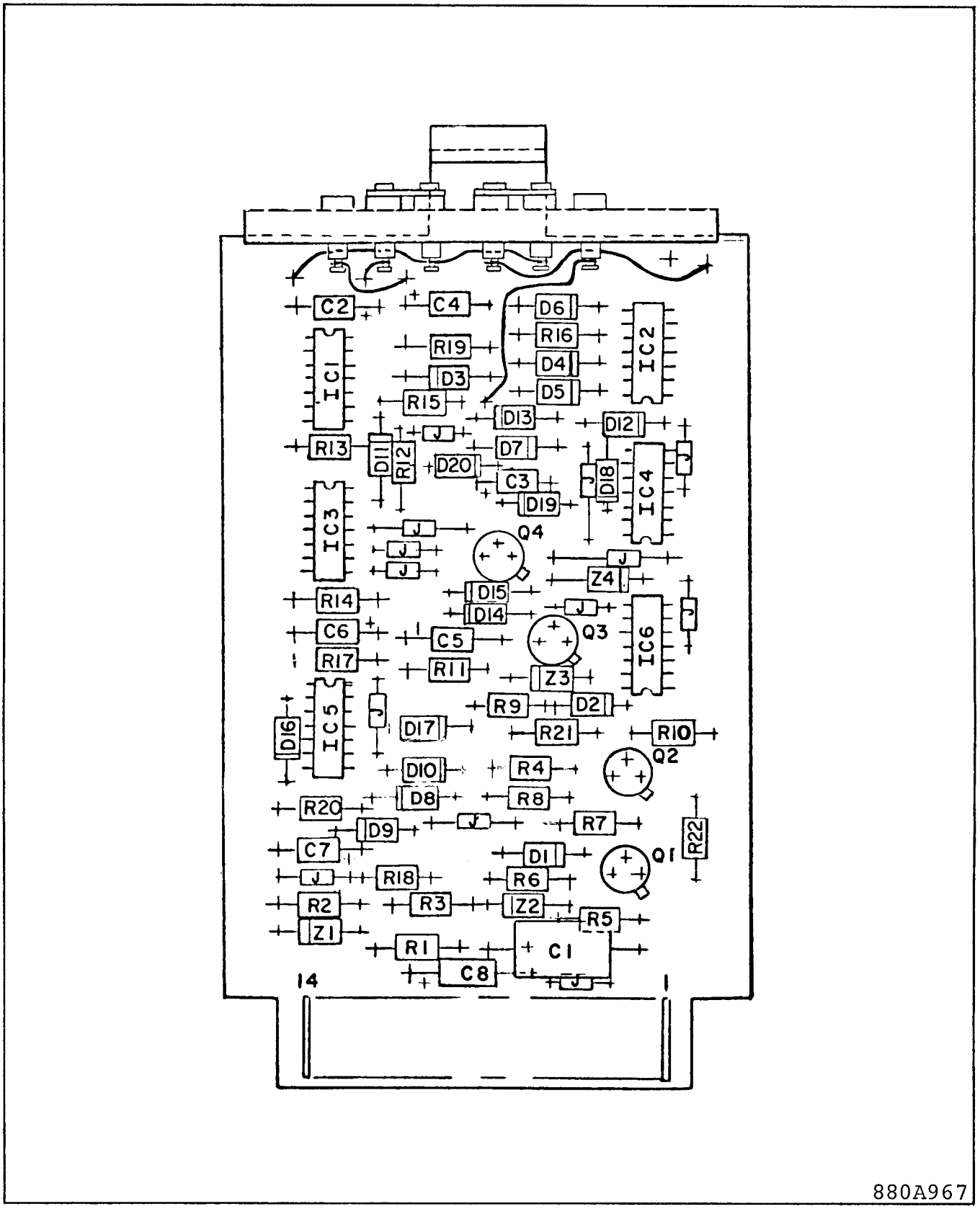


Fig. 14 Counter Module Component Location

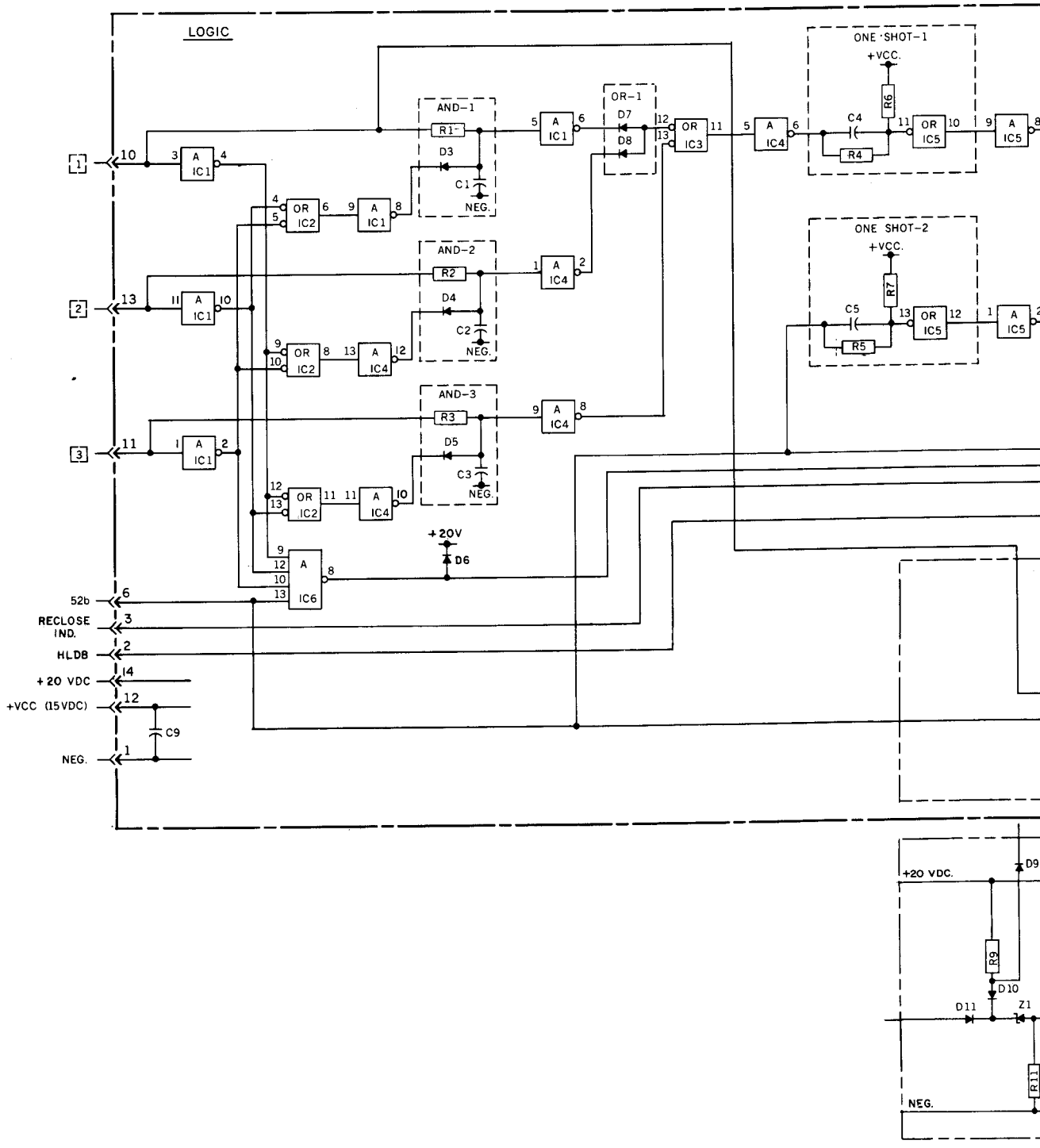
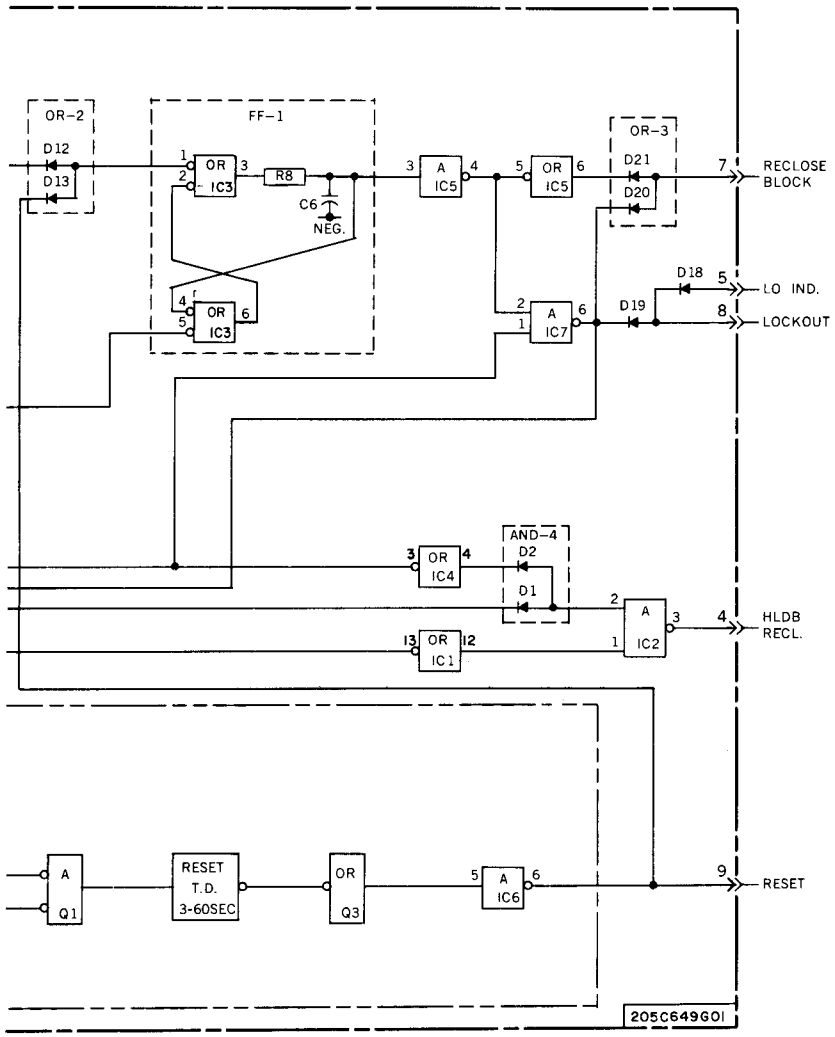
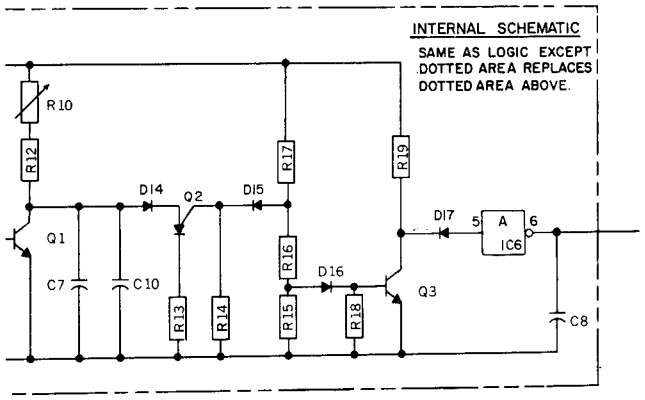


Fig. 16 Reset Mod





RESISTOR	DESCRIPTION	STYLE NO.
R1–R2–R3·R6 R7–R11–R18	10K 1/2W ±5%	184A763H51
R4–R5–R9	20K 1/2W ±5%	184A763H58
R8–R13	100Ω 1/2W ±5%	184A763H03
R12	8.2K 1/2W ±5%	184A763H49
R17	68.1K 1/2W ±1%	848A821H26
R16–R19	82K 1/2W ±2%	629A531H78
R15	100K 1/2W ±2%	629A531H80
R14	1 MEG 1/2W ±5%	184A763H99
R10	250K 1/2W ±10%	862A649H01

CAPACITOR	DESCRIPTION	STYLE NO.
C1–C2–C3	4.7MFD. 35V.	184A661H12
C4–C5	.27MFD. 200V.	849A437H02
C6	.22MFD. 60V.	187A508H22
C7–C10	150MFD. 30V.	849A007H01
C8	.01MFD. 200V.	764A278H10
C9	.47MFD. 50V.	762A680H04

DIODE	DESCRIPTION	STYLE NO.
D1 TO D21	1N4148	836A928H06

TRANSISTOR	DESCRIPTION	STYLE NO.
Q1–Q3	2N2219A	762A672H11
Q2	U13T1	878A289H01

ZENER DIO.	DESCRIPTION	STYLE NO.
Z1	IN960B	186A797H10

INT. CKT.	DESCRIPTION	STYLE NO.
IC2–IC3	MC672L	6296D58H01
IC6–IC7	MC679L	6296D58H02
IC1–IC4	MC680L	6296D58H03

COMPONENT LOCATION _ _ _ 880A969

6668D74

Ie Internal Schematic

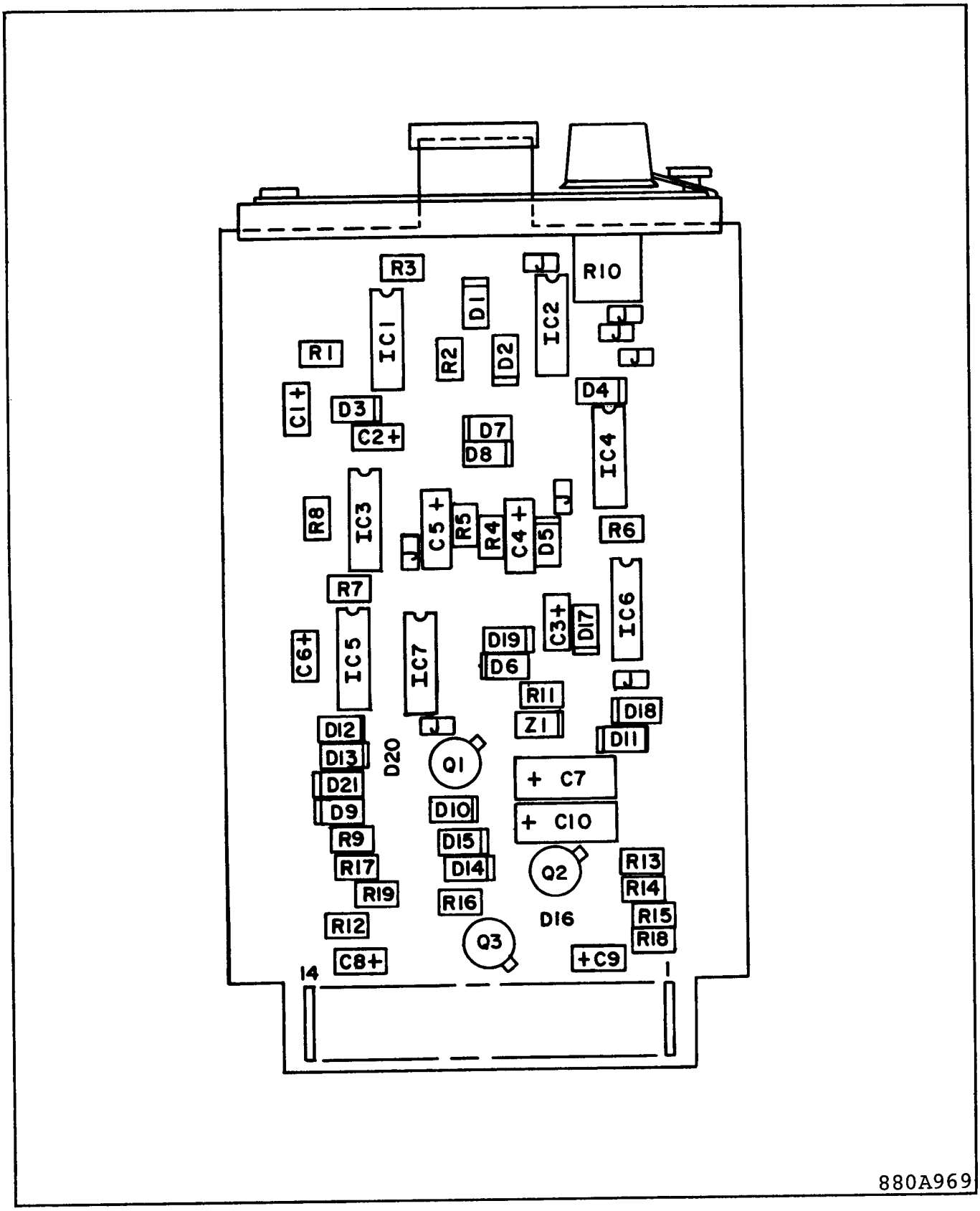
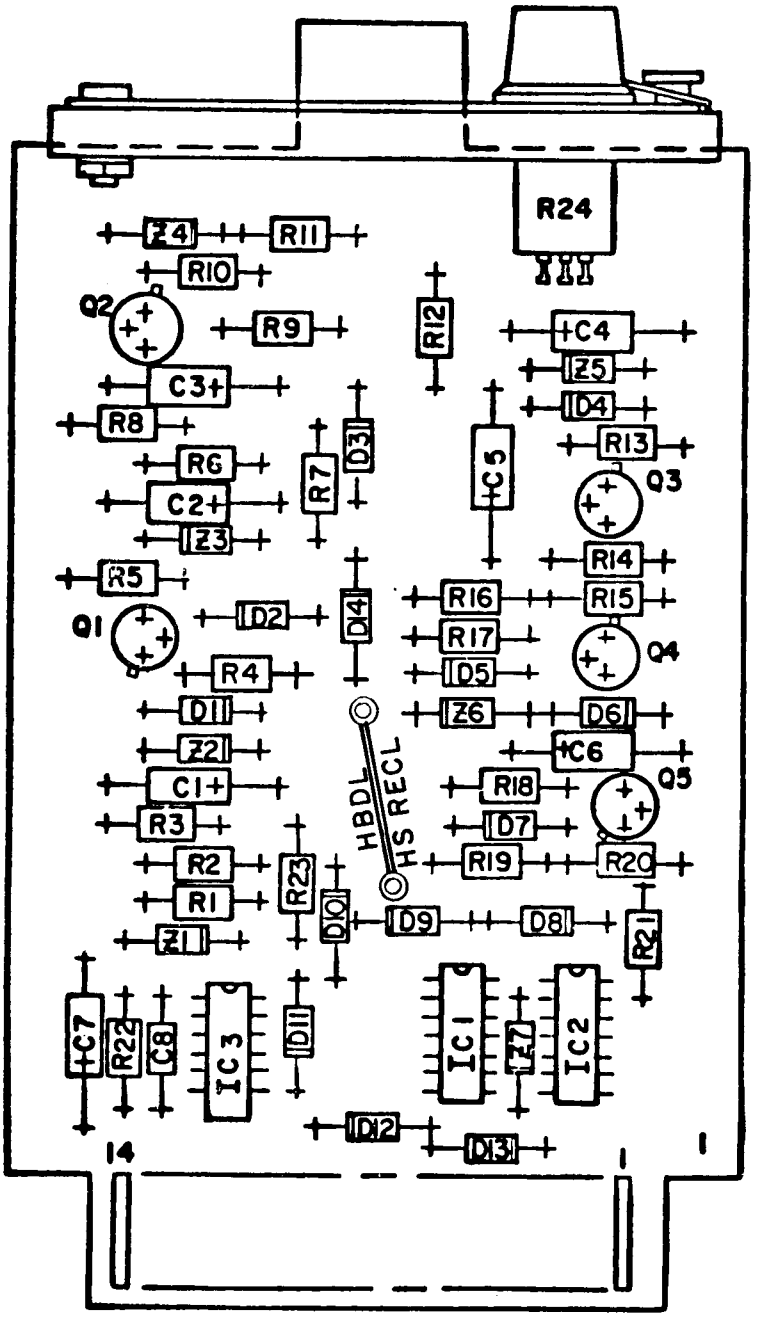


Fig. 17 Reset Module Component Location



3489A39

Fig. 18. High Speed Reclose Module Component Loc.

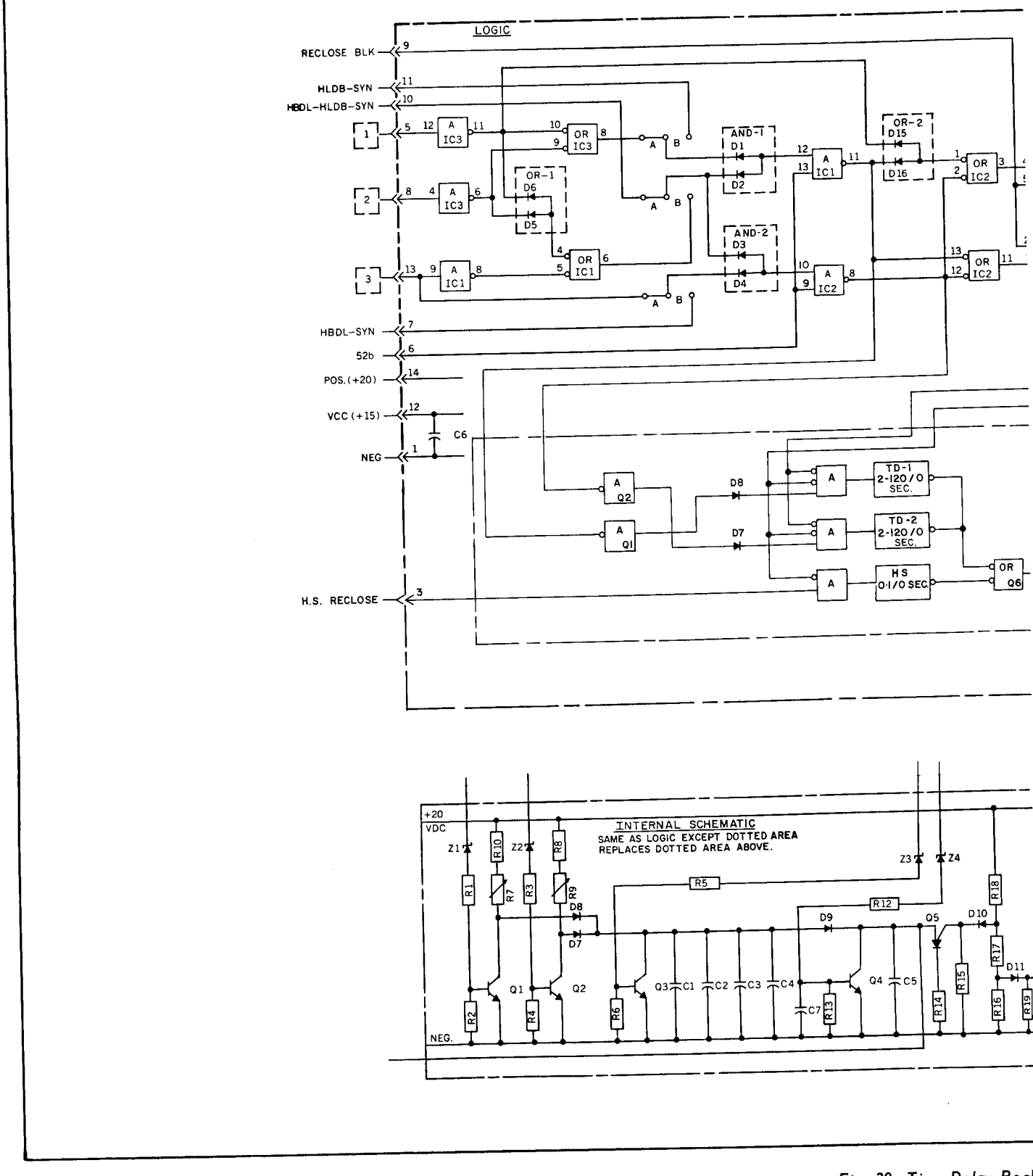
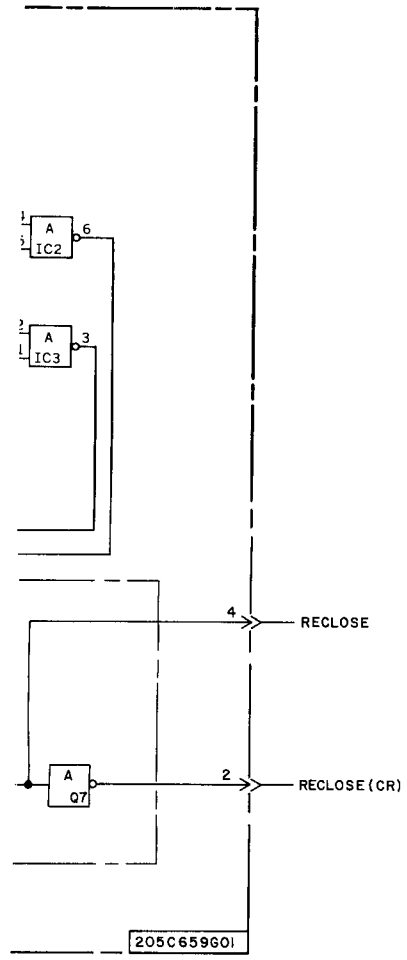
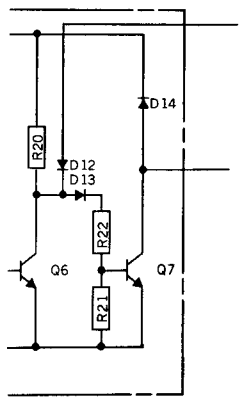


Fig. 20 Time Delay Recl





RESISTOR	DESCRIPTION	STYLE NO.
R1-3-5-12	27K 1/2W±2%	629A531H66
R2-4-6-13,21	10K 1/2W±2%	629A531H56
R8-R10	3.3K 1/2W±2%	629A531H44
R14	100Ω 1/2W±2%	629A531H08
R15	1MEG 1/2W±1%	848A822H39
R16	100K 1/2W±2%	629A531H80
R17	90.9K 1/2W±1%	848A821H38
R18	68.1K 1/2W±1%	848A821H26
R19	20K 1/2W±2%	629A531H63
R20	15K 1/2W±2%	629A531H60
R22	30K 1/2W±2%	629A531H67
POT	DESCRIPTION	STYLE NO.
R7-R9	250K 1/2W±10%	862A649H01
CAPACITOR	DESCRIPTION	STYLE NO.
C1 TO C4	150MFD 30V	862A177H05
C5	6.8MFD. 35V	184A661H10
C7	.47MFD 35V	187A508H05
C6	.47MFD 50V	762A680H04
DIODE	DESCRIPTION	STYLE NO.
D1 TO D13 D15-D16	1N4148	836A928H06
D14	1N4818	188A342H06
TRANSISTOR	DESCRIPTION	STYLE NO.
Q1 TO Q4, Q6 Q7	2N2219A	762A672H11
Q5	U13T1	878A289H01
ZENER	DESCRIPTION	STYLE NO.
Z1 TO Z4	1N957B	186A797H06
INT CKT.	DESCRIPTION	STYLE NO.
IC1 TO IC3	MC672L	6296D58H01
JUMPER	DESCRIPTION	STYLE NO.
LINK	A-B	3489A69G01
COMPONENT	0Ω	862A478H01

COMPONENT LOCATION__ 880A940

6668D76

›se Module Internal Schematic

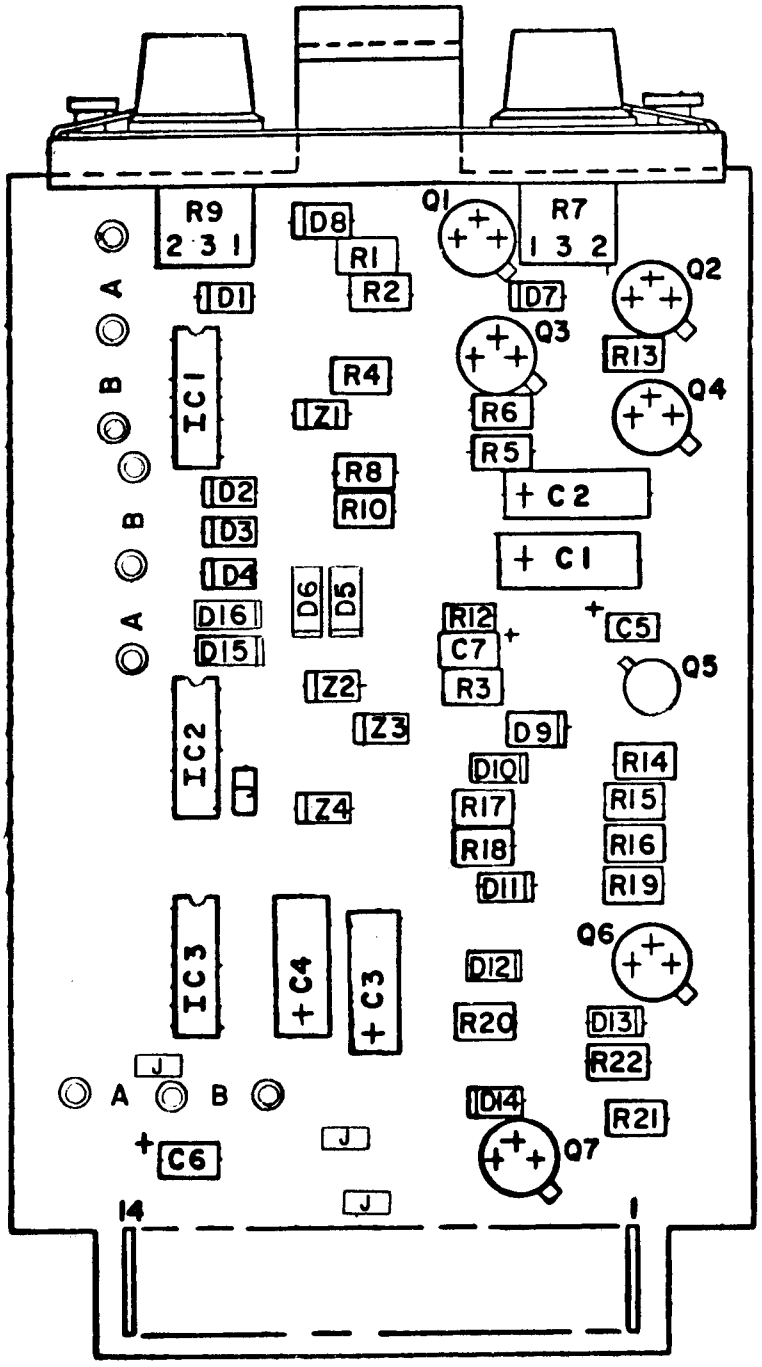
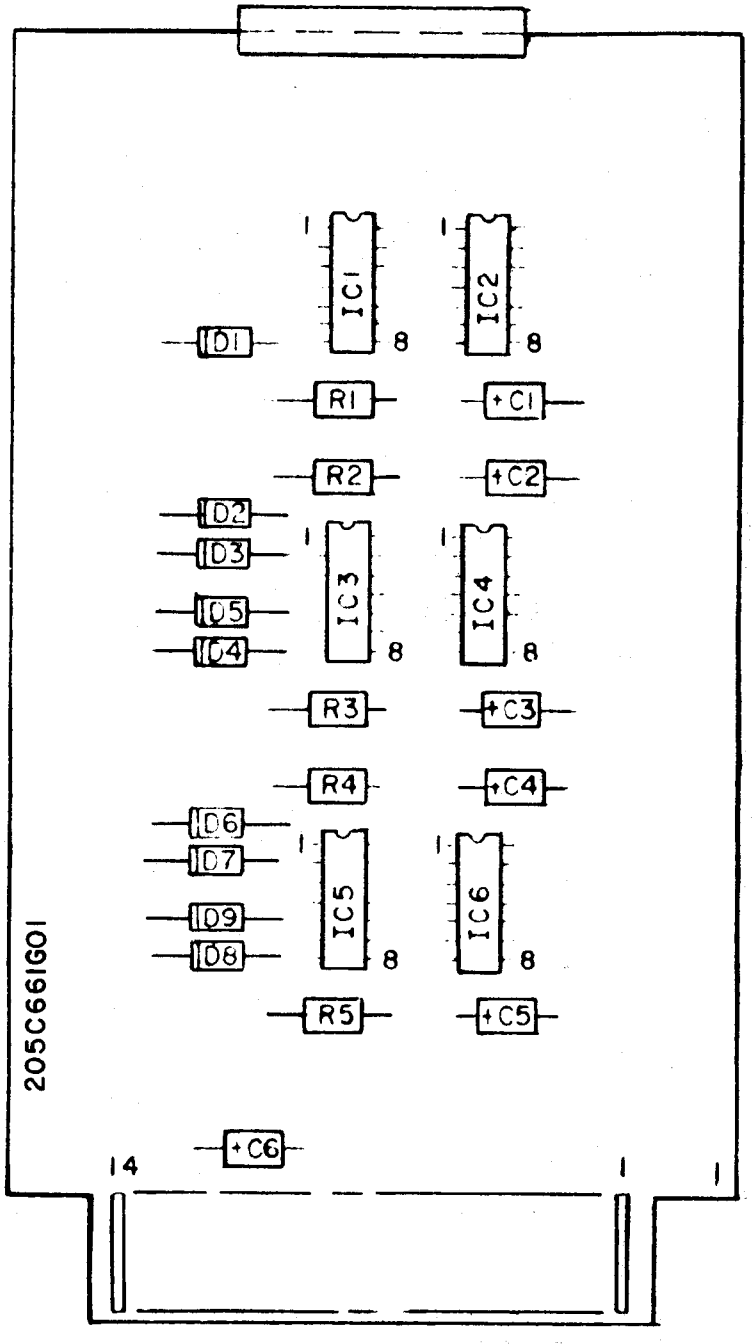


Fig. 21 Time Delay Reclose Module Component Location



880A822

Fig. 22 Indicator Module Component Location