IL41–965

INSTRUCTIONS

DIT 1 and DIT 1T Frequency-Shift Audio-Tone for Protective Relaying

WESTINGHOUSE ELECTRIC CORPORATION

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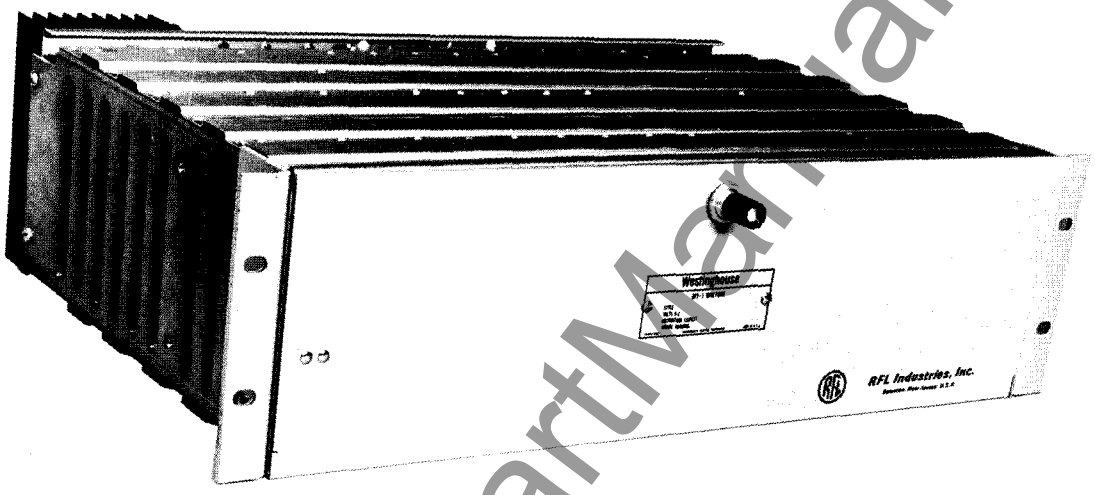


DIT-1 Frequency-Shift Audio-Tone

Introduction

The DIT-1 Tone System is a voice-frequency-carrier communication system designed especially and solely for the purpose of carrying a single command from one point to another, while simultaneously, exhibiting an unusually high degree of security against weakness that could result in either false commands or failure to deliver valid commands. Such features, in a communication system, make it especially attractive when applied for protective relaying, and the DIT-1 equipment has been designed specifically for that application. Throughout the description of the circuits, the discerning reader will sense an underlying philosophy of design that constantly trades between the often-conflicting demands for both security and dependability. Redundancy, supervisory monitoring, and logical testing for validity are used freely in the system to enhance its reliability.

The DIT-1 Tone System is a completely self-contained, solid-state, dual sub-channel system. It can be used either directly over communication circuits with self-generated voice-frequency signals, or it may be frequency translated to power-line carrier frequencies, including single-sideband systems.

Specifications

GENERAL

Primary dc Supply Voltage: 21-28 V, 42-56 V or 104-140 V dc. Power-input circuit is floating.

Power Consumption: Less than 50 watts.

Operating Temperature Range: -30^{o} to $+60^{o}$C.

Recommended Tone Frequencies: See Table 1.

Tone Input and Output: Balanced 600 ohms, adjustable links for selecting either two-wire or four-wire circuits.

Input and Output Filters: High-pass, with greater than 30 dB rejection at 50-60 Hz. A received signal at a level of −30 dBm will not be affected by an extraneous 50-60 Hz signal at the input as great at 40 V rms.

Trip-Time Delay: With transmitter and receiver connected back-to-back, trip-time delay is 12 mS with channel spacing of 340 Hz, 8 mS with spacing at 680 Hz. Shorter times are available, for permissive-trip applications, with a reduction in security.

Security and Dependability: See Figures 1 and 2.

Trip Input: Twenty to thirty milliamperes into floating, optical-isolator input, from 24, 48, or 125 Vdc source.

Trip Output: Type AR relay (10-watt) for electromechanical systems, or 18 Vdc buffers for solid-state relay systems. For details on AR relay see IL 41-759.

Block Output: Output signal is the transfer of two sets of Form-C relay contacts, each rated 2 A, 50 Vdc, resistive load. These must be derated at higher voltages. Relay de-energizes after 100 ms if abnormal signal or power failure is sensed. An 18-Vdc buffer output is available for solid-state systems.

Alarm Output: Same as Block Output, foregoing, except relay de-energizes after 2 sec.

System Reset Time: 12 mS for 340 Hz channel spacing; 8 mS for 680-Hz channel spacing.

Interface Dielectric Strength: Trip input, trip output, and tone lines are isolated from ground and from all other circuits. Breakdown is 1500 Vrms, 50-60 Hz, or 2200 Vdc.

Surge Capability: The system meets the SWC requirements of ANSI C37.90a-1974.

Dimensions and Weight: Fully contained in rack-mounted chassis conforming to EIA specifications, 5¼ inches high, 12½ inches deep, 19 inches panel width; less than 15 lbs. weight.

TRANSMITTER

Tone-Frequency Tolerance: ±0.02%, crystal controlled.

Trip-boost Level and Duration: Adjustable by using plug-in networks with ranges from 0-12 dB boost, 0-200 mS duration.

Output Level: Adjustable; −40 to +30 dBm (1 watt) for four-wire operation, −40 to +20 dBm for two-wire operation.

Harmonic Output: All harmonics in output are more than 40 dB below level of fundamental.

Amplitude Stability: Output amplitude will vary no more than ±1 dB over the specified ranges of primary input voltage and ambient temperature.

Relative Output Amplitudes: (a) Levels of guard-signal output from Channels A and B are within 1.5 dB; (b) Level difference between guard and trip output of each channel is within 0.5 dB.

RECEIVER

Sensitivity: Adjustable from −40 to 0 dBm.

AGC: Dynamic range is 22 dB.

Bandwidth: See Figure 3.

Discriminator Response: See Figure 4.

Purpose and Description

The Audio Tone System is a self-contained, solid-state, dual-channel system, with excellent security against false trip combined with dependability and good response time.

Recommended frequency assignments are shown in Table 1. The selection of precise frequencies may be quite arbitrary so long as, for one set of guard and trip signals, one frequency is taken from an "A" subchannel and paired with one from a "B" subchannel. Equipment can be supplied for operation on carrier frequencies as high as 10 kHz.

Transmitter, receiver, power supply, and all options are housed in a rack-mounted chassis illustrated in Figures 5 and 6. These illustrations show the back plate equipped with either a barrier-type terminal strip or a Varicon connector. The Model 68 Chassis contains 32 one-half-inch horizontal spaces for mounting circuit cards. Table 2 shows the horizontal space required by each module of the System. Cards may be stacked in the Model 68 Chassis up to the total of 32 one-half-inch spaces available.

As shown in Figure 5, the front door drops below horizontal for convenient access to circuit cards for testing or removal. Figure 7 details the outline of the Model 68 Chassis.

A block diagram of the system is shown in Figure 8. The two channels of the transmitter are on one circuit card. Each receiver is on a separate card which feeds both a common, shared frequency-shift (FS) and amplitude-modulation (AM) detector card, and a receiver-logic card. A separate card carries trip circuits for both transmitter input and receiver output; and the block relay and the alarm relay are mounted together on one card. An optional guard-output circuit and a transmit-flasher circuit are available on this card.

At top left of Figure 8, a trip voltage of 24, 48, or 125 Vdc is applied, through a current-limiting resistor, to two optical isolators used as input devices. Each isolator drives a separate Schmitt trigger. The high-frequency filtering and the hysteresis of the Schmitt trigger suppress transients that may be fed to the trip-input terminals from utility cables or other extraneous sources. Each keying circuit is wired out separately for test purposes. Keying circuits are connected in parallel for keying by the relay system.

The transmitter has two sub-channels each of which uses a crystal-controlled oscillator to determine output frequency on the channel on which it operates. One generates guard signal; the other generates a signal at trip frequency. Either can be gated to feed a digital frequency divider, the output of which passes through an active bandpass filter used to suppress harmonics and to deliver a pure sine wave at its output. A trip command from the output of the Schmitt trigger will gate from the guard oscillator to the trip oscillator, and it will simultaneously switch feedback resistors in the active filter to program its resonant frequency from guard to trip. This approach produces a constant-level, continuous-phase, low-harmonic sine wave signal with the stability of a crystal oscillator. Crystals and bandpass-filter frequency-determining components are plug-in units, so that field change of channel frequencies is possible.

Both sub-channels of this dual system are fed to a summing amplifier, shown at the top-right section of Figure 8. Gain of the summing amplifier can be raised upon command from a trip-logic circuit, activitated when a trip signal appears at the outputs of both Schmitt triggers. A plug-in network determines both level and time duration of the trip signal chosen to improve dependability of the system.

The summing amplifier drives an output amplifier capable of +30 dBm (1 watt) output. An adjustable attenuator, on the interface card, will bring this level to any convenient range between −40 and +30 dBm. The output of the transmitter is then fed to a line-matching circuit which can be used for either two-wire or four-wire operation.

Line-coupling transformers for both transmit and receive functions are linear toroidal units, combined with tuning capacitors to form high-pass filters with 600-Hz cutoff. They will suppress any 50-60 Hz signal that may be induced in the communication circuit. These filters will not saturate with as much as 40 volts, rms, of 50/60-Hz noise appearing at their input terminals and thus will not distort a received signal of −30 dBm.

Received signals, shown at the left of Figure 8, are fed through two bandpass filters each selected for the channel frequency of its receiver, and thence to an input amplifier with slow automatic-gain control (AGC). The dynamic range of the AGC function is usually set for 22 dB.

The input signal, leveled by the AGC action, is fed to a novel signal-level detector which has short response time and low output ripple. The leveled, incoming signal is also split into a quadrature signal. The two components then are full-wave rectified, using operational amplifier (opamp) techniques, and applied to a summing amplifier feeding a three-pole, active, low-pass filter. The signal-level detector is extremely fast and will effectively recognize both noise and weak signal, and will block before a false trip can be generated. The quadrature, full-wave-rectified signals are interleaved so that ripple frequency is doubled and ripple amplitude is reduced by 70%. This technique permits good rejection of the ripple while using a filter with fast response obtained from a higher cutoff frequency.

The input signal, leveled by AGC, is also fed to a special linear discriminator which has high rejection against noise and so avoids generating false trip signals caused by high-level interference or noise. This is a phase-shift discriminator which features high speed (short response time), good linearity, and low output ripple.

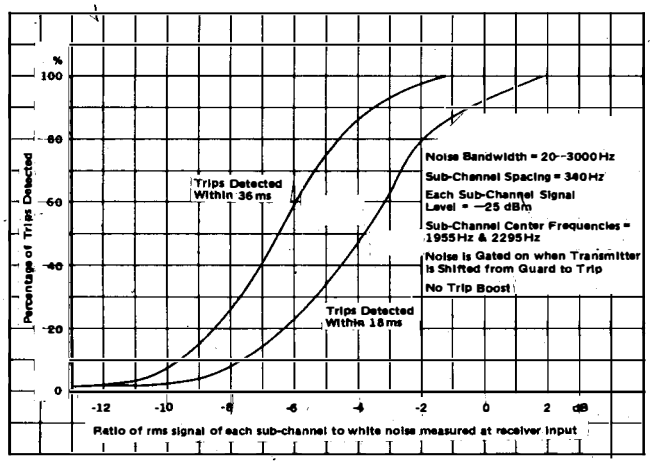


Figure 1. Dependability, 340-Hz Sub-Channel Spacing.

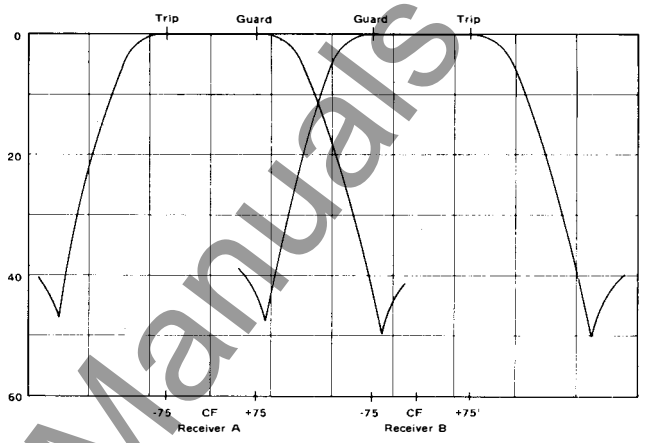


Figure 3. Typical Response, Receiver-Input Filter, 340-Hz Sub-Channel Spacing.

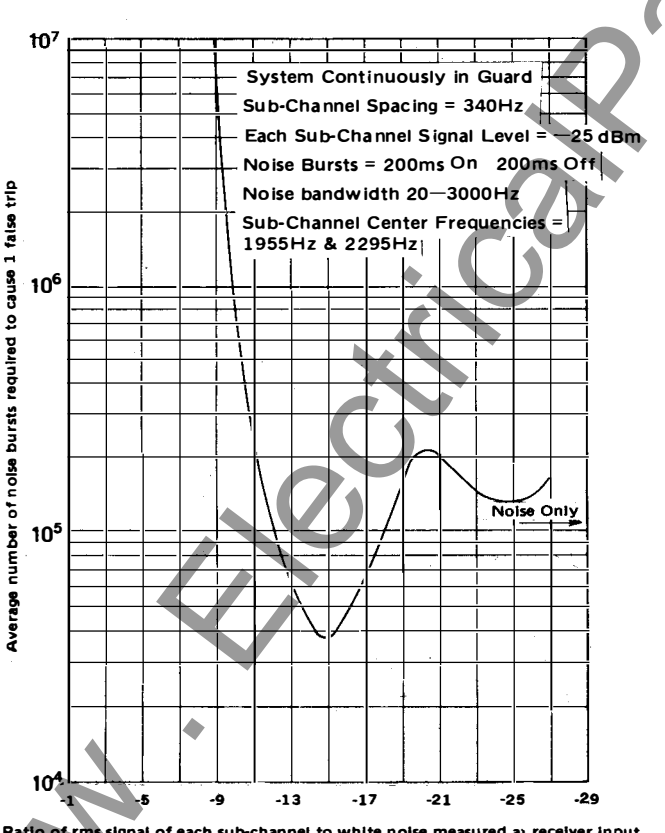


Figure 2. Security, 340-Hz Sub-Channel Spacing.

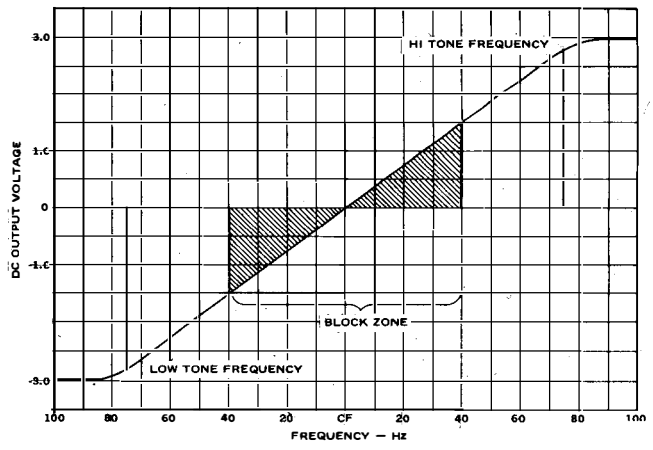


Figure 4. Typical Discriminator Response, 340-Hz Sub-Channel Spacing.

TABLE 1
RECOMMENDED TONE FREQUENCIES
340 Hz SUB-CHANNEL SPACING – 170 Hz NOMINAL BANDWIDTH

GROUP	SUB-CHANNEL	FREQUENCY & MODE	SUB-CHANNEL CENTER FREQUENCY
1	A	860 Trip 1010 Guard	935 Hz
	B	1200 Guard 1350 Trip	1275 Hz
2	A	1200 Trip 1350 Guard	1275 Hz
	B	1540 Guard 1690 Trip	1615 Hz
3*	A	1540 Trip 1690 Guard	1615 Hz
	B	1880 Guard 2030 Trip	1955 Hz
4*	A	1880 Trip 2030 Guard	1955 Hz
	B	2220 Guard 2370 Trip	2295 Hz
5*	A	2220 Trip 2370 Guard	2295 Hz
	B	2560 Guard 2710 Trip	2635 Hz
6	A	2560 Trip 2710 Guard	2635 Hz
	B	2900 Guard 3050 Trip	2975 Hz
7	A	2900 Trip 3050 Guard	2975 Hz
	B	3240 Guard 3390 Trip	3315 Hz
		680 Hz SUB-CHANNEL SPACING **340 Hz NOMINAL BANDWIDTH**	
8	A	785 Trip 1085 Guard	935 Hz
	B	1465 Guard 1765 Trip	1615 Hz
9*	A	1465 Trip 1765 Guard	1615 Hz
	B	2145 Guard 2445 Trip	2295 Hz
10	A	2145 Trip 2445 Guard	2295 Hz
	B	2825 Guard 3125 Trip	2975 Hz

**Preferred groups for minimum noise and to avoid roll-off at lower or upper end of communications channel. CCITT frequencies and spacings are available on request.*

TABLE 2
SPACE AND POWER REQUIREMENTS FOR CIRCUIT CARDS

MODEL	ASSEMBLY	DESCRIPTION	CURRENT REQUIRED		CHASSIS SPACE REQ'D.
			+12V	−12V	
68 HPS−(XXX)−1	HB-41505 (1)	Power supply, current capacity	1.0A (2)	1.0A (2)	1.5"
68 PS−(XXX)−1	HB-41500	Power supply, current capacity	0.375A (2)	0.375A (2)	1.5"
67 REC	HB-41005	Receiver, Channel A	30 mA	30 mA	1.0"
67 REC 2	HB-41005	Receiver, Channel B	30 mA	30 mA	1.0"
67 TRANS	HB-41010	Transmitter, Channels A and B	110 mA	20 mA	1.0"
67 FS/AM	HB-41015	FS/AM Detector	55 mA	55 mA	1.0"
67 LOGIC	HB-41020	Logic Card	60 mA	50 mA	1.0"
67 LOGIC	HB-41020	Logic Card (Redundant)	40 mA	10 mA	1.0"
67A INTER	HB-45790	Interface Card	0 (3)	50 mA	1.0"
67B INTER	HB-46170	Interface Card	0 (3)	50 mA	1.0"
67 RELAY	HB-41030	Block and Alarm Relay Card	0	45 mA	1.0"
67 NB REC	HB-41085	Narrowband Receiver, Channel A	60 mA	25 mA	1.0"
67 NB REC	HB-41085	Narrowband Receiver, Channel B	60 mA	25 mA	1.0"
67 BUFF	HB-41110	Buffer Card	100 mA (5)	25 mA	1.0"
67 LEVEL IND	HB-41100	Signal-Level Indicator	20 mA	40 mA	1.0"

NOTES: (1) Requires also Regulator HB-41520 mounted at back of Chassis, See Figure 6.
(2) Also delivers 10 kHz, 40 V, unregulated.
(3) Also requires 35 mA from 10-kHz output of 68 Series Power Supply.
(4) Operates directly from station battery.
(5) Requires 35 mA from 10-kHz output of 68 Series Power Supply when +18 V output required.

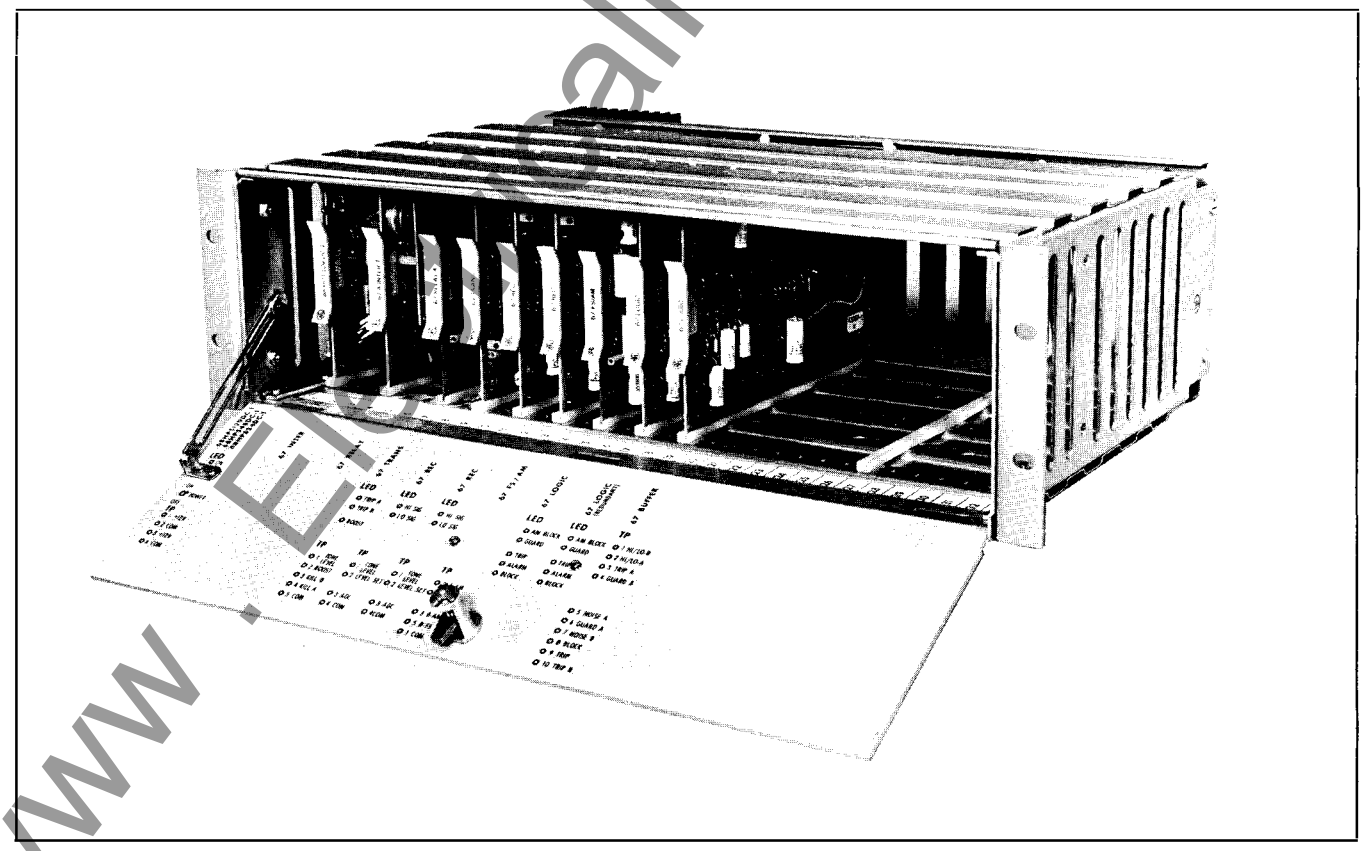


Figure 5. Card Chassis with Front Door Open.

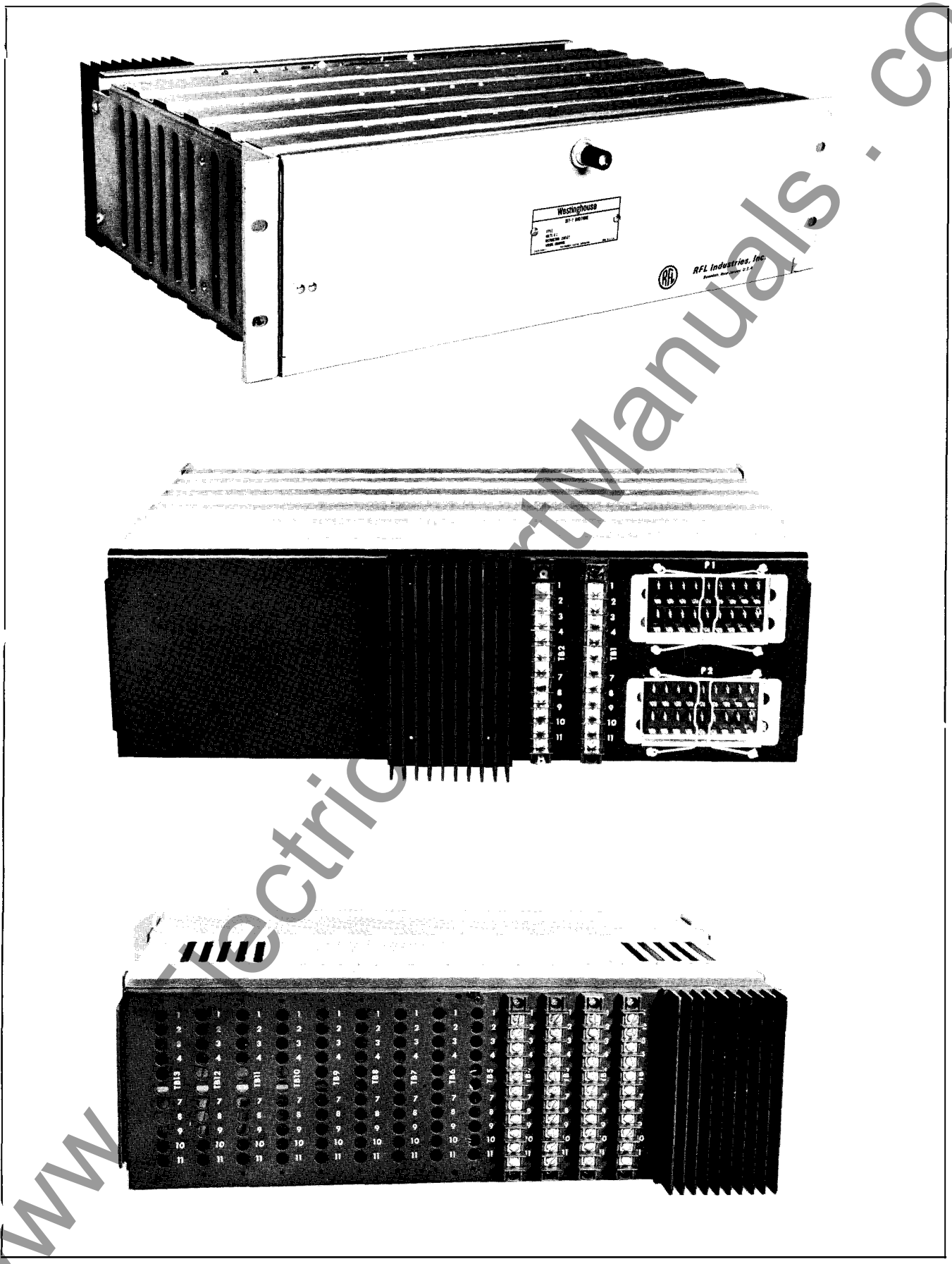


Figure 6. Typical Card Chassis

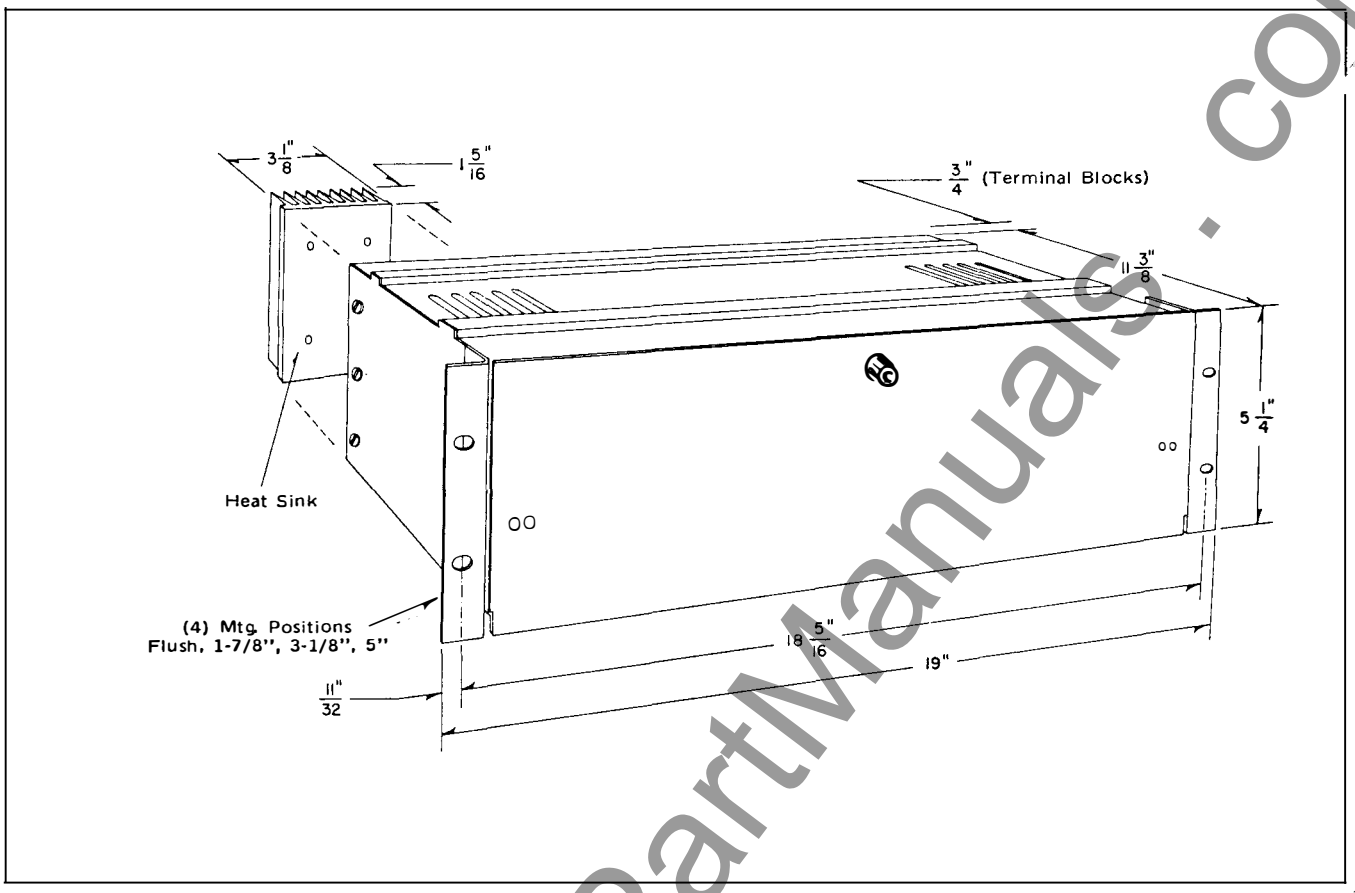


Figure 7. Outlines, Model 68 Chassis.

Each receiver sends the following signals, via the FS/AM detectors, to the receive-logic circuits, located on another card:

(a) Tone output, which is the received signal after amplification and leveling by the AGC circuits. In-band noise or interfering tones will modulate this level away from its normal value. A "dual-threshold window comparator", using voltage comparators set at the desired clipping levels for positive and negative excursions of the input signal, causes the receive-logic circuit to deliver a block-output signal when the level of the received signal reaches either the high or the low set point of the window comparator.

(b) Output from the FS discriminator, which is a dc voltage that is negative when the tone is at guard frequency, positive at trip frequency. Threshold detectors sense whether a guard or trip signal is received. A signal from the receiver near zero volts indicates that the FS discriminators are in their dead zone, that neither trip nor guard signal is being received, and this causes a block-output signal from the receiver-logic circuits.

(c) The receiver monitors the AGC-control-voltage level with detectors for both high level and low level. When beyond limits, the receiver sends an out-of-limit signal to the logic circuits which will deliver a block-output signal, as well as give a visual indication of status with lamps.

A plug-in network, located on the logic card, sets threshold levels for the AGC circuit, and for the threshold and window detectors. It is chosen to be complementary to the network used at the transmitter for trip boost.

The logic circuits monitor both received signals at all times for the following normal conditions:

(a) On the low-frequency channel, (Channel A) the guard frequency is high, and on the high-frequency channel, (Channel B) the guard frequency is low. This is the guard mode. Both window comparators sense no unacceptable noise or interference, and received-signal levels are within limits — neither too high nor too low. Or, . . .

(b) On the low-frequency channel, the trip frequency is low, and on the high-frequency channel the trip frequency is high. This is the trip mode. Level is either boosted, or not boosted, as predetermined when the system was set up. Window comparators detect no unacceptable noise or interference, and signal levels are within prescribed limits.

If neither condition (a) nor (b), foregoing, prevails, or if (b) is not immediately preceded by (a), trip output will be inhibited by block output or alarm output.

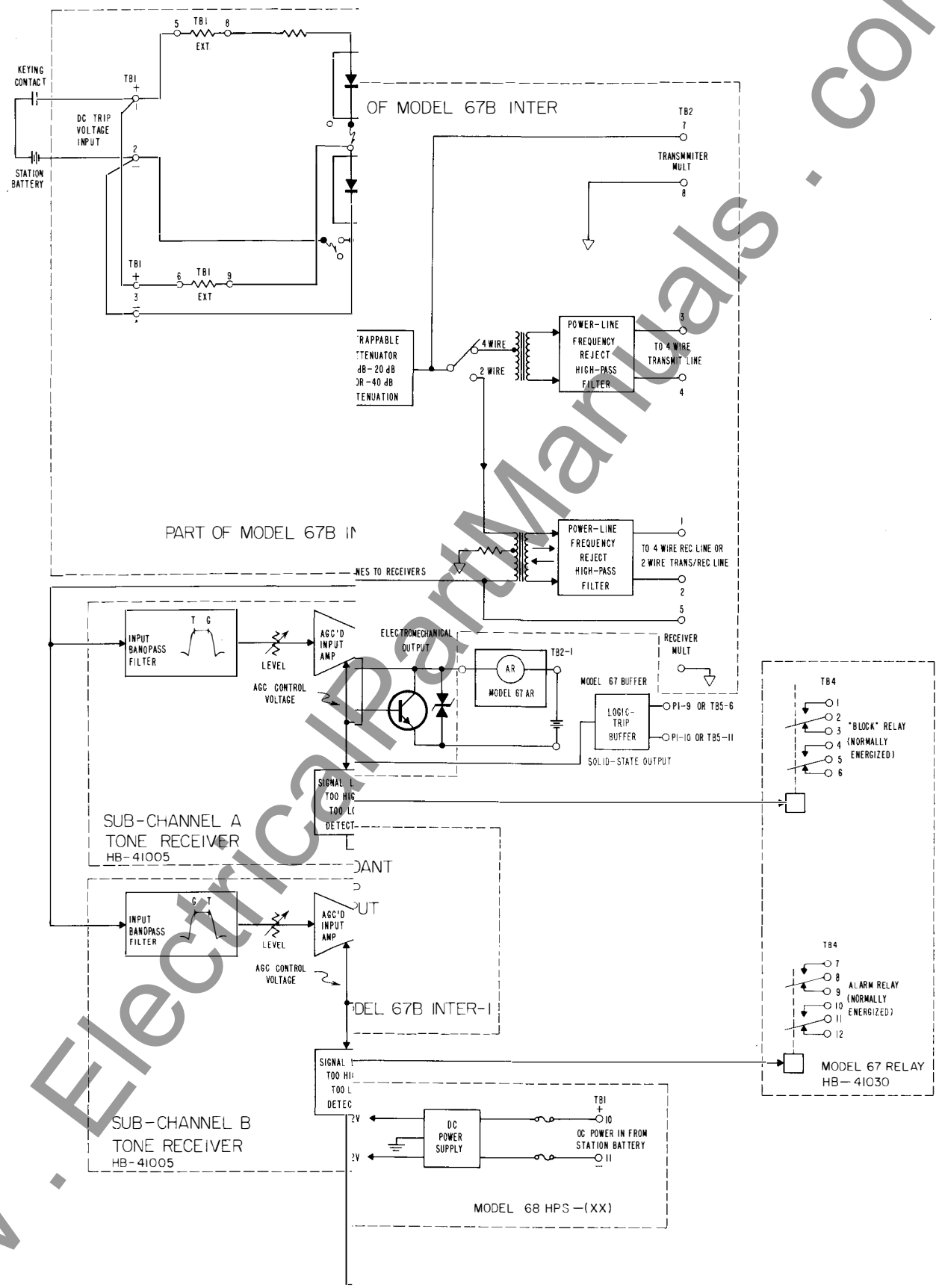


Figure 8. Block Diagram Protective Relaying System.

Trip output can be inhibited by noise, by interference, by frequency translation, or if guard has been absent more than 100 mS prior to receipt of trip. The inhibition will be removed only after guard has been received for 100 mS, or more, when the jumper on the Model 67 LOGIC card is set in the G/T position. If any abnormal condition persists for 100 mS or more, or if other abnormalities exist, such as loss of signal or wrong disposition of guard and trip frequencies, a block condition will occur that can be removed only by return to the guard state for at least 100 mS. This is the guard-before-trip feature of the system. When the block condition occurs, a relay de-energizes; and if the block persists for two seconds the alarm relay will de-energize.

For permissive-trip applications, the receive-logic circuits can be connected to defeat conditionally the guard-before-trip requirement. High security, however, is maintained because guard signal must still precede the first trip, after which guard signal need no longer precede trip signal to initiate a subsequent trip, providing that an invalid signal does not occur between trips. If guard signals are received, the guard-before-trip requirement is again restored. This occurs when the jumper on the Model 67 LOGIC is set in the T position.

To provide for the condition where a valid trip signal is received and accepted by the logic, but is not sustained long enough, perhaps because of failure of the communication circuit, to have the command executed, an optional trip-hold timer is available. Its hold time may be selected between zero and 250 mS.

Finally, the trip circuit drives an optical isolator which, in turn, delivers base-drive current to an NPN transistor switch. This floating electronic switch is capable of up to one ampere collector current, which is used to drive an AR relay. For solid-state relay systems, the trip-buffer output is driven directly from the logic card.

Bibliography

(1) Bell System Technical Reference, PUB-41004, *Transmission Specifications for Voice Grade Private Line Data Channels.*

(2) Bell System Technical Reference PUB-41011, *Transmission Specifications for Voice Grade Private Protective Relaying Channels, May 1973.*

(3) L. R. Berke, E. W. Geer, Jr., D. R. Tucker, *Staged Fault Testing of Leased Audio Tone Relaying Channels Subject to Ground Potential Rise and Induced Voltage* — Proceeding of the IEEE, International Communications Conference, 1972.

(4) L. R. Berke, E. W. Geer, Jr., M. Parente, T. L. Berri, *Audio Tone Relaying Tests on Telephone Channels in the Presence of Induced Voltage* — IEEE Trans. on Communication, Vol. COM-20, No. 3, June 1972.

(5) *IEEE Guide for Surge Withstand Capability (SWC) Tests ANSI C37.90a–1974* — IEEE Std 472-1974.

DIT-1 PROTECTIVE RELAYING MODULE DESIGNATION	HB-41005 Receiver	HB-41010 Dual Transmitter	HB-41015 FS/AM Detector	HB-46170 Interface Card	HB-41080 Second Trip Out	HB-41505 1A P/S–129VDC	HB-41515 1A P/S–48VDC	HB-41935 1A P/S–24VDC	*HB-41520 P/S Regulator	HB-41535 Overvoltage Protection				
67 REC	•													
67 TRANS		•												
67 FS/AM			•											
67B INTER				•										
67B INTER–1				•	•									
68 HPS 129 DC–1						•			•	•				
68 HPS 48 DC–1							•		* •	•				
68 HPS 24 DC–1								•	* •	•				
68 REG									•					

67 Buffer HB-41110 Buffer Card

68 CHAS – HB-41140 – 5¼" Chassis

MOD WIRING – HB-41138 – Module Wiring

68 EXT – HB-39585 – Card Extender

This regulator is a module separate from the power supply, but is always required except when ordering spare or replacement modules.

DIT-1 PROTECTIVE RELAYING MODULE DESIGNATION	HB-41020 Logic Card	Alarm Relay	Block Relay	HB-41040 Guard Out	HB-41039 Flasher	HB-41085 Narrowband Rec.	HB-24311 Merc. Guard Rel.							
67 LOGIC	•													
67 RELAY		•	•											
67 RELAY–1			•											
67 GUARD OUT–2				•			•							
67 RELAY–4		•	•	•	•		•							
67 RELAY–5		•	•		•									
67 RELAY–6		•	•	•			•							
67 RELAY–7		•			•									
67 RELAY–9		•	•	•	•									
67 NB REC						•								

67 TRIP RELAY–1: w/AR 125 VDC–4M

67 TRIP RELAY–2: w/AR 48 VDC–4M

67 TRIP RELAY–3: w/AR 125 VDC–2M/2B

67 TRIP RELAY–4: w/AR 48 VDC–2M/2B

67 T/G RELAY–1: w/AR 125 VDC–2M/2B (DUAL)

STANDARD 6745 ASSEMBLY CONSISTS OF: (2) 67 REC, (1) 67 TRANS, (1) 67 FS/AM, (1) 67B INTER, (1) 67 LOGIC, (1) 67 RELAY, (1) 68 HPS –– DC–1, (1) 68 CHAS.

DUAL LOGIC ASSEMBLY is same as above except add (1) LOGIC and substitute (1) 67B INTER–1 for 67B INTER.

Installation

CAUTION: *If the tone set is mounted in a cabinet, it must be bolted down to the floor, or otherwise secured, before swinging out the equipment rack, to prevent its tipping over.*

General: The standard chassis used for the DIT-1 System was described in the foregoing. Each chassis requires three standard 1¾-inch relay rack spaces in a 19-inch wide relay rack. Each chassis contains the complement of modules needed for the application specified, and each is individually wired for that application. Complete systems comprising a number of chassis may be ordered as assemblies mounted in relay-rack cabinets; and in such cases the assembly is shipped as a unit, mounted in a wood crate, in a horizontal position.

Unpacking the Equipment: Individual chassis are shipped in commercial packing cartons, one per carton. Care should be taken when opening to ensure that the equipment is not damaged or scratched. Carefully examine all packing material so that items of value are not discarded. Any packing material used in the chassis to keep modules in place during transportation should be removed carefully.

The 5¼-inch high chassis is fitted with a hinged front door. Access to the modules is gained by turning the locking screws counterclockwise until the door can be opened. The 1¾-inch chassis has a removable front panel, and access to the modules is the same.

Chassis-mounting ears can be positioned so that the front panel is either flush or forward-mounted with respect to the vertical supporting channels of the rack. Two sets of mounting holes for these ears are provided. By reversing the mounting ears in either set of holes, four choices of position are available.

Care should be taken, when running the trip-input leads, to reduce the possibility of a false trip caused by induced currents in the trip leads. It is recommended that the trip-input leads be a shielded, twisted pair, with the shield grounded at both ends. Refer to "Silent Sentinels", Publication 72-1, for recommended protection practices.

Ventilation: To enhance reliability, the equipment should be operated within the range of ambient temperature specified. Ventilation should be provided to ensure that limits set for ambient temperature are not exceeded within the enclosure in which the equipment is mounted.

Electrical Connections: Connections to either type chassis are made through barrier-type terminal blocks, or Varicon connector, mounted on the rear. Details of input and output connections are shown in the accompanying drawings at the end of this section.

Table 4 is a tabulation of part numbers for all frequency-dependent components for both Transmitter and Receiver, for all standard operating frequencies.

Table 5 lists the standard choices for network RZ3, used to establish the level of the transmitted signal, including non-boost, during both guard and trip, and the standard choices for network RZ16, mounted on the logic card, used to establish signal levels from the three output circuits of the receiver. Other choices can be supplied.

TABLE V

PART NUMBERS FOR STANDARD LEVEL NETWORKS

FUNCTION		TRANSMITTER (RZ3)	RECEIVER (RZ16)
LEVEL	PULSE DURATION MILLISECONDS		
Non-Boost		HB-41066-1	HB-41067-1
3 dB Boost	70	HB-41066-2	HB-41067-2
6 dB Boost	70	HB-41066-4	HB-41067-4
9 dB Boost	70	HB-41066-5	HB-41067-5
12 dB Boost	70	HB-41066-3	HB-41067-3

Set-up Procedure: All connections to the equipment are made on terminal blocks at the rear of the chassis. These terminals appear in Figure 6. Details are shown on the chassis-wiring drawing supplied with each individual system; and that drawing number is stamped on the back of the chassis. The following procedure then applies:

(1) Connect the primary-power supply, either 24, 48, or 125 Vdc, as appropriate, to TB1, Pins 10 and 11. Pin 10 is positive.

(2) To trip the Transmitter, apply 24, 48, or 125 Vdc to Pins 1 and 2. Pin 1 is positive.

(3) To detect a trip from the Receiver, apply 24, 48, or 125 Vdc in series with either a lamp or relay to TB3, Pins 1 and 2. Pin 1 is positive. See Figures 12, 13, and 14.

(4) The Transmitter-output signal is on TB2, Pins 3 and 4; 600 ohms balanced.

(5) The Receiver input is on TB2, Pins 1 and 2, 600 ohms balanced.

(6) Connect the output of the Transmitter (see (4) foregoing) either to the communication system to be used, or to an adjustable attenuator if Transmitter and Receiver are to be tested locally.

(7) Connect the Receiver input (see (5) foregoing) to the output of the communication system or of the attenuator.

(8) Output level of the Transmitter is adjusted with the potentiometer on the front of the Transmitter card, Model 67 TRANS.

(9) Sensitivity of the Receiver is adjusted with the potentiometer on the front of the Receiver card, Model 67 REC.

(10) Connect an RMS voltmeter to the input of the Receiver at TB2, Pins 1 and 2.

(11) Turn on power.

(12) Adjust the Transmitter's output for −10 dBm. If a communication system is being used, adjust the output level of the Transmitter so that it will drive the system properly.

(13) The level of the received signal at the input to the Receiver, TB2, Pins 1 and 2, should be about −20 dBm.

(14) Drop the level of the received signal by 10 dB, so that it is −30 dBm.

(15) Adjust the sensitivity control of each Receiver until the low-level indicator of each Receiver just goes out.

(16) Return the level of received signal to −20 dBm. The Receivers are now adjusted so that a signal at −20 dBm is in the middle of the dynamic range of the AGC system.

(17) There should be only two lamps lighted, one on the Power Supply, and the guard-signal indicator on the Model 67 LOGIC. If trip boost is used, however, the AM-block lamp on the Logic card also will be lighted.

EXTERNAL CONNECTIONS TO CHASSIS

Connections to Communication Circuit			
MODE (1)	FUNCTION	CONNECTIONS	
		DIT−1	DIT−1T
2-Wire	Transmit and Receive	P1−13, 14	TB2−1 & 2
4-Wire	Receive	P1−13, 14	TB2−1 & 2
	Transmit	P1−11, 12	TB2−3 & 4

(1) Be sure that jumpers A, B, C, D, and E on Model 67 INTER (Interface Card) correspond to mode selected.

TABLE 6

MAXIMUM BOOST LEVELS AND DURATIONS

BOOST LEVEL	BOOST TIME					
	70 ms	75 ms	100 ms	125 ms	150 ms	Units
3 dB	−.112 .977 .765	−.124 .975 .764	−.158 .967 .761	−.192 .960 .758	−.227 .952 .755	dBm mW volts
6 dB	−.308 .934 .748	−.331 .930 .746	−.424 .909 .738	−.531 .888 .729	−.615 .869 .722	dBm mW volts
9 dB	−.663 .859 .718	−.712 .851 .714	−.921 .810 .697	−1.123 .774 .681	−1.316 .740 ..666	dBm mW volts
12 dB	−1.316 .740 .666	−1.395 .727 ..660	−1.771 .666 .632	−2.122 .615 .607	−2.443 .571 .585	dBm mW volts
	This table represents the maximum level that may be sent over a 600 ohm phone-line without violating the Bell System 3-SEC. Rule.					

TABLE 7
PLACEMENT OF JUMPERS

MODULE	ACTION AT INSTALLATION
67 Receiver	Jumper for slow AGC must be in place when trip boost is used, absent in non-boost condition.
67 Transmitter	Select level network from Table 5 and install on transmitter card.
67 FS/AM Detector	Standard practice is to install Jumpers A, C, F, and G, although non-standard applications may require other arrangements.
67 Logic	Placement of G/T jumper is determined following settlement of the options given in the first and second paragraphs on page 13.
67B Interface	Set Jumpers G and H to single or dual trip, as required. Set Jumpers A, B, C, D, and E for two-wire or four-wire operation as indicated on the schematic for this card. For multiplex operation, refer to Figures 9 and 10.
67 Buffer	Jumper is connected from G to E when single logic card is used, or from G to F when redundant card is used.
Note	In operating systems supplied by the factory jumpers are installed.

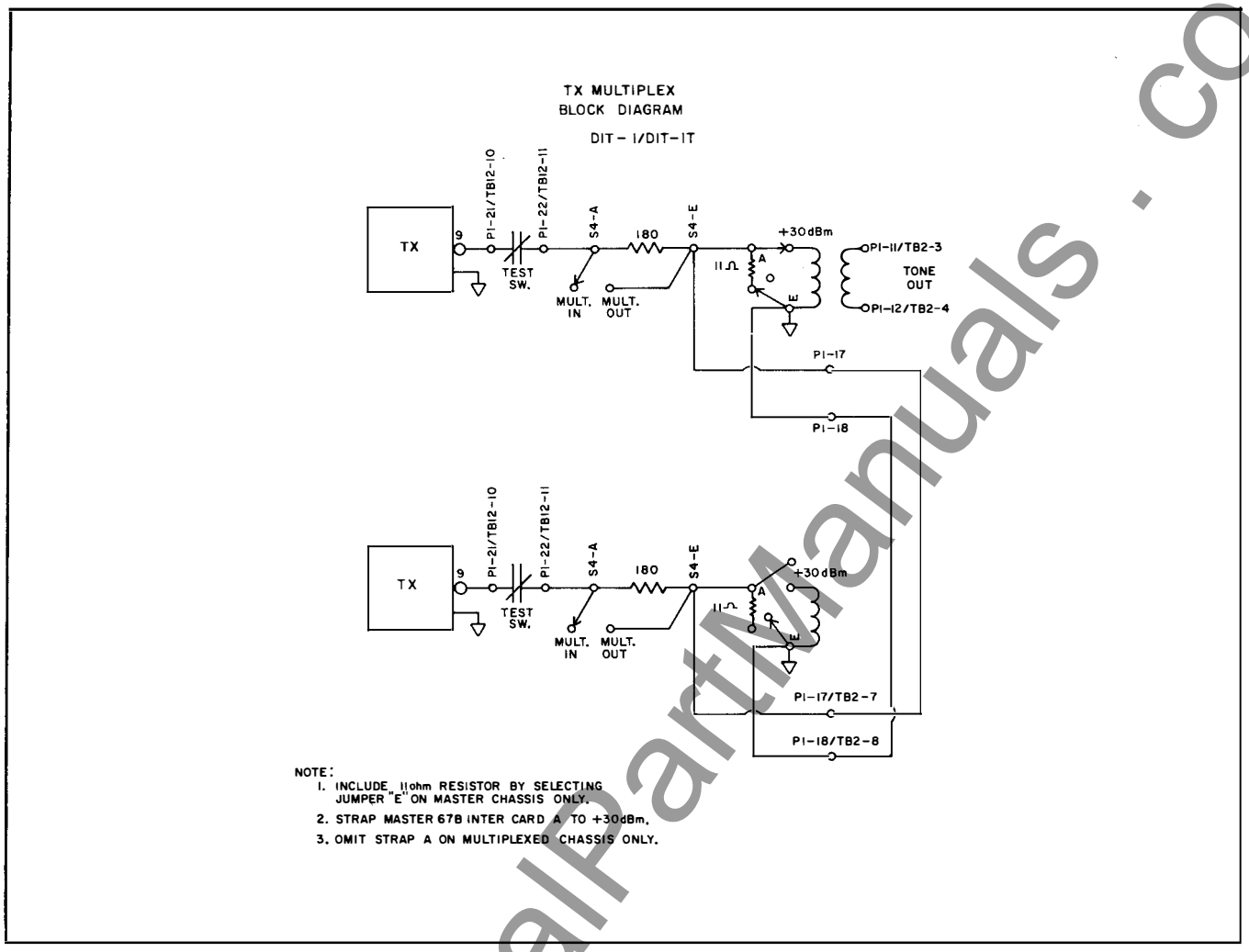


Figure 9. Multiplex Connections for Transmitters.

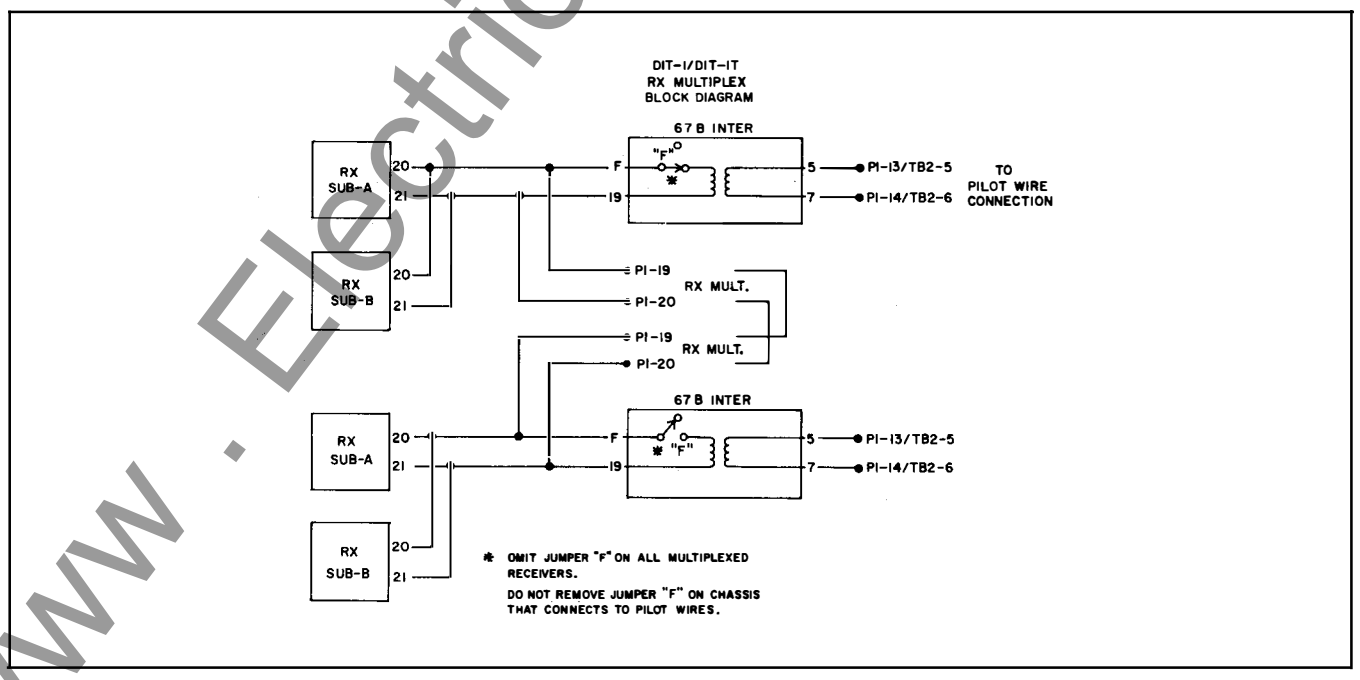
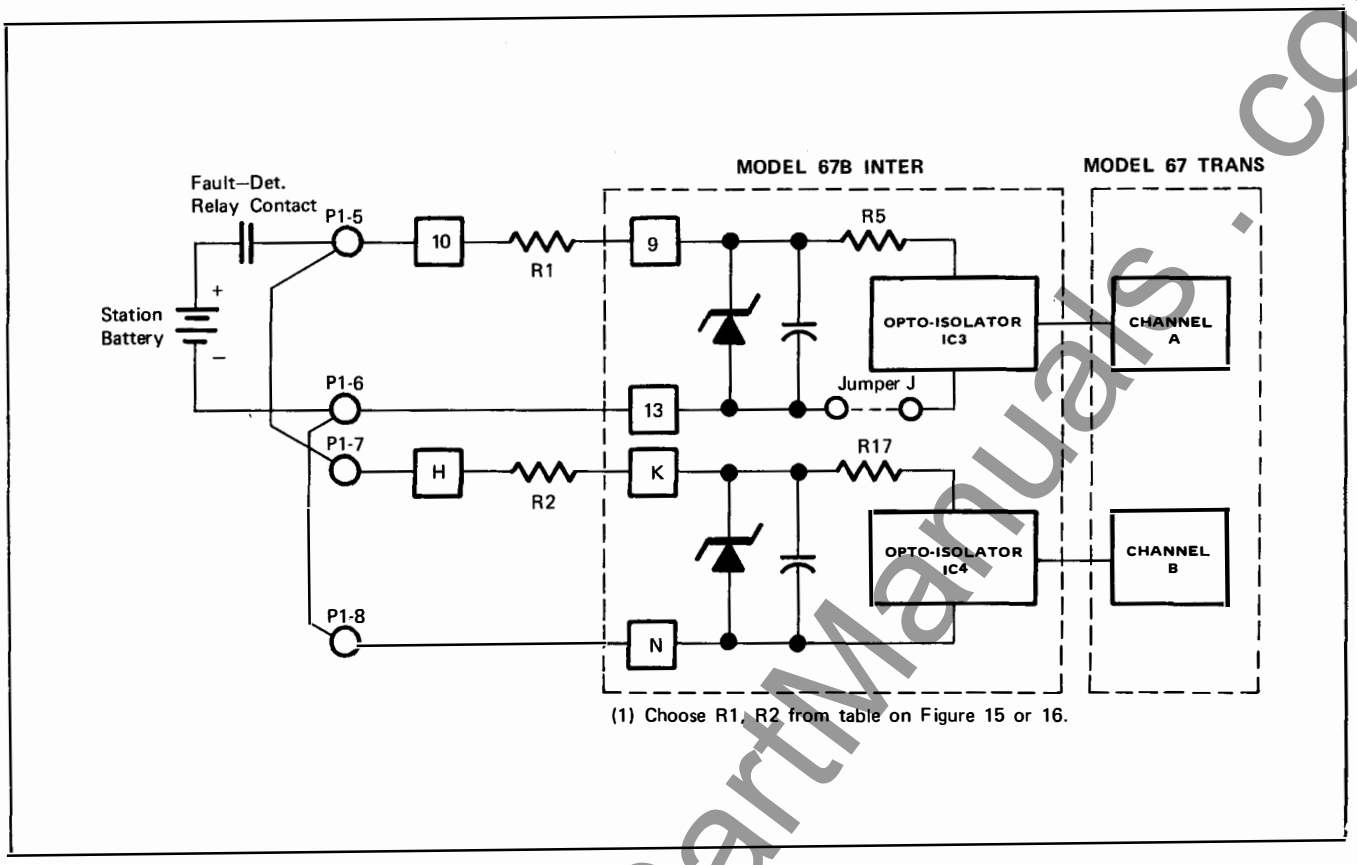
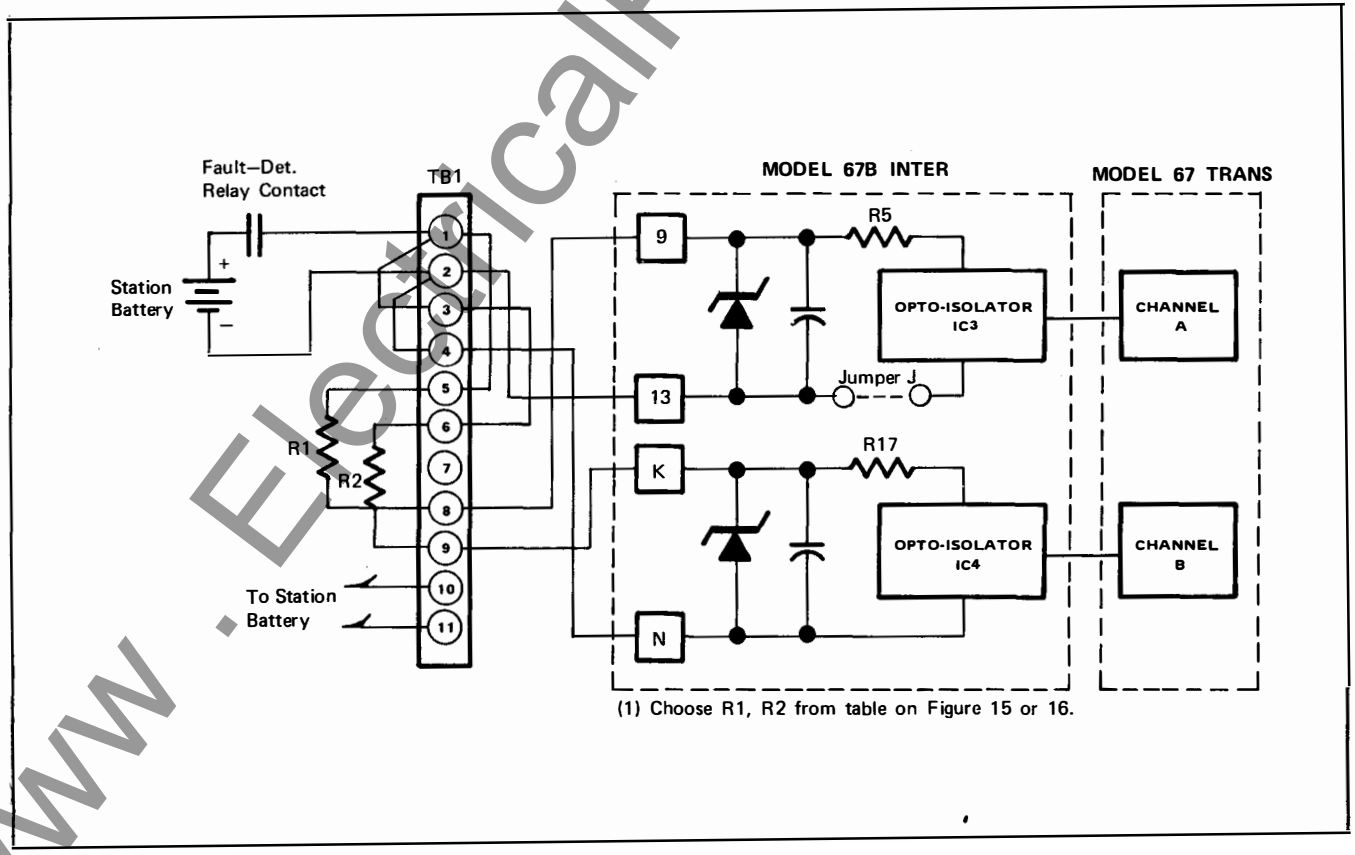


Figure 10. Multiplex Connections for Receivers.



(1) Choose R1, R2 from table on Figure 15 or 16.

Figure 11. Dual-keying trip input, DIT-1.



(1) Choose R1, R2 from table on Figure 15 or 16.

Figure 12. Dual-keying trip input, DIT-1T.

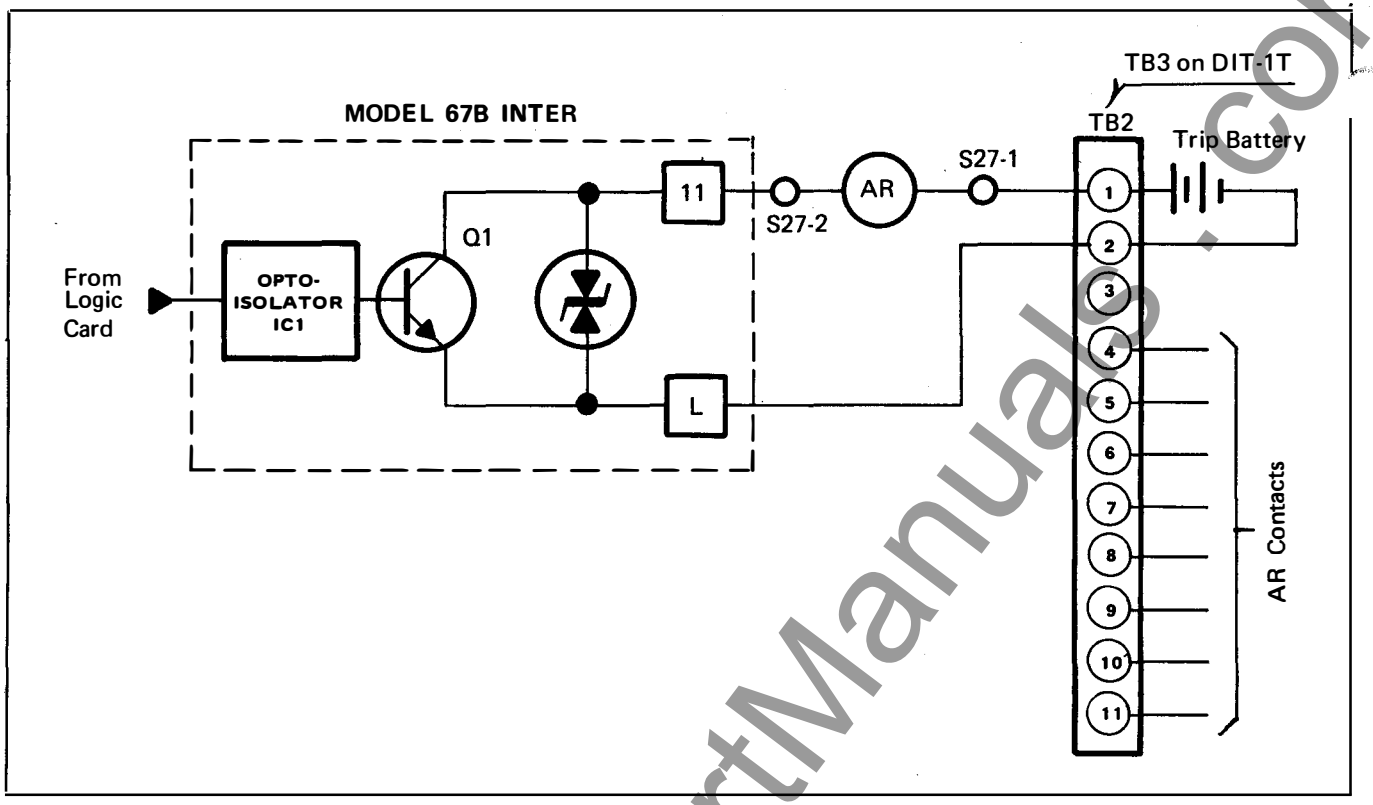


Figure 13. Single trip output with single logic card, DIT-1 and DIT-1T.

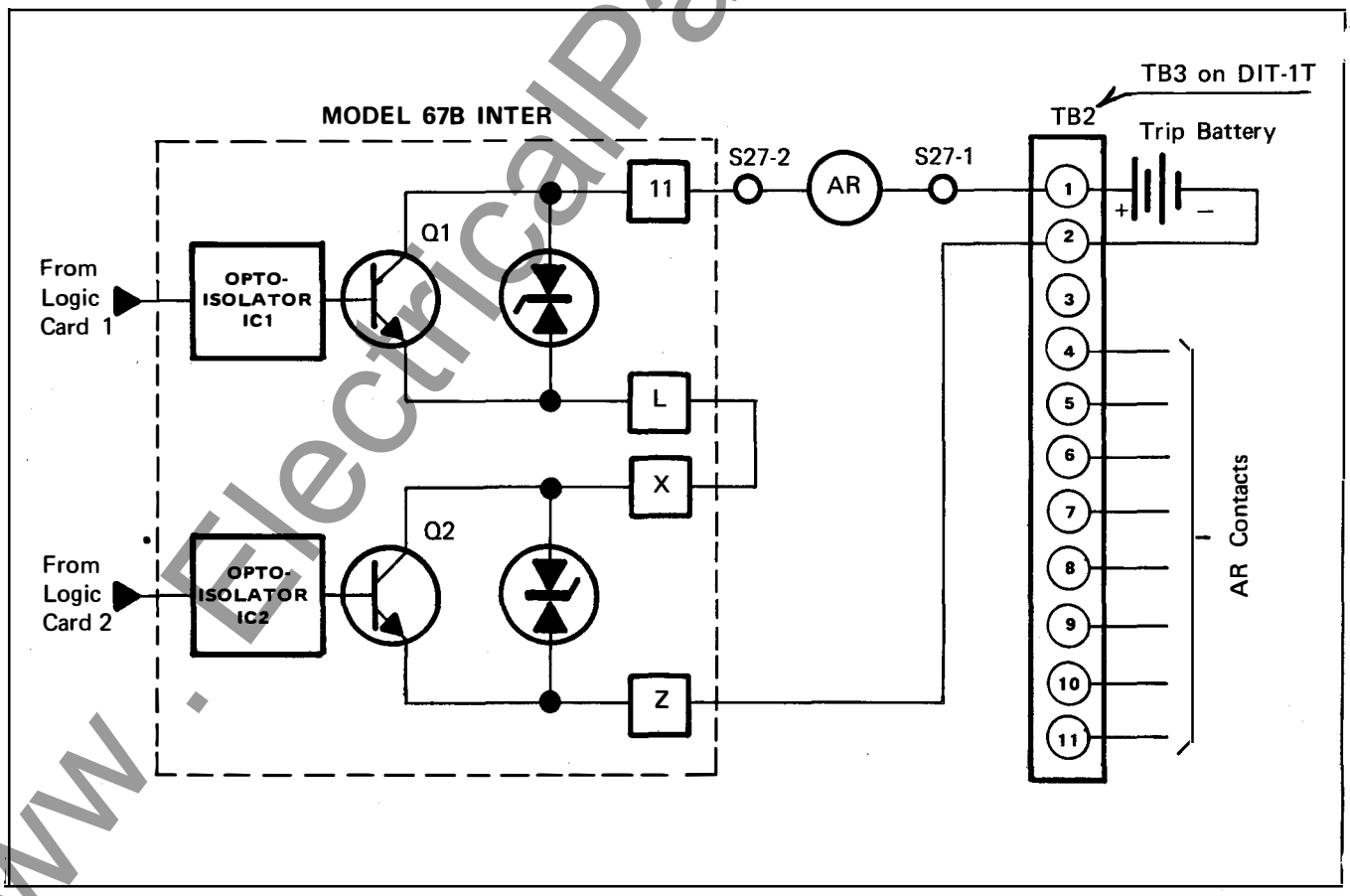


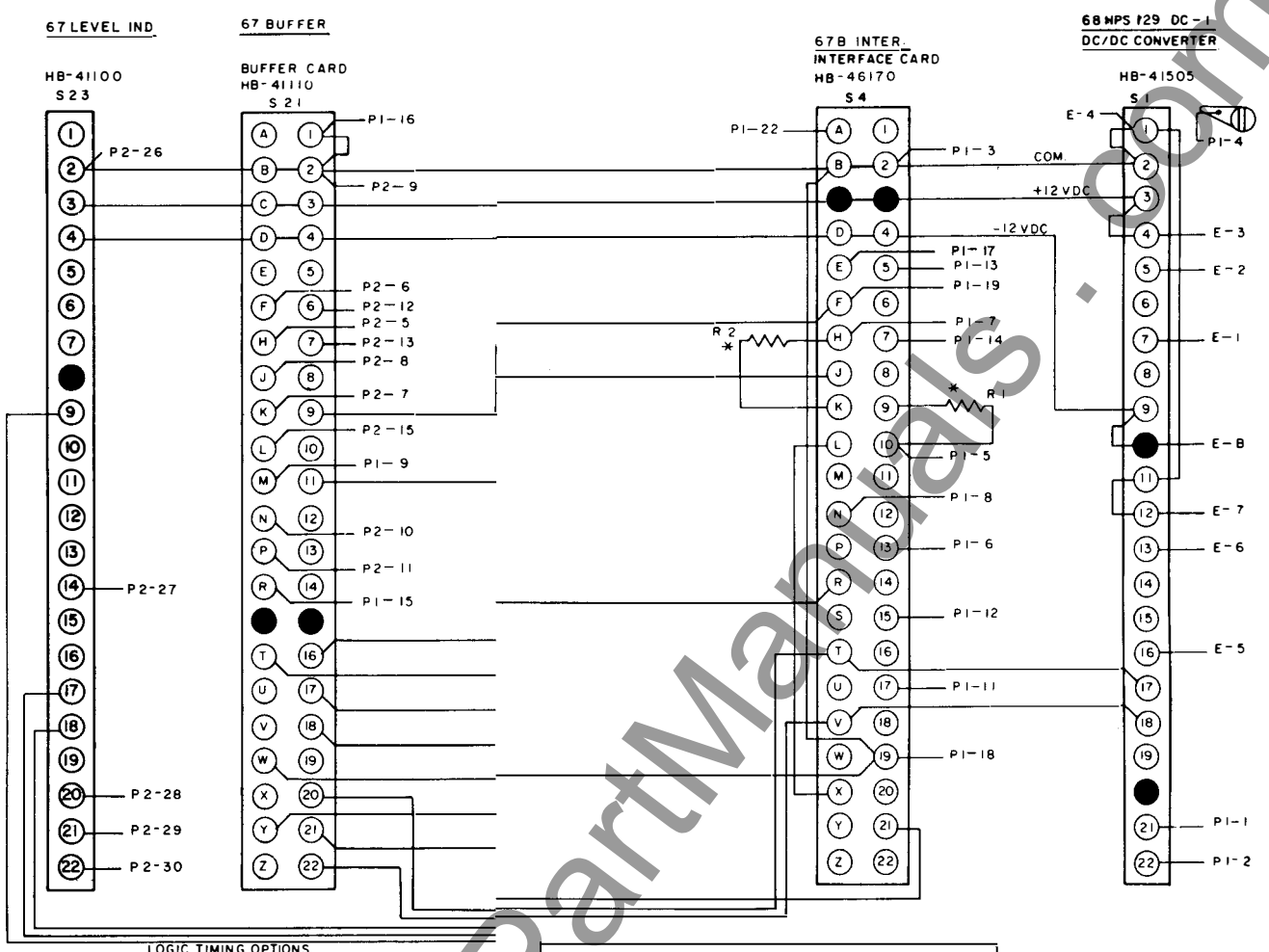
Figure 14. Trip outputs in series with dual logic cards, DIT-1 and DIT-1T.

TABLE 8. COMPONENTS FOR DETERMINING FREQUENCY

GROUP	CENTER-FREQ. OF SUB-CHANNEL Hz	CHANNEL SPACING Hz (NOTE 2)	MODE AND FREQ. Hz	TRANSMITTER						WIDEBAND RECEIVER		BOTH RECEIVERS	NARROWBAND RECEIVER				
				CRYSTAL				FREQ. DETER. NETWORK									
				SUFFIX FOR XTAL P/N HA-41034-	FREQ. MHz	CIRCUIT POSITION	JUMPER POSITION	P/N FOR POSITION RZ1	P/N FOR POSITION RZ2	INPUT FILTER P/N	DISCRIMINATOR NETWORK P/N	POSITION IN CARD CAGE (NOTE 1)	BEAT FREQ. Hz	SUFFIX FOR XTAL P/N HA-41034-	CRYSTAL FREQ. MHz	JUMPER POSITION	RZ1 NETWORK PART NUMBER
1	A 935	340	T 860	–7	3.522560	Y1	A	HB-41065-1		HB-74200-1	HB-74300-1	A	1200	–5	2.45760	F	HB-41064-1
			G 1010	–8	4.136960	Y3											
	B 1275	340	G 1200	–5	2.457600	Y4	F		HB-41065-2	HB-74200-2	HB-74300-2	B	1010	–8	4.13690	A	HB-41064-1
			T 1350	–6	2.764800	Y2											
2	A 1275	340	T 1200	–5	2.457600	Y1	B	HB-41065-2		HB-74200-2	HB-74300-2	A	1540	–9	3.15392	F	HB-41064-1
			G 1350	–6	2.764800	Y3											
	B 1615	340	G 1540	–9	3.153920	Y4	F		HB-41065-3	HB-74200-3	HB-74300-3	B	1350	–6	2.76480	F	HB-41064-1
			T 1690	–10	3.461120	Y2											
3	A 1615	340	T 1540	–9	3.153920	Y1	B	HB-41065-3		HB-74200-3	HB-74300-3	A	1880	–11	3.85024	F	HB-41064-1
			G 1690	–10	3.461120	Y3											
	B 1955	340	G 1880	–11	3.850240	Y4	F		HB-41065-4	HB-74200-4	HB-74300-4	B	1690	–10	3.46112	F	HB-41064-1
			T 2030	–12	4.157440	Y2											
4	A 1955	340	T 1880	–11	3.850240	Y1	B	HB-41065-4		HB-74200-4	HB-74300-4	A	2220	–13	4.54656	F	HB-41064-1
			G 2030	–12	4.157440	Y3											
	B 2295	340	G 2220	–13	4.546560	Y4	F		HB-41065-5	HB-74200-5	HB-74300-5	B	2030	–12	4.15744	F	HB-41064-1
			T 2370	–14	4.853760	Y2											
5	A 2295	340	T 2220	–13	4.546560	Y1	B	HB-41065-5		HB-74200-5	HB-74300-5	A	2560	–3	2.62144	E	HB-41064-1
			G 2370	–14	4.853760	Y3											
	B 2635	340	G 2560	–3	2.621440	Y4	G		HB-41065-6	HB-74200-6	HB-74300-6	B	2370	–14	4.85367	F	HB-41064-1
			T 2710	–4	2.775040	Y2											
6	A 2635	340	T 2560	–3	2.621440	Y1	C	HB-41065-6		HB-74200-6	HB-74300-6	A	2900	–1	2.96960	E	HB-41064-1
			G 2710	–4	2.775040	Y3											
	B 2975	340	G 2900	–1	2.969600	Y4	G		HB-41065-7	HB-74200-7	HB-74300-7	B	2710	–4	2.77504	E	HB-41064-1
			T 3050	–2	3.123200	Y2											
7	A 2975	340	T 2900	–1	2.969600	Y1	C	HB-41065-7		HB-74200-7	HB-74300-7	A	3240	–15	3.31776	E	HB-41064-1
			G 3050	–2	3.123200	Y3											
	B 3315	340	G 3240	–15	3.317760	Y4	G		HB-41065-8	HB-74200-8	HB-74300-8	B	3050	–2	3.12320	E	HB-41064-1
			T 3390	–16	3.573760	Y2											
8	A 935	680	T 785	–17	3.215360	Y1	A	H8-41065-9		HB-74200-9	HB-74300-9	A	1465	–19	3.00032	F	HB-41064-2
			G 1085	–18	4.444160	Y3											
	B 1615	680	G 1465	–19	3.000320	Y4	F		H8-41065-10	HB-74200-10	HB-74300-10	B	1085	–18	4.44416	A	HB-41064-2
			T 1765	–20	3.614720	Y2											
9	A 1615	680	T 1465	–19	3.000320	Y1	B	HB-41065-10		HB-74200-10	HB-74300-10	A	2145	–21	4.39296	F	HB-41064-2
			G 1765	–20	3.614720	Y3											
	B 2295	680	G 2145	–21	4.392960	Y4	F		HB-41065-11	HB-74300-11	HB-74300-11	B	1765	–20	3.61472	F	HB-41064-2
			T 2445	–22	5.007360	Y2											
10	A 2295	680	T 2145	–21	4.392960	Y1	B	HB-41065-11		HB-74200-11	HB-74300-11	A	2825	–23	2.89280	E	HB-41064-2
			G 2445	–22	5.007360	Y3											
	B 2975	680	G 2825	–23	2.892800	Y4	G		HB-41065-12	HB-74200-12	HB-74300-12	B	2445	–22	5.00736	F	HB-41064-2
			T 3125	–24	3.200000	Y2											

(1) There are two receiver cards per group, one for subchannel A and one for subchannel B. Positions shown are for both wideband and narrowband receiver at their respective locations. Do NOT place narrowband receiver cards in wideband locations, and vice versa.

(2) The pre-trip timer on the logic card is 4.5 ms for 340-Hz channel spacing, and is 2.5 ms for 680-Hz channel spacing.

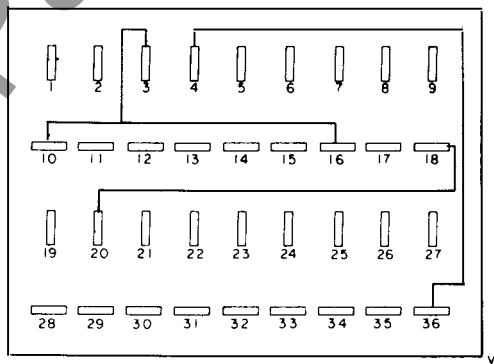


LOGIC TIMING OPTIONS
TABLE IV

LOGIC CARD	PRE TRIP TIMER	GUARD BEFORE TRIP	TRIP AFTER GUARD
67 LOGIC	4.5 MS	100 MS	100 MS
67 LOGIC-1	3.2 MS	100 MS	100 MS
67 LOGIC-2	.5 MS	100 MS	100 MS
67LOGIC-13	4.5 MS	25 MS	25 MS

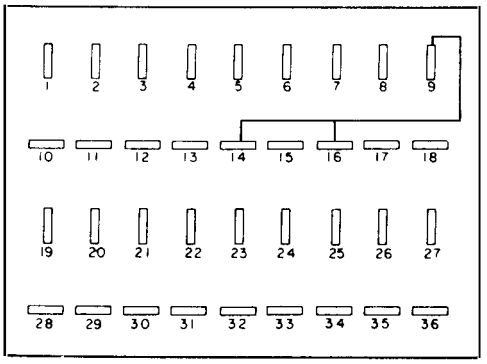
PIN NO.	WIRE COLOR
1	B
2	R
3	O
4	Y
5	G
6	B
7	V
8	W
9	B
10	G
11	B
12	R
13	O
14	Y
15	G
16	B
17	V
18	W
19	B
20	O
21	B
22	R
23	O
24	Y
25	G
26	B
27	V
28	W
29	B
30	G
31	B
32	R
33	O
34	Y
35	G
36	B

SEE NOTE 6



P 1
SEE TABLE II

P 1 & P 2
VIEW LOOKING FROM REAR OF CHASSIS
WITH REAR PANEL MOUNTED

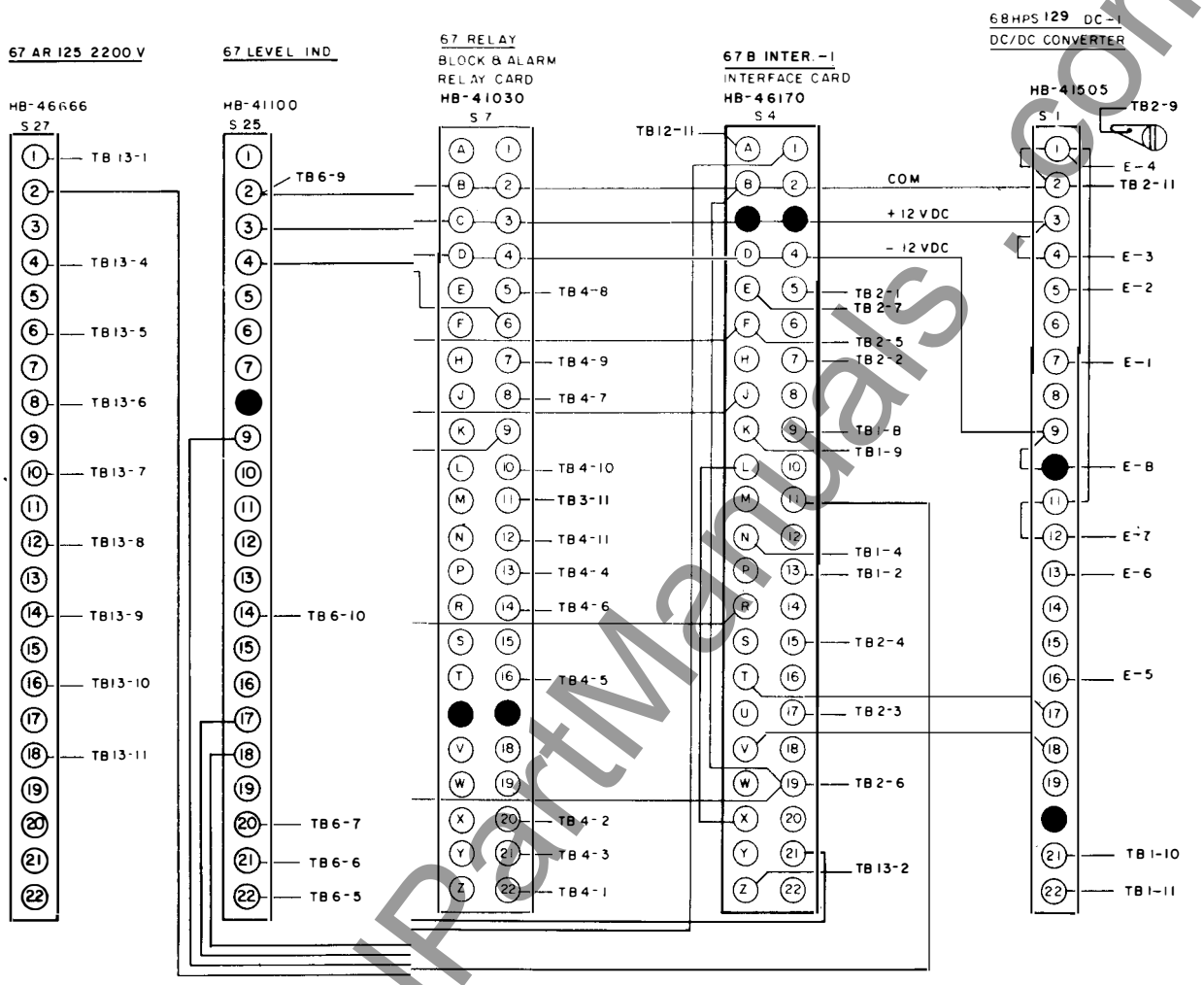


P 2
SEE TABLE III

NOTES

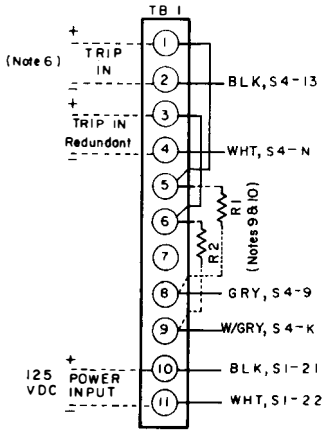
1. S – INDICATES PRINTED CIRCUIT BOARD SOCKETS
2. TB – INDICATES BARRIER STRIPS
3. ● – INDICATES KEY LOCATION
4. WIRING IS NO 22 STRANDED OF COLOR MARKED UNMARKED WIRE IS BUSS WIRING
5. RELAY CONTACTS ARE SHOWN UNENERGIZED
6. JUMPER P1-21 TO P1-22 WHEN EXTERNAL TEST SWITCH IS NOT USED.

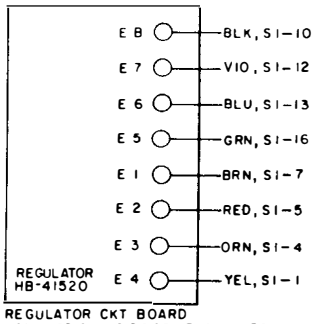
ssis for Solid State STU-12 Application with Level Indicator Option.



LOGIC TIMING OPTIONS
TABLE II

LOGIC CARD	PRE TRIP TIMER	GUARD BEFORE TRIP	TRIP AFTER GUARD
67 LOGIC	4.5 MS	100 MS	100 MS
67 LOGIC-1	3.2 MS	100 MS	100 MS
67 LOGIC-2	.5 MS	100 MS	100 MS
67LOGIC-13	4.5 MS	25 MS	25 MS





REGULATOR CKT BOARD
MOUNTED ON INSIDE OF REAR PLATE

NOTES:

1. S — INDICATES PRINTED CIRCUIT BOARD SOCKET
2. TB — INDICATES BARRIER STRIPS
3. ● — INDICATES KEY LOCATION
4. WIRING IS NO. 22 STRANDED OF COLOR MARKED UNMARKED WIRE IS BUSS WIRING
5. RELAY CONTACTS ARE SHOWN UNENERGIZED
6. TO SEND TRIP APPLY VOLTAGE TO TB1-1 & 2 AND PARALLEL TB1-1 & 3 AND TB1-2 & 4.

s for ElectroMechanical Direct Transfer Trip Application with Level Indicator Option.

Wideband Receiver, Model 67 REC

General: The Receiver Input Assembly, Model 67 REC, the schematic of which is shown as Figure 2, consists of a bandpass filter, preamplifier, amplifier, frequency discriminator, quadrature-signal network and amplifier, and automatic-gain-control (AGC) circuits. The receiver usually operates in the frequency range between 800 and 3300 Hz, although operation can be extended to as high as 10 kHz. Maximum input sensitivity is −40 dBm. Dynamic range of the AGC is usually set for 22 dB.

Theory of Operation: The incoming signal is applied to a bandpass filter which is a passive, four-coil, 35 dB, Cauer (elliptical) filter. The filter assembly, HB-74200-X, is selected for the channel frequency. Jumper A is a factory adjustment for bandwidth and should not be altered in the field. From the filter, the signal is passed to a 20-turn, cermet, stepless potentiometer used as a sensitivity control, and to a preamplifier. The output of the preamplifier, IC1, is fed to a voltage divider consisting of R6 and Q1. The signal then passes through two opamps, IC2/B and IC2/A, to the receiver output which delivers AM signal to the detector card. The same signal also is delivered to IC6/A and B for further processing.

IC6/A is the active element of a frequency-shift discriminator, a discriminator whose center frequency is selected by choice of Filter Assembly HB-74300-X. The choice is a function of channel frequency. The output of the discriminator is fed to the FS/AM Detector Card, 67 FS/AM.

IC6/B is an amplifier which takes the same signal delivered to the discriminator, IC6/A, but develops an output signal leading the received signal by 90^{o} because of the phase shift of R16 and C16 at its non-inverting input, Pin 5. This signal is used on the FS/AM Detector Card, 67 FS/AM.

AGC Control System: IC3/B is a linear voltage comparator used to compare the level of the received signal against a reference voltage of magnitude determined by the level of trip boost selected for a given installation. The dc reference, applied at Pin 6, is selected by choice of plug-in network RZ-16 on the Receiver Logic Card, 67 Logic. At Pin 5 there is delivered, from the FS/AM Detector Card, 67 FS/AM, a rectified dc voltage, taken from an operational-rectifier signal-level detector, which is portional to the magnitude of the signal received. The difference, if any, between reference level and actual signal level appears at the output of IC3/B. It is subsequently amplified and used to control the gate voltage of Q1. This transistor, with R6, forms a signal-voltage divider between IC1 and IC2/B, and the voltage division is adjustable by changing the resistance from drain to source by variation of the gate voltage. If the signal is too low, gate voltage changes to increase R_{ds}, thus increasing signal at Pin 5 of IC2/B. High signal, of course, causes a reverse action. There is provision on the circuit card for adding a jumper for slow AGC when trip boost is used.

It is desirable to establish a reference level for the AGC voltage at the gate of Q1, so that the dynamic range of the gate of Q1 is in the same span of voltage as is the AGC-control signal. This is done by making zero signal (minimum attenuation) correspond to the pinchoff voltage. But the pinchoff voltage of Q1, the voltage for maximum R_{ds} and for minimum attenuation, is not accurately predictable. IC3/A is provided, therefore, to establish whateverpinchoff voltage is required at the gate of Q1, by selection of R25.

R25 and R27 establish the selected reference voltage at Pin 3 of IC3/A. At the junction of CR3 and CR4, the chosen reference voltage, plus the drop across CR1 and CR2, and less the voltage drop across CR3, is added to the rectified signal to set the absolute level of control voltage at the gate of Q1.

Resistor R25 is selected, during manufacture, to make the reference-voltage level for the AGC circuits equal to pinchoff voltage of the unit used at Q1. Resistor R26 is selected, at the same time, to provide the dynamic range desired for the AGC voltage.

R29, C21, and C22 provide filtering and the necessary AGC time constant. IC4 provides both needed gain and output capacity for loads in addition to Q1.

IC5/A & B are low- and high-signal detectors. Both are voltage comparators. The low-signal detector uses AGC-reference voltage from IC3/A as its minimum-signal reference. The high-signal reference is ground potential. Each opamp excites an appropriate limit indicator, DS1 or DS2; and their outputs also deliver an out-of-limit signal to Pin 10 for use at the Receiver Logic Card, 67 LOGIC.

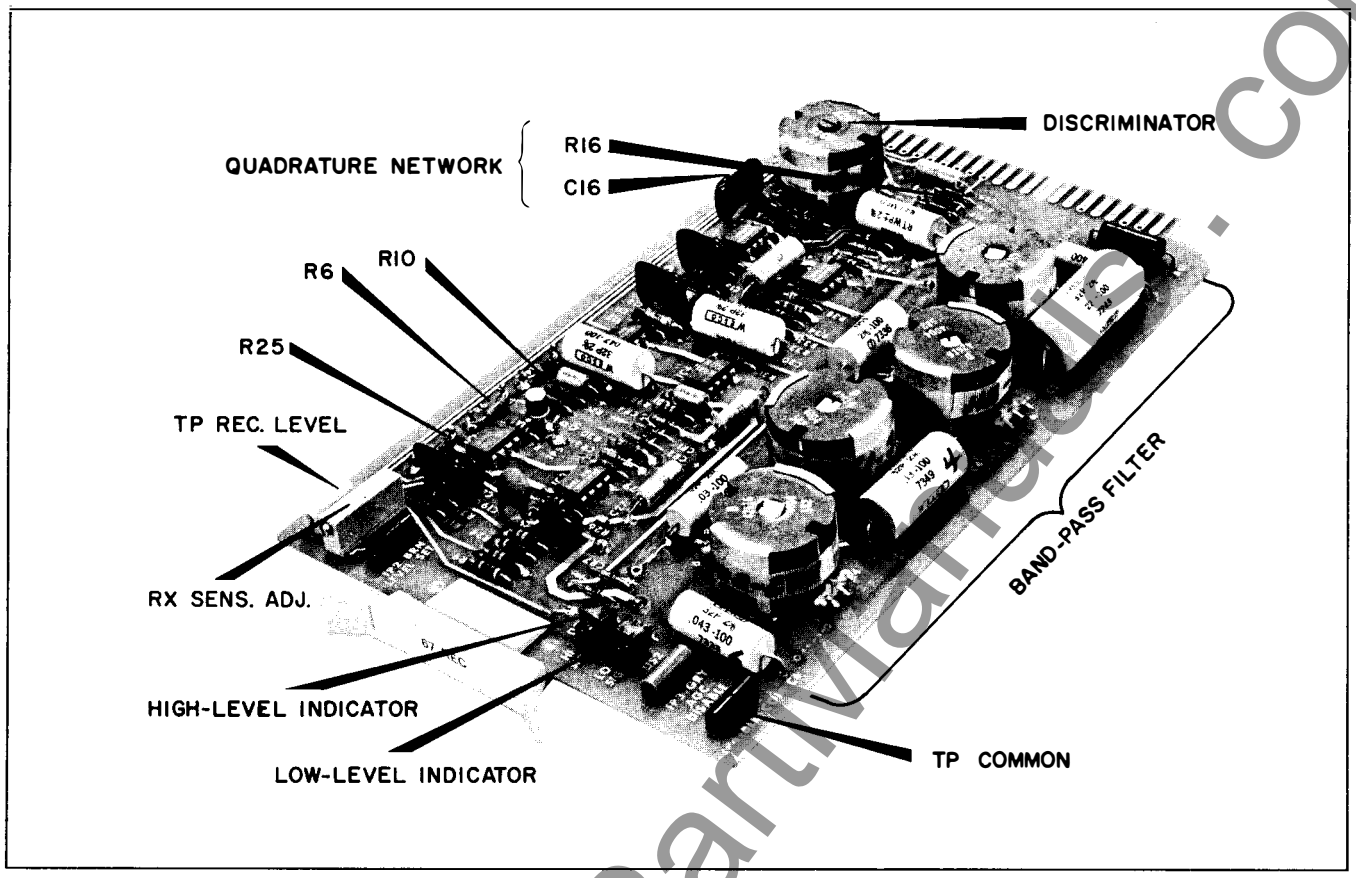


Figure 1. Receiver Card

Table of Replaceable Parts

DIAGRAM SYMBOL	NAME OF PART AND DESCRIPTION	PART NO.
	MODEL 67 REC, P/N HB-41005	
	CAPACITORS	
C1 thru C6	Part of input – filter assembly. P/N HB-74200-X. Absolute values depend upon frequency. See Table	
C7	Capacitor, dipped mica, 220 pF, 2%, 500 V, Electromotive DM-19	HA-16616
C8, 15, & 17	Capacitor, dipped mica, 22 pF, 5%, 500 V, Electromotive DM-15	H-1080-325
C9, 14, & 21	Capacitor, tantalum, 3.3 μF, 20%, 35 V, Corning CCL-035-335-20	H-1007-1260
C10 & 20	Capacitor, poly., 0.047 μF, 2%, 100 V, Wesco 32P	H-5115-67
C11	Capacitor, tantalum, 1 μF, 20%, 35 V, Corning CCM-035-105-20	H-1007-496
C12 & 13	Capacitor, dipped mica, 100 pF, 2%, 500 V, Electromotive DM-19	HA-16600

DIAGRAM SYMBOL	NAME OF PART AND DESCRIPTION	PART NO.
C16	Capacitor, dipped mica, 2000 pF, ±2%, Electromotive DM-19 or DM-20	HA-16222
C18	Same as C8, 33 pF	HA-16511
C19	Capacitor, ceramic disc, 0.01 μF, 20%, 100 V, Cornell-Dubilier MGP01	H-1007-1261
C22	Capacitor, tantalum, 15 μF, 20%, 35 V, Corning CCZ-035-156-20	H-1007-654
C23	Part of discriminator assembly, P/N HB-74300-X. See Table	
C24, 25, 26, & 27	Capacitor, tantalum, 15 μF, 20%, 20 V, Corning CCD-020-156-20	H-1007-716
	RESISTORS	
R1, 7, 8, 13, 14, 15, 17, 18, 19, 20, 24, 27, 30, 31, 35, & 41	Resistor, metal-film, precision 1%, 1/8 W, value per schematic, per RFL Spec HA-38301	H-1510-(XXX)
R2	Resistor, variable, cermet trimmer, 10 K, 10%, 0.75 W, Helipot 79PR10K	HA-39539
R3, 4, 5, 6, 9, 10, 11, 12, 21, 22, 23, 24, 25, 26, 28, 32, 33, 34, 36, 37, 38, 39, 40, 42	Resistor, fixed composition, 5%, ¼ W, value per schematic, Allen Bradley CB	H-1009-(XXX)
R16	Same as R1, for values see following Table	

Center Freq. Hertz	R16 Value	R16 P/N
935	84.5K	H-1510-1554
1275	61.9K	H-1510-1555
1615	49.9K	H-1510-569
1955	40.2K	H-1510-720
2295	34.8K	H-1510-1554
2635	30.1K	H-1510-569
2975	26.7K	H-1510-1152
3315	24.3K	H-1510-477

	SEMICONDUCTORS	
CR1 thru CR8	Diode, silicon, type 1N914B	HA-26482
DS1 & 2	Light emitting diode, Dialight 550-0102	HA-39568
IC1	Integrated circuit, high performance linear opamp, National LM741CN, or equal	H-0620-52
IC2, 3, 5, & 6	Integrated Circuit, linear dual opamp, National LM-1458M, or equal	H-0620-51
IC4	Integrated Circuit, high performance linear opamp, National LM307N, or equal	H-0620-93
Q1	Transistor, FET, siliconix VCR4N	HA-41008

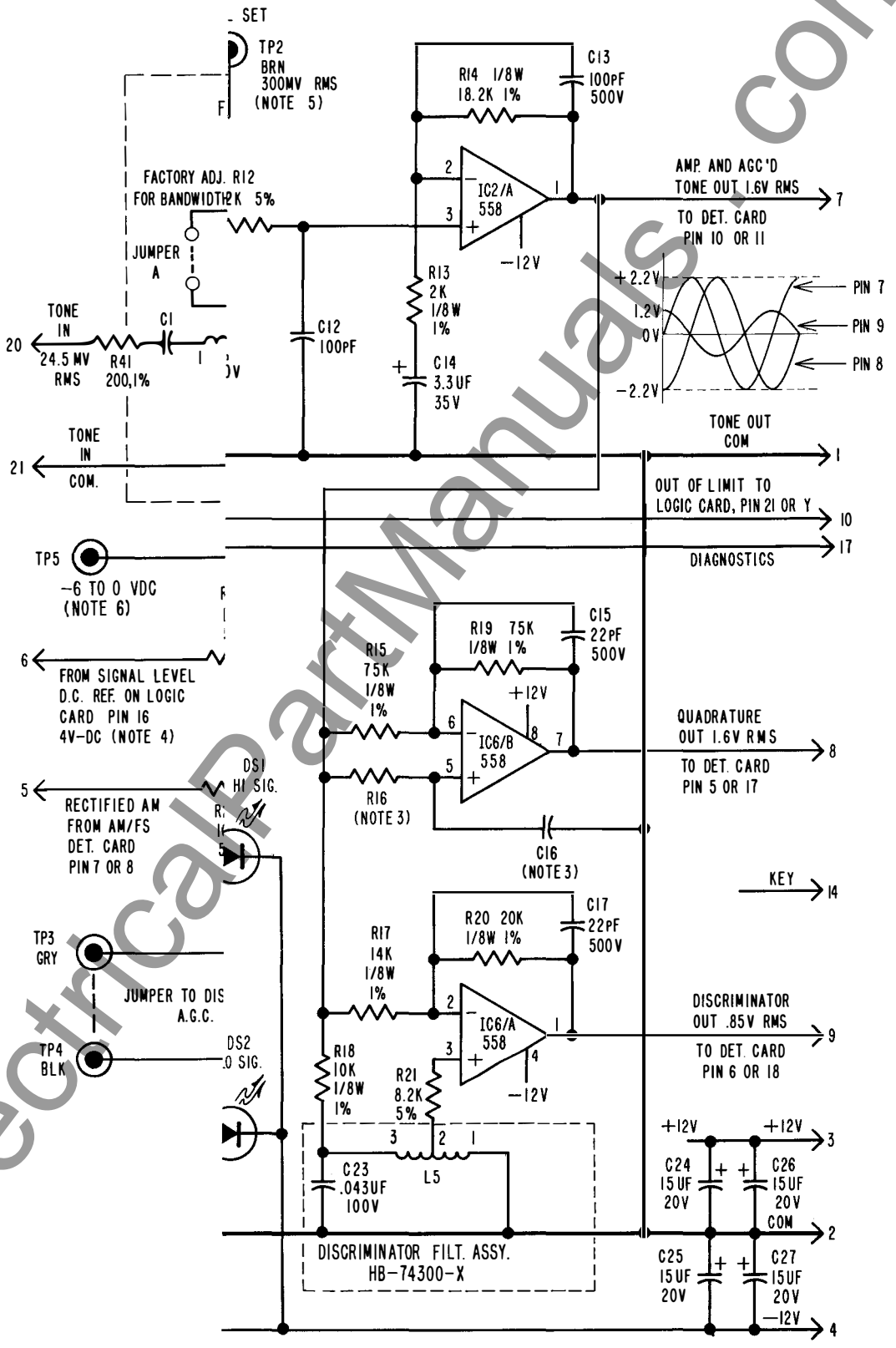


Figure 2. Schematic of Receiver

Transmitter, Model 67 TRANS

General: The schematic of the transmitter is shown on Figure 3. The two channels of the transmitter are shown on this schematic diagram. Channel A will be described in detail, with the understanding that the same discussion applies to Channel B. The symmetry of the drawing makes identification of components simple for either channel. Each channel has its own Schmitt trigger circuit to accept trip-input signal, guard-frequency and trip-frequency crystal-controlled oscillators which are running continuously, a digital frequency divider, and a bandpass filter. At the output of each filter, the channels are combined in a summing amplifier which, in turn, drives an output amplifier.

Theory of Operation: Under normal conditions, the Transmitter sends two guard signals. Thus, for Channel A, the tone frequency controlled by Y3, oscillating with IC1/A, is transmitted. That signal is divided by the digital divider, IC3, the output of which is a squarewave. Straps, A, B, C, and D, at the output of IC3, permit a choice of dividing the crystal frequency by 2^9, 2^{10}, 2^{11}, or 2^{12}. These choices, combined with the freedom to select a crystal frequency in the range between 2.4 and 4.5 MHz, make it possible to select any channel frequency that may be desired in a range from the lowest frequency shown on Table 1 to 3.5 kHz.

IC4/B and IC5/A & B are three opamps constituting the active elements of an active bandpass filter which shapes the squarewave output of IC3 into a pure sine wave. Resonant frequency of the filter is determined, in part, by RZ-1, a plug-in element chosen for the frequencies of the channel in use, and by C13 and C15.

Output of the bandpass filter for Channel A is combined with that from Channel B in the summing amplifier, IC12/A. As described later, the summing amplifier never has a gain greater than unity. Transmitter-output level is set by R56. IC14 is the driver amplifier for the output circuit, whose active elements are Q1, Q2, Q3, and Q4.

The foregoing outlines the operation of the transmitter when guard tones are transmitted. Several changes occur when a trip signal from the interface card is received. Channel A is discussed. Channel B parallels it.

A negative-going, grounded, trip-input signal at Pin 19 causes the output of the Schmitt trigger, IC10/B, to generate a positive-going signal at its output, Pin 7. Before trip, the guard signal passed through IC2/A and IC2/D to the divider. With the appearance of the trip signal at Pin 1 of IC2/A, and of an inverted trip pulse at Pin 5 of IC2/B, guard signal is cut off and trip-frequency signal is passed through IC2/B and IC2/D to the divider. Hence, trip-frequency tone is transmitted.

The trip pulse from the output of IC10/B via IC1/C is used also to control switches IC6/A and IC6/C. These switches open, thereby increasing the resistances used as frequency-determining elements in the active filter, and so to lower its resonant frequency to the lower, trip frequency of Channel A. Note that a positive-going trip pulse is used to control IC6/B and IC6/D to close the switches. This action adds resistors in parallel, and thus raises the resonant frequency of the bandpass filter, as required for Channel B in accordance with the fundamental philosophy of the system.

Finally, it will be observed that the trip monitor, DS1, will be excited through the presence of trip signal on Pins 8 and 9 of IC2/C.

Trip-Boost Timer: The trip-boost timer, when used, effects an increase in output level of the transmitter when trip signal is sent, and it determines the length of time for which the signal level is increased, selectable up to a maximum period of 250 mS. The slow-AGC jumper in the Model 67 REC must always be in place when trip boost is used. References 1 and 2 of the Bibliography discuss the considerations involved.

Signals from the two Schmitt triggers appear at Pins 5 and 6 of IC11/B, the output of which is combined, at IC11/A, with a guard-signal level to produce a positive pulse at Pin 3 of IC11/A. That pulse, coupled to the input of a voltage comparator, IC12/B, forces the comparator to change state, from a high level to a low level. Output from the comparator excites the trip-boost monitor, DS3, through IC11/D, and it opens switch IC13/A.

When IC13/A is opened, the resistance in the feedback loop of IC12/A, the summing amplifier, is increased, thus raising its gain. The magnitude of the increase in output level during the trip-boost function is adjustable by choice of Resistors R16-11 and R14-9 in the plug-in network, RZ-3. The length of time for which the enhanced trip signal continues is adjusted by Resistor R8-3 in the same network. The time constant of this resistor and C21 determines when the charge on C21 falls to the point where the voltage on Pin 6 of IC12/B falls below the threshold level, held at Pin 5 by R51 and R52, and so causes the output to return to the non-boost state.

IC13/C & D are normally closed switches used for routine maintenance and diagnostic work on the transmitter. They are used to reduce the output of the transmitter to zero in the event that the power-supply voltage drops below a predetermined value at which the transmitter may fail to function properly. Under normal conditions, Q5 is saturated, so that its collector is at about +11.8 V. This holds the two switches closed. If power-supply voltage drops to 9.8 V, or below, base drive for Q5 is lost, and its collector falls to ground potential, thereby opening the two switches and interrupting the signals from Channels A and B.

Figure 2 shows the format of transmitted signals during conditions of guard, trip boost, trip, and return to guard.

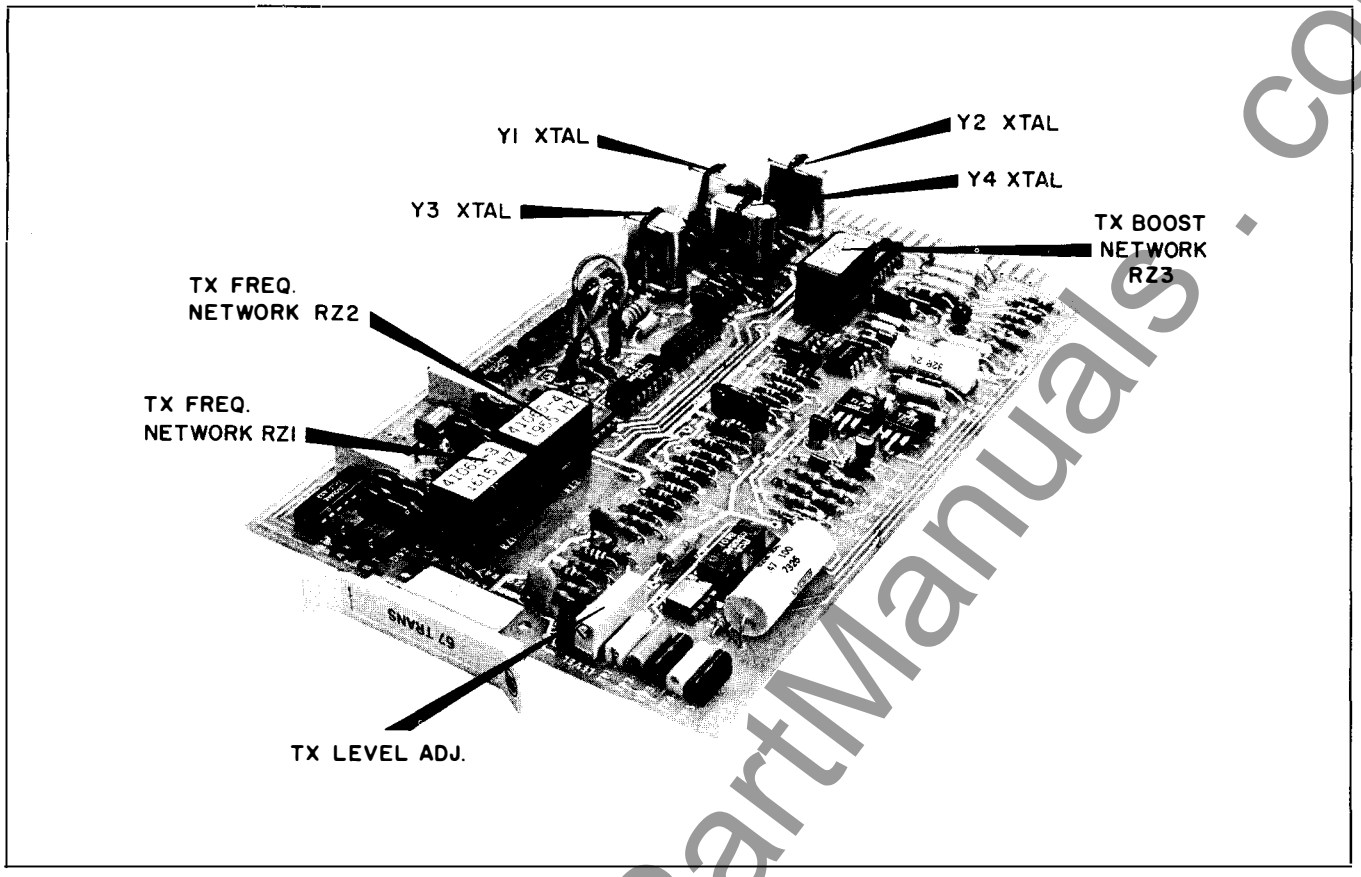


Figure 1. Transmitter Card

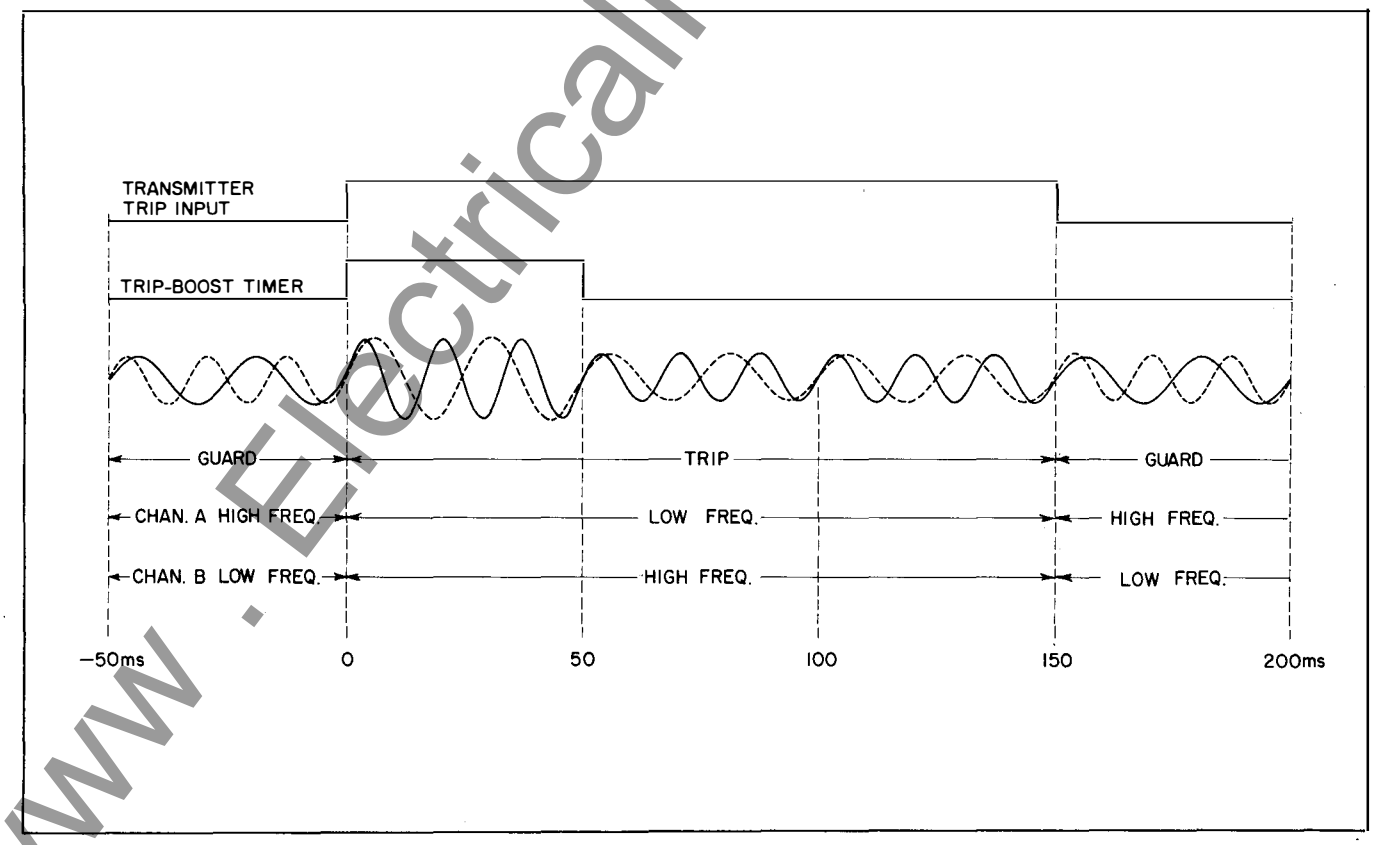


Figure 2. Signals During Guard, Trip Boost, Trip, and Return to Guard.

Table of Replaceable Parts

DIAGRAM SYMBOL	NAME OF PART AND DESCRIPTION	PART NO.
	MODEL 67 TRANS, HB-41010	
	CAPACITORS	
C1, 2, 3, & 4	Capacitor, dipped mica, 47 pF, 5%, 500 V, Electromotive DM-15	HA-16515
C5 thru C12	Same as C1, 56 pF	HA-16517
C13 thru C16	Capacitor, silver mica, 0.002 μF, 2%, 500 V, Electromotive DM-20	HA-16222
C17 & 18	Capacitor, ceramic disc, 0.002 μF, 20%, 1000 V, Sprague 5GA-D20	H-1007-942
C19	Capacitor, ceramic disc, 220 pF, 10%, 500 V, Erie 831-000X5F0221K	H-1007-493
C20	Capacitor, ceramic disc, 0.02 μF, +80 −20%, 25 V, Erie 5835-000Y 5U203Z	H-1007-754
C21	Capacitor, mylar, 0.47 μF, 2%, 100 V, Wesco 32M	H-1007-448
C22	Capacitor, silver mica, 100 pF, 2%, 500 V, Electromotive DM-19	HA-16600
C23 & 25	Same as C1, 33 pF	HA-16511
C24 & 30	Capacitor, tantalum, 1 μF, 20%, 35 V, Corning CCM-035-105-20	H-1007-496
C26, 27, 28, 29, & 33	Capacitor, tantalum, 15 μF, 20%, 20 V, Corning CCD-020-156-20	H-1007-716
C31	Capacitor, tantalum, 33 μF, 20%, 10 V, Corning CCD-010-336-20	H-1007-653
C32	Capacitor, MPC, 0.047 μF, 2%, 100 V, Wesco 32 MPC	H-1007-1196
C34, 35	Capacitor, ceramic, 0.1 μF, +80 −20%, 25 V, Erie 5815-000Y5U 104Z, or eq.	H-1007-646
	CRYSTALS	
Y1, 2, 3, & 4	Piezoelectric quartz crystals determining frequency of oscillators. For fundamental frequencies see Table 4.	
	RESISTORS	
R1 thru R10 R19 thru R22 R29 thru R50 R53, 54, & 55 R57 thru R65 R68 R70 thru R76	Resistor, fixed composition, 5%, ¼W, value per schematic, Allen Bradley CB	H-1009-(XXX)
R11 thru R18 R25, 26, 27, 28, R51 & 52	Resistor, precision, 1%, 1/8 W, value per schematic, per RFL Spec HA-38301	H-1510-(XXX)
R23 & 24	Resistor, variable cermet, 2 K, 10%, 0.75 W, Helipot 79PR2K	HA-39537
R56	Same as R23, 10 K, Helipot 79PR10K	HA-39539
R66 & 67	Resistor, wirewound, 1 ohm, 5%, 1½ W, Ohmite 4030, Style 995-1A	H-1100-585

DIAGRAM SYMBOL	NAME OF PART AND DESCRIPTION	PART NO.
R69	Resistor, wirewound, 10 ohms, 5%, 3¼ W, Ohmite 4361, Style 995-3A	H-1100-479
RZ1 & RZ2	Bandpass filter frequency-adjusting network. See Table for part numbers.	
R23	Gain-adjusting network for trip boost. Values per sales order.	
	SEMICONDUCTORS	
CR1, 2, 5, & 6	Diode, silicon, type 1N914B	HA-26482
CR3 & 4	Diode, silicon rect., 1 A, Solitron S4003TA20	HA-30769
CR7	Diode, zener, 6.2 V, 10%, 500 mW, Motorola 1N5234	HA-29227
CR8	Diode, zener, 9.1 V, 5%, 400 mW, Fairchild 1N960B	HA-41014
DS1, 2, & 3	Light - emitting diode, Dialight 550-0102	HA-39568
IC1	Integrated Circuit, COS/MOS, Hex inverter/buffer, RCA CD4049AE, or eq.	H-0615-7
IC2 & 9	Integrated Circuit, CMOS Quad, 2-input, NDR gate, RCA CD4001AE, or eq.	H-0615-3
IC3 & 8	Integrated Circuit, CMOS, 12-stage ripple-carry binary counter/divides RCA CD4040AE, or eq.	H-0615-21
IC4, 5, 7, 10, & 12	Integrated Circuit, linear dual opamp, T1SN72558-P or eq.	H-0620-51
IC6 & 13	Integrated Circuit, CMOS, Quad bilatered switch, RCA CD4016AE, or eq.	H-0615-15
IC11	Integrated Circuit, COS/MOS, Quad, 2-input NAND gate, RCA CD4011AE, or eq.	H-0615-5
IC14	Integrated Circuit, hi-performance, linear opamp. TI SN72741P, or eq.	H-0620-52
Q1	Transistor, silicon, NPN, type 2N3904	HA-21563
Q2	Transistor, silicon, PNP, type 2N3906	HA-21565
Q3	Transistor, silicon, PNP, power, TI TIP-30	HA-39493
Q4	Transistor, silicon, NPN, 30 W, TI TIP-29	HA-37425
Q5	Transistor, PNP, type 2N4249	HA-41919

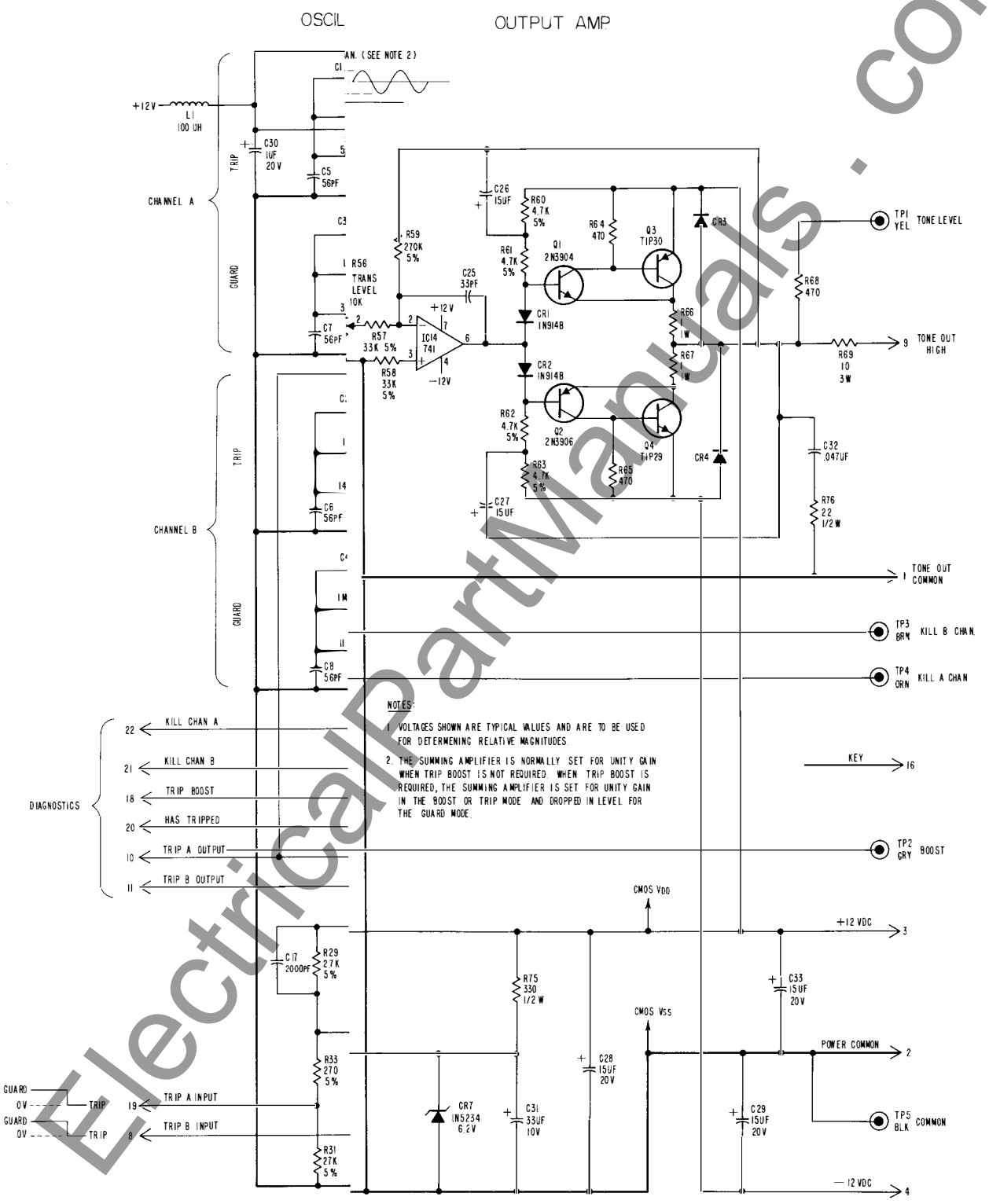


Figure 3. Schematic of Transmitter

67 TRANS

FS/AM Detectors, Model 67 FS/AM

General: The FS/AM Detector Assembly, 67 FS/AM, carries two identical sets of circuits, one for Channel A (low frequency) and one for Channel B (high frequency). Each channel uses operational rectifiers, sum and difference amplifiers, summing and inverting amplifiers, and low-pass filters. And these circuits are identical for the two channels. The block diagram of Figure 2 relates specifically to the low-frequency channel. Figure 3 is keyed to the block diagram and shows the waveforms at each point in the circuit. There input signals are applied to each set of detectors, all taken from the Receiver, Figure 2.

Theory of Operation: The signal-level detectors operate as follows: On Figure 2, the received tone signal, amplified and controlled by the receiver's AGC circuits, is applied to IC3, a precision rectifier with a negative output. Another tone signal, called quadrature, identical to the first in amplitude but lagging in phase by 90^{o}, is applied to a second precision rectifier, IC6. The input signals are shown as A and B on Figure 3. Output signals for the two rectifiers are K and L, which are identical but displaced by 90^{o}

The rectified tone signals are added and inverted with IC4/B, whose output is waveform M. Note that ripple frequency is four times the frequency of the input signals. This approach permits the use of a filter with a relatively short time constant, thereby improving the speed of response of the signal-level (AM) detectors. This is the "high-speed" detector appearing in Figure 8 of the Description.

Finally, the rectified signal is filtered with IC4/A, which functions as an active, low-pass filter. The dc output of this is returned to the receiver for AGC control, and it is also sent to the receiver logic card for use in the signal-level and noise-detection logic functions performed there.

The foregoing discussion, based on Channel A, applies directly to Channel B excepting for a change in the designation of integrated circuits used. Those for Channel B can be identified easily by reference to Figure 4, whose layout embodies much symmetry to simplify such identification.

Operation of the FS detector is based upon the fact that when high frequency is received the output signal from the discriminator is 180^{o} out of phase with the quadrature signal, and that when low frequency is received the discriminator delivers a signal in phase with the quadrature-signal output from the receiver. The lower part of Figure 2 shows the FS detector plan for Channel A.

Sum and difference of the two input signals, discriminator and quadrature, are taken in IC1/B and IC1/A, respectively. Note, at D and E, Figure 3, the change between sum and difference signals for the change from guard (high) to trip (low) frequency, as in Channel A. When guard is present, the output of the FS detector is negative (low). When trip is present, the output is positive (high). The relative frequency distribution of guard and trip signals is, of course, opposite for Channel B.

IC2/A & B is a precision rectifier with output positively polarized, and the output of rectifier IC5/A & B is negative. The results of rectification and of choice of output polarity appear as F and G, Figure 3.

As in the case of the AM detector, the FS signals are added and, inverted by IC11/B, and filtered by IC11/A to deliver an FS output. This is negative for guard and positive for trip as shown at J.

Connections shown between the sum and difference amplifiers and their respective rectifiers in Figure 2 apply only for the case of Channel A. Protection against frequency translation depends upon the fact that in Channel B the frequency disposition of guard and trip signals is reversed from that used in Channel A. It still is required, however, that the FS output, J, for Channel B be the same as for A, with trip positive and guard negative. This is effected by connecting the summed signal to the upper rectifier, Figure 2, and the difference signal to the lower rectifier. Implementation of this appears in Figure 4, where, at the output of IC1, straps A and D are used for Channel A, while for Channel B straps F and G are used at the output of IC8. Straps are preferred over fixed wiring to provide for versatility in applying the equipment to the requirements of differing applications.

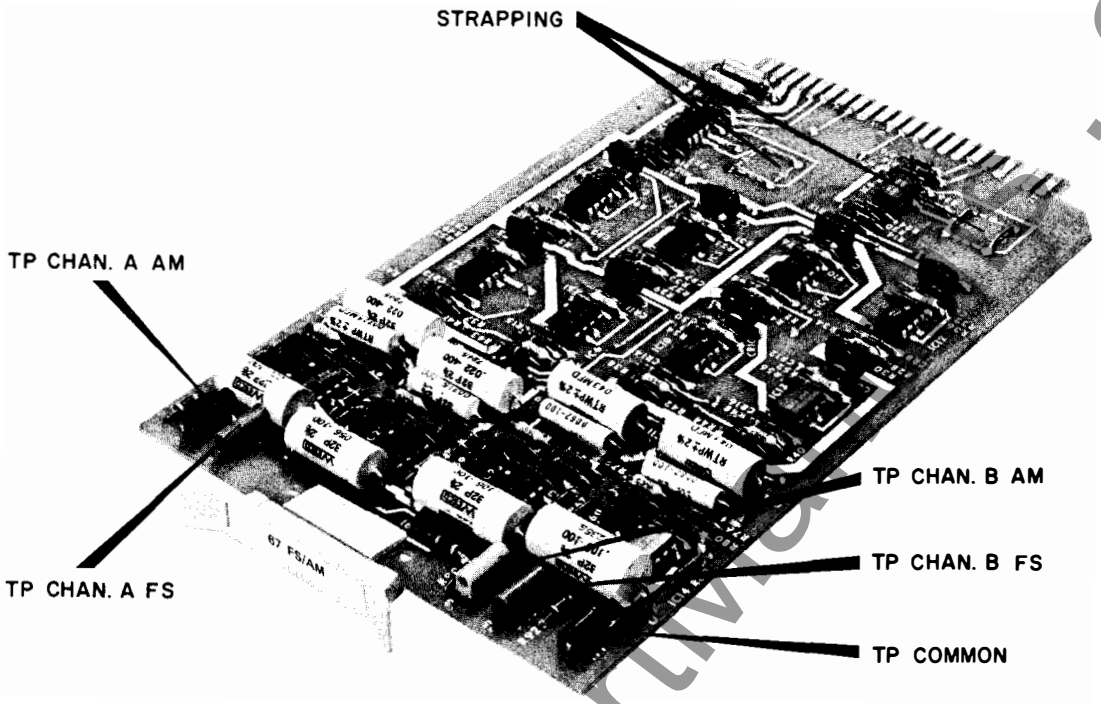


Figure 1. FS/AM Detector Card

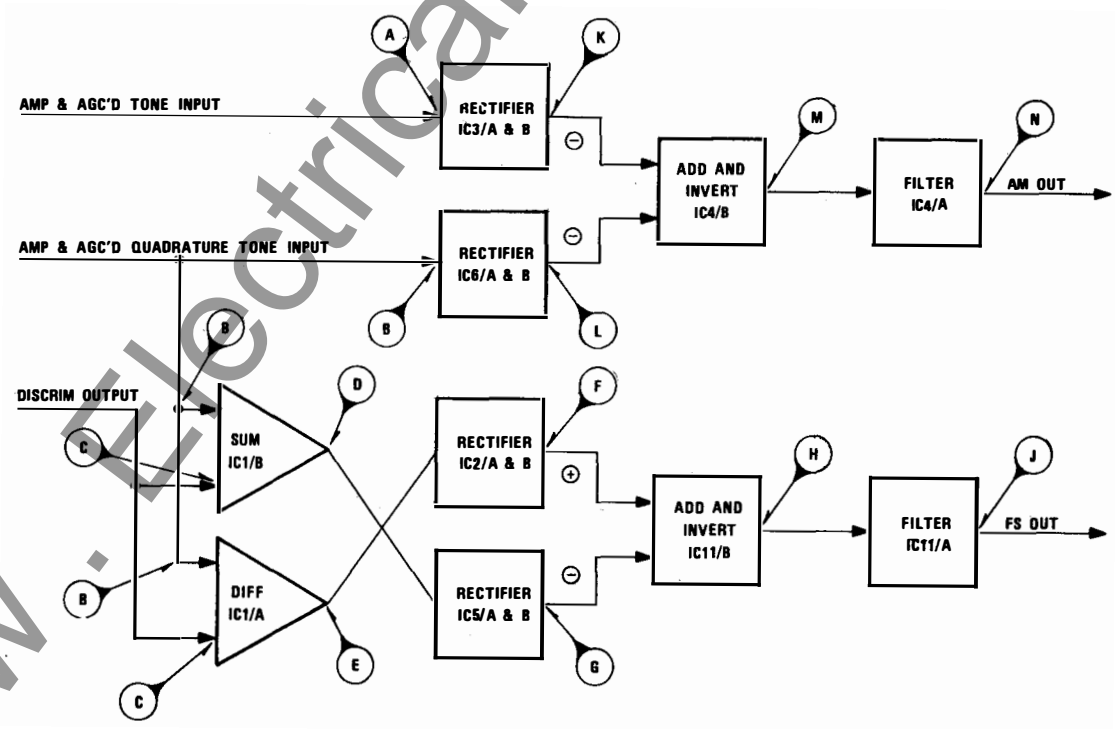


Figure 2. Block Diagram Showing Operation of Low-Frequency Channel

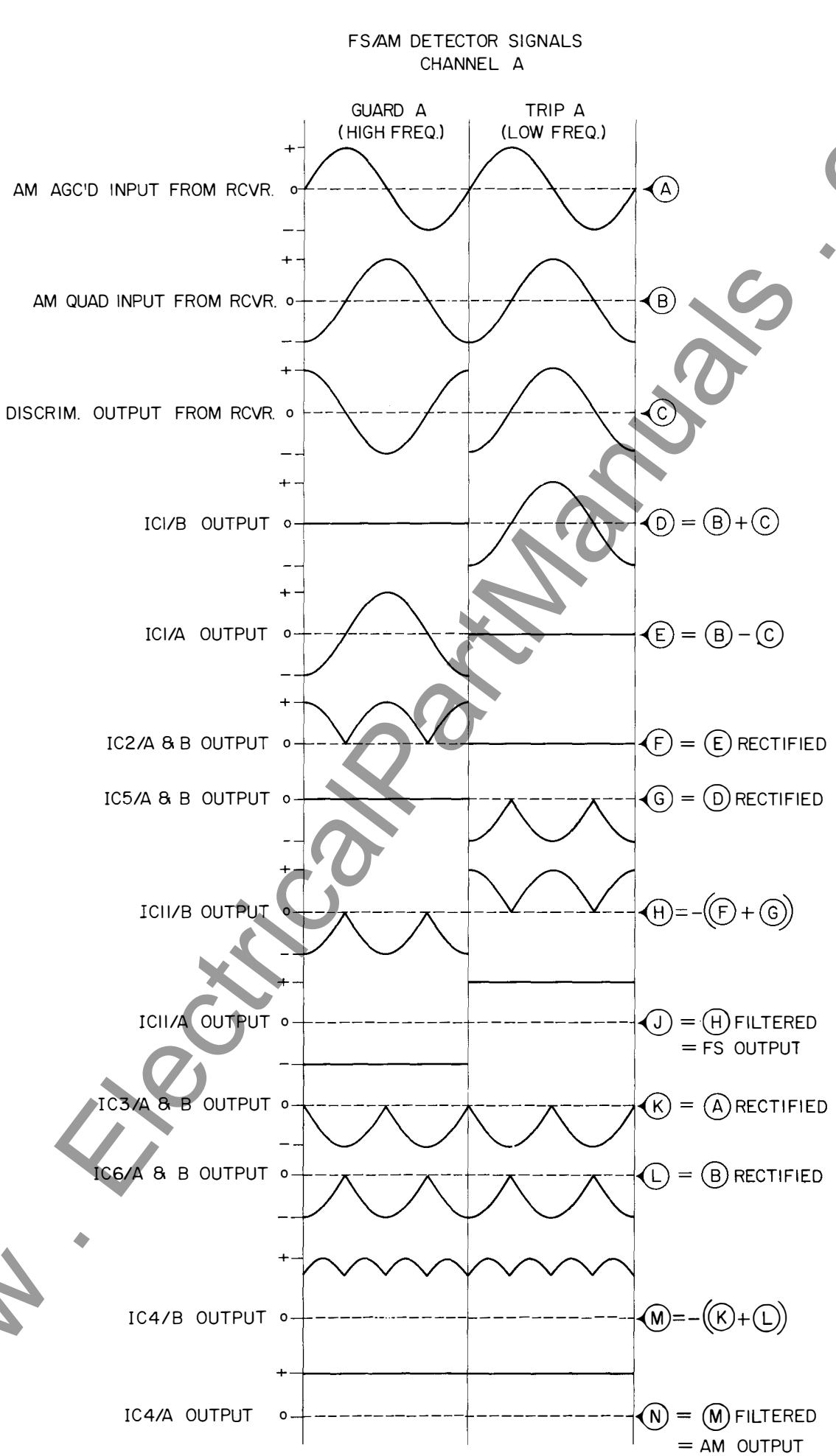


Figure 3. Typical FS/AM Detector Waveforms.

Table of Replaceable Parts

DIAGRAM SYMBOL	NAME OF PART AND DESCRIPTION	PART NO.
	MODEL 67 FS/AM, HB-41015	
	CAPACITORS	
C1 thru C8, C21 thru C24	Capacitor, dipped mica, 33 pF, 5%, 500 V, Electromotive DM-15	HA-16511
C9 & 10	Capacitor, poly., 0.022 μF, 2%, 100 V, Wesco 32P	H-5115-51
C11 & 12	Same as C9, 0.043 μF	H-5115-65
C13 & 14	Same as C9, 0.056 μF	H-5115-71
C15 & 16	Same as C9, 0.105 μF	H-5115-84
C17 & 18	Same as C9, 0.00315 μF	H-5115-10
C19 & 20	Same as C9, 0.0062 μF	H-5115-25
C25 & 26	Capacitor, tantalum, 15 μF, 20%, 20 V, Corning CCD-020-156-20	H-1007-716
C27 thru C32	Capacitor, ceramic disc, 0.1μF, −20 +80%, 25 V, Erie 5815000Y5U1047	H1007-646
R1, 2, 5, 6, 11, 12, R13, 14, 15, 16, 17, R18, 19, 20, 21, 22, R23, 24, 25, 26, 27, R28, 31, 32, 37, 38, R39, 40, 49, 50, 51, R52, 57, 58, 59, 60, R61, 62, 63, 64, 69, R70, 71, 72, 73, 74, R75, 76, 77, 78, 79, R80, 81, 82, 83, 84	Resistor, metal film, precision per RFL Spec HA-38301, value per schematic	H-1510-(XXX)
R3, 4, 7, 8, 9, 10, 29, R30, 33, 34, 35, 36, R41, 42, 43, 44, 45, R46, 47, 48, 53, 54, R55, 56, 65, 66, 67, R68, 85, 86, 87, 88, R89, 90, 91, & 92	Resistor, fixed composition, 5%, ¼ W, value per schematic, Allen Bradley CB, or eq.	H-1009-(XXX)
	SEMICONDUCTORS	
CR1 thru CR16	Diode, silicon, Type 1N914B	HA-26482
IC1 thru IC14	Integrated circuit, linear dual opamp., National LM1458N, or eq.	H-0620-51

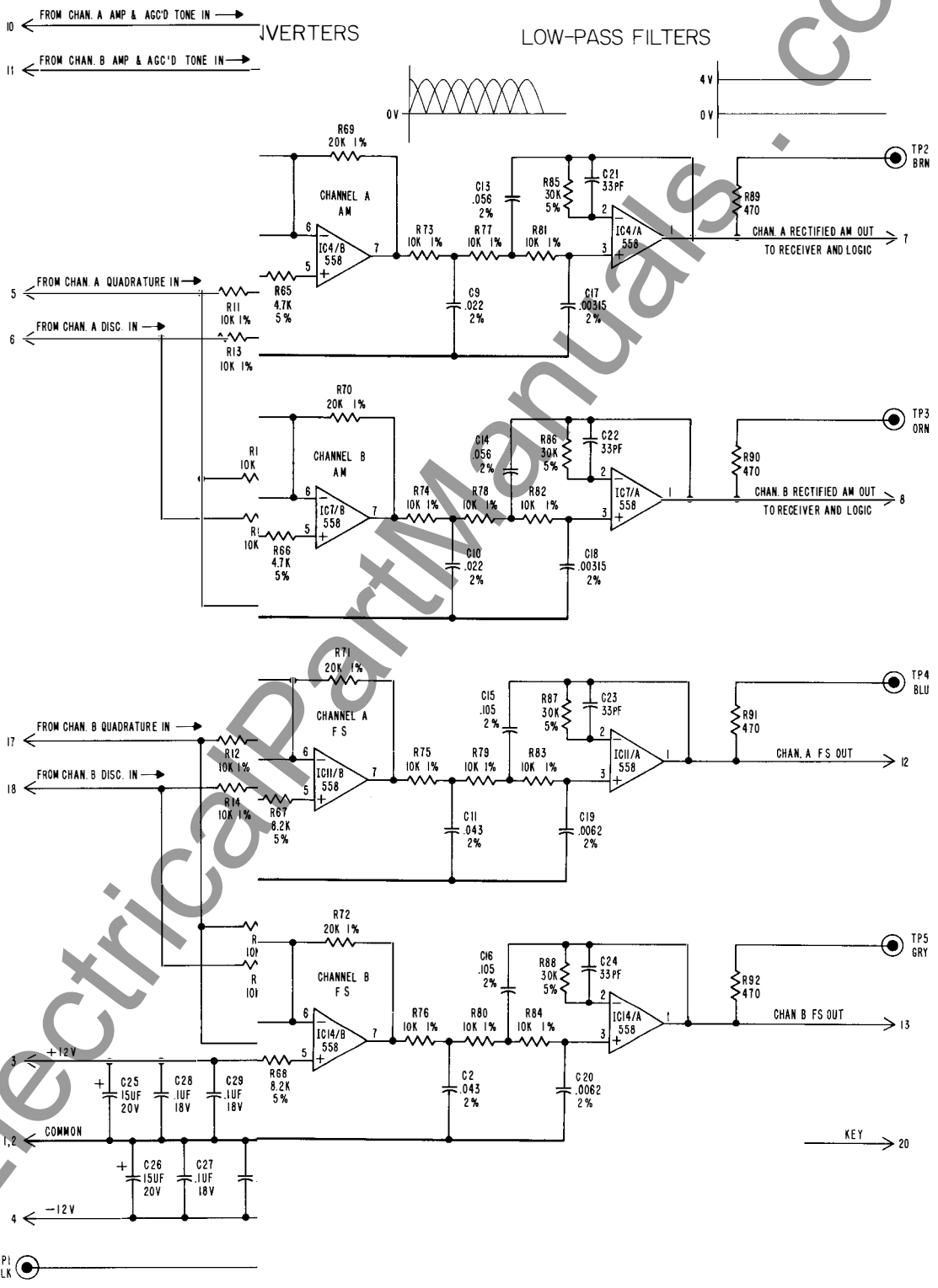


Figure 4. Schematic of FS/AM Detectors

Logic Circuits, Model 67 LOGIC

General: The purpose of the logic card is to evaluate the incoming signal and to determine (a) whether a valid trip is received, or (b) a valid guard is received, and (c) whether an invalid condition prevails. In each case, appropriate action is taken.

In order for the logic card to signal a received trip at its output terminal, the following conditions must be satisfied.

(a) The amplitude of both signals received in the AM channels must be within limits, neither too high nor too low.

(b) Both guard signals must have been received for at least 100 mS prior to the arrival of trip signal.

(c) Both trip signals must have appeared within 100 mS after the loss of guard signal.

(d) Trip signal must last for at least 4.5 mS.

(e) No block conditions are received from any internal or external source.

AM Window Detectors: Irrespective of whether guard or trip signals are being received, the AM detectors monitor the level of signal received on both channels. Their function is to signal appropriate action, usually by blocking the trip function, when the received signal falls below or above certain prescribed limits. Channels A and B are identical.

Considering only Channel A, the signal received from the FS/AM Detector Card, at Pin 18, should be +4 Vdc, normally, for a system not using the trip-boost feature. At IC1/A, a rise in received signal above +5.2 V will change the output from logic low to high. Similarly, a drop in signal below +2.8 Vdc will cause an identical change of state at the output of IC1/B. So long as the level of received signal stays within the limits prescribed, both inputs of IC4/D will be low, and its output high. If signal level crosses either the low or the high limit, as by the presence of excessive noise or an in-band signal, IC4/D will change its output to low for the duration of that condition.

For Channel B, the same analysis pertains, with the output of IC4/A high under normal conditions, low if either limit is transgressed.

Outputs of IC4/D and IC4/A are fed to the input of IC5/A. A change of level from either channel will cause the output of IC5/A to go high, and this state is known as "AM Noise Block". This high appears at Output-Terminal U for use elsewhere. Through IC6/B it excites monitor DS1 to indicate a "block" condition, and it also appears at Pin 3 of IC7/A. Finally, for a non-boost system, it also appears at Pin 8 of IC7/B.

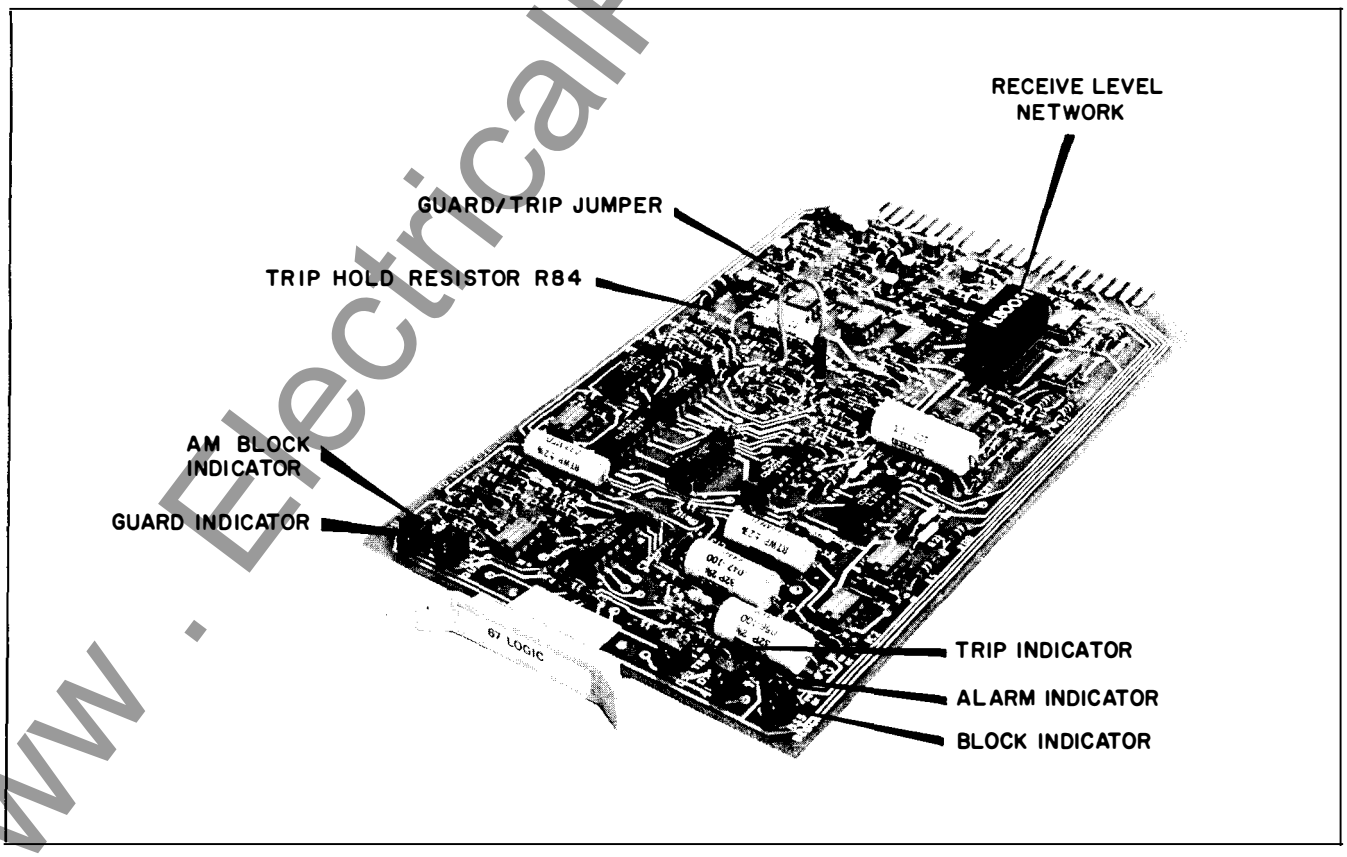


Figure 1. Logic Card

Reference to Figure 2 shows that IC4/B tests only for high-level limits, but on both channels. A signal above the high limit on either channel will cause the output of IC4/B to go low and, after inversion through IC6/A, this information appears as an output at Output-Terminal 1 for use elsewhere in the system, and at Pin 2 of IC7/B for further use on this logic card.

FS Guard Detection and Logic: Reference to Figure 2 will show that guard signals from Channels A and B are detected by IC14/A and IC15/A, respectively. Typical input signals are shown on this Figure. Consider the non-boost condition, when the non-inverting input of each of these opamps is fixed at approximately −1.5 V by network RZ16. With guard signals received at the inverting input of any level more negative than −1.5 V, the outputs of IC14/A and IC15/A each are high; and the output of NAND gate IC5/D, therefore, will be low. Through R48, this holds the inverting input of IC13/A low. Thus, its output is high, and the guard indicator, DS2, is excited.

While guard signal is being received, the trip detectors, IC3/A & B, IC14/B, and IC15/B all have their outputs at logic low. This negates any possibility for trip action, both by holding C2 charged through IC5/B and by holding the output of IC7/B high. Similar analysis of the high-level trip detectors, whose output levels are combined in IC5/C, will show that IC7/A holds C1 fully discharged. A simultaneous change of state of the outputs of IC7/A, IC7/B, and IC5/B is necessary to initiate and sustain a trip. Failure of any one to change state will either inhibit or cancel the trip action.

FS Trip Detection and Logic: When the received signal changes from guard to trip frequency, the signals from the six FS detectors all change their logic state. Consider the condition where the system has been arranged for non-boost operation. For this case, all six detectors, which are voltage comparators, are referenced to 1.5 Vdc. The low- and high-level trip detectors are referred to +1.5 V; the guard detectors to −1.5 V. For non-boost operation, the input signal to all detectors changes from more negative than −1.5 V to more positive than +1.5 V. By symmetry, it can be seen that with a change from guard to trip the outputs of IC5/B, IC5/C, and IC5/D all change state. Assuming no protective actions are prevailing, then the circuit is "normal" and the following action occurs:

(1) Output of IC7/A goes high, thus charging C1 whose time constant with R33 constitutes the pre-trip time delay established to defeat the possibility of the system's responding to trip-frequency noise of duration less than approximately 4.5 mS. It will be observed that the output of IC8/A does not change state until C1 charges above +6 V, which requires about 4.5 mS. Protective signals (discussed later) at Pin 3 and 4 of IC7/A can defeat this action.

(2) In analogous fashion, the output of IC8/B will not change state in response to a trip condition, which is a low at the output of IC5/B until C2 has discharged through R39 for about one time constant which, here, is about 10 mS. Thus IC8/A always responds to trip signal before IC8/B.

(3) Finally, excepting for protective action at Pins 2 and 8 of IC7/B (discussed later), the output of IC7/B, Pin 9, will go low when guard is removed.

Thus, excepting for protective actions, the following conditions are necessary and sufficient to initiate and sustain a trip:

(1) IC7/A output is high
(2) IC5/B output is low
(3) IC7/B output is low

The presence of these signals indicates that (1) the high-level trip detector senses a trip (IC7/A), (2) the low-level trip detector senses a trip (IC5/B), and (3) guard signal from IC7/B has been absent no more than 100 mS prior to the establishment of conditions (1) and (2). With these conditions prevailing, it is possible to follow the trip signal through the logic card to its output at Pin H.

With the output of IC7/A high (trip), Pin 2 of IC8/A also will be high about 4.5 mS later, owing to the time needed to charge C1 through R33. The output of IC8/A, then, will place a logic low at Pin 1 of IC10/A.

Next, the logic low (trip) at the output of IC5/B, Pin 4, will result in a delayed low at the input of IC8/B. The delay is about one time constant of C2 and R39, or about 10 mS. Thus, 10 mS after IC5/B delivers its trip signal, the output of IC8/B moves high and appears at input Pin 6 of IC10/B.

Third, the output of IC5/D goes high because of loss of guard due to trip. This causes the timing capacitor for guard-before-trip (C3) to charge instantaneously so that the inverting input of IC13/A drives the output of that opamp to a logic low. Besides removing excitation from DS2, the guard-condition indicator, the output of IC9/D is driven high, thereby causing the flip-flop, IC10/C & D, to introduce a logic high at Pin 5 of IC10/B. Coincidence of this logic high with one at Pin 6, IC10/B from IC8/B causes similar coincidence of logic signals at the input of IC10/A. With this coincidence, a "valid" trip signal appears as a logic high at the output of IC10/A, Pin 3.

From this point, the trip signal is easily traced to the output of IC11/B where the logical high of trip charges C8 almost instantaneously through R83. The resulting low at the output of IC12 drives Q2 and Q1 as an output signal for trip and excites DS3, the trip indicator, through IC6/C.

Protective Logic: Many systems of protective logic are incorporated, and most of them are executed on the logic card. Some are intended to prevent delivery of a trip signal when the signal received fails to conform to certain established standards. Others permit trip only after an established series of events, indicating validity, have, in fact, met the tests set for amplitude, duration, and sequence of signals. All contribute to the ability of the Series 6745 to exhibit good security without sacrificing dependability, and vice versa. The following discussion describes these features item-by-item.

The various sources of "block" information, or other conditions which will inhibit a trip-signal output, are listed and discussed in the following:

Item	Condition	Enters Logic At
(a)	Loss of guard signal	IC5/D, Pin 11
(b)	Loss of trip signal	IC5/C & IC5/B
(c)	Trip too late after guard	IC12
(d)	Signal level out of limit for Channel A or B	IC4/C
(e)	High- and low-limit noise	IC7/A, Pin 3 IC7/B, Pin 8 (note 1)
(f)	High-limit noise	IC7/B, Pin 2
(g)	Block input for delayed response	IC11/A, Pin 4
(h)	Block input for fast response	IC7/C, Pin 13
(j)	Noise block from narrow-band receiver or from diagnostic card	IC9/A, Pin 2
(k)	Block input from diagnostic card	IC11/B, Pin 1
(l)	Block and alarm circuit	
(m)	Undervoltage from power supply	Q7
(n)	Timing circuits	

(a) Loss of Guard Signal: When guard signal is present, a logic low is at the output of IC5/D, as discussed previously, and this presents a low at Pin 1 of IC7/B. Loss of guard signal reverses the situation, places a high at Pin 1 and a low at Pin 9 of IC7/B. Passing through IC9/B whose output goes high, the signal charges C6 quickly through CR11, and so causes a change of state at the outputs of IC13/B and of IC9/C and at Pin 3 of IC11/A, which integrated circuit is a collecting point for several protective-block signals.

The change at the output of IC11/A is to a logic low, and with this change C5 discharges through R31. If the loss of guard signal persists for one time constant (about 120 mS, here) the inverting terminal of opamp IC17/A, used as a voltage comparator, will cross the threshold at which it changes state and the output will go high and so introduce a low at the output of IC7/C, which is another collecting point for protective-block signals. It will be observed that the output of IC7/C normally is high and that C7, thus, is normally charged; and under normal conditions the charge on this capacitor holds the output of IC17/B low.

When any block information, such as loss of guard signal, moves the output of IC7/C low, C7 discharges rapidly through R58 and CR12 to move the output of IC17/B, Pin 7 high and so indicate a block, as follows:

(1) A block output (logic high) appears at Logic-Card-Terminal 11 for use elsewhere.

(2) Alarm timer, R69, C9 (discussed later) is activitated.

(3) The base of Q7 goes high, thus opening the transistor to cut off energizing current to K1, thereby releasing its contacts to indicate a block condition by whatever means has been chosen for the installation.

(4) Lamp DS5 is energized to signal visually that a block condition exists.

(5) The block condition is indicated by a logic high at Pin 12, IC9/D and at Pin 1, IC9/A, and used for further logical control.

With a logic high at IC9/A, Pin 1, reference to Figure 2 will show that Pin 2 of IC12 is held low through CR26, thus holding the output circuit in a block condition and thereby blocking the possibility of a trip. This condition is reinforced, also, by simultaneously placing a logic high at Pin 4 of IC7/A which, again, corresponds to a guard condition, for a logic high at any input of IC7/A inhibits the passage of a trip signal.

(b) Loss of Trip Signal: As a protective measure against false trips, the philosophy of the design requires that a trip signal persist for about 4.5 mS before it is accepted as being valid. This delay has been introduced as a protection against the possibility of spurious noise conforming to the pattern of a trip signal. It is known to be statistically unlikely that such an invalid signal would persist for a significant period of time.

To effect the delay, trip signal, which is a logic high at Pin 6 of IC7/A, will not be transmitted to Pin 2 of IC8/A until C1 has charged, for about one time constant, through R33. When C1 has charged above the reference voltage on Pin 3 of IC8/A, which requires about 4.5 mS, the trip will pass through the circuit. C1 and R33 are identified as the Pre-Trip Timer.

With Jumper G/T-T placed in the G/T position, a valid guard is required to precede every trip signal. With this Jumper in the T position, a valid guard must precede only the first trip signal received. Should the trip signal later be lost, as by carrier failure or other disturbance on the line, it is not necessary that a guard signal precede the trip signal to return the equipment to trip status when the trip signal returns.

(c) Trip Too Late After Guard: It was shown in (a) foregoing, that loss of guard signal for 100 mS or more results in a block (logic high) at Pin 4 of IC7/A. Thus, if a guard signal has not been present within the 100 mS period just prior to arrival of a trip signal, no trip is possible, because a block is applied to Pin 2 of IC12.

(d) Signal Level Out-of-Limit: Out-of-limit levels of incoming signal, either too high or too low, are sensed at the receiver. When either condition persists, a logic high appears at the logic card on Terminal 21 for Channel A, Terminal Y for Channel B. In either case, the condition appears as a logic high at Pin 5, IC11/A, and so initiates discharge of C5 through R31. If the condition persists for 100 mS or more, Pin 2 of IC17/A will drop below the reference voltage on Pin 3 and so initiate a block condition as described earlier.

(e) High- and Low-Limit Noise: Out-of-limit signal levels discussed in (d), foregoing, must continue for a period of time determined by the time constant of the automatic-gain-control (AGC) circuit of the receiver before protective action is taken. To protect against short bursts, or spikes, of noise, the four "window" or limit detectors of IC1 and IC2 are used. These all are opamp voltage comparators which change the state of their output when their reference levels, shown on Figure 2 are crossed. The four possibilities of high-limit and low-limit noise are collected in IC5/A, where any noise signal appears as a logic high at Pin 3 and, thus, as a block preventing trip at IC7/A.

(f) High-Limit Noise: Noise signals exceeding the predetermined high limit are collected at IC4/B and, so, appear as a block at the input of IC7/B. From there, they cause a logic high at the output of IC9/B which charges C6 nearly instantly through CR11, and so passes a block condition to the input of IC11/A. When the noise disappears, this block will continue for about 20 mS while C6 discharges through R50. For non-boost systems, it will be observed that the same action occurs also with high- and low-limit noise signals at Pin 8 of IC7/B. And, in all systems, a valid guard signal must persist at Pin 1 of IC7/B for 20 mS before block is released by discharge of C6.

(g) Block Input for Delayed Response: Terminal 13 of the logic card is provided for acceptance of a block signal from elsewhere. A logic high applied here will be delayed by the block timer, C5, R31, for about 100 mS, after which time the system will be blocked.

(h) Block Input for Fast Response: Terminal A of the logic card is provided for acceptance of a block signal from elsewhere with instantaneous response thereto. When a second logic card is used, its block output from Terminal 11 is connected to Terminal A of the first logic card.

(j) Noise Block Input: When the system is equipped with either a narrowband receiver or a diagnostic card, a block signal representing noise is introduced at Terminal 22, and delivered to the input of IC9/A. Response of the circuit is the same as to an internal block at the other input of IC9/A.

(k) Block Input: Terminal 14 has been provided primarily as a block-signal input from a diagnostic card, when used, although it may be used for any other purpose.

(l) Block and Alarm Circuit: If a block condition persists for more than about two seconds, the logic high corresponding to block at Pin 7, IC17B, will appear at the input, Pin 6, to IC18B because C9 discharges through R69. The resulting low at the output of IC18 excites the alarm indicator, DS4, and, through IC6/D, removes base drive to Q8. Loss of collector current in Q8 removes coil current from K2, on the block and alarm relay card, releases its contacts, and so activitates whatever alarm system has been provided.

(m) Undervoltage Protection: Provisions are made to block the output of a trip signal and to establish a block and alarm condition when the level of the power supply becomes less than either plus or minus 9.8 Vdc.

To effect this, the dc supply for Q1, Q2, Q7, and Q8 is taken from the collector of Q6, so when Q6 is open, an output signal clearly will be prevented. Q6 is controlled by the level of power-supply voltage. The operation of the circuit follows:

So long as the +12 V supply line is at a level greater than 9.8 V (9.1 V across zener CR21 plus 0.7 V E_{BE}) Q3 is a short circuit (saturated) and holds the base of Q5 at about zero volts through the divider of R98 and R100. Simultaneously, so long as the −12 V supply line is at a level greater (more negative) than −9.8 V (9.1 V across zener CR22 plus 0.7 V V_{BE}) Q4 is a short circuit (saturated) and so holds the emitter supply of Q5 at about −11.8 V. Thus, so long as power-supply output voltage is above the limits of plus and minus 9.8 V, Q5 is conducting, Q6 is forward-biased and saturated, and the supply voltage of Q1, Q2, Q7, and Q8 is 9.8 V or greater, so that dependability is assured.

If either power supply falls below 9.8 V, then either base or emitter of Q5 will be open-circuited to cut off Q6 and, thus, to remove supply voltage from the other transistors. Hence, protection against low power-supply voltage is effected. Finally, when Q7 opens, collector current drawn through K1 (on the block-and-alarm-relay card) drops to zero, thereby initiating a block signal by movement of the contacts of K1.

(n) Timing Circuits: There is a group of nine RC circuits each of whose time constants contribute to the system of protective logic. These will be described separately. Each timer is arranged so that its capacitor must charge, or discharge, for about one time constant to reach a new voltage level, after receipt of an input pulse, at which new level it will cause an opamp voltage comparator to change state. There is also an alternate path, through a diode, for fast charge or discharge, as the case may be.

(1) Pre-Trip Timer: C1 R33, time constant about 4.5 mS. This timer holds off response to a trip command for about 4.5 mS to ensure that the system does not trip on short bursts of noise. If a trip signal does not persist for at least 4.5 mS, there will be no response thereto when the channel spacing is 340 Hz. In systems using 680-Hz spacing, this period is reduced to 2.5 ms.

(2) Trip-Sequence Timer: C2 R39, time constant about 10 mS, this timer delays transmission of low-level trip signal for a period greater than the delay of the Pre-Trip Timer, which operates only on high-level trip signals. The delay is necessary to ensure that loss of guard at Pin 5 of IC10/B will give a logic low at output Pin 4 with the arrival of low-level trip at Pin 6.

(3) Guard Before Trip: C3 R48, time constant about 10 mS. This timer provides that there shall have been an acceptable guard signal present for at least 10 mS before

trip can be effected. With guard signal present, the output of IC5/D is low and C3 is discharged through R48. Loss of guard signal causes C3 to charge almost instantly through CR5 and thus change the output of IC13/A from high to low, where it will stay until its input-terminal 2 drops below about +6 V.

Upon return of guard signal, C3 will discharge slowly through R48 and IC5/D. About 10 mS later, its potential will drop below 6 volts and so cause IC13/A to change state and thereby acknowledge receipt of a valid guard signal for the prescribed period of time. Note that to unblock the system after a hard-block condition has occurred an undisturbed guard signal must be received for at least 100 mS to enable the system again to receive a trip signal.

(4)Trip Hysteresis: C4 R66, time constant about 20 mS. There is always the possibility that extraneous noise can be present in conjunction with receipt of a trip signal, but this need not invalidate the trip. The noise, however, will introduce rapid blocking at IC7/A which could cancel the trip permanently owing to the possible absence of guard signal for more than 100 mS prior.

At the start of trip, C4 is charged rapidly through CR13 and R65. Thereafter, with a brief loss of trip it discharges slowly through R66 and so holds Pin 8 of IC9/C high for about one time constant. This prevents the block signal at Pin 9, IC9/C, due to absence of guard, from becoming effective at Pin 10 of IC9/C.

(5)Block Timer: C5 R31, time constant about 100 mS. This timer delays transmission of a block signal from IC11/A, Pin 6, for about 100 mS. Block signals of shorter duration are considered transient and relatively inconsequential, so that the system is protected only during the period of the disturbance, and no longer. Block signals of greater duration, as sensed by this timer, initiate further protective action by activitating the Restore Timer C7, R57. A new 100 mS period of undisturbed guard is required to remove the block condition.

(6)Pulse Stretcher: C6 R50, time constant about 20 mS. Whenever a short noise spike is received, this timer charges C6 rapidly through CR11 and then holds the block condition for about 20 mS. It also stretches a loss-of-guard signal, and so requires a good-quality guard signal for at least 20 mS before the block is released.

(7)Restore Timer: C7 R57, time constant about 100 mS. This timer establishes that all prohibitions against trip must have been removed for at least 100 mS before trip is permitted. It restores permission to trip about 100 mS after the output of IC7/C goes high, but it restores a block condition rapidly through CR12 if block, a logic low, appears at the output of IC7/C.

(8)Trip Hold: C8 R83. This timer is optional, and its time constant is selected when the system is specified. C8 charges rapidly when trip is received and holds it for RC seconds by holding the input of IC12 high. It is useful for ensuring completion of the trip action when such completion is essential even though the communication system may have failed or become noisy.

(9)Alarm Timer: C9 R69, time constant about 2 sec. This time holds the block signal from the input to IC18/B for about 2 sec., after which the alarm signal is released to Q8, and DS4 is excited.

Except for the alarm timer, all timing capacitors are returned to ground. C9 is returned to +12 V so that in the event of power failure followed by subsequent restoration of power the alarm will not cease until both guard signals have been received for 100 mS.

From the action of these timers, it is apparent that three distinct levels of protection have been established:

(a) For faults lasting less than about 100 mS, the system blocks during the fault, but is fully operative immediately thereafter.

(b) For faults lasting more than 100 mS, but less than 2 Seconds, the system waits for about 120 mS after the block condition is removed before trip is permissible.

(c) For faults lasting more than about 2 Seconds, the alarm timer alerts supervisory personnel.

Voltage Reference: IC18/A is an opamp connected as a voltage follower. Its input, from divider across the +12 V power supply, is about +6V. Thus, at its output there is +6 V available with very low source impedance, and this is used as a reference for many opamp voltage comparators on the logic card.

Trip-Boost Operation: For simplicity, the foregoing discussion of logic functions was based on a system without the trip-boost feature. The following describes the changes effected when trip boost is added.

Both duration and amplitude of trip boost may be selected quite arbitrarily, as an option, when the equipment is specified. An increase beyond 12 dB, however, is not recommended. When Bell System circuits are used, other limitations apply on amplitude and time; and it is recommended that References 1 and 2 of the Bibliography be used when establishing the trip-boost characteristic.

To describe the operation of a logic system using trip boost, it will be assumed that a 12 dB boost, lasting for 70 mS, has been selected. For this system, plug-in network RZ16 is specified so that:

R4–5 is open

R10–15 and R7–2 are scaled to provide a reference of –0.375 V

R11–16 and R14–9 are scaled to provide a reference of +0.375 V

R3–8 and R6–1 are scaled to provide an AGC reference of 1.0 V

Under the foregoing conditions, input signals from Channels A and B will be 1.0 V, as determined by the AGC reference level. Reference levels for the four window detectors of IC1 and IC2 have not been changed, and so the system will block at IC7/A because the AM signals received are below the low-limit level of 2.8 V. Note, however, that because of the removal of R4—5 in RZ16 the block signal does not appear at Pin 8 of IC7/B. Thus, guard signal is not blocked. It should be noted, however, that in any system using trip boost the AM-block indicator, DS1, will always be excited except during periods of trip boost.

The level of FS input signals, from both channels, which was just above 1.5 V in non-boost operation, is now about 0.7 V. But, with the reference levels for the trip and guard detectors now at 0.375 V, these detectors function as previously described, and all guard and protective features are operational.

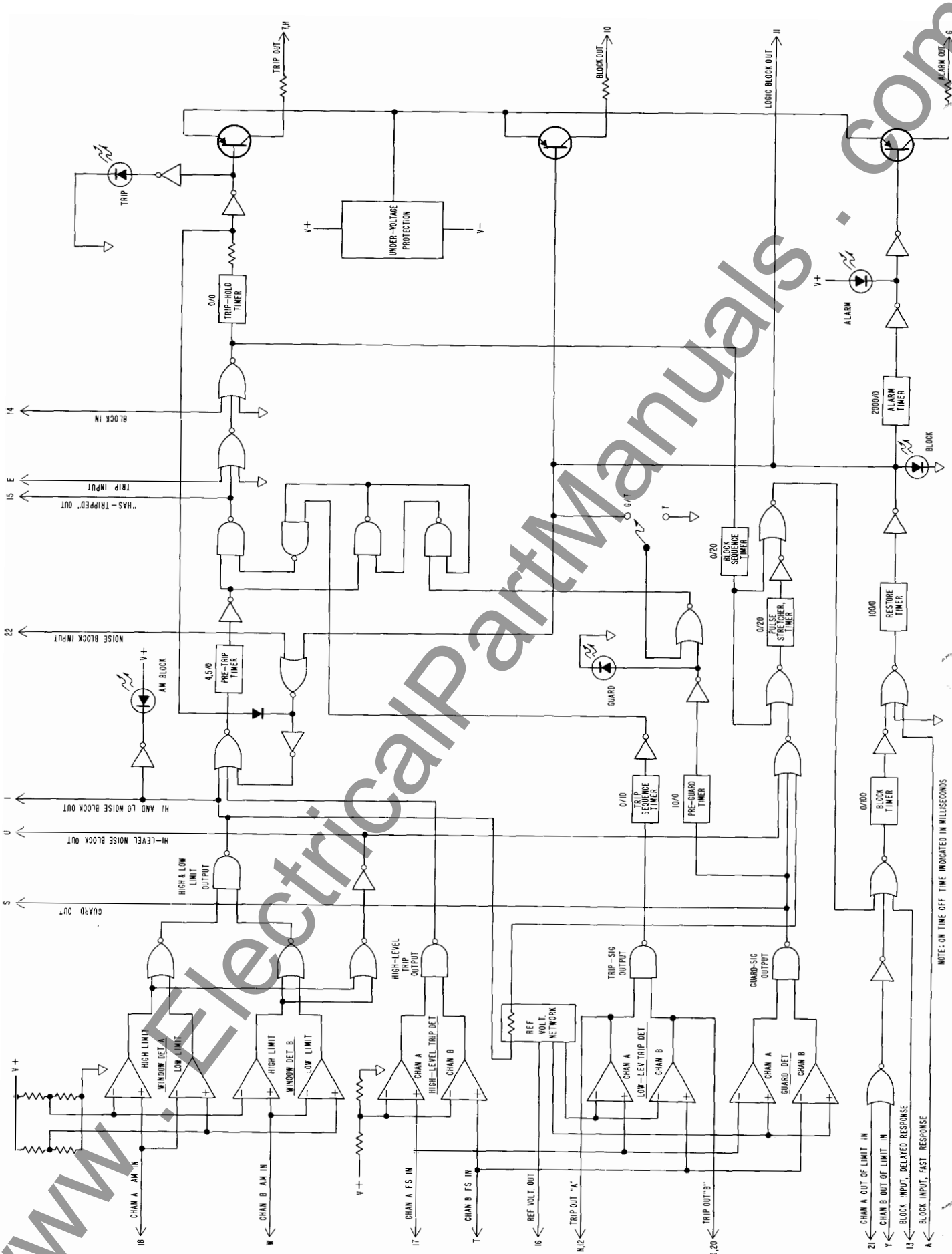
When the boosted trip signal arrives, the AM signal now rises to a level of 4 volts and so removes the block signal at IC7/A.

The arrival of boosted FS trip signal at the high-level detector, IC3, and its propagation through the circuit, starting at IC7/A occurs as previously described for the non-boost case. Simultaneously, the trip-output signal from the low-level trip detectors, delayed only by the trip-sequence timer, passes through IC8/B and introduces a logic high at Pin 6 of IC10/B. At the same time, loss of guard signal places a logic high at the other input of IC10/B. These combine for a logic low at output and, thus, at the input of IC10/A, Pin 2.

The logic low at Pin 1 of the same gate, caused by the high-level trip signal, causes a high, which is a trip, at the output. At the end of the boost period, the AM detectors will return to block and so cancel the signal from the high-level detectors and thereby introduce a high at Pin 1 of IC10/A. Low-level trip signal is still present, however, and so the trip-output signal from IC10/A will continue so long as a trip signal is present at the input, even though at low level. It is clear, however, that no trip can be initiated with the presence of only a low-level signal.

Table of Replaceable Parts

DIAGRAM SYMBOL	NAME OF PART AND DESCRIPTION	PART NO.
	MODEL 67 LOGIC, HB-41020	
	CAPACITORS	
C1	Capacitor, poly., 0.047 μF, 2%, 100 V, Wesco 32P	H-5115-67
C2 & 3	Same as C1, 0.033 μF	H-5115-59
C4	Same as C1, 0.1 μF	H-5115-83
C5 & 7	Capacitor, tantalum, 1 μF, 10%, 35V, Union Carbide T110A105K035AS	H-1007-1156
C6	Same as C1, 0.056 μF	H-5115-71
C8	Same as C1, 0.01 μF	H-5115-35
C9, 11, & 12	Capacitor, tantalum, 15 μF, 20%, 20 V, Corning CCD-020-156-20	H-1007-716
C10	Capacitor, tantalum, 0.33 μF, 20%, 35 V, Corning CCT-035-334-20	H-1007-871
C13	Capacitor, tantalum, 3.3 μF, 20%, 35 V, Corning CCL-035-335-20	H-1007-1260
	RESISTORS	
R1, 2, 3, 4, 9, 10, 31, 33, 39, 41, 48, 50, 57, 69, 102, & 103	Resistor, metal film, precision, per RFL Spec HA-38301, value per schematic	H-1510-(xxx)
R5 thru R8, R11 thru R30, R32, R34 thru R38, R40, R34, thru R47, R49, R50 thru R56 R58 thru R68 R70 thru R83 R85 thru R101 R104 thru R113	Resistor, fixed composition, 10%, ¼ W, Allen Bradley CB or eq.	H-1009-(xxx)
R87	Same as R1, value per sales order	H-1510-(xxx)
	SEMICONDUCTORS	
CR1 thru CR20 CR23 thru CR26	Diode, silicon, Type 1N914B	HA-26482
CR21 & 22	Diode, zener, 9.1 V, 5%, 400 mW, Type 1N960B	HA-41014
DS1 thru DS5	Light – emitting diode, Dialight 550-0102	HA-39568
IC1, 2, 3, 8, 13, 14, 15, 17, & 18	Integrated circuit, linear dual opamp., National LM1458N, or eq.	H-0620-51
IC4 & 9	Integrated circuit, COS/MOS, Quad. 2-input NOR, RCA CD4001AE, or eq.	H-0615-3
IC5 & 10	Integrated circuit, COS/MOS, Quad. 2-input NAND, RCA CD4011AE, or eq.	H-0615-5
IC6	Integrated circuit, COS/MOS Hex Inverter/Buffer, RCA CD4049AE, or eq.	H-0615-7
IC7 & 11	Integrated circuit, COS/MOS Triple 3-input NOR, RCA CD4025AE, or eq.	H-0615-20
IC12	Integrated circuit, linear high-perf. opamp., National LM741CN, or eq.	H-0620-52
Q1, 6, 7, & 8	Transistor, silicon, PNP, Type 2N2907A	HA-37439
Q2, 4, & 5	Transistor, silicon, NPN, Type 2N2222A	HA-37445
Q3	Transistor, power, PNP, National 2N4249, or eq.	HA-41919



Logic Diagram, Model 67 Logic.

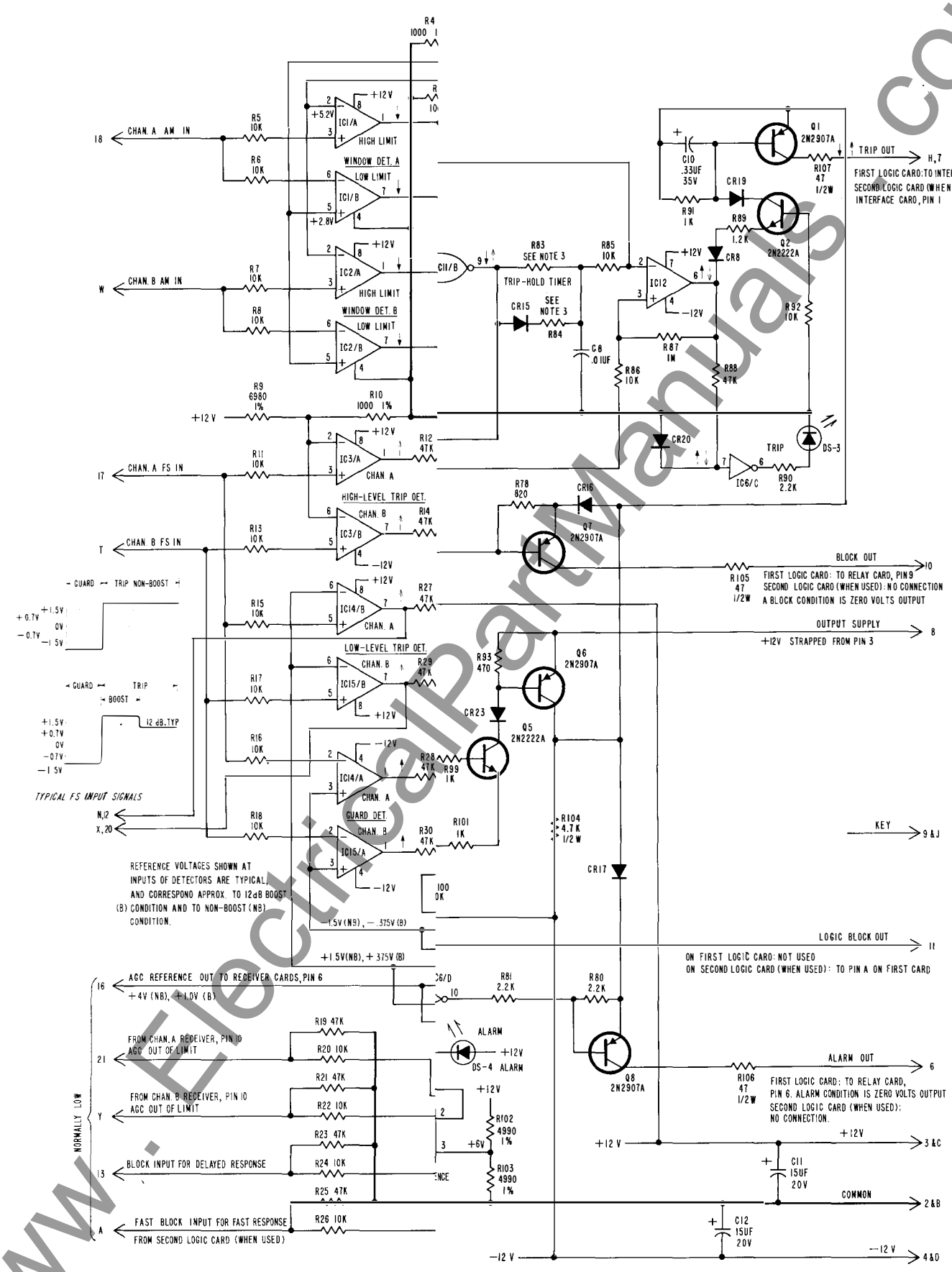


Figure 2. Schematic of Logic Circuits

Interface Card, Model 67B INTER

General: The interface card is provided to connect the Series 6745 equipment to the external devices with which it is associated. Interfaces for trip input, trip output, and communication circuits are collected at this point. The card also protects the equipment from any transient potentials that may be induced in input or output lines. Figure 3 details the circuits involved.

Signal Interface: Transformers T2 and T3 provide line matching in either 2-wire or 4-wire form. CR18 and CR19 protect against high, transient voltages that may be induced. C4, C5, C7, and C8, in conjunction with the inductance of T2 and T3, provide high-pass filters with a low-frequency cutoff at about 375 Hz. Jumpers A, B, C, D, and E may be adjusted in the field for choosing between 2-wire and 4-wire systems, and for selecting the range of transmitter-output level desired.

Trip-Input Circuits: Two optical isolators are used to key the transmitter from guard to trip. The isolators have a breakdown-voltage rating of 2300 Vac. Reference to Figure 3 will show that jumpers G and H have been provided so that Channels A and B can be tripped from a single source (ST position), or the jumpers may be plugged so that dual sources of trip (DT) are required.

Trip is effected by passing a current through the trip-input terminals at TB1, Terminals 1 through 4. The current-limiting resistor is installed externally, at the barrier-strip terminals of the 68 CHAS; and resistance values for different station-battery voltages are listed on the installation (CR) drawings supplied with the equipment.

Trip-Output Circuits: Trip output is effected with a floating electronic switch, based upon use of an NPN transistor driven by an optical isolator. Through the use of an isolator and an independent, floating power supply, the trip-output circuits are completely isolated from ground and from the balance of the equipment.

The circuit is relatively simple. Trip signal from the logic card excites a light-emitting diode in IC1 and so provides base drive to the transistors in IC1 and to Q1. The output transistor, Q1, acts as a switch for the external load circuit, it is protected against transients by CR16.

Greater security is available by use of a second trip-output circuit, 67B INTER–1, also shown on Figure 3. Its physical form is as a "piggy-back" plug-on to the main board, and its layout is a mirror image of the basic circuit. Use of this option requires the use, also, of a second (redundant) logic card.

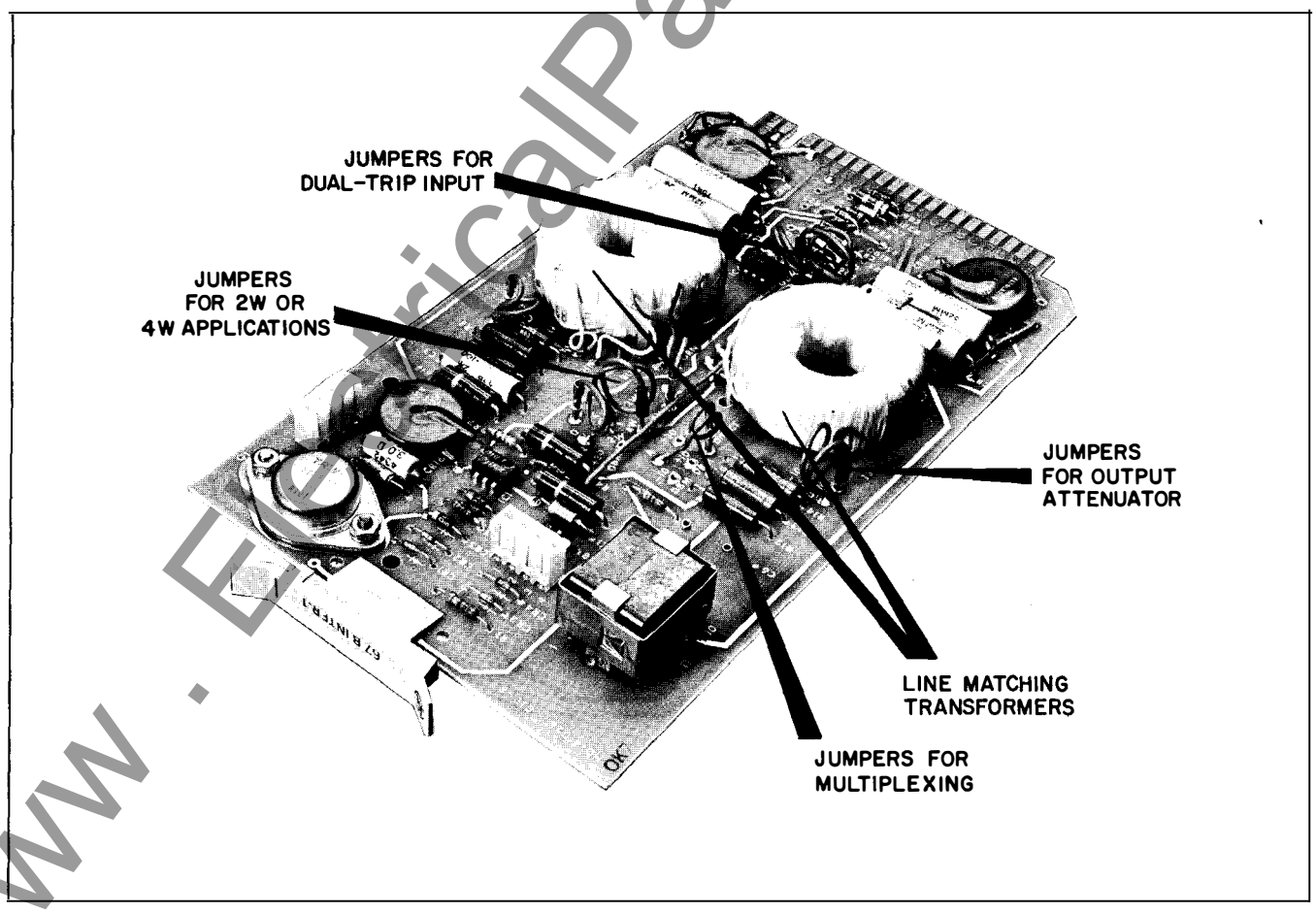


Figure 1. Interface Card

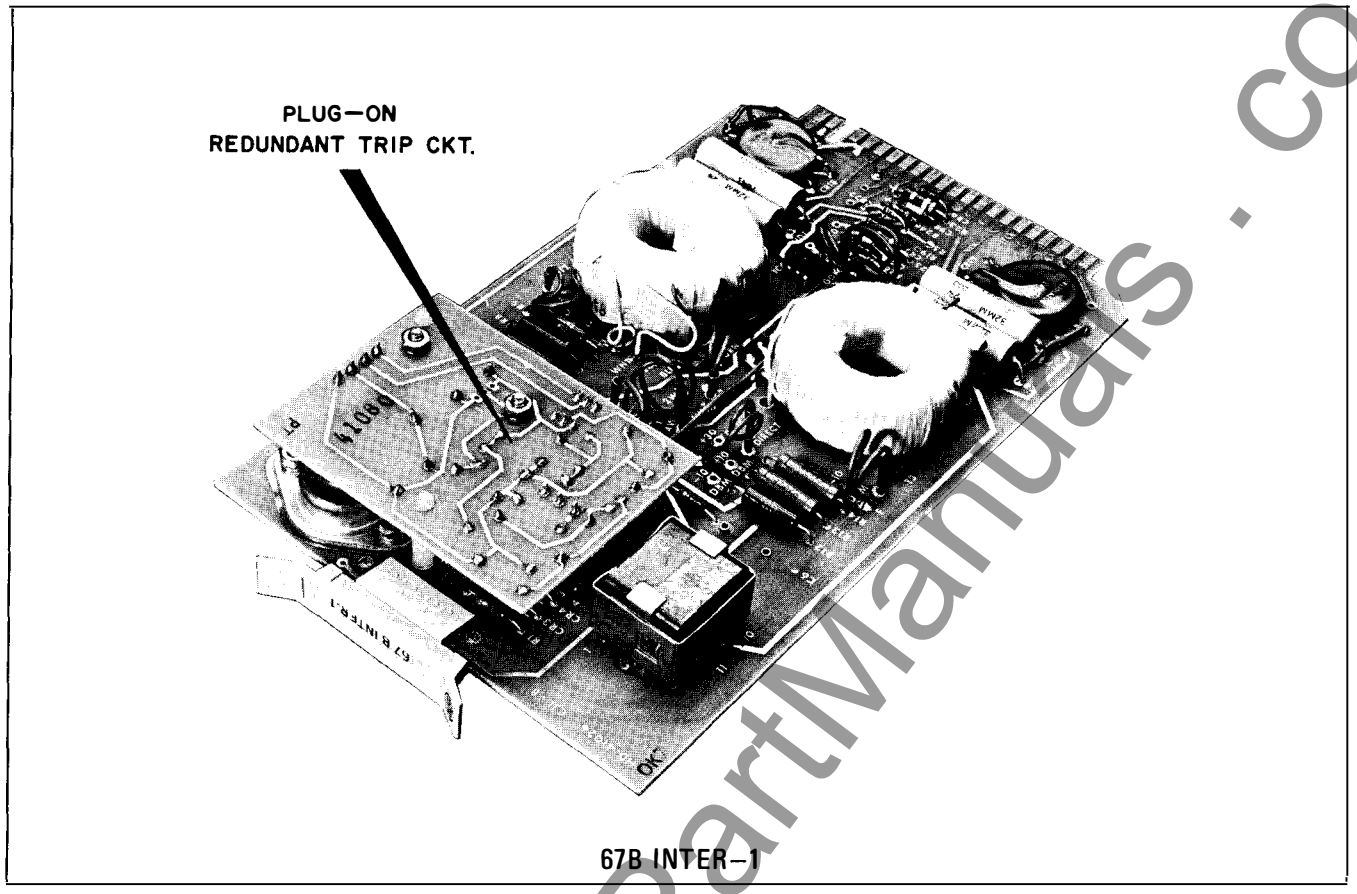


Figure 2. Optional, Redundant Trip-Output Circuit for Interface Card

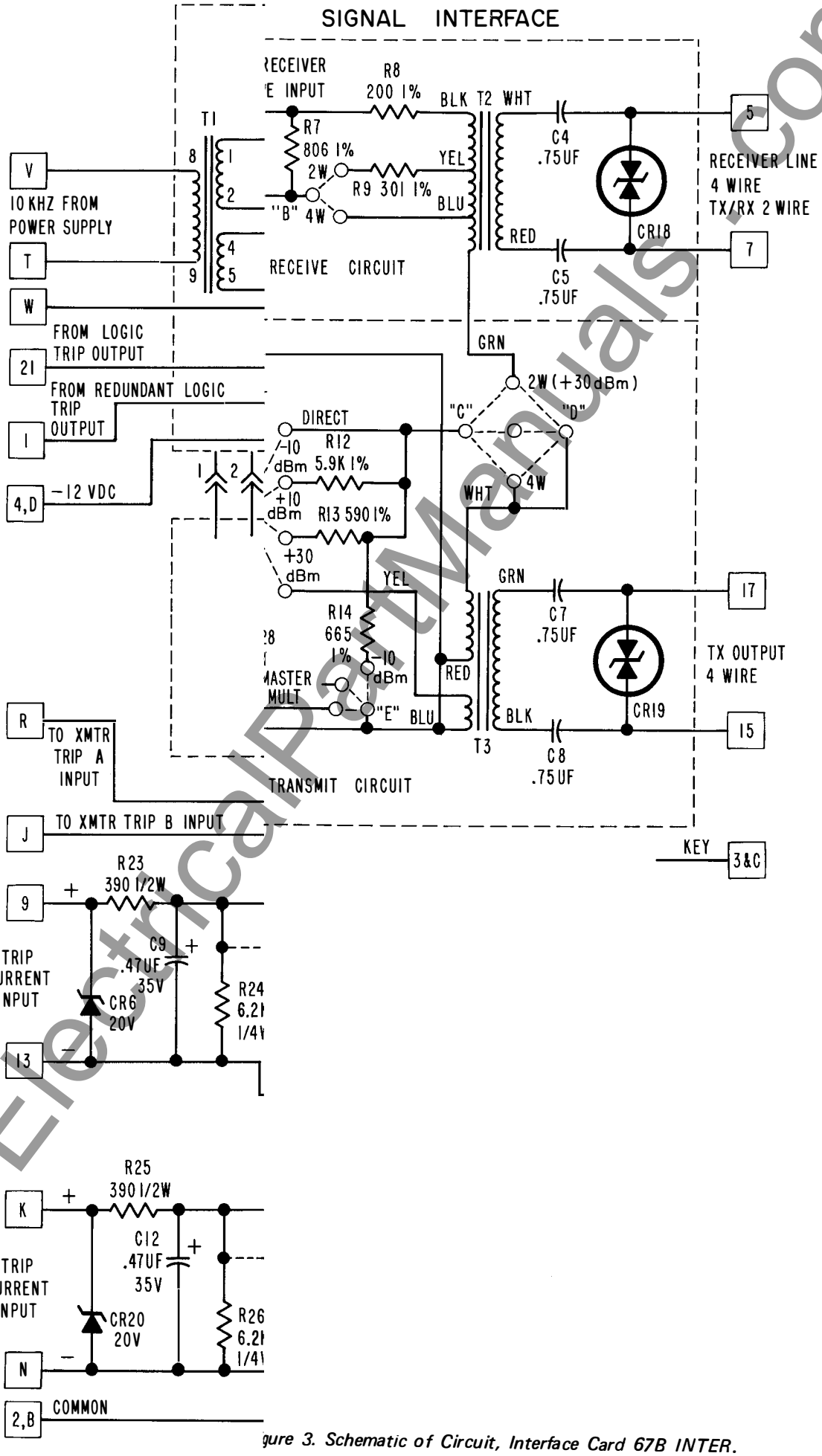
DIT–1 PROTECTIVE RELAYING Module Designation	HB-46170 Interface Card	HB-41080 Sec. Trip Out	HB-45780 Interface Rec. Only	HB-45770 Interface Trans. Only				
67B INTER	•							
67B INTER–1	•	•						

Table of Replaceable Parts

DIAGRAM SYMBOL	MODEL	NAME OF PART AND DESCRIPTION	RFL PART NO.
		CAPACITORS	
C1	All	Capacitor, met. poly.: 0.1 μF, 10%, 250 V, Seacor 106-01	H-1007-1255
C2	All	Capacitor, electrolytic: 50 μF, -10% - +100%, 150 V, C-D WBR-50-150	H-1007-1263
C3	All	Capacitor, mylar, 2.2 μF, 5%, 200 V, Wesco 32MM	H-1007-833
C4	All 129 V	Same as C1	
C4	All 48 V	Same as C1	
C4	All 24 & 12 V	C4 is omitted	
C5	All 129 V	Capacitor, tantalum: 6.8 μF, 20%, 35 V, Corning CCD-035-685-20	H-1007-655
C5	All 48, 24 V, & 12 V	Capacitor, tantalum: 2.2 μF, 10%, -25 V	H-1007-752
C6 & 7	All	Capacitor, tantalum: 22 μF, 20%, 35 V, Corning CCZ-035-226-20	H-1007-657
C8 & 11	All 0.375-A		
C9 & 12	All 0.375-A	Capacitor, met. poly.: 0.1 μF, 10%, 250 V, Seacor 106-0.1	H-1007-1255
C10 & 13	All with O-V Protection	Capacitor, met. poly.: 0.1 μF, 10%, 250 V, Seacor 106-0.1	H-1007-1255
C14	All	Capacitor, ceramic disc: 0.005 μF, -20 - +80%, 3 kV RMC 3KV5000Z5U	H-1007-1264
C15	All 129 V	Capacitor, dipped mica, 470 pF, 2%, 500 V, Electro Motive DM-19	HA-16632
C15	All 48 V	Capacitor, dipped mica, 2000 pF, 5%, 500 V, Electro Motive DM-20	HA-16222
C15	All 24 & 12 V	Omitted	
		FUSES	
F1 & 2	All 129 V	Fuse, slo-blo, ¾ A, 125 V	HA-10780
	All 48 V	Same, 1.5 A	HA-35852
	All 24 & 12 V	Same, 3.0 A, 125 V, Littlefuse 313 003	HA-6607
F3 & 4	All with O-V Protection	Fuse, 1.5 A, 250 V, 3AG, Littlefuse 312-01.5	HA-41524
		INDUCTORS	
L1	All	Choke, Ferrite-core, 100 μH, 2 A, 0.103 ohm, Caddel Burns 6310-8	HA-41074
T1	All	Transformer, inverter-driver	HB-38366
T2	All 129 V	Transformer, power	HB-38061
T2	All 48 V	Transformer, power	HB-38062
T2	All 24 V	Transformer, power	HB-41939
T2	All 12 V	Transformer, power	HC-46357

Table of Replaceable Parts

DIAGRAM SYMBOL	MODEL	NAME OF PART AND DESCRIPTION	PART NO.
		MISCELLANEOUS COMPONENTS	
S1	All	Switch, toggle SPDT: Right angle mtg. C & K Components 7101-A	HA-39562
TP1 & 3	All	Test jack, red: Cinch 119437-B	HA-38116-2
TP2 & 4	All	Test jack, black: Cinch 119437-C	HA-38116-3
		RESISTORS	
R1	All 129 V	Resistor, fixed comp.: 15 K, 5%, 2 W, Allen Bradley HB	H-1009-251
	All 48V and All 24V & 12V	Same as above, 2.7 K	H-1009-1062
R2	All 129 V	Resistor, fixed.: 33 ohm, 5%, 2 W, Allen Bradley HB	H-1009-1064
	All 48 V and All 24V and 12V	Same as above, 22 ohm	H-1009-1063
R3	All 129 V	Resistor, fixed comp.: 12 ohm, 5%, 1W, Allen Bradley GB	H1009-1065
	All 48V and All 24V and 12V	Same as above, 10-ohm	H-1009-4
R4, 5, 6, & 7	All with O-V Protection	Resistor, fixed comp.: 47 ohm, 5%, ¼W, Allen Bradley CB	H-1009-832
R8	All	Resistor, fixed comp.: 3K, 5%, 1 W, Allen Bradley GB	H-1009-466
R9	All	Resistor, fixed comp.: 5.1 ohm, 5%, ½W, Allen BradleyGB	H-1009-712
		SEMICONDUCTORS	
CR1, 2, 12, 13	All	Diode silicon, Type 1N914B	HA-26482
CR3 & 4	All	Rectifier bridge assy., Varo VS-148X	HA-39509
CR5 & 7	All with O-V Protection	Diode, zener: 14 V, 5%, 500 mW, Type 1N5244B	HA-41075
CR6, 8, 10, 11	All 0.375-A units	Diode, rectifier: 1 A, Type 1N4003, Solitron S4Q03TA20	HA-30769
DS1	All	Light-emitting diode, Dialight Cp. 550-0102	HA-39568
IC1 & 2	All	Three-terminal voltage reg., Fairchild UGH 7812393 National LM340-12T	H-0620-69
Q1 & 2	All 129V	Transistors, matched pair	HA-46756
	All 24V & 12 V	Transistors, matched pair	HA-46757
SCR1 & 2	All with O-V Protection	Silicon controlled rectifier, Motorola 2N4441 or GE C122F	HA-41072
	All	Schematic	HD-41502
		PARTS LIST FOR 1-AMP EXTERNAL REGULATOR, P/N HB-41520	
C1 & 2	All 1-Amp.	Same as C8 in basic unit	
C3 & 4	All 1-Amp.	Same as C9 in basic unit	
CR1, 2, 3, & 4	All 1-Amp.	Diode, rectifier, 1 A, Type 1N4003	HA-30769
IC1 & 2	All 1-Amp.	Same as in basic unit	



gure 3. Schematic of Circuit, Interface Card 67B INTER.

Block and Alarm Relay Card, Model 67 RELAY

Description: The block and alarm relay card is equipped with two 24-volt relays, each with two sets of Form C contacts. The 2-Ampere contacts are silver, gold-diffused.

There is ample space on the card for mounting additional relays, or other components, if the user so desires. Of the 44 pins available on the card, only 19 are used, so that many terminals are available for use with additional equipment, if desired.

Operation: The coil of each relay is held energized by circuits on the logic card, so long as no block or alarm condition occurs. If a block, or alarm, condition arises, the logic circuits will interrupt the coil current, and thus cause the contacts to fall to the de-energized position. Release of the contacts can be used to create any signal desired to indicate the unsatisfactory condition. Visual signals, audible signals, or both frequently are used.

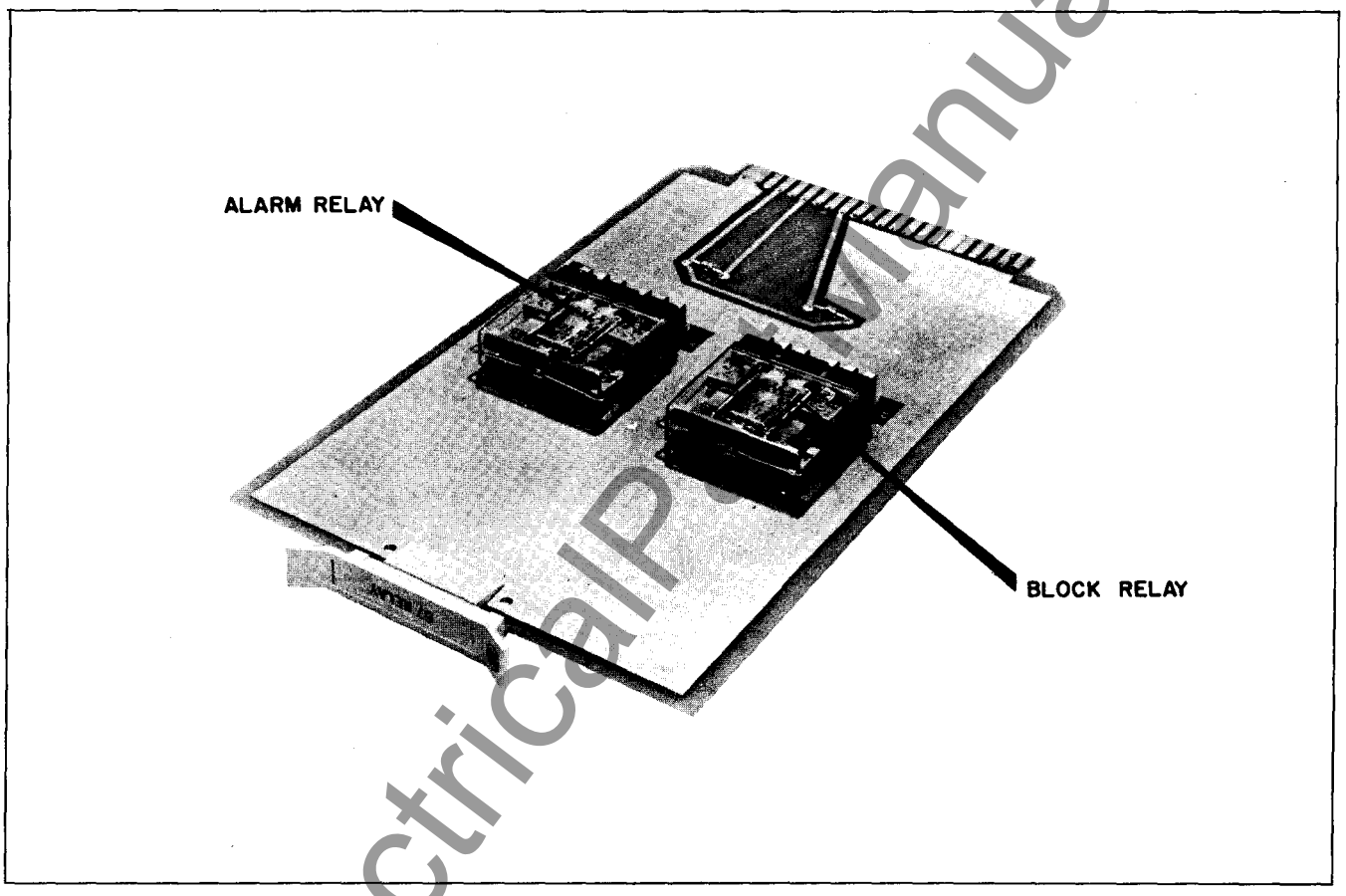


Figure 1. Block and Alarm Relay Card, Series 6745.

Table of Replaceable Parts

DIAGRAM SYMBOL	NAME OF PART AND DESCRIPTION	PART NO.
	MODEL 67 RELAY, HB-41035	
CR1 & 2	Diode, silicon, Type 1N914B	HA-26482
K1 & 2	Relay, P/C mtg. two Form C contacts, silver, gold-diffused 2 amps., Coil: 800 ohms, 24 Vdc Potter and Brumfield R40-E1-W2-V800	HA-46592

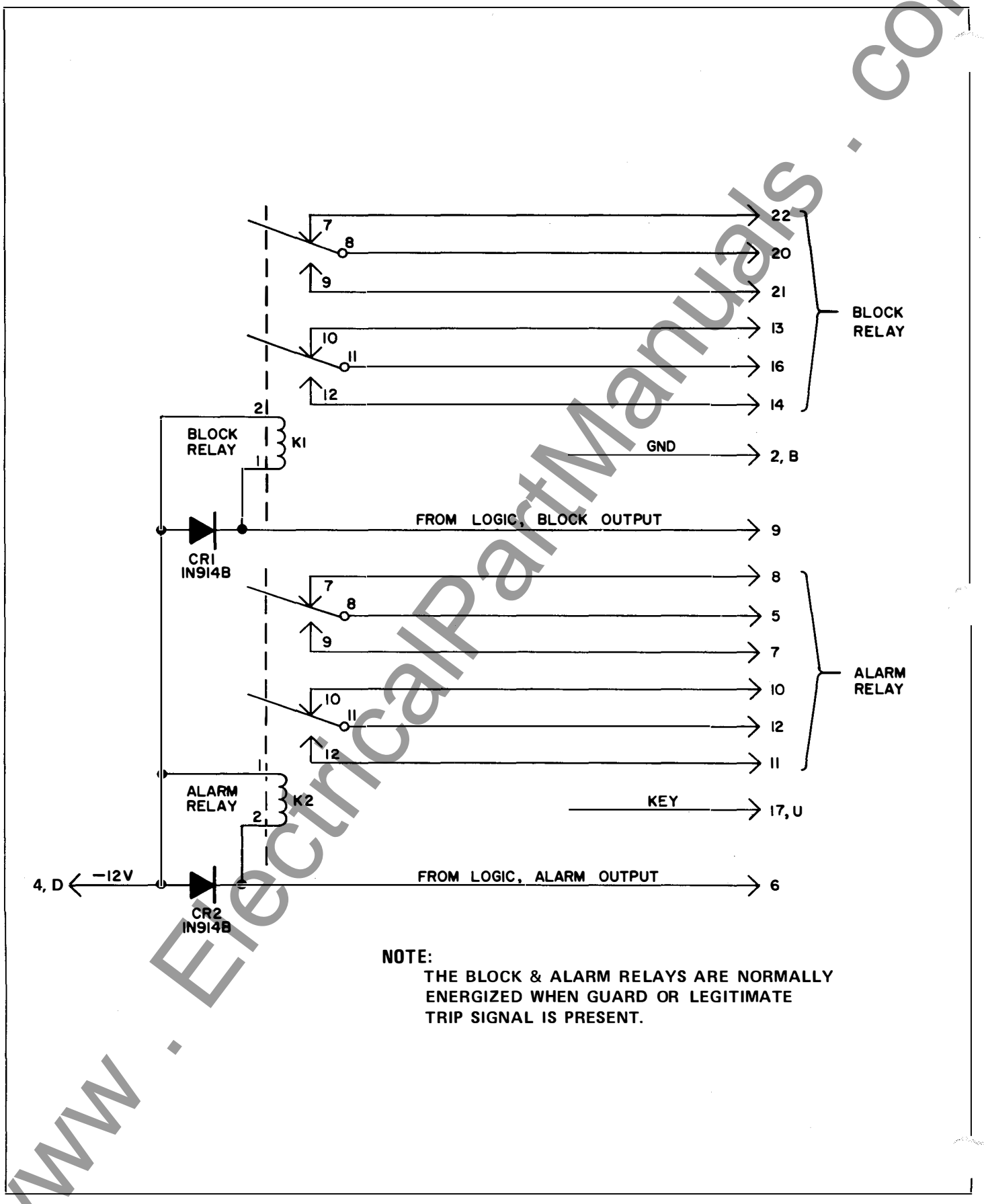


Figure 2. Schematic of Block and Alarm Relay

SERIES 6000 DC-DC CONVERTER POWER SUPPLIES

MODELS:

68 PS 12DC

68 PS 24DC

68 PS 48DC

68 PS 129DC

68 HPS 24DC

68 HPS 48DC

68 HPS 125DC

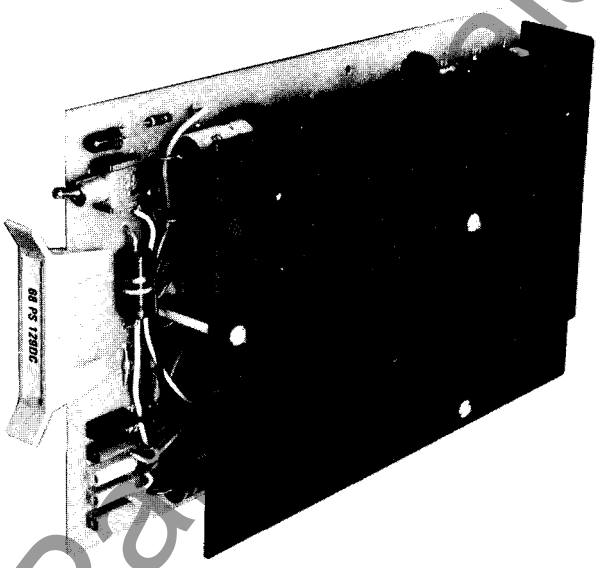


Figure 1. Typical 0.375-Ampere DC-DC Power Supply. Metal bracket spanning the circuit card is the heat sink for IC1 and IC2.

DESCRIPTION

These seven DC-DC Converters are part of the group designed to supply necessary dc power to the DIT-1 and DIT-1T equipment. Power supplies operating from an ac source are not described in this data sheet. All power supplies provide dual 12-Vdc outputs which are isolated and surge-protected from the primary-power source. The two 12-volt outputs are completely independent and may be wired externally to obtain plus and minus 12 Vdc, +24 Vdc, or -24 Vdc. An auxiliary 10-kHz squarewave output has been provided for low-power external functions.

Models with "PS" in their designation utilize an integral series-pass-type voltage regulator and will deliver 0.375 ampere from each, independent output.

Models with "HPS" in their designation utilize an external regulator and heat dissipator, and will deliver 1 ampere from each independent output.

As suggested by their model numbers, both low-current and high-current models are available for operation from primary-power sources with levels of 104-140 Vdc (nominal 125 V), 42-56 Vdc (nominal 48 V), 21-28 Vdc (nominal 24 V); or 10.5 - 14 Vdc (nominal 12 V).

Overvoltage protection, based upon the familiar crowbar principle, is optional on all models. Its presence is indicated by adding the suffix "-1" to the model number.

Table 1 summarizes the various models.

THEORY OF OPERATION

These supplies use a two-transformer inverter, as shown on Figure 6. Power transistors Q1 and Q2 act as switches alternately turning on and off, and so reversing the flow of primary current through T2.

In both T1 and T2, the sides of the windings indicated by dots have the same polarity. When Q1 is on, for example, all the dotted sides are positive. The secondary windings of T1 hold Q1 on and Q2 off. When the flux density of T1 reaches stauration, its voltages drop to zero and then reverse. At this point, Q2 turns on and Q1 turns off, and the sequence starts over again. The frequency of oscillation is approximately 10 kHz.

The output of T2 is rectified and filtered by CR3, CR4, C6, and C7. IC1 and IC2 are integrated circuits

functioning as series regulators. In low-current converters, these regulators are located on a heat sink attached to the circuit board carrying all other circuits. For one-ampere converters these series regulators and their associated filter capacitors C8 and C9, or C11 and C12, are located on the external heat dissipator of Option HB-41520. Notes on Figure 6 describe the physical and electrical differences. The schematic of Option HB-41520 is shown in Figure 5.

On converters equipped with overvoltage protection (OVP), the output voltage is monitored by zener diode CR5 or CR7. If output voltage exceeds the zener voltage, current through R5, or R7, will fire the gate of SCR1, or SCR2, and the SCR thus becomes a short-circuit across the power supply. The current so drawn will destory Fuse F3, or F4 and, so, drop the output voltage to zero. Power to the load cannot be restored unless the fuse is replaced, and should not be restored until the fault is cleared.

An auxiliary 10-kHz squarewave output is available at Pins 17 and 18 for external functions. The output will vary between 34 and 52 volts, peak-to-peak, depending upon input voltage to the converter. The sum of currents taken from Terminals 17 and 18 plus that from the lower output circuit, Figure 6, should not exceed 1 ampere.

TECHNICAL DATA

Input Voltage: 12-volt units: 10.5-14 Vdc
24-volt units: 21-28 Vdc
48-volt units: 42-56 Vdc
125-volt units: 104-140 Vdc
Allowable ripple: 1.5 Vrms, max.

Output Voltage: Two independent 12-Vdc outputs, not adjustable. Each output will be between 11.4 and 12.6 V for any combination of input voltage, load, and temperature.

Output Current: 0.375 A max. from each output for 68 PS units, 1.0 A from each output for 68 HPS units. See Figure 4 for max. total rating of 68 PS units.

Overvoltage Trip: 13.5 to 15.5 Vdc, not adjustable.

Ambient Temperature: -30°C to +70°C.

Size: 1.5" x 4.713" x 8". Requires three module increments in Model 68 Chassis for either high-current or low-current modules. In addition, 1-Ampere units require space at rear of 68 Chassis for mounting HB-41520, for which provision is made with certain backplates.

TABLE I

Module Designation

Module Designation	HB-41505 1 A Pwr. Sply. - 125VDC	HB-41515 1 A Pwr. Sply. - 48 VDC	HB-41935 1 A Pwr. Sply. - 24VDC	*HB-41520 Pwr. Sply. Reg.	HB-41535 Overvolt. Prot. Opt.	HB-41500 Pwr. Sply. -125VDC	HB-41510 Pwr. Sply. - 48VDC	HB-41930 Pwr. Sply. - 24VDC	HB-46350 Pwr. Sply. - 12VDC	
68 HPS 129DC	•			*•						
68 HPS 129DC-1	•			*•	•					
68 HPS 48DC		•		*•						
68 HPS 48DC-1		•		*•	•					
68 HPS 24DC			•	*•						
68 HPS 24DC-1			•	*•	•					
68 PS 129DC						•				
68 PS 129DC-1					•	•				
68 PS 48DC							•			
68 PS 48DC-1					•		•			
68 PS 24DC								•		
68 PS 24DC-1					•			•		
68 PS 12DC									•	
68 PS 12DC-1					•				•	

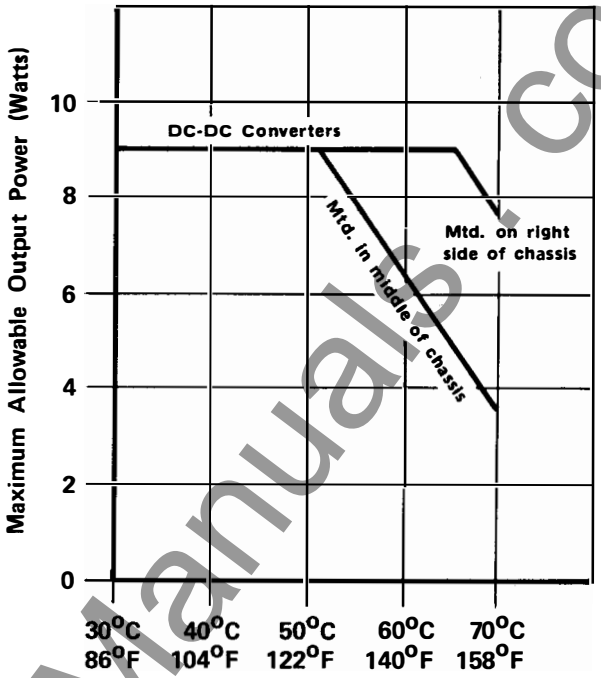
*This regulator is a unit separate from the power supply, but is always required except when ordering spare or replacement modules.

INSTALLATION

The accompanying curve shows recommended deratings for all 0.375-ampere power supplies. It does not apply to one-ampere units, for which no derating is required owing to their external heat sink. These curves are based upon maximum input voltage and upon installation in a chassis which itself was mounted between two unventilated chassis in a 19-inch rack.

Other considerations can modify the curves. If forced air is used, the curves will improve. On the other hand, the temperature inside a chassis will rise approximately ½°C per watt dissipated in the chassis itself and so cause the curves to worsen. A small improvement is obtained when an air gap of 1-¾ inches is left between chassis.

The power output is based upon the sum of the powers taken from the two output sections. One side of the supply may be used at a higher output current than the other; and it is necessary only to keep the total power output below the derating curves. Of course, the maximum output-current levels given in the Specifications should not be exceeded.



Derating curve for all 0.375-ampere DC-DC Converters.

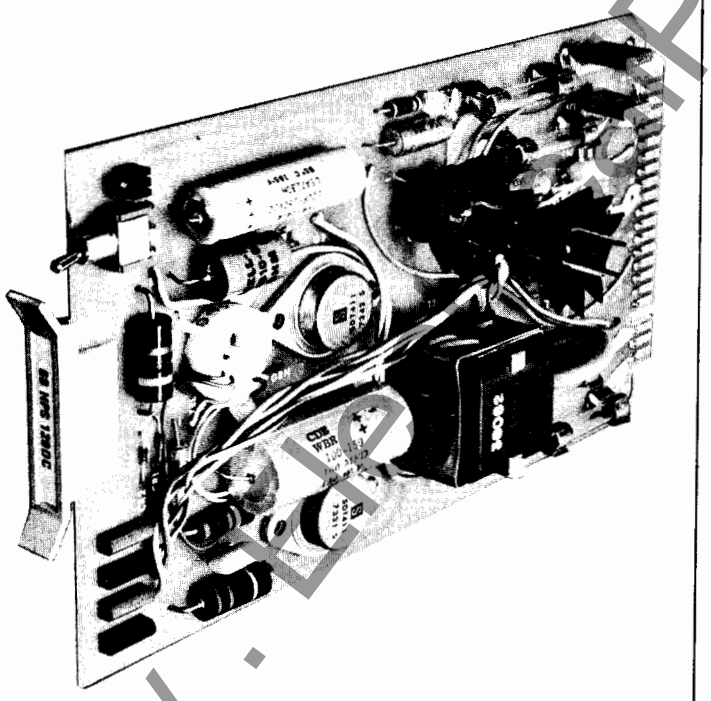


Figure 2. Typical 1-Ampere DC-DC Power Supply. Heat radiators shown on CR3 and CR4 are used to increase heat dissipation. Series regulator for one-ampere units is separate module, shown in Figure 3.

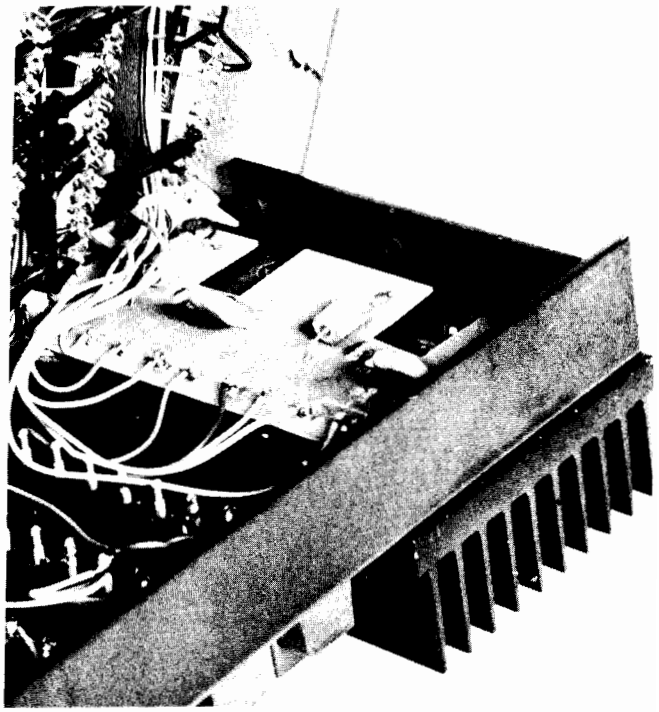


Figure 3. Option HB-41520, used with all one-ampere supplies, is externally mounted at rear of 68 Chassis used to house all Series 6000 equipment.

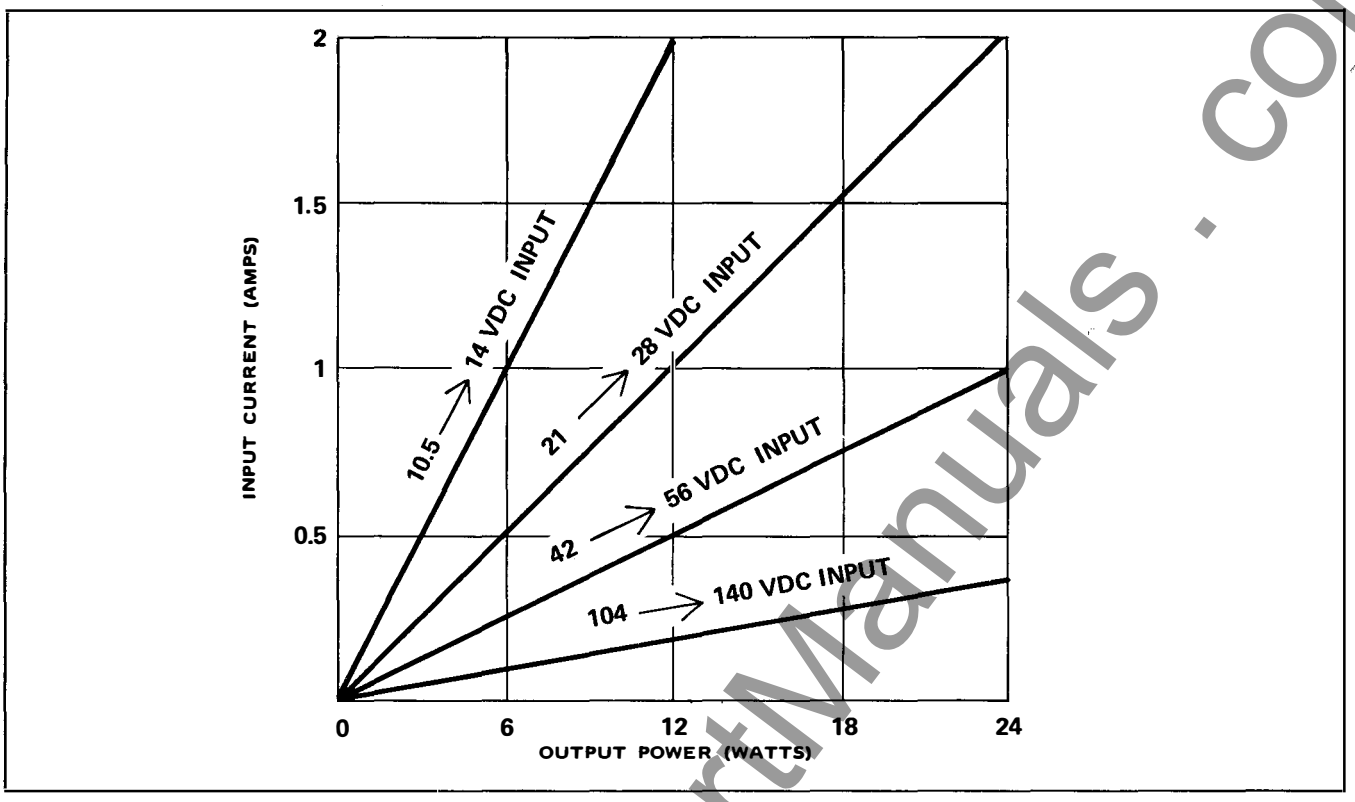


Figure 4. Typical Input Current vs. Output Power.

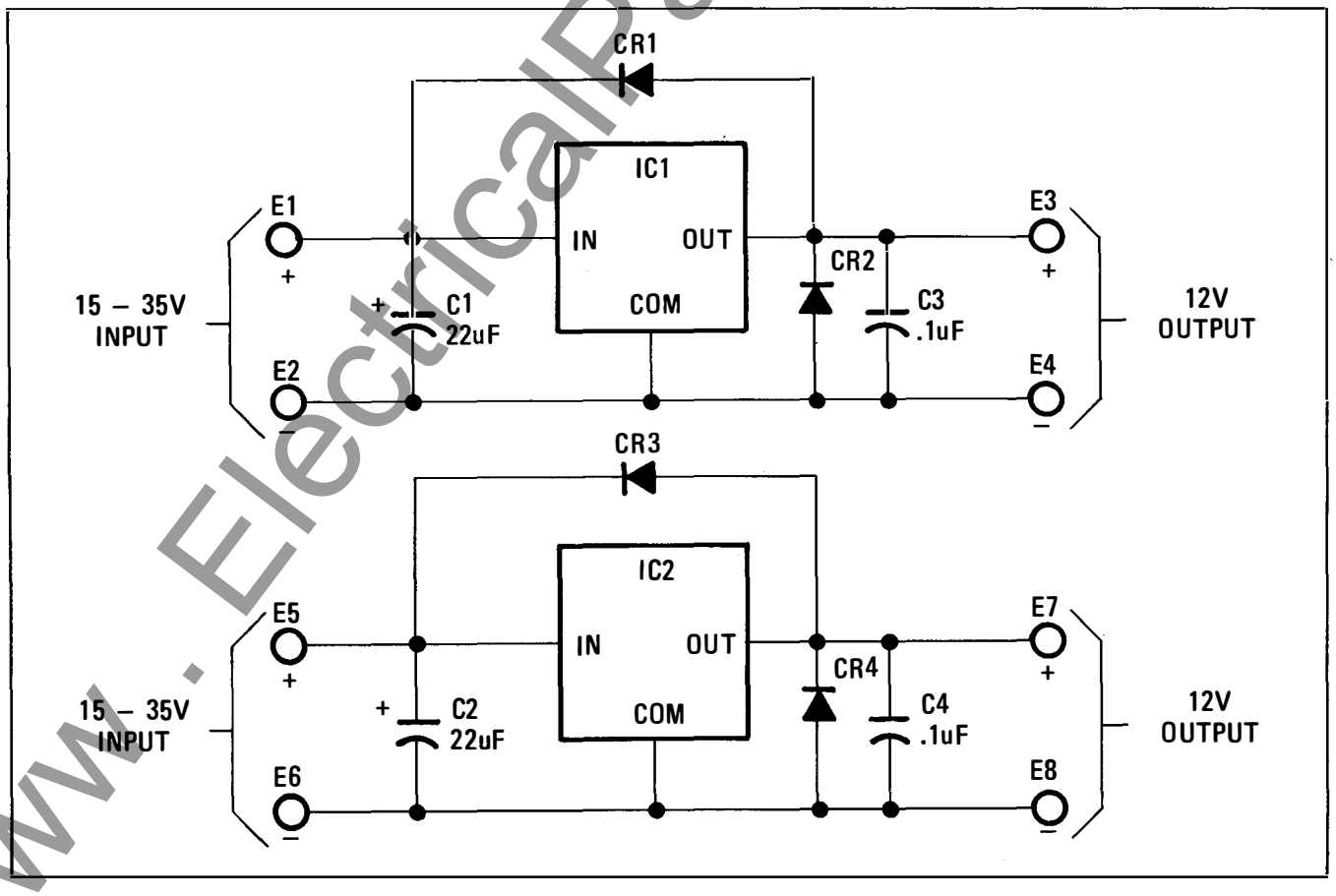


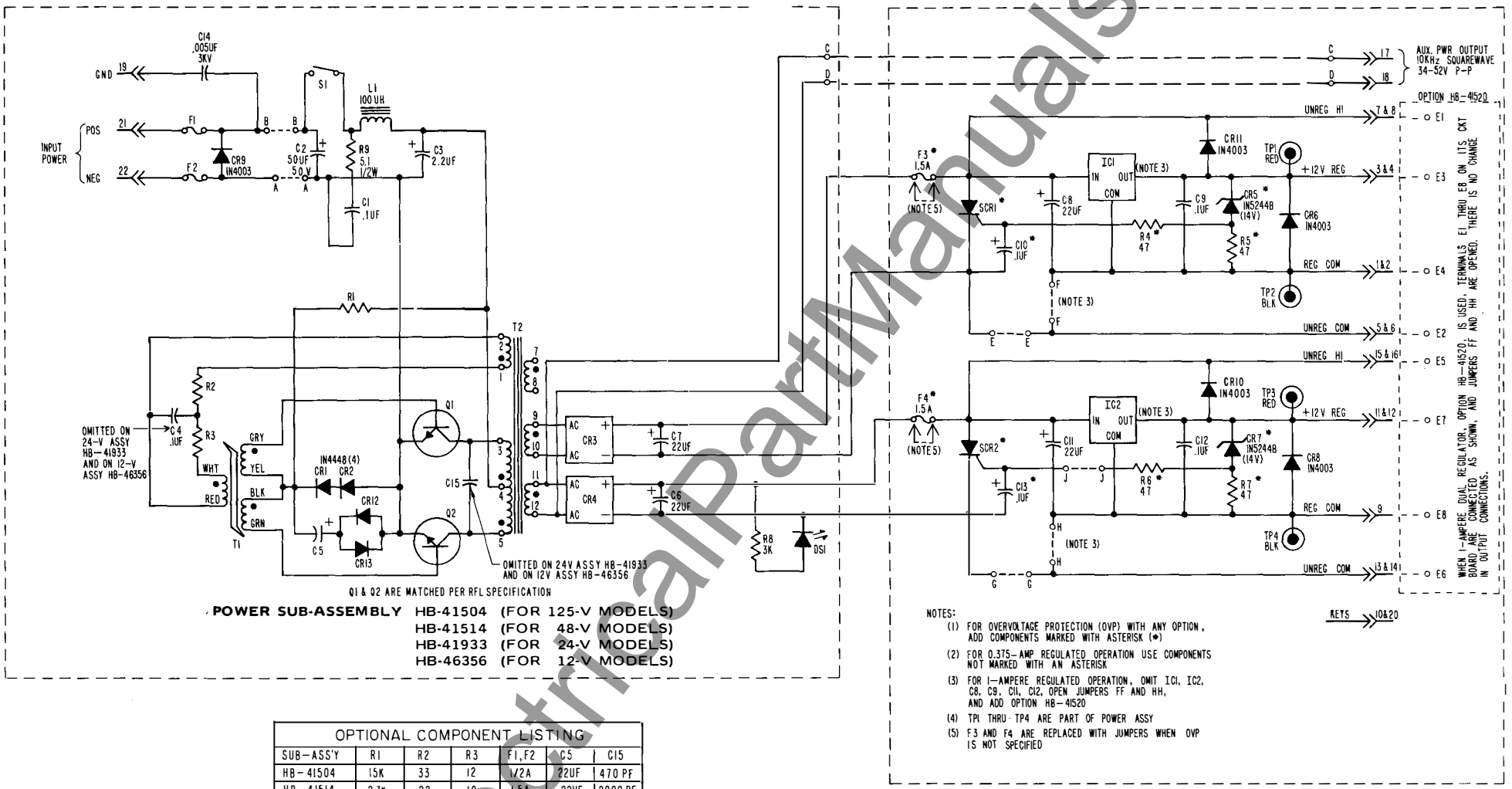
Figure 5. Schematic of Option HB-41520 external regulator and heat dissipator used on all one-ampere models.

Table of Replaceable Parts

DIAGRAM SYMBOL	MODEL	NAME OF PART AND DESCRIPTION	PART NO.
		MISCELLANEOUS COMPONENTS	
S1	All	Switch, toggle SPDT: Right angle mtg. C & K Components 7101-A	HA-39562
TP1 & 3	All	Test jack, red: Cinch 119437-B	HA-38116-2
TP2 & 4	All	Test jack, black: Cinch 119437-C	HA-38116-3
		RESISTORS	
R1	All 129 V	Resistor, fixed comp.: 15 K, 5%, 2 W, Allen Bradley HB	H-1009-251
	All 48V and All 24V & 12V	Same as above, 2.7 K	H-1009-1062
R2	All 129 V	Resistor, fixed.: 33 ohm, 5%, 2 W, Allen Bradley HB	H-1009-1064
	All 48 V and All 24V and 12V	Same as above, 22 ohm	H-1009-1063
R3	All 129 V	Resistor, fixed comp.: 12 ohm, 5%, 1W, Allen Bradley GB	H1009-1065
	All 48V and All 24V and 12V	Same as above, 10-ohm	H-1009-4
R4, 5, 6, & 7	All with O-V Protection	Resistor, fixed comp.: 47 ohm, 5%, ¼W, Allen Bradley CB	H-1009-832
R8	All	Resistor, fixed comp.: 3K, 5%, 1 W, Allen Bradley GB	H-1009-466
R9	All	Resistor, fixed comp.: 5.1 ohm, 5%, ½W, Allen BradleyGB	H-1009-712
		SEMICONDUCTORS	
CR1 & 2	All	Diode silicon, Type 1N4448	HA-29074
CR3 & 4	All	Rectifier bridge assy., Varo VS-148X	HA-39509
CR5 & 7	All with O-V Protection	Diode, zener: 14 V, 5%, 500 mW, Type 1N5244B	HA-41075
CR6, 8, 10, 11	All 0.375-A units	Diode, rectifier: 1 A, Type 1N4003, Solitron S4003TA20	HA-30769
DS1	All	Light-emitting diode, Dialight Cp. 550-0102	HA-39568
IC1 & 2	All	Three-terminal voltage reg., Fairchild UGH 7812393 National LM340-12T	H-0620-69
Q1 & 2	All 129V	Transistors, matched pair	HA-46756
	All 24V & 12V	Transistors, matched pair	HA-46757
SCR1 & 2	All with O-V Protection	Silicon controlled rectifier, Motorola 2N4441 or GE C122F	HA-41072
	All	Schematic	HD-41502
		PARTS LIST FOR 1-AMP EXTERNAL REGULATOR, P/N HB-41520	
C1 & 2	All 1-Amp.	Same as C8 in basic unit	
C3 & 4	All 1-Amp.	Same as C9 in basic unit	
CR1, 2, 3, & 4	All 1-Amp.	Diode, rectifier, 1 A, Type 1N4003	HA-30769
IC1 & 2	All 1-Amp.	Same as in basic unit	

Table of Replaceable Parts

DIAGRAM SYMBOL	MODEL	NAME OF PART AND DESCRIPTION	PART NO.
		MISCELLANEOUS COMPONENTS	
S1	All	Switch, toggle SPDT: Right angle mtg. C & K Components 7101-A	HA-39562
TP1 & 3	All	Test jack, red: Cinch 119437-B	HA-38116-2
TP2 & 4	All	Test jack, black: Cinch 119437-C	HA-38116-3
		RESISTORS	
R1	All 129 V	Resistor, fixed comp.: 15 K, 5%, 2 W, Allen Bradley HB	H-1009-251
	All 48V and All 24V & 12V	Same as above, 2.7 K	H-1009-1062
R2	All 129 V	Resistor, fixed.: 33 ohm, 5%, 2 W, Allen Bradley HB	H-1009-1064
	All 48 V and All 24V and 12V	Same as above, 22 ohm	H-1009-1063
R3	All 129 V	Resistor, fixed comp.: 12 ohm, 5%, 1W, Allen Bradley GB	H1009-1065
	All 48V and All 24V and 12V	Same as above, 10-ohm	H-1009-4
R4, 5, 6, & 7	All with O-V Protection	Resistor, fixed comp.: 47 ohm, 5%, ¼W, Allen Bradley CB	H-1009-832
R8	All	Resistor, fixed comp.: 3K, 5%, 1 W, Allen Bradley GB	H-1009-466
R9	All	Resistor, fixed comp.: 5.1 ohm, 5%, ½W, Allen BradleyGB	H-1009-712
		SEMICONDUCTORS	
CR1, 2, 12, 13	All	Diode silicon, Type 1N914B	HA-26482
CR3 & 4	All	Rectifier bridge assy., Varo VS-148X	HA-39509
CR5 & 7	All with O-V Protection	Diode, zener: 14 V, 5%, 500 mW, Type 1N5244B	HA-41075
CR6, 8, 10, 11	All 0.375-A units	Diode, rectifier: 1 A, Type 1N4003, Solitron S4Q03TA20	HA-30769
DS1	All	Light-emitting diode, Dialight Cp. 550-0102	HA-39568
IC1 & 2	All	Three-terminal voltage reg., Fairchild UGH 7812393 National LM340-12T	H-0620-69
Q1 & 2	All 129V	Transistors, matched pair	HA-46756
	All 24V & 12 V	Transistors, matched pair	HA-46757
SCR1 & 2	All with O-V Protection	Silicon controlled rectifier, Motorola 2N4441 or GE C122F	HA-41072
	All	Schematic	HD-41502
		PARTS LIST FOR 1-AMP EXTERNAL REGULATOR, P/N HB-41520	
C1 & 2	All 1-Amp.	Same as C8 in basic unit	
C3 & 4	All 1-Amp.	Same as C9 in basic unit	
CR1, 2, 3, & 4	All 1-Amp.	Diode, rectifier, 1 A, Type 1N4003	HA-30769
IC1 & 2	All 1-Amp.	Same as in basic unit	



NOTES:

(1) FOR OVERVOLTAGE PROTECTION (OVP) WITH ANY OPTION, ADD COMPONENTS MARKED WITH ASTERISK (*)

(2) FOR 0.375-AMP REGULATED OPERATION USE COMPONENTS NOT MARKED WITH AN ASTERISK

(3) FOR 1-AMPERE REGULATED OPERATION, OMIT IC1, IC2, C8, C9, C11, C12, OPEN JUMPERS FF AND HH, AND ADD OPTION HB-41520

(4) TP1 THRU TP4 ARE PART OF POWER ASSY

(5) F3 AND F4 ARE REPLACED WITH JUMPERS WHEN OVP IS NOT SPECIFIED

OPTIONAL COMPONENT LISTING

SUB-ASS'Y	R1	R2	R3	F1, F2	C5	C15
HB-41504	15K	33	12	1/2A	22UF	470 PF
HB-41514	2.7K	22	10	1.5A	22UF	2000 PF
HB-41933	2.7K	22	10	3A	22UF	
HB-46356	820	22	10	3A	22UF	

Figure 6. Composite schematic of wiring for all models of DC-DC converters for Series 6850.

MODEL 67 BUFFER
(A part of Series 6745 System)

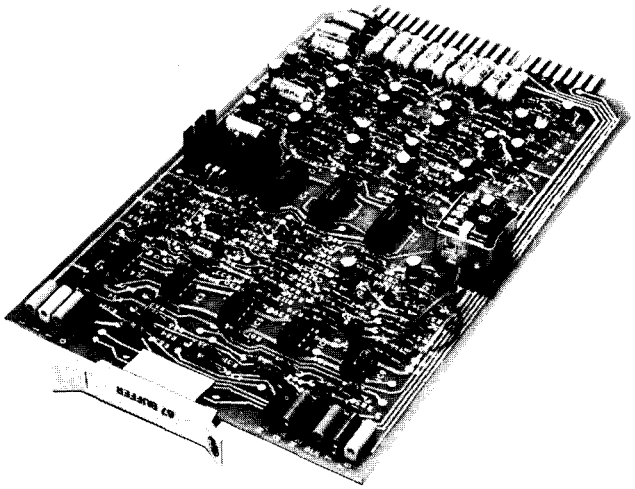


Figure 1. Model 67 Buffer.

SPECIFICATIONS

Inputs: Six logic-level inputs and four analog-signal inputs, taken from the Series 6745 System.

Outputs: All buffers deliver a logic one when the condition is present, except for the Block-signal output, which is a logic one when the condition of the System is normal.

Each buffer will deliver either (a) 12 Vdc at up to 10 mA, when operated from a +12-V power supply, or (b) 18 Vdc at up to 10 mA, when operated from the isolated 18-V power supply provided on the circuit card.

Ambient-Temperature Range: −30 to +60°C.

Power Requirements: (a) −12 Vdc, 25 mA under all conditions, plus one of the following: Either +12 Vdc, 100 mA when the 18-V isolated power supply is not used, or +12 Vdc, 40 mA, plus 42 V, 10 kHz, 35 mA ac when the 18-V isolated power supply is used. All voltages may be taken from the 6000 Series DC-DC Converter supplied with the System.

Dimensions: The circuit card is 4.713 inches high, by 8 inches deep, by 1 inch wide. It occupies two one-half-inch module spaces in the Model 68 Chassis.

DESCRIPTION

The Model 67 Buffer is a unit of the DIT-1 System. This card provides buffered outputs for diagnosis and monitoring purposes. It is a single, plug-in circuit card with eleven identical output-buffer amplifiers, designed to accept the various output signals of the DIT-1 equipment, and to provide buffered, solid-state outputs.

The eleven buffered outputs are: Guard, Subchannel A; Guard, Subchannel B; Trip, Subchannel A; Trip, Subchannel B; Noise, Subchannel A; Noise, Subchannel B; Out-of-limits, Subchannel A; Out-of-limits, Subchannel B; Block; Trip; and Trip, Subchannels A and B.

All buffers deliver a logic one when the condition is present, except for the Block output which delivers a logic one when the block is absent. Test points are provided for monitoring the output of each buffer amplifier. Amplifiers are powered, as a group, from either the 12-V supply or from an 18-Vdc collector supply isolated from the main power supply of the Series 6745.

Supplementing the buffer amplifiers, the Model 67 Buffer also carries window detectors for guard and for trip signals, window detectors for noise in Channels A and B, an undervoltage detector which prevents generation of a trip signal in the event of failure of the power supply, and a stable reference-voltage generator used to supply reference voltages to the several detectors on the card. Figure 2 is a block diagram outlining the plan of the design.

THEORY OF OPERATION

Typical Buffer: All buffers are essentially identical. For typical detail, consider the logic-block buffer at the right-hand edge of Figure 3 the input of which will be a logic one at Terminal 11. The resulting low at the emitter of Q23 brings that transistor into conduction and produces a logic low at the base of Q24. When Q24 is thus caused to conduct, it pulls Terminal R high to produce the desired logic one at that point. A logic one at the output is 12 or 18 Vdc, depending upon the power supply used, and each buffer can supply a load up to 10 mA dc.

Detectors: From the FS/AM Detector card, the AM-signal output of each subchannel is fed to four sets of window detectors. Referring to Figure 3, it will be seen that IC5A and IC5B form the window detector for noise from Subchannel A, and IC2A and IC2B detect the signal for Subchannel B. Any noise whose level exceeds the limits set by these detectors will be detected and passed to the appropriate buffer amplifier.

The FS-signal output of the FS/AM Detector card is fed to two window detectors to sense the trip and guard signals. Signals from Subchannel A pass through the detector formed from IC7B and IC9A. For the same function, Subchannel B uses IC7A and IC3B.

Reference-Voltage Generator: Reference voltages used for the window detectors are based upon AGC-reference levels which have been determined by the choice of network RZ16 on the Logic card. RZ16 is chosen on the basis of trip-boost level desired for the system, including the case of non-boost operation. Based upon the AGC level received at terminal 16, IC9B supplies positive reference voltages. The level established at the output of IC9B is inverted by IC3A to create a negative reference. The low output impedance of the two opamps minimizes coupling among the detectors.

Isolated Power Supply: The isolated power supply is powered from a 10-kHz power source provided by the DC-to-DC Converter. Isolation is effected by Transformer T1, which is followed by a separate rectifier, filter, and series-type regulator. Note that the Model 67 Buffer also requires positive and negative 12-V power from the main power supply of the System.

Undervoltage Detector: Q5 is the undervoltage detector used to sense failure of the 12-V power supply. So long as 12-V power is present, CR10 holds the base of Q5 at about 9.1 V so that Q5 is conducting with its collector at about 8.4 V. This is applied to the bases of Q3 and Q4 to bias them so that they will conduct whenever a logic high is received. If power fails, the collector of Q5 moves to ground potential and cuts off Q3 and Q4 to prevent the possibility of creating a false trip because of faulty voltage levels.

Redundant Logic: When a second logic card is used in the basic Series 6745 to create a redundant-logic system, the trip-output signal from each logic card is fed separately to the Model 67 Buffer. Here, using separate buffers, they are combined by the series connection of Q1 and Q2 to produce a single buffered output at Terminal M. Placement of Jumper E determines whether the logic-trip buffers respond to single or to a dual logic-trip-input signal.

Summation of Detected-Trip Signals: Diodes CR28 and CR29 form an AND gate for trip signals detected at IC7B and IC7A. When this occurs simultaneously, Terminal L rises to a logic one, driven by the buffer comprised of Q6, Q7, Q8, and IC8B.

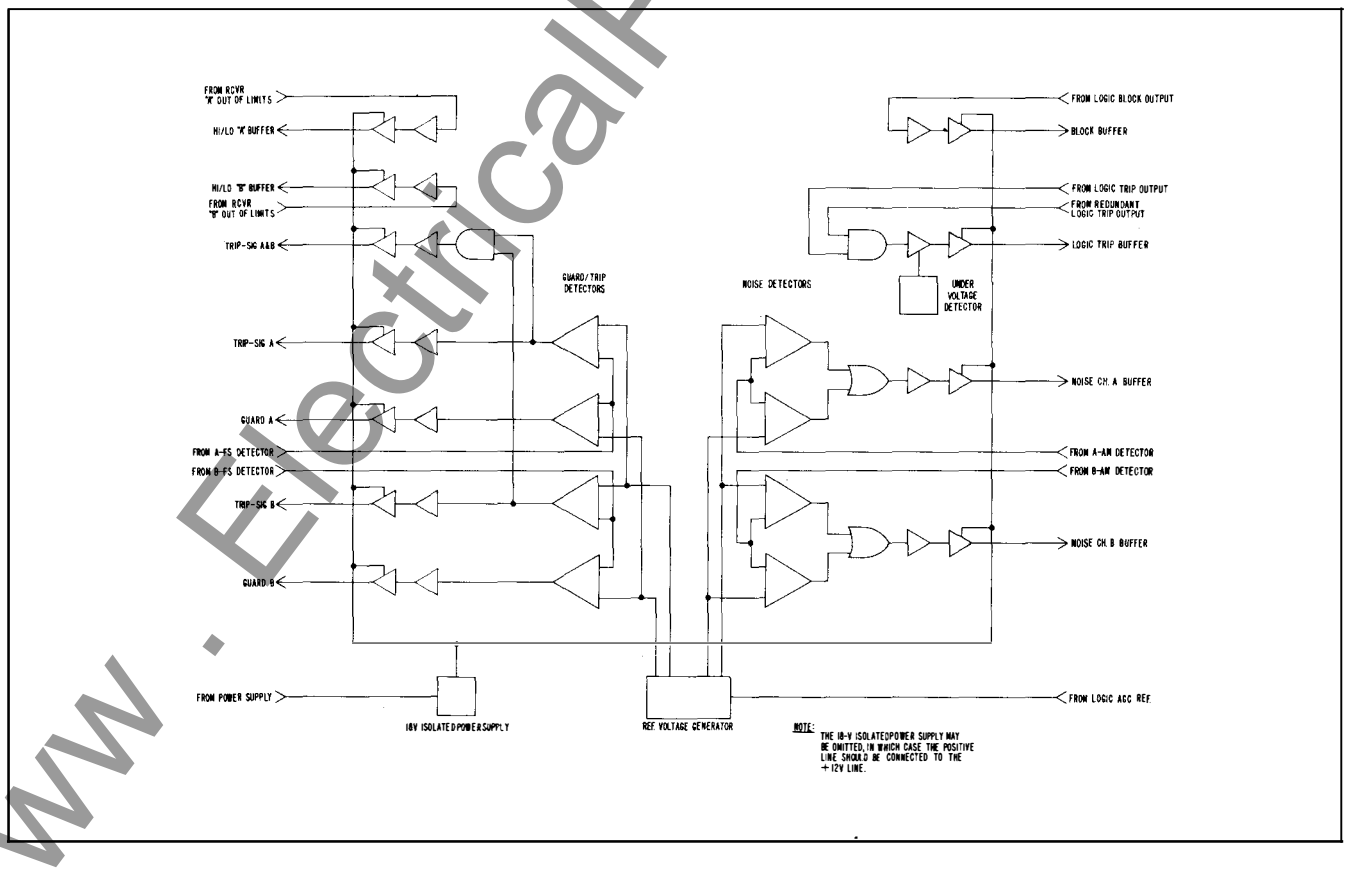


Figure 2. Block Diagram Model 67 Buffer.

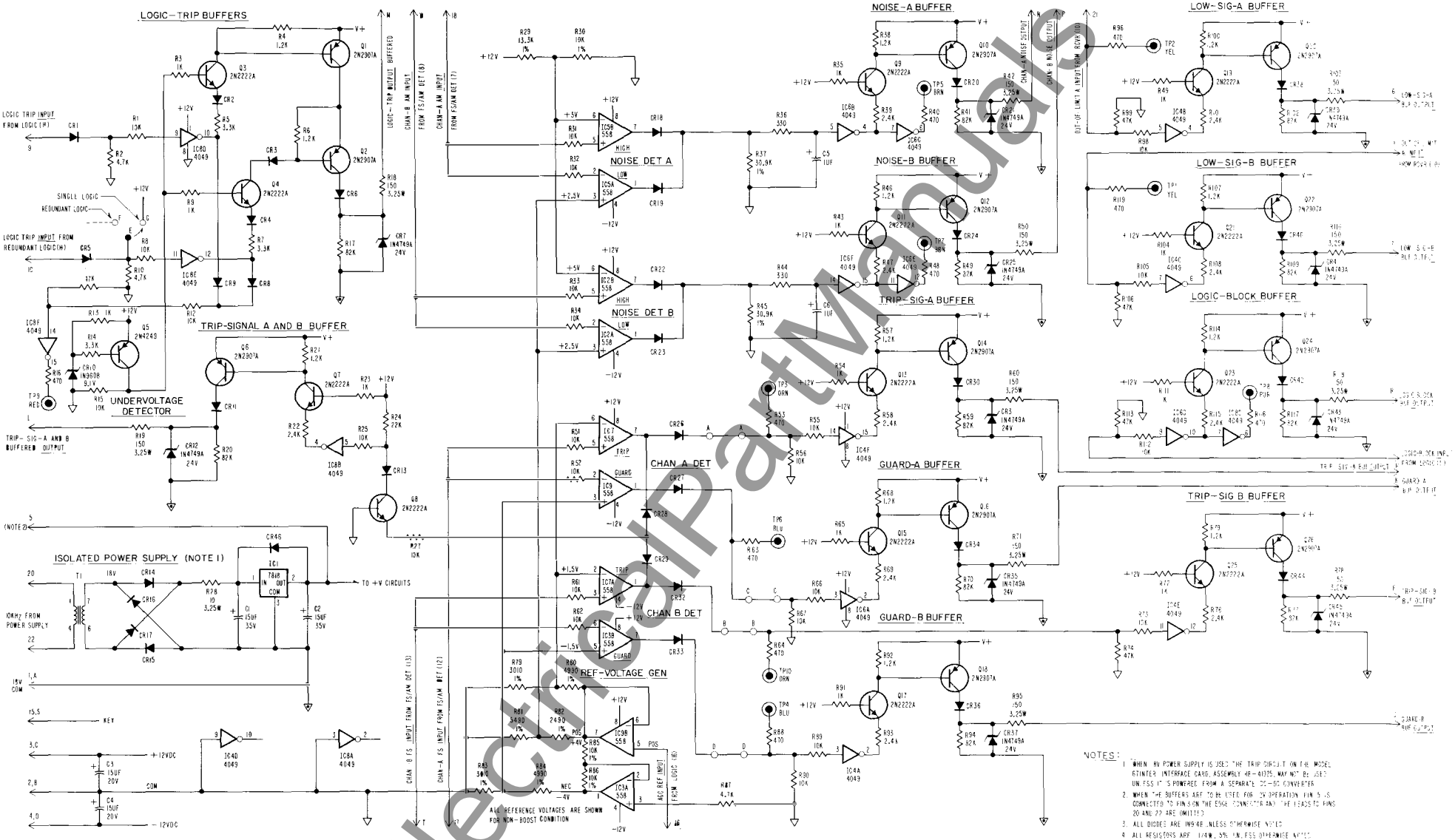


Figure 3. Schematic of Model 67 Buffe.

Table of Replaceable Parts

DIAGRAM SYMBOL	NAME OF PART AND DESCRIPTION	PART NO.
	MODEL 67 BUFFER, HB-41110	
	CAPACITORS	
C1, 2	Capacitor, tantalum, 15 μF, 20%, 35 V, Corning CCZ-035-156-20, or eq.	H-1007-654
C3, 4	Capacitor, tantalum, 15 μF, 20%, 20 V, Kemet T324D156MO2OAS, or eq.	H-1007-716
C5, 6	Capacitor, tantalum, 1 μF, 20%, 35 V, Kemet T324A473M035AS, or eq.	H-1007-496
	RESISTORS	
R1-18, 20-27, 31-36, 38-41, 43-44, 46-50, 51-59, 61-70, 72-77, 87-94, 96-102, 104-109, 111-117, and 119	Resistor, fixed composition, 5%, ¼ W, value per schematic, Allen Bradley CB, or eq.	H-1009-(XXX)
R29, 30, 37, 45, 79-86	Resistor, metal-film, 1%, 1/8 W, value per schematic, per RFL Spec HA-38301	H-1510(XXX)
R18, 19, 28, 42, 50, 60, 71, 78, 95, 103, 110, 118	Resistor, wirewound, 150 ohms, 5%, 3¼W, Ohmite 4396, or eq.	H-1100-566
R28	Resistor, wirewound, 10 ohms, 5%, 3¼ W, Ohmite 4361, or eq.	H-1100-479
	SEMICONDUCTORS	
CR1-6, 8, 9, 11, 13-20, 22-24, 26-30, 32-34, 36, 38, 40, 42, 44, 46	Diode, Type 1N914B	HA-26482
CR7, 12, 21, 25, 31, 35, 37, 39, 41, 43, 45	Diode, zener, 24 V, Type 1N4749A	HA-34619
CR10	Diode, zener, 9.1 V, Type 1N960B	HA-41014
IC1	IC Regulator, +18 V, Motorola MC7818CP, or eq.	H-0620-79
IC2, 3, 5, 7, 9	Dual Linear, opamp., National LM1458N, or eq.	H-0620-51
IC4, 6, 8	CMOS Hex Inverter, RCA CD4049AE, or eq.	H-0615-7
Q1, 2, 6, 10, 12, 14, 16, 18, 20, 22, 24, 26	Transistor, PNP, Type 2N2907A	HA-37439
Q3, 4, 7-9, 11, 13, 15 17, 19, 21, 23, 25	Transistor, NPN, Type 2N2222A	HA-37445
Q5	Transistor, PNP, Type 2N4249	HA-41919
T1	Transformer, power, RFL mfg.	HA-43838
	Schematic	HE-41112

Model 67AR ( )
TRIP AND GUARD RELAY ASSEMBLY

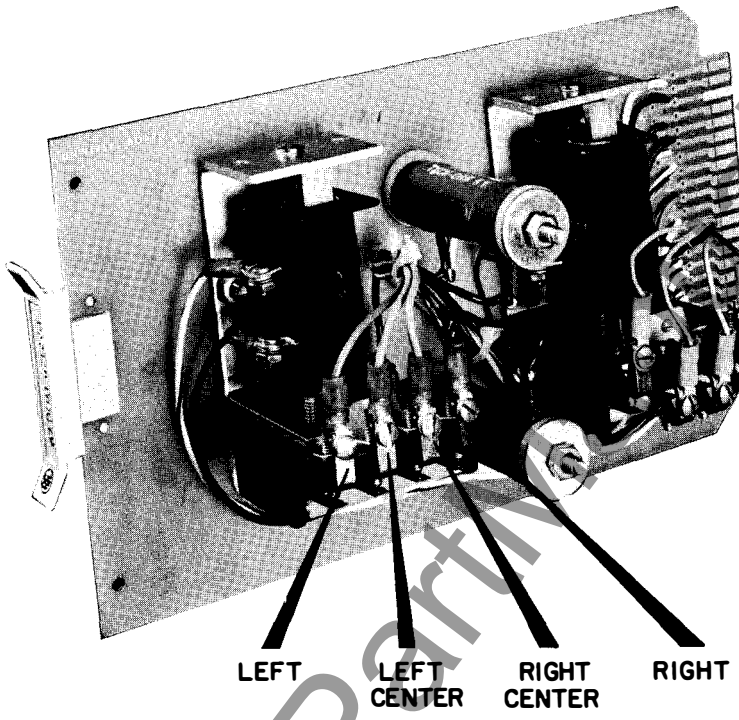


Figure 1. Model 67AR ( ) Trip and Guard Relay Assembly.

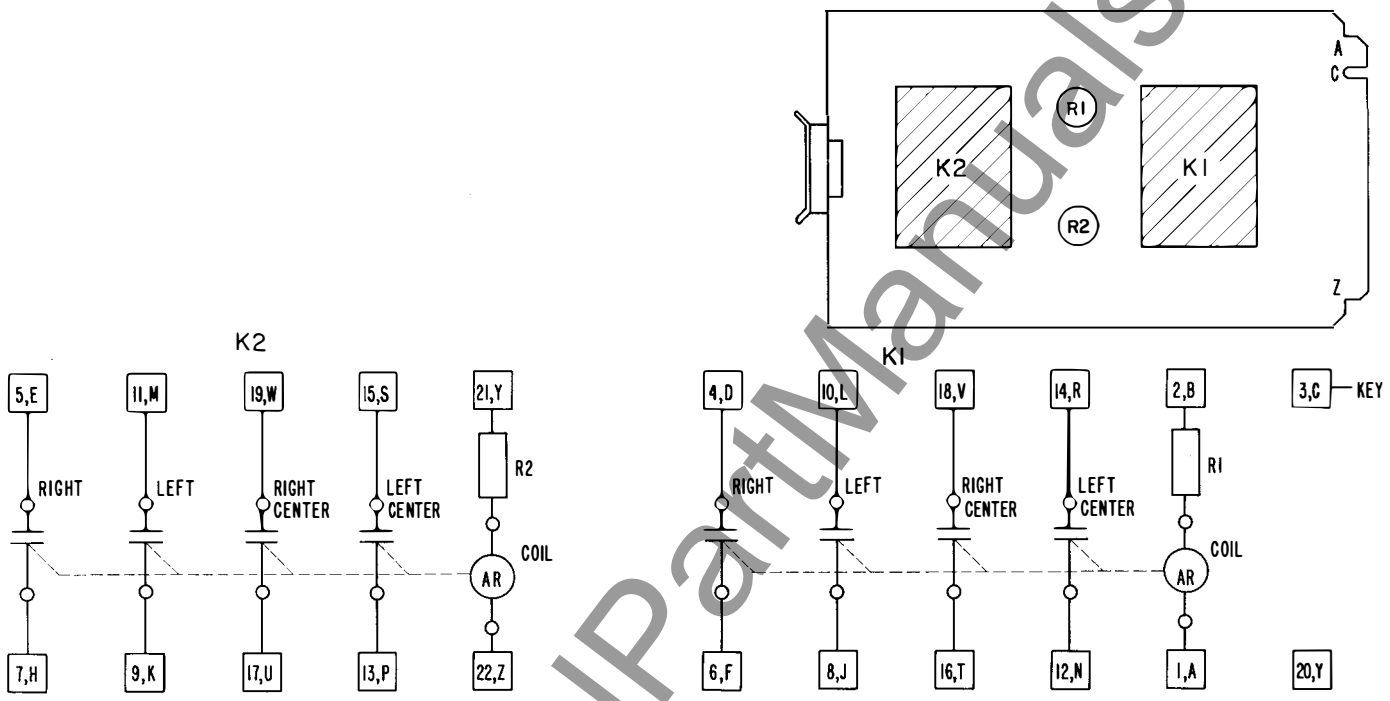
DESCRIPTION

The Model 67AR ( ) is a module that mounts either one or two Westinghouse AR relays for convenient insertion into a DIT-1 or a DIT-3 chassis. Mounting cards carrying either dual or single relays occupy 3.5 inches (seven one-half-inch horizontal chassis spaces) in the chassis. The module is usually mounted on the far-right of the chassis, as viewed from the front.

Detailed model numbers, shown on the front handle of each module, are based on the structure shown on Figure 2. Note that a 00 in the contacts position designates that the relay is not supplied. Cards can be supplied with relays mounted either vertically or horizontally, when the card stands vertical in the chassis, according to whether the final letter is V or H.

NOTE: Relay coil must be in the vertical position when the card is mounted within the chassis.

For more detailed information on the relays used, consult Westinghouse Publication IL-41-759.



HANDLE STRAPPING INFORMATION

MODULE NO.	STAMP HANDLE
HB-46666-1	67 AR 125 4000V
HB-46666-2	67 AR 48 4000V
HB-46666-3	67 AR 125 2200V
HB-46666-4	67 AR 48 2200V
HB-46666-5	67 AR 125 2222V
HB-46666-6	67 AR 125 4022V
HB-46666-7	67 AR 125 3100V
HB-46666-8	67AR 125 4022V
HB-46666-10	67AR 125 3122H

CALL OUT BREAK DOWN

V=VERTICAL
H=HORIZONTAL

MODEL	COIL VOLTAGE	K1 RELAY CONTACTS MAKE	K1 RELAY CONTACTS BREAK	K2 RELAY CONTACTS MAKE	K2 RELAY CONTACTS BREAK	CARD MOUNTING POSITION
EXAMPLE 67AR	125	3	1	0	0	V OR H

	K1					K2			
STYLE NO. 408C845G-	RT 4,6	LT 10,8	RC 18,16	LC 14,12	STYLE NO. 408C845G-	RT 5,7	LT 11,9	RC 19,17	LC 15,13
01	NO	NO	NO	NO	——	—	—	—	—
05	NO	NO	NO	NO	——	—	—	—	—
09	NO	NO	NC	NC	——	—	—	—	—
25	NO	NO	NC	NC	——	—	—	—	—
09	NO	NO	NC	NC	09	NO	NO	NC	NC
01	NO	NO	NO	NO	09	NO	NO	NC	NC
23	NO	NO	NO	NC	——	—	—	—	—
23	NO	NO	NO	NC	09	NO	NO	NC	NC
23	NO	NO	NO	NC	09	NO	NO	NC	NC

R1 & R2	DC VOLTAGE
200 OHMS	48V
1.5K	125V
6K	250V

Figure 2. Schematic of circuit and details of model designations, Model 67AR ( ).

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