INSTALLATION • OPERATION • MAINTENANCE

INSTRUCTIONS

TYPE SDG-1, -2, -3, -4, -5 STATIC GROUND DISTANCE RELAYS

APPLICATION

These instructions cover the five basic types listed in Table I. This line of relays provides single-zone ground-distance protection. The relay reaches the preset amount for single-line-to-ground faults and as much as 20% less for double-line-to-ground faults for SDG, SDG-1, SDG-2 relays when set for S = 1. For S = 2 or S = 3 relay will overreach on phase-to-phase-ground faults.

TABLE I

Relay	I_0 Fault Det.	Freq. Verifier	‡ Phase-to-Phase Desensitizer	Output	Application
SDG	X	X	X	Thyristor	Zone 1
SDG-1	X	X	X	Transistor	Zone 1
SDG-2	–	X	X	Transistor	(Note 1)
SDG-3	X	–	–	Transistor	Timed Trip
SDG-4	–	–	–	Transistor	Blocking Start
SDG-5	–	X	–	Transistor	Pilot trip

‡ Where balance point product of $3I_0Z_C < 40$ disconnect this circuit and set Zone 1 reach for 70%.

NOTE 1: Also suitable for timed trip, except disconnect 2ϕ-G circuit. See Page 14.

The potential supply must be wye-grounded. The broken delta potential connection is provided inside the relay.

As shown in Table I the SDG is equipped with a thyristor trip output; use this type where a single zone is needed in conjunction with an otherwise electromechanical system.

The relays with transistor output provide 15 to 19 volts and up to 0.01 ampere d-c. An auxiliary unit such as an ARS tripping relay or an SRU output package is necessary to trip a breaker or operate other electromechanical devices.

The frequency-verifier circuit should be utilized for all high-speed trip applications to avoid undesired trips due to high-frequency transients. This circuit is not needed for timed trips (e.g., zone 2), but the SDG-1 or SDG-2 or SDG-5 may be utilized instead of the SDG-3 in the interest of standarization.

Relays with I_0 current detector are used to prevent tripping due to potential circuit trouble; the SDG-2 and SDG-5 relays require SI- or SI-1 current detector supervision.

The phase-phase desensitizer is used to eliminate a possible 15% overreach on two-line-to-ground faults. This circuit is needed for zone 1 applications where the relay reaches 85% towards the far bus. This feature is not needed for pilot trip (SDG-5 relay).

In general, no compensation for zero sequence mutual induction is needed. In case of two parallel two-terminal lines and an 85% self-impedance relay, setting zone 1 will reach at least 70% to the far end; accordingly, there is not much gain in mutual compensation of zone 1. However, zone 2 backup relay may be mutually compensated since its reach is affected more than zone 1. See Appendix 1 for details.

FUNDAMENTALS OF DISTANCE MEASUREMENT ON GROUND FAULTS

The SDG distance relay operates on both single and double line-to-ground faults. In either case, neglecting fault resistance, the faulted phase-to-ground voltages at the relay consists of the line drop:

$$V_{LG} = \text{Faulted phase-to-ground relay voltage}$$
$$= K_1 I_1 n Z_{1L} + K_2 I_2 n Z_{1L} + K_0 I_0 n Z_{0L} + I_{OE} n Z_{OM} \quad (1)$$

Where K_1, K_2, K_0 are current distribution factors for the pos., neg., and zero sequence networks, respectively.

I_1, I_2, I_0 are the pos., neg., and zero sequence currents in the fault.

nZ_{1L}, nZ_{0L} are the pos. and zero sequence line impedances to the fault.

I_{0E} is the adjacent line zero sequence current.

Z_{0M} zero sequence mutual impedance.

See Fig. 16 for further definition of terms. For an A to ground fault eq. (1) would be written in terms of the phase A quantities (ignoring mutual effect).

$$V_{AG} = K_1 I_{A1} nZ_{1L} + K_2 I_{A2} nZ_{1L} + K_0 I_0 nZ_{0L} \quad (2)$$

Eq. (2) also applies for an AB to ground fault or any other fault. Additional expressions apply for the phase B and C quantities. Ab to ground fault.

A distance ground relay made to respond to single phase-to-ground faults will also respond in the same way to double line-to-ground faults. This is true except for the effect of ground resistance, R_G. The different nature of these effects can be sensed from Fig. 17. In Fig. 17 the ground current $3I_0$ flowing through R_G is essentially in phase with the total faulted phase current. This is so, since $I_{A1} = I_{A2} = I_0$. This is not true for a 2L-G fault. The current $3I_0$ is out of phase with $K_1 I_{A1}$ and $K_2 I_{A2}$ (also out of phase with $K_1 I_{B1}$ and $K_2 I_{B2}$). As a result the drop across R_G produces an apparent reactance term to the distance relay, causing it to underreach on one phase and overreach on the other faulted phase. The SDG, SDG-1 and SDG-2 relays contain a desensitizer circuit to prevent overreach on 2L-G faults, by reducing the reach of the relay.

The restraint voltages V_{XN}, V_{YN}, V_{ZN} are obtained by the use of compensators with an impedance Z_C, set to match the desired positive sequence line impedance reach. Only positive and negative sequence voltages appear in eq. (3) to (5).

$$V_{XN} = (V_{A1} + V_{A2}) - Z_C(K_A I_{A1} + K_2 I_{A2}) \quad (3)$$

$$V_{YN} = (V_{B1} + V_{B2}) - Z_C(K_1 I_{B1} + K_2 I_{B2}) \quad (4)$$

$$V_{ZN} = (V_{C1} + V_{C2}) - Z_C(K_L I_{C1} + K_2 I_{C2}) \quad (5)$$

The zero sequence voltage is filtered out by not grounding the neutral of the set of Y-connected auxiliary transformers (T_{A2}, T_{B2} and T_{C2}) which are used to feed the restraint portion of the magnitude comparison circuit. These same connections render the zero sequence current flowing in the phase compensators ineffective. So the restraint voltages duplicate the delta voltage conditions at the fault when the fault is Z_C ohms from the relay (i.e., at the balance point). Zero sequence quantities are not required to duplicate the system voltage triangle at the balance point since zero sequence voltage cancels out of the line to line voltages.

The operating voltage is:

$$V_{WO} = V_0 - \frac{Z_{0L}}{Z_{1L}} \times Z \left(K_0 I_0 + I_{0E} \frac{Z_{0M}}{Z_{0L}}\right) \quad (6)$$

Here V_0 is the relay zero sequence voltage: it is compensated by using a compensator impedance (Z_{0L}/Z_{1L}) Z_C representing the zero sequence line impedance to the desired balance point. For mutual coupled lines this compensator can be fed with not only the protected line current but also with a portion of the mutual current I_{0E} (See Fig. 16). The operating voltage V_{WO} duplicates the system zero sequence voltage for fault at the balance point.

Since the faulted phase-to-ground voltage is zero at the fault (neglecting fault resistance), the operating and faulted phase restraint voltage will be equal for a balance point fault. This can be seen by manipulating the fault voltage expression, remembering that the relay compensated voltages are a replica of the fault-point voltages:

V_{LGF} = Faulted phase to ground voltage at the fault

$$= V_{1F} + V_{2F} + V_{0F} = 0 \quad (7)$$

$$V_{1F} + V_{2F} = -V_{0F} \quad (8)$$

$$|V_{1F} + V_{2F}| = |V_{0F}| \quad (9)$$

Eq. (9) states that the magnitude of the sum of the pos. and neg. sequence voltage equals the magnitude of the zero sequence voltage at the fault. This holds regardless of how many phases are grounded. Eq. (9) is the keystone of the SDG system.

This balance point condition is shown in Fig. 18 for an A-G fault. The bus voltages $(V_{A1} + V_{A2})$ and V_0 are shown along with the compensator voltages, which modify the bus voltages to produce restraint voltage V_{XN} and operating voltage V_{WO}.

For this condition V_{YN} and V_{ZN} are also produced but these will be larger in magnitude since

these are derived from the sound phases. Since these voltages exceed V_{XN}, they are irrelevant.

In Fig. 13 for a fault beyond the balance point. V_{XN} exceeds V_{WO}; the reverse is true for the fault within the balance point. Note that for all these faults in the trip direction that the phase compensation acts to reduce the bus positive and negative sequence voltages; whereas, the zero sequence compensation is added to V_0. The reverse is true for a fault behind the relay. For this reason the SDG is inherently directional as long as relay is set for no more than 1.5 times the impedance of the protected line.

One other aspect of Fig. 18 bears amplification. Note for the fault within the balance point that the phase compensation is almost enough to reverse V_{XN} polarity. It is possible for such a reversal to occur, and it is possible if very little zero sequence flows for the phase compensation to overtake the operating voltage and restrain the relay. Thus, the relay may fail to see a close-in fault if the zero sequence current is quite small. Any time this extreme condition occurs the phase distance relay will operate. The phase-distance relay will clear the fault when:

$$Z_1 > \frac{V_0 / I_0}{K_1 + K_2 + pK_0}$$

where Z_1 is positive-sequence relay reach

V_0 = zero sequence bus voltage for close-in fault

I_0 = total zero-sequence fault current for close-in fault

K_1, K_2, K_0 pos.-, neg.- & zero-sequence current-distribution factors for close-in fault.

p = ratio of zero-sequence to positive-sequence line impedance

CONSTRUCTION AND OPERATION

The type SDG relay consists of: four air gap transformers, three auto-transformers for reach adjustment, four phase-splitter transformers, one isolating transformer which couples the zero sequence network a-c output to the static frequency verifier circuit, one zero sequence current-to-voltage transformer, four phase-splitter and rectifier networks, a double line-to-ground fault desensitizer, one voltage regulating zener diode, a thyristor for the tripping function (if used), and printed circuit assemblies.

The large printed circuit assembly contains a magnitude comparator, frequency check circuit, the thyristor tripping unit, and the zero sequence current detector.

Compensators (T_A, T_B, T_C, T_0)

The compensators, which are designated T_A, T_B, T_C, and T_0 are two-winding air gap transformers. Each current winding has seven taps which terminate at the tap block. A voltage is induced in the secondary which is proportional to the primary tap and current magnitude. This proportionality is established by the cross sectional area of the laminated steel core, the length of an air gap which is located in the center of the coil, and the tightness of the laminations. All of these factors which influence the secondary voltage have been precisely set at the factory. The clamps which hold the lamination should not be disturbed by either tightening or loosening the clamp screws.

The secondary winding has a single tap which divides the winding into two sections. One section is connected subtractively in series with the relay terminal voltage. Thus a voltage which is proportional to the phase current is subtracted vectorially from the relay terminal voltage. The second section is connected to an adjustable loading resistor (R_1, R_2, R_3, R_4) and provides a means of adjusting the phase angle between primary current and the induced secondary voltage. The phase angle may be set for any value between 60° and 90° by adjusting this resistor. The factory setting is for a maximum sensitivity angle of 75° current lagging voltage.

A tertiary winding M has four taps which may be connected to directly modify the T setting by any value from −18 to +18 percent in steps of 3 percent. The sign of M is negative when the R lead is above the L lead. M is positive when L is in a tap location which is above the tap location of the R lead. The M setting is determined by the sum of per unit values between the R and L lead. The actual per unit values which appear on the tap plate between taps are 0, .03, .09 and .06.

Auto-Transformer (T_{A1}, T_{B1}, T_{C1})

The auto-transformers T_{A1}, T_{B1}, T_{C1} have three taps on their main winding S which are numbered 1, 2 and 3 on the tap block.

The three secondary windings of the auto-transformers are connected in a "broken delta", thus

serving as a source of zero sequence voltage for the operating circuit. The primary to secondary turn ratio is 3:1, thus producing the proper zero sequence voltage magnitude as required by the theory or relay operation. Using S=2 or S=3 settings reduces zero sequence voltage in the same proportion as the line-to-neutral voltages.

The auto-transformer makes it possible to expand the basic range of T ohms by a multiplier of S.

Phase-Splitter Transformer (T_{A2}, T_{B2}, T_{C2}, T_{O2})

The phase splitter transformer provides isolation between the a-c analog network and the magnitude comparer circuitry located on the printed circuit board, and couples the restraint and operating outputs to the phase splitter network. The tap connection on the secondary winding serves as part of the phase splitting circuit that converts a single-phase input into a three-phase output, thus minimizing the ripple of the rectified output.

Isolating Transformer (I_O)

The isolating transformer I_O serves two purposes: First it isolates the a-c circuit from the d-c circuit, and second, it produces a secondary voltage in the presence of zero sequence current.

Isolating Transformer (T_{FV})

The isolating transformer T_{FV} serves two purposes: First, it isolates the a-c circuit from the d-c circuit and second, it steps up the clipped a-c signal to make the frequency check circuit sensitive to low level input signals.

Double Line-to-Ground Fault Desenesitizer (Fig. 5)

The double line-to-ground fault desensitizer consists of the three networks. Each network consists of a resistor and a minimum voltage network. In this network the largest restraint voltage is blocked by a combination of two restraining voltages. If any two restraining voltages become smaller than the third restraint voltage, transistors Q17 and Q18 are turned on to prevent Q1 transistor from turning on. When operating voltage becomes larger than the highest restraint the relay is allowed to trip.

The desensitizer effect is limited to S = 1 setting only and is not effective on the S = 2 or S = 3 setting. If S = 2 or S = 3 setting is used for zone 1 the setting should be reduced to 75% of the protected line to avoid overreach on double-line-to-ground faults.

Magnitude Comparator Circuit (Fig. 5)

The magnitude comparator circuit consists of a minimum voltage network of the voltage balance type in which operating current is caused to flow through a current detector whenever one of the phase restraint voltages becomes smaller than the operating voltage.

Resistors (R9, R10, R11) provide a return path for the operating current.

The sharp turn-on characteristic is obtained by use of special voltage reference circuit that consists of R33, R34, R35 and TH2 (for temperature compensation). The TP2 potential derived from this reference circuit provides base drive for Q8 transistor that is prevented from turning on as long as Q2 is turned on by TP1 potential. Whenever operating voltage V_{WO} exceeds one of the restraint voltage (V_{XN}, V_{YN} or V_{ZN}) transistor Q1 is turned on lowering the TP1 potential below TP2 potential thus making it possible for Q8 to conduct, thus turning on Q9 and after time delay controlled by R45-C9 time constant (or R76-C9 for SDG-1, 2, 5 or R77-C9 for SDG-3, 4 relays), producing an output.

Zero Sequence Current Detector (Fig. 5)

To prevent operation of the magnitude comparator during a blown potential fuse or similar condition, a zero sequence current detector supervises the operation of the triggering network by preventing capacitor C10 in the triggering circuit from charging, keeping the input to D51 at negative potential through the diode D59.

The detector employs tunnel diode TD1, TD2) as a level detector. The tunnel diode is biased through resistors R64 and R63 to the high voltage state so that enough voltage is maintained across the base-to-emitter junction of Q12 transistor to keep it conducting.

In the presence of the residual current a current derived negative voltage through transformer I_O appears across resistor R60, switching TD1 & TD2 to the low voltage state, thus turning transistor Q12 off and raising its collector close to the positive DC voltage supply level, blocking D59 from discharging the C10 capacitor in SDG relay or allow-

ing Q13 to operate for transistor output relays. (Fig. 6).

Frequency Verification (Fig. 5)

During certain switching conditions, such as energization of a transmission line, residual currents and voltages may exist of higher frequencies than 60 cycles per second. The frequency verifier prevents relay operation when the operating voltage period is less than 4.3 ms. The frequency verification circuit consists of two functional parts: zero-crossing and timing circuit. The zero-crossing circuit consists of transistors Q3, Q4, Q5 and Q6. The zero-crossing circuit is used to allow operation in the presence of higher frequencies of small magnitude superimposed on a fundamental of 60 cps. During the positive or negative half cycles of the operating voltage V_{WO}, Q3 or Q4 transistors are driven into saturation by the output of the T_{FV} transformer. Transistor Q5 conducts until capacitors C6 or C7 respectively are fully charged. While either capacitor is charging through R29, transistor Q5 drives transistor Q6 to discharge timing capacitor C9, thus starting the timing cycle with close to zero charge on the capacitor. The function of the timing capacitor is to delay the operation of the relay for 4 to 4.3 milliseconds. The delay is obtained by delaying the firing time of Z2 zener diode. If a next zero-crossing should occur within the preset delay time, C9 capacitor is discharged again and the timing cycle is repeated. In case of presence of predominant higher frequencies (over 100-140 Hz), zero-crossing pulses will occur within the preset time delay, thus keeping the C9 capacitor from charging up to the zener firing voltage.

TheThe transient blocking is accomplished through the operation of Q7 transistor that is driven by a short pulse formed through R46 and C8 capacitor to clear C9 capacitor of any charge before initiating 4.0 to 4.3 millisecond delay. Any tripping signal coming off Q9 transistor of a duration less than 4.0 to 4.3 will not produce a relay output.

Triggering Circuit for SDG Relay (Fig. 5)

The triggering circuit consists of a four-layer diode D51, resistor R58, diodes D49 and D50 and pulse transformer TR-1. When Q11 transistor is turned on capacitor C10 starts charging to the breakdown voltage of the four layer diode D51.

After breakdown of D51, capacitor C10 discharges through the primary of the TR-1 transformer thus producing a gating impulse that fires the output thyristor QS1. Diode D49 provides a quick discharge of C10 after Q11 is turned off through R57. Diode D50 protects D51 from reverse polarity. The triggering circuit is supervised by the residual overcurrent unit through diode D59. D59 prevents charging of C10 in the absence of residual current.

Output Circuit (Fig. 19)

The output circuit or SDG relay consists of the secondary of the pulse transformer TR-1, diode D52 capacitor C11, resistor R59, and Zener diode Z3. The output of the SDG relay is a thyristor which is gated into conduction by a pulse transformer. The transformer is pulsed as described under "Triggering Circuit Operation." Zener diode Z3, resistor R59 and capacitor C11 form a network protecting the thyristor unit from voltage surges coming through the d-c supply. The function of diode D52 is to short out negative pulses coming from the TR-1 pulse transformer.

Transistor output relays provide 10 milliamps of d.c. current at not less than 15.5 volts through Q14, D52, R75 and Z_3 (Fig. 6). Q14 is operated after Q10, Q11 and Q13 transistor have operated. Q13 operation is supervised by residual current detector through diode D59. This diode shunts base drive to Q13 through Q12 in the current detector to the d.c. negative in the absence of residual current.

Transistors Q15 and Q16 provide output indication during a pushbutton checkout procedure.

Pushbutton Check Circuit (Fig. 20)

For the SDG relay the pushbutton check circuit is used for in-service operational check-out of the output thyristor when relay is used on S = 1 setting. Depressing the pushbutton provides an internal d-c supply to the thyristor switch and operates the overcurrent circuit. This action must be preceded by the opening of the relay trip circuit (red handle) and relay voltage to neutral switch 7. The opening of the voltage switch produces operating voltage conditions in the magnitude comparator that gates the thyristor switch. Operation of the thyristor switch is indicated by the lighting of the bulb built into the pushbutton. A similar circuit is provided in the SDG-1, -2, -3, & -4, -5 relays to check the operation of the output transistor Q14.

CHARACTERISTICS

Distance Characteristics

Fig. 24 shows the relay characteristic in the complex plane is $Z = nZ1L + \frac{3R_G}{F}$ for single-line-to ground faults where factor $F = K_1 + K_2 + pK_0$, where K_1, K_2, K_0 are positive, negative and zero sequence current distribution factors and p = ratio of zero sequence to positive sequence line impedance. Impedance nZ_{1L} is the positive-sequence line impedance from the relay to the fault. The apparent impedance Z must fall within the characteristic shown in Fig. 24 in order to operate. The R-X characteristic is a composite of three circles whose centers are A, B, and C in Fig. 24A. The circle whose center is A is produced from the comparison of faulted phase restraint and operating voltage for a single-line-to-ground fault; whereas the "B" and "C" circles result from sound-phase restraint comparison with operating voltage. Note that part (A) of Fig. 24 applies for the case of a low source impedance vs line impedance; parts (B) and (C) represent increasing amounts of source impedance, or conversely shorter line lengths. The solid-line characteristic is based on current distribution factors for a balance point fault with all breakers closed. As the fault moves toward the relay these distribution factors increase, with the relay approaching the dashed-line characteristic. In the case of Fig. 24C, the dashed-line characteristic is not shown, as it essentially coincides with the solid-line characteristic. Regardless of system conditions, the relay reaches Z_C positive-sequence ohms for a fault at the compensator angle. The fact that the circle diameter expands with increasing source impedance is beneficial, since this provides increased fault resistance accommodation for the shorter line applications. By this we mean that it takes a greater $\frac{3R_G}{K_1+K_2+pK_0}$ component to yield a Z phasor which is outside the operate zone. In Fig. 24C only the faulted phase characteristic is shown, since the other two fall well out of the first quadrant.

One might conclude from Fig. 24 that the relay is not directional since its characteristic includes the origin. This conclusion would be erroneous, since the characteristic equations assume faults in the trip direction per Fig. 14 and do not apply for reversed faults. The relay is directional. In Fig. 24 the second and third quadrants are essentially theoretical since a "negative resistance" is only possible due to out-of-phase infeed. The fourth quadrant is pertinent for series capacitor applications. So we are normally only interested in the first quadrant.

General Characteristics

Impedance settings in ohms reach can be made in steps of 3 per cent. The maximum sensitivity angle, which is set for 75 degrees at the factory, may be set for any value from 60 degrees to 82 degrees. A change in the maximum sensitivity angle will produce a slight change in reach for any given setting of the relay. Referring to Fig. 15, note that the compensator secondary voltage output V, is largest when V leads the primary current, I, by 90°. This 90° relationship is approached, if the compensator loading resistor is open-circuited. The effect of the loading resistor, when connected, is to produce an internal drop in the compensator, which is out-of-phase with the induced voltage, IT_A, IT_B or IT_C. Thus the net voltage, V, is phase-shifted to change the compensator maximum sensitivity angle. As a result of this phase shift the magnitude of V is reduced, as shown in Fig. 15. The tap markings are based upon a 75° compensator angle setting. If the resistors R1, R2, R3, and R4 are adjusted for some other maximum sensitivity angle the nominal reach is different than that indicated by the taps. The reach Z_θ, varies with the maximum sensitivity angle, θ, as follows:

$$Z_\theta = \frac{TS \sin \theta (1+M)}{\sin 75°}$$

TAP PLATE MARKINGS

T_A, T_B, T_C (Positive Sequence)

For 1.0-31 Ohms range – 1.2, 1.5, 2.1, 3.0, 4.5, 6.3, 8.7

For 2.-4.35 Ohms range – .23, .307, .383, .537, .69, .92, 1.23

T_0 (Zero Sequence)

For 1.0-31 Ohms range – 3.60, 4.5, 6.3, 9.0, 13.5, 18.9, 26.1

For .2-4.35 Ohms range– 0.69, 0.92, 1.15, 1.61, 2.07, 2.76, 3.69

$$\frac{(S_A \text{ and } S_C)}{1 \quad 2 \quad 3}$$

± Values between taps $\frac{(M_A, M_B, M_C, M_0)}{.03 \quad .09 \quad .06}$

TIME CURVES AND BURDEN DATA

Operating Time

The speed of operation is shown in Fig. 21. The curves indicate the time in milliseconds required for the relay to provide an output for tripping after the occurrence of a fault at any point on a line within the relay setting.

Current Circuit Rating in Amperes

(All Ranges, All Settings)

Continuous — 10 Amperes
1 Second — 240 Amperes

Burden

The potential burden at 69 volts varies from a maximum of 1.4 volt-amperes at S = 1 setting to a minimum of 0.42 volt-amperes based on 69 volts line-to-neutral per phase. Current burden varies from a maximum of 4.5 volt-amperes at 5 amperes for a maximum T-setting to a minimum of 0.60 volt-amperes for a minimum T-setting. This burden applies to each phase and residual current circuit. D.C. current burden is .07 amperes at all rated voltages.

Trip Circuit Constants

1 Ampere I.C.S. 0.1 Ohms d-c Resistance.

Thyristor (SDG Only)

The thyristor is a three-terminal semiconductor device. In the reverse, or non-conducting direction, the device exhibits the very low leakage characteristics of a silicon rectifier. In the forward, or conducting directions conduction can be initiated by the application of a control pulse to the control terminal or "gate." If a gate signal is not applied, the device will not conduct at below rated forward blocking voltage. With the application of a gate signal, however, the device switches rapidly to a conducting state characterized by a very low voltage drop and a high current-carrying capability. Once a conduction has been initiated, the gate terminal no longer has any effect. In order to turn the thyristor off the anode-cathode current must be reduced to a value less than the holding current.

It should be noted that the SDG differs from mechanically operated contacts. A certain minimum trip current must flow before the thyristor will latch on. However, voltage will be applied to the load for the duration of each pulse. Pulses are applied to the gate circuit at a rate of four every one milliseconds.

Current Rating Per Circuit:

Ambient Temperature	25°C	50°C	75°C
For 50 ms. (3 cycle breaker)	60A	49A	37A
For 83 ms. (5 cycle breaker)	54A	44A	33A
Continuous	6.5A	4.5A	3A

Trip Circuit Requirements:

$\frac{Vdc}{R_{LOAD\ OHMS}}$ = .25 amp or more

$\frac{L_{HENRYS}}{R_{LOAD\ OHMS}}$ = .02 or less

Thyristor:

Max. forward leakage current at rated voltage
125°C 8 MA d-c

Max. reverse leakage current at rated voltage
125°C 8 MA d-c

Max. forward voltage drop at 10 amps
25°C 1.6 volts

CALCULATIONS AND SELECTION OF SETTING

Relay reach is set on the tap plate. Maximum sensitivity angle, θ, is set for 75° (current lagging voltage) in the factory. This adjustment need not be disturbed for line angles of 65° or higher. For line angles below 65°, set θ for a 60° maximum sensitivity angle, by adjusting R_1, R_2, R_3 & R_4 as per calibration procedure for zone 1 application only. Set zone 1 reach to be 85% of the line, if S = 1 is used; 75% if S = 2 or 3 are used. Do not change angle for pilot trip or Zone 2, or Zone 3 applications.

Assume a desired balance point which is 85% of the total length of the line. The general formulas for setting the ohms reach of the relay are:

$$Z_1 = Z_{1L}\frac{0.85R_C}{R_V};\quad Z_0 = Z_{0L}\frac{0.85R_C}{R_V}$$

The terms used in this formula and hereafter are defined as follows:

Z_0 = Zero sequence ohmic reach to be used for relay settings.

Z_1 = Positive sequence ohmic reach to be used for relay settings.

$Z_{1,0}$ = TS (1 + M) = the tap plate setting.

T = Compensator tap value.

S = Auto-transformer tap value.

θ = Maximum sensitivity angle setting of the relay.

$\pm M$ = Compensator tertiary tap value. (This is a per unit value and is determined by the sum of the values between the "L'" and the "R" leads. The sign is positive when "L" is above "R" and acts to raise the Z setting. The sign is negative when "R" is above "L" and acts to lower the "Z" setting).

Z_{1L} = Positive sequence ohms per phase of the total line section, referred to the primary.

Z_{0L} = Zero-sequence ohms per phase of the total line section,referred to the primary.

R_C = Current transformer ratio.

R_V = Potential transformer ratio.

The following procedure should be followed in order to obtain an optimum setting of the relay.

Zone 1 Setting (SDG, SDG-1, SDG-2 Relays)

1. a. Establish the desired values of Z_1 and Z_0 as above (available from transmission line data) and desired maximum sensitivity angle $\theta°$.

   b. Determine the desired tap plate value Z' using the formula a:

   $$Z_1 = Z_{1\theta} \frac{\text{Sin } 75°}{\text{Sin } \theta} \text{ and } Z_0 = Z_0 \frac{\text{Sin } 75°}{\text{Sin } \theta°}$$

   θ = Angle to which relay is recalibrated. Then, for factory calibration θ = 75°, $Z_1 = Z_{1\theta}$ and $Z_0 = Z_{0\theta}$

2. Now refer to Table II or IV giving preferred zone 1 settings for the SDG relays. If the desired reach exceeds the relay range for S = 1, use S = 2 & Table III or V (set for 75% of line).

   a. Locate a table value for relay reach nearest to the desired Z_1-value (it will always be within 1.5% of the desired value.)

   b. From this table read off the "S", "T" and "M" settings. The "M" column includess additional information for the "L" and "R" lead setting for the specified "M" value. If the desired settings cannot be found on this table proceed to Table III or V to find the desired setting in this case. The relay reach must now be reduced from 85 to 75 percent to avoid ovvereach on two phase-to-ground faults on high fault resistance faults.

   c. Recheck relay settings for Z_1 and Z_0 using equation:

   $Z = TS (1 + M)$

   For example, assume the desired reach, $Z_{1\theta}$ is 7 ohms at 60° (Step 1a) and $Z_{0\theta}$ is 21 ohms at 60°.

   Next step is (1b). Making correction of maximum sensitivity angle of the relay to match the characteristic angle of the line (60°) that is different from factory setting of 75°, we find the relay tap setting.

   $Z_1 = 7 \times 1.11 = 7.77$ ohms

   $Z_0 = 21 \times 1.11$ v 23.31 ohms

   This procedure is followed when R_1, R_2, R_3, R_4 settings are changed, otherwise follow alternative procedure below.

   Step 2a. In Table IV we find 7.65 to be the nearest value to 7.77 ohms.

   $100 \times \frac{7.65}{7.77} = 98.8\%$ or 1.2% from the desired value

   For the Z_θ selection find the nearest value to 23.31 ohms using the same S setting as above. 23.0 ohms is the nearest value.

   $100 \times \frac{23.0}{23.31} =$ 98.8% or 1.2% within the desired value.

   Step (2b). From Table IV read off:

   S = 1

   T = 8.7

   M = -.12

   T_0 = 26.1

   M_0 = - .12

   The "R" - lead should be connected over "L" - lead, with "L" lead connected to "O" - tap and "R" - lead to tap "09". (The sum of the values between L & R is 0.12).

TABLE II

.2 - 4.35 OHMS RELAY RANGE

POSITIVE SEQUENCE (Z_1) S = 1								ZERO SEQUENCE (Z_0) S = 1								M		CONNECT		
																		"L" LEAD TO TAP	"R" LEAD TO TAP	
T	.230	.307	.383	.537	.69	.92	1.23	T_0	.69	.921	1.15	1.61	2.07	2.76	3.69	+M	−M			
	.272	.362	.452	.632	.815	1.09	1.45		.815	1.09	1.36	1.90	2.44	3.26	4.40	+.18		.06	0	
	.264	.352	.441	.617	.794	1.06	1.41		.794	1.06	1.32	1.85	2.38	3.18	4.25	+.15		.06	.03	"R" OVER "L"
	.258	.344	.430	.601	.772	1.03	1.38		.772	1.03	1.29	1.80	2.32	3.10	4.15	+.12		.09	0	
	.251	.335	.418	.585	.754	1.00	1.34		.754	1.00	1.25	1.76	2.26	3.00	4.04	+.09		.09	.03	
	.244	.325	.405	.570	.732	.975	1.30		.732	.975	1.22	1.71	2.20	2.92	3.92	+.06		.06	.09	
	.237	.316	.396	.555	.710	.950	1.27		.710	.950	1.18	1.66	2.13	2.84	3.80	+.03		.03	0	
	.230	.307	.383	.537	.69	.920	1.23		.69	.921	1.15	1.61	2.07	2.76	3.69	0	0	0	0	
	.223	.298	.370	.520	.670	.892	1.19		.670	.892	1.12	1.56	2.00	2.68	3.58		−.03	0	.03	
	.216	.288	.360	.505	.650	.865	1.15		.650	.865	1.08	1.52	1.95	2.60	3.46		−.06	.09	.06	
	.209	.280	.348	.488	.627	.840	1.12		.627	.840	1.05	1.47	1.88	2.51	3.36		−.09	.03	.09	"L" OVER "R"
	.202	.270	.336	.472	.607	.810	1.08		.607	.810	1.01	1.42	1.82	2.43	3.25		−.12	0	.09	
	.195	.260	.324	.456	.587	.782	1.05		.587	.782	.980	1.37	1.76	2.35	3.14		−.15	.03	.06	
	.188	.252	.314	.440	.565	.755	1.01		.565	.755	.940	1.32	1.70	2.26	3.02		−.18	0	.06	

TABLE III

.2-4.35 OHM RELAY RANGE

POSITIVE SEQUENCE SETTINGS (Z_1)									ZERO SEQUENCE SETTINGS (Z_0)									M		CONNECT		
S = 2							S = 3		S = 2							S = 3				"L" LEAD TO TAP	"R" LEAD TO TAP	
T	.230	.307	.383	.537	.69	.92 1.23	.92	1.23	T_0	.69	.921	1.15	1.61	2.07	2.76	3.69	2.76	3.69	+M	−M		
	.544	.724	.905	1.26	1.63	2.17 2.90	3.26	4.40		1.63	2.17	2.72	3.80	4.90	6.50	8.70	9.80	12.1	+.18		.06	0	"L" OVER "R"
	.528	.704	.880	1.23	1.59	2.12 2.82	3.18	4.25		1.59	2.12	2.65	3.70	4.76	6.35	8.48	9.55	12.7	+.15		.06	.03	
	.516	.688	.860	1.20	1.55	2.06 2.76	3.10	4.15		1.55	2.06	2.58	3.60	4.65	6.20	8.25	9.30	12.4	+.12		.09	0	
	.502	.670	.835	1.17	1.51	2.00 2.68	3.00	4.04		1.51	2.00	2.50	3.50	4.52	6.00	8.05	9.05	12.1	+.09		.09	.03	
	.488	.650	.810	1.13	1.46	1.95 2.60	2.92	3.92		1.46	1.95	2.44	3.41	4.40	5.85	7.80	8.80	11.8	+.06		.06	.09	
	.474	.632	.790	1.10	1.42	1.90 2.53		3.80		1.42	1.90	2.37	3.32	4.26	5.70	7.60		11.4	+.03		.03	0	
	.460	.614	.766	1.07	1.38	1.84 2.46		3.69		1.38	1.84	2.30	3.22	4.14	5.52	7.38		11.1	0	0	0	0	
	.446	.596	.740	1.04	1.34	1.78 2.40		3.58		1.34	1.78	2.24	3.12	4.02	5.35	7.15		10.7		−.03	0	.03	"R" OVER "L"
	.432	.576	.716	1.01	1.30	1.73 2.32		3.46		1.30	1.73	2.16	3.02	3.90	5.16	6.94		10.4		−.06	.09	.06	
	.418	.560	.695	.975	1.25	1.67 2.24		3.36		1.25	1.67	2.09	2.94	3.78	5.00	6.70		10.1		−.09	.03	.09	
	.404	.540	.674	.940	1.21	1.62 2.17				1.21	1.62	2.02	2.83	3.66	4.85	6.50		9.8		−.12	0	.09	
	.390	.520	.650	.910	1.17	1.56 2.10				1.17	1.56	1.95	2.74	3.55	4.67	6.27		9.4		−.15	.03	.06	
	.376	.504	.625	.880	1.13	1.50 2.08				1.13	1.50	1.79	2.64	3.40	4.50	6.05		9.1		−.18	0	.06	

TABLE IV

1.1-31 OHMS RELAY RANGE

	POSITIVE SEQUENCE (Z_1') S = 1							ZERO SEQUENCE (Z_0) S = 1								M		CONNECT		
																		"L" LEAD TO TAP	"R" LEAD TO TAP	
T	1.2	1.5	2.1	3.0	4.5	6.3	8.7	T_0	3.6	4.5	6.3	9.0	13.5	18.9	26.1	+M	−M			
	1.42	1.77	2.48	3.54	5.3	7.43	10.2		4.25	5.30	7.45	10.6	15.9	22.2	30.8	+.18		.06	.0	"L" OVER "R"
	1.38	1.73	2.42	3.45	5.17	7.25	10.0		4.15	5.17	7.25	10.4	15.5	21.7	30.0	+.15		.06	.03	
	1.34	1.68	2.36	3.36	5.04	7.05	9.75		4.05	5.04	7.05	10.1	15.1	21.2	29.3	+.12		.09	0	
	1.31	1.64	2.29	3.27	4.90	6.89	9.50		3.94	4.90	6.89	9.81	14.7	20.6	28.4	+.09		.09	.03	
	1.27	1.59	2.22	3.18	4.77	6.70	9.25		3.82	4.77	6.70	9.54	14.3	20.0	27.7	+.06		.06	.09	
	1.24	1.55	2.16	3.09	4.64	6.50	8.95		3.71	4.64	6.50	9.27	13.9	19.5	26.9	+.03		.03	0	
	1.20	1.5	2.10	3.00	4.50	6.30	8.70		3.6	4.50	6.30	9.0	13.5	18.9	26.1	0	0	0	0	
	1.16	1.45	2.04	2.91	4.36	6.10	8.45		3.50	4.36	6.10	8.73	13.1	18.3	25.2		−.03	0	.03	"R" OVER "L"
	1.13		1.97	2.82	4.23	5.90	8.15		3.38		5.90	8.46	12.7	17.7	24.5		−.06	.09	.06	
	1.09		1.91	2.73	4.10	5.74	7.90		3.27		5.74	8.19	12.3	17.2	23.7		−.09	.03	.09	
	1.06		1.85	2.64	3.96	5.55	7.65		3.16		5.55	7.92	11.9	16.6	23.0		−.12	0	.09	
	1.02		1.77	2.55	3.82	5.35			3.06		5.35	7.65	11.5	16.0			−.15	.03	.06	
	0.99				3.69				2.95				11.1				−.18	0	.06	

TABLE V

1.1-31 OHMS RELAY RANGE

T	POSITIVE SEQUENCE SETTINGS (Z_1)									ZERO SEQUENCE SETTINGS (Z_0)										M		CONNECT		
	S = 2							S = 3		S = 2								S = 3				"L" LEAD TO TAP	"R" LEAD TO TAP	
	1.2	1.5	2.1	3.0	4.5	6.3	8.7	6.3	8.7	T_0	3.6	4.5	6.3	9.0	13.5	18.9	26.1	18.9	26.1	+M	−M			
	2.84	3.54	4.96	7.08	10.62	14.9	20.5	22.3	30.8		8.50	10.6	14.9	21.2	31.8	44.5	61.5	66.6	92.5	+.18		.06	0	"L" OVER "R"
	2.76	3.46	4.84	6.90	10.35	14.5	20.0	21.6	30.0		8.30	10.34	14.5	20.7	31.0	43.5	60.0	65.1	90.0	+.15		.06	.03	
	2.68	3.36	4.72	6.72	10.08	14.1	19.5	21.2	29.3		8.10	10.08	14.1	20.2	30.2	42.4	58.5	63.6	87.5	+.12		.09	0	
	2.62	3.28	4.58	6.54	9.81	13.8	19.0		28.4		7.88	9.80	13.8	19.6	29.4	41.2	56.8		85.2	+.09		.09	.03	
	2.54	3.18	4.44	6.36	9.54	13.4	18.5		27.7		7.64	9.54	13.4	19.1	28.6	40.0	55.3		83.0	+.06		.06	.09	
	2.48	3.10	4.32	6.18	9.27	13.0	17.9		27.0		7.42	9.28	13.0	18.5	27.8	39.0	53.8		80.5	+.03		.03	0	
	2.4	3.0	4.20	6.0	9.0	12.6	17.4		26.1		7.20	9.0	12.6	18.0	27.0	37.8	52.2		78.3	0	0	0	0	
	2.32	2.90	4.08	5.82	8.73	12.2	16.9		25.2		7.00	8.72	12.2	17.5	26.2	36.6	50.5		75.8		−.03	0	.03	"R" OVER "L"
	2.26		3.95	5.64	8.46	11.8	16.3		24.5		6.76		11.8	16.9	25.4	35.4	49.0		73.5		−.06	.09	.06	
	2.18		3.82	5.46	8.19	11.5	15.8		23.7		6.54		11.5	16.4	24.6	34.4	47.5		71.0		−.09	.03	.09	
	2.12		3.70	5.28	7.92	11.1	15.3		23.0		6.32		11.1	15.8	23.8	33.2	45.8		68.8		−.12	0	.09	
	2.04		3.54	5.10	7.65	10.7			22.7		6.12		10.7	15.3	23.0	32.0					−.15	.03	.06	
	1.98				7.38										22.2						−.18	0	.06	

Step (2c). Recheck Settings.

$Z_1 = TS\ (1 \pm M) = 1 \times 8.7\ (.88) = 7.65$ and

$Z_0 = 1 \times 26.1\ (.88) = 23.0$

$Z_1 = Z_{1\theta}\frac{\text{Sin } 60°}{\text{Sin } 75°}$ 7.65 x 900 = 6.90 ohms at 60°

$Z_0 = Z_{0\frac{\text{Sin } 60°}{\text{Sin } 75°}} = 23.0 \times 900 = 20.7$ ohms at 60°.

Where balance point product of $3I_oZ_1 < 40$ volts (where Z_1 is positive sequence relay setting and $3I_o$ is zero sequence current in the relay for L-G fault) disconnect the phase-to-phase desensitizer and set Zone 1 reach for 70%. See Page 14.

Alternative Calculations and Settings

If it is desired to avoid recalibration of the relay maximum sensitivity setting the following procedure should be followed.

Follow Step 1a as above.

Change Step 1b to compute desired reach according with equation:

$$Z' = \frac{Z}{\text{Cos } (75-\theta)}$$

Note: Do not use equation to predict relay response for angles more than 15° away from θ.

Then $Z_1 = \frac{7}{\text{Cos } (75\text{-}60)} = \frac{7}{.965} = 7.25$

$Z_0 = \frac{21}{\text{Cos } (75\text{-}60)} = \frac{21}{.965} = 21.75$

Step 2 (a) as above from Table IV we find 7.25 value and 21.75 ohm-values as the exact values.

Step 2 (b) from Table IV read off:

S = 1

T = 6.3 T_0 = 18.9

M = +.15 M_0 = +.15

Step 2 (c) Recheck Settings:

$Z_1 = Z_1 \cos (75° - \theta) = 7.25 \times 965 = 7$ ohms

$Z_0 = Z_0 \cos (75° - \theta) = 21.75 \times 965 = 21$ ohms

Zone 2 & 3 Settings or Pilot Trip Applications

For zone 2 and 3 settings use a procedure similar to alternative for zone 1 described above. Tables II to V give the required settings. There is no need to recalibrate relay for zone 2 or 3 application for difference in maximum torque angle.

Note: The S setting must be the same for both the positive and zero-sequence reach.

SETTING THE RELAY

The SDG relays require settings for the four compensators (T_A, T_B, T_C and T_O), the three autotransformer primaries (S_A, S_B, and S_C), and the four compensator tertiaries (M_A, M_B, M_C, and M_0). All of these settings are made with taps on the tap plate, with relay deenergized.

Compensator (T_A, T_B, T_C, T_O and M_A, M_B, M_C, M_O)

Each set of compensator primary T_A, T_B, T_C, T_O, taps terminates in inserts which are grouped on a socket and form approximately three-quarters of a circle around a center insert which is the common connection for all of the taps. Electrical connections between common insert and tap inserts are made with a link that is held in place with two connector screws, one in the common and one in the tap. A compensator tap setting is made by loosening the connector screw in the center. Before removing the screw open switches 12 through 19 to bypass the current around the relay. Remove the connector screw in the tap end of the link, swing the link around until it is in position over the insert for the desired tap setting, replace the connector screw to bind the link to this insert, and retighten the connector screw in the center. Since the link and connector screws carry operating current, be sure that the screws are turned to bind snugly. Compensator secondary tap connections are made through two leads identified as L and R for each compensator. These leads come out of the tap plate each through a small hole, one on each side of the vertical row of "M" tap inserts. The lead connectors are held in place on the proper tap by connector screws.

Values for which an "M" setting can be made are from -.18 to + .18 in steps of .03. The value of a setting is the sum of the numbers that are crossed when going from the R lead position to the L lead position. The sign of the "M" value is determined by which lead is in the higher position on the tap plate. The sign is positive (+) if the L lead is higher and negative (—) if the R lead is higher.

An "M" setting may be made in the following manner. Remove the connector screws so that the L and R leads are free. Refer to Table II through Table V to determine the desired "M" value. Neither lead connector should make electrical contact with more than one tap at a time.

Line Angle Adjustment

Maximum sensitivity angle is set for 75° (current lagging voltage) in the factory. This adjustment need not be disturbed for line angles of 65° or higher. For line angles below 65° set for 60° maximum sensitivity angle by adjusting the compensator loading resistors R_1, R_2, R_3, R_4. Refer to repair calibration under "Maximum Torque Angle Adjustment," when a change in maximum sensitivity angle is desired. For zone 2 and 3 or pilot trip application no need to recalibrate relay.

In general, the change in maximum torque angle adjustment, if desired, can be avoided. In this case the tap plate setting of the relay is adjusted to compensate for difference in the maximum torque angle of the relay (75°) and the characteristic angle of the line 8, according to the following equation: (In this case, follow procedure underlined under alternative calculations & settings).

$$Z_{1'0} = \frac{Z_{1,0}}{\text{Cos}\,(75° - \theta)}$$

Here $Z_{1,0}$ – Tap Plate Setting.

$Z_{1,0}$ – Desired Ohmic Reach

Phase-to-Phase Desensitizer

When it is necessary to disconnect this circuit unsolder or cut terminal 8 to the 2ϕ-6 board (see Figure 31).

INSTALLATION

The relays should be mounted on switchboard panels or their equivalent in a location free from dirt, moisture, excessive vibration and heat. Mount the relay by means of the mounting stud for the type FT projection case or by means of the four mounting. holes on the flange for the semi-flush type FT case. Either the stud or the mounting screws may be made directly to the terminals by means of screws for steel panel mounting or to the terminal stud furnished with the relay for thick panel mounting. The terminal stud may be easily removed or inserted by locking two nuts on the stud and then turning the proper nut with a wrench.

For detailed information on the FT case refer to I.L. 41-076.

EXTERNAL CONNECTIONS

Figure 22 shows typical connection for single zone protection using an SDG relay. SPP capacitors are not required unless surge voltage may exceed 2500 volts.

ACCEPTANCE TEST

Acceptance tests consists of:

1. A visual inspection.
2. "Push-button" - check.
3. An electrical test to make certain that the relay measures the balance point impedance accurately.

1. Visual Inspection

Give a visual check to the relay to make sure there are no loose connections, broken resistors or broken wires.

.2-4.35 Ohm Relay	1.0-31.0 Ohm Relay
All T = 1.23	All T = 8.7
All T_0 = 3.69	T_0 = 26.1
All S = 1	All S = 1
All M = +.18	All M +.18

2. Push-Button Check

For SDG - only open relay terminal 10 and 11.

Using the test connections of Fig. 40. Connect the a-c voltages as per test No. 1. No current connections are required. Connect the rated d-c voltages as shown. Open circuit the connections to terminal No. 7. Set $V_{BN} = V_{CN} = 70$ volts. Depress the white pushbutton. The pushbutton should light. If the pushbutton does not light, connect a d-c voltmeter or a 25 watt lamp as per Fig. 40. The voltmeter should have a minimum deflection of at least 5 volts. If there is a deflection but the lamp does not light this indicates a fault in the pushbutton circuit. If there is no indication proceed with the electrical test to isolate the fault in the pushbutton circuit or the relay.

3. Electrical Tests

Distance Unit

Tripping is indicated for the SDG relay when the 25 watt lamp shown on Fig. 23 turns on and for SDG-1, -2, -3, & -4, -5 relays when DC voltmeter indicates a minimum deflection of 5 volts for balance point condition. Refer to Fig. 40 for all test connections.

For .2-4.35 Ohm Relay

A. Use connections for test No. 5 and Set V_{AN} voltage = 20 volts. $V_{BN} = V_{CN} = 70$ volts. Set the phase shifter for 75° current lagging voltage.

   The relay current required to make the trip should be between 8.0-8,6 amp.

B. Use connections for Test No. 6 and set V_{BN} voltage = 20 volts. $V_{AN} = V_{CN} = 70$ volts. Set the phase shifter as above. The relay trip current should be 8.0-8.6 amps.

C. Use connections for Test No. 7 and set V_{CN} = 20 volts $V_{AN} = V_{BN} = 70$ volts. Set the phase shifter as above. The SDG relay trip current should be 8,0 - 8.6 amp.

For 1.0 - 31.0 Ohm Relay

A. Use connections for test #5 and set $V_{AN} = V_{BN} = V_{CN} = 70$ volts. Set the phase shifter for 75° current lagging voltage. The relay trip current should be 3.95 - 4.20 amperes.

B. Use connections for test #6 and set $V_{AN} = V_{BN} = V_{CN} = 70$ volts, and set the phase shifter as above. The relay trip current should be 3.95 - 4.20 amperes.

C. Use test connections for test #7 and set $V_{AN} = V_{BN} = V_{CN} = 70$ volts. Set the phase shifter as above. The relay trip current should be 3.95 - 4.20 amperes.

If the electrical response is outside the limits a more complete series of tests outlined in the section titled "Calibration" may be performed to determine which component is faulty or out of calibration.

If it is desired to check relay response at some other settings use following equation for the trip value of current.

$$I = \frac{3V_{LN}}{(2+p)\,Z_1}, \text{ where } p = \frac{Z_0}{Z_1}$$

Z_0 = Zero sequence reach

Z_1 = Positive sequence reach (in above cases p = 3)

V_{LN} = desired fault voltage

WARNING If testing required trip current over 15 amp. over prolonged periods, it is recommended that a heavy short lead be connected from terminal 19 to the center tap of T_0 socket. Also connect a jumper lead from terminal 16 to terminal 1 on the large printed circuit board for SDG-1 and SDG-3 relays and terminal 2 to terminal 4 for SDG relay on the large printed circuit board. (Lower set of terminals rear view).

MAXIMUM TORQUE ANGLE

Maximum torque angle check is optional. In general, this check is complicated for SDG, SDG-1 and SDG-2 relays by the presence of transient blocking circuit, and the two-phase-to-ground fault desensitizer circuit.

The presence of transient blocking circuit requires that check for maximum torque angle should be made going from non-tripping to tripping condition at each end of the tripping range of the relay under test. Since the lab method of testing as used here presents artifical voltage conditions, under certain voltage and phase angle condition two-phase-to-ground desensitizer will distort phase angle response; hence, it is required to disable the 2ϕ-G for SDG-1, SDG-2, SDG-5 by connecting 10K resistor between terminals #10 to #1 on large printed circuit board (for SDG relay between terminal #10 and #4).

To disable transient blocking circuit short out resistor R48 on large printed circuit board.

Phase A Check

Use connection #5. Relay tap settings should be the same as before. For all ranges set $V_{AN} = 20$ volts, $V_{BN} - V_{CN} = 70$ volts.

Set current for 1-30 ohm relay for 1.54 amp, and for .2 - 4.35 ohm relay for 11 amp. Set phase-shifter for 75° current lagging V_{AN} voltage. Turn phase-shifter toward 0° after relays have dropped out reverse phase-shifter rotation and note the angle (ϕ 1) at which relay is fully tripped. Then rotate the phase-shifter past the 75° until relay resets again. Then rotate phase shifter toward 75° again until relay is fully tripped. Note the angle again (ϕ 2).

Maximum torque angle is equal then to

$$\frac{\phi 1 + \phi 2}{2} = 75° \ (\pm 3°)$$

Any other T setting may be used, except use 130% current of the trip current at 75° angle.

Phase B Check

Use connection #6. Set V_{BN} = 20 volts. V_{AN} = V_{CN} = 70 volts. Otherwise follow the same procedure as for Phase A.

Phase C Check

Use connection #7. Set V_{CN} = 20 volts, V_{AN} = V_{BN} = 70 volts. Otherwise follow the same procedure as for Phase A. When completed remove 10K resistor and jumper from R48 resistor.

TWO-PHASE-TO-GROUND DESENSITIZER CHECK

Use connection #5, except no current connection is required for this test.

AB - Combination

Set V_{CN} = 70 V. V_{AN} = V_{BN} = 10 volts. Check d-c voltage on small P.C. board located just behind R1-R4 potentiometers terminal "10" (positive) located behind R1 potentiometer (second from the bottom) and relay terminal "2". It should measure 11.5 to 20 volts. Reset V_{AN} = V_{BN} = 70 volts. DC output should disappear.

BC - Combination

Same check as for AB except first set V_{AN} = 70 V. V_{BN} = V_{CN} = 10 volts and then reset V_{BN} = V_{CN} = 70 volts.

CA - Combination

Same check as for AB except first set V_{BN} = 70 v. V_{CN} = V_{AN} = 10 volts and then reset V_{CN} = V_{AN} = 70 volts.

Overcurrent Unit

Check operation of the overcurrent unit by using ✪ test connection #5 of the Fig. 40. Set V_{AN} = 0, V_{BN} = V_{CN} = 70 volts. The .2 - 4.35 ohm relay should operate at .75 - .83 amperes, and the 1 - 31.0 ohms relay should operate at .37 - .420 amperes. If not, check adjustment of R63 potentiometer.

Indicating Contactor Switch (ICS) (SDG Only)

With the SDG relay tripping, pass sufficient d-c current through the trip circuit to close the contact of the ICS. This value of current should be not less than 1,0 ampere or greater than 1.2 amperes, for the 1 ampere ICS. The current should not be greater than the particular ICS tap setting being used for the 0.2 - 2.0 ampere ICS. The operation indicator target should drop freely.

The contact gap should be approximately 0.047" for the 0.2 - 2.0 ampere unit and 0.070" for the 1.0 ampere unit between the bridging moving contact and the adjustable stationary contacts. The bridging moving contact should touch both stationary contacts simultaneously.

ROUTINE MAINTENANCE

The relays should be inspected periodically, at such intervals as may be dictated by experience, to insure that the relays have retained their calibration and are in proper operating condition.

"In-Service Test" (If relay is set for S = 1 only)

In-service testing is performed as follows:

1. 1. Open relay trip circuit by opening red handle switch No. 11 for SDG-1, -2, -3, -4, -5. For SDG relay open No. 10 and No. 11. (Fig. 20)
   2. Open relay voltage terminal 7.
   3. Press white pushbutton. Pushbutton light should light.

   This test checks out the operation of the magnitude comparator and output circuitry.

   When pushbutton is used for direct breaker trip, depress pushbutton for short time only.

REPAIR CALIBRATION

Use the following procedure for calibrating the relay if the relay has been taken apart for repairs or the adjustments disturbed. Printed circuit boards styles are components are identified on Figures 14 to 10. Component location as per Fig. 26 to 37.

For easier access to the parts, the relay should be tested without the case.

✪ Use Fig. 23 for Test Point Traces reference.

Part A Preliminary Settings

1. Remove the printed circuit board(s) (PCB) in the rear of the relay.

2. Set R_1, R_2, R_3, R_4 potentiometers fully counter-clockwise for maximum resistance.

3. Set relay for S = 1, M = +18 ("L" lead over "R" lead), all T = 8.7, T_0 = 26.1 for the 1.0 - 31.0 ohm relays and for the .2 - 4.35 ohms relay all T = 1.23 T_0 = 3.69.

Part B Voltage Circuit Tests

1. Apply 3 phase balanced voltages as per test 1 ✪ of Fig. 40. except no current is applied.

2. Set $V_{AN} = V_{BN} = V_{CN}$ = 70 volts a-c. Measure following a-c voltages.

   From relay terminal 6 to S_A = 1 Tap 70 (±1) volts

   From relay terminal 6 to S_A = 2 Tap 140 (±2) volts

   From relay terminal 6 to S_A = 3 Tap 221 (±3) volts on latest relays, it should measure 210 (±3) volts.

   From relay terminal 6 to R_A lead 39.2 (± 5) volts

   Repeat the same measurements for S_B, S_C, and R_B, R_C leads.

3. Disconnect R_0 lead from M_O=0 Tap and measure the voltage from relay terminal "4" to the R_0 lead. It should be below 0.7 volts ac.

4. Apply rated d-c voltage to the relay. Check the d-c voltage across the lower set of plug-in terminals (rear view) "5" and "1" for the SDG-1, -2, -3, & -4 relays and terminals "6" and "4" for the SDG relay. It should measure 20 (±2) volts. (Notice 250 V. d-c relay requires external resistor.

5. Plug in the lower and upper boards.

Part C Potentiometer Adjustments

NOTE: All potentiometers are locked type and should be unlocked before adjustment and locked after adjustment is complete.

1. Set R5, R6, R7, R8 for maximum setting (counter-clockwise).

2. If no scope is available then measure the voltages with a Rectox-type voltmeter across the specified terminals of the small upper terminal board located in the rear. All the following measurements are done on the small upper board. Terminal numbers refer to this board only. Use of scope is preferred.

R5 Adjustment

Measure the voltage across terminals 2 & 3. Adjust R5 until voltages across 4 & 2 and 4 & 3 are equal (±0.1 volt) to each other and are within 1.0 volt of voltage across 2 & 3. If oscilloscope is available observe voltage across R9 and set R5 so that two peaks on the 360Hz ripple are equal and the third slightly higher.

R6 Adjustment

Measure the voltage across terminals 6 & 8. Adjust R6 until voltages across terminals 7 and 6 and 7 and 8 are equal (±.1 volt) to each other and are within 1.0 volt of voltage across 6 & 8. If oscilloscope is available observe voltage across R10 and set R6 so that two peaks are equal and the third slightly higher.

R7 Adjustment

Measure the voltage across terminals 17 and 18. Adjust R7 until voltages across terminals 15 and 18 and 15 and 17 are equal (±0.1 volt) to each other and are within 1.0 volt of voltage across 17 and 18. If oscilloscope is available observe voltage across R11 and set R7 so that two peaks are equal and the third slightly higher.

R8 Adjustment

Reduce V_{AN} to zero and measure the voltage across terminals 11 & 12. Adjust R8 until voltages across terminals 14 and 11 and 14 and 12 are equal (±0.1 volt) to each other and are within 1.0 volt of voltage across 11 & 12. If oscilloscope is available observe voltage across R12 and set R8 so that the two lower valleys are equal and the third lower.

Maximum Torque Angle Adjustment

Disconnect all R & L leads and jumper relay terminals 5 & 6.

R-1 Adjustment

For the 1.0 - 31.0 ohm relay use the #1 test ✪ connection of Fig. 40. Apply 5.08 amp. a-c current to the relay. Set V_{AN} 45 volts and $V_{BN} = V_{CN} = 0$ volts. Set the phase shifter for 75° current lagging voltage.

For .20-4.35 ohm relay use the same procedure as above except set the current for 15.65 amp. and V_{AN} = 20 volts.

Insert an a-c voltmeter of 0.3 volts range between R_A and L_A leads. Adjust R1 potentiometer for a minimum ("null" reading) and lock R1 in place. Vary current slightly to achieve lower "null" reading.

For other angles multiply current by $K = \frac{\text{Sin } 75}{\text{Sin } \theta}$ where θ = desired maximum torque angle, for $\theta = 60°$ K = 1.11.

R2 Adjustment

Use #2 test connections of Fig. 40. Set V_{BN}=45 volts and $V_{AN} = V_{BN} = 0$ volts. Set $I_B = 5.08$ amps. 75° lagging V_{BN}. (Modify voltage and current settings for the .2-4.35 ohm relay as above). Measure the voltage between R_B & L_B leads. Adjust R2 potentiometer for a minimum ("null" reading) and lock R2 in place.

R3 Adjustment

Use #3 test connections of Fig. 40. Set V_{BN} = 45 volts and $V_{AN} = V_{BN} = 0$ volts. $I_C = 5.08$ amp. 75° lagging V_{CN}. (Modify voltage and current for the .2 - 4.35 ohm relay as above).

Measure the voltage between R_C and L_C leads. Adjust R3 potentiometer for a minimum ("null" reading) and lock R3 in place.

R4 Adjustment

Remove jumper from relay terminals 5 and 6. Use the #4 test connections of Fig. 40. Connect all "L" and "R" leads back to previous setting, except R_0-lead. Set $V_{CN} = 0$ and $V_{AN} = V_{BN} = 70$ volts. Set $I_C = 2.34$ amp. 75° lagging V_{CN}. (For the .2 to 4.35 relay set $V_{CN} = 0$ and $V_{BN} = V_{AN} = 45$ volt. $I_C = 9.9$ amperes). Measure the voltage between R_0 and the lowest M_0 tap marked "0".

Adjust the R-4 potentiometer for minimum voltage ("null" reading) and lock R4 in place.

Part D M Taps Check

Use a Rectox-Type Voltmeter.

Open all "R" & "L" leads.

M_A Taps - Use test connection #1 of Fig. 40. Pass 10 amp. current through the relay. The voltage should read the following.

1.5 (±0.2) volts for between 0 tap and .03 tap

6.0 (±0.6) volts 1-30 between 0 tap and .09 tap

9.0 (±1.0) volts Ohms between 0 tap and .06 tap

M_B Taps - Use test connection #2 and repeat above.

M_C Taps - Use test connection #3 and repeat above.

M_0 Taps - Use test connection #4 and repeat above.

For .2 - 4.35 ohm relay.

NOTE: Provide a jumper from terminal 19 to center tap of the T_0 tap block for the SDG, SDG-1, and -3 relays.

M_A Taps - Use connection #1 of Fig. 40. Pass 20 amp. of current through relay. The voltage should read the following.

.425 (±.05 volts) between "0" tap and ".03" tap

1.70 (± .1 volts) between "0" tap and ".09" tap

2.55 (± .1 volts) between "0" tap and ".06" tap

M_B Taps - Use test connection #2 and repeat above.

M_C Taps - Use test connection #3 and repeat above.

Part E - Overcurrent Detector (For SDG, SDG-1, SDG-3)

1. Energize d-c circuit with rated d-c voltage.
2. Use test connection #5. Set $V_{AN} = 0$, $V_{BN} = V_{CN} = 70$ volts. Set current for 0.4 ampere for 1 - 30 ohm relays, and for 0.8 ampere for .2-4.35 ohm relays.

   Check relay output at test point 12 with voltmeter or oscilloscope. There should be a continuous output of 18-22 volt level under conditions specified above. Adjust R63 potentiometer for specified pickup current. Dropout should occur at:

   .38 to .3 amp for 1-30 ohm relays

   .76 to .6 amp for .2-4.35 ohm relays

Part F - Magnitude Comparator Circuit Adjustment (large Printed Circuit Board) - All Relays

R33 Adjustment

Energize relay with d-c only. Connect 10K resistor (±5%) between TP1 of the large PC board and relay term. 2. Use scope to monitor TP9 and adjust R33 until a positive output is obtained at TP9 (17- 23 volts).

Frequency Verifier Adjustment (For SDG, SDG-1-2)

Use oscilloscope to observe wave shape at test point TP10. Use test connection #5. Set V_{AN} = 0 V_{BN} = V_{CN} = 70 volts. Set current for 2.5 amps lagging voltage by 75°. Adjust R45 for SDG and R76 for SDG-1 until less than 1 volt signal of 4.0 to 4.3 ms duration is followed by a positive pulse (17-23 volts) of approximately 4 ms duration. See Test Point Wave Shape, Fig. 23A.

Impedance Check

Start with 2.5 volts test. Use voltmeter for monitoring the relay output, first short deflection as positive indication of meeting current limits. Then increase current slightly to see if full 18 volt d-c output is obtained. There should be no drop in output to zero volts while current is increased. If the currents are outside the limits for 2.5 volt-test outlined below, proceed as follows:

Set V_{AN} = V_{BN} = V_{CN} = 70 volts as close to each other as possible. Use connection #5. No current is applied. Measure DC voltage across R9, R10, R11 resistors. Readjust potentiometers R5, R6, R7 until the voltages across R9, R10, R11 are as close to each other as possible. These voltages should be in 20-25 volts range. In most cases only slight adjustment of R5, R6, or R7 will be required. Then recheck pickup current for 2.5 volt test again. If the pickup currents are close together but outside the specified limits readjust R18 or R8 to move all pickup values up or down. Note that R5, R6, R7 are interacting. Hence, recheck all three voltages after each adjustment if difficulties in balancing at 2.5 volts persist use 5 volts and double the limits. If it is desired to check relay response at some other settings use following equation for the trip value of current.

$$I = \frac{3V_{LN}}{(2+p)Z_1}, \text{ where } p = \frac{Z_0}{Z_1}$$

Z_0 = Zero sequence reach

Z_1 = Positive sequence reach (in above cases p = 3)

V_{LN} = Faulted Phase Voltage

1 - 30 OHM

SDG, SDG-1, SDG-3, and SDG-4, SDG-5 Relays

Using previous relay tap settings, apply rated d-c voltage and proceed as follows.

PART A: 2.5 VOLT TEST

A. PHASE A

Use test connection #5. Set V_{AN} = 2.5 volts. V_{BN} = V_{CN} = 70 volts.

Adjust R18 for proper pickup level. Pickup current should be (amp) .140 - .155, 75° lagging voltage. Disable overcurrent unit for this test by jumpering large board terminals 2 and 4 for SDG; terms 1 and 16 for SDG-1 and 3.

B. PHASE B

Set V_{BN} = 2.5 volts. V_{AN} = V_{CN} = 70 volts. Pickup current should be -140 - .155 - 75° lagging V_{BN} voltage.

C. PHASE C

Set V_{CN} = 2.5 volts. V_{AN} = V_{CN} = 70 volts use connection #7. Pickup current should be .140 - .155 - 75° lagging V_{CN} voltage. If limits above are not met, see note under "IMPEDANCE TEST". Remove jumpers from overcurrent unit.

PART B 70 VOLTS TEST

A. Use connections for test #5 and set V_{AN} = V_{BN} = V_{CN} = 70 volts. Set phase shifter for 75° current lagging voltage. The relay trip current should be 3.95 - 4.20 amperes.

B. Use connections for test #6 and set V_{AN} - V_{BN} = V_{CN} = 70 volts, and set the phase shifter as above. The relay trip current should be 3.95 - 4.20 amperes, lagging 75° V_{CN} voltage.

C. Use test connections for test #7 and set V_{AN} = V_{BN} = V_{CN} — 70 volts. Set the phase shifter as above. The relay trip current should be 3.95 - 4.20 amperes, lagging 75° V_{CN} voltage.

PART C: S = 3 TEST

Set S_A, S_B, S_C = 3. Set V_{BN} = V_{CN} = 70 volts. V_{AN} = 10 volts. Disable overcurrent unit again as for 2.5 volts test.

PHASE A

Use test connection #5. Pickup current I A should be (amp.) - .190 - .218 - 75° lagging voltage.

PHASE B

Set V_{BN} = 10 volts $V_{CN} - V_{AN}$ = 70 volts. Use test connection #6. Pickup current I_B should be .190 - .218 amp 75° lagging V_{BN} voltage.

PHASE C

Set V_{CN} = 10 volts $V_{AN} = V_{BN}$ = 70 volts. Use test connection #7. Pickup current I_C should be .190 - .218 amp 75° lagging V_{CN} voltage. Remove jumpers from overcurrent unit. Return all connections to S = 1.

.2 - 4.25 OHM RELAY

SDG, SDG-1, SDG-2, SDG-3, SDG-4, SDG-5 Relays

Using previous relay tap settings, apply rated d-c voltage and proceed as follows.

PART A: 2.5 VOLT TEST

PHASE A

Use test connection #5. Set V_{AN} - 2.5 volts. $V_{BN} = V_{CN}$ = 70 volts. Pickup current should be 1.0 - 1.10 amp 75° current lagging voltage. Adjust R18 for proper pickup level.

PHASE B

Set V_{BN} = 2.5 volts, $V_{AN} = V_{BN}$ = 70 volts. Use test connection #6. Pickup current should be 1.0 - 1.10 amp - 75° lagging V_{BN} voltage.

PHASE C

Set V_{CN} = 2.5 volts, $V_{AN} = V_{BN}$ = 70 volts. Use test connection #7. Pickup current should be 1.0 - 1.10 amp - 75° lagging V_{CN} voltage.

If limits above are not met see special note under "Impedance Test."

PART B: 20-VOLT TEST

PHASE A

Use test connection #5. Set V_{AN} = 20 volts. $V_{BN} = V_{CN}$ = 70 volts. Set phase shifter for 75° current lagging voltage. Pickup current I_A should be 8.05 - 8.55 amp, 75° lagging V_{AN} voltage.

PHASE B

Set V_{BN} = 20 volts, $V_{AN} = V_{CN}$ = 70 volts. Use test connection #6. Pickup current I_B should be 8.05 - 8.55 amp, 75° lagging V_{BN} voltage.

PHASE C

Set V_{CN} = 20 volts, $V_{AN} = V_{BN}$ = 70 volts. Use test connection #6. Pickup current I_C should be 8.05-8.55 amp, 75° lagging V_{CN} voltage.

PART C: S = 3 TEST

Set $S_A = S_B = S_C$ = 3. Set V_{AN} = 10 volts. $B_{BN} = V_{CN}$ = 70 volts.

PHASE A

Use test connection #5. Pickup current I_A should be 1.35 - 1.43 75° lagging V_{AN} voltage.

PHASE B

Set V_{BN} = 10 volts $V_{AN} = V_{CN}$ = 70 volts. Use test connection #6. Pickup current, I_B should be 1.35 - 1.43 amp 75° lagging V_{BN} voltage.

PHASE C

Set V_{CN} = 10 volts, $V_{AN} = V_{BN}$ = 70 volts. Use test connection #7. Pickup current I_C should be 1.35 - 1.43 amp 75° lagging V_{CN} voltage.

Return all "S" connections to S = 1.

PUSHBUTTON TEST

Use test connection #1. No current is required. Apply d-c to the relay. Open circuit voltage connection to relay terminal #7. Set $V_{BN} = V_{CN}$ = 70 volts. Depress white pushbutton and it should light.

Indicating Contactor Switch (when used)

With relay tripped, pass sufficient d-c current through the trip circuit to close the contacts of ICS. This value of current should be not less than 1.0 ampere, nor greater than 1.2 amperes for the 1 ampere ICS. The current should not be greater than the particular ICS setting being used for the 0.2-2.0 amperes ICS. The operation indicator target should drop freely.

The contact gap should be approximately 0.047" for the 0.2-2.0 ampere unit and 0.070" for the 1.0 ampere unit between the bridging moving contact and the adjustable stationary contacts. The bridg-

ing moving contact should touch both stationary contacts simultaneously.

RENEWAL PARTS

Repair work can be done most satisfactorily at the factory. However, interchangeable parts can be furnished to the customers who are equipped for doing repair work. When ordering parts, always give the complete nameplate data, and component style number given in the electrical parts list.

See detailed Internal Schematics for printed circuit styles and reference Dwg. list for component location details.

APPENDIX 1

MUTUAL IMPEDANCE EFFECT

Do not compensate a zone 1 or pilot-trip relay because of loss of directional sensing for a nearby fault on the mutually couples line. By not compensating for zone 1-setting, the relay reach varies between 85 percent and 70 percent of the line impedance if relay is set for 85 percent of the line impedance.

Where mutual compensation of zone 2 (timed trip) is desired, a type IK auxiliary current transformer (Fig. 39 and 41) may be used with a step-down current ratio of: $\frac{Z_{OM}}{Z_{OL}} = C'$

Z_{OM} is the zero sequence mutual impedance, and Z_{OL} is the zero sequence self-impedance of line. Do not compensate a zone 1 or pilot-trip relay because of loss of directional sensing for a nearby fault on the mutually-coupled line.

The "parallel line" leads on the IK transformer are set for factor C' as defined above. The leads are set so that the difference between the taps is nearest to the desired C' value.

The external terminals of the IK transformer numbered 3 and 4 are connected across the SDG-3 relay terminals 19 and 18 as shown in the external schematic, Figure 22a. The external terminals 5 and 6 are connected in series with the residual CT circuit of the parallel line.

The IK transformer is set as follows: (a) Before the proper tap settings are made, the cover of the transformer should be completely open. Complete opening of the cover assures continuity in the residual current transformer circuits and isolates the IK transformer windings from the residual circuits. (b) The taps are set so that difference between the two taps is equal to the desired setting of C'. For instance, C setting equal to 8 is set by connecting leads coming out of opening marked "parallel line", Figure 41, to the terminals marked "C". Black lead (which is of the same polarity as the plug-marked external terminal) is connected to terminal marked ".2" and the white lead to the terminal marked "1.0". The difference between the two taps, 1.0 -.2 = .8, is the desired "C'" setting. To make this setting remove the top nut from the desired terminal, place the lug of the proper lead on the terminal and replace the locking nut. Make sure that the nut holds the lug snugly against the terminal to avoid the possibility of developing a loose or high-resistance connection.

The leads coming out of openings marked "protective relay" and "protected line" are connected to the terminals "0" and "1.0" in the row marked "C" observing the same polarity marking as above. This connection is the same for all "C" values less or equal to 1.

After the setting is completed, the cover should be closed to restore the connection between the transformer winding and the external terminals.

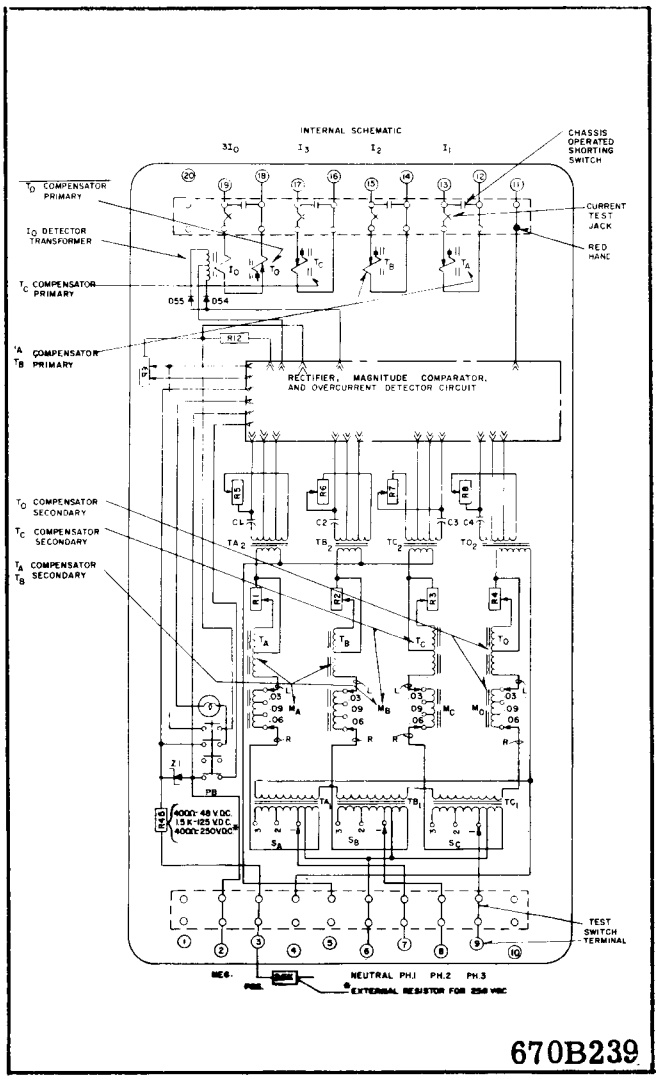


Fig. 8 Internal Schematic of the Type SDG-3 Relay in FT-42 Case.

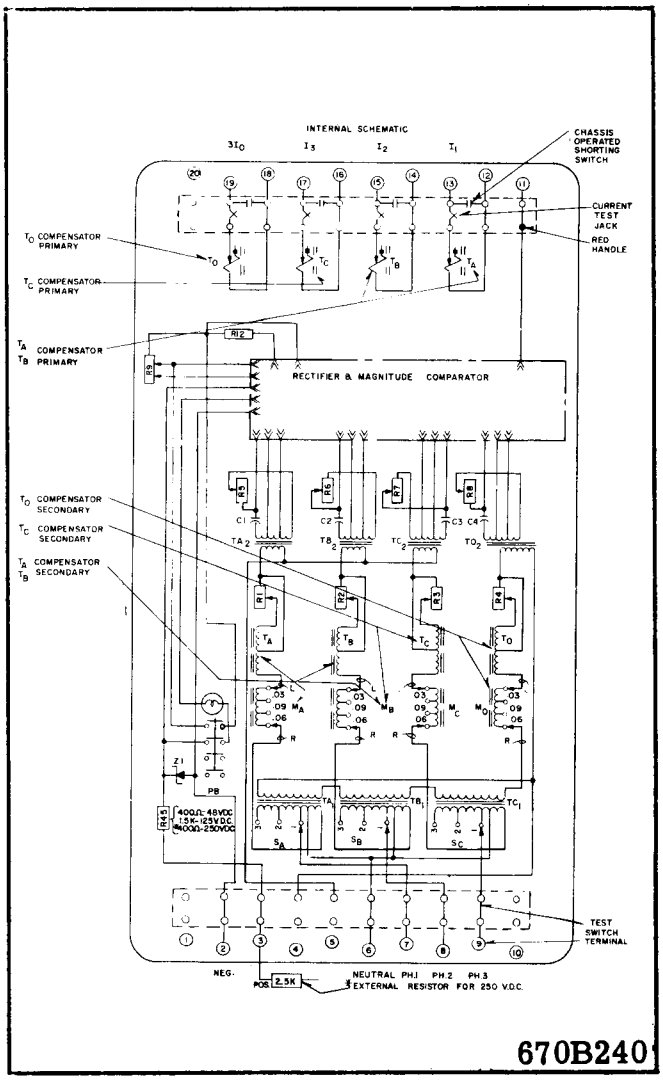


Fig. 9 Internal Schematic of the Type SDG-4 Relay in FT-42 Case.

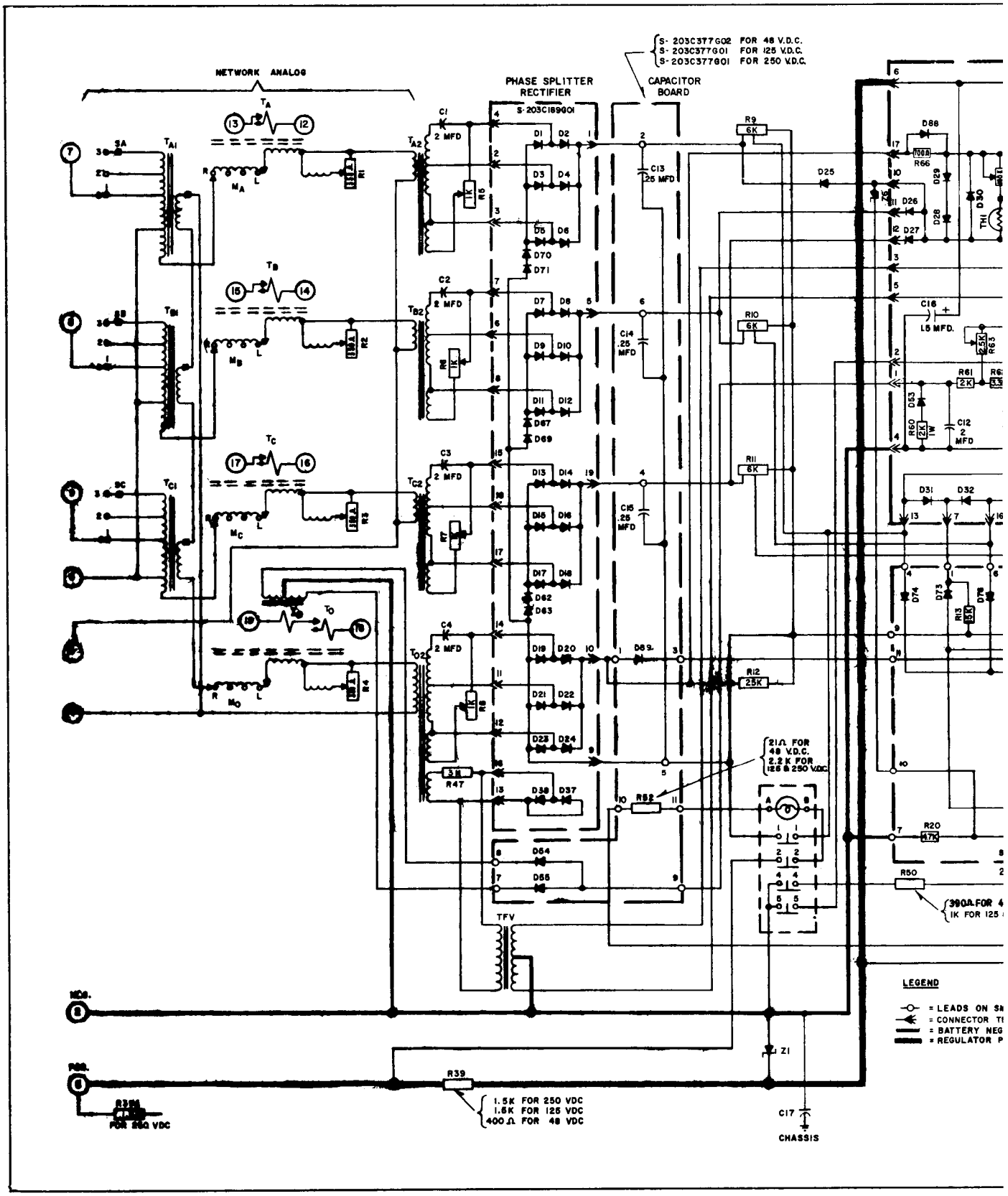
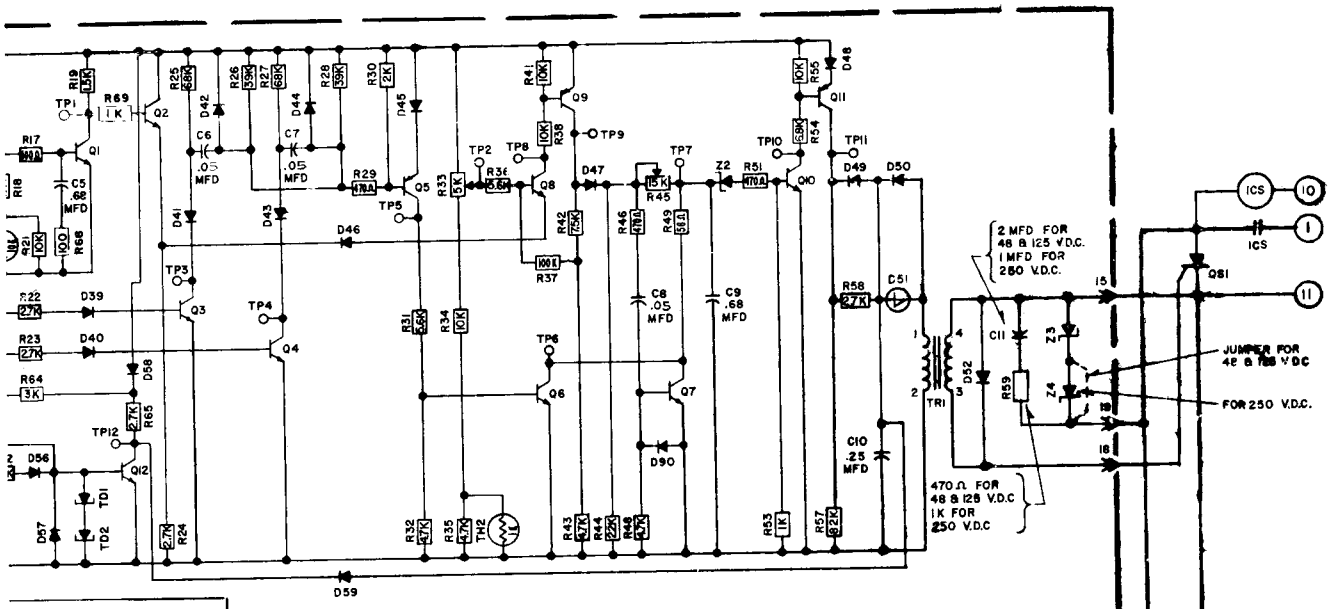
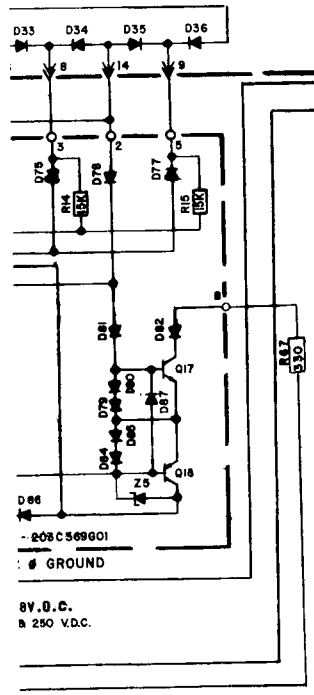


Fig. 5 Detailed Internal Schemat





SCHEMATIC SYMBOL	ENGINEERING REFERENCE	STYLE	REQ.
RI TO R4	POTENTIOMETER-350Ω-12½W	836A635H01	4
R5 TO R8	POTENTIOMETER- 1K -12½W	836A636H03	4
R18	POTENTIOMETER-100K- ¼ W	629A430H04	1
R33	POTENTIOMETER- 5K- ¼ W	629A430H07	1
R63	POTENTIOMETER-2.5K- ¼ W	629A430H03	1
R45	POTENTIOMETER- 15K- ¼ W	629A430H08	1
	RESISTORS		
R9 TO R11	6K-12 W	849A379H02	3
R12	25K-10 W	184A856H18	1
R13 TO R15	15K- 5 W	763A129H09	3
R39 (48 V.D.C.)	400Ω-25 W	184A856H14	1
R39 (125 & 250 V.D.C.)	1.5K-25 W	184A856H11	1
R39A (250 V.D.C.)	1.5K-40 W	1955645	1
R47	3K- 10 W	184A856H19	1
R60	2K- 1 W	187A643H34	1
R50 (125 & 250 V.D.C.)	1K- 3 W	763A127H02	1
R66	700Ω - 3 W	763A127H28	1
R17	100Ω - ½ W	629A531H09	2
R19 - R68	1.5K- ½ W	629A531H36	1
R20-R36-R48-R32-R43	4.7K- ½ W	629A531H48	5
R21-R34-R38-R41 R55	10 K- ½ W	629A531H56	5
R22-R23-R65-R58-R24	2.7K- ½ W	629A531H42	5
R53 - R69	1K- ½ W	629A531H32	2
R25-R27	68K- ½ W	629A531H76	2
R26-R28	39K- ½ W	629A531H70	2
R29-R46-R51	470Ω - ½ W	629A531H24	3
R30-R61	2K- ½ W	629A531H39	2
R31-R35	5.6K- ½ W	629A531H50	2
R37	100K- ½ W	629A531H80	1
R42	7.5K- ½ W	629A531H53	1
R44	22K- ½ W	629A531H64	1
R49	56Ω- ½ W	629A531H02	1
R59 (48 & 125 V.D.C.)	470Ω - ½ W	629A531H24	1
R62	3.3K- ½ W	629A531H44	1
R64	3K- ½ W	629A531H43	1
R59 (250 V.D.C.)	1K- ½ W	629A531H32	1
R54	6.8K- ½ W	629A531H62	1
R57	8.2K- ½ W	629A531H54	1
R52 (48 V.D.C.)	21Ω- 3 W	763A127H33	1
R52 (125 & 250 V.D.C.)	2.2K-3 W	763A127H11	1
R50 (48V.D.C.)	390 OHM - 3 W	763A127H09	1
R67	330Ω 1/2W	629A531H20	1
TRI	TRANSFORMER	629A453H02	1

SCHEMATIC SYMBOL	ENGINEERING REFERENCE	STYLE	REQ.
DI TO D27-	DIODE - 82N9	837A692H04	27
D28 TO D30-D39 TO D47-D49-D50-D52-D64 TO D69-D62-D63-D67-D69-D70-D71-D73 TO D80-D82-D84 TO D88-D90	DIODE - IN4385	184A855H14	43
D31 TO D36-D48	DIODE - IN3283	837A692H02	7
D37-D38-D48	DIODE - IN3283	837A692H02	3
D83	DIODE - IN4818	188A343H06	1
D81	DIODE - M4L2063	629A370H04	1
CI TO C3	CAPACITOR 2 MFD	606B540H06	3
C4	CAPACITOR 2 MFD	606B540H01	1
C5-C9	CAPACITOR .68 MFD	764A278H18	5
C6 TO C8	CAPACITOR .05 MFD	187A624H06	3
C10	CAPACITOR .25 MFD	187A624H02	1
C11 (48 & 125 V.D.C.)	CAPACITOR 2 MFD	184A662H07	1
C12	CAPACITOR 2 MFD	764A278H18	1
C13 TO C15	CAPACITOR .25 MFD	187A624H02	3
C11 (250 V.D.C.)	CAPACITOR 1 MFD	876A409H09	1
C16	CAPACITOR 1.5 MFD	187A300H08	1
C17	CAPACITOR .04 MFD	188A105H03	1
TH1	THERMISTOR 10 K	184A211H04	1
TH2	THERMISTOR 1 K	184A211H02	1
QS1	THYRISTOR (SCR) 2N1850A	184A814H05	1
Q2-Q8-Q10-Q12-Q17	TRANSISTOR 2N697	184A638H18	5
Q11-Q18	TRANSISTOR 2N1132	184A638H28	2
Q3-Q4	TRANSISTOR 2N336	184A638H06	2
Q5-Q9	TRANSISTOR 2N3443	849A441H01	2
Q6-Q7-Q1	TRANSISTOR 2N1417	184A638H02	3
TDI-TD2	TUNNEL DIODE IN3713	877A809H01	2
ZI	ZENER DIODE 1N5948	763A453H01	1
Z2	ZENER DIODE IN746A	837A692H01	1
Z3	ZENER DIODE 15KE100	878A611H01	1
Z4 (250 V.D.C.)	ZENER DIODE 15KE200	878A611H01	1
Z5-Z6	ZENER DIODE IN5988B	763A453H05	2

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ic of SDG Relay with Parts List.

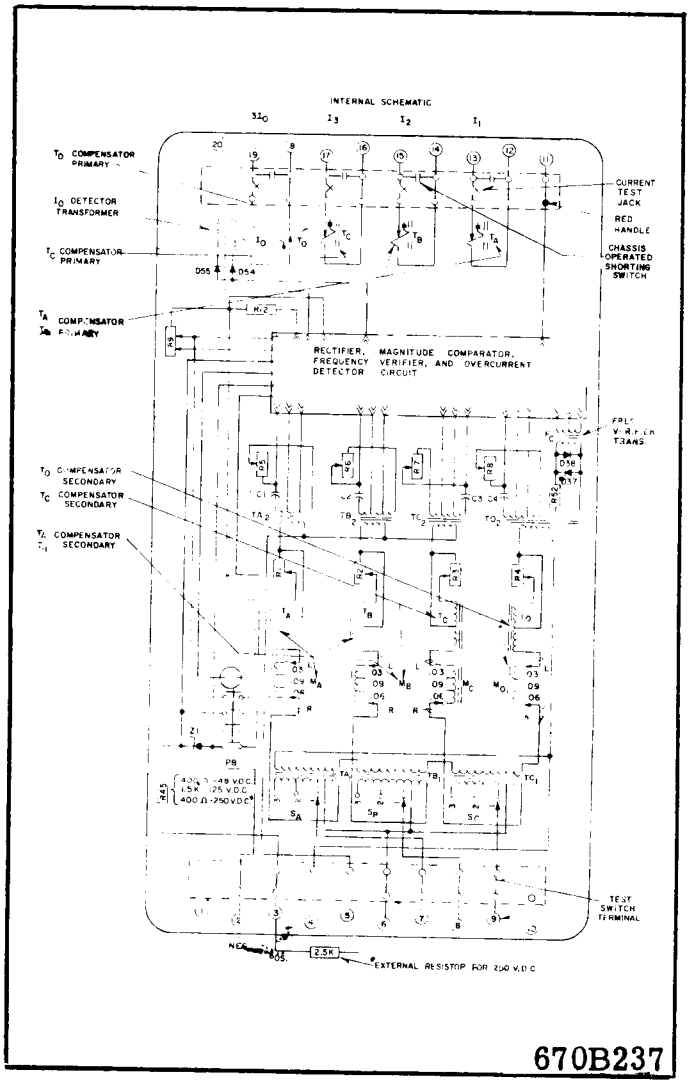


Fig. 6 Internal Schematic of the Type SDG-1 Relay in FT-42 Case.

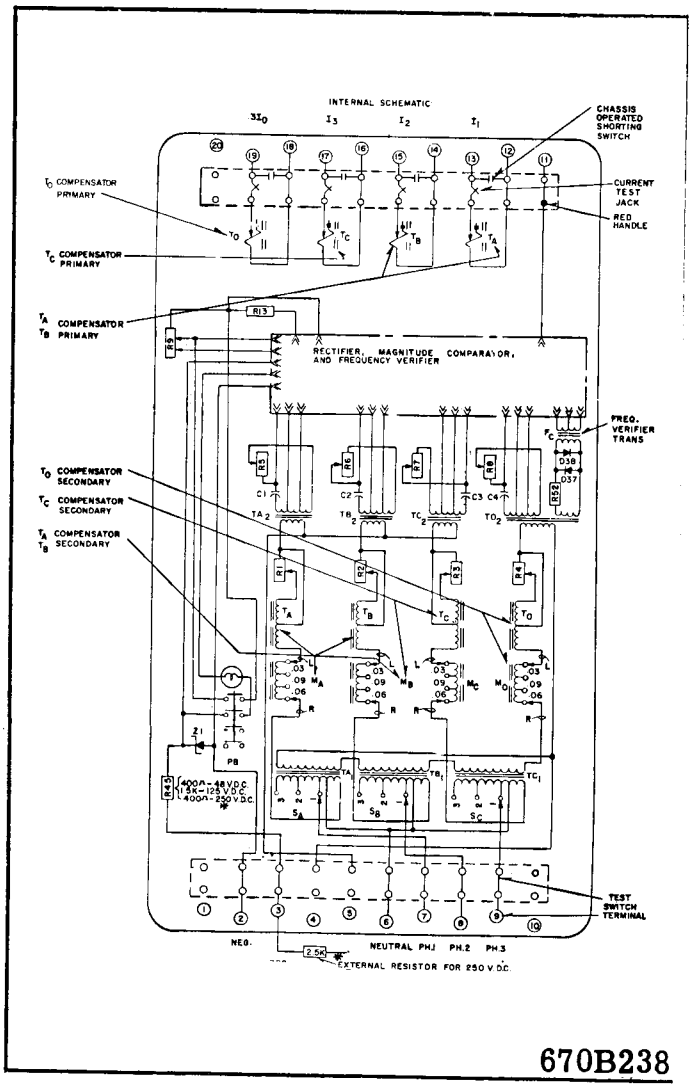
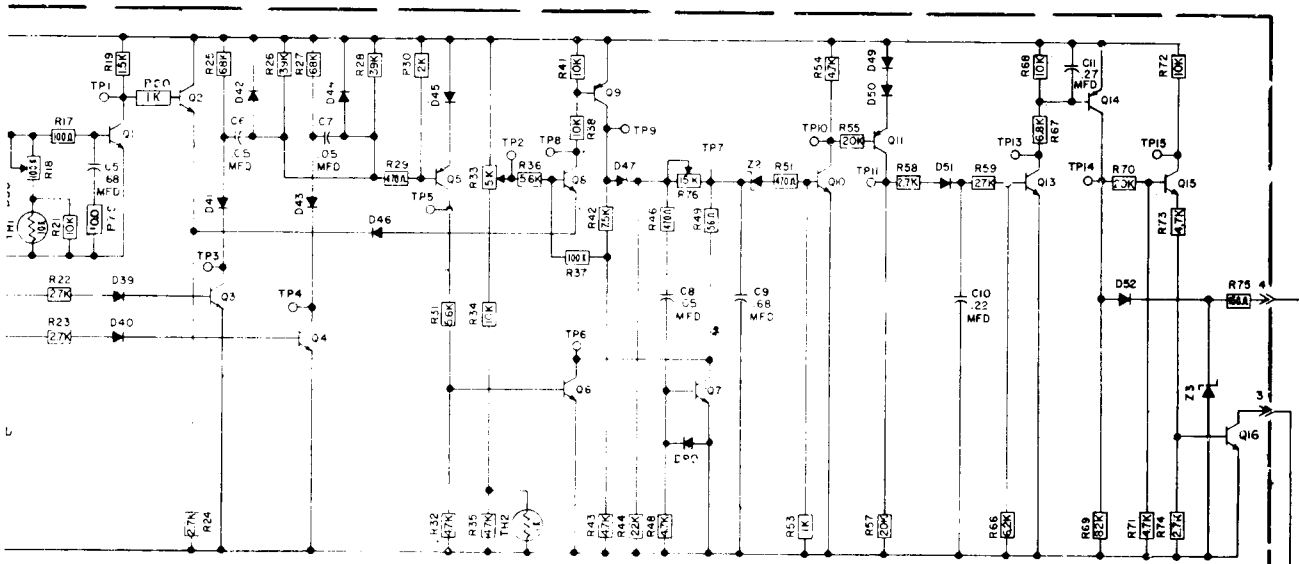
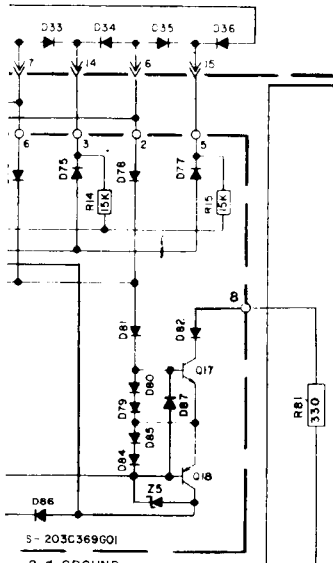


Fig. 7 Internal Schematic of the Type SDG-2 Relay in FT-42 Case.





SCHEMATIC SYMBOL	ENGINEERING REFERENCE	STYLE	REQ.
R1 TO R4	POTENTIOMETER 350Ω 12½W	836A635H01	4
R5 TO R8	POTENTIOMETER 1K 12½W	836A635H03	4
R18	POTENTIOMETER 100K ¼ W	629A430H04	
R33	POTENTIOMETER 5K ¼ W	629A430H07	1
R76	POTENTIOMETER 15K ¼ W	629A430H08	1
	RESISTORS		
R9 TO R11	6K 12 W	849A379H02	3
R12	25K 10 W	184A856H15	1
R13 TO R15	15K 5 W	763A129H09	3
R45 (48 @ 250 V.D.C.)	400Ω 25 W	184A856H14	1
R45 (125 V.D.C.)	1.5K 25 W	184A856H11	1
R45A (250 V.D.C.)	2.5K 40 W	1336127	1
R52	2K 10 W	184A856H19	1
R75	150Ω 3 W	762A679H01	1
R78	700Ω 3 W	763A127H28	1
R17 R79	100Ω ½ W	629A531H08	2
R19	1.5K ½ W	629A531H36	1
R69	82K ½ W	629A531H78	1
R21 R34 R38 R41 R68 R72	10K ½ W	629A531H56	6
R22 R23 R24 R74 R58	2.7K ½ W	629A531H42	5
R53 R60	1K ½ W	629A531H32	2
R25 R27	68K ½ W	629A531H76	2
R26 R28	39K ½ W	629A531H70	2
R29 R46 R51	470Ω ½ W	629A531H24	3
R30	2K ½ W	629A531H39	1
R31 R36	5.6K ½ W	629A531H50	2
R55 R57 R70	20K ½ W	629A531H63	3
R37	100K ½ W	629A531H80	1
R42	75K ½ W	629A531H53	1
R44	22K ½ W	629A531H64	1
R49	56Ω ½ W	629A531H02	1
R59	27K ½ W	629A531H66	1
R81	330Ω 1/2 W	629A531H20	1
R66	62K ½ W	629A531H51	1
R67	68K ½ W	629A531H52	1
R20 R32 R35 R43 R54 R71 R73	4.7K ½ W	629A531H48	7

SCHEMATIC SYMBOL	ENGINEERING REFERENCE	STYLE	REQ.
D1 TO D27	DIODE - 82N9	837A692H04	27
D28 TO D30 D39 TO D47 D49 TO D52 D59 - D62 D63 D67 D69 D70 D71 D73 TO D80 D82 D84 TO D88 D90	DIODE - IN4385	184A835H14	37
D31 TO D36 D89	DIODE - IN3283	837A692H02	7
D37 D38 D81	DIODE - IN3283	837A692H02	3
C1 TO C3	CAPACITOR 2 MFD	606B340H06	3
C4	CAPACITOR 2 MFD	606B340H01	1
C5 C9	CAPACITOR .68 MFD	764A278H16	2
C6 TO C8	CAPACITOR .05 MFD	187A624H08	3
C10	CAPACITOR .22 MFD	188A669H12	1
C11	CAPACITOR .27 MFD	188A669H05	1
C12	CAPACITOR 1.5 MFD	187A608H18	1
C13 TO C15	CAPACITOR .25 MFD	187A624H02	3
	CAPACITOR .04 MFD	187A624H09	1
TH1	THERMISTOR 10K	185A211H04	1
TH2	THERMISTOR 1K	185A211H02	1
Q2 Q8 Q10 Q13 Q15 Q17	TRANSISTOR 2N697	184A638H18	6
Q11 Q14 Q18	TRANSISTOR 2N1132	184A638H20	3
Q3 Q4	TRANSISTOR 2N336	184A638H06	2
Q5 Q9	TRANSISTOR 2N3645	849A441H01	2
Q6 Q7 Q11 Q16	TRANSISTOR 2N3417	848A851H02	4
Z1	ZENER DIODE 1N2984B	762A631H01	1
Z2	ZENER DIODE 1N759A	837A613H01	1
Z3	ZENER DIODE 1N3688A	862A288H01	1
Z5-Z6	ZENER DIODE 1N3035B	188A302H08	2

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matic of the SDG-2 Relay with Parts List.

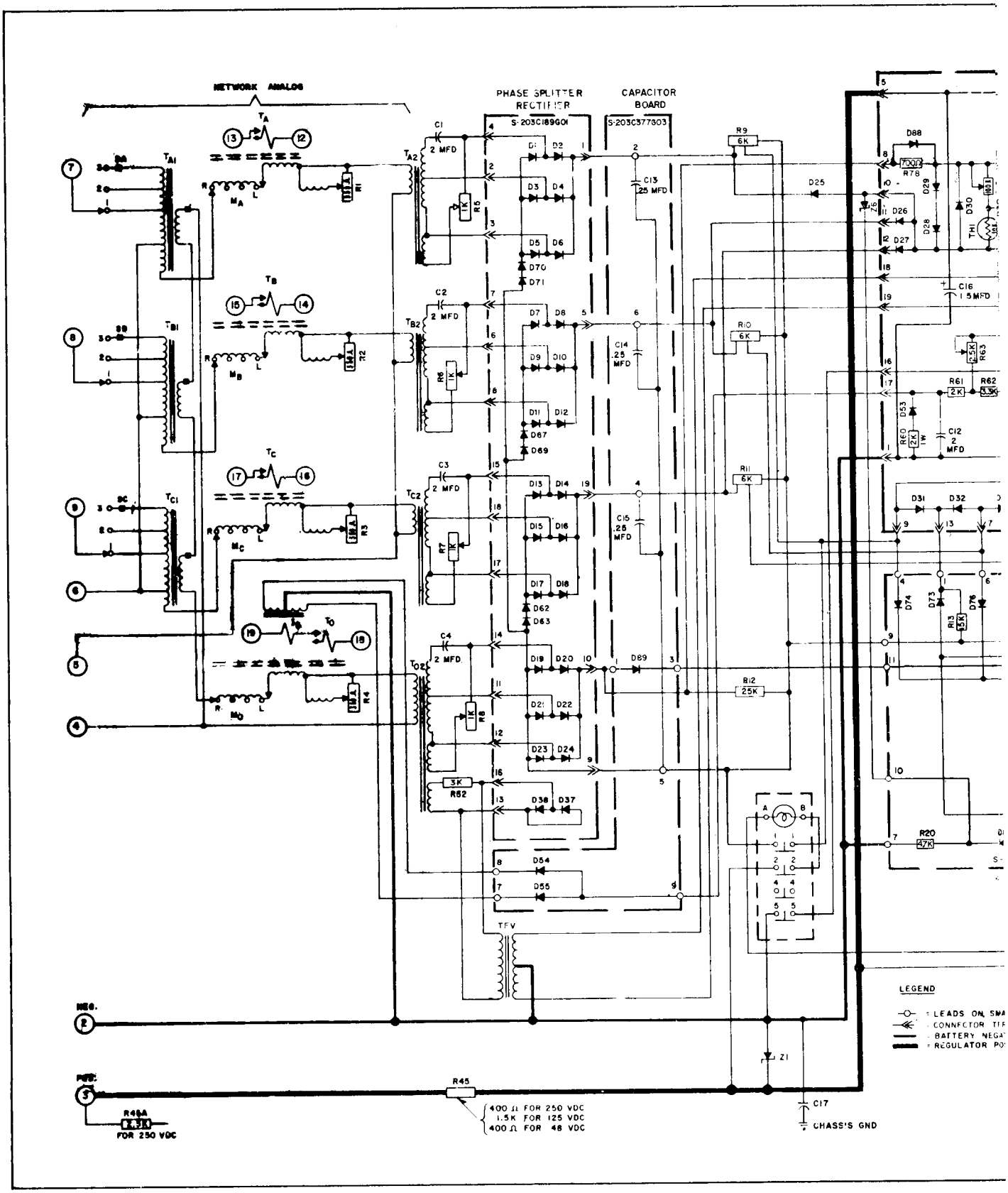
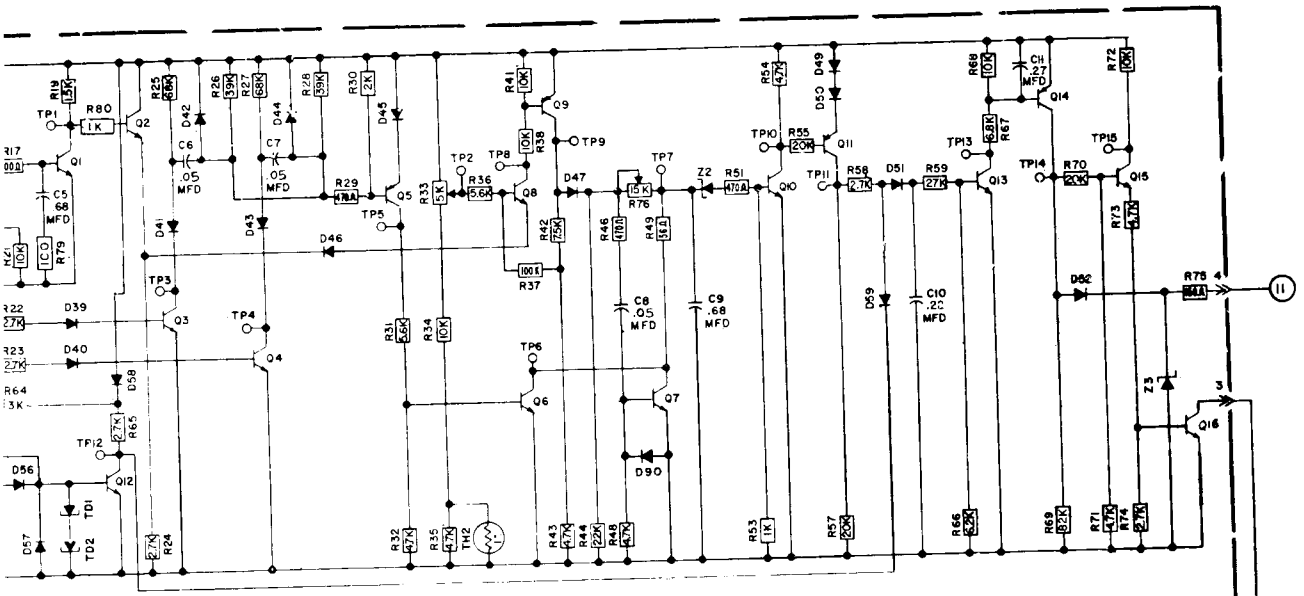


Fig. 10 Detailed Internal Schematic of th



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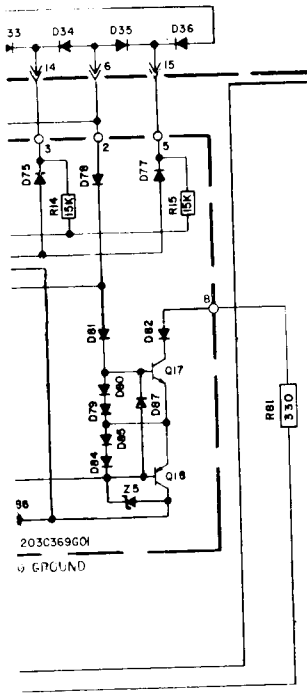
MAGNITUDE COMPARATOR



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SCHEMATIC SYMBOL	ENGINEERING REFERENCE	STYLE	REQ.
RI TO R4	POTENTIOMETER-350Ω-12½W	836A635H01	4
R5 TO R8	POTENTIOMETER-1K-12½W	836A635H03	4
R18	POTENTIOMETER-100K-¼ W	629A430H04	1
R33	POTENTIOMETER-5K-¼ W	629A430H07	1
R63	POTENTIOMETER-2.5K-¼ W	629A430H03	1
R76	POTENTIOMETER-15K-¼ W	629A430H08	1
	RESISTORS		
R9 TO R11	6K-12 W	849A379H02	3
R12	25K-10 W	184A856H15	1
R13 TO R15	15K-5 W	763A129H09	3
R45(48 & 250 V.D.C.)	400Ω-25 W	184A856H14	1
R45(125 V.D.C.)	1.5K-25 W	184A856H11	1
R45A (250 V.D.C.)	2.5K-40 W	1336127	1
R52	2K-10 W	184A856H19	1
R60	2K-1 W	187A643H34	1
R75	150Ω-3 W	762A679H01	1
R78	700Ω-3 W	763A127H28	1
R17 R79	100Ω-½ W	629A531H08	1
R19	1.5K-½ W	629A531H36	1
R69	82K-½ W	629A531H78	1
R21-R34-R38-R41-R68-R72	10K-½ W	629A531H56	6
R22-R23-R24-R36-R65-R58	2.7K-½ W	629A531H42	6
R53 R60	1K-½ W	629A531H32	1
R25-R27	68K-½ W	629A531H76	2
R26-R28	39K-½ W	629A531H70	2
R29-R46-R51	470Ω-½ W	629A531H24	3
R30-R61	2K-½ W	629A531H39	2
R31-R36	5.6K-½ W	629A531H50	2
R55-R57-R70	20K-½ W	629A531H63	3
R37	100K-½ W	629A531H80	1
R42	75K-½ W	629A531H53	1
R44	22K-½ W	629A531H64	1
R49	56Ω-½ W	629A531H02	1
R59	27K-½ W	629A531H66	1
R62	3.3K-½ W	629A531H44	1
R64	3K-½ W	629A531H43	1
R66	6.2K-½ W	629A531H51	1
R67	6.8K-½ W	629A531H52	1
R32-R35-R43-R48-R54-R71-R73-R20	4.7K-½ W	629A531H48	8
R81	330Ω 1/2 W	629A531H20	1

SCHEMATIC SYMBOL	ENGINEERING REFERENCE	STYLE	REQ.
D1 TO D27	DIODE - 82N9	837A692H04	27
D28 TO D30-D39 TO D47-D49 TO D62-D64 TO D59-D62-D63-D67-D68-D70-D71-D73 TO D80-D82-D84 TO D88-D90	DIODE - IN4385	184A855H14	43
D31 TO D36-D89	DIODE - IN3283	837A692H02	7
D37-D38-D81	DIODE - IN3283	837A692H02	3
D53	DIODE - IN4818	188A342H06	1
C1 TO C3	CAPACITOR 2 MFD	606B340H06	3
C4	CAPACITOR 2 MFD	606B340H01	1
C5-C9	CAPACITOR .68 MFD	764A278H18	2
C6 TO C8	CAPACITOR .05 MFD	187A624H08	3
C10	CAPACITOR .22 MFD	188A669H12	1
C11	CAPACITOR .27 MFD	188A669H06	1
C12	CAPACITOR 2 MFD	764A278H13	1
C13 TO C15	CAPACITOR .25 MFD	187A624H02	3
C16	CAPACITOR 1.5 MFD	187A508H13	1
C17	CAPACITOR .04 MFD	188A105H03	1
TH1	THERMISTOR 10K	185A211H04	1
TH2	THERMISTOR 1K	185A211H02	1
Q2-Q8-Q10-Q12-Q13-Q15-Q17	TRANSISTOR 2N697	184A638H18	7
Q11-Q14-Q18	TRANSISTOR 2N1132	184A638H20	3
Q3-Q4	TRANSISTOR 2N336	184A638H08	2
Q5-Q9	TRANSISTOR 2N3645	849A441H01	2
Q6-Q7-Q1-Q16	TRANSISTOR 2N3417	848A851H02	4
TD1-TD2	TUNNEL DIODE IN3713	877A809H01	2
Z1	ZENER DIODE 1N2984B	762A631H01	1
Z2	ZENER DIODE 1N759A	837A693H01	1
Z3	ZENER DIODE 1N3688A	862A288H01	1
Z5-Z6	ZENER DIODE 1N3035B	188A302H08	2

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e SDG-1 Relay with Parts List.

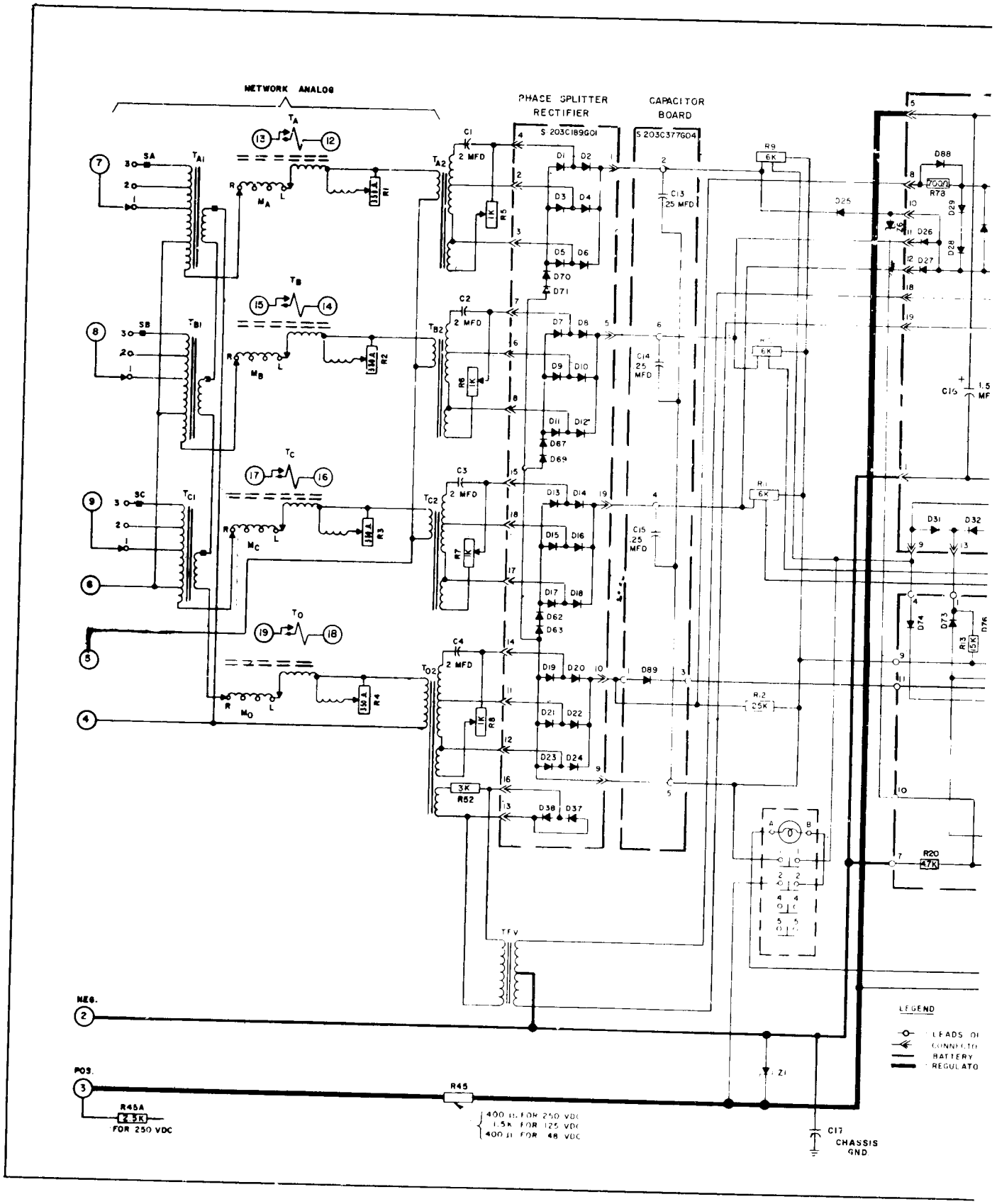
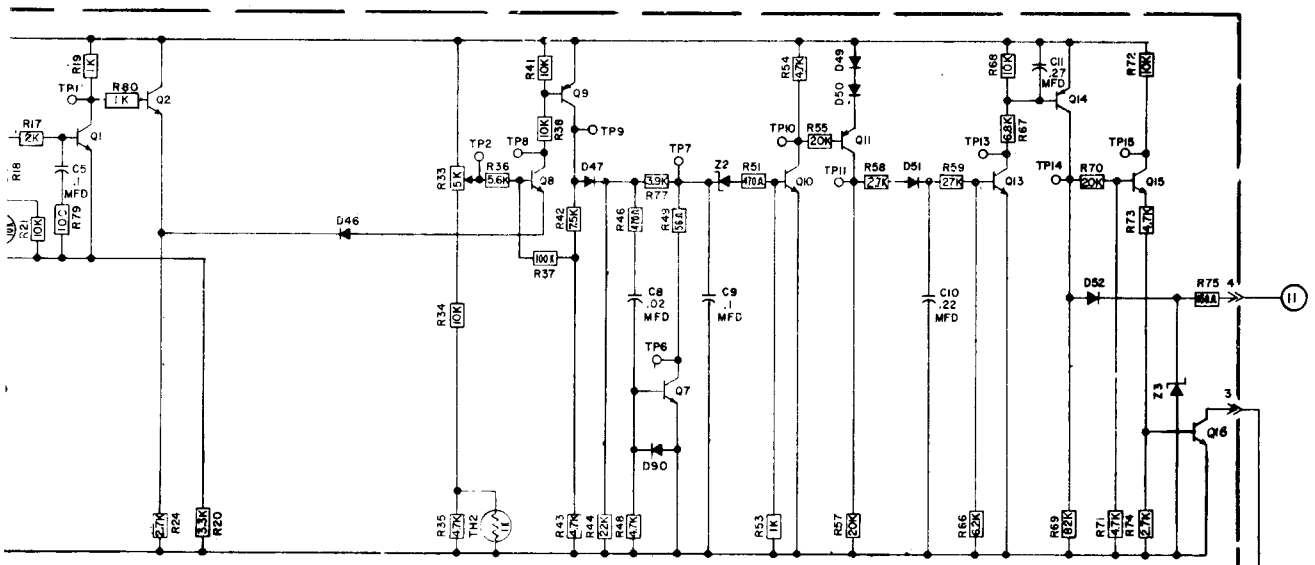


Fig. 11 Detailed Internal Sche



S-5506D36G01

MAGNITUDE COMPARATOR

SCHEMATIC SYMBOL	ENGINEERING REFERENCE	STYLE	REQ.
R1 TO R4	POTENTIOMETER-350Ω-12½W	836A635H01	4
R5 TO R8	POTENTIOMETER-1K-12½W	836A635H03	4
R18	POTENTIOMETER-100K-¼ W	629A430H04	1
R33	POTENTIOMETER-5K-¼ W	629A430H07	1
	RESISTORS		
R9 TO R12	6K-12 W	849A379H02	4
R45 (48 & 250 V.D.C.)	400Ω-25 W	184A856H14	1
R45 (125 V.D.C.)	1.5K-25 W	184A856H11	1
R45A (250 V.D.C.)	2.5K-40 W	1336127	1
R79	100Ω 1/2W	629A531H08	1
R75	150Ω-3 W	762A679H01	1
R78	3K-3 W	184A636H05	1
R17	2K-½ W	629A531H39	1
R20	3.3K ½ W	629A531H44	1
R35-R48-R54-R71-R73-R43	4.7K-½ W	629A531H48	6
R21-R34-R38-R41-R68-R72	10 K-½ W	629A531H56	6
R74-R24-R58	2.7K-½ W	629A531H42	3
R19-R53-R80	1K-½ W	629A531H32	3
R51-R46	470Ω-½ W	629A531H24	2
R77	3.9K ½ W	629A531H46	1
R36	5.6K-½ W	629A531H50	1
R70-R55-R57	20K-½ W	629A531H63	3
R37	100K-½ W	629A531H80	1
R42	75K-½ W	629A531H53	1
R44	22K-½ W	629A531H64	1
R49	56Ω-½ W	629A531H02	1
R59	27K ½ W	629A531H66	1
R66	6.2K-½ W	629A531H51	1
R67	6.8K-½ W	629A531H52	1
R69	82K-½ W	629A531H78	1

SCHEMATIC SYMBOL	ENGINEERING REFERENCE		STYLE	REQ.
D1 TO D27	DIODE - B2N9		837A692H04	27
D28 TO D30-D46-D47-D49 TO D52-D62 D63-D67-D69-D70-D71 D90	DIODE - IN4385		184A855H14	17
C1 TO C3	CAPACITOR	2 MFD	606B340H06	3
C4	CAPACITOR	2 MFD	606B340H01	1
C5-C9	CAPACITOR	.1 MFD	187A624H01	2
C8	CAPACITOR	.02 MFD	187A624H09	1
C10	CAPACITOR	.22 MFD	188A669H12	1
C11	CAPACITOR	.27 MFD	188A669H05	1
C17	CAPACITOR	.04 MFD	186A105H03	1
C16	CAPACITOR	1.5 MFD	187A508H18	1
TH1	THERMISTOR	10 K	185A211H04	1
TH2	THERMISTOR	1 K	185A211H02	1
Q2-Q8-Q10-Q13-Q15	TRANSISTOR	2N697	184A638H18	5
Q11-Q14	TRANSISTOR	2N1132	184A638H20	2
Q9	TRANSISTOR	2N3645	849A441H01	1
Q7-Q1-Q16	TRANSISTOR	2N3417	848A851H02	3
Z1	ZENER DIODE	1N2984B	762A631H01	1
Z2	ZENER DIODE	1N759A	837A693H01	1
Z3	ZENER DIODE	1N3688A	862A288H01	1

ALL BOARDS.
RMINALS
ATIVE.
OSITIVE

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c of the SDG-4 Relay with Parts List

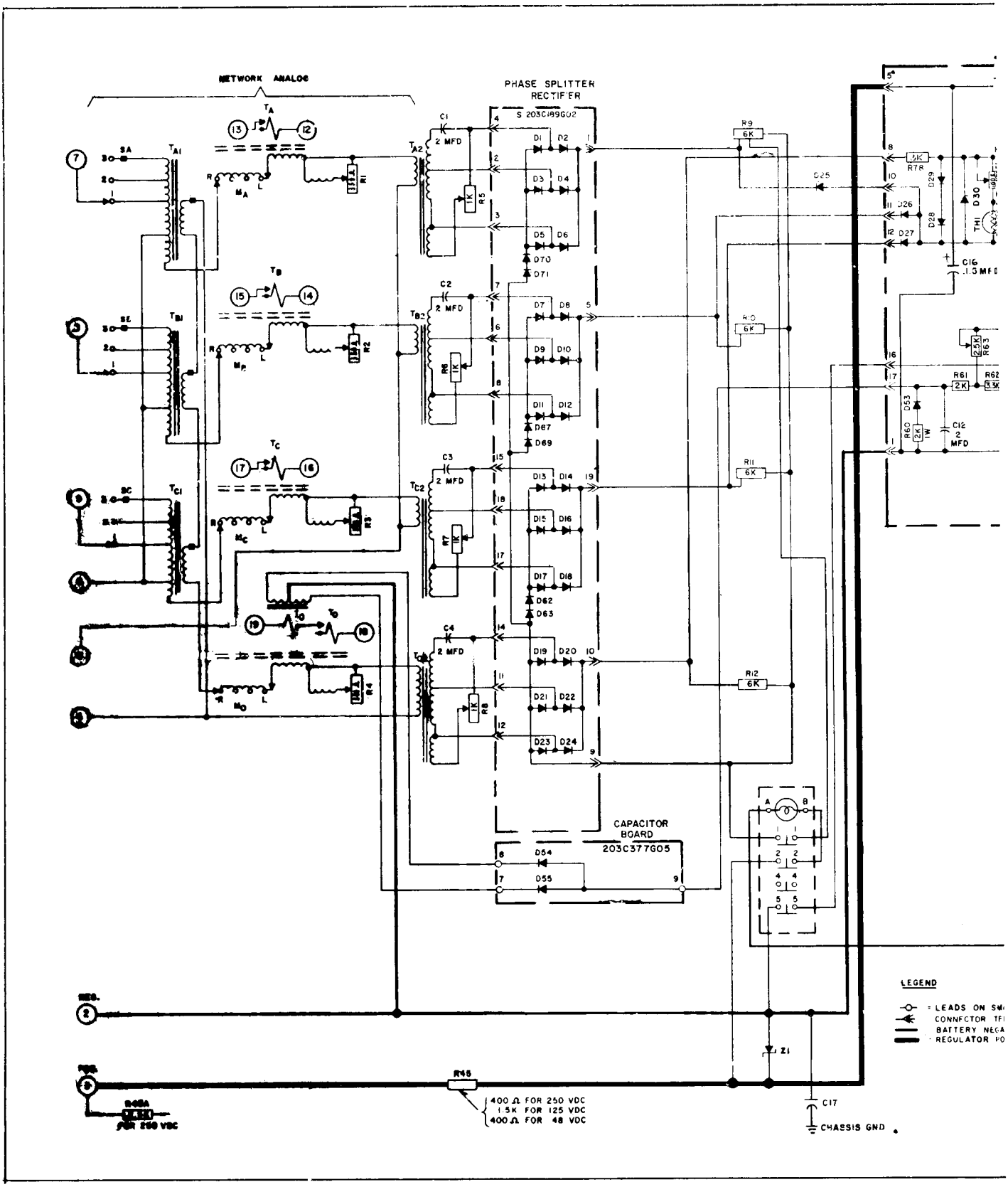
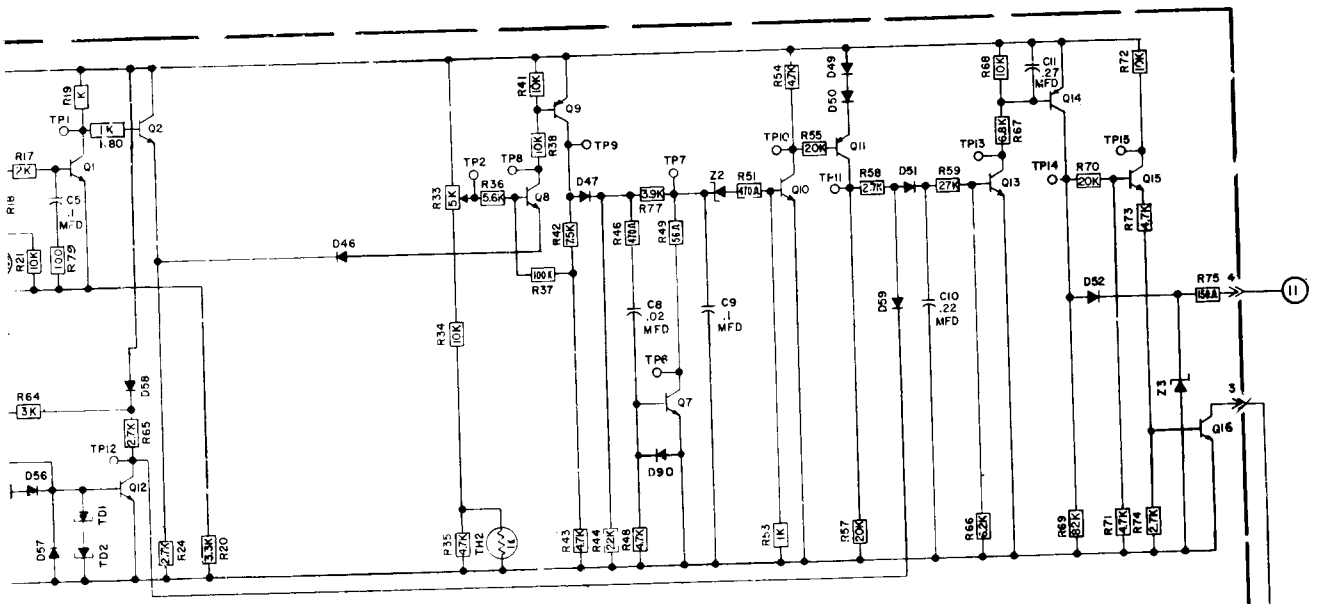


Fig. 12 Detailed Internal Schematic



S-5506D35G01

MAGNITUDE COMPARATOR

SCHEMATIC SYMBOL	ENGINEERING REFERENCE	STYLE	REQ.
R1 TO R4	POTENTIOMETER-350Ω-12½W	836A635H01	4
R5 TO R8	POTENTIOMETER-1K-12½W	836A635H03	4
R18	POTENTIOMETER-100K-¼ W	629A430H04	1
R33	POTENTIOMETER-5K-¼ W	629A430H07	1
R63	POTENTIOMETER-2.5K-¼ W	629A430H03	1
	RESISTORS		
R9 TO R12	6K-12 W	849A379H02	4
R79	100Ω 1/2 W	629A531H08	1
R45 (48 & 250 V.D.C.)	400Ω-25 W	184A856H14	1
R45 (125 V.D.C.)	1.5K-25 W	184A856H11	1
R45A (250 V.D.C.)	2.5K-40 W	1336127	1
R60	2K-1 W	187A643H34	1
R75	150Ω-3 W	762A679H01	1
R78	3K-3 W	184A636H05	1
R17	2K-½ W	629A531H39	1
R35-R48-R54-R71-R73-R43	4.7K-½ W	629A531H48	6
R21-R34-R38-R41-R68-R72	10 K-½ W	629A531H56	6
R65-R74-R24-R6[illegible]	2.7K-½ W	629A531H42	4
R19-R53-R80	1K-½ W	629A531H32	3
R77	3.9K-½ W	629A531H46	1
R46-R51	470Ω-½ W	629A531H24	2
R61	2K-½ W	629A531H39	1
R36	5.6K-½ W	629A531H50	1
R55-R57-R70	20K-½ W	629A531H63	3
R37	100K-½ W	629A531H80	1
R42	7.5K-½ W	629A531H53	1
R44	22K-½ W	629A531H64	1
R49	56Ω-½ W	629A531H02	1
R59	27K-½ W	629A531H66	1
R62 R20	3.3K ½ W	629A531H44	2
R64	3K ½ W	629A531H43	1
R66	6.2K-½ W	629A531H51	1
R67	6.8K-½ W	629A531H52	1
R69	82K-½ W	629A531H78	1

SCHEMATIC SYMBOL	ENGINEERING REFERENCE	STYLE	REQ.
D1 TO D27	DIODE - 82N9	837A692H04	27
D28 TO D30-D46 D47 D49 TO D52-D54 TO D59-D62-D63-D67-D69-D70-D71 D90	DIODE - 1N4385	184A858H14	22
D53	DIODE - CER 69	188A342H06	1
C1 TO C3	CAPACITOR 2 MFD	6068340H06	3
C4	CAPACITOR 2 MFD	6068340H01	1
C5-C9	CAPACITOR .1 MFD	187A624H01	5
C8	CAPACITOR .02 MFD	187A624H09	1
C10	CAPACITOR .22 MFD	188A669H12	1
C11	CAPACITOR .27 MFD	188A669H05	1
C12	CAPACITOR 2 MFD	764A278H13	1
C16	CAPACITOR 1.5 MFD	187A508H18	1
C17	CAPACITOR .04 MFD	186A105H03	1
TH1	THERMISTOR 10 K	185A211H04	1
TH2	THERMISTOR 1 K	185A211H02	1
Q2-Q8-Q10 Q12-Q13-Q15	TRANSISTOR 2N697	184A638H18	6
Q11-Q14	TRANSISTOR 2N1132	184A638H20	2
Q9	TRANSISTOR 2N3645	849A441H01	1
Q1-Q7-Q16	TRANSISTOR 2N3417	648A851H02	3
TD1-TD2	TUNNEL DIODE 1N3713	877A809H01	2
Z1	ZENER DIODE 1N2984B	762A631H01	1
Z2	ZENER DIODE 1N759A	837A693H01	1
Z3	ZENER DIODE 1N3688A	862A288H01	1

ALL BOARDS.
RMINALS
TIVE
SITIVE

5508D61

of the SDG-3 Relay with Parts List.

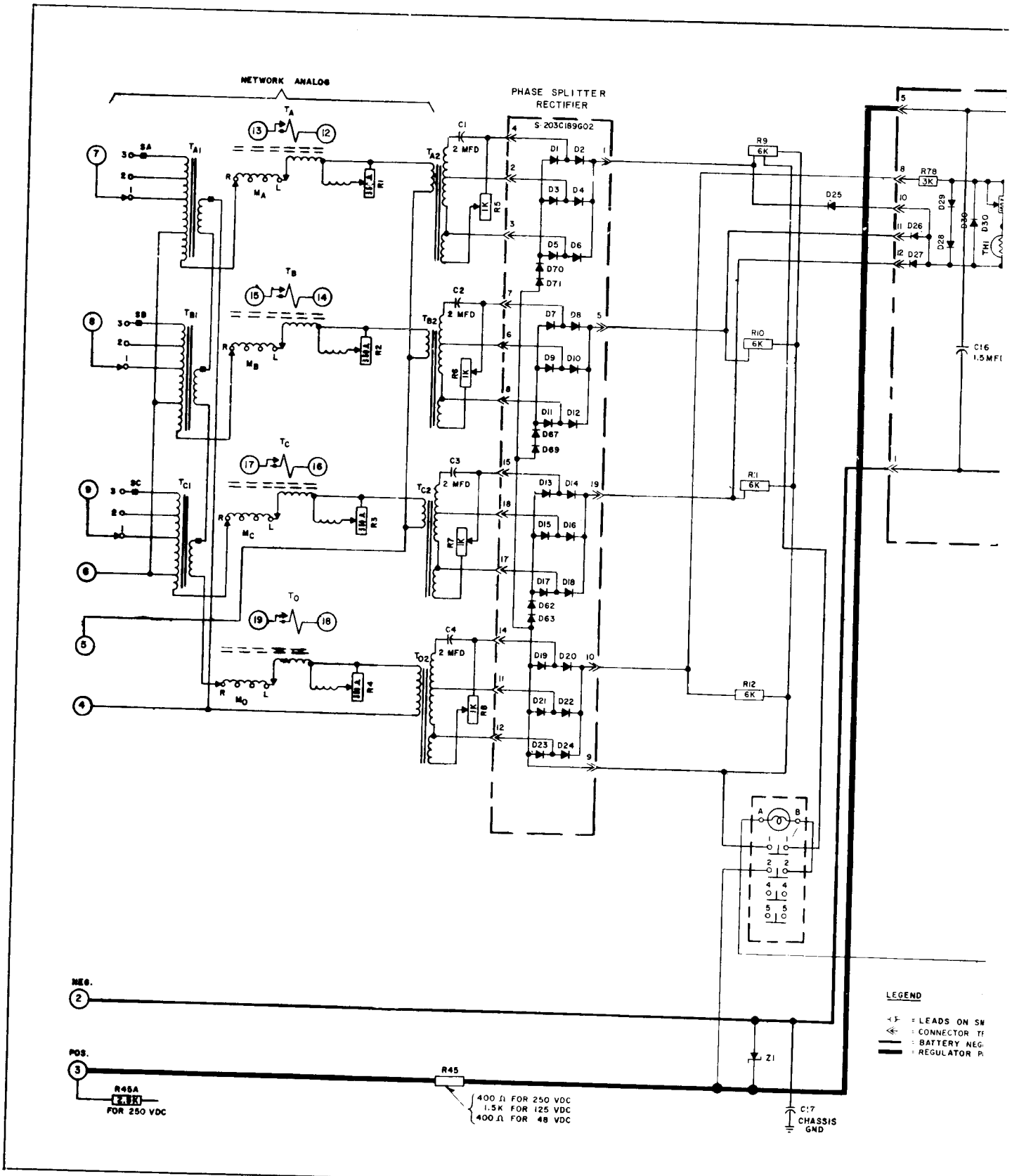


Fig. 13 Detailed Internal Schemati

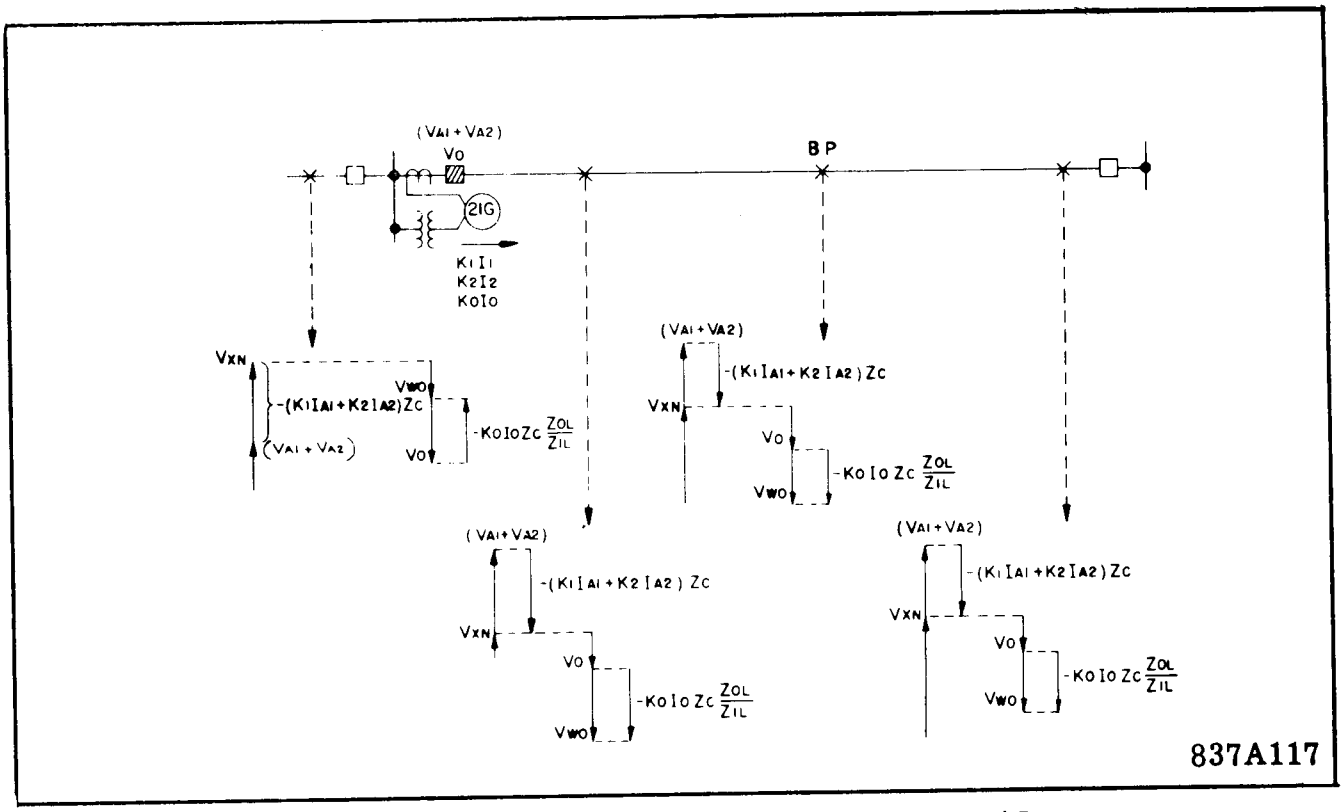


Fig. 18 Relay Voltages for A-to-Ground Faults at Selected Points.

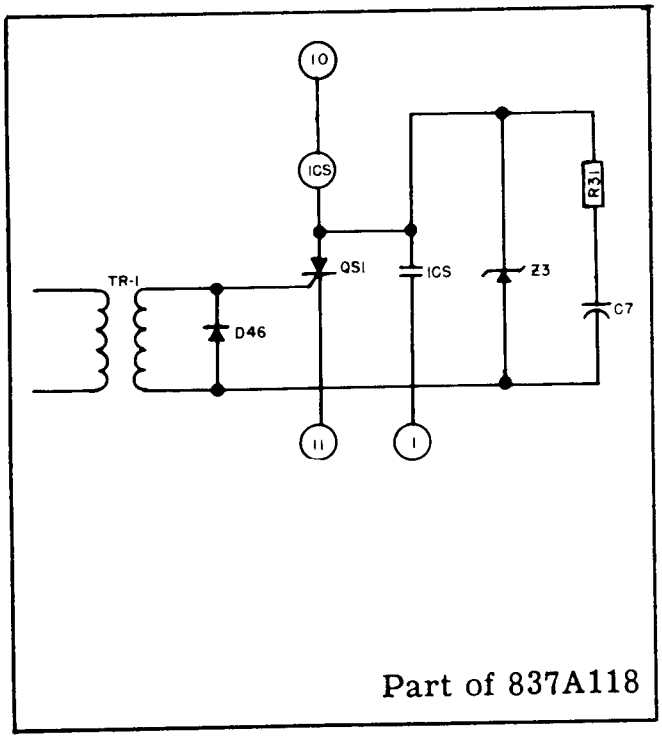


Fig. 19 Output Circuit for the SDG Relay.

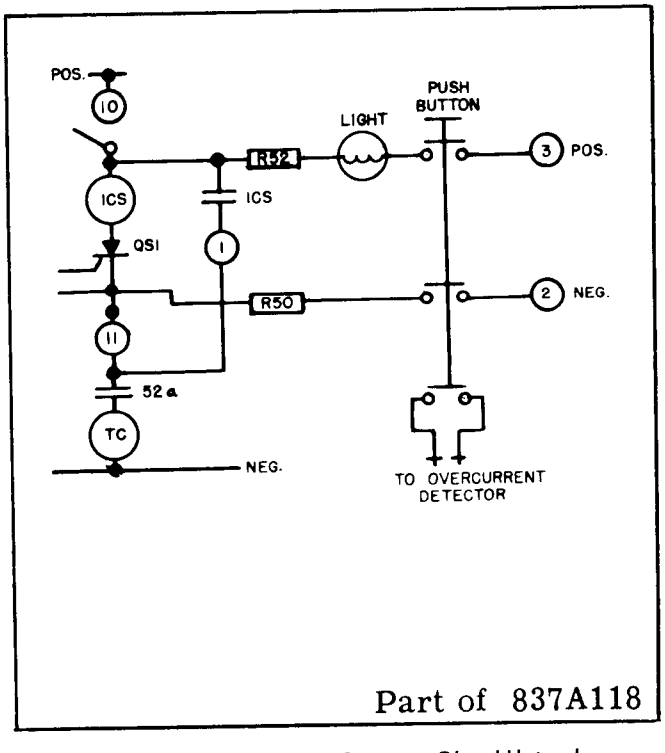


Fig. 20 Pushbutton "In Service Check" in the SDG Relay.

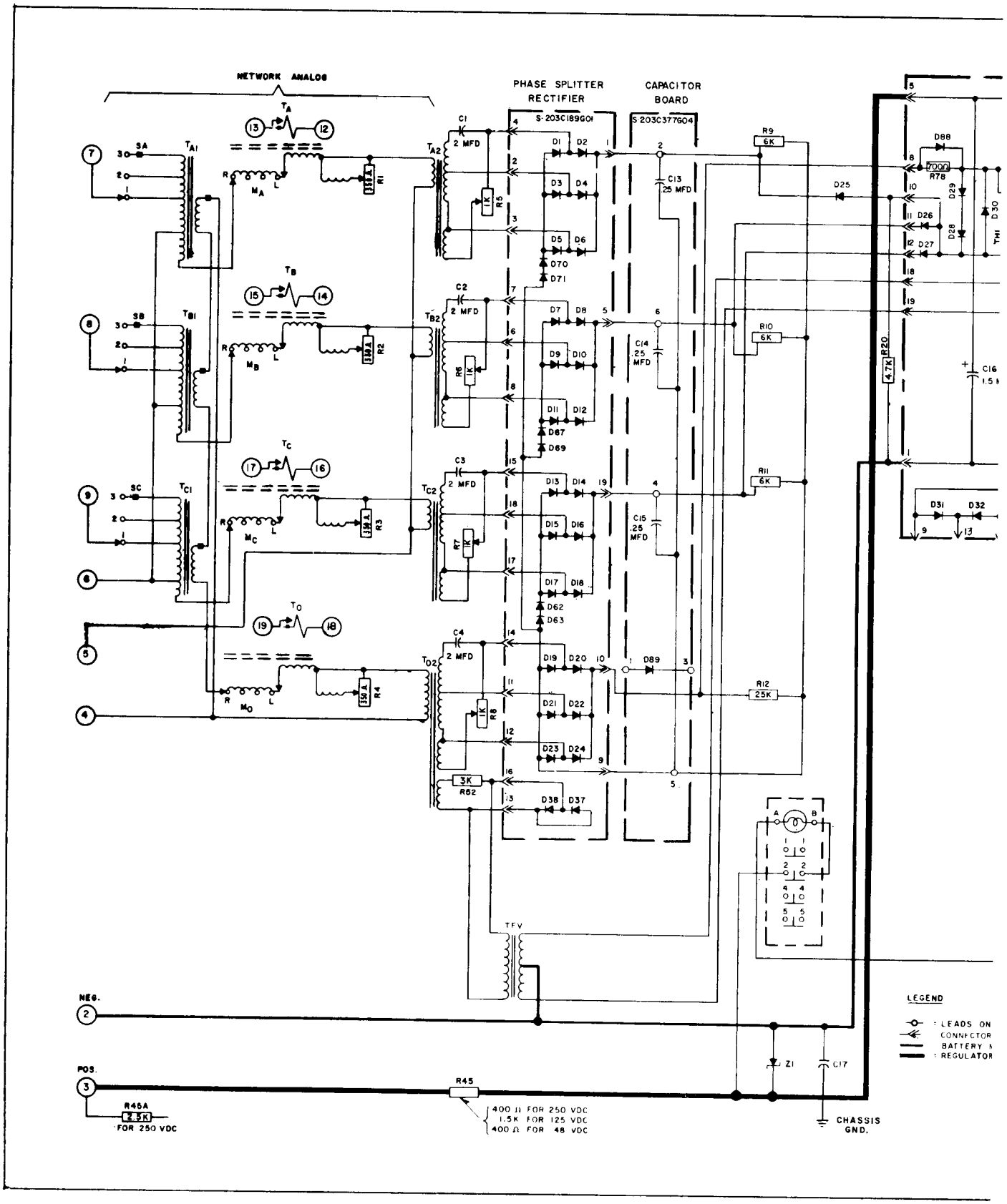
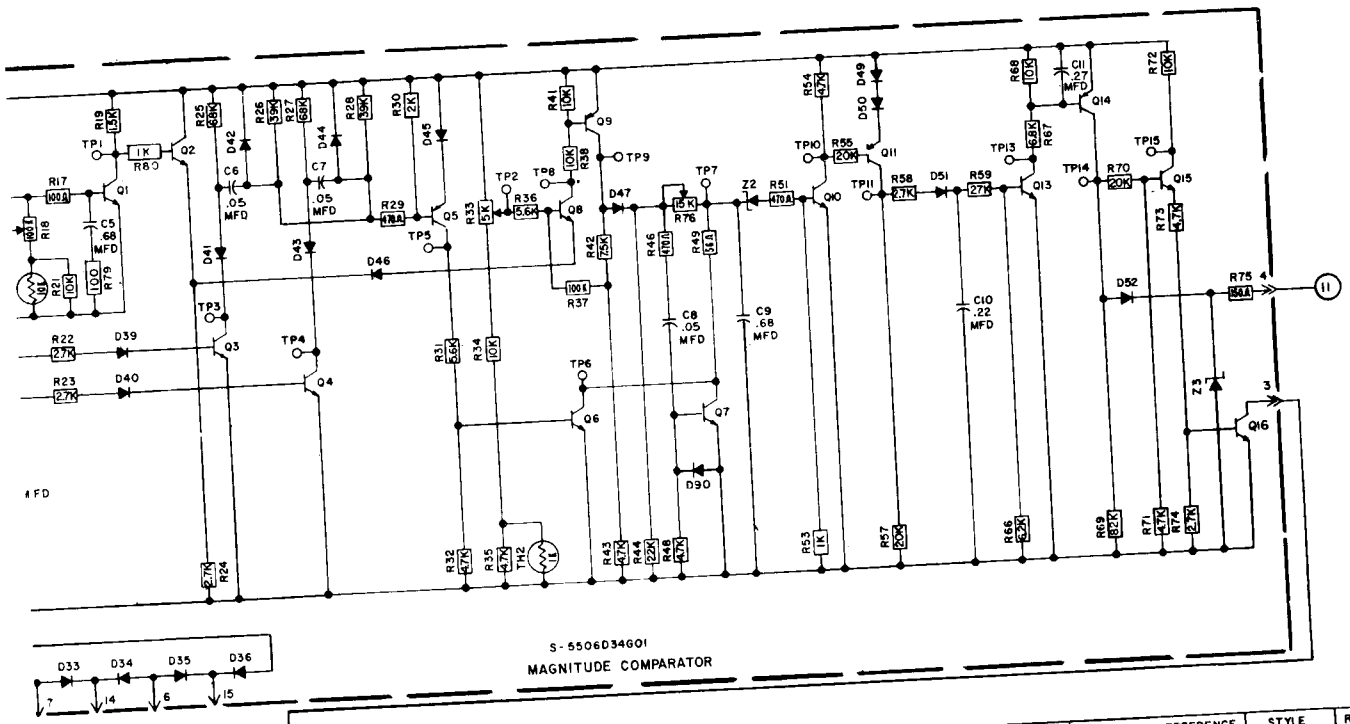


Fig. 14 Detailed Internal Schemati



S-5506D34G01

MAGNITUDE COMPARATOR

SCHEMATIC SYMBOL	ENGINEERING REFERENCE	STYLE	REQ.
R1 TO R4	POTENTIOMETER-350Ω-12½W	836A635H01	4
R5 TO R8	POTENTIOMETER-1K-12½W	836A635H03	4
R18	POTENTIOMETER-100K-¼ W	629A430H04	1
R33	POTENTIOMETER-5K-¼ W	629A430H07	1
R76	POTENTIOMETER-15K-¼ W	629A430H08	1
	RESISTORS		
R9 TO R11	6K-12 W	849A379H02	3
R12	25K-10 W	184A856H15	1
R45 (48 & 250 V.D.C.)	400Ω-25 W	184A856H14	1
R45 (125 V.D.C.)	1.5K-25 W	184A856H11	1
R45A (250 V.D.C.)	2.5K-40 W	1336127	1
R52	2K-10 W	184A856H19	1
R75	150Ω-3 W	762A679H01	1
R78	700Ω-3 W	763A127H28	1
R17 R79	100Ω-½ W	629A531H08	1
R19	1.5K-½ W	629A531H36	1
R69	82K-½ W	629A531H78	1
R21-R34 R38-R41-R68-R72	10K-½ W	629A531H56	6
R22-R23-R24-R74-R58	2.7K-½ W	629A531H42	5
R53 R80	1K-½ W	629A531H32	1
R25-R27	68K-½ W	629A531H76	2
R26-R28	39K-½ W	629A531H70	2
R29-R46-R51	470Ω-½ W	629A531H24	3
R30	2K-½ W	629A531H39	
R31-R36	5.6K-½ W	629A531H50	2
R55-R57-R70	20K-½ W	629A531H63	3
R37	100K-½ W	629A531H80	1
R42	7.5K-½ W	629A531H53	1
R44	22K-½ W	629A531H64	1
R49	56Ω-½ W	629A531H02	1
R59	27K-½ W	629A531H66	1
R66	6.2K-½ W	629A531H51	1
R67	6.8K-½ W	629A531H52	1
R20-R32-R35-R43-R54 R71-R73	4.7K ½ W	629A531H48	7

SCHEMATIC SYMBOL	ENGINEERING REFERENCE	STYLE	REQ.
D1 TO D27	DIODE - B2N9	837A692H04	27
D28 TO D30-D39 TO D47-D49 TO D52-D59-D62-D63-D67-D69-D70-D71-D90	DIODE - 1N4385	184A855H14	23
D88	DIODE - 1N3283	837A692H02	7
D31 TO D36-D89	DIODE - 1N3283	837A692H02	3
D37-D38-D81			
C1 TO C3	CAPACITOR 2 MFD	606B340H06	3
C4	CAPACITOR 2 MFD	606B340H01	1
C5-C9	CAPACITOR .68 MFD	764A278H16	2
C6 TO C8	CAPACITOR .05 MFD	187A624H08	3
C10	CAPACITOR .22 MFD	188A669H12	1
C11	CAPACITOR .27 MFD	188A669H05	1
C16	CAPACITOR 1.5 MFD	187A508H18	1
C13 TO C15	CAPACITOR .25 MFD	187A624H02	3
C17	CAPACITOR .04 MFD	186A105H03	1
TH1	THERMISTOR 10 K	185A211H04	1
TH2	THERMISTOR 1 K	185A211H02	1
Q2-Q8-Q10-Q13	TRANSISTOR 2N697	184A638H18	5
Q15	TRANSISTOR 2N1132	184A638H20	2
Q11-Q14	TRANSISTOR 2N336	184A638H06	2
Q3-Q4	TRANSISTOR 2N3645	849A441H01	2
Q5-Q9	TRANSISTOR 2N3417	848A851H02	4
Q6-Q7-Q1-Q16			
Z1	ZENER DIODE 1N2984B	762A631H01	1
Z2	ZENER DIODE 1N759A	837A693H07	1
Z3	ZENER DIODE 1N3688A	862A288H01	1

SMALL BOARDS
TERMINALS
EGATIVE
POSITIVE

6280D38

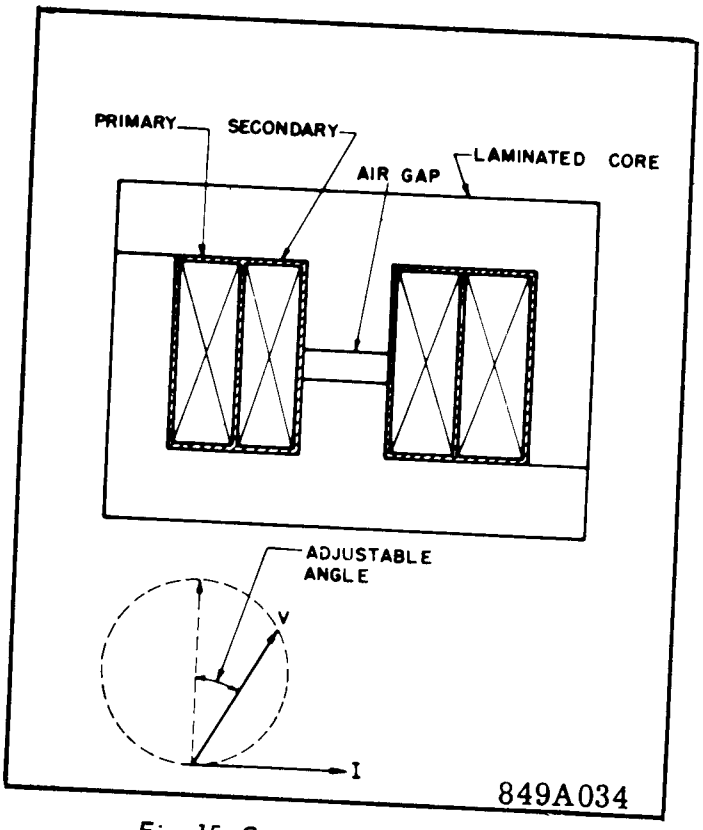


Fig. 15 Compensator Construction

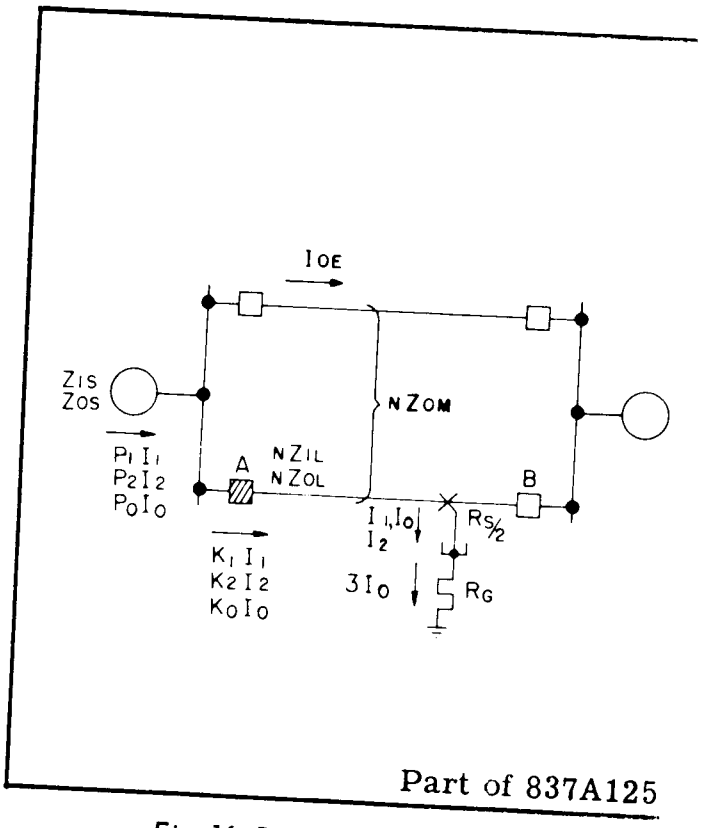
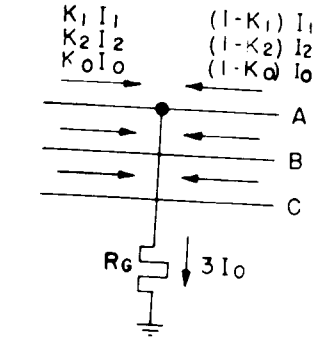
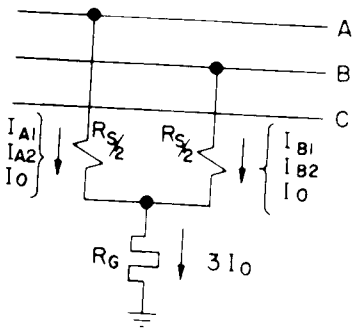


Fig. 16 Definition of Terms



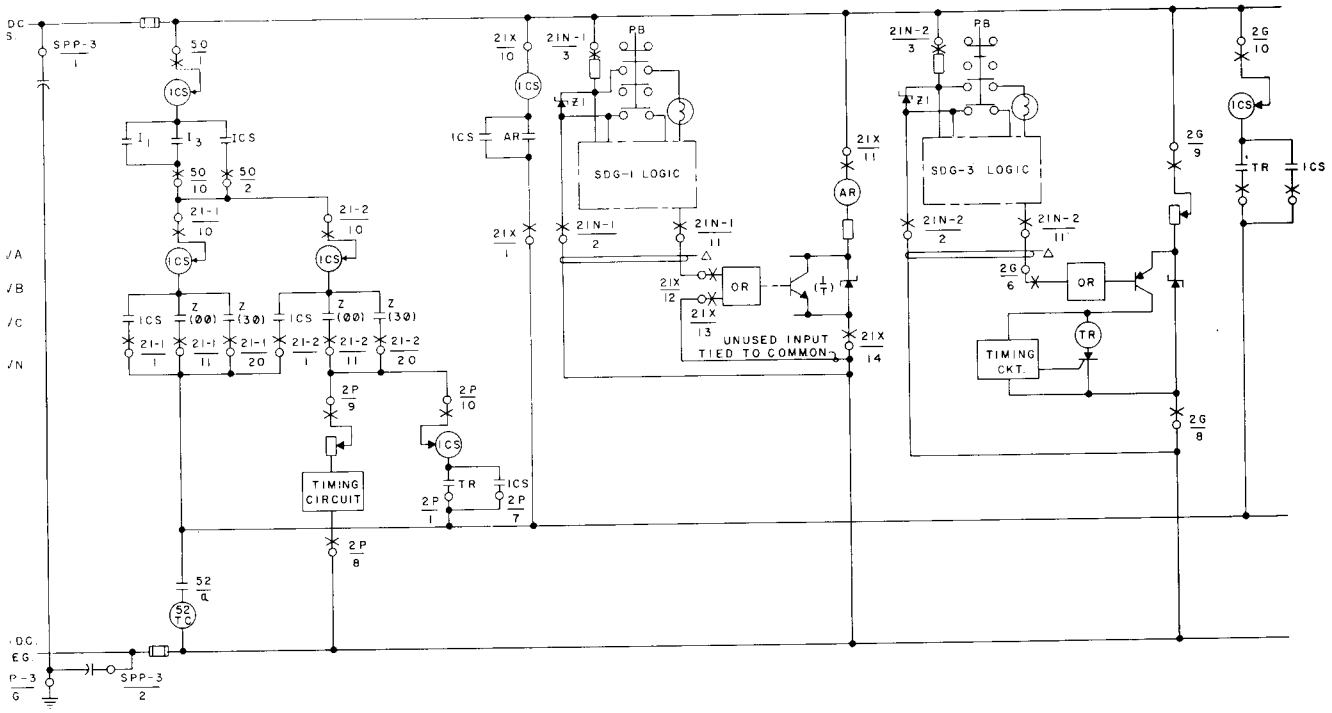
A) PHASE A - GROUND



B) PHASE AB - GROUND

Part of 837A125

Fig. 17 Fault Resistance

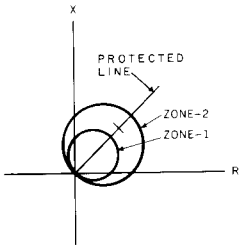


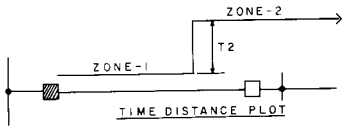
△-SHIELDED TWISTED PAIR WITH SHIELD GROUNDED AT BOTH ENDS REQUIRED ONLY WHERE SURGE EXPOSURE EXISTS BETWEEN RELAYS

†-THIS SPP NOT REQUIRED IF INSTRUMENT TRANSFORMER NEUTRAL GROUND IS MADE IN THIS PANEL

INTERNAL SCHEMATIC		
DEVICE NO	DEVICE	DWG. NO
2P	TD-5 RELAY	187A293
21-1	KD-10 RELAY SHORT RANGE	3490A81
21-2	KD-10 RELAY MED & LONG RANGE	880A988
2G	TD-50 RELAY	763A930
21N-1	SDG-1 RELAY	670B237
21N-2	SDG-3 RELAY	670B239
21X	ARS RELAY	862A287
50	KC-2 RELAY	837A454
+ SPP-1	SURGE PROT. CAPACITOR	877A862
+ SPP-2	SURGE PROT. CAPACITOR	877A862
+ SPP-3	SURGE PROT. CAPACITOR	877A862

+3 SURGE PROTECTIVE CAPACITOR ASSEM. S#550D57G01 SHOULD BE USED WHEN SURGE VOLTAGE MAY EXCEED 2500 VOLTS PEAK.





SUB. 3
647F796

Phase & Distance Ground Relaying.

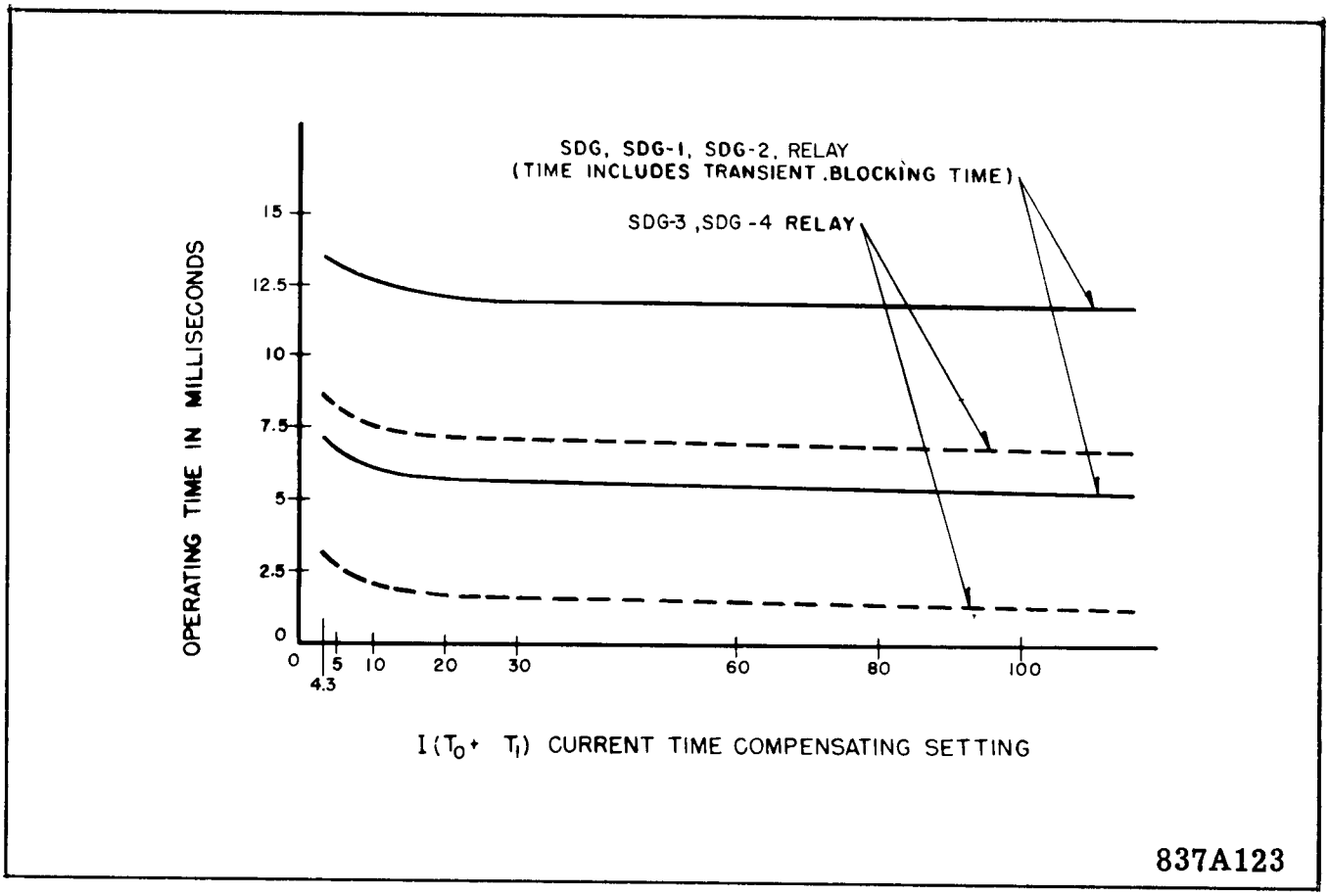


Fig. 21 Typical Operating Time Curves of the Type SDG-Line Relay.

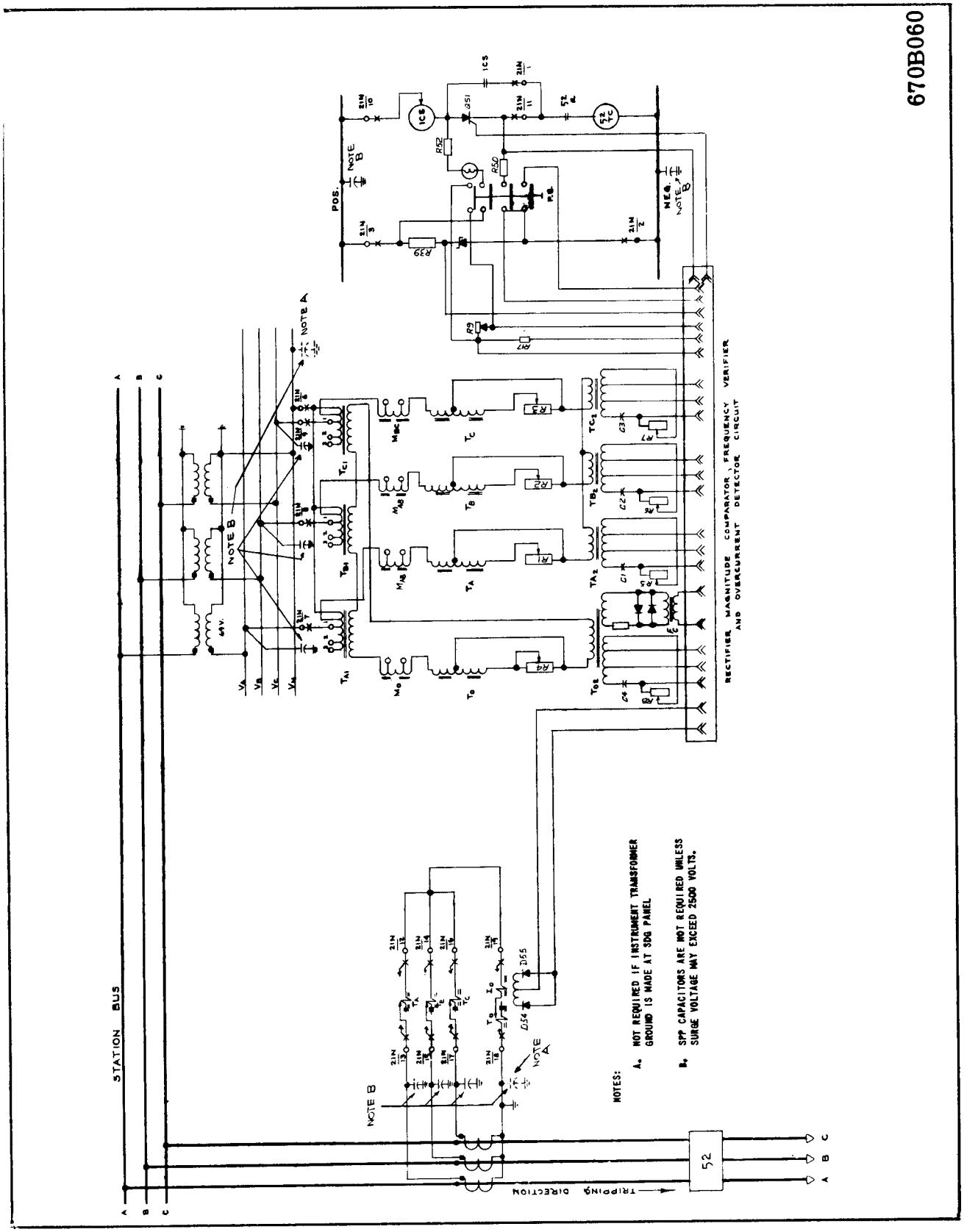


Fig. 22 External Connections for the SDG Relay.

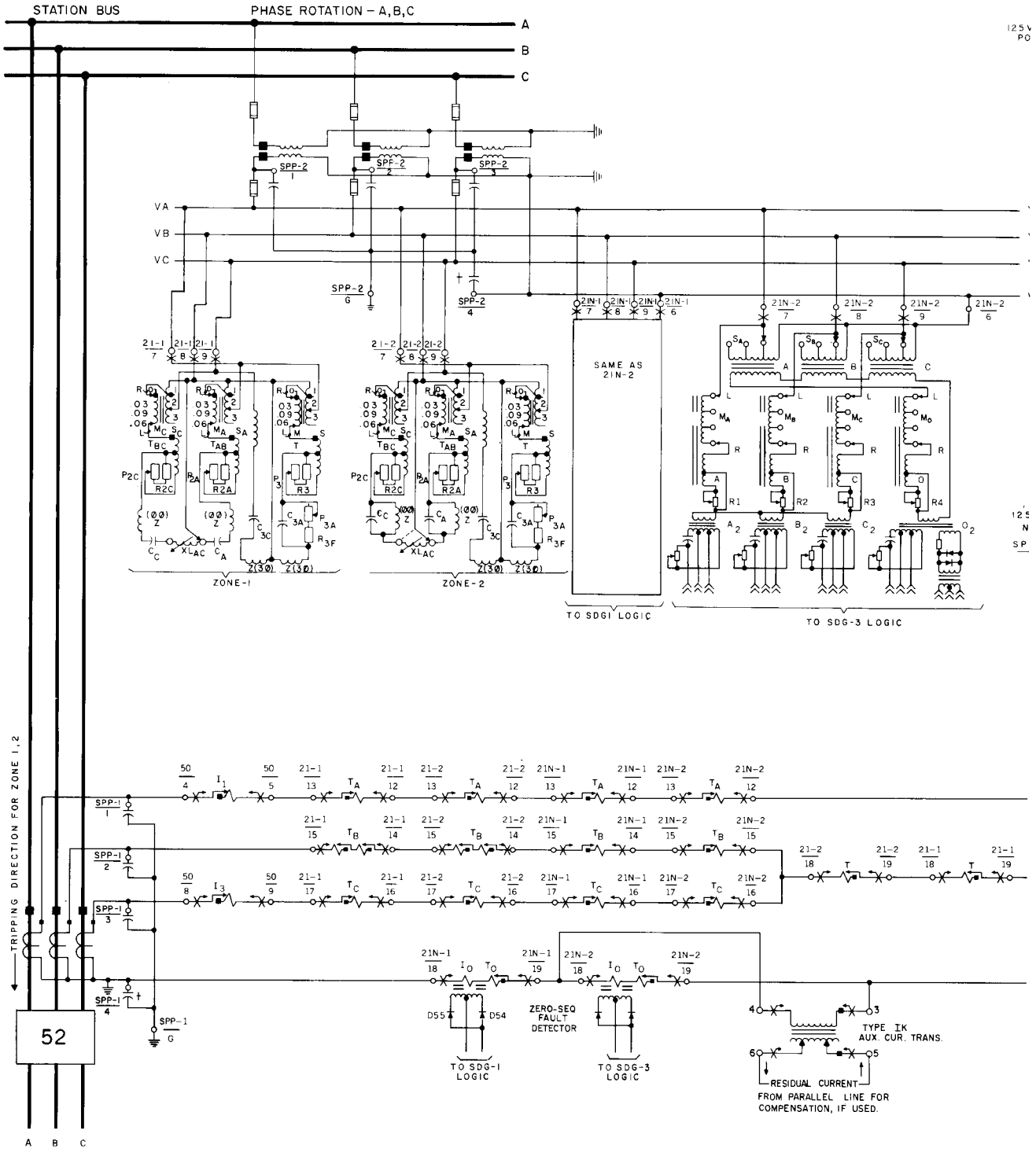


Fig. 22a Two Zone Distance

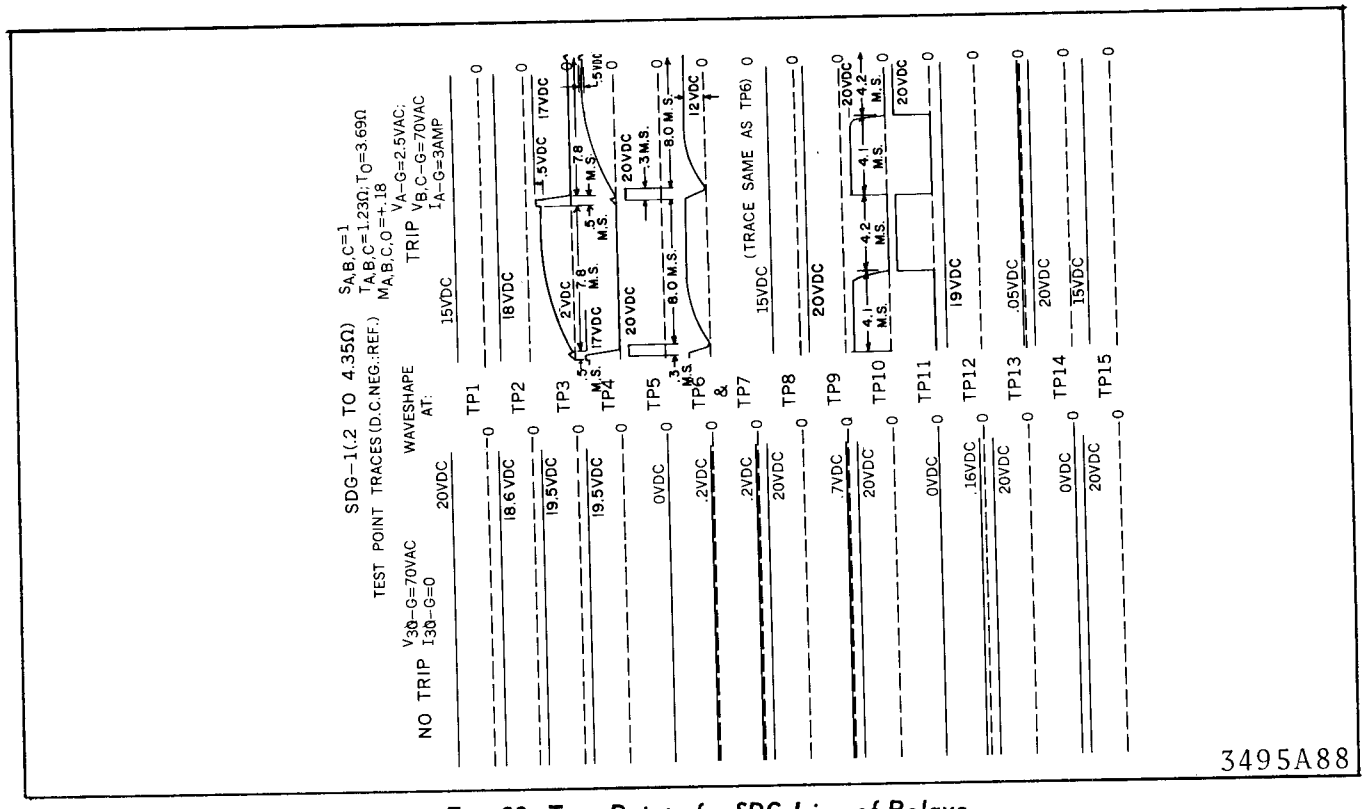
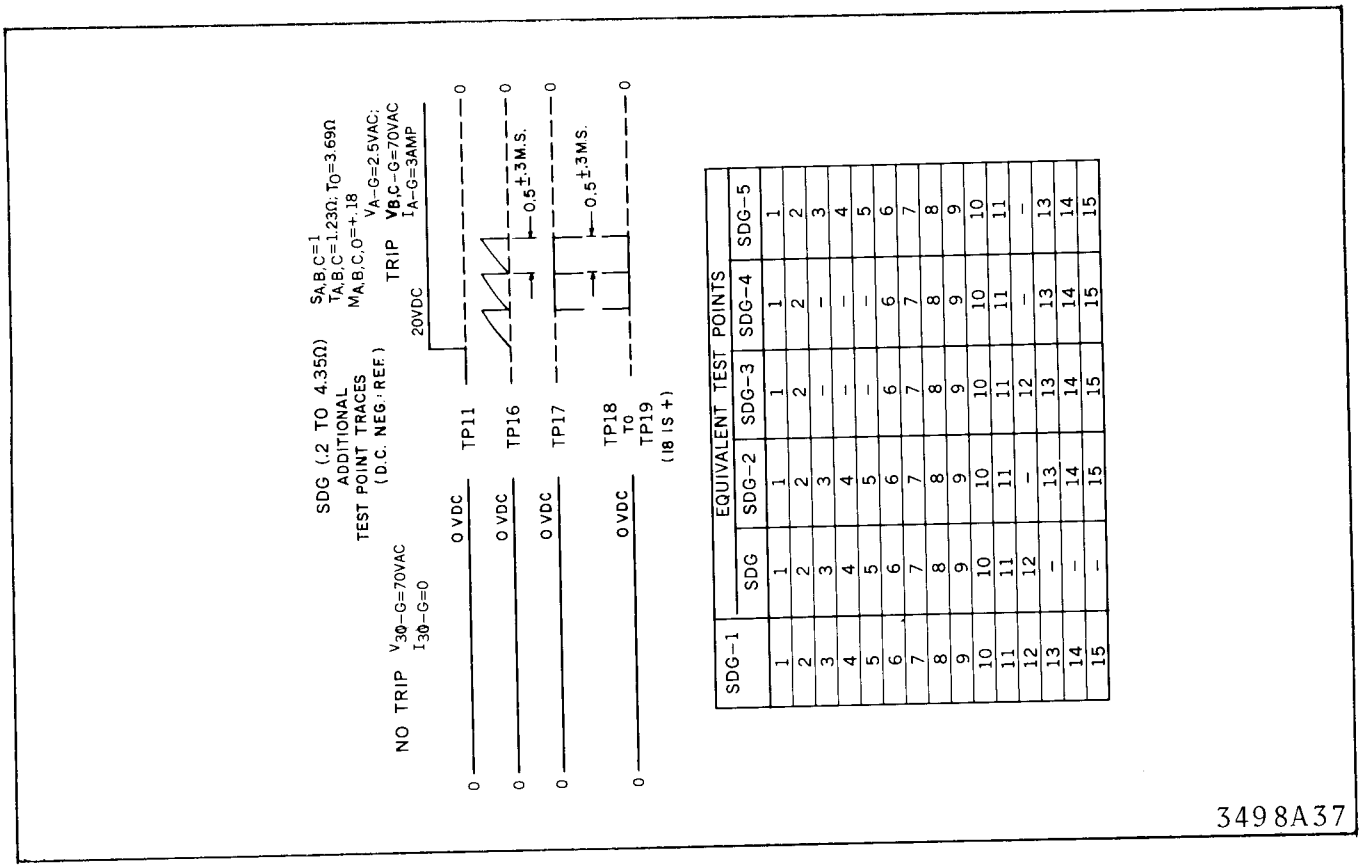
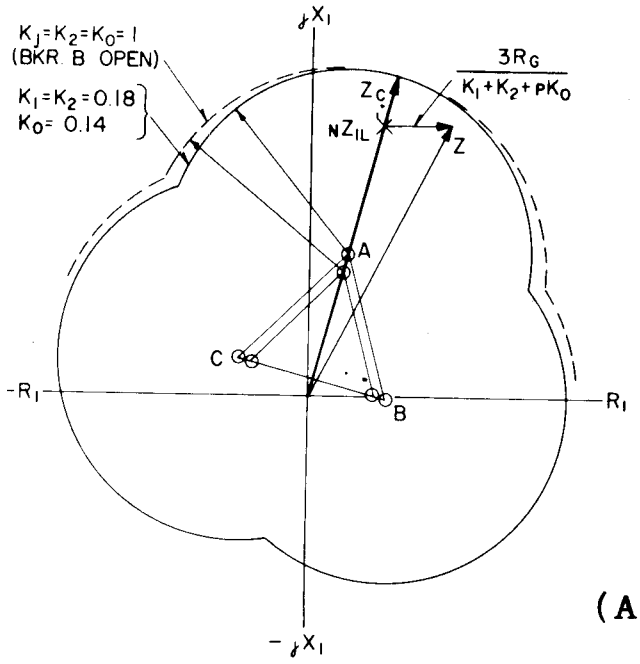


Fig. 23 Test Points for SDG Line of Relays



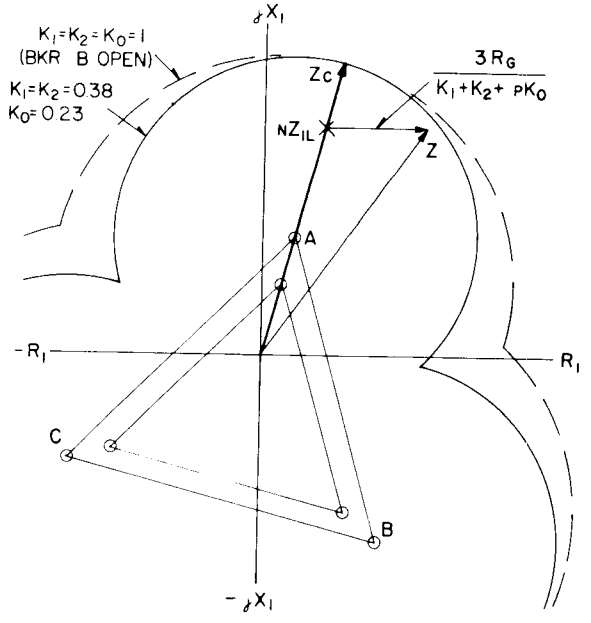
SDG-1	EQUIVALENT TEST POINTS				
	SDG	SDG-2	SDG-3	SDG-4	SDG-5
1	1	1	1	1	1
2	2	2	2	2	2
3	3	3	–	–	3
4	4	4	–	–	4
5	5	5	–	–	5
6	6	6	6	6	6
7	7	7	7	7	7
8	8	8	8	8	8
9	9	9	9	9	9
10	10	10	10	10	10
11	11	11	11	11	11
12	12	–	12	–	–
13	–	13	13	13	13
14	–	14	14	14	14
15	–	15	15	15	15

Fig. 23a SDG Test Point Traces.



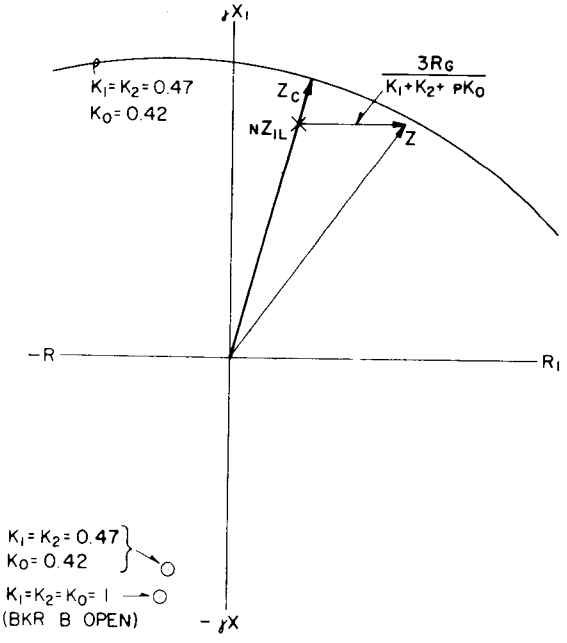
(A) 837A116

a) Long Line



(B) 837A114

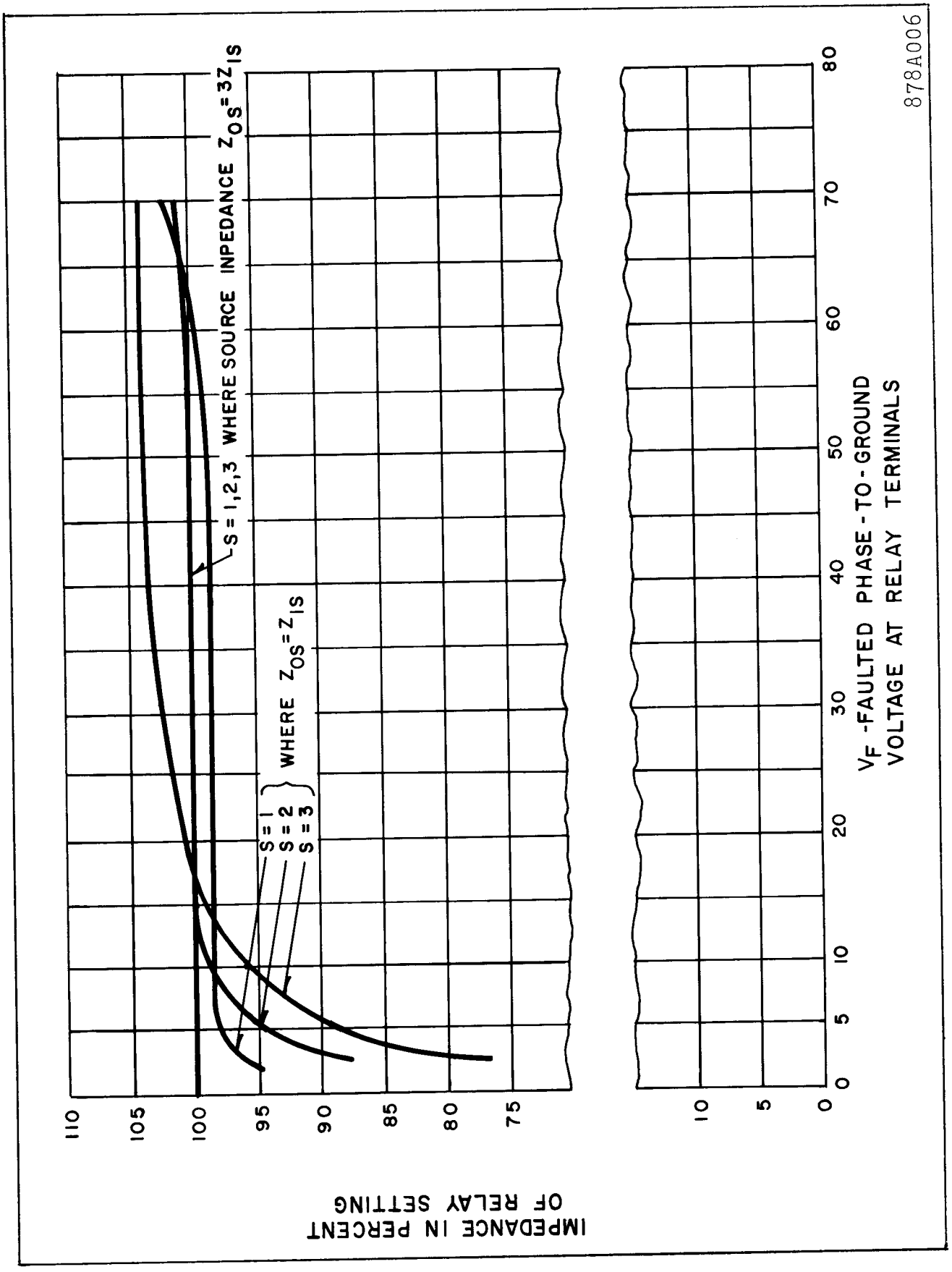
b) Medium-length Line



(C) 837A115

c) Short Line

Fig. 24 Impedance Circles for the SDG Line Relays.



✪ *Fig. 25 Impedance Curve for the SDG Line Relays.*

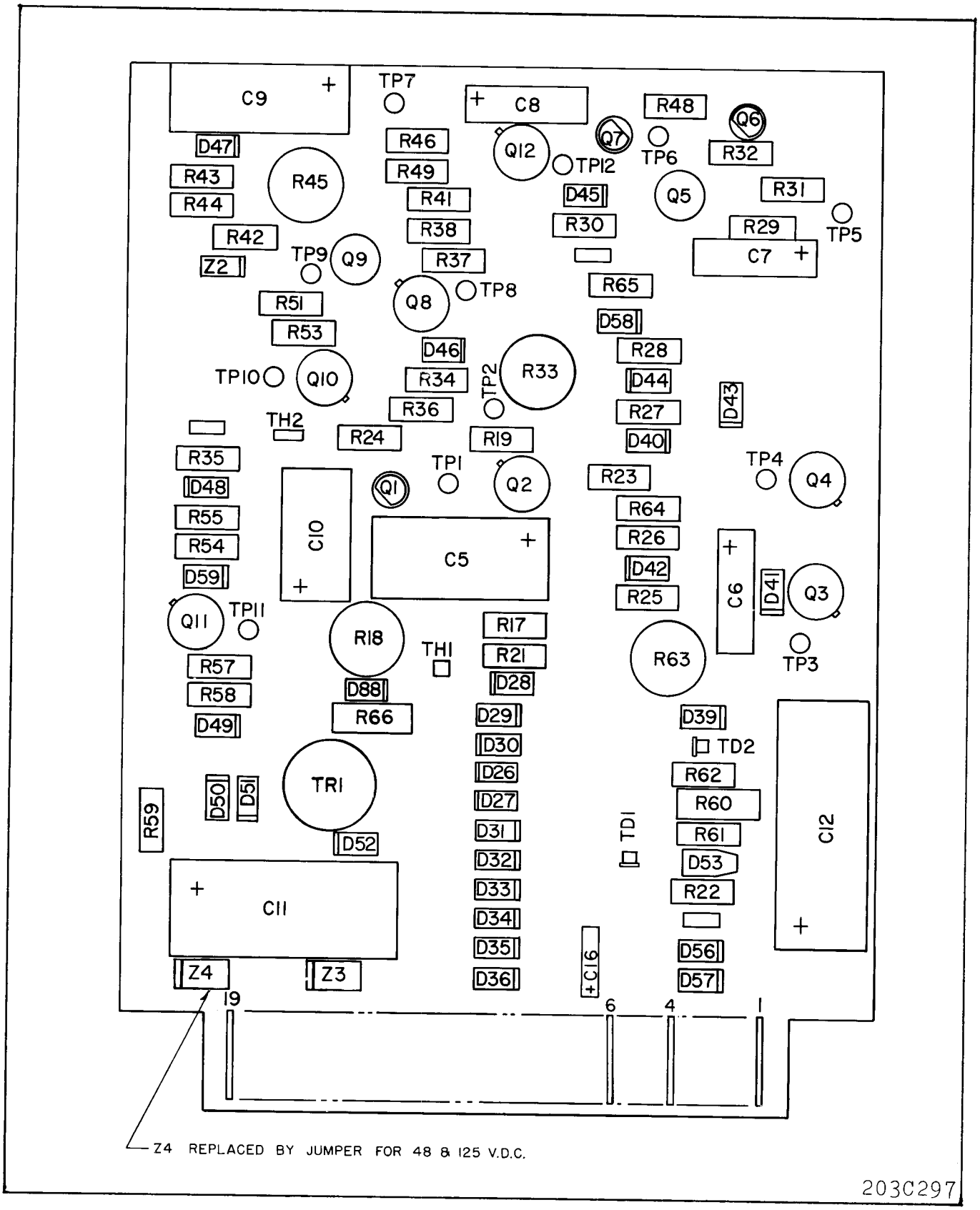
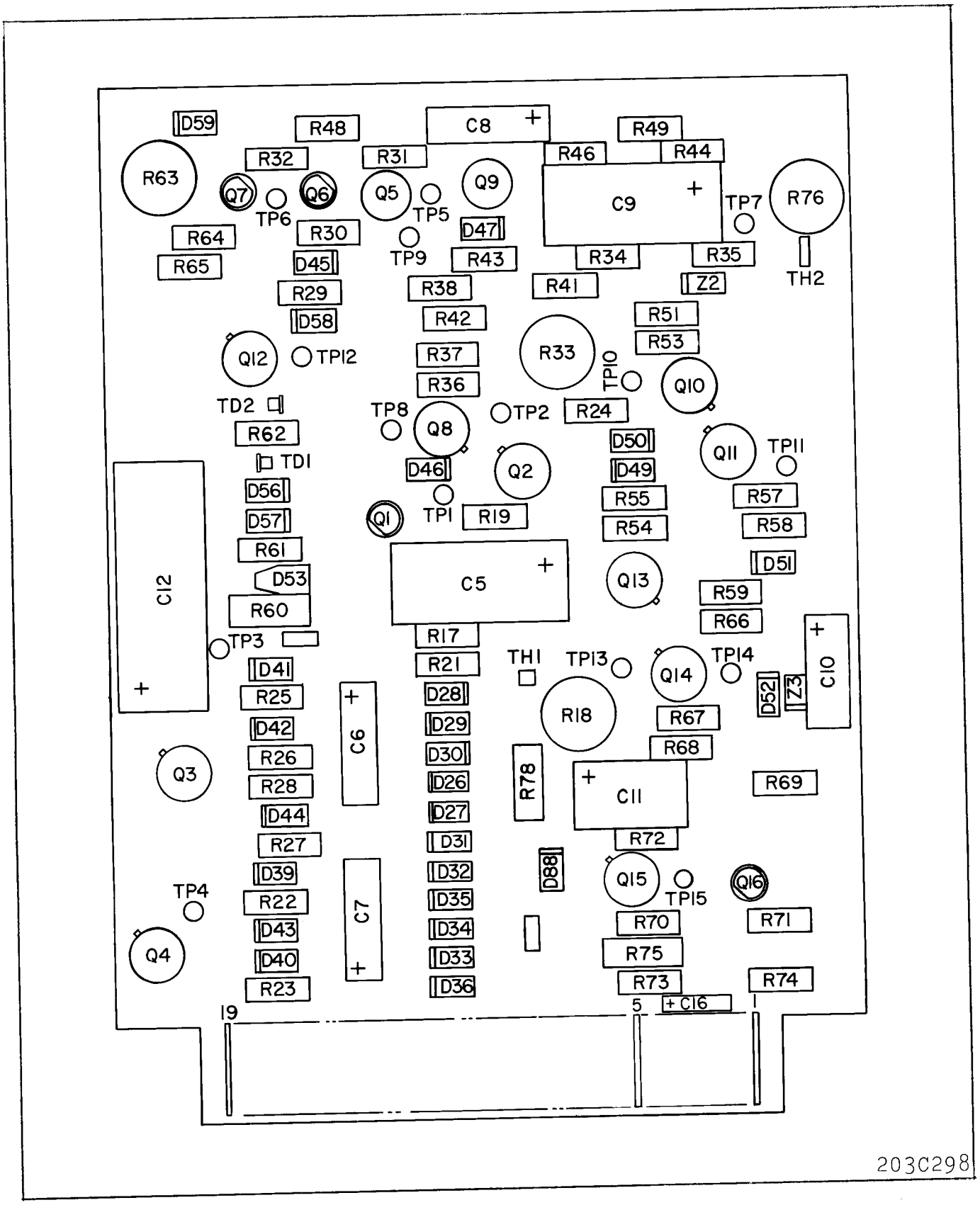


Fig. 26 SDG Component Location Magnitude Comparator.



203C298

Fig. 27 SDG-1 Comp. Loc. Magnitude Comparator.

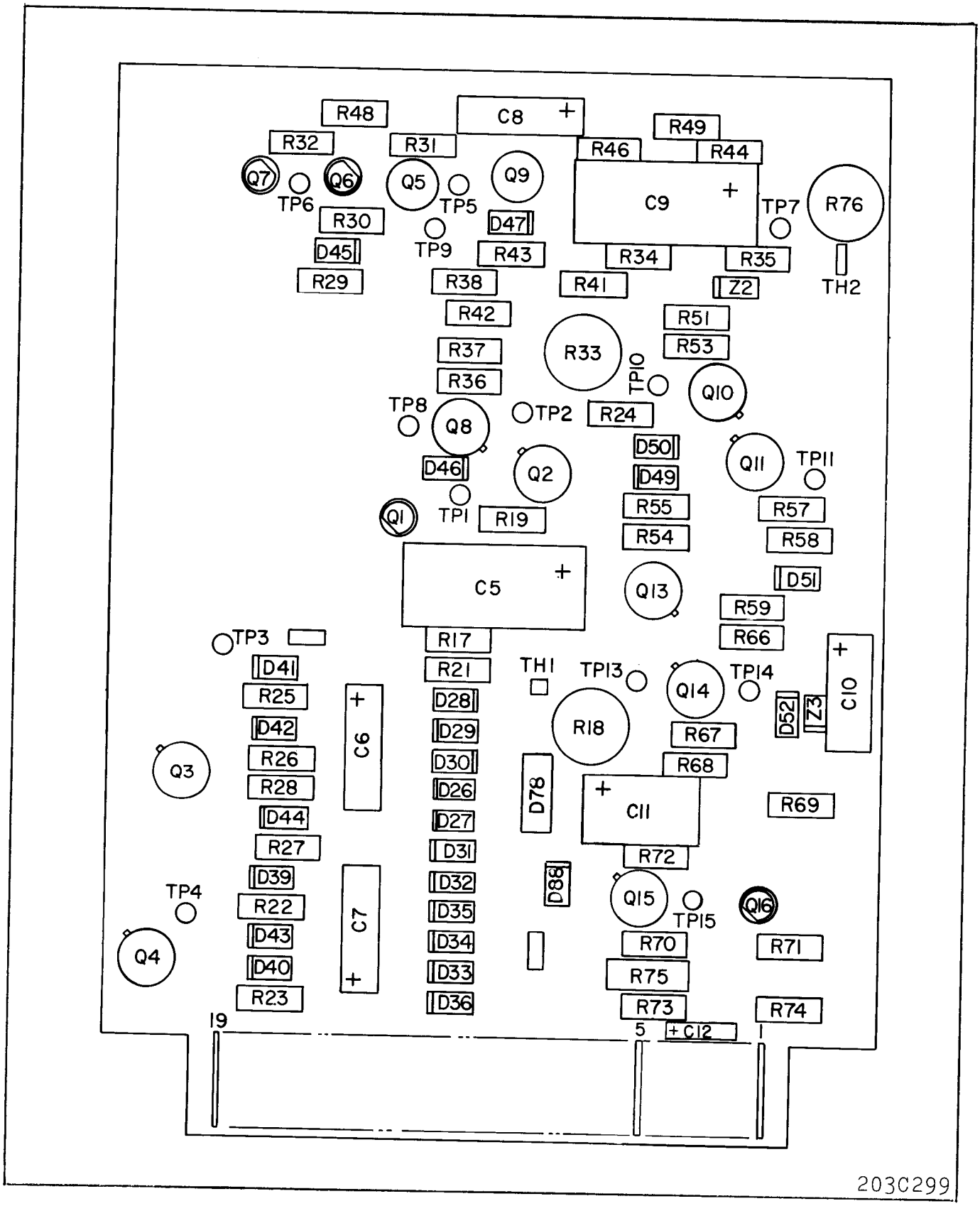


Fig. 28 SDG-2, 5 Comp. Loc. Magnitude Comparator.

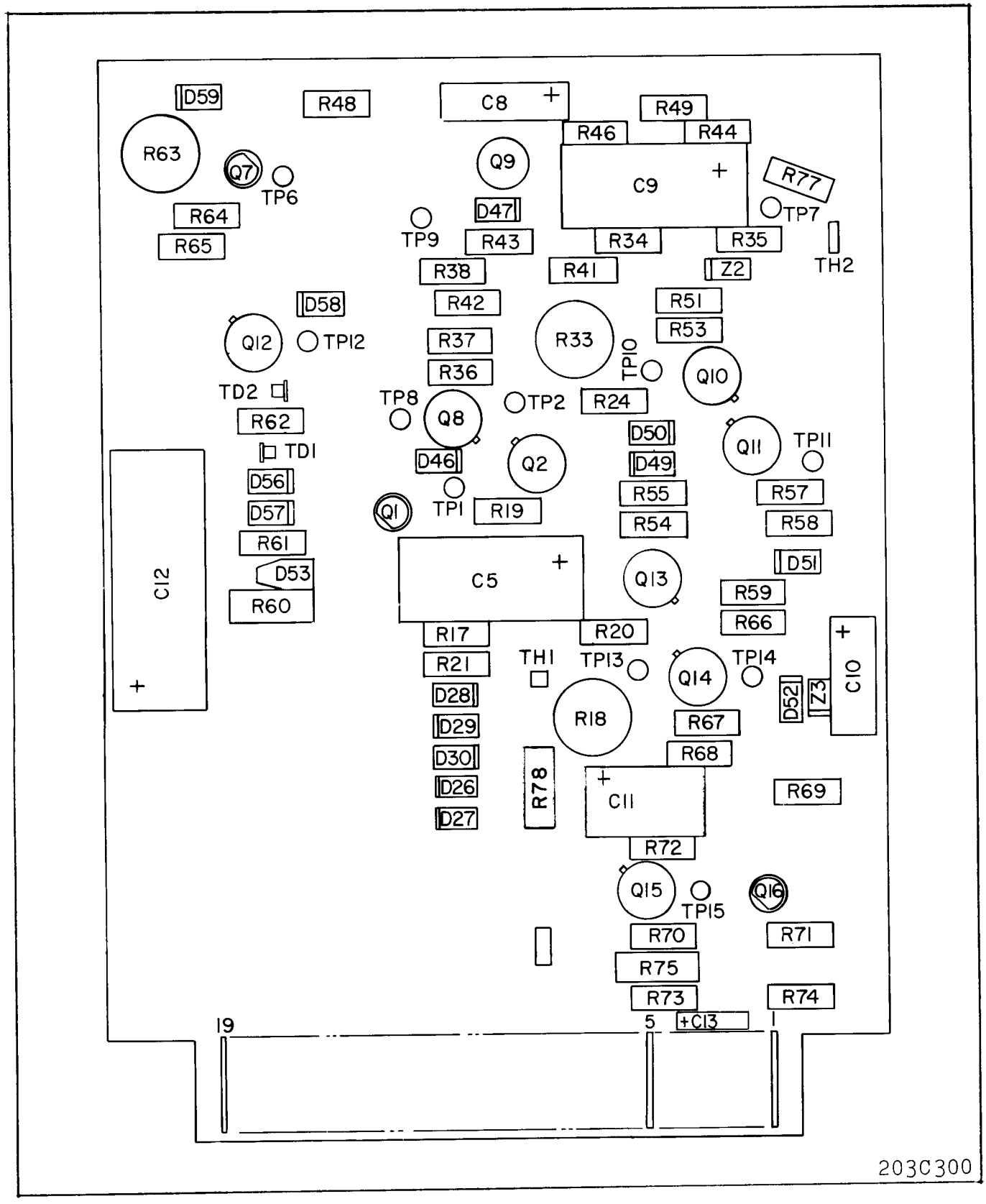


Fig. 29 SDG-3 Comp. Loc. Magnitude Comparator.

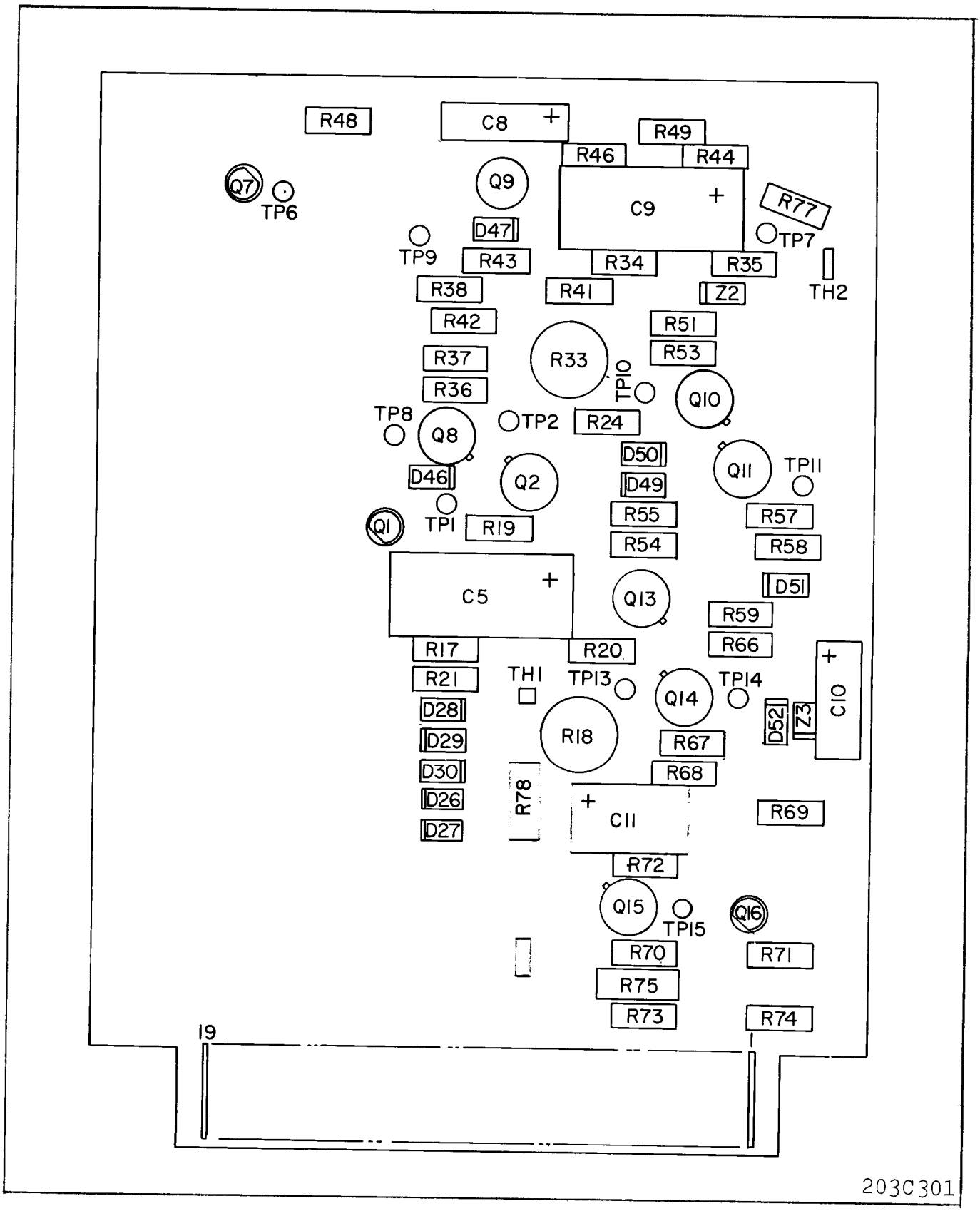


Fig. 30 SDG-4 Comp. Loc. Magnitude Comparator.

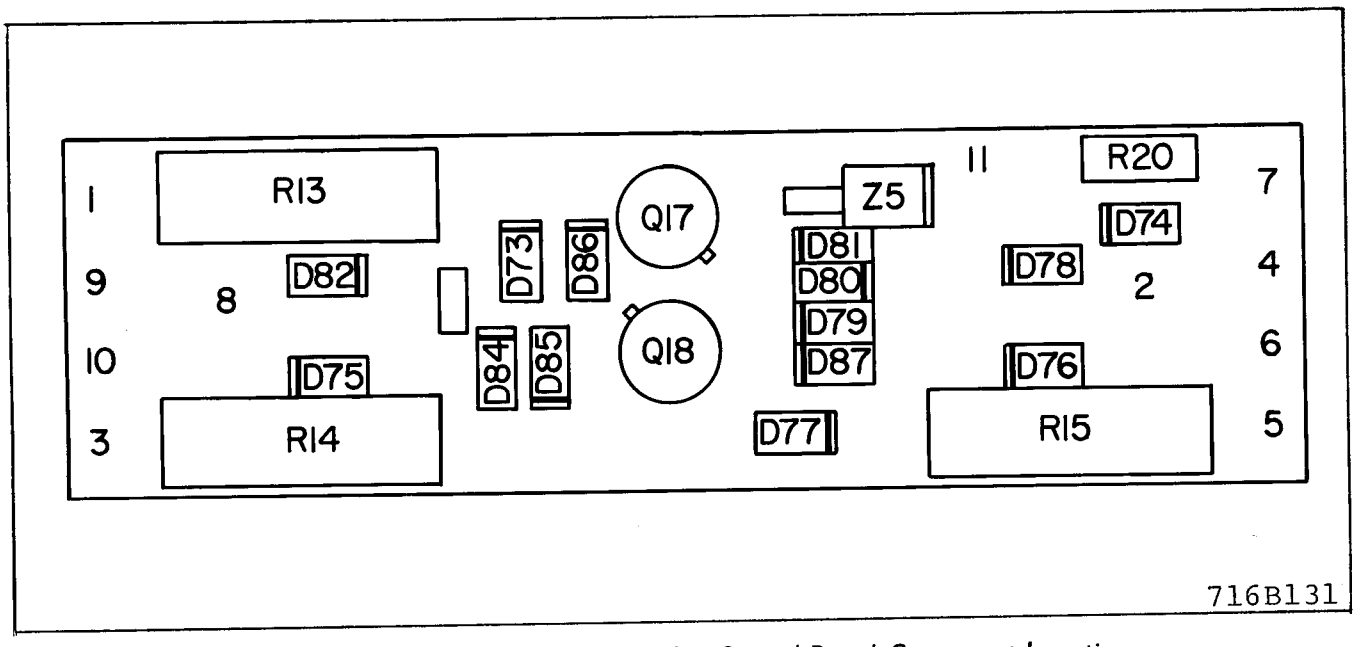


Fig. 31 SDG, SDG-1, SDG-2, 2 ϕ Ground Board Component Location.

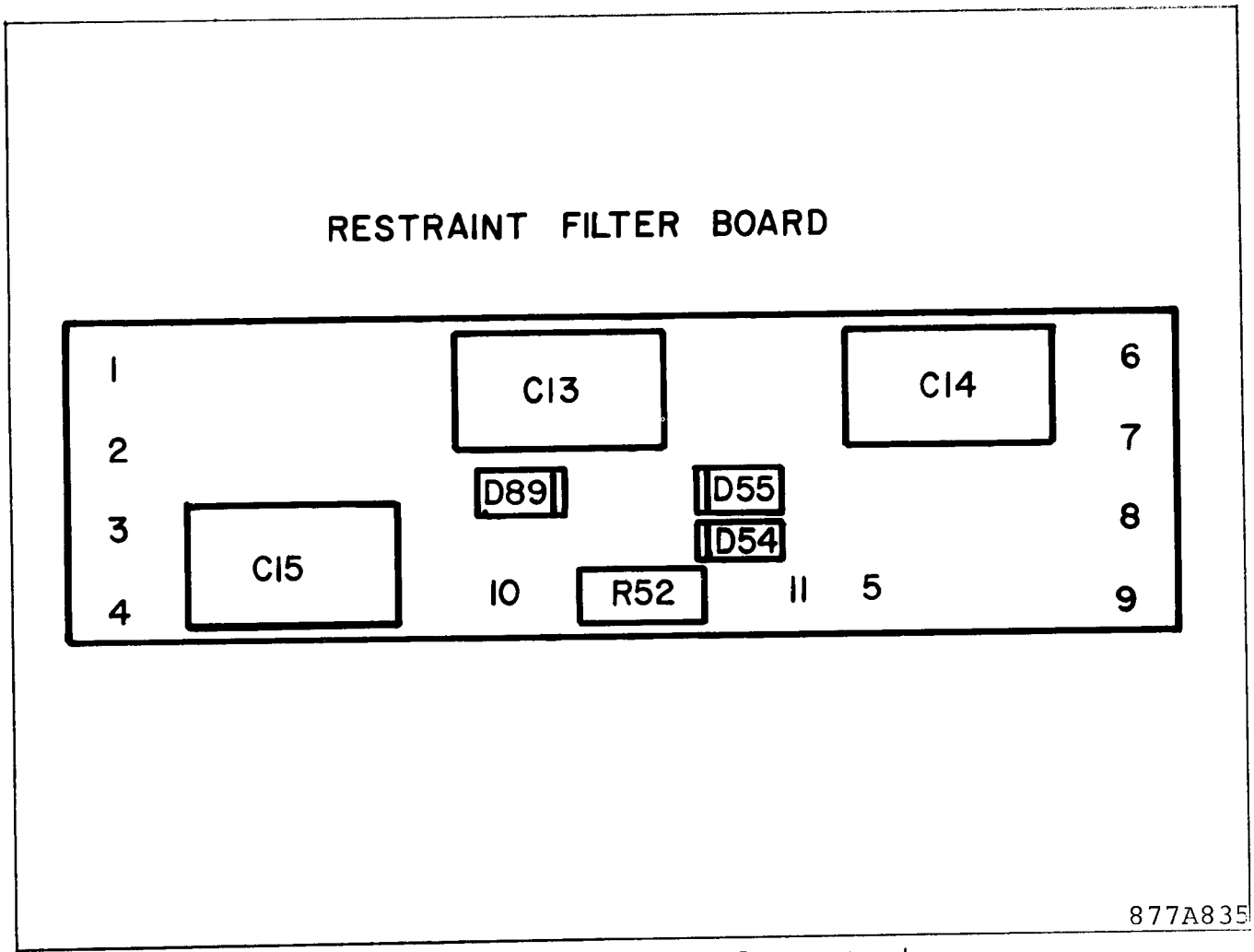


Fig. 32 SDG Component Loc. Capacitor Board

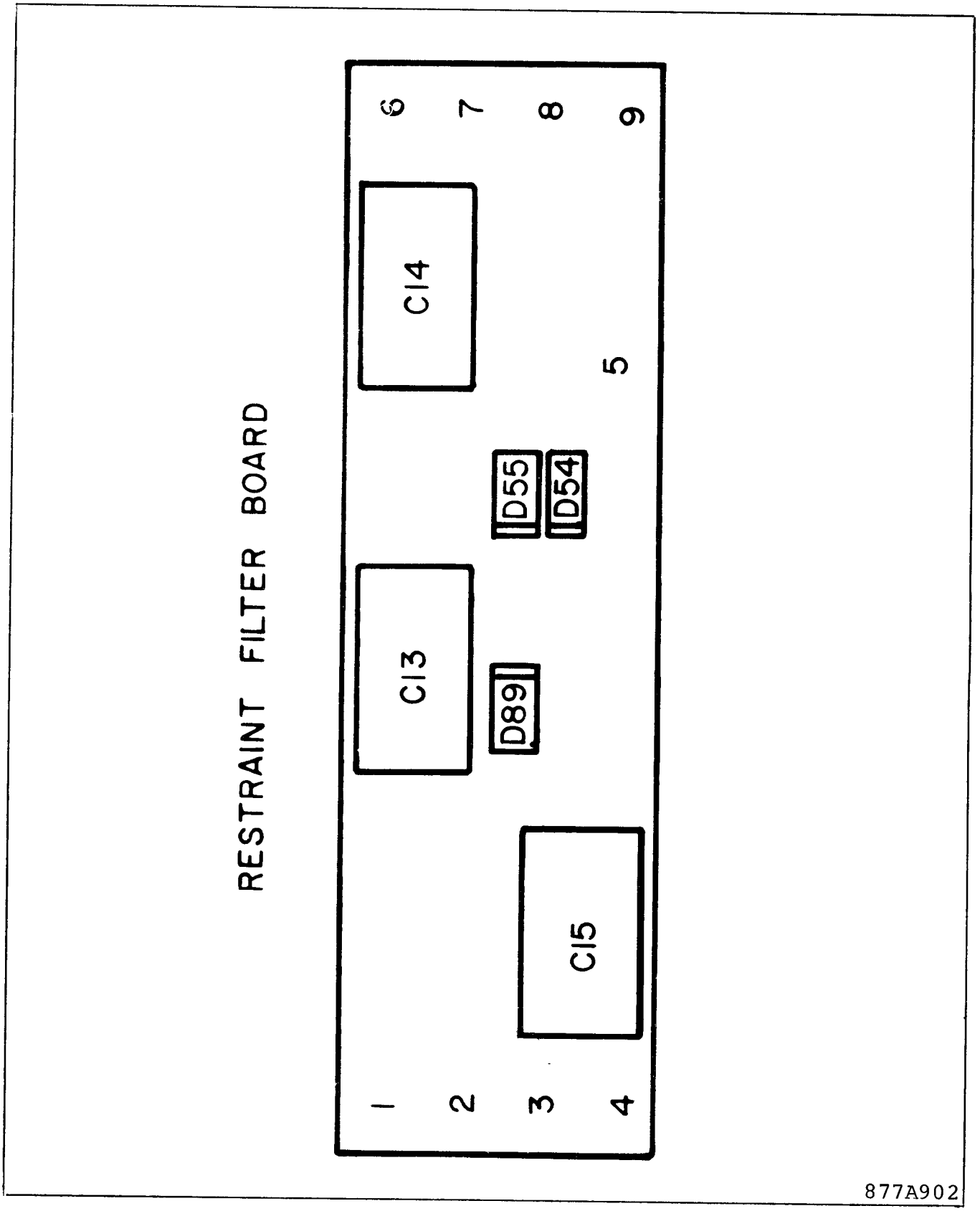


Fig. 33 SDG-1 Component Loc. Capacitor Board

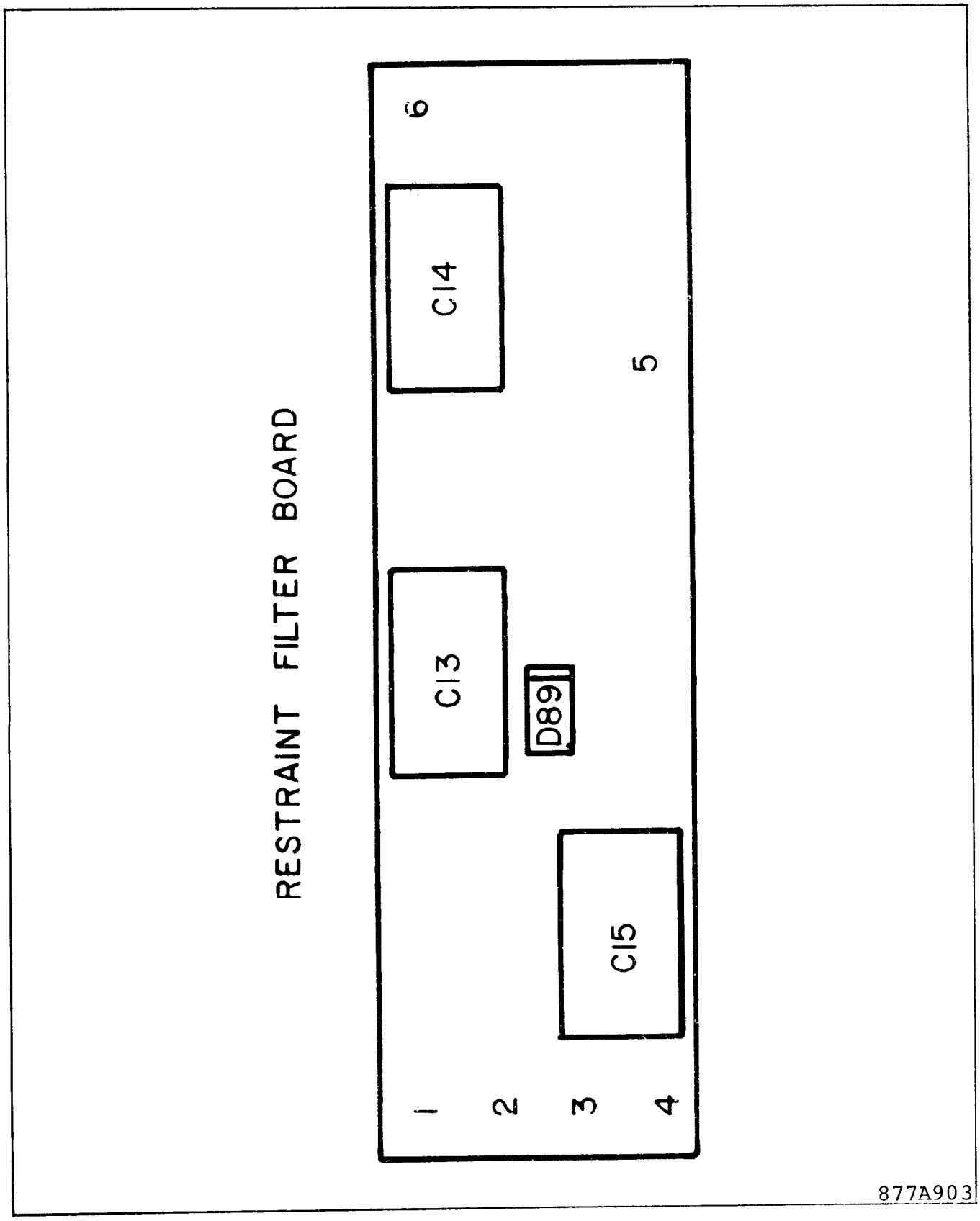


Fig. 34 SDG-2 Component Loc. Capacitor Board

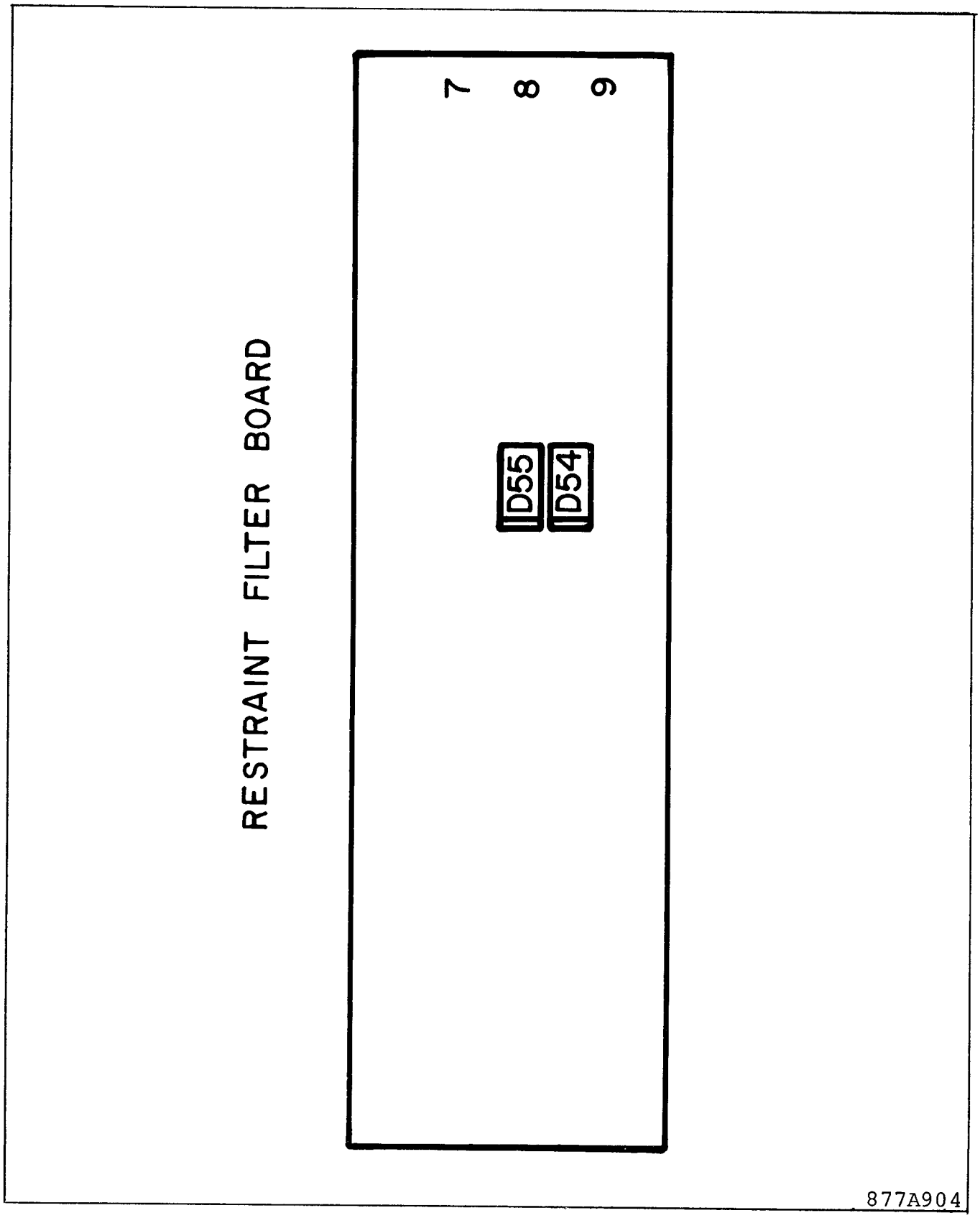


Fig. 35 SDG-3 Component Loc. Capacitor Board

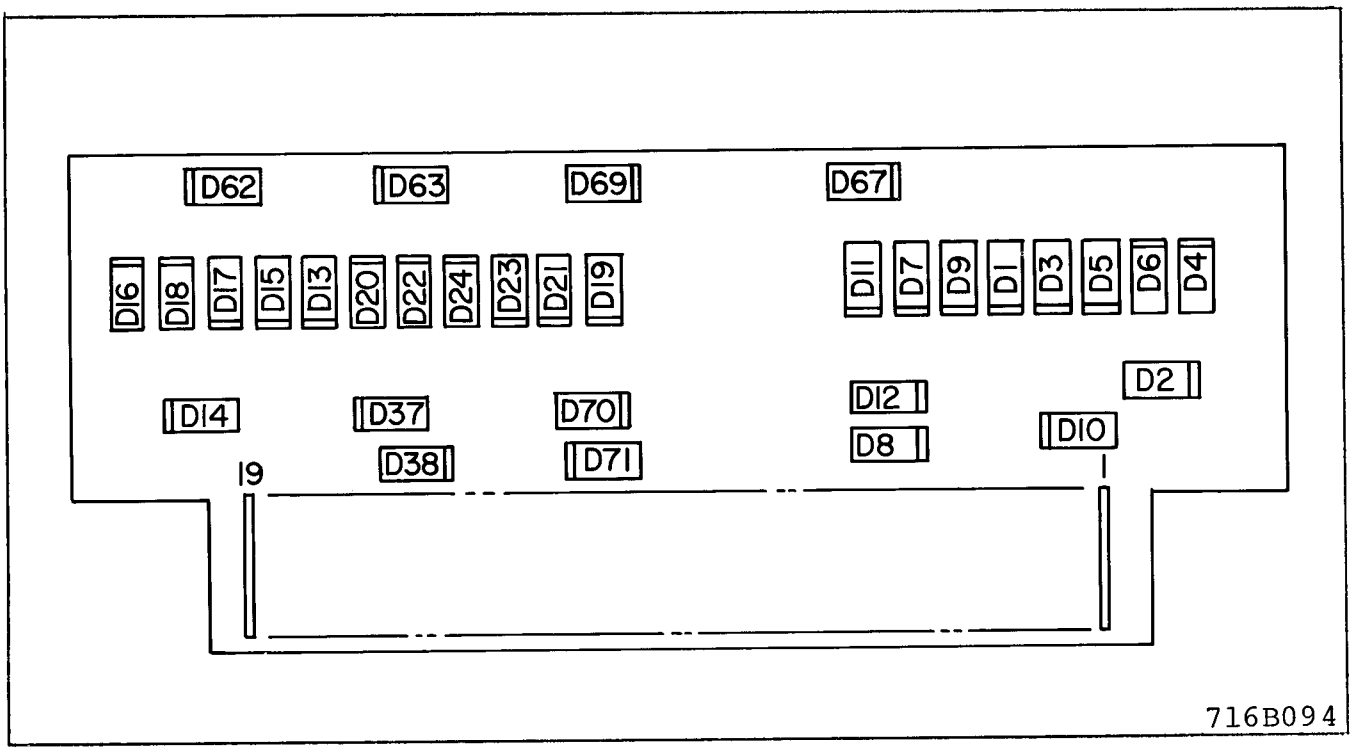


Fig. 36 SDG, SDG-1, SDG-2, SDG-5 Comp. Phase Splitter Board.

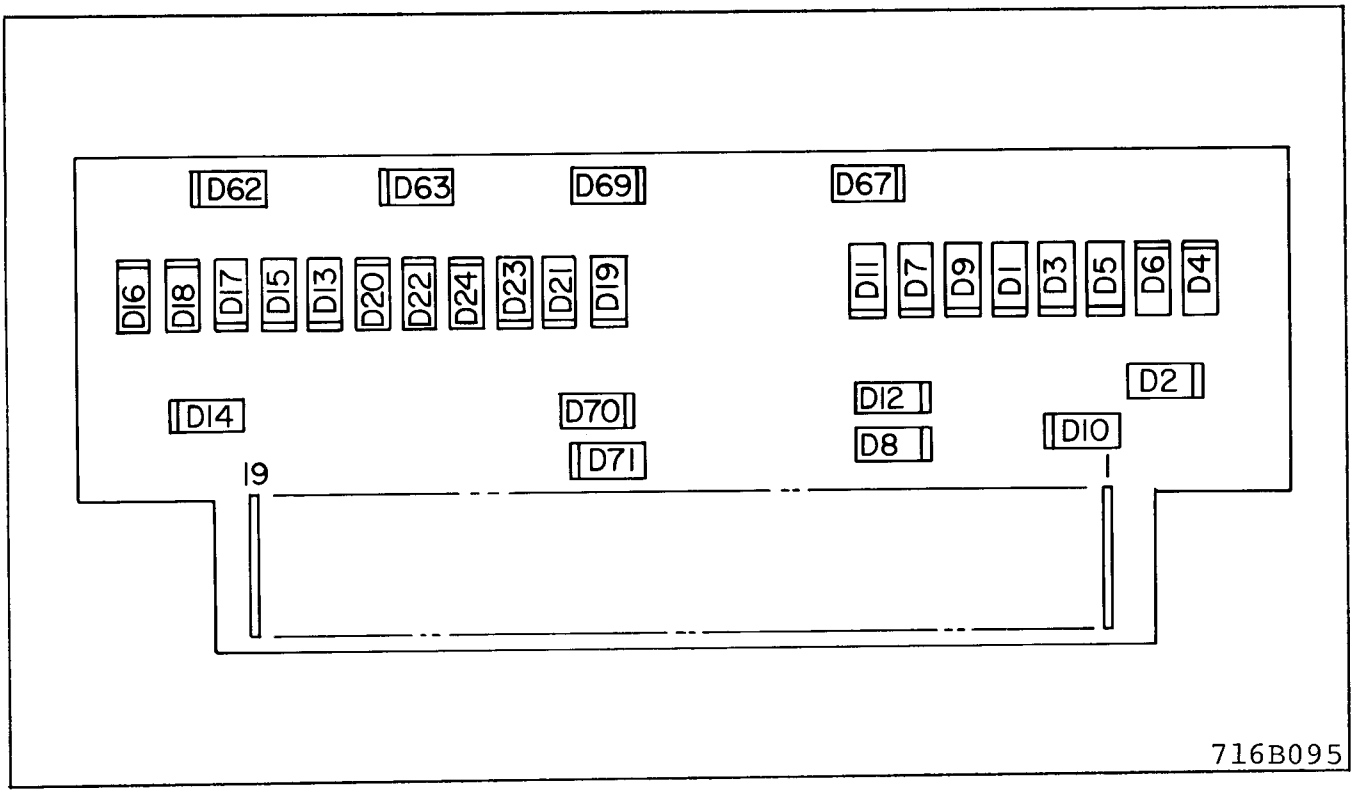


Fig. 37 SDG-3, SDG-4 Component Location Phase Splitter Board.

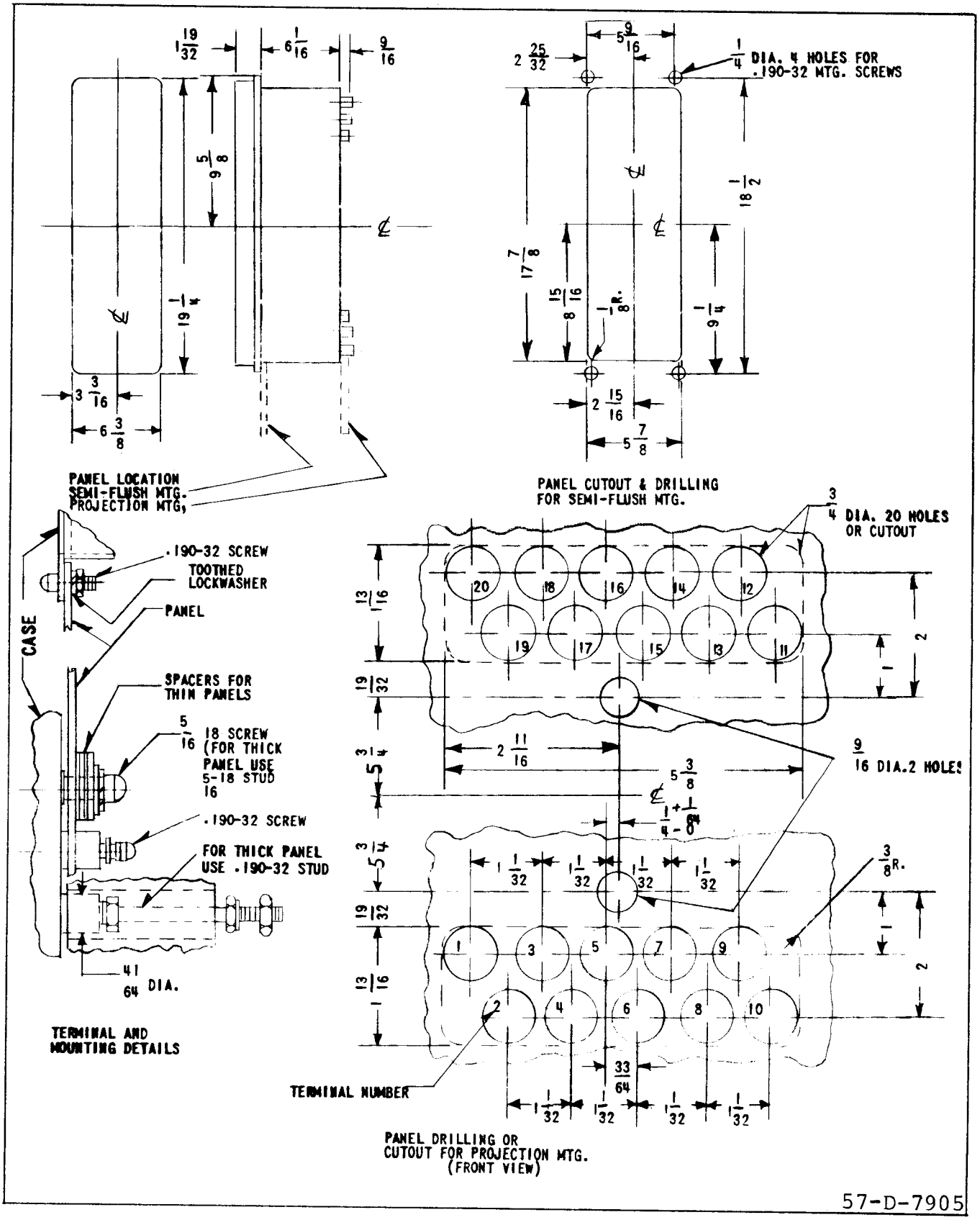


Fig.38 Outline and Drilling Plan for the Type SDG Line Relays in an FT-42 Case.

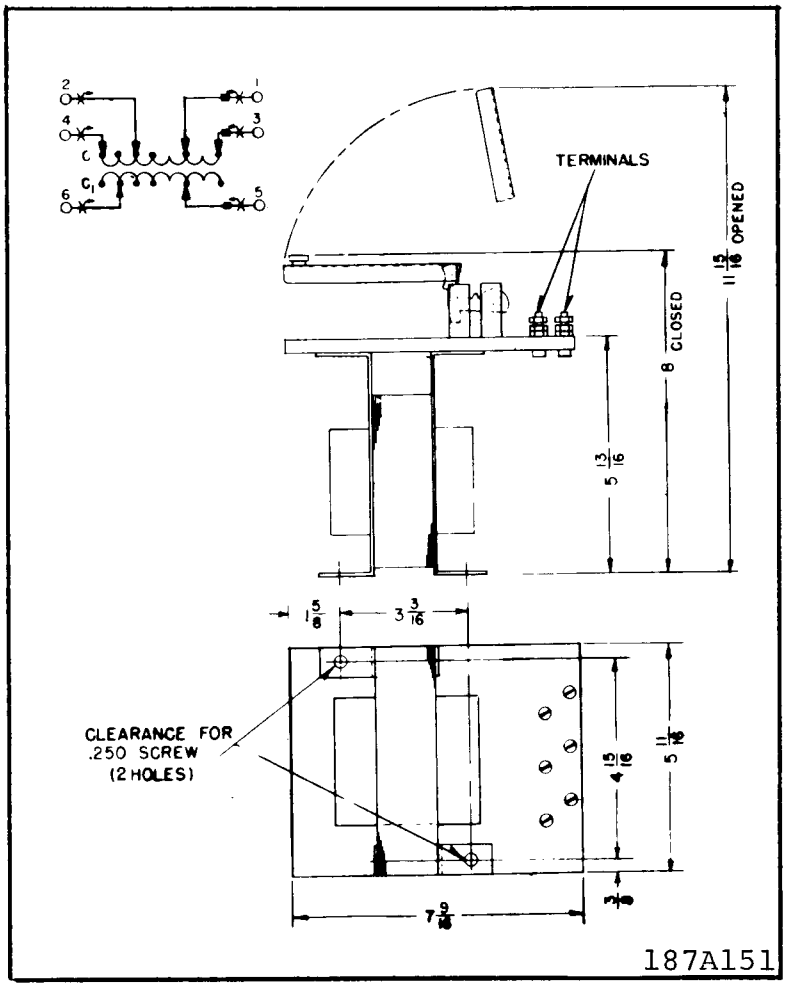
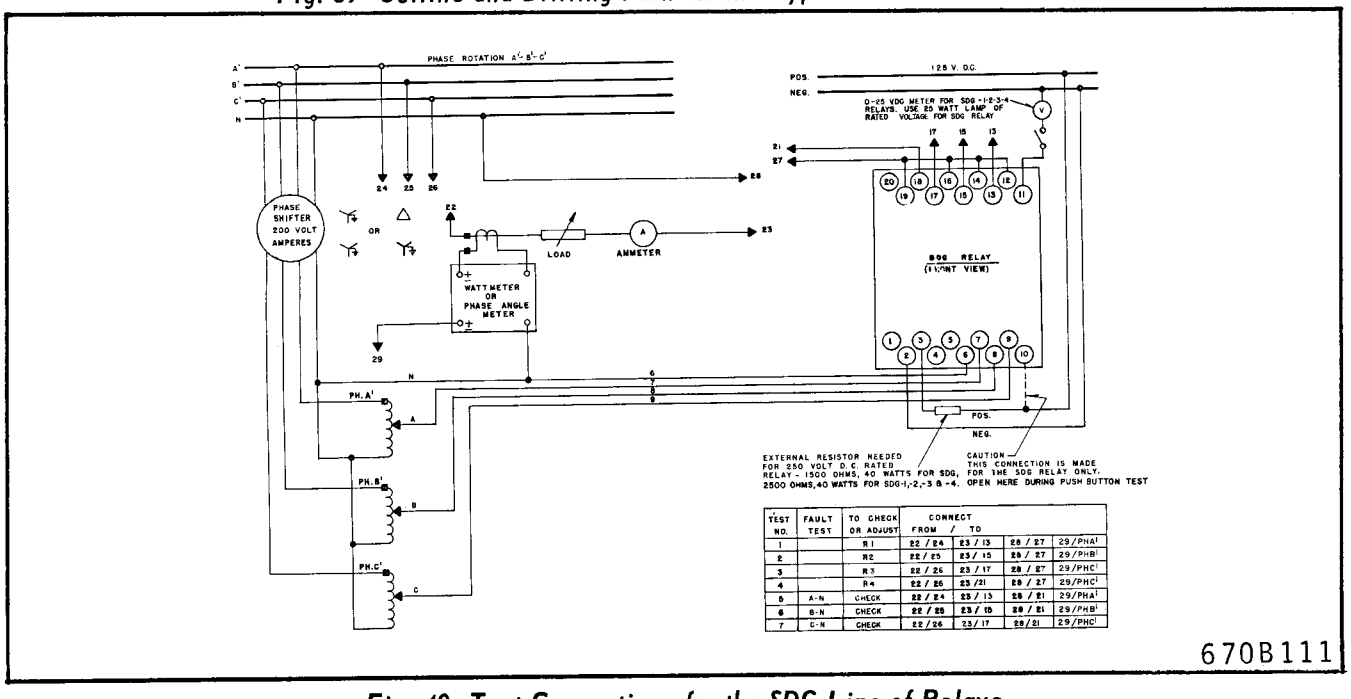
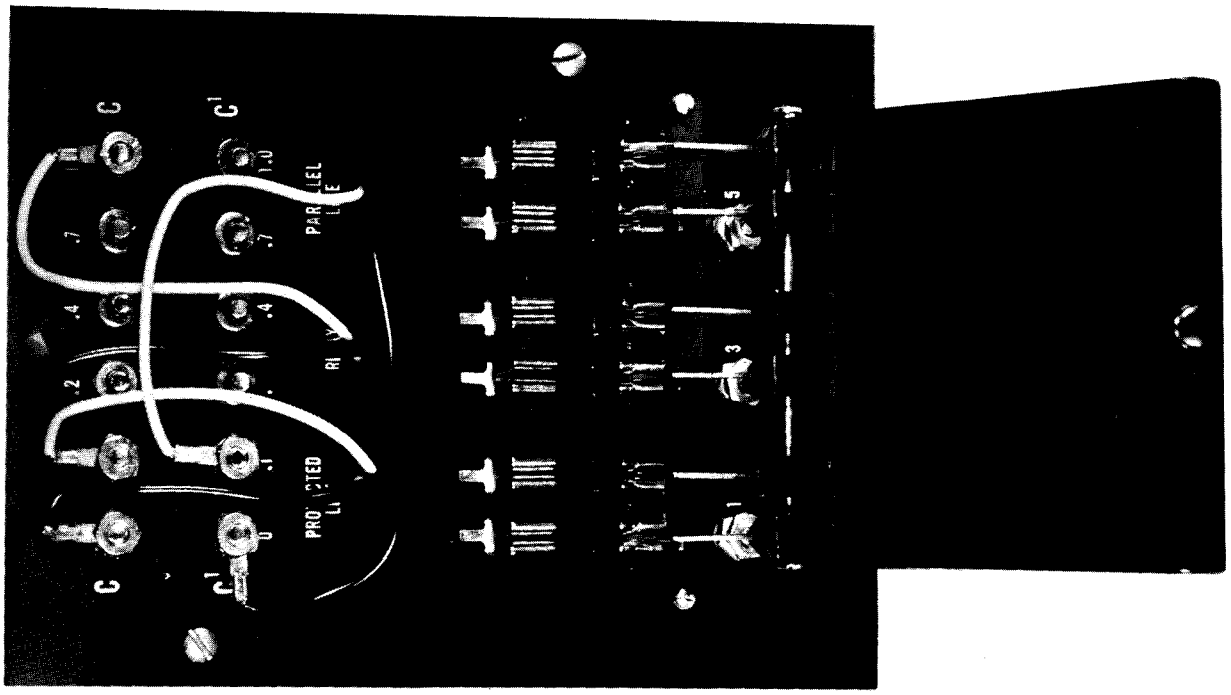


Fig. 39 Outline and Drilling Plan for the Type IK Transformer.



TEST NO.	FAULT TEST	TO CHECK OR ADJUST	CONNECT FROM	TO		
1		R1	22 / 24	23 / 13	28 / 27	29/PHA'
2		R2	22 / 25	23 / 15	28 / 27	29/PHB'
3		R3	22 / 26	23 / 17	28 / 27	29/PHC'
4		R4	22 / 26	23 /21	28 / 27	29/PHC'
5	A-N	CHECK	22 / 24	23 / 13	28 / 21	29/PHA'
6	B-N	CHECK	22 / 25	23 / 15	28 / 21	29/PHB'
7	C-N	CHECK	22 / 26	23 / 17	28/21	29/PHC'

Fig. 40 Test Connections for the SDG Line of Relays



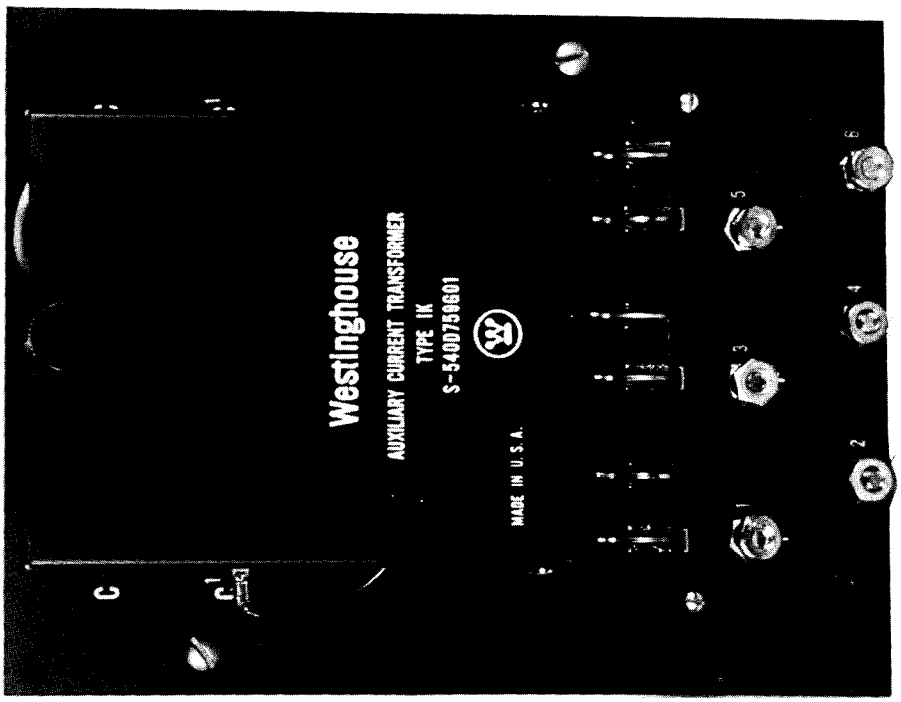


Fig. 41 Type IK Transformer

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