INSTALLATION • OPERATION • MAINTENANCE

INSTRUCTIONS

TYPE SDG LINE GROUND-DISTANCE RELAY

APPLICATION

These instructions cover the five basic types listed in Table I. This line of relays provides single-zone ground-distance protection. The relay

TABLE I

RELAY	I_0 FAULT DET.	FREQ. VERIFIER	PHASE TO PHASE DESENSITIZER	OUTPUT	APPLICATION
SDG	X	X	X	Thyristor	Zone 1
SDG-1	X	X	X	Transistor	Zone 1 or Pilot Trip (Note 1)
SDG-2	-	X	X	Transistor	
SDG-3	X	-	-	Transistor	Timed Trip
SDG-4	-	-	-	Transistor	Blocking Start

NOTE 1: Also suitable for timed trip.

reaches the preset amount for single-line-to-ground faults and as much as 20% less for double-line-to-ground faults.

The potential supply must be wye-grounded. The broken delta potential connection is provided inside the relay.

As shown in Table I the SDG is equipped with a thyristor trip output; use this type where a single-zone is needed in conjunction with an otherwise electromechanical system. For all-static-systems use the transistor output types, utilizing the thyristor trips in the type SRU output package.

The frequency-verifier circuit should be utilized for all high-speed trip applications to avoid undesired trips due to high-frequency transients. This circuit is not needed for timed trips (e.g. zone 2), but the SDG-1 or SDG-2 may be utilized instead of the SDG-3 in the interests of standardization.

Relays with an I_0 current detector are used to prevent tripping due to potential circuit trouble; the SDG-2 requires SI or SI-1 current-detector supervision.

The phase-phase desensitizer is used to eliminate a possible 15% over-reach on two-line-to-ground faults. This circuit is needed for zone 1 applications where the relay reaches 85% towards the far bus.

A type IK auxiliary current transformer may be used to compensate for zero-sequence mutual induction. Otherwise, this transformer is not needed. For the case of two parallel two-terminal lines and an 85% self impedance relay, zone 1 will reach at least 70% to the far end; accordingly, there is not much gain in mutual compensation of zone 1. However, zone 2 should be mutually compensated since its reach is affected more than zone 1. Where zone 1 is mutually compensated, a type SCC current-comparer relay is required to supervise distance relay tripping.

FUNDAMENTALS OF DISTANCE MEASUREMENT ON GROUND FAULTS

The SDG distance relay operates on both single and double line-to-ground faults. In either case, neglecting fault resistance, the faulted phase-to-ground voltage (s) at the relay consists of the line drop:

V_{LG} = Faulted phase-to-ground relay voltage

$$= K_1 I_1 nZ_{1L} + K_2 I_2 nZ_{1L} + K_0 I_0 nZ_{0L} + I_{0E} nZ_{0M} \qquad (1)$$

Where K_1, K_2, K_0 are current distribution factors for the pos., neg., and zero sequence networks, respectively

I_1, I_2, I_0 are the pos., neg., and zero sequence currents in the fault.

nZ_{1L}, nZ_{0L} are the pos. and zero sequence line impedances to the fault.

I_{0E} is the adjacent line zero sequence current.

Z_{0M} zero sequence mutual impedance.

See Fig. 12 for further definition of terms. For an A to ground fault eq. (1) would be written in terms of the phase A quantities.

$$V_{AG} = K_1 I_{A1} nZ_{1L} + K_2 I_{A2} nZ_{1L} + I_{0E} nZ_{0M} \qquad (2)$$

Eq. (2) also applies for an AB to ground fault; an additional expression applies for the phase B quantities for an AB to ground fault.

Hence, a distance ground relay made to respond to single phase-to-ground faults will also respond in the same way to double line-to-ground faults. This is true except for the effect of ground resistance, R_G. The different nature of these effects can be sensed from Fig. 13. In Fig. 13 the ground current $3I_0$ flowing through R_G is essentially in phase with the total faulted phase current. This is so, since $I_{A1} = I_{A2} = I_0$. This is not true for a 2L-G fault. The current $3I_0$ is out of phase with $K_1 I_{A1}$ and $K_2 I_{A2}$ (also out of phase with $K_1 I_{B1}$ and $K_2 I_{B2}$). As a result the drop across R_G produces an apparent reactance term to the distance relay, causing it to under-reach on one phase and over-reach on the other faulted phase. The SDG relay contains a desensitizer circuit to prevent over-reach on 2L-G faults, by reducing the reach of the relay.

$$V_{XN} = (V_{A1} + V_{A2}) - Z_C\,(K_1 I_{A1} + K_2 I_{A2}) \tag{3}$$

$$V_{YN} = (V_{B1} + V_{B2}) - Z_C\,(K_1 I_{B1} + K_2 I_{B2}) \tag{4}$$

$$V_{ZN} = (V_{C1} + V_{C2}) - Z_C\,(K_1 I_{C1} + K_2 I_{C2}) \tag{5}$$

The restraint voltages are obtained by the use of compensators with an impedance Z_C, set to match the desired positive sequence line impedance reach. Only positive and negative sequence voltages appear in eq. (3) to (5). The zero sequence voltage is filtered out by not grounding the neutral of the set of Y-connected auxiliary transformers (T_{A2}, T_{B2} and T_{C2}) which are used to feed the restraint portion of the magnitude comparison circuit. These same connections render the zero sequence current flowing in the phase compensators ineffective. So the restraint voltages duplicate the delta voltage conditions at the fault when the fault is Z_C ohms from the relay (i.e. at the balance point). Zero sequence quantities are not required to duplicate the system voltage triangle at the balance point since zero sequence voltage cancels out of the line to line voltages.

The operating voltage is:

$$V_{WO} = V_O - \frac{Z_{OL}}{Z_{1L}} \times Z_C\,(K_O I_O + I_{OE}\,\frac{Z_{OM}}{Z_{OL}}) \tag{6}$$

Here V_O is the relay zero sequence voltage: it is compensated by using a compensator impedance $\frac{Z_{OL}}{Z_{1L}}\,Z_C$, representing the zero sequence line impedance to the desired balance point. For mutual coupled lines this compensator can be fed with not only the protected line current but also with a portion of the mutual current I_{OE} (See Fig. 12). The operating voltage V_{WO} duplicates the system zero sequence voltage for a fault at the balance point.

Since the faulted phase-to-ground voltage is zero at the fault (neglecting fault resistance), the operating and faulted phase restraint voltage will be equal for a balance point fault. This can be seen by manipulating the fault voltage expression, remembering that the relay compensated voltages are a replica of the fault-point voltages:

V_{LGF} = Faulted phase to ground voltage at fault

$$= V_{1F} + V_{2F} + V_{OF} = 0 \tag{7}$$

$$V_{1F} + V_{2F} = - V_{OF} \tag{8}$$

$$\left|V_{1F} + V_{2F}\right| = \left|V_{OF}\right| \tag{9}$$

Eq. (9) states that the magnitude of the sum of the pos. and neg. sequence voltage equals the magnitude of the zero sequence voltage at the fault. This holds regardless of how many phases are grounded. Eq. (9) is the keystone of the SDG system.

This balance point condition is shown in Fig. 14 for an A-G fault. The bus voltages ($V_{A1} + V_{A2}$) and V_O are shown along with the compensator voltages, which modify the bus voltages to produce restraint voltage V_{XN} and operating voltage V_{WO}.

For this condition V_{YN} and V_{ZN} are also produced but these will be larger in magnitude since these are derived from the sound phases. Since these voltages exceed V_{XN}, they are irrelevant.

In Fig. 14 for a fault beyond the balance point, V_{XN} exceeds V_{WO}; the reverse is true for the fault within the balance point. Note that for all these faults in the trip direction that the phase compensation acts to reduce the bus positive and negative sequence voltages; whereas, the zero sequence compensation is added to V_O. The reverse is true for a fault behind the relay. For this reason the SDG is inherently directional.

One other aspect of Fig. 14 bears amplification. Note for the fault within the balance point that the phase compensation is almost enought to reverse V_{XN} polarity. It is possible for such a reversal to occur, and it is possible if very little zero sequence current flows for the phase compensation to overtake the operating voltage and restrain the relay. Thus, the relay may fail to see a close-in fault if the zero sequence current is quite small. Any time this extreme occurs the phase distance relay will operate. The phase-distance relay will clear the fault when:

$$Z_1 > \frac{V_o/I_o}{K_1+K_2-pK_o}$$

where Z_1 is positive-sequence relay reach

V_o = zero-sequence bus voltage for close-in fault

I_o = <u>total</u> zero-sequence fault current for close-in fault

K_1, K_2, K_o pos.-, neg.- & zero-sequence current-distribution factors for close-in fault.

p = ratio of zero-sequence to positive-sequence line impedance.

CONSTRUCTION & OPERATION

The type SDG relay consists of: four air gap transformers, three auto-transformers for reach adjustment, four phase splitter-transformers, one isolating transformer which couples the zero sequence network a-c output to the static frequency verifier circuit, one zero sequence current-to-voltage transformer, four phase-splitter and rectifier networks, a double line-to-ground fault desensitizer, one voltage regulating zener diode, a thyristor for the tripping function (if used), and printed circuit assemblies.

The large printed circuit assembly contains a magnitude comparator, frequency check circuit, the trigger circuit for the thyristor tripping unit, and the zero sequence current detector.

Compensators (T_A, T_B, T_C, T_O)

The compensators, which are designated T_A, T_B, T_C and T_O are two-winding air-gap transformers. Each current winding has seven taps which terminate at the tap block. A voltage is induced in the secondary which is proportional to the primary tap and current magnitude. This proportionality is established by the cross sectional area of the laminated steel core, the length of an air gap which is located in the center of the coil, and the tightness of the laminations. All of these factors which influence the secondary voltage have been precisely set at the factory. The clamps which hold the lamination should not be disturbed by either tightening or loosening the clamp screws.

The secondary winding has a single tap which divides the winding into two sections. One section is connected subtractively in series with the relay terminal voltage. Thus a voltage which is proportional to the phase current is subtracted vectorially from the relay terminal voltage. The second section is connected to an adjustable loading resistor (R_1, R_2, R_3, R_4) and provides a means of adjusting the phase angle between primary current and the induced secondary voltage. The phase angle may be set for any value between 60^o and 90^o by adjusting this resistor. The factory setting is for a maximum sensitivity angle of 75^o current lagging voltage.

A tertiary winding M has four taps which may be connected to directly modify the T setting by any value from -18 to +18 percent in steps of 3 percent. The sign of M is negative when the R lead is above the L lead. M is positive when L is in a tap location which is above the tap location of the R lead. The M setting is determined by the sum of per unit values between the R and L lead. The actual per unit values which appear on the tap plate between taps are 0, .03, .09 and .06.

Auto-Transformer (T_{A1}, T_{B1}, T_{C1})

The auto-transformers T_{A1}, T_{B1}, T_{C1} have three taps on their main winding S which are numbered 1, 2 and 3 on the tap block.

The three secondary windings of the auto-transformers are connected in a "broken delta", thus serving as a source of zero sequence voltage for the operating circuit. The primary to secondary turn ratio is 3:1, thus producing the proper zero sequence voltage magnitude as required by the theory of relay operation. Using S=2 or S=3 settings reduces zero sequence voltage in the same proportion as the line-to-neutral voltages.

The auto-transformer makes it possible to expand the basic range of T ohms by a multiplier of S.

Phase-Splitter Transformer (T_{A2}, T_{B2}, T_{C2}, T_{O2})

The phase splitter transformer provides isolation between the a-c analog network and the magnitude comparer circuitry located on the printed circuit board, and couples the restraint and operating outputs to the phase splitter network. The tap connection on the secondary winding serves as part of the phase splitting circuit that converts a single-phase input into a three-phase output, thus minimizing the ripple of the rectified output.

Isolating Transformer (I_O)

The isolating transformer I_O serves two purposes: First it isolates the a-c circuit from the d-c circuit, and second, it produces a secondary voltage in the presence of zero sequence current.

Isolating Transformer (T_{FV})

The isolating transformer T_{FV} serves two purposes: First, it isolates the a-c circuit from the d-c circuit and second, it steps up the clipped a-c signal to make the frequency check circuit sensitive to low level input signals.

Double Line-to-Ground Fault Desensitizer

The double line-to-ground fault desensitizer in Figs. 5 & 10 consists of the three networks. Each network consists of a resistor and a minimum voltage network. In this network the largest restraint voltage is blocked by a combination of two restraining voltages. If any two restraining voltages become smaller than the third restraint voltage, transistors Q17 and Q18 are turned on the prevent Q1 and Q2 transistors from turning on. When operating voltage becomes larger than the highest restraint the relay is allowed to trip. The desensitizer effect is limited to S=1 setting only and is not effective on the S=2 or S=3 setting. If S=2 or S=3 setting is used for zone 1 the setting should be reduced to 75% of the protected line to avoid overreach on double-line-to-ground faults.

Magnitude Comparator Circuit (Fig. 15)

The magnitude comparator circuit consists of a minimum voltage network of the voltage balance type in which operating current is caused to flow through a current detector whenever one of the phase restraint voltages becomes smaller than the operating voltage.

Resistors (R9, R10, R11) provide a return path for the operating current.

The current detector consists of a tunnel-diode TD1 and a transistor Q1. When the tunnel diode is switched to the high voltage state, the transistor is turned on. The use of the tunnel diode secures a sharp turn on characteristic for the triggering network.

When transistor Q1 is turned on it in turn switches transistor Q2 on, when transistor Q2 is "on" the collector voltage is raised to high positive voltage that starts the operation of the triggering circuit.

Triggering Circuit for SDG Relay (Fig. 16)

The triggering circuit consists of a four-layer diode D50, resistor R28, diode D51, and pulse transformer TR-1. Whenever Q2 transistor is turned on capacitor C6 starts charging to the breakdown voltage of the four layer diode D50.

After breakdown of D50, capacitor C6 discharges through the primary of the TR-1 transformer thus producing a gating impulse that fires the output thyristor QS1 Diode D49 provides a quick discharge of C6 after Q2 is turned off through R24. Diode D51 protects D50 from reverse polarity. The triggering circuit is supervised by the residual overcurrent unit and frequency verifier circuit through diodes D52 and D60. D52 diode bypasses the charging capacitor C6 during the 4 ms.

period the frequency verifier output is held at ground potential. D60 performs the same function in the absence of residual current.

Zero Sequence Current Detector (Fig. 17)

To prevent operation of the magnitude comparator during a blown potential fuse or similar condition a zero sequence current detector supervises the operation of the triggering network by preventing capacitor C6 in the triggering circuit from charging, keeping the point "P" at negative potential through the diode D60.

The detector employs a tunnel diode (TD3) as a level detector. The tunnel diode is biased through resistor R45 to the high voltage state so that enough voltage is maintained across the base-to-emitter junction of Q8 transistor to keep it conducting.

In the presence of the residual current a current derived negative voltage through transformer I_0 appears across resistor R41, switching TD3 to the low voltage state, thus turning transistor Q8 off and raising its collector to the positive DC voltage supply level, blocking D60 from discharging the C6 capacitor.

Frequency Verification (Fig. 18)

During certain switching conditions, such as energization of a transmission line, residual currents and voltages may exist of higher frequencies than 60 cycles per second. The frequency verifier prevents relay operation when the operating voltage period is less than 4.3 ms. The frequency verification circuit consists of two functional parts: zero-crossing and commutator circuits. The zero-crossing circuit consists of transistors Q3, Q4, Q5, and Q6. The zero-crossing circuit is used to allow operation in the presence of higher frequencies of small magnitude superimposed on a fundamental of 60 cps. During the positive or negative half cycles of the operating voltage V_{WO}, Q3 or Q4 transistors are driven into saturation by the output of the T_{FV} transformer. Transistors Q5 or Q6 conduct until capacitors C8 or C10 respectively are fully charged. While either capacitor charges, a voltage output in the form of very narrow pulse is developed across R32 & R33 resistors during the start of each half cycle. This pulse triggers QS2 control switch. When transistors Q3 or Q4 are not conducting, C8 and C10 capacitors discharge respectively through D45 or D44 and the parallel combination of R26 and R30 or R25 and R29.

While QS2 is "on" its anode is only about 0.7 volt above negative, thus preventing capacitor C6 in the triggering circuit from charging for 4.3 milliseconds. The time delay of 4.3 milliseconds is controlled by the resistor R38, the capacitor C11 and the reference Zener diode Z4. After 4.3 milliseconds of delay the control switch QS3 fires applying the voltage of capacitor C9 across QS2, turning it off. This raises the potential of the QS2 anode, leaving the triggering circuit free to operate. After the next zero crossing pulse, QS2 switch is turned on again, the QS3 switch is turned off by capacitor C9. Charge and commutator action is repeated all over again. Transistor Q7 when turned on by the same voltage that fires the gate of QS2, discharges timing capacitor C11, thus starting the timing cycle with close to zero charge on the capacitor. If the period of the V_{WO} voltage is less than 4.3 ms, the Q7 transistor discharges the timing capacitor thus preventing the turning off of QS3 switch. This keeps QS2 switch on to prevent operation of the triggering circuit.

Output Circuit (Fig. 19)

The output circuit or SDG relay consists of the secondary of the pulse transformer TR-1, diode D46, capacitor C7, resistor R31, and Zener diode Z3. The output of the SDG relay is a thyristor which is gated into conduction by a pulse transformer. The transformer is pulsed as described under "Triggering Circuit Operation". Zener diode Z3, resistor R31 and capacitor C7 form a network protecting the thyristor unit from voltage surges coming through the d-c supply. The function of diode D46 is to short out negative pulses coming from the TR-1 pulse transformer.

In the SDG-1, -2, -3, & -4 relays the output circuitry consists of transistors Q3, Q5, & Q6 and other associated components.

Upon the operation of the Q2-transistor in the magnitude comparator circuit, transistor Q3 is driven into conduction by the positive voltage developed across resistor R22. Transistor Q3, in turn, shunts the base drive current of transistor Q5, to turn Q5 off. At the same time the turned on Q3-transistor provides a base current path to transistor Q6 turning it on. An output voltage consequently is developed through transistor Q6, resistor R28, across Q5 and appears at relay terminal 11. In absence of the output from the magnitude comparator circuit the Q5 transistor is biased to conduct through resistor R24 and no output appears at relay terminal 11.

Q7 and QS1 form the pushbutton light circuit that operates an indicating light during a pushbutton check-out procedure.

Pushbutton Check Circuit (Fig. 20)

The pushbutton check circuit is used for in-service operational check-out of the output thyristor. Depressing the pushbutton provides an internal d-c supply to the thyristor switch and operates the overcurrent circuit. This action must be preceded by the opening of the relay trip circuit (red handle) and relay voltage switch (7). The opening of the voltage switch produces operating voltage conditions in the magnitude comparator that gates the thyristor switch. Operation of the thyristor switch is indicated by the lighting of the bulb built into the pushbutton. A similar circuit is provided in the SDG-1, -2, -3, & -4 relays (See Fig. 10).

CHARACTERISTICS

Distance Characteristics

Fig. 24 shows the relay characteristic in the complex plane is $Z = nZ_{1L} + \frac{3R_G}{F}$ for single line to ground faults where factor $F = K_1 + K_2 + pK_0$. Impedance nZ_{1L} is the positive-sequence line impedance from the relay to the fault. The apparent impedance Z must fall within the characteristic shown in Fig. 24 in order to operate. Note that part (A) of Fig. 24 applies for the case of a low source impedance vs line impedance; parts (B) and (C) represent increasing amounts of source impedance, or conversely shorter line lengths. The solid-line characteristic is based on current distribution factors for a balance point fault with all breakers closed. As the fault moves toward the relay these distribution factors increase, with the relay approaching the dashed-line characteristic. In the case of Fig. 24C, the dashed-line characteristic is not shown, as it

essentially coincides with the solid-line characteristic. Regardless of system conditions, the relay reaches Z_C positive-sequence ohms for a fault at the compensator angle. The fact that the circle diameter expands with increasing source impedance is beneficial, since this provides increased fault resistance accommodation for the shorter line applications. By this we mean that it takes a greater $\frac{3R_G}{K_1+K_2+pK_0}$ component to yield a Z phasor which is outside the operate zone. The R-X characteristic is a composite of three circles whose centers are A, B, and C in Fig. 24A. The circle whose center is A is produced from the comparison of faulted phase restraint and operating voltage for a single-line-to-ground fault; whereas the "B" and "C" circles result from sound-phase restraint comparison with operating voltage. In Fig. 24C only the faulted phase characteristic is shown, since the other two fall well out of the first quadrant.

One might conclude from Fig. 24 that the relay is not directional since its characteristic includes the origin. This conclusion would be erroneous, since the characteristic equations assume faults in the trip direction per Fig. 14 and do not apply for reversed faults. The relay is directional. In Fig. 24 the second and third quadrants are essentially theoretical since a "negative resistance" is only possible due to out-of-phase infeed. The fourth quadrant is pertinent for series capacitor applications. So we are normally only interested in the first quadrant.

General Characteristics

Impedance settings in ohms reach can be made in steps of 3 percent. The maximum sensitivity angle, which is set for 75 degrees at the factory, may be set for any value from 60 degrees to 90 degrees. A change in the maximum sensitivity angle will produce a slight change in reach for any given setting of the relay. Referring to Fig. 11, note that the compensator secondary voltage output V, is largest when V leads the primary current, I, by 90°. This 90° relationship is approached, if the compensator loading resistor is open-circuited. The effect of the loading resistor, when connected, is to produce an internal drop in the compensator, which is out-of-phase with the induced voltage, IT_A, IT_B or IT_C. Thus the net voltage, V, is phase-shifted to change the compensator maximum sensitivity angle. As a result of this phase shift the magnitude of V is reduced, as shown in Fig. 11. The tap markings are based upon a 75° compensator angle setting. If the resistors R1, R2, R3, and R4 are adjusted for some other maximu sensitivity angle the nominal reach is different than that indicated by the taps. The reach Z_Θ, varies with the maximum sensitivity angle, Θ, as follows:

$$Z_\Theta = \frac{TS \sin \Theta (1+M)}{\sin 75^\circ}$$

TAP PLATE MARKINGS

T_A, T_B, T_C,	1.2	1.5	2.1	3.0	4.5	6.3	8.7	- for 1.0-31 ohms range
(Pos. Seq.)	.23	.307	.383	.537	.69	.92	1.23	- for .2-4.35 ohms range

T_0	3.60	4.5	6.3	9.0	13.5	18.9	26.1	- for 1.0-31 ohms range
(Zero Seq.)	0.69	0.92	1.15	1.61	2.07	2.76	3.69	- for .2-4.35 ohms range

	(S_A and S_C)	
	1	2 3
± Values between taps	(M_A and M_C)	
	.03	.09 .06

TIME CURVES AND BURDEN DATA

Operating Time

The speed of operation is shown in Fig. 21. The curves indicate the time in milliseconds required for the relay to provide an output for tripping after the occurance of a fault at any point on a line within the relay setting.

Current Circuit Rating in Amperes

Continuous - 10 Amperes

1 Second - 240 Amperes

Burden

The potential burden at 69 volts varies from a maximum of 1.4 volt-amperes at S=1 setting to a minimum of 0.42 volt-amperes based on 69 volts line to neutral per phase. Current burden varies from a maximum of 4.5 volt-amperes at 5 amperes for a maximum T-setting to a minimum of 0.60 volt-amperes for a minimum T-setting. This burden applies to each phase and residual current circuit. D.C. current burden is .07 amperes at all rated voltages.

Trip Circuit Constants

1 Ampere I.C.S. 0.1 ohms d-c resistance

Thyristor (SDG only)

The thyristor is a three-terminal semiconductor device. In the reverse, or non-conducting direction, the device exhibits the very low leakage characteristics of a silicon rectifier. In the forward, or conducting directions conduction can be initiated by the application of a control pulse to the control terminal or "gate". If a gate signal is not applied, the device will not conduct at below rated forward blocking voltage. With the application of a gate signal, however, the device switches rapidly to a conducting state characterized by a very low voltage drop and a high current-carrying capability. Once a conduction has been initiated, the gate terminal no longer has any effect. In order to turn the thyristor off the anode-cathode current must be reduced to a value less than the holding current.

It should be noted that the SDG differs from mechanically operated contacts. A certain minimum trip current must flow before the thyristor will latch on. If the minimum turn on current is not established during the first millisecond after the first gate pulse is received, the unit will not latch on. However, voltage will be applied to the load for the duration of each pulse. Pulses are applied to the gate circuit at a rate of four every one milliseconds.

Current rating per circuit:

Ambient Temperature	25°C	50°C	75°C
For 50 ms.(3 cycle breaker)	60 A	49 A	37 A
For 83 ms.(5 cycle breaker)	54 A	44 A	33 A
Continuous	6.5 A	4.5 A	3 A

Trip Circuit Requirements:

$$\frac{Vdc}{R_{LOAD\ OHMS}} = .25 \text{ amp or more}$$

$$\frac{L_{HENRYS}}{R_{LOAD\ OHMS}} = .02 \text{ or less}$$

Thyristor

Max forward leakage current at rated voltage	125° C	8 MA d-c
Max reverse leakage current at rated voltage	125° C	8 MA d-c
Max forward voltage drop at 10 amps	25° C	1.6 volts

CALCULATIONS AND SELECTION OF SETTINGS

Relay reach is set on the tap plate. Maximum sensitivity angle, θ, is set for 75° (current lagging voltage) in the factory. This adjustment need not be disturbed for line angles of 65° or higher. For line angles below 65°, set θ for a 60° maximum sensitivity angle, by adjusting R_1, R_2, R_3 & R_4. Set zone 1 reach to be 85% of the line, if S=1; 75% if S=2 or 3.

Assume a desired balance point which is 85% of the total length of the line. The general formulas for setting the ohms reach of the relay are:

$$Z_1 = Z_{1L} \frac{0.85\ Rc}{Rv} \quad ; \quad Z_0 = Z_{0L} \frac{0.85\ Rc}{Rv}$$

The terms used in this formula and hereafter are defined as follows:

Z_0 = Zero sequence ohmic reach.

Z_1 = Positive sequence ohmic reach

$Z'_{1,0}$ = TS (1 + M) = the tap plate setting.

T = Compensator tap value.

S = Auto-transformer tap value.

θ = Maximum sensitivity angle setting of the relay.

$\pm M$ = Compensator tertiary tap value. (This is a per unit value and is determined by the sum of the values between the "L" and the "R" leads. The sign is positive when "L" is above "R" and acts to raise the Z setting. The sign is negative when "R" is above "L" and acts to lower the "Z" setting).

Z_{1L} = Positive sequence ohms per phase of the total line section, referred to primary.

Z_{0L} = Zero-sequence ohms per phase of the total line section, referred to primary.

R_c = Current transformer ratio.

R_v = Potential transformer ratio.

The following procedure should be followed in order to obtain an optimum setting of the relay.

Zone 1 Setting (SDG, SDG-1, SDG-2 Relays)

1. (a) Establish the desired values of Z_1 and Z_0 as above (available from transmission line data).
   (b) Determine the desired tap plate value Z' using the formula:

$$Z_1' = Z_1 \frac{\text{Sin } 75^\circ}{\text{Sin } \theta^\circ} \text{ and } Z_0' = Z_0 \frac{\text{Sin } 75^\circ}{\text{Sin } \theta^\circ}$$

When $\theta = 75^\circ$, $Z_1' = Z_1$ and $Z_0' = Z_0$

2. Now refer to Table II or IV giving preferred zone 1 settings for the SDG relays. If the desired reach exceeds the relay range for S=1, use S=2 & Table III or V (set for 75% of line).

   (a) Locate a table value for relay reach nearest to the desired Z' value (it will always be within 1.5% of the desired value.)
   (b) From this table read off the "S", "T" and "M" settings. The "M" column includes additional information for the "L" and "R" lead setting for the specified "M" value. If the desired settings cannot be found on this table proceed to Table III or V to find the desired setting. The relay reach must now be reduced from 85 to 75 percent to avoid overreach on two phase to ground faults on high fault resistance faults.
   (c) Determine actual values for Z_1 & Z_0 using equation:

$$Z = TS\ (1+M)$$

For example, assume the desired reach, Z_1 is 7 ohms at 60° (Step 1a) and Z_0 is 21 ohms at 60°.

Next step is (1b). Making correction for maximum sensitivity angle of the line (60°) that is different from factory setting of 75°, we find the relay tap setting

$$Z_1' = 7 \times 1.11 = 7.77 \text{ ohms}$$

$$Z_0' = 21 \times 1.11 = 23.31 \text{ ohms}$$

Step (2a). In Table IV we find 7.65 to be the nearest value to 7.77 ohms.

$$100 \times \frac{7.65}{7.77} = 98.8\% \text{ or } 1.2\% \text{ from the desired value}$$

For the Z_0 selection find the nearest value to 23.31 ohms using the same S setting as above. 23.0 ohms is the nearest value.

$$100 \times \frac{23.0}{23.31} = 98.8\% \text{ or } 1.2\% \text{ within the desired value}$$

Step (2b). From Table IV read off:

$$S = 1$$
$$T = 8.7$$
$$T_0 = 26.1$$
$$M = -.12$$

The "R" - lead should be connected over "L" - lead, with "L" lead connected to "0" - tap and "R" - lead to tap "09". (The sum of the values between L & R is 0.12)

Step (2c). Recheck Settings.

$Z_1' = TS(1 \pm M) = 1 \times 8.7\ (.88) = 7.65$ and $Z_0' = 1 \times 26.1\ (.88) = 23.0$

$$Z_1 = Z_1' \frac{\text{Sin } 60^\circ}{\text{Sin } 75^\circ} = 7.65 \times .900 = 6.90 \text{ ohms at } 60^\circ$$

$$Z_0 = Z_0^1 \frac{\text{Sin } 60^\circ}{\text{Sin } 75^\circ} = 23.0 \times .900 = 20.7 \text{ ohms at } 60^\circ$$

Zone 2 & 3 Settings

For zone 2 and 3 settings use a procedure similar to that for zone 1 described above. Tables II to V give the required settings.

Note: The S setting must be the same for both the positive and zero-sequence reach.

SETTING THE RELAY

The SDG relays require settings for the four compensators (T_A, T_B, T_C, and T_0), the three auto-transformer primaries (S_A, S_B, and S_C), and the four compensator tertiaries (M_A, M_B, M_C, and M_0). All of these settings are made with taps on the tap plate.

Compensator (T_A, T_B, T_C, T_O, and M_A, M_B, M_C, M_O)

Each set of compensator primary T_A, T_B, T_C, and T_O, taps terminates in inserts which are grouped on a socket and form approximately three-quarters of a circle around a center insert which is the common connection for all of the taps. Electrical connections between common insert and tap inserts are made with a link that is held in place with two connector screws, one in the common and one in the tap. A compensator tap setting is made by loosening the connector screw in the center. Before removing the screw open switches 12 through 19 to bypass the current around the relay. Remove the connector screw in the tap end of the link, swing the link around until it is in position over the insert for the desired tap setting, replace the connector screw to bind the link to this insert, and retighten the connector screw in the center. Since the link and connector screws carry operating current, be sure that the screws are turned to bind snugly. Compensator secondary tap connections are made through two leads identified as L and R for each compensator. These leads come out of the tap plate each through a small hole, one on each side of the vertical row of "M" tap inserts. The lead connectors are held in place on the proper tap by connector screws.

Values for which an "M" setting can be made are from -.18 to +.18 in steps of .03. The value of a setting is the sum of the numbers that are crossed when going from the R lead position to the L lead position. The sign of the "M" value is determined by which lead is in the higher position on the tap plate. The sign is positive (+) if the L lead is higher and negative (-) if the R lead is higher.

An "M" setting may be made in the following manner. Remove the connector screws so that the L and R leads are free. Refer to Table II through Table V to determine the desired "M" value. Neither lead connector should make electrical contact with more than one tap at a time.

Line Angle Adjustment

Maximum sensitivity angle is set for 75° (current lagging voltage) in the factory. This adjustment need not be disturbed for line angles of 65° or higher. For line angles below 65° set for 60° maximum sensitivity angle by adjusting the compensator loading resistors R_1, R_2, R_3, R_4. Refer to repair calibration under "Maximum Torque Angle Adjustment," when a change in maximum sensitivity angle is desired.

TABLE II
.2-4.35 OHMS RELAY RANGE
PREFERRED ZONE 1 IMPEDANCE SETTINGS

POSITIVE SEQUENCE (Z_1') S=1								ZERO SEQUENCE (Z_0') S=1								M		CONNECT		
T	.230	.307	.383	.537	.69	.92	1.23	T_0	.69	.921	1.15	1.61	2.07	2.76	3.69	+M	-M	"R" LEAD TO TAP	"L" LEAD TO TAP	
	.272	.362	.452	.632	.815	1.09	1.45		.815	1.09	1.36	1.90	2.44	3.26	4.40	+.18		.06	0	
	.264	.352	.441	.617	.794	1.06	1.41		.794	1.06	1.32	1.85	2.38	3.18	4.25	+.15		.06	.03	
	.258	.344	.430	.601	.772	1.03	1.38		.772	1.03	1.29	1.80	2.32	3.10	4.15	+.12		.09	0	
	.251	.335	.418	.585	.754	1.00	1.34		.754	1.00	1.25	1.76	2.26	3.00	4.04	+.09		.09	.03	
	.244	.325	.405	.570	.732	.975	1.30		.732	.975	1.22	1.71	2.20	2.92	3.92	+.06		.06	.09	"L" OVER "R"
	.237	.316	.396	.555	.710	.950	1.27		.710	.950	1.18	1.66	2.13	2.84	3.80	+.03		.03	0	
	.230	.307	.383	.537	.69	.920	1.23		.69	.921	1.15	1.61	2.07	2.76	3.69	0	0	0	0	
	.223	.298	.370	.520	.670	.892	1.19		.670	.892	1.12	1.56	2.00	2.68	3.58		-.03	0	.03	
	.216	.288	.360	.505	.650	.865	1.15		.650	.865	1.08	1.52	1.95	2.60	3.46		-.06	.09	.06	
	.209	.280	.348	.488	.627	.840	1.12		.627	.840	1.05	1.47	1.88	2.51	3.36		-.09	.03	.09	
	.202	.270	.336	.472	.607	.810	1.08		.607	.810	1.01	1.42	1.82	2.43	3.25		-.12	0	.09	
	.195	.260	.324	.456	.587	.782	1.05		.587	.782	.980	1.37	1.76	2.35	3.14		-.15	.03	.06	
	.188	.252	.314	.440	.565	.755	1.01		.565	.755	.940	1.32	1.70	2.26	3.02		-.18	0	.06	"R" OVER "L"

TABLE III
.2-4.35 OHM RELAY RANGE
PREFERRED ZONE 2 & 3 IMPEDANCE SETTINGS

POSITIVE SEQUENCE SETTINGS (Z_1') S=2								S=3		ZERO SEQUENCE SETTINGS (Z_0') S=2								S=3		M		CONNECT		
T	.230	.307	.383	.537	.69	.92	1.23	.92	1.23	T_0	.69	.921	1.15	1.61	2.07	2.76	3.69	2.76	3.69	+M	-M	"R" LEAD TO TAP	"L" LEAD TO TAP	
	.544	.724	.905	1.26	1.63	2.17	2.90	3.26	4.40		1.63	2.17	2.72	3.80	4.90	6.50	8.70	9.80	13.1	+.18		.06	0	"L" OVER "R"
	.528	.704	.880	1.23	1.59	2.12	2.82	3.18	4.25		1.59	2.12	2.65	3.70	4.76	6.35	8.48	9.55	12.7	+.15		.06	.03	
	.516	.688	.860	1.20	1.55	2.06	2.76	3.10	4.15		1.55	2.06	2.58	3.60	4.65	6.20	8.25	9.30	12.4	+.12		.09	0	
	.502	.670	.835	1.17	1.51	2.00	2.68	3.00	4.04		1.51	2.00	2.50	3.50	4.52	6.00	8.05	9.05	12.1	+.09		.09	.03	
	.488	.650	.810	1.13	1.46	1.95	2.60	2.92	3.92		1.46	1.95	2.44	3.41	4.40	5.85	7.80	8.80	11.8	+.06		.06	.09	
	.474	.632	.790	1.10	1.42	1.90	2.53		3.80		1.42	1.90	2.37	3.32	4.26	5.70	7.60	8.53	11.4	+.03		.03	0	
	.460	.614	.766	1.07	1.38	1.84	2.46		3.69		1.38	1.84	2.30	3.22	4.14	5.52	7.38	8.28	11.1	0	0	0	0	
	.446	.596	.740	1.04	1.34	1.78	2.40		3.58		1.34	1.78	2.24	3.12	4.02	5.35	7.15	8.03	10.7		-.03	0	.03	"R" OVER "L"
	.432	.576	.716	1.01	1.30	1.73	2.32		3.46		1.30	1.73	2.16	3.02	3.90	5.16	6.94	7.80	10.4		-.06	.09	.06	
	.418	.560	.695	.975	1.25	1.67	2.24		3.36		1.25	1.67	2.09	2.94	3.78	5.00	6.70	7.55	10.1		-.09	.03	.09	
	.404	.540	.674	.940	1.21	1.62	2.17				1.21	1.62	2.02	2.83	3.66	4.85	6.50	7.30	9.8		-.12	0	.09	
	.390	.520	.650	.910	1.17	1.56	2.10				1.17	1.56	1.95	2.74	3.55	4.67	6.27	7.05	9.4		-.15	.03	.06	
	.376	.504	.625	.880	1.13	1.50	2.08				1.13	1.50	1.79	2.64	3.40	4.50	6.05	6.80	9.1		-.18	0	.06	

TABLE IV
1.1-31 OHMS RELAY RANGE
PREFERRED ZONE 1 IMPEDANCE SETTINGS

POSITIVE SEQUENCE (Z_1') S=1								ZERO SEQUENCE (Z_0') S=1								M		CONNECT		
																		"R" LEAD TO TAP	"L" LEAD TO TAP	
T	1.2	1.5	2.1	3.0	4.5	6.3	8.7	T_0	3.6	4.5	6.3	9.0	13.5	18.9	26.1	+M	-M			
	1.42	1.77	2.48	3.54	5.3	7.45	10.2		4.25	5.30	7.45	10.6	15.9	22.2	30.8	+.18		.06	0	"L" OVER "R"
	1.38	1.73	2.42	3.45	5.17	7.25	10.0		4.15	5.17	7.25	10.4	15.5	21.7	30.0	+.15		.06	.03	
	1.34	1.68	2.36	3.36	5.04	7.05	9.75		4.05	5.04	7.05	10.1	15.1	21.2	29.3	+.12		.09	0	
	1.31	1.64	2.29	3.27	4.90	6.89	9.50		3.94	4.90	6.89	9.81	14.7	20.6	28.4	+.09		.09	.03	
	1.27	1.59	2.22	3.18	4.77	6.70	9.25		3.82	4.77	6.70	9.54	14.3	20.0	27.7	+.06		.06	.09	
	1.24	1.55	2.16	3.09	4.64	6.50	8.95		3.71	4.64	6.50	9.27	13.9	19.5	26.9	+.03		.03	0	
	1.20	1.5	2.10	3.00	4.50	6.30	8.70		3.6	4.50	6.30	9.0	13.5	18.9	26.1	0	0	0	0	
	1.16	1.45	2.04	2.91	4.36	6.10	8.45		3.50	4.36	6.10	8.73	13.1	18.3	25.2		-.03	0	.03	"R" OVER "L"
	1.13		1.97	2.82	4.23	5.90	8.15		3.38		5.90	8.46	12.7	17.7	24.5		-.06	.09	.06	
	1.09		1.91	2.73	4.10	5.74	7.90		3.27		5.74	8.19	12.3	17.2	23.7		-.09	.03	.09	
	1.06		1.85	2.64	3.96	5.55	7.65		3.16		5.55	7.92	11.9	16.6	23.0		-.12	0	.09	
	1.02		1.77	2.55	3.82	5.35			3.06		5.35	7.65	11.5	16.0			-.15	.03	.06	
	0.99				3.69				2.95				11.1				-.18	0	.06	

TABLE V
1.1-31 OHMS RELAY RANGE
PREFERRED ZONE 2 & 3 IMPEDANCE SETTINGS

POSITIVE SEQUENCE SETTINGS (Z_1') S=2							S=3		ZERO SEQUENCE SETTINGS (Z_1') S=2								S=3		M		CONNECT		
T	1.2	1.5	2.1	3.0	4.5	6.3	8.7	6.3	8.7	T_0	3.6	4.5	6.3	9.0	13.5	18.9	26.1	18.9	26.1	+M	-M	"R" LEAD TO TAP	"L" LEAD TO TAP	
	2.84	3.54	4.96	7.08	10.62	14.9	20.5	22.3	30.8		8.50	10.6	14.9	21.2	31.8	44.5	61.5	66.6	92.5	+.18		.06	0	"L" OVER "R"
	2.76	3.46	4.84	6.90	10.35	14.5	20.0	21.6	30.0		8.30	10.34	14.5	20.7	31.0	43.5	60.0	65.1	90.0	+.15		.06	.03	
	2.68	3.36	4.72	6.72	10.08	14.1	19.5	21.2	29.3		8.10	10.08	14.1	20.2	30.2	42.4	58.5	63.6	87.5	+.12		.09	0	
	2.62	3.28	4.58	6.54	9.81	13.8	19.0		28.4		7.88	9.80	13.8	19.6	29.4	41.2	56.8		85.2	+.09		.09	.03	
	2.54	3.18	4.44	6.36	9.54	13.4	18.5		27.7		7.64	9.54	13.4	19.1	28.6	40.0	55.3		83.0	+.06		.06	.09	
	2.48	3.10	4.32	6.18	9.27	13.0	17.9		27.0		7.42	9.28	13.0	18.5	27.8	39.0	53.8		80.5	+.03		.03	0	
	2.4	3.0	4.20	6.0	9.0	12.6	17.4		26.1		7.20	9.0	12.6	18.0	27.0	37.8	52.2		78.3	0	0	0	0	
	2.32	2.90	4.08	5.82	8.73	12.2	16.9		25.2		7.00	8.72	12.2	17.5	26.2	36.6	50.5		75.8		-.03	0	.03	"R" OVER "L"
	2.26		3.95	5.64	8.46	11.8	16.3		24.5		6.76		11.8	16.9	25.4	35.4	49.0		73.5		-.06	.09	.06	
	2.18		3.82	5.46	8.19	11.5	15.8		23.7		6.54		11.5	16.4	24.6	34.4	47.5		71.0		-.09	.03	.09	
	2.12		3.70	5.28	7.92	11.1	15.3		23.0		6.32		11.1	15.8	23.8	33.2	45.8		68.8		-.12	0	.09	
	2.04		3.54	5.10	7.65	10.7			22.7		6.12		10.7	15.3	23.0	32.0					-.15	.03	.06	
	1.98				7.38						5.90				22.2						-.18	0	.06	

INSTALLATION

The relays should be mounted on switchboard panels or their equivalent in a location free from dirt, moisture, excessive vibration and heat. Mount the relay by means of the mounting stud for the type FT projection case or by means of the four mounting holes on the flange for the semi-flush type FT case. Either the stud or the mounting screws may be utilized for grounding the relay. The electrical connections may be made directly to the terminals by means of screws for steel panel mounting or to the terminal stud furnished with the relay for thick panel mounting. The terminal stud may be easily removed or inserted by locking two nuts on the stud and then turning the proper nut with a wrench.

For detailed information on the FT case refer to I.L. 41-076.

EXTERNAL CONNECTIONS

Figure 22 shows typical connection for single zone protection using an SDG relay.

ACCEPTANCE TEST

Acceptance tests consists of:

1. A visual inspection.
2. "Push-Button" - check.
3. An electrical test to make certain that the relay measures the balance point impedance accurately.

1. Visual Inspection

Give a visual check to the relay to make sure there are no loose connections, broken resistors or broken wires.

Set Relay as follows:

.2-4.35 ohm relay	1.0-31.0 ohm relay
all T = 1.23	all T = 8.7
T_0 = 3.69	T_0 = 26.1
all S = 1	all S = 1
all M = +.15	all M = +.15

2. Push-Button Check

Using the test connections of Fig. 23. Connect the a-c voltages as per test no. 1. No current connections are required. Connect the rated d-c voltages as shown. Open circuit the connections to terminal no. 7. Set $V_{BN} = V_{CN} = 70$ Volts. Depress the white pushbutton. The pushbutton should light. If the pushbutton does not light, connect a d-c voltmeter or a 25 watt lamp as per Fig. 23. The voltmeter should have a minimum deflection of at least 5 volts. If there is a deflection but the lamp does not light this indicates a fault in the pushbutton circuit. If there is no indication proceed with the electrical test to isolate the fault in the pushbutton circuit or the relay.

3. Electrical Tests

Distance Unit

Tripping is indicated for the SDG relay when the 25 watt lamp shown on Fig. 23 turns on and for SDG-1, -2, -3, & -4 relays when DC voltmeter indicates a minimum deflection of 5 volts for balance point condition. Refer to Fig. 23 for all test connections.

For .2-4.35 ohm relay

A. Use connections for test No. 5 and set V_{AN} voltage = 20 volts. $V_{BN} = V_{CN} = 70$ volts. Set the phase shifter for 75° current lagging voltage.

B. The relay current required to make the trip should be between 8.0 - 8.6 amp.

C. Use connections for Test No. 6 and set V_{BN} voltage = 20 volts. $V_{AN} = V_{CN} = 70$ volts. Set the phase shifter as above. The relay trip current should be 8.0 - 8.6 amps.

D. Use connections for Test No. 7 and set V_{CN} = 20 volts $V_{AN} = V_{BN} = 70$ volts. Set the phase shifter as above. The SDG relay trip current should be 8.0 - 8.6 amp.

For 1.0-31.0 ohm relay

A. Use connections for test #5 and set $V_{AN} = V_{BN} = V_{CN} = 70$ volts. Set phase shifter for 75° current lagging voltage. The relay trip current should be 3.95-4.20 amperes.

B. Use connections for test #6 and set $V_{AN} = V_{BN} = V_{CN} = 70$ volts, and set the phase shifter as above. The relay trip current should be 3.95-4.20 amperes.

C. Use test connections for test #7 and set $V_{AN} = V_{BN} = V_{CN} = 70$ volts. Set the phase shifter as above. The relay trip current should be 3.95-4.20 amperes.

If the electrical response is outside the limits a more complete series of tests outlined in the section titled "Calibration" may be performed to determine which component is faulty or out of calibration.

If it is desired to check relay respnse at some other settings use following equation for the trip value of current.

$$I = \frac{3V_{LN}}{(2+p)\,Z_1}, \quad \text{Where } p = \frac{Z_0}{Z_1}$$

Z_0 = Zero sequence reach

Z_1 = Positive sequence reach (in above cases p = 3)

WARNING If testing requires trip current over 15 amp. over prolonged periods, it is recommended that a heavy short lead be connected from terminal 19 to the center tap of T_0-socket. Also connect a jumper lead from terminal 16 to terminal 1 on the large printed circuit board for SDG-1 and SDG-3 relays and terminal 2 to terminal 4 for SDG-relay on the large printed circuit board. (Lower set of terminals rear view).

Overcurrent Unit

Check operation of the overcurrent unit by using test connection #5 of the Fig. 23. Set $V_{AN} = 0$, $V_{BN} = V_{CN} = 70$ volts. The .2-4.35 ohm relay should operate at .75-.83 ampere, and the 1-31.0 ohms relay should operate at .37-.420 amperes.

Indicating Contactor Switch (ICS) (SDG only)

With the SDG relay tripped, pass sufficient d-c current through the trip circuit to close the contacts of the ICS. This value of current should be not less than 1.0 ampere or greater than 1.2 amperes, for the 1 ampere ICS. The current should not be greater than the particular ICS tap setting being used for the 0.2-2.0 ampere ICS. The operation indicator target should drop freely.

The contact gap should be approximately 0.047" for the 0.2-2.0 ampere unit and 0.070" for the 1.0 ampere unit between the bridging moving contact and the adjustable stationary contacts. The bridging moving contact should touch both stationary contacts simultaneously.

ROUTINE MAINTENANCE

The relays should be inspected periodically, at such time intervals as may be dictated by experience, to insure that the relays have retained their calibration and are in proper operating condition.

"In-Service" Test (If relay is set for S=1 only)

In service testing is performed as follows:

1. Open relay trip circuit by opening red opening red handle switch No. 11.

2. Open relay voltage terminal 7.

3. Press white pushbutton. Pushbutton light should light.

This test checks out the operation of the magnitude comparator and output circuitry.

REPAIR CALIBRATION

Use the following procedure for calibrating the relay if the relay has been taken apart for repairs or the adjustments disturbed.

For easier access to the parts, the relay should be tested without the case.

Part A Preliminary Settings

1. To set resistors loosen the adjustable band and carefully move the band to a different setting. Retighten the band so not to damage resistance wires. Set R9, R10, R11 resistors (located in front) using the following procedure:

   a) Remove the printed circuit board (s) (PCB) in the rear of the relay.

   b) Using a bridge type instrument, set the adjustable band next to the fixed terminal having the wire connection to measure 1600 ($\pm$ 35) ohms

   c) Set the second adjustable band from the same fixed terminal to measure a total 6000 ($\pm$ 100) ohms.

2. Set R_1-R_2-R_3-R_4 potentiometers fully counter-clockwise for maximum resistance.

3. Set relay for S=1, M=+18 ("L" lead over "R" lead), all T=8.7, T_0=26.1 for the 1.0-31.0 ohm relays and for the .2-4.35 ohms relay all T=1.23 and T_0=3.69.

Part B Voltage Circuit Tests

1. Apply 3 phase balanced voltages as per test 1 of Fig. 23, except no current is applied.

2. Set $V_{AN} = V_{BN} = V_{CN}$ = 70 volts a-c. Measure following a-c voltages:

From relay terminal 6 to S_A = 1 Tap	70	($\pm$1) volts
From relay terminal 6 to S_A = 2 Tap	140	($\pm$2) volts
From relay terminal 6 to S_A = 3 Tap	221	($\pm$3) volts
From relay terminal 6 to R_A lead	40.2	($\pm$5) volts

   Repeat the same measurements for S_B, S_C, and R_B, R_C-leads.

3. Disconnect R_0-lead from M_0=0 Tap and measure the voltage from relay terminal "4" to the R_0-lead. It should be below 0.5 volts ac.

4. Apply rated d-c voltage to the relay. Check the d-c voltage across the lower set of plug-in terminals (rear view) "5" and "1" for the SDG-1, -2, -3, & -4 relays and terminals "6" and "4" for the SDG-relay. It should measure 20 ($\pm$2) volts. (Notice 250 V. d-c relay requires external resistor).

5. Plug in the lower and upper boards.

Part C Potentiometer Adjustments

NOTE: All potentiometers are the lockedtype and should be unlocked before adjustment and locked after adjustment is complete.

1. Set R1, R2, R3, R4, R5, R6, R7, R8 for maximum setting (counter-clockwise).

3. Measure the voltages with a Rectox type voltmeter across the specified terminals of the small upper terminal board located in the rear. All the following measurements are done on the small upper board. Terminal numbers refer to this board only.

R5-Adjustment

Measure the voltage across terminals 2 & 3. Adjust R5 until voltages across 4 & 2 and 4 & 3 are equal (± .1 volt) to each other and are within 1.0 volt of voltage across 2 & 3.

R6-Adjustment

Measure the voltage across terminals 6 & 8. Adjust R6 until voltages across terminals 7 & 6 and 7 & 8 are equal (± .1 volt) to each other and are within 1.0 volt of voltage across 6 & 8.

R-7 Adjustment

Measure the voltage across terminals 17 & 18. Adjust R7 until voltages across terminals 15 & 18 and 15 & 17 are equal (± 0.1 volt) to each other and are within 1.0 volt of voltage across 17 & 18.

R8-Adjustment

Reduce V_{AN} to zero and measure the voltage across terminals 11 & 12. Adjust R8 until voltages across terminals 14 & 11 and 14 & 12 are equal (± 0.1 volt) to each other and are within 1.0 volt of voltage across 11 & 12.

Disconnect all L-leads.

Maximum Torque Angle Adjustment

R-1 Adjustment

For the 1.0-31.0 ohm relay use the # 1 test connection of Fig. 23. Apply 5.5 amp. a-c current to the relay. Set V_{AN} = 10 volts and $V_{BN} = V_{CN}$ = 70 volts. Set the phase shifter for 75° current lagging voltage.

For .20-4.35 ohm relay use the same procedure as above except set the current for 11 amp. and V_{AN} = 3.0 volts.

Insert an a-c voltmeter of 0-3 volts range between relay terminal #6 and the upper M_A tap marked ".06". Adjust R1-potentiometer for a minimum ("null"-reading) and lock R1 in place.

R2-Adjustment

Use #2 test connections of Fig. 23. Set V_{BN} = 10 volts and V_{AN} = V_{CN} = 70 volts. Set I_B=5.5 amps. 75° lagging V_{BN}. (Modify voltage and current settings for the .2-4.35 ohm relay as above). Measure the voltage between relay terminal #6 and the upper M_B tap marked ".06". Adjust R2-potentiometer for a minimum ("null"-reading) and lock R2 in place.

R3-Adjustment

Use the #3 test connections of Fig. 23. Set V_{CN} = 10 volts and V_{AN} = V_{BN} = 70 volts. I_C=5.5 amp. 75° lagging V_{CN}. (Modify voltage and current for the .2-4.35 ohm relay as above).

Measure the voltage between relay terminal #6 and the upper M_C-Tap marked ".06". Adjust R3-potentiometer for a minimum ("null"-reading) and lock R3 in place.

R4-Adjustments

Use the #4 test connections of Fig. 23. Connect all "L"-leads back. Set V_{CN}=0 and V_{AN} = V_{BN} = 70 volts. Set I_C = 5.5 amp. 75° lagging V_{CN}. (For the .2 to 4.35 relay set V_{CN}=0 and V_{BN} = V_{AN} = 30 volt. I_C=8 amperes). Measure the voltage between R_0 and the lowest M_0-tap marked "0". Adjust the R-4 potentiometer for minimum voltage ("null"-reading) and lock R4 in place.

Part D M-Taps Check

Use a Rectox type voltmeter

For 1.0-31.0 ohm relay M_A-Taps - Use test connection #1 of Fig. 23. Pass 10 amp. current through the relay. The voltage should read the following:

1.73 (± .1 volts) between "0" tap and ".03" tap
7.0 (± .1 volts) between "0" tap and ".09" tap
10.5 (± .1 volts) between "0" tap and ".06" tap

M_B-Taps - Use test connection #2 and repeat above.

M_C-Taps - Use test connection #3 and repeat above.

M_0-Taps - Use test connection #4 and repeat above.

For .2-4.35 ohm relay

NOTE: Provide a jumper from terminal 19 to center tap of the T_0 tap block for the SDG, SDG-1, & -3 relays.

M_A-Taps - Use test connection #1 of Fig. 23. Pass 20 amp. of current through relay. The voltage should read the following:

.50 (± .05 volts) between "0" tap and ".03" tap
2.0 (± .1 volts) between "0" tap and ".09" tap
3.0 (± .1 volts) between "0" tap and ".06" tap

M_B-Taps - Use test connection #2 and repeat above.

M_C-Taps - Use test connection #3 and repeat above.

M_O-Taps - Use test connection #4 and repeat above.

Part E Impedance Tests

Tripping is indicated for the SDG relay when the 25 watt lamp shown on Fig. 23 turns on and for SDG-1, -2, -3, & -4 relays when DC voltmeter indicates minimum deflection of 5 volts for balance point condition. Refer to Fig. 23 for all test connections.

For .2-4.35 ohm relay

A Use connections for test No. 5 and set V_{AN} voltage = 20 volts. $V_{BN} = V_{CN} = 70$ volts. Set the phase shifter for 75° current lagging voltage.

B. The relay current required to make the trip should be between 8.0-8.6 amp.

C. Use connections for Test No. 6 and set V_{BN} voltage = 20 volts. $V_{AN} = V_{BN} = 70$ volts. Set the phase shifter as above. The SDG relay trip current should be 8-8.6 amp.

D. Use connections for Test No. 7 and set V_{CN} = 20 volts. $V_{AN} = V_{BN} = 70$ volts. Set the phase shifter as above. The SDG relay trip current should be 8.0-8.6 amp.

For 1.0-31.0 ohm relay

A. Use connections for test #5 and set $V_{AN} = V_{BN} = V_{CN} = 70$ volts. Set phase shifter for 75° current lagging voltage. The relay trip current should be 3.95-4.20 amperes.

B. Use connections for test #6 and set $V_{AN} = V_{BN} = V_{CN} = 70$ volts, and set the phase shifter as above. The relay trip current should be 3.95-4.20 amperes.

C. Use test connections for test #7 and set $V_{AN} = V_{BN} = V_{CN} = 70$ volts. Set the phase shifter as above. The relay trip current should be 3.95-4.20 amperes.

If it is desired to check relay response at some other settings use following equation for the trip value of current.

$$I = \frac{3V_{LN}}{(2+p)\,Z_1}, \qquad \text{Where } p = \frac{Z_0}{Z_1}$$

Z_0 = Zero sequence reach

Z_1 = Positive sequence reach
(in above cases p = 3)

WARNING If testing requires trip current over 15 amp. over prolonged periods, it is recommended that a heavy short lead be connected from terminal 19 to the center tap of T_0-socket. Also connect a jumper lead from terminal 16 to terminal 1 on the large printed circuit board for SDG-1 and SDG-3 relays and terminal 2 to terminal 4 for SDG-relay. (Lower set of terminals rear view).

Change all the S-setting to S=3 and repeat the impedance test. Trip current for the 1.0-31.0 ohm relay should be 2.66-2.87 amp. and 1.3-1.40 amp. for the .2-4.35 ohm relay.

Overcurrent Unit

Check operation of the overcurrent unit by using test connection #5 of Fig. 23. Set $V_{AN} = 0$, $V_{BN} = V_{CN} = 70$ volts. The .2-4.35 ohm relay should operate at .75-.83 ampere, and the 1-31.0 ohms relay should operate at .37-.42 amperes.

Indicating Contactor Switch

With the relay tripped, pass sufficient d-c current through the trip circuit to close the contacts of ICS. This value of current should be not less than 1.0 ampere, nor greater than 1.2 amperes for the 1 ampere ICS. The current should not be greater than the particular ICS setting being used for the 0.2-2.0 amperes ICS. The operation indicator target should drop freely.

The contact gap should be approximately 0.047" for the 0.2-2.0 ampere unit and 0.070" for the 1.0 ampere unit between the bridging moving contact and the adjustable stationary contacts. The bridging moving contact should touch both stationary contacts simultaneously.

RENEWAL PARTS

Repair work can be done most satisfactorily at the factory. However, interchangeable parts can be furnished to the customers who are equipped for doing repair work. When ordering parts, always give the complete nameplate data, and component style number given in the electrical parts list.

ELECTRICAL PARTS LIST

Circuit Symbol	Description	Westinghouse Style Number
Printed Circuit Board (SDG,-1,-2,-3 & -4) (Fig. 26)		836A776H01
	DIODES	
D1 To D24	B2N9	837A692H04
D37-D38-D62-D67-D70	1N3283	837A692H02
	CONTACT STRIP	187A637H02
Printed Circuit Board (SDG) Fig. 27A)		870B499H01
(SDG-1 & 3) (Fig. 27B)		870B499H02
(SDG-2 & 4) (Fig. 27C)		870B499H03
	CAPACITORS	
C13-C14-C15	.5 MFD.	187A624H03
	DIODES	
D54-D55	1N4385	184A855H14
	RESISTORS	
R52 (125V DC)	2.4K Ohm-$\frac{1}{4}$W.	836A908H72
R56	2.K Ohm-$\frac{1}{4}$W.	629A531H39
R52 (48V DC)	510 Ohm-$\frac{1}{4}$W.	836A908H56
Printed Circuit Board (SDG) (Fig. 28)		411C212H01
	CAPACITORS	
C5-C7	2 MFD.	187A662H07
C6	.25 MFD.	187A624H02
C8-C10-C19-C20	.02 MFD.	187A624H09
C12	2.2 MFD.	187A508H19
C9	.10 MFD.	187A624H01
C11	.68 MFD.	764A278H16
	DIODES	
D40 To D49-D51-D52 D57-D58-D60-D61 D64 To D66-D87	1N4385	184A855H14
D50	M4L2053	629A370H04

ELECTRICAL PARTS LIST

Printed Circuit Board (SDG) (Fig. 28) (Continued) — Westinghouse Style Number: 411C212H01

Circuit Symbol	Description	Westinghouse Style Number
	DIODES	
D29-D30-D32 D33-D35-D36	TW120	837A692H01
D72	CER69	188A342H06
D26-D27	B2N9	837A692H04
D53-D59	1N3283	837A692H02
	TUNNEL DIODES	
TD3	1N3713	836A602H01
TD4-TD5	1N2928	836A602H02
	ZENER DIODES	
Z3	1R200	629A369H01
Z4	1N759A	837A693H01
Z5	1N3805A	185A089H05
	POTENTIOMETER	
R45	1K Ohm-$\frac{1}{4}$W.	629A430H02
	RESISTORS	
R17	100 Ohm-$\frac{1}{2}$W.	629A531H08
R18	56 Ohm-$\frac{1}{2}$W.	629A531H02
R19	1.5K Ohm-$\frac{1}{2}$W.	629A531H36
R20-R21-R46	2.7K Ohm-$\frac{1}{2}$W.	629A531H42
R24	22K Ohm-$\frac{1}{2}$W.	629A531H64
R25-R26	68K Ohm-$\frac{1}{2}$W.	629A531H76
R28	2.7K Ohm-$\frac{1}{2}$W.	629A531H42
R29-R30	39K Ohm-$\frac{1}{2}$W.	629A531H70
R31-R37	470K Ohm-$\frac{1}{2}$W.	629A531H24
R32-R33	1K Ohm-$\frac{1}{2}$W.	629A531H32
R34	6.2K Ohm-$\frac{1}{2}$W.	629A531H51
R36	1.5K Ohm-$\frac{1}{2}$W.	836A503H30
R38	10K Ohm-$\frac{1}{2}$W.	836A503H49
R65	5.6K Ohm-$\frac{1}{2}$W.	629A531H50
R43	1.8K Ohm-$\frac{1}{2}$W.	629A531H38
R48	3.3K Ohm-$\frac{1}{2}$W.	629A531H44
R49	2K Ohm-$\frac{1}{2}$W.	836A503H33
R35-R27	30K Ohm-$\frac{1}{2}$W.	629A531H67
R42	47K Ohm-1W.	629A371H17
R44	1.1K Ohm	1333983
R55	2K Ohm	1333591

ELECTRICAL PARTS LIST

		Westinghouse Style Number
Printed Circuit Board (SDG) (Fig. 28) (Continued)		411C212H01
Circuit Symbol	Description	
	RESISTORS	
R53-R54	2K Ohm-½W.	836A503H33
R57	2K Ohm-1W.	187A643H34
	TRANSISTORS	
Q2-Q5-Q6	2N1132	184A638H20
Q3-Q4-Q7	2N336	184A638H06
Q1-Q8	2N697	184A638H18
	SWITCHES	
QS2-QS3	2N886	185A517H03
	TRANSFORMER	
T1	-	629A453H02
	TEST TERMINALS	
TP1 To TP9	-	187A639H01
	CONTACT STRIP	
	-	187A637H02
	TRANSISTOR RADIATOR	
		188A002H01
Printed Circuit Board (SDG-1) Fig. 29)		411C823H01
(SDG-2)		411C823H02
(SDG-3)		411C833H02
(SDG-4)		411C833H02
	CAPACITORS	
C5	2 MFD.	184A662H07
C6	.10 MFD.	187A624H01
C7-C9-C19-C20	.02 MFD.	187A624H09
C8	.10 MFD.	187A624H01
C10	.68 MFD.	764A278H16
C11	2.2 MFD.	187A508H19

ELECTRICAL PARTS LIST

		Westinghouse Style Number
Printed Circuit Board (SDG-1) (SDG-2) (SDG-3) (SDG-4) (Fig. 29) (Continued)		411C212H01
Circuit Symbol	Description	
	DIODES	
D26-D27	B2N9	837A692H04
D40-D43 To D53-D56-D57-D59 D64 To D66-D87 To D90	1N4385	184A855H14
D72	CER69	188A342H06
D29-D30-D32 D33-D35-D36	TW120	837A692H01
D39-D5	1N3283	837A692H02
	TUNNEL DIODES	
TD1-TD3	1N2928	836A602H02
TD2	1N3713	836A602H01
	ZENER DIODES	
Z3	1N9578	186A797H06
Z4	1N3686B	185A212H06
Z6	1N3805A	185A089H05
Z5		
	POTENTIOMETERS	
R48	1K	629A430H02
	RESISTORS	
R57	2K Ohm-1W.	187A643H34
R17	100 Ohm-$\frac{1}{2}$W.	629A531H08
R18	56 Ohm-$\frac{1}{2}$W.	629A531H02
R30-R65	4.7K Ohm-$\frac{1}{2}$W.	629A531H48
R22-R26	22K Ohm-$\frac{1}{2}$W.	629A531H64
R23	27K Ohm-$\frac{1}{2}$W.	629A531H66
R24	4.7K Ohm-$\frac{1}{2}$W.	629A531H48
R19	1.5K Ohm-$\frac{1}{2}$W.	629A531H36
R28-R37-R38	1K Ohm-$\frac{1}{2}$W.	629A531H32
R31-R32-R51	2.7K Ohm-$\frac{1}{2}$W.	629A531H42

ELECTRICAL PARTS LIST

Circuit Symbol	Description	Westinghouse Style Number
Printed Circuit Board (SDG-1) (SDG-2) (SDG-3) (SDG-4) (Fig. 29) (Continued)		411C212H01
	RESISTORS	
R33-R34	68K Ohm-½W.	629A531H76
R35-R36	39K Ohm-½W.	629A531H70
R39	6.2K Ohm-½W.	629A531H51
R21-R40	30K Ohm-½W.	629A531H67
R41	1.5K Ohm-½W.	836A503H30
R42	470 Ohm-½W.	629A531H24
R43	10K Ohm-½W.	836A503H49
R44	2K Ohm-½W.	836A503H33
R46	47 Ohm-1W.	629A371H17
R47	1.8K Ohm-½W.	629A531H38
R49	3.3K Ohm-½W.	629A531H44
R50	1.1K	1333983
R54-R66	5.6K Ohm-½W.	629A531H50
R55	2K Ohm	1333591
R58-R59	2K Ohm-½W.	836A503H33
	TRANSISTORS	
Q1-Q5-Q7-Q13	2N697	184A638H18
Q2-Q6-Q10-Q11	2N1132	184A638H20
Q8-Q9-Q12	2N336	184A638H06
Q3	2N3391	848A851H01
	SWITCHES	
QS1	2N1881	184A640H08
QS2-QS3	2N886	185A517H03
	TEST TERMINALS	
TP1 To TP12	-	187A639H01
	CONTACT STRIP	
		187A637H02
	TRANSISTOR RADIATOR	
		188A002H01

INDEX TO FIGURES

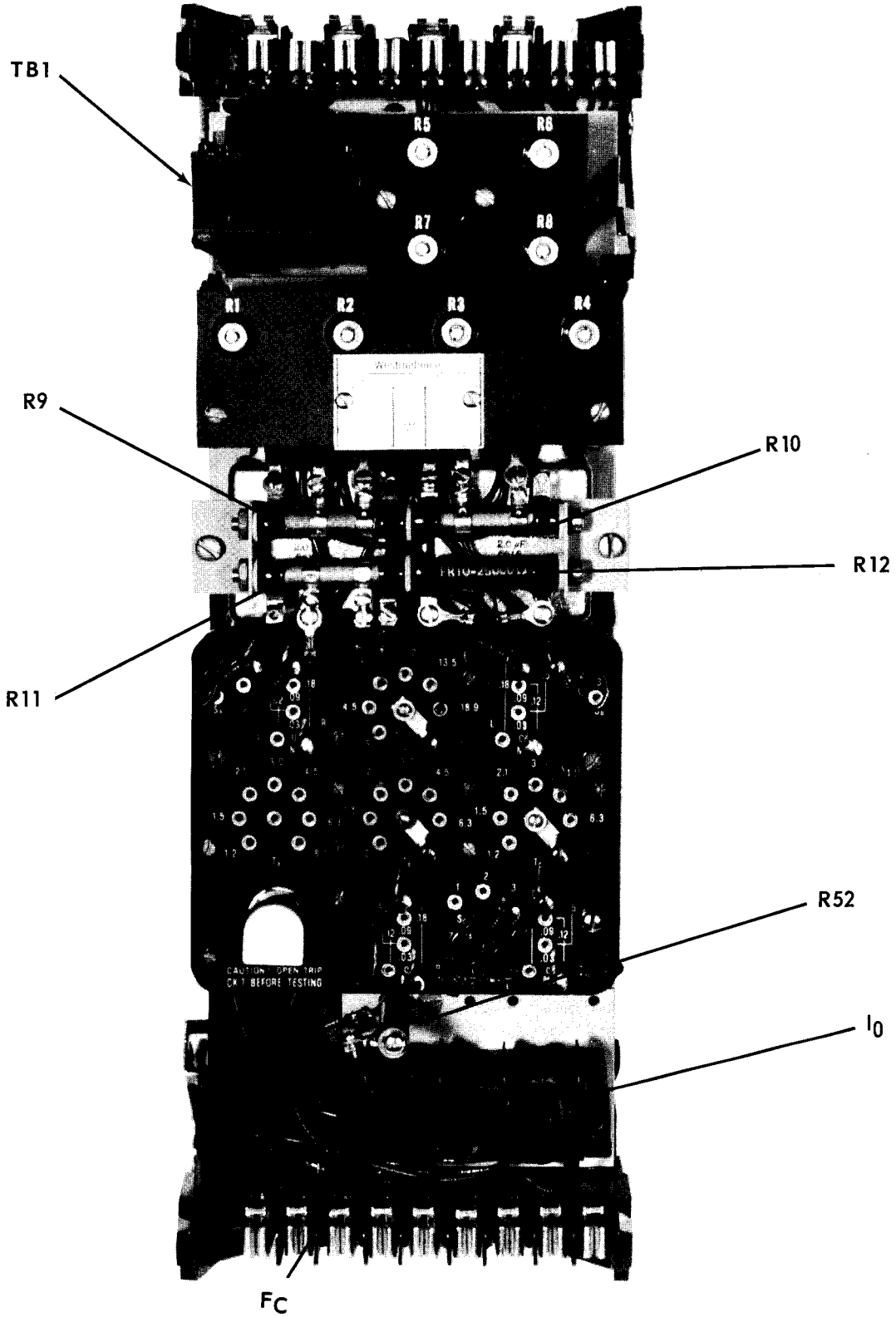


Fig. 1 Type SDG-1 Relay without Case (Front View)

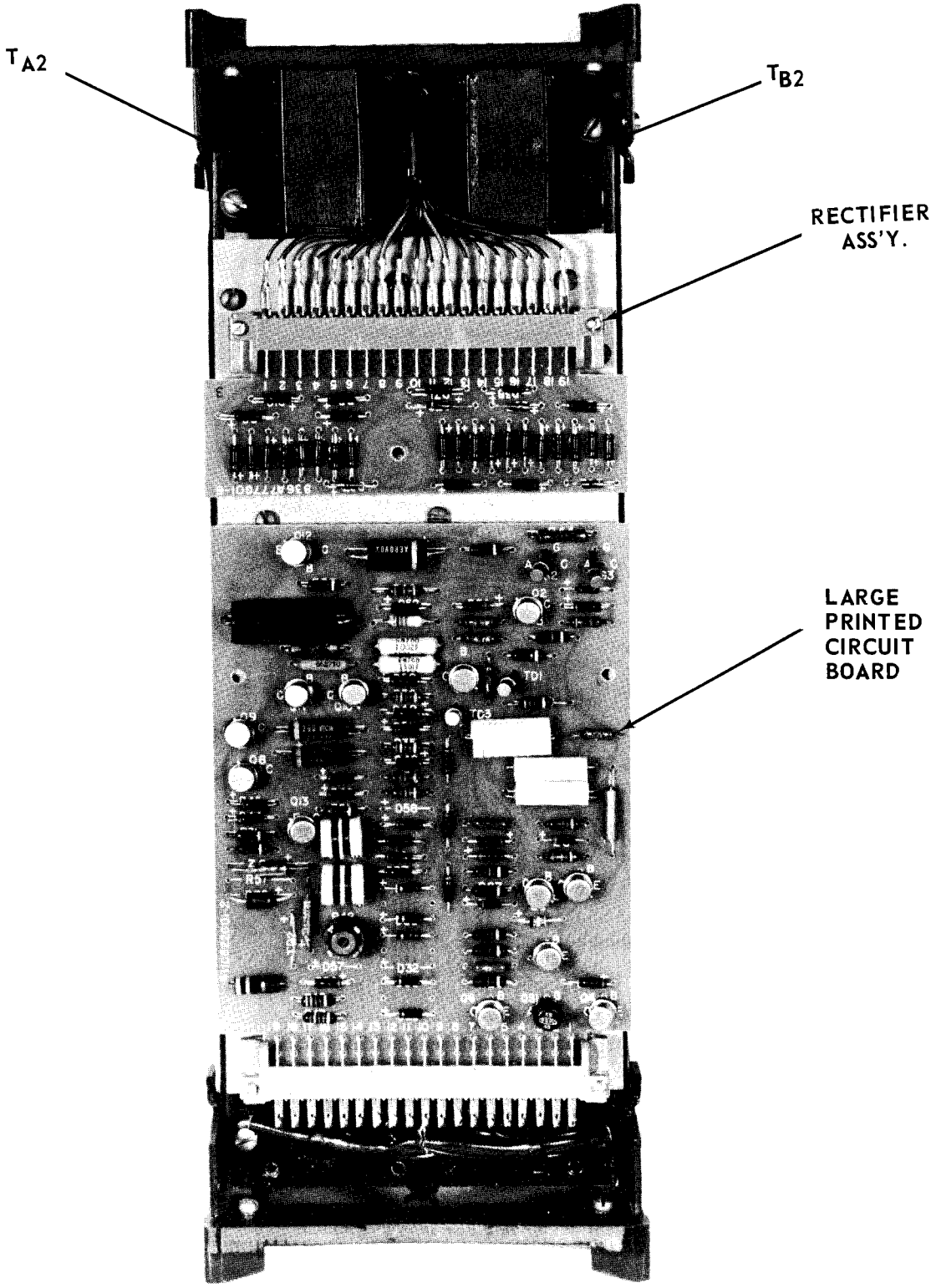


Fig. 2 Type SDG-1 Relay without Case (Rear View)

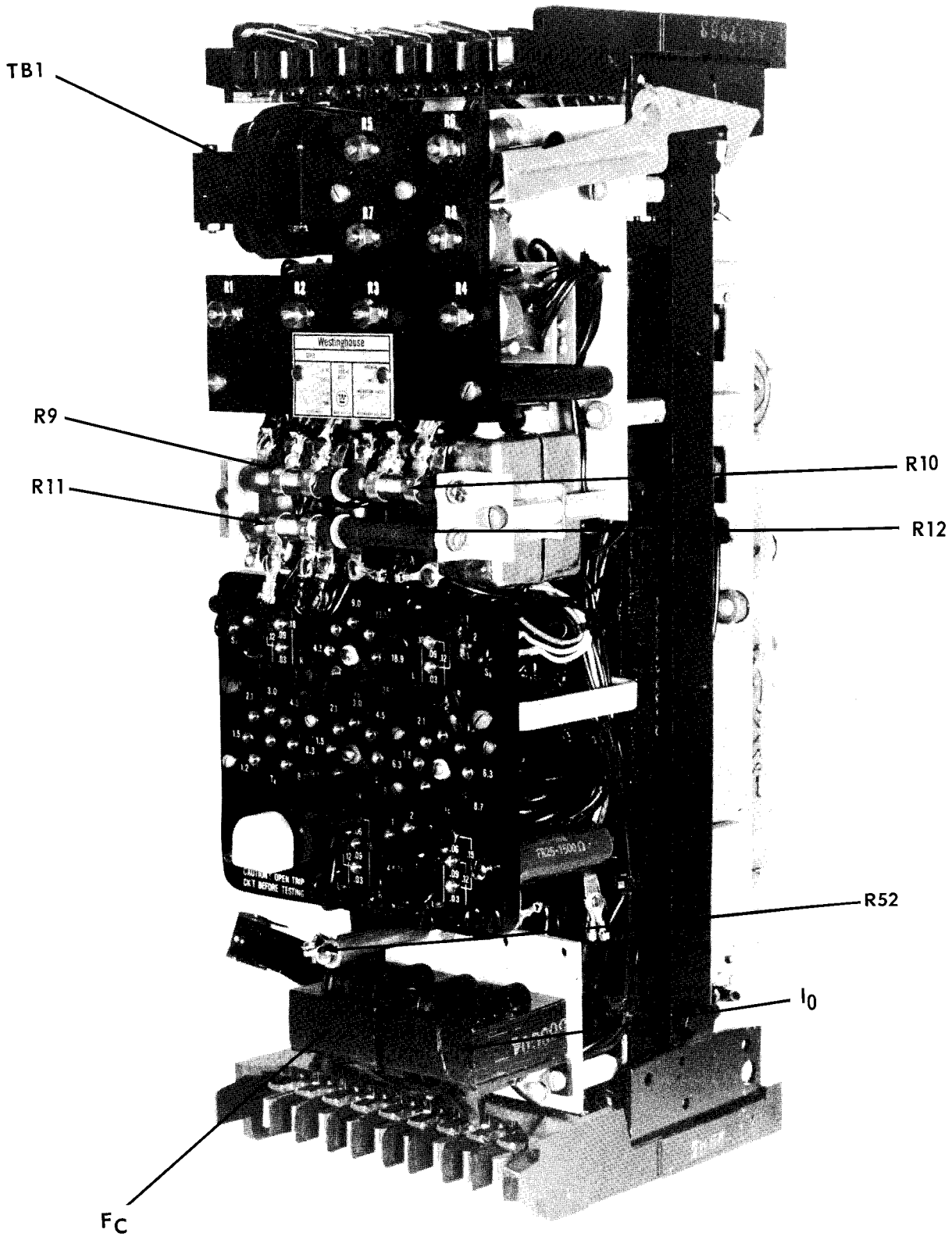


Fig. 3 Type SDG-1 Relay without Case (Side View).

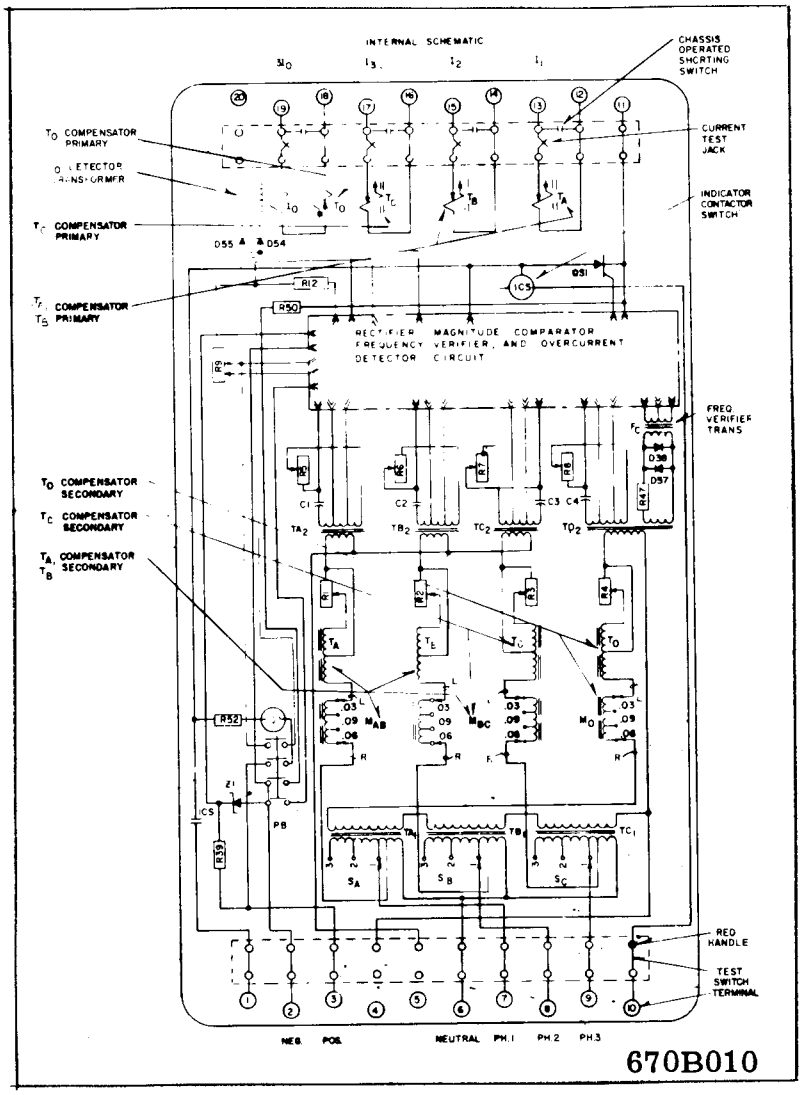


Fig. 4 Internal Schematic of the Type SDG Relay in FT-42 Case

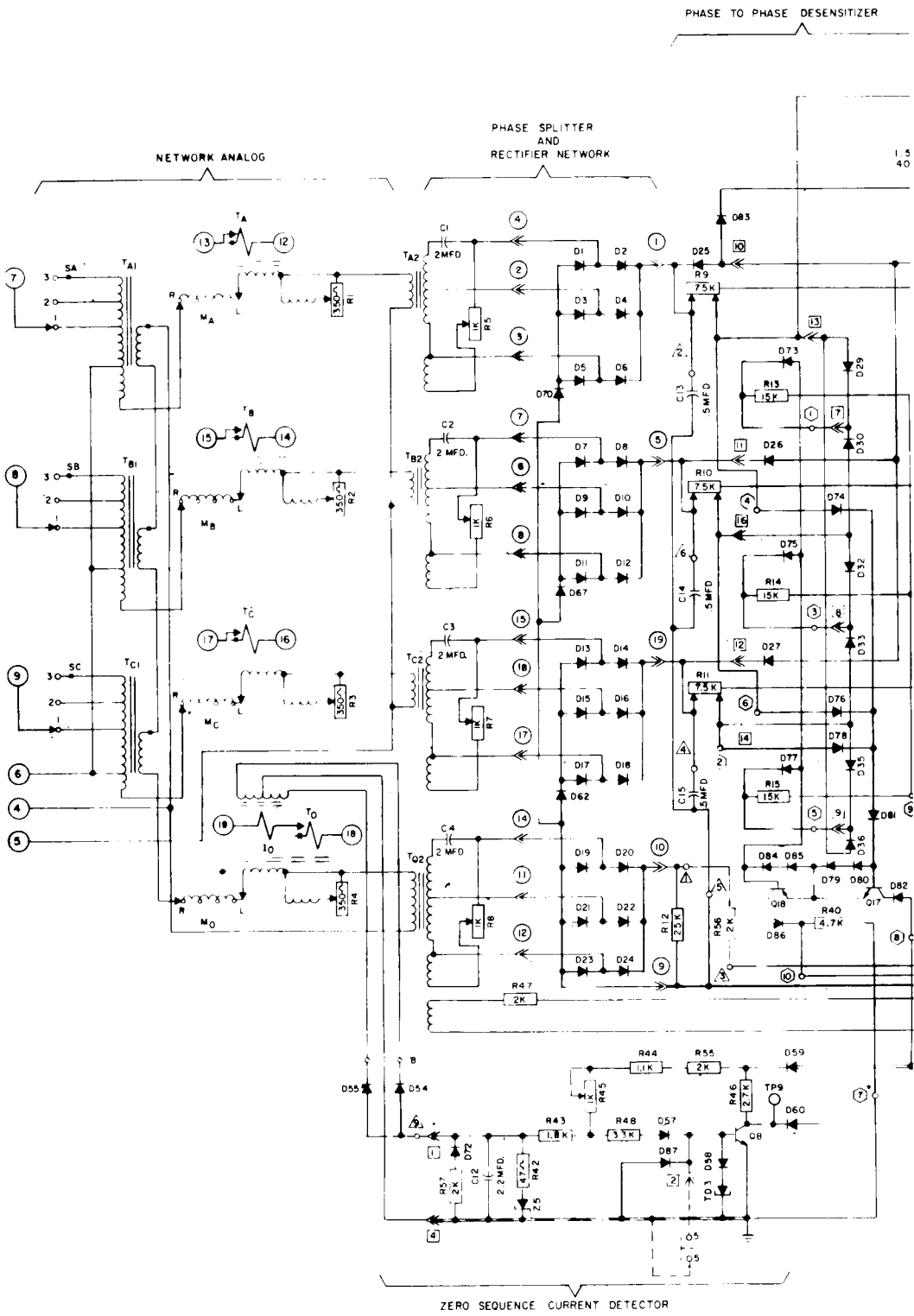


Fig. 5 Detailed Interna

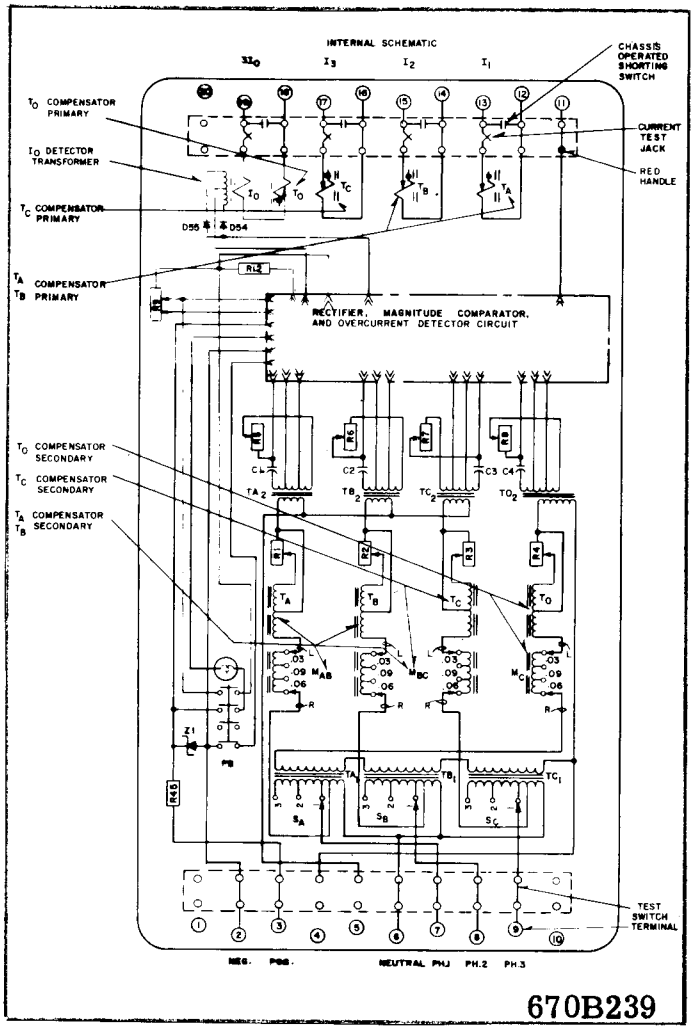


Fig. 8 Internal Schematic of the Type SDG-3 Relay in FT-42 Case

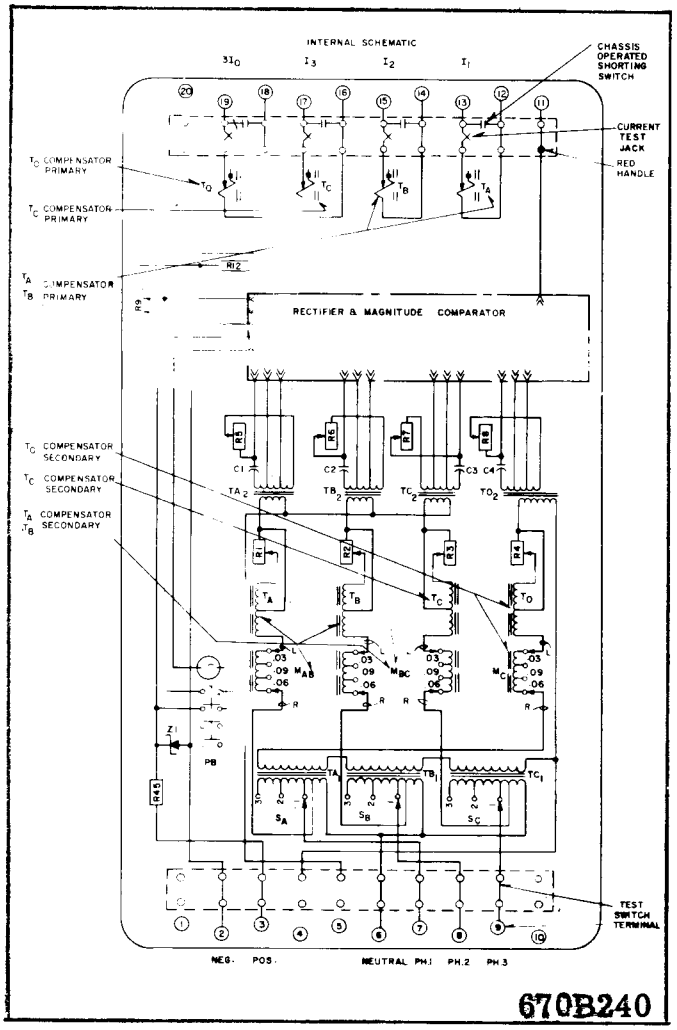
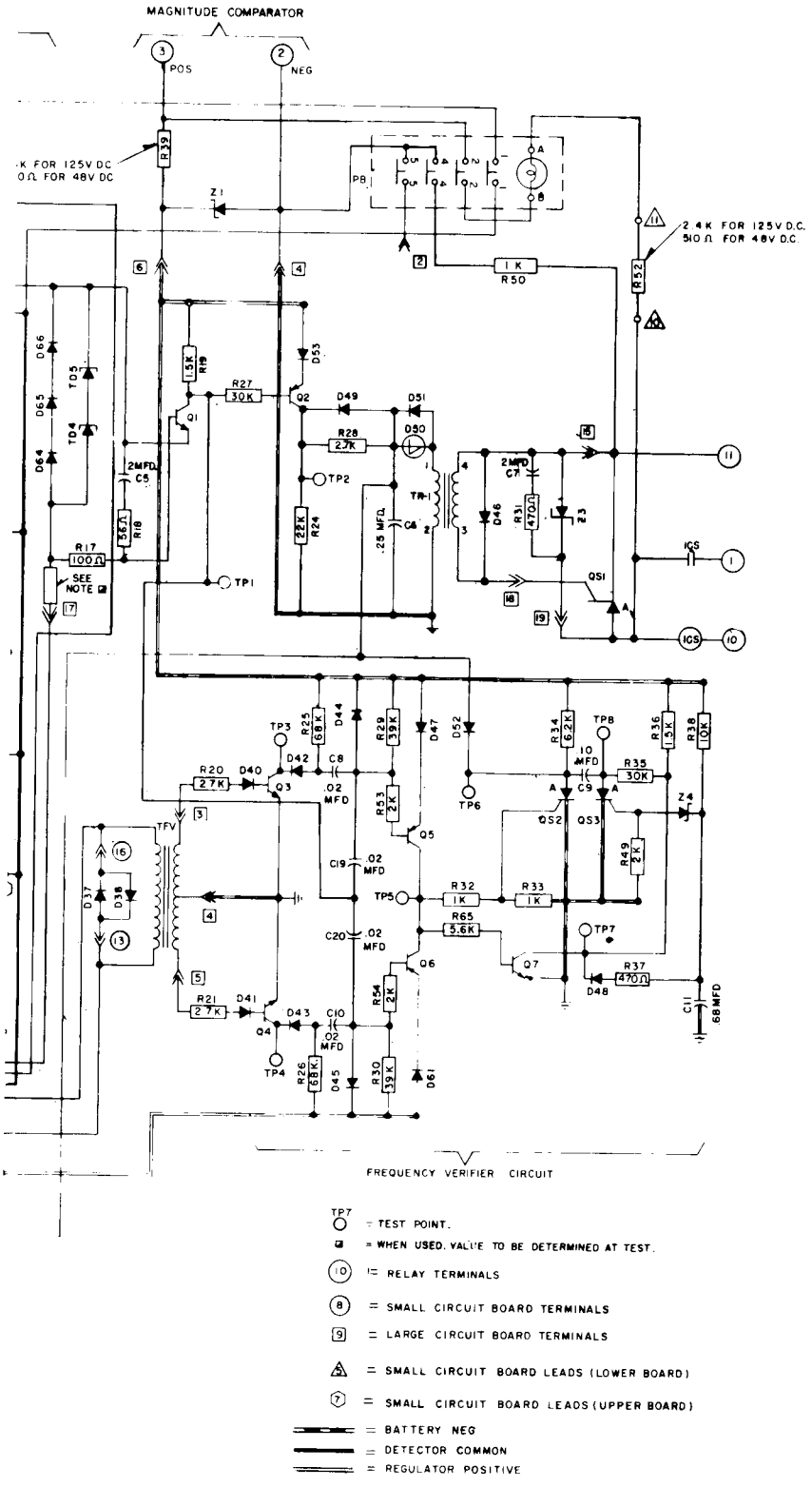


Fig. 9 Internal Schematic of the Type SDG-4 Relay in FT-42 Case



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1 Schematic of SDG Relay

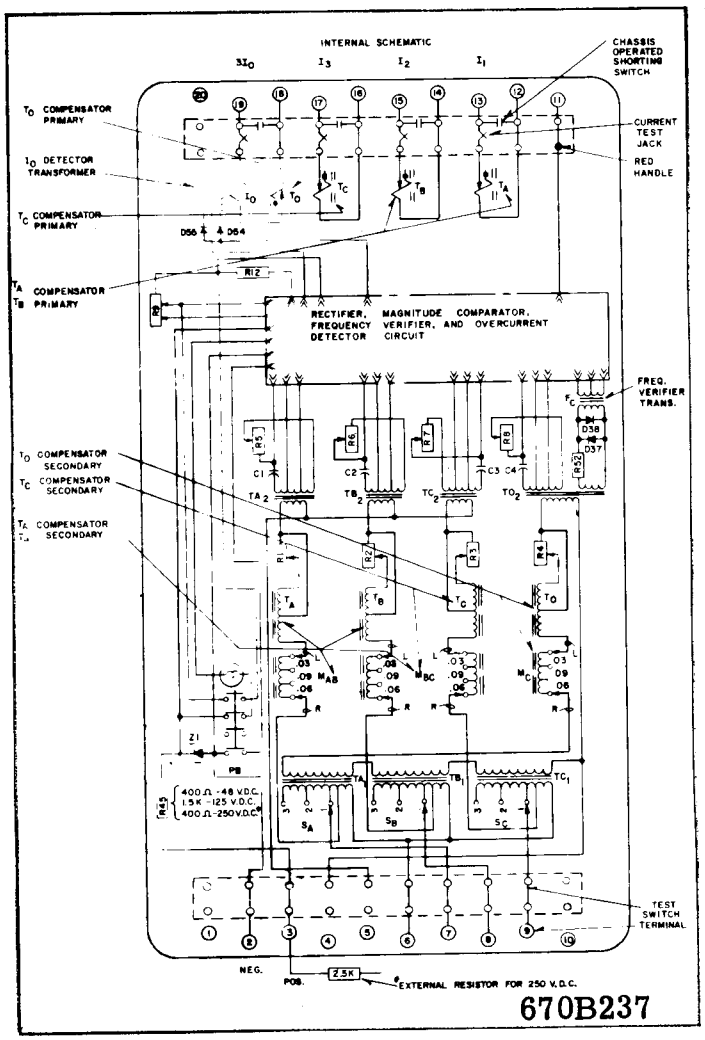


Fig. 6 Internal Schematic of the Type SDG-1 Relay in FT-42 Case

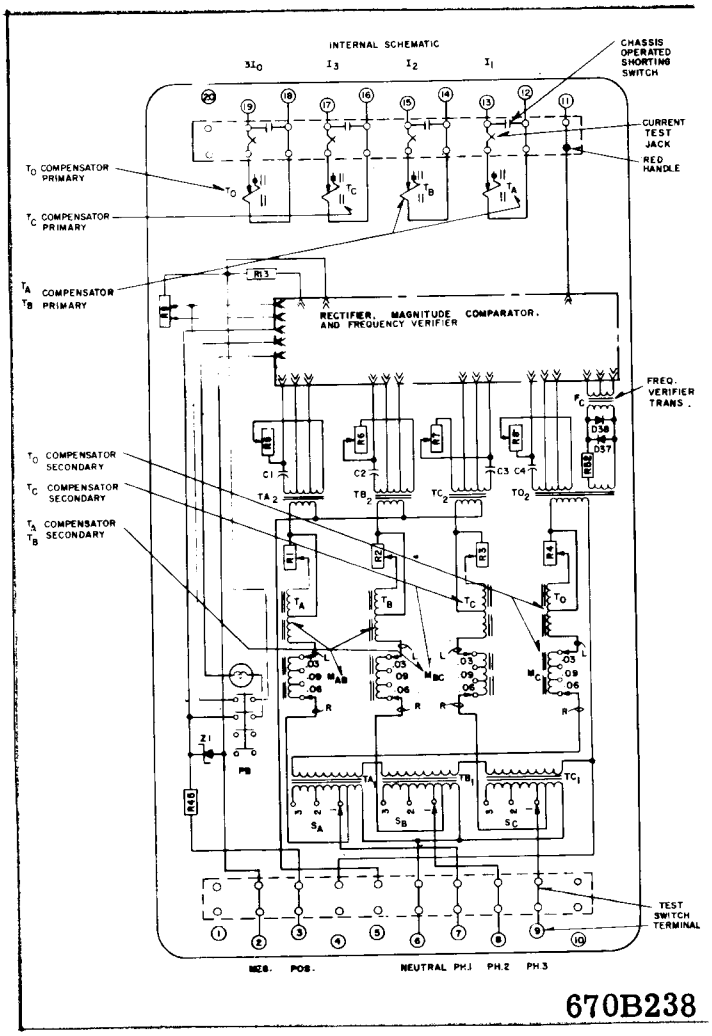


Fig. 7 Internal Schematic of the Type SDG-2 Relay in FT-42 Case

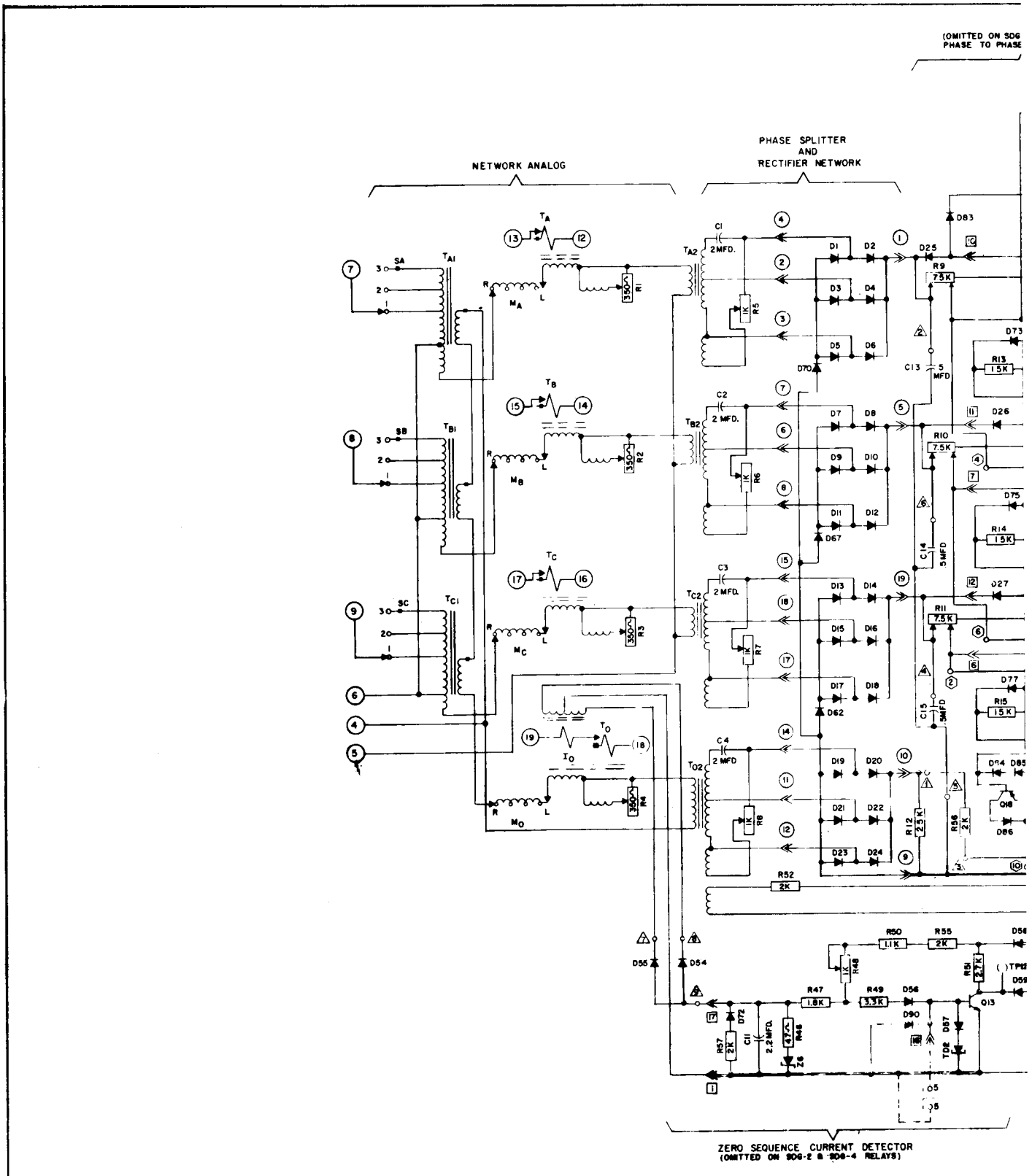


Fig. 10 Detailed Internal Schem

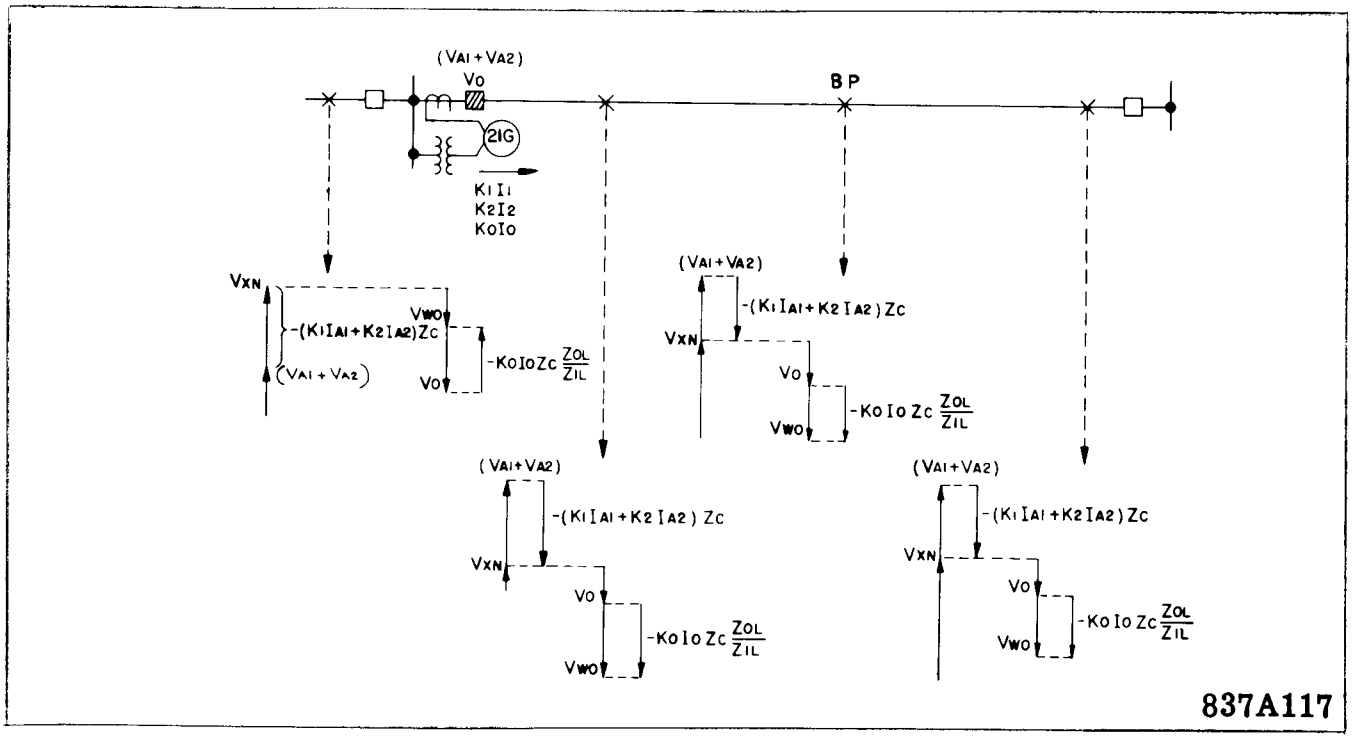


Fig. 14 Relay Voltages for A-to-Ground Faults at Selected Points

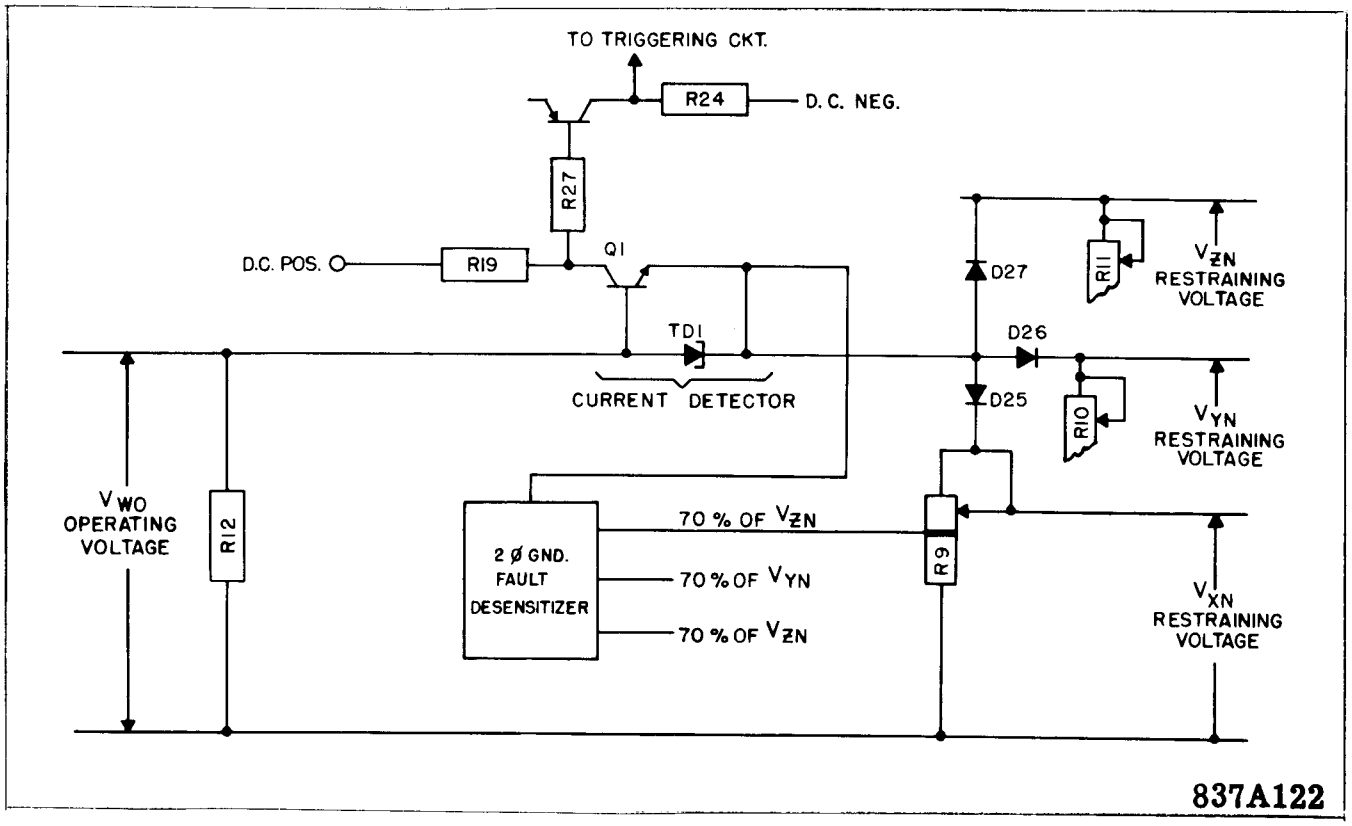
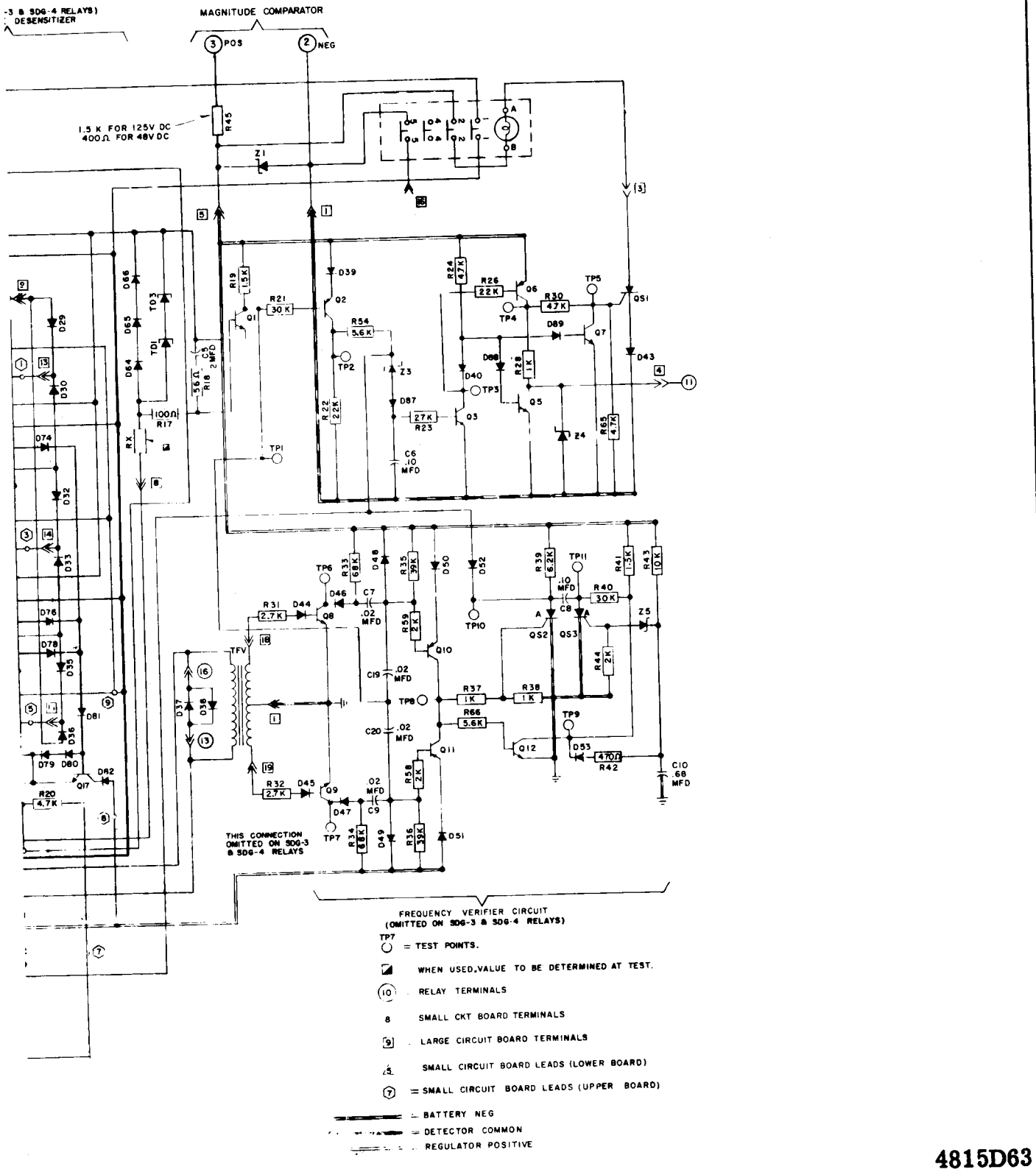


Fig. 15 Magnitude Comparator Circuit



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atic of the SDG-1, 2, 3, & 4 Relays

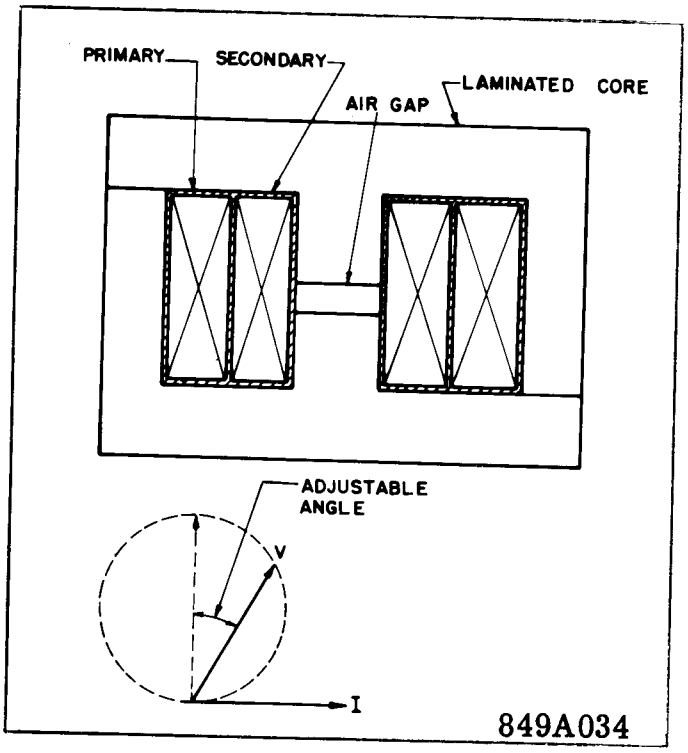


Fig. 11 Compensator Construction

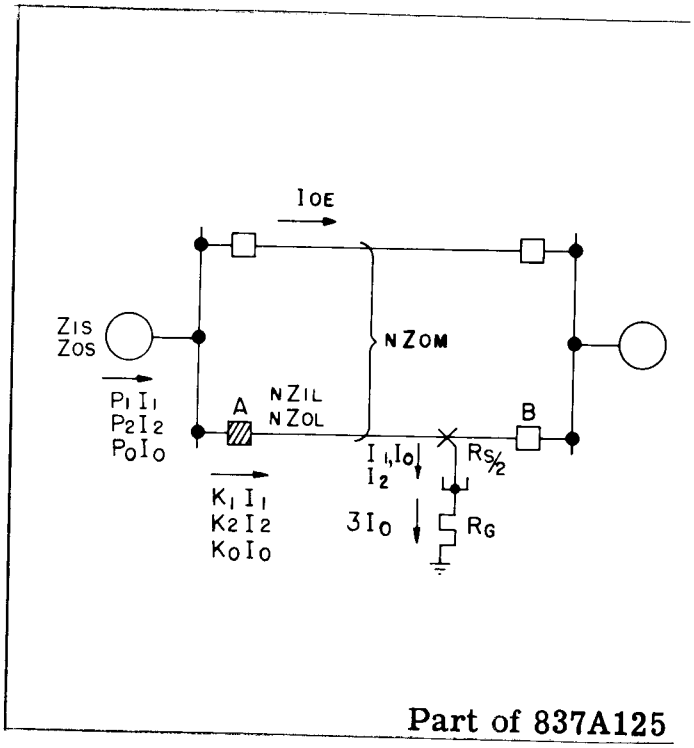


Fig. 12 Definition of Terms

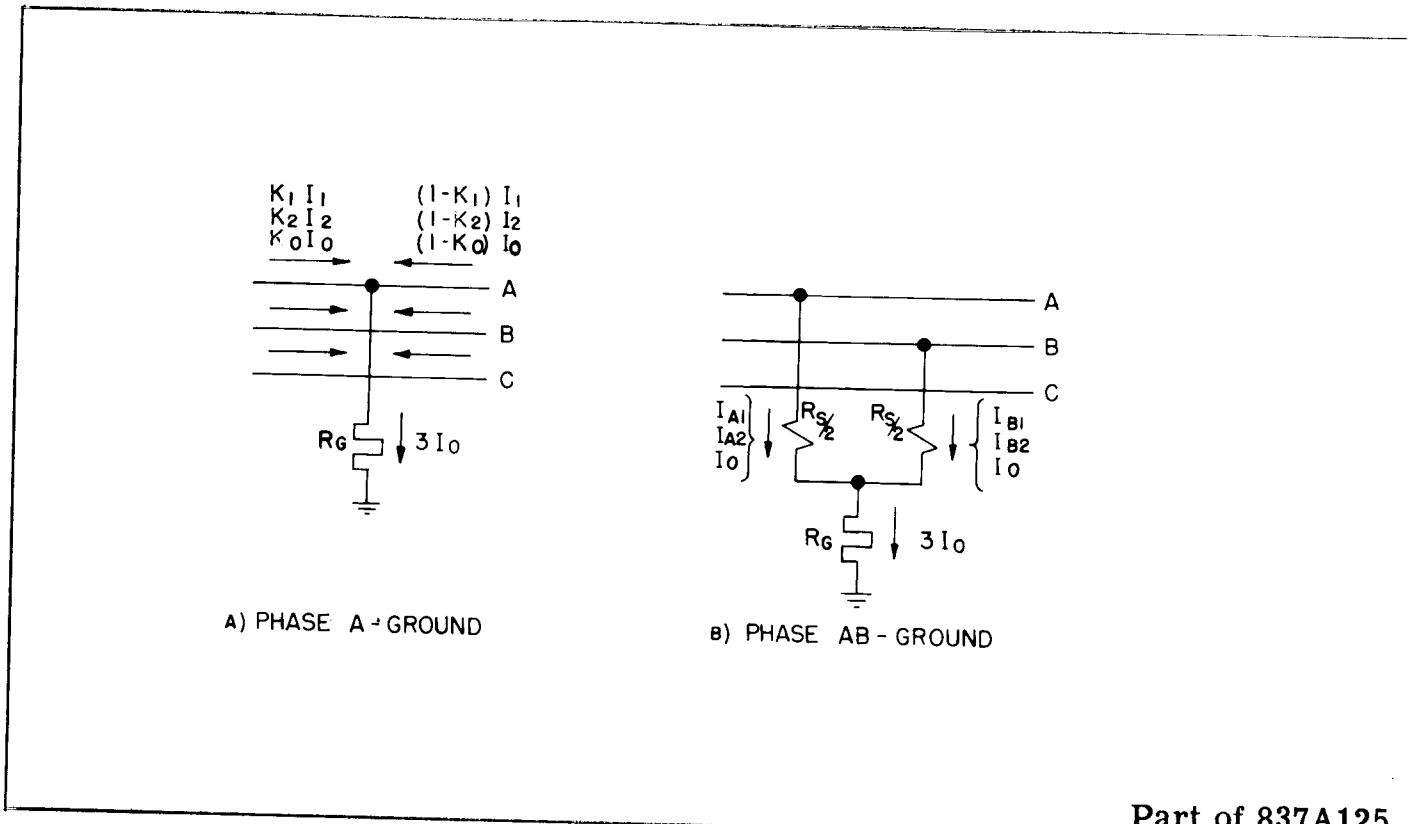


Fig. 13 Fault Resistance

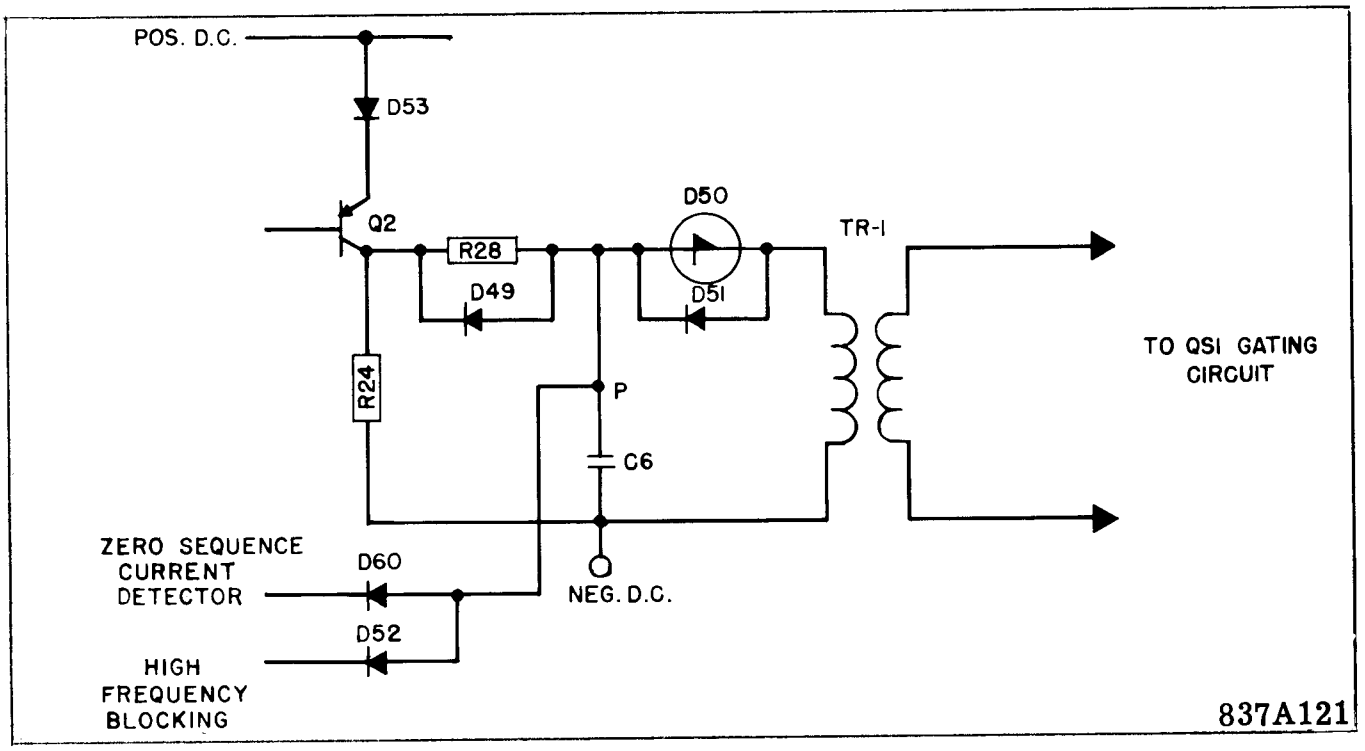


Fig. 16 Triggering Circuit

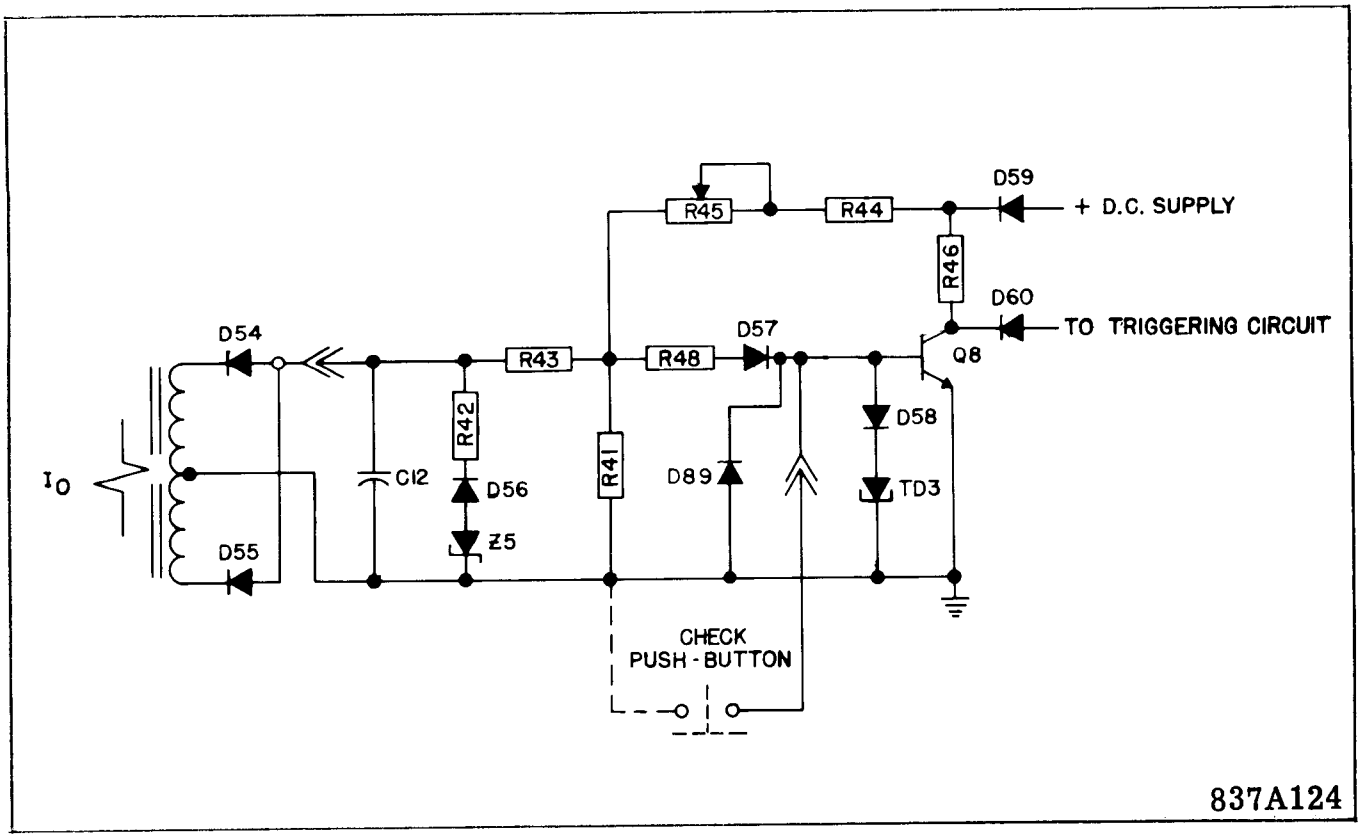


Fig. 17 Zero Sequence Current Detector Circuit

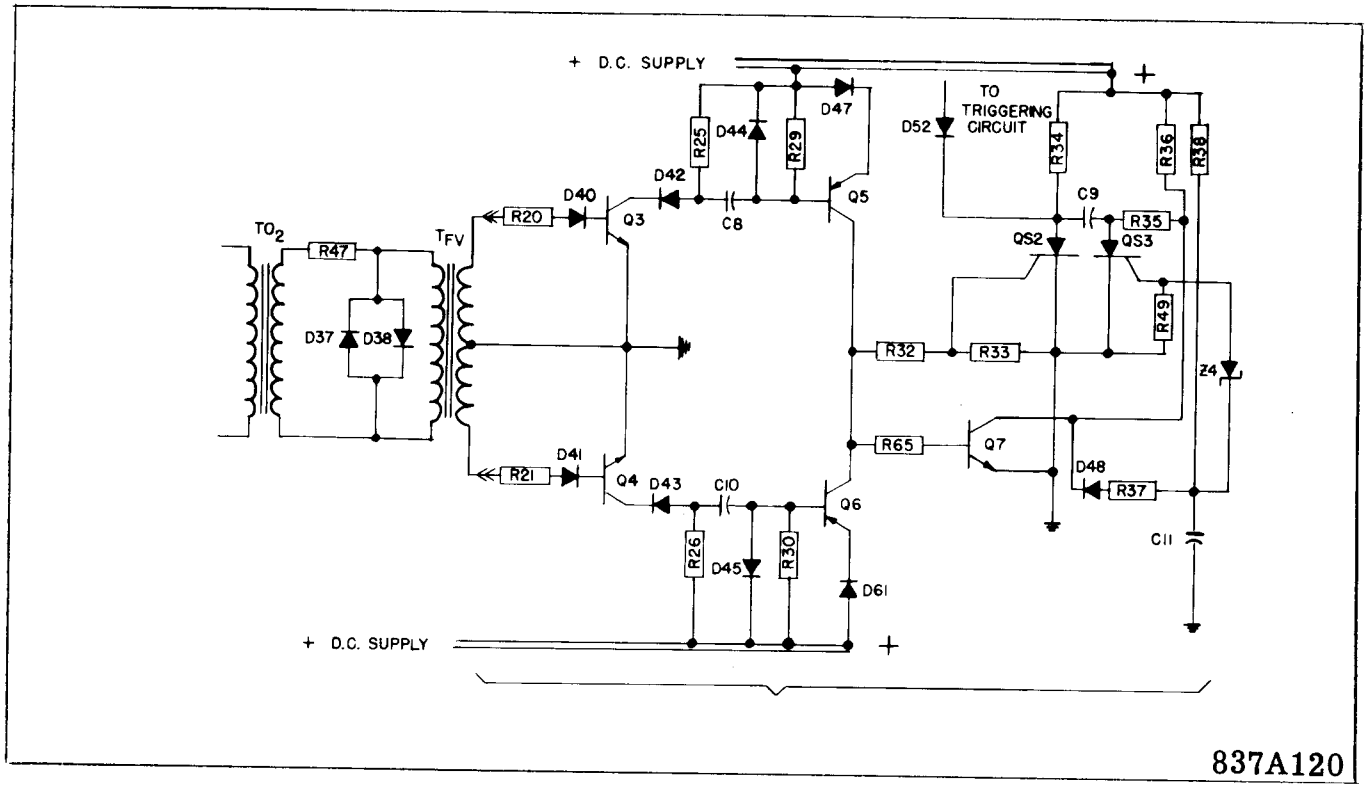


Fig. 18 Frequency Verifier Circuit

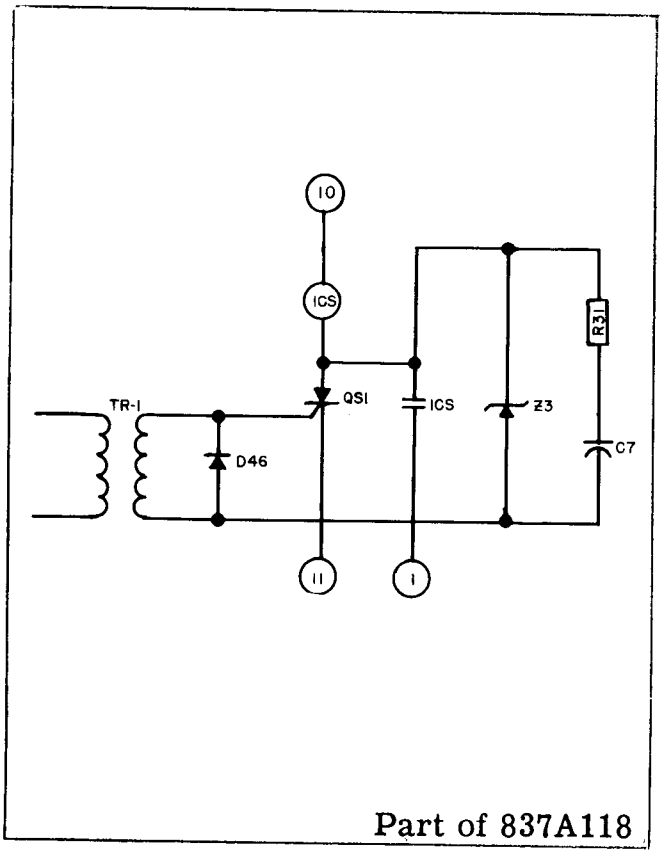


Fig. 19 Output Circuit of the SDG Relay

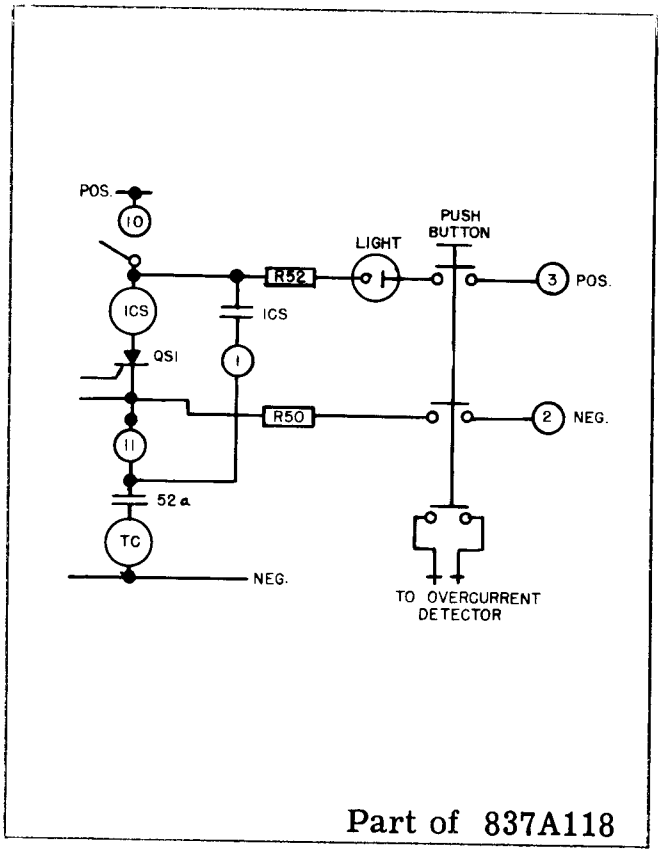


Fig. 20 Push Button "In Service Check" in the SDG Relay

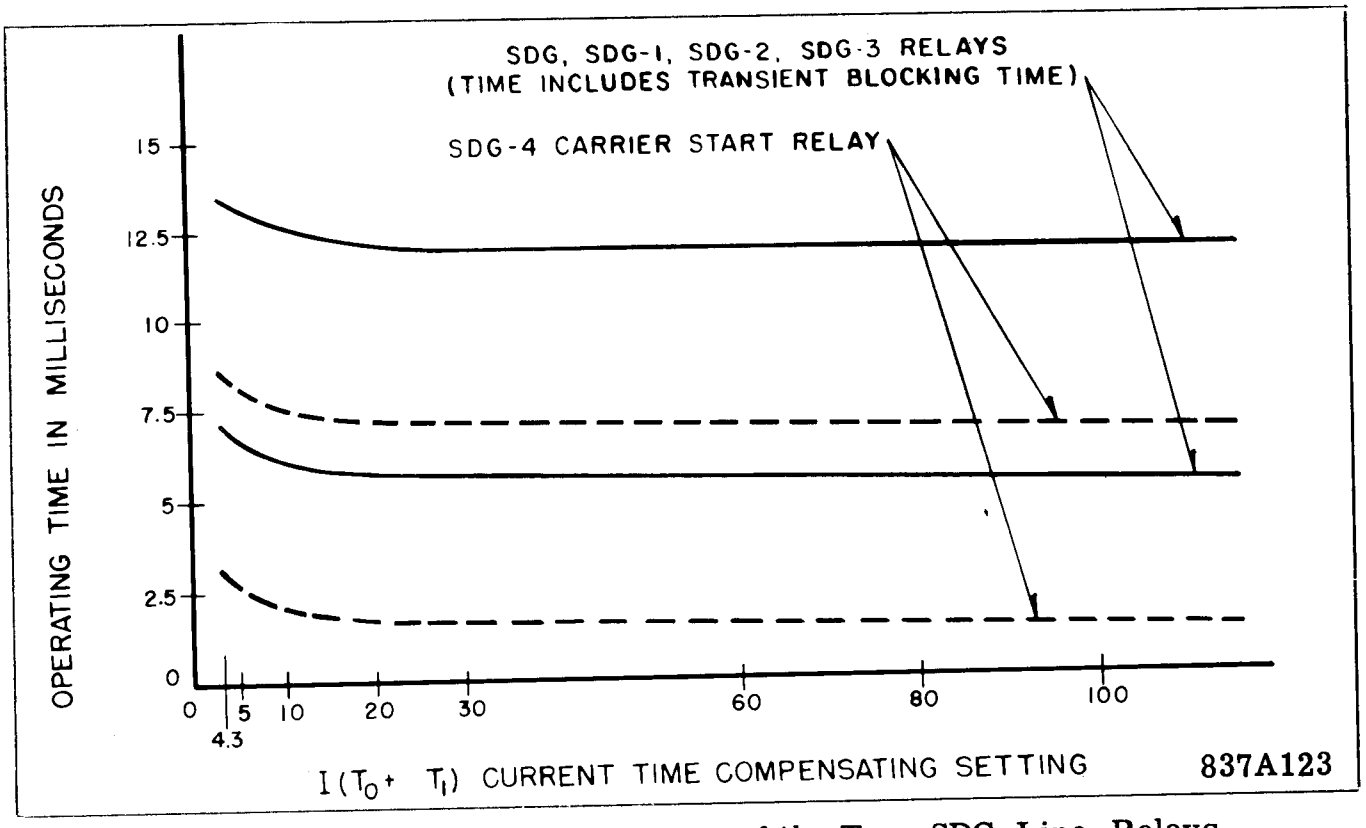


Fig. 21 Typical Operating Time Curves of the Type SDG-Line Relays

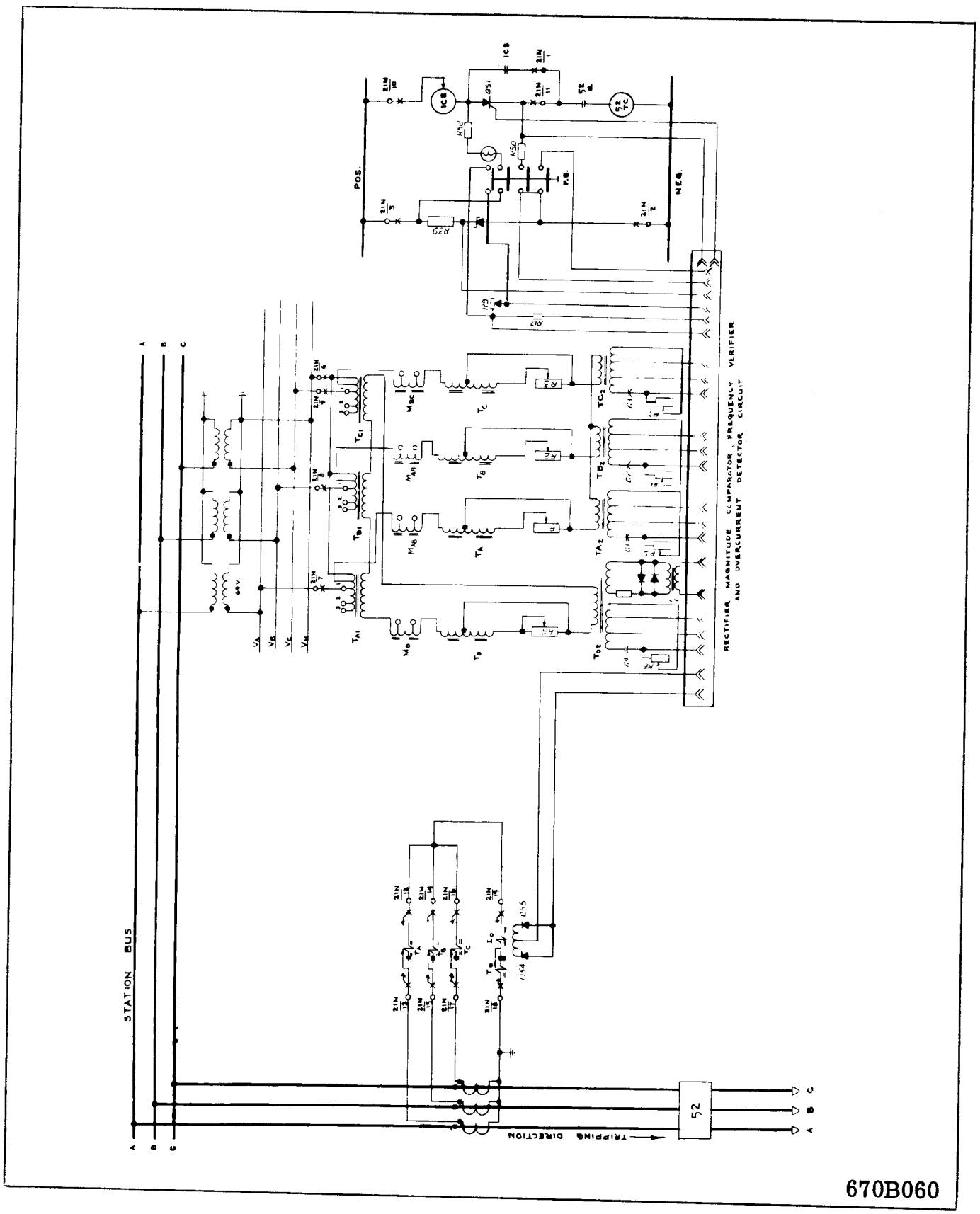
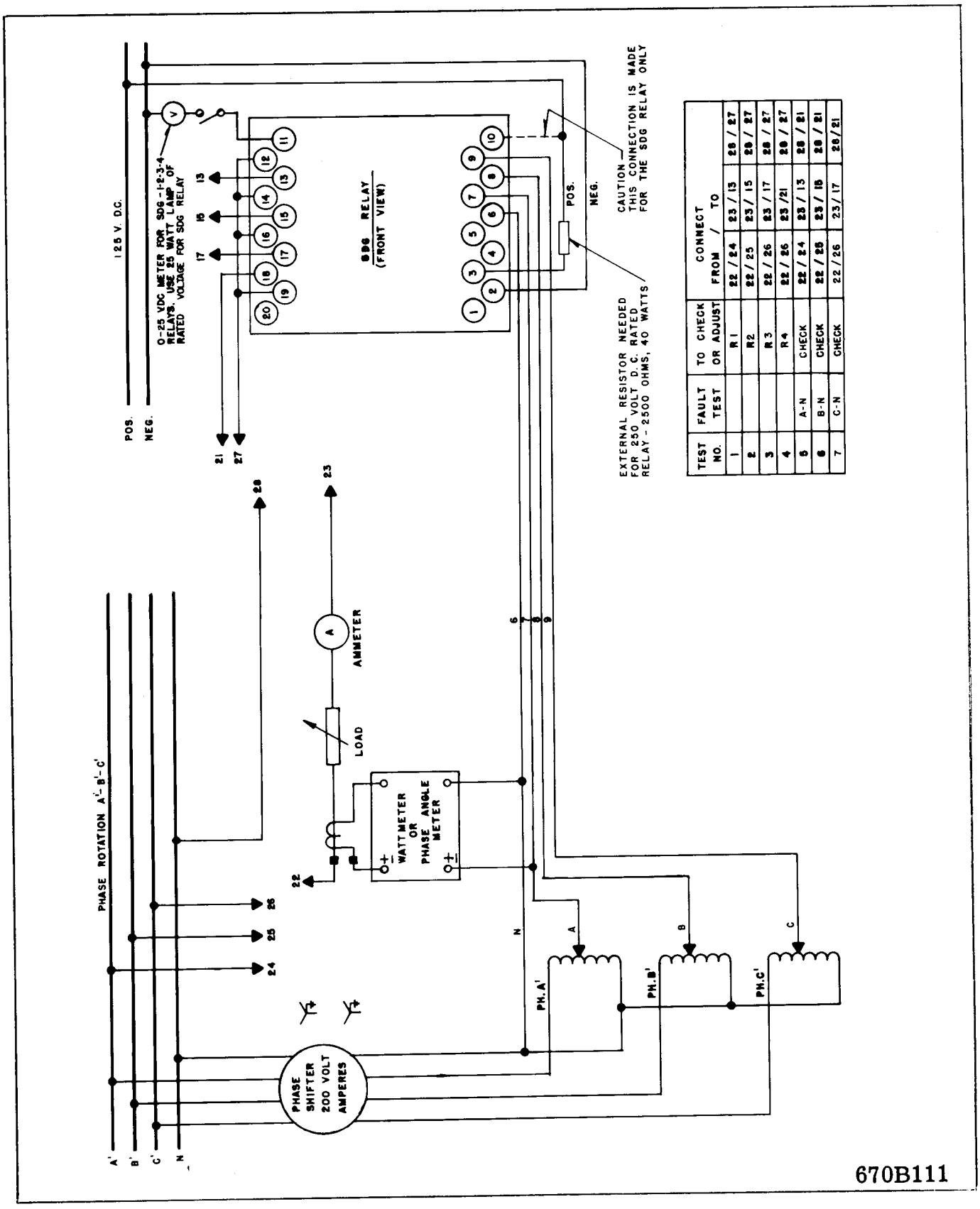
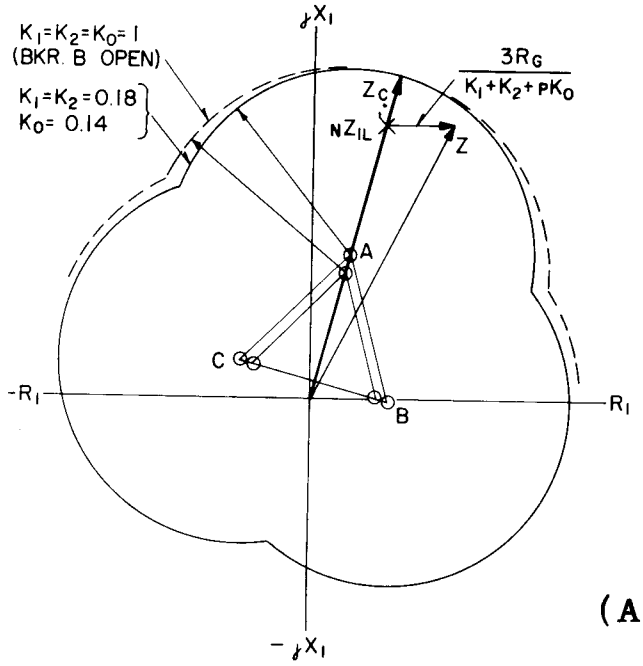


Fig. 22 External Connections for the SDG Relay



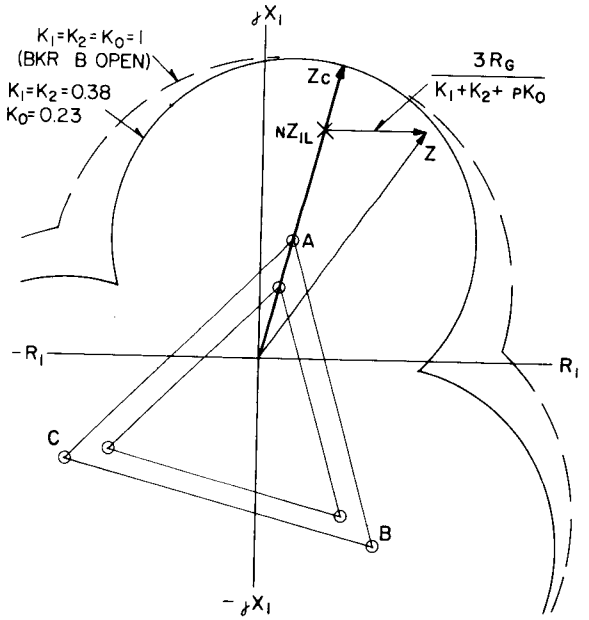
TEST NO.	FAULT TEST	TO CHECK OR ADJUST	CONNECT FROM / TO		
1		R1	22 / 24	23 / 13	28 / 27
2		R2	22 / 25	23 / 15	28 / 27
3		R3	22 / 26	23 / 17	28 / 27
4		R4	22 / 26	23 /21	28 / 27
5	A-N	CHECK	22 / 24	23 / 13	28 / 21
6	B-N	CHECK	22 / 25	23 / 15	28 / 21
7	C-N	CHECK	22 / 26	23 / 17	28 / 21

Fig. 23 Test Connections for the SDG Line Relays



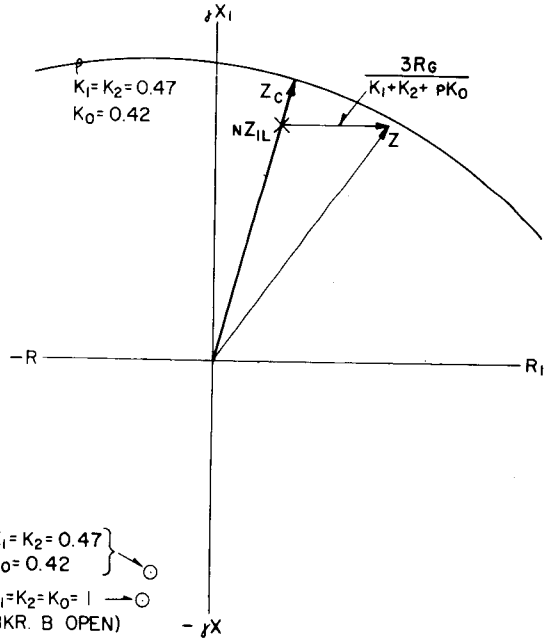
(A) 837A116

a) Long Line



(B) 837A114

b) Medium-length Line



(C) 837A115

c) Short Line

Fig. 24 Impedance Circles for the SDG Relays

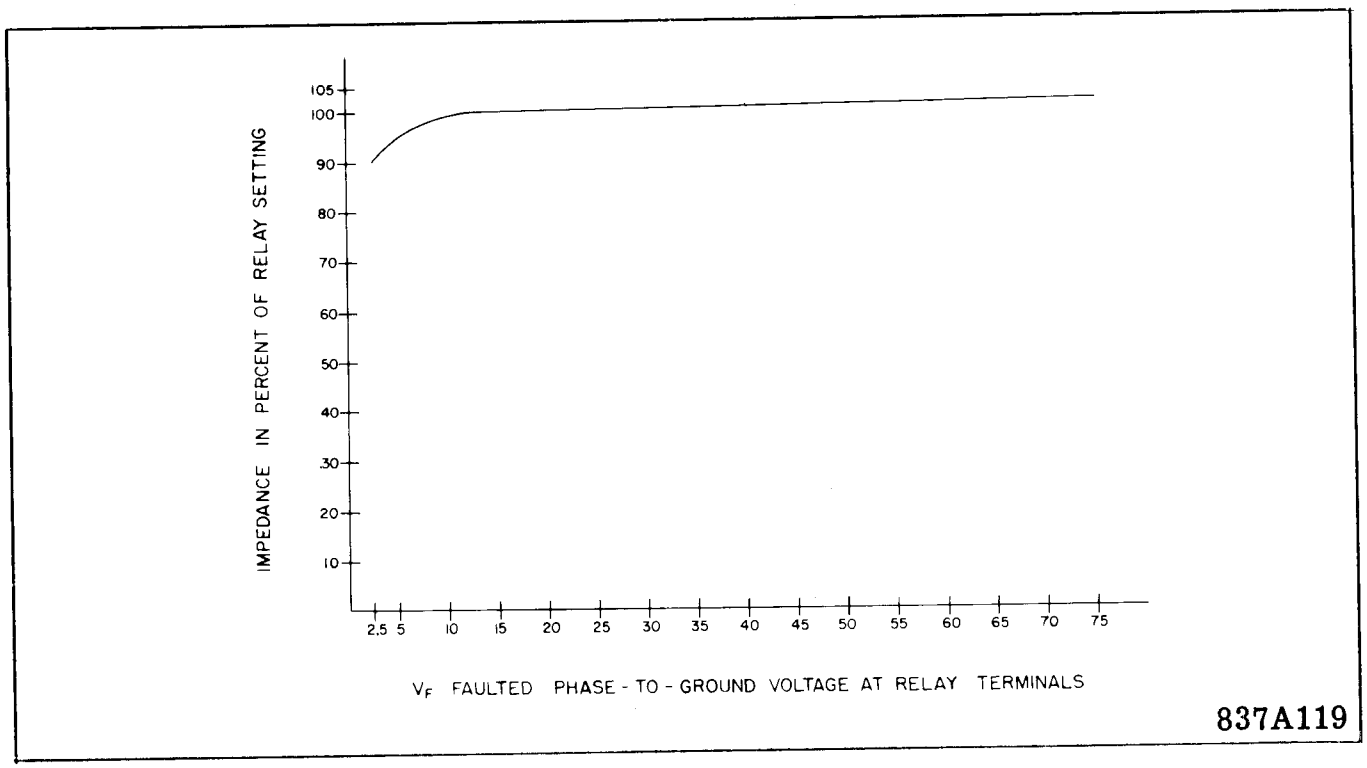


Fig. 25 Impedance Curves for the SDG Line Relays

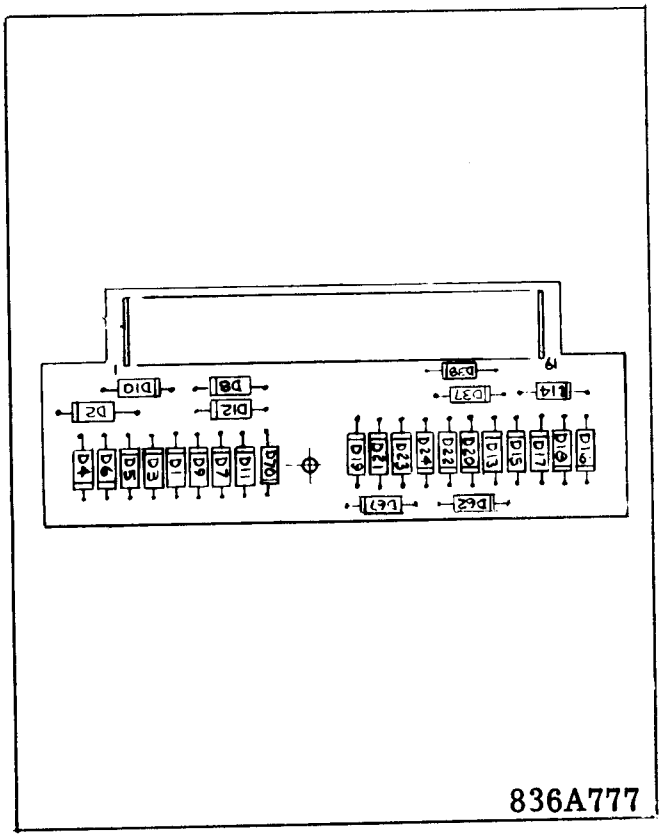


Fig. 26 Printed Circuit Board Assembly for SDG, SDG-1, 2, 3 & 4 Relays

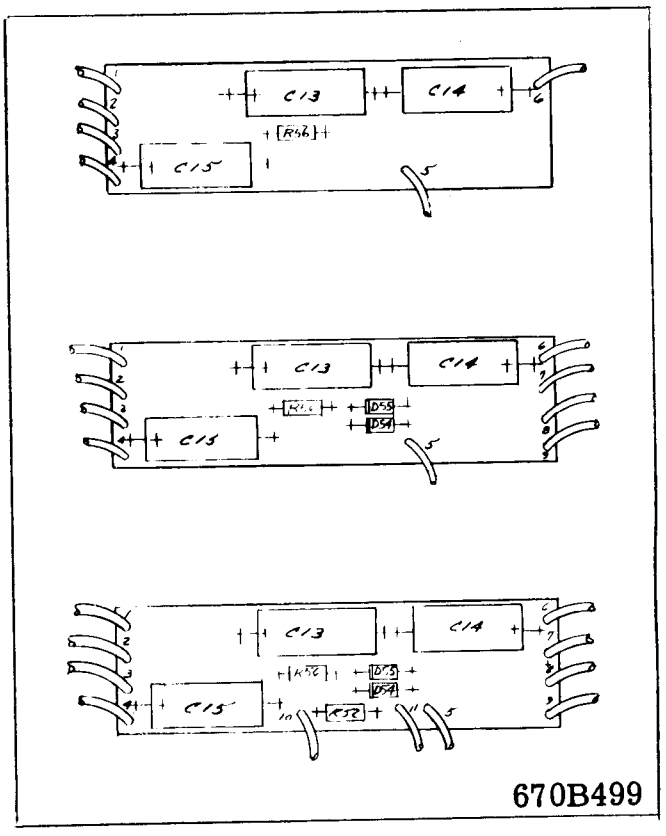


Fig. 27 Printed Circuit Board Assembly for SDG, SDG-1, 2, 3 & 4 Relays

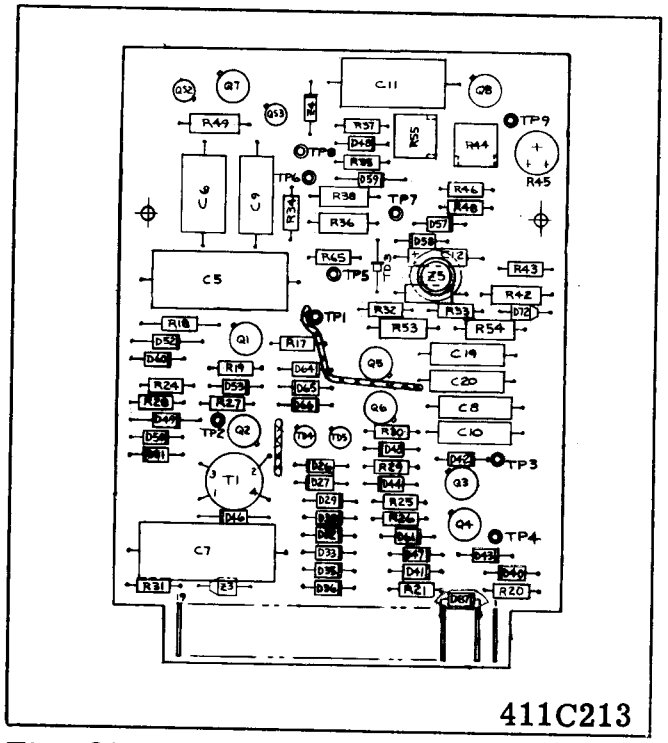


Fig. 28 Printed Circuit Board Assembly for SDG Relay

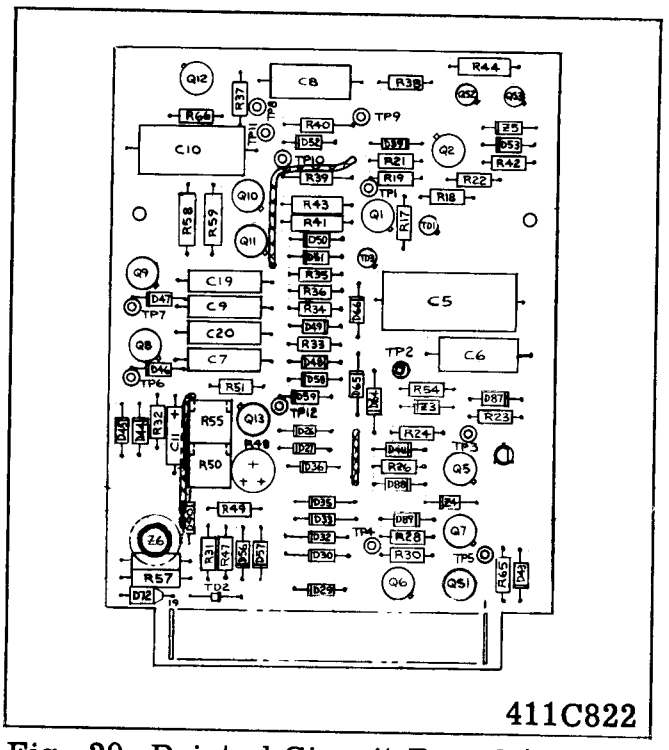


Fig. 29 Printed Circuit Board Assembly for SDG-1 Relay

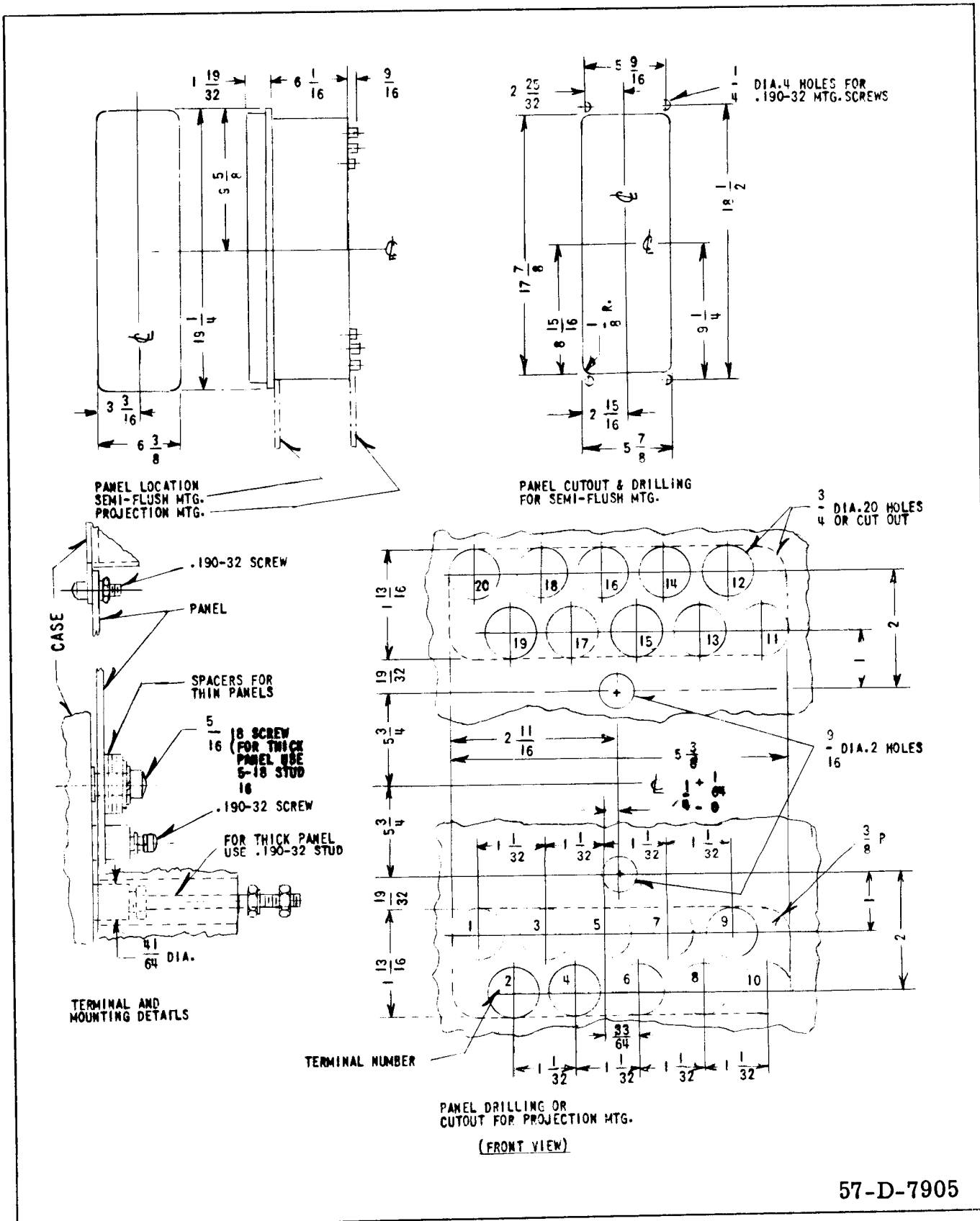


Fig. 30 Outline and Drilling Plan for the Type SDG Line Relays in an FT-42 Case

APPENDIX I

MUTUAL IMPEDANCE EFFECT

Where mutual compensation is desired, a type IK auxiliary current transformer (Fig. 32) maybe used with a step down current ratio of $\frac{|Z_{OM}|}{|Z_{OL}|} = C^1$ Z_{OM} is the zero sequence mutual impedance and Z_{OL} is the zero sequence self impedance of the line. Zone 1 maybe set to cover 85% of the line.

The "parallel line" leads on the IK-transformer are set for factor C^1, as defined above. These leads are set so that the difference between the taps is nearest to the desired C^1-value.

The external terminals of the IK-transformer numbered 3 and 4 are connected across the SDG-relay terminals 19 and 18 as shown in the external schematic figure 22. The external terminals 5 and 6 are connected in series with the residual CT circuit of the parallel line.

The IK transformer is set as outlined below. Before the proper tap settings are made, the cover of the transformer should be completely open. Complete opening of the cover assures continuity in the residual current transformer circuits and isolates the IK transformer windings from the residual circuits.

The taps are set so that difference between the two taps is equal to the desired setting of C^1. For instance, C^1 setting equal to 8, is set as follows:

Connect leads coming out of opening marked"parallel line" Fig. 32 to the terminals marked "C^1". Black lead (which is of the same polarity as the plus marked external terminal) is connected to terminal marked".2" and the white lead to the terminal marked "1.0". The difference between the two taps 1.0 - .2 = .8, is the desired "C^1" setting. Physically, this is done as follows:

Remove the top nut from the desired terminal, place the lug of the proper lead on the terminal and replace the locking nut. Make sure that nut holds the lug snugly against the terminal to avoid the possibility of developing a loose or high resistance connection.

The leads coming out of opening marked "protective relay" and "protected line" are connected to the terminals "0" and "1.0" in the row marked "C" observing the same polarity marking as above. This connection is the same for all "C^1" values less or equal to 1.

After the setting is completed the cover should be closed to restore the connection between the transformer winding and the external terminals.

General Considerations

In considering mutual zero-sequence impedance effects it is well to consider that the mutual impedance works to reduce fault-current level when the currents flow in the same direction in the coupled lines. The converse is true when the currents flow in opposite directions. For example, in Fig. 33(a), the currents are flowing in the same direction from the left, causing the relay at A to underreach. If, however, $|Z_{OS}| >> |Z_{OU}|$ then for a balance point fault (e.g. 85% from A to B), the

current I_{OM} reverses as in Fig. 24(b). Here the fault current K_oI_o is larger than for a similar situation except with $Z_{OM} = 0$; so a relay set for 85% of the line actually reaches farther due to mutual effects assuming no mutual compensation. Of course, as the fault moves closer to B, a point is reached where I_{OM} reverses, so that relay A will never overreach to see a bus fault at B.

If mutual compensation is used in Fig. 33(b) for relay A, it will have the harmful effect of reducing the operating current and hence the reach. We see then, that mutual compensation eliminates the effect of mutual impedance if, and only if, both K_oI_o & I_{OM} are flowing from the local bus into the lines.

For the usual case of Fig. 33(a) mutual compensation may be used to maintain zone 1 reach at 85% of the line regardless of whether the adjacent line is in or not. Without compensation, if the relay is set for 85% of the zero-sequence self-impedance, it will cover at least 70% (but less than 85% except for the Fig. 33(b) case) of the line with the adjacent line closed. Two things work to minimize the underreach: first, as the fault moves closer to bkr. A, I_{OM} decreases & K_oI_o increases; secondly, as the fault moves within the balance point, the restraint voltages are overcompensated, reducing the restraint. The amount of underreach varies with system impedances, but one can expect to cover at least 70% of the line, with an 85% nominal setting.

Mutual compensation of zone 2 is of more value: 1) Since I_{OM} is flowing in the same direction as K_oI_o for the entire length for end-zone faults, and 2) we need to make sure of 100% protected-line coverage.

We have already seen in Fig. 33(b) that mutual compensation is not always efficacious; we must also consider the adjacent-line faults of Fig. 34. In Fig. 34(a) we can be greatly overcompensated so that relay A operates due to the compensation current $I_{OM}\left(\frac{Z_{OM}}{Z_{OL}}\right)$. The SCC relay will minimize the possibility of SDG-line overreach for the case in Fig. 34(b).

In Fig. 34(c) bkr. C is open so that the same conditions exist for relay A whether or not mutual compensation is used. In this case, adjacent line current flows in the opposite direction to that of K_oI_o for the entire length. The zone-1-relay phase compensation at bkr. A is less than half of the proper amount to reach the fault, but the ground compensation may be in excess of the apparent zero-sequence impedance to the fault. The worst case occurs when there is no current source at U. Fortunately, zone 1 at A cannot overreach; however, zone 2 at A can see this fault if source U is weak, necessitating more time delay to coordinate with zone 2 time at D.

Note in both Fig. 34(b) & (c) that the system condition which can cause trouble with relays A & C is a poor source at U. This is also the condition yielding the greatest zone 1 underreach for protected line faults.

As mentioned earlier we can get at least 70% zone 1 coverage without mutual compensation. The advantages of tolerating a reduced reach with the parallel line in service (vs. 85% coverage with mutual compensation) are:

1) Type SCC current comparer not required.

2) No overreach tendencies for adjacent line faults - (Fig. 34(b))

3) Simplified current circuit (where we have zone 1 only).

Zone 2 should definitely be mutually compensated unless the mutual impedance effects are negligible. The SCC current comparer need not be applied for zone 2 supervision even though the zone 2 relay at A will operate for close-in faults (Fig. 34(a) since bkr. C is opened at high speed. In rare cases, after bkr. C opens (Fig. 34(c), zone 2 at A will remain operated (poor source at U), requiring time coordination with zone 2 at D.

Type SCC Current Comparer

The SCC relay prevents the SDG relay types from tripping for close-in adjacent line faults, where the mutual compensating current may reach many times the protected line current, as in Fig. 35(a). It is a static magnitude-comparison circuit. It operates on protected line current K_oI_o and restrains on $0.4\left|K_oI_o - dI_{om}\right| = 0.4\left|K_oI_o - \frac{Z_{OM}}{Z_{OL}} I_{om}\right|$. That is, it restrains on the difference between the protected line current and the mutual compensation current.

Fig. 35 illustrates the SCC relay operation for various conditions. It is in balance in Fig. 35(b). In Figs. 35(c), (d) & (e) it operates to permit distance relay trip.

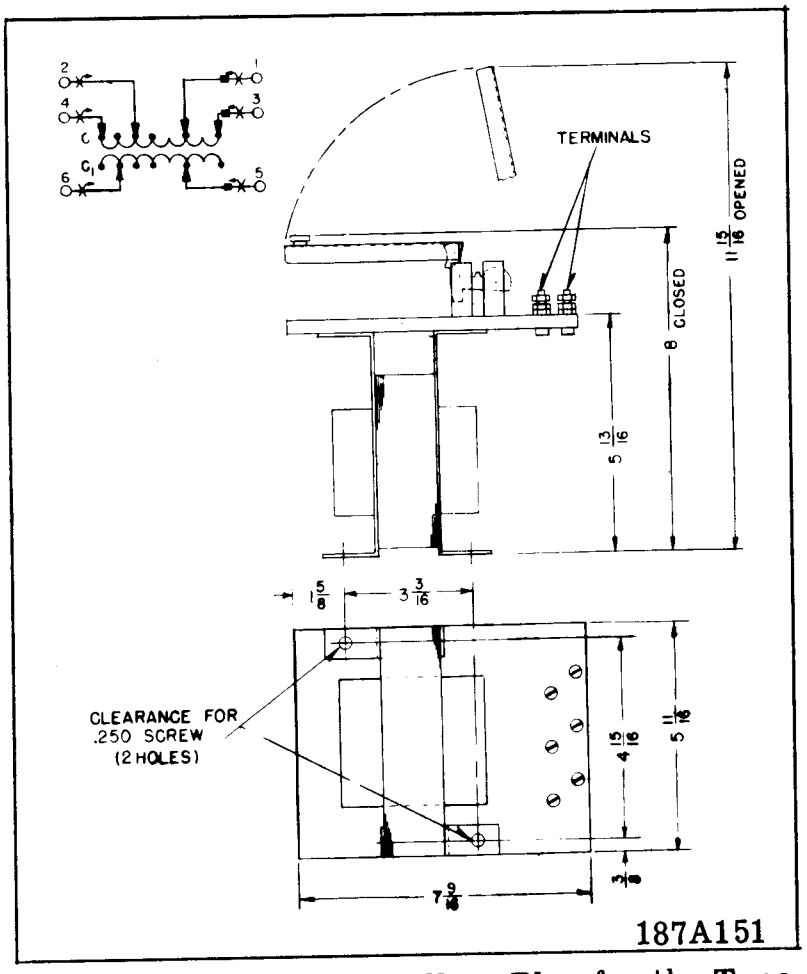


Fig. 31 Outline and Drilling Plan for the Type IK Transformer

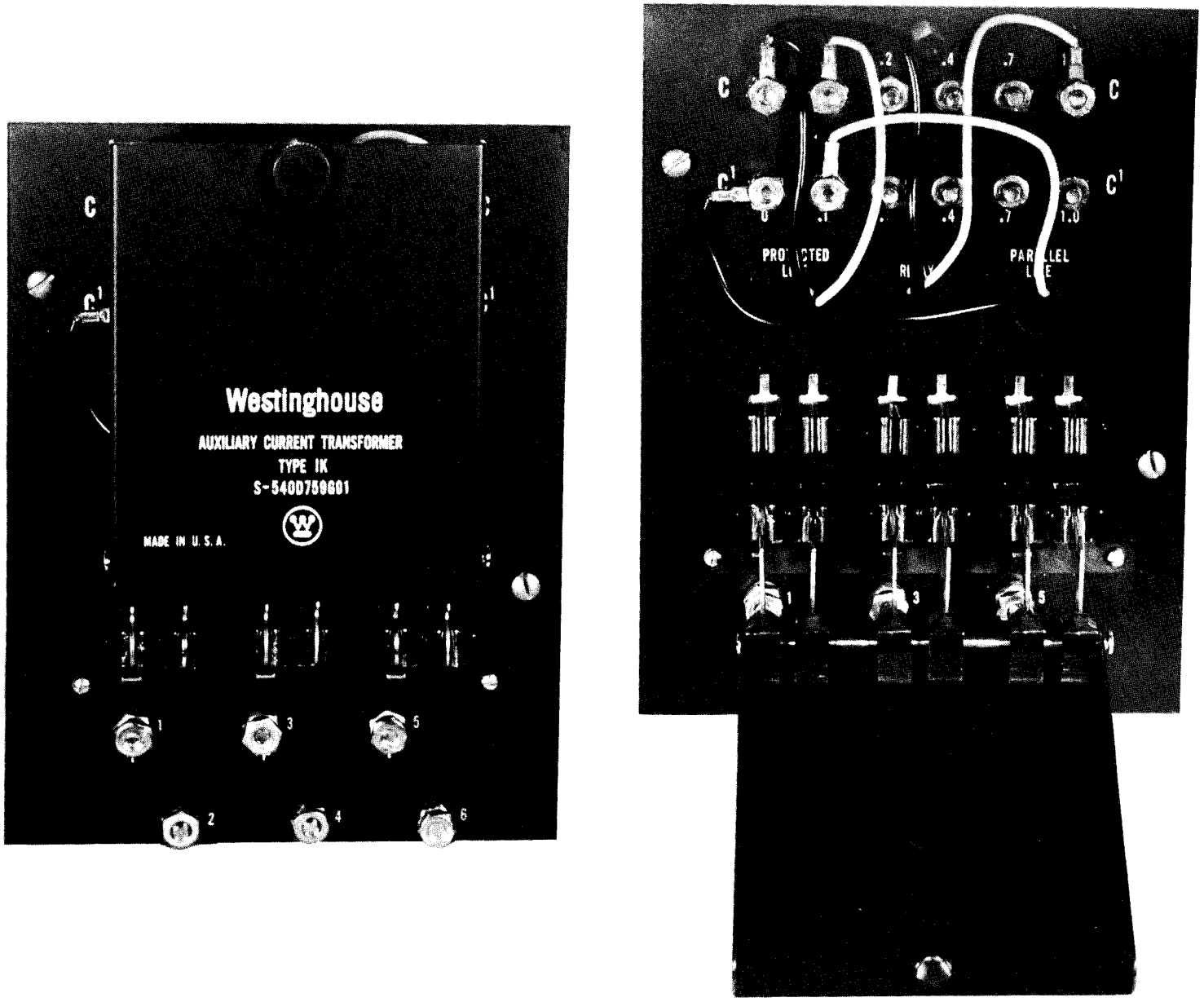
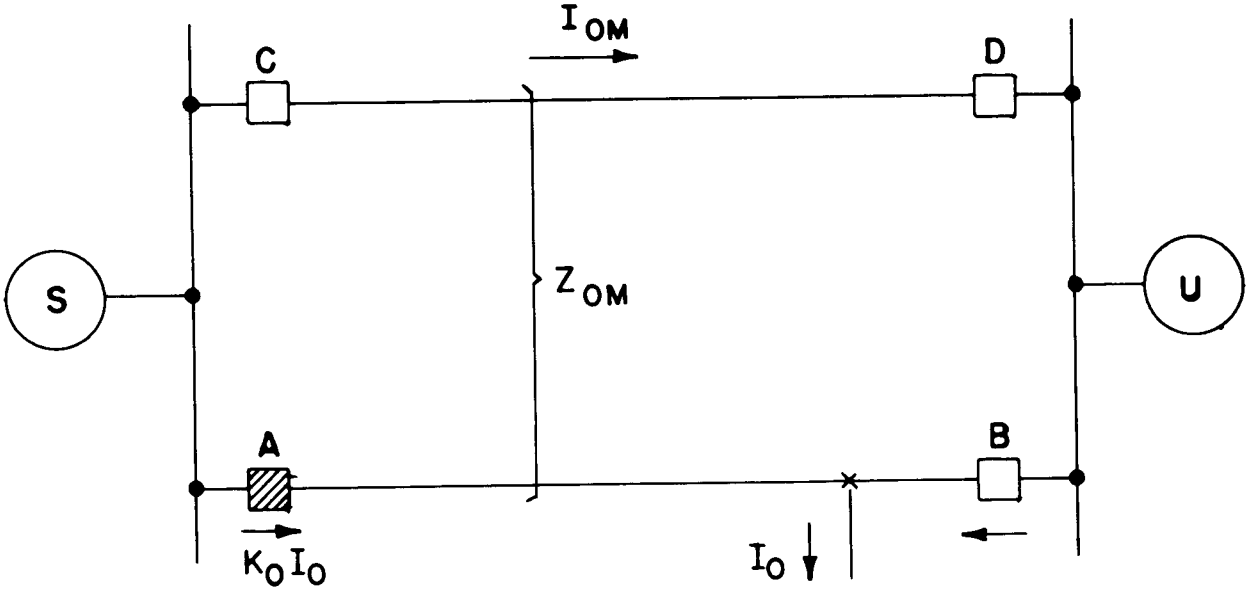
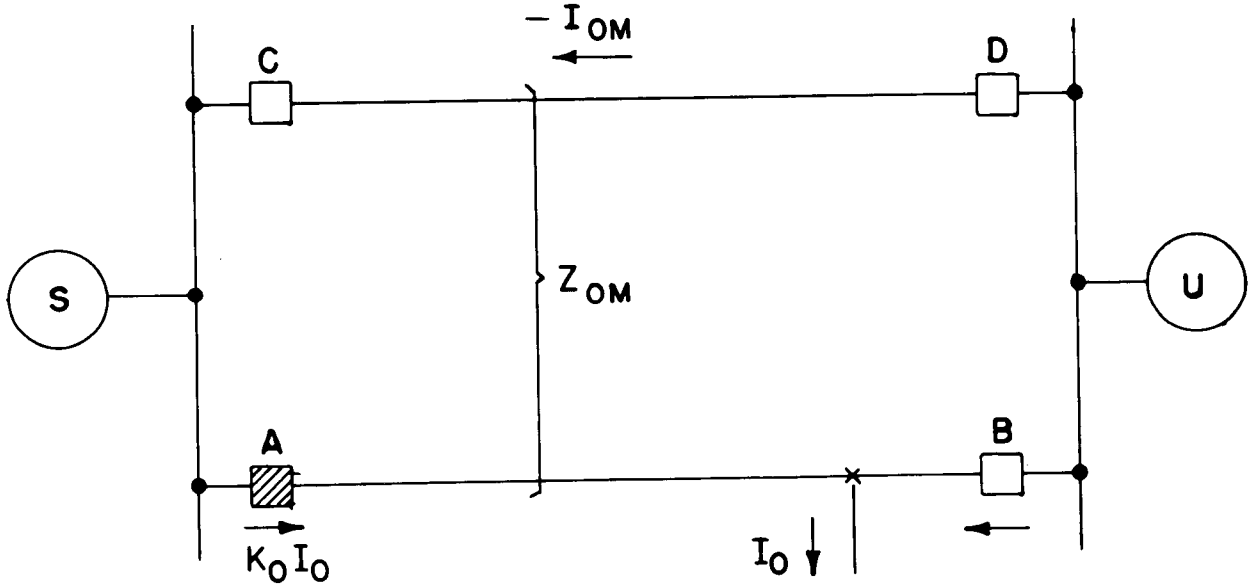


Fig. 32 Type IK Transformer



a) Mutual compensation helpful



b) Mutual compensation harmful ($|Z_{os}| >> |Z_{ou}|$)

Fig. 33 Zero-Sequency Currents for Zone 1 Balance-Point Fault with Mutual Coupling

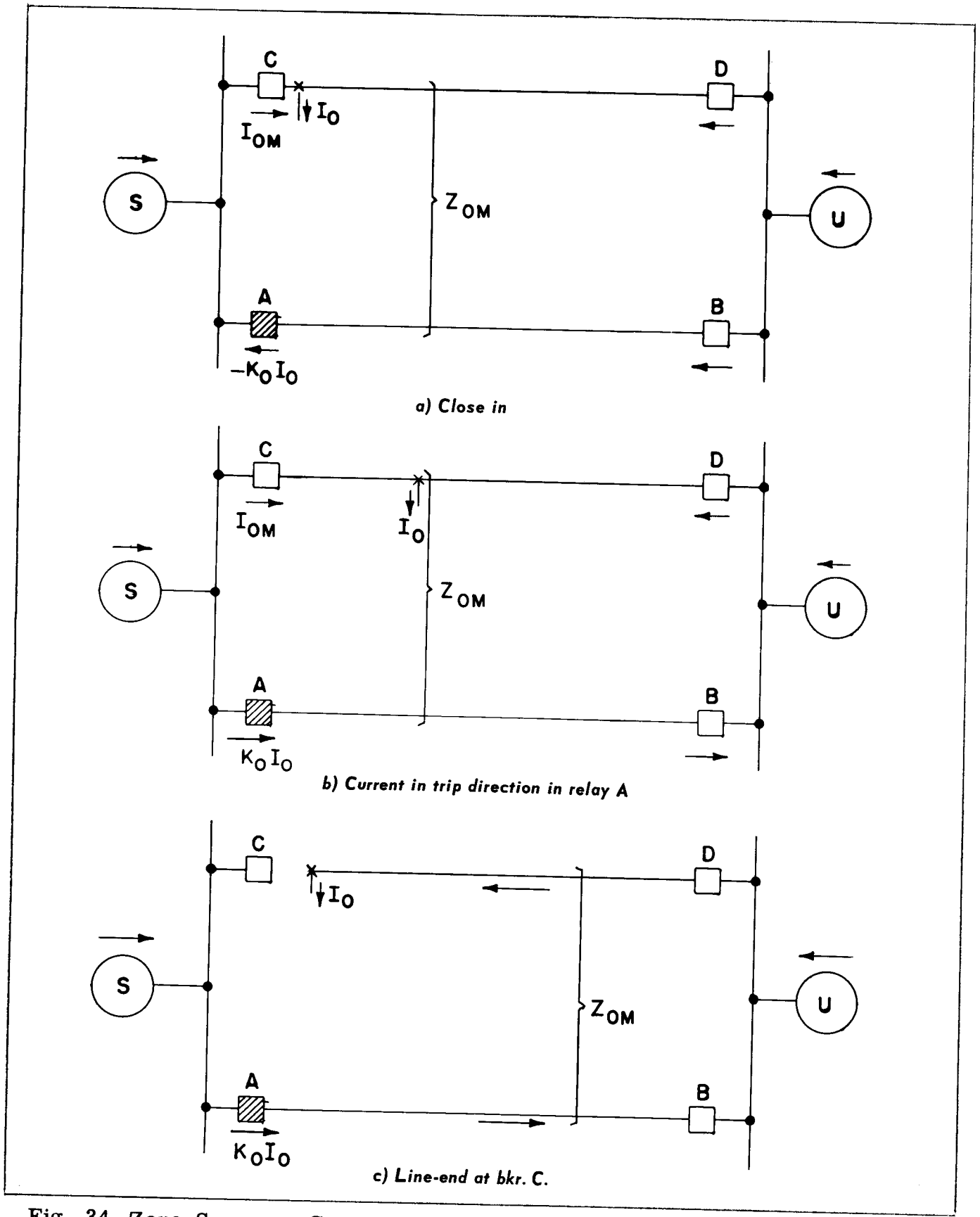


Fig. 34 Zero-Sequence Currents for Adjacent-Line Faults with Mutual Coupling

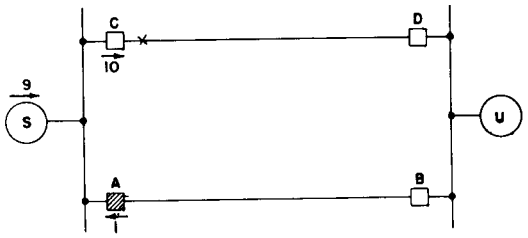
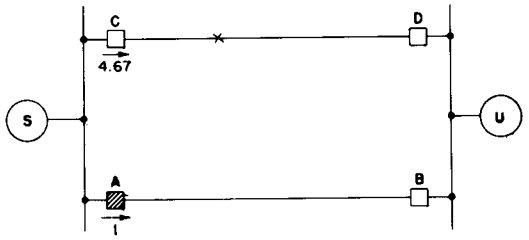
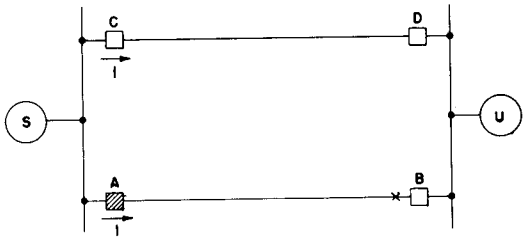
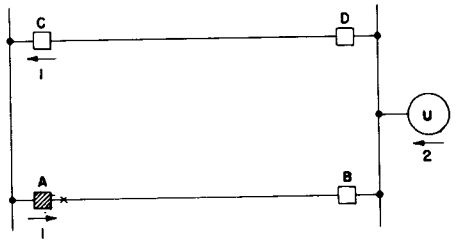
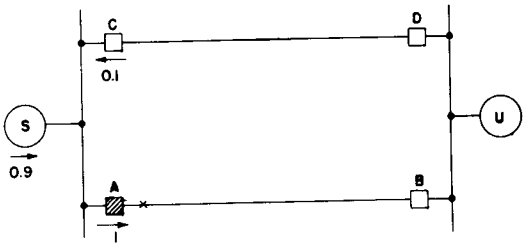
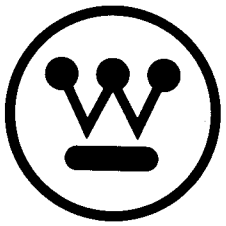
SCC OPER.		K_oI_o	$0.75\,I_{om}$	$0.4\,\lvert K_oI_o - 0.75\,I_{om}\rvert$
a) No		−1	7.5	3.4
b) Bal.		1	3.5	1.0
c) Yes		1	0.75	0.1
d) Yes		1	−0.75	0.7
e) Yes		1	−0.08	0.43

Fig. 35 Type SCC Relay Operation



WESTINGHOUSE ELECTRIC CORPORATION
RELAY-INSTRUMENT DIVISION
NEWARK, N. J.
Printed in U.S.A.

INSTALLATION • OPERATION • MAINTENANCE

INSTRUCTIONS

TYPE SDG LINE GROUND-DISTANCE RELAY

APPLICATION

These instructions cover the five basic types listed in Table I. This line of relays provides single-zone ground-distance protection. The relay reaches the preset amount for single-line-to-ground faults and as much as 20% less for double-line-to-ground faults.

TABLE I

Relay	I_0 Fault Det.	Freq. Verifier	Phase to Phase Desensitizer	Output	Application
SDG	X	X	X	Thyristor	Zone 1
SDG-1	X	X	X	Transistor	Zone 1 or Pilot Trip (Note 1)
SDG-2	—	X	X	Transistor	
SDG-3	X	—	—	Transistor	Timed Trip
SDG-4	—	—	—	Transistor	Blocking Start

NOTE 1: Also suitable for timed trip.

The potential supply must be wye-grounded. The broken delta potential connection is provided inside the relay.

As shown in Table I the SDG is equipped with a thyristor trip output; use this type where a single-zone is needed in conjunction with an otherwise electromechanical system. For all-static-systems use the transistor output types, utilizing the thyristor trips in the type SRU output package.

The frequency-verifier circuit should be utilized for all high-speed trip applications to avoid undesired trips due to high-frequency transients. This circuit is not needed for timed trips (e.g. zone 2), but the SDG-1 or SDG-2 may be utilized instead of the SDG-3 in the interests of standardization.

Relays with I_0 current detector are used to prevent tripping due to potential circuit trouble; the SDG-2 requires SI or SI-1 current-detector supervision.

The phase-phase desensitizer is used to eliminate a possible 15% overreach on two-line-to-ground faults. This circuit is needed for zone 1 applications where the relay reaches 85% towards the far bus.

A type IK auxiliary current transformer may be used to compensate for zero-sequence mutual induction. Otherwise, this transformer is not needed. For the case of two parallel two-terminal lines and an 85% self impedance relay, zone 1 will reach at least 70% to the far end; accordingly, there is not much gain in mutual compensation of zone 1. However, zone 2 may be mutually compensated since its reach is affected more than zone 1. Where zone 1 is mutually compensated, a type SCC current-comparer relay is required to supervise distance relay tripping. See Appendix 1 for details.

FUNDAMENTALS OF DISTANCE MEASUREMENT ON GROUND FAULTS

The SDG distance relay operates on both single and double line-to-ground faults. In either case, neglecting fault resistance, the faulted phase-to-ground voltages(s) at the relay consists of the line drop:

$$V_{LG} = \text{Faulted phase-to-ground relay voltage}$$

$$= K_1 I_1 n Z_{1L} + K_2 I_2 n Z_{1L} + K_0 I_0 n Z_{0L} + I_{0E} n Z_{0M} \quad (1)$$

Where K_1, K_2, K_0 are current distribution factors for the pos., neg., and zero sequence networks, respectively

I_1, I_2, I_0 are the pos., neg., and zero sequence currents in the fault.

$^{n}Z_{1L}$, $^{n}Z_{0L}$ are the pos. and zero sequence line impedances to the fault

I_{0E} is the adjacent line zero sequence current.

Z_{0M} zero sequence mutual impedance.

See Fig. 12 for further definition of terms. For an A to ground fault eq. (1) would be written in terms of the phase A quantities.

$$V_{AG} = K_1 I_{A1} {}^{n}Z_{1L} + K_2 I_{A2} {}^{n}Z_{1L} + I_{0E} {}^{n}Z_{0M} \quad (2)$$

Eq. (2) also applies for an AB to ground fault; an additional expression applies for the phase B quantities for an AB to ground fault.

Hence, a distance ground relay made to respond to single phase-to-ground faults will also respond in the same way to double line-to-ground faults. This is true except for the effect of ground resistance, RG. The different nature of these effects can be sensed from Fig. 13. In Fig. 13 the ground current $3I_0$ flowing through R_G is essentially in phase with the total faulted phase current. This is so, since $I_{A1} = I_{A2} = I_0$. This is not true for a 2L-G fault. The current $3I_0$ is out of phase with $K_1 I_{A1}$ and $K_2 I_{A2}$ (also out of phase with $K_1 I_{B1}$ and $K_2 I_{B2}$). As a result the drop across R_G produces an apparent reactance term to the distance relay, causing it to under-reach on one phase and over-reach on the other faulted phase. The SDG relay contains a desensitizer circuit to prevent over-reach on 2L-G faults, by reducing the reach of the relay.

$$V_{XN} = (V_{A1} + V_{A2}) - Z_C(K_A I_{A1} + K_2 I_{A2}) \quad (3)$$

$$V_{YN} = (V_{B1} + V_{B2}) - Z_C(K_1 I_{B1} + K_2 I_{B2}) \quad (4)$$

$$V_{ZN} = (V_{C1} + V_{C2}) - Z_C(K_1 I_{C1} + K_2 I_{C2}) \quad (5)$$

The restraint voltages are obtained by the use of compensators with an impedance Z_C, set to match the desired positive sequence line impedance reach. Only positive and negative sequence voltages appear in eq. (3) to (5). The zero sequence voltage is filtered out by not grounding the neutral of the set of Y-connected auxiliary transformers (T_{A2}, T_{B2} and T_{C2}) which are used to feed the restraint portion of the magnitude comparison circuit. These same connections render the zero sequence current flowing in the phase compensators ineffective. So the restraint voltages duplicate the delta voltage conditions at the fault when the fault is Z_C ohms from the relay (i.e. at the balance point). Zero sequence quantities are not required to duplicate the system voltage triangle at the balance point since zero sequence voltage cancels out of the line to line voltages.

The operating voltage is:

$$V_{W0} = V_0 - \frac{Z_{0L}}{Z_{1L}} \times Z_C \left(K_0 I_0 + I_{0E} \frac{Z_{0M}}{Z_{0L}}\right) \quad (6)$$

Here V_0 is the relay zero sequence voltage: it is compensated by using a compensator impedance $\frac{Z_{0L}}{Z_{1L}} Z_C$, representing the zero sequence line impedance to the desired balance point. For mutual coupled lines this compensator can be fed with not only the protected line current but also with a portion of the mutual current I_{0E} (See Fig. 12). The operating voltage V_{W0} duplicates the system zero sequence voltage for a fault at the balance point.

Since the faulted phase-to-ground voltage is zero at the fault (neglecting fault resistance), the operating and faulted phase restraint voltage will be equal for a balance point fault. This can be seen by manipulating the fault voltage expression, remembering that the relay compensated voltages are a replica of the fault-point voltages:

V_{LGF} = Faulted phase to ground voltage at fault

$$= V_{1F} + V_{2F} + V_{0F} = 0 \quad (7)$$

$$V_{1F} + V_{2F} = -V_{0F} \quad (8)$$

$$\left| V_{1F} + V_{2F} \right| = \left| V_{0F} \right| \quad (9)$$

Eq. (9) states that the magnitude of the sum of the pos. and neg. sequence voltage equals the magnitude of the zero sequence voltage at the fault. This holds regardless of how many phases are grounded. Eq. (9) is the keystone of the SDG system.

This balance point condition is shown in Fig. 14 for an A-G fault. The bus voltages ($V_{A1} + V_{A2}$) and V_0 are shown along with the compensator voltages, which modify the bus voltages to produce restraint voltage V_{XN} and operating voltage V_{WO}.

For this condition V_{YN} and V_{ZN} are also produced but these will be larger in magnitude since these are derived from the sound phases. Since these voltages exceed V_{XN}, they are irrelevant.

In Fig. 14 for a fault beyond the balance point, V_{XN} exceeds V_{WO}; the reverse is true for the fault within the balance point. Note that for all these faults in the trip direction that the phase compensation acts to reduce the bus positive and negative sequence voltages; whereas, the zero sequence compensation is added to V_0. The reverse is true for a fault behind the relay. For this reason the SDG is inherently directional.

One other aspect of Fig. 14 bears amplification. Note for the fault within the balance point that the phase compensation is almost enough to reverse V_{XN} polarity. It is possible for such a reversal to occur, and it is possible if very little zero sequence flows for the phase compensation to overtake the operating voltage and restrain the relay. Thus, the relay may fail to see a close-in fault if the zero sequence current is quite small. Any time this extreme occurs the phase distance relay will operate. The phase-distance relay will clear the fault when:

$$Z_1 > \frac{V_0/I_0}{K_1+K_2+pK_0}$$

where Z_1 is positive-sequence relay reach

V_0 = zero sequence bus voltage for close-in fault

I_0 = total zero-sequence fault current for close-in fault

K_1, K_2, K_0 pos.-, neg.- & zero-sequence current-distribution factors for close-in fault.

p = ratio of zero-sequence to positive-sequence line impedance.

CONSTRUCTION AND OPERATION

The type SDG relay consists of: four air gap transformers, three auto-transformers for reach adjustment, four phase splitter-transformers, one isolating transformer which couples the zero sequence network a-c output to the static frequency verifier circuit, one zero sequence current-to-voltage transformer, four phase-splitter and rectifier networks, a double line-to-ground fault desensitizer, one voltage regulating zener diode, a thyristor for the tripping function (if used), and printed circuit assemblies.

The large printed circuit assembly contains a magnitude comparator, frequency check circuit, the trigger circuit for the thyristor tripping unit, and the zero sequence current detector.

Compensators (T_A, T_B, T_C, T_O)

The compensators, which are designated T_A, T_B, T_C and T_O are two-winding air-gap transformers. Each current winding has seven taps which terminate at the tap block. A voltage is induced in the secondary which is proportional to the primary tap and current magnitude. This proportionality is established by the cross sectional area of the laminated steel core, the length of an air gap which is located in the center of the coil, and the tightness of the laminations. All of these factors which influence the secondary voltage have been precisely set at the factory. The clamps which hold the lamination should not be disturbed by either tightening or loosening the clamp screws.

The secondary winding has a single tap which divides the winding into two sections. One section is connected subtractively in series with the relay terminal voltage. Thus a voltage which is proportional to the phase current is subtracted vectorially from the relay terminal voltage. The second section is connected to an adjustable loading resistor (R_1, R_2, R_3, R_4) and provides a means of adjusting the phase angle between primary current and the induced secondary voltage. The phase angle may be set for any value between 60° and 90° by adjusting this resistor. The factory setting is for a maximum sensitivity angle of 75° current lagging voltage.

A tertiary winding M has four taps which may be connected to directly modify the T setting by any value from −18 to +18 percent in steps of 3 percent. The sign of M is negative when the R lead is above the L lead. M is positive when L is in a tap location which is above the tap location of the R lead. The M setting is determined by the sum of per unit values between the R and L lead. The actual per unit values which appear on the tap plate between taps are 0, .03, .09 and .06.

Auto-Transformer (T_{A1}, T_{B1}, T_{C1})

The auto-transformers T_{A1}, T_{B1}, T_{C1} have three taps on their main winding S which are numbered 1, 2 and 3 on the tap block.

The three secondary windings of the auto-transformers are connected in a "broken delta", thus serving as a source of zero sequence voltage

for the operating circuit. The primary to secondary turn ratio is 3:1, thus producing the proper zero sequence voltage magnitude as required by the theory of relay operation. Using S=2 or S=3 settings reduces zero sequence voltage in the same proportion as the line-to-neutral voltages.

The auto-transformer makes it possible to expand the basic range of T ohms by a multiplier of S.

Phase-Splitter Transformer (T_{A2}, T_{B2}, T_{C2}, T_{O2})

The phase splitter transformer provides isolation between the a-c analog network and the magnitude comparer circuitry located on the printed circuit board, and couples the restraint and operating outputs to the phase splitter network. The tap connection on the secondary winding serves as part of the phase splitting circuit that converts a single-phase input into a three-phase output, thus minimizing the ripple of the rectified output.

Isolating Transformer (I_O)

The isolating transformer I_O serves two purposes: First it isolates the a-c circuit from the d-c circuit, and second, it produces a secondary voltage in the presence of zero sequence current.

Isolating Transformer (T_{FV})

The isolating transformer T_{FV} serves two purposes: First, it isolates the a-c circuit from the d-c circuit and second, it steps up the clipped a-c signal to make the frequency check circuit sensitive to low level input signals.

Double Line-to-Ground Fault Desensitizer

The double line-to-ground fault desensitizer in Figs. 5 & 10 consists of the three networks. Each network consists of a resistor and a minimum voltage network. In this network the largest restraint voltage is blocked by a combination of two restraining voltages. If any two restraining voltages become smaller than the third restraint voltage, transistors Q17 and Q18 are turned on the prevent Q1 and Q2 transistors from turning on. When operating voltage becomes larger than the highest restraint the relay is allowed to trip. The desensitizer effect is limited to S=1 setting only and is not effective on the S=2 or S=3 setting. If S=2 or S=3 setting is used for zone 1 the setting should be reduced to 75% of the protected line to avoid overreach on double-line-to-ground faults.

Magnitude Comparator Circuit (Fig. 15)

The magnitude comparator circuit consists of a minimum voltage network of the voltage balance type in which operating current is caused to flow through a current detector whenever one of the phase restraint voltages becomes smaller than the operating voltage.

Resistors (R9, R10, R11) provide a return path for the operating current.

The current detector consists of a tunnel-diode TD1 and a transistor Q1. When the tunnel diode is switched to the high voltage state, the transistor is turned on. The use of the tunnel diode secures a sharp turn on characteristic for the triggering network.

When transistor Q1 is turned on it in turn switches transistor Q2 on, when transistor Q2 is "on" the collector voltage is raised to high positive voltage that starts the operation of the triggering circuit.

Triggering Circuit for SDG Relay (Fig. 16)

The triggering circuit consists of a four-layer diode D50, resistor R28, diode D51, and pulse transformer TR-1. When Q2 transistor is turned on capacitor C6 starts charging to the breakdown voltage of the four layer diode D50.

After breakdown of D50, capacitor C6 discharges through the primary of the TR-1 transformer thus producing a gating impulse that fires the output thyristor QS1 Diode D49 provides a quick discharge of C6 after Q2 is turned off through R24. Diode D51 protects D50 from reverse polarity. The triggering circuit is supervised by the residual overcurrent unit and frequency verifier circuit through diodes D52 and D60. D52 diode bypasses the charging capacitor C6 during the 4 ms. period the frequency verifier output is held at ground potential. D60 performs the same function in the absence of residual current.

Zero Sequence Current Detector (Fig. 17)

To prevent operation of the magnitude comparator during a blown potential fuse or similar condition a zero sequence current detector supervises the operation of the triggering network by preventing capacitor C6 in the triggering circuit from charging, keeping the point "P" at negative potential through the diode D60.

The detector employs a tunnel diode (TD3) as a level detector. The tunnel diode is biased through resistor R45 to the high voltage state so that enough voltage is maintained across the base-to-emitter junction of Q8 transistor to keep it conducting.

In the presence of the residual current a current derived negative voltage through transformer I_0 appears across resistor R41, switching TD3 to the low voltage state, thus turning transistor Q8 off and raising its collector to the positive DC voltage supply level, blocking D60 from discharging the C6 capacitor.

Frequency Verification (Fig. 18)

During certain switching conditions, such as energization of a transmission line, residual currents and voltages may exist of higher frequencies than 60 cycles per second. The frequency verifier prevents relay operation when the operating voltage period is less than 4.3 ms. The frequency verification circuit consists of two functional parts: zero-crossing and commutator circuits. The zero-crossing circuit consists of transistors Q3, Q4, Q5, and Q6. The zero-crossing circuit is used to allow operation in the presence of higher frequencies of small magnitude superimposed on a fundamental of 60 cps. During the positive or negative half cycles of the operating voltage V_{WO}, Q3 or Q4 transistors are driven into saturation by the output of the T_{FV} transformer. Transistors Q5 or Q6 conduct until capacitors C8 or C10 respectively are fully charged. While either capacitor charges, a voltage output in the form of very narrow pulse is developed across R32 & R33 resistors during the start of each half cycle. This pulse triggers QS2 control switch. When transistors Q3 or Q4 are not conducting, C8 and C10 capacitors discharge respectively through D45 or D44 and the parallel combination of R26 and R30 or R25 and R29.

While QS2 is "on" its anode is only about 0.7 volt above negative, thus preventing capacitor C6 in the triggering circuit from charging for 4.3 milliseconds. The time delay of 4.3 milliseconds is controlled by the resistor R38, the capacitor C11 and the reference Zener diode Z4. After 4.3 milliseconds of delay the control switch QS3 fires applying the voltage of capacitor C9 across QS2, turning it off. This raises the potential of the QS2 anode, leaving the triggering circuit free to operate. After the next zero crossing pulse, QS2 switch is turned on again, the QS3 switch is turned off by capacitor C9. Charge and commutator action is repeated all over again. Transistor Q7 when turned on by the same voltage that fires the gate of QS2, discharges timing capacitor C11, thus starting the timing cycle with close to zero charge on the capacitor. If the period of the V_{WO} voltage is less than 4.3 ms. the Q7 transistor discharges the timing capacitor thus preventing the turning off of QS3 switch. This keeps QS2 switch on to prevent operation of the triggering circuit. Capacitors C19 and C20 serve as coupling capacitors to start transient blocking whenever Q1 operates, this prevents tripping if V_{WO} – voltage stays at operating level for less than 4 msec.

Output Circuit (Fig. 19)

The output circuit or SDG relay consists of the secondary of the pulse transformer TR-1, diode D46, capacitor C7, resistor R31, and Zener diode Z3. The output of the SDG relay is a thyristor which is gated into conduction by a pulse transformer. The transformer is pulsed as described under "Triggering Circuit Operation". Zener diode Z3, resistor R31 and capacitor C7 form a network protecting the thyristor unit from voltage surges coming through the d-c supply. The function of diode D46 is to short out negative pulses coming from the TR-1 pulse transformer.

In the SDG-1, -2, -3, & -4 relays the output circuitry consists of transistors Q3, Q5, & Q6 and other associated components.

Upon the operation of the Q2-transistor in the magnitude comparator circuit, transistor Q3 is driven into conduction by the positive voltage developed across resistor R22. Transistor Q3, in turn, shunts the base drive current of transistor Q5, to turn Q5 off. At the same time the turned on Q3-transistor provides a base current path to transistor Q6 turning it on. An output voltage consequently is developed through transistor Q6, resistor R28, across Q5 and appears at relay terminal 11. In absence of the output from the magnitude and parator circuit the Q5 transistor is biased to conduct through resistor R24 and no output appears at relay terminal 11.

Q7 and QS1 form the pushbutton light circuit that operates an indicating light during a pushbutton check-out procedure.

Pushbutton Check Circuit (Fig. 20)

The pushbutton check circuit is used for in-service operational check-out of the output thyristor.

Depressing the pushbutton provides an internal d-c supply to the thyristor switch and operates the overcurrent circuit. This action must be preceded by the opening of the relay trip circuit (red handle) and relay voltage switch (7). The opening of the voltage switch produces operating voltage conditions in the magnitude comparator that gates the thyristor switch. Operation of the thyristor switch is indicated by the lighting of the bulb built into the pushbutton. A similar circuit is provided in the SDG-1, -2, -3, & -4 relays (See Fig. 10).

CHARACTERISTICS

Distance Characteristics

Fig. 24 shows the relay characteristic in the complex plane is $Z = nZ_{1L} + \frac{3R_G}{F}$ for single line to ground faults where factor $F = K_1 + K_2 + pK_0$, where K_1, K_2, K_0 are positive, negative and zero sequence current distribution factors and p = ratio of zero sequence to positive sequence line impedance. Impedance nZ_{1L} is the positive-sequence line impedance from the relay to the fault. The apparent impedance Z must fall within the characteristic shown in Fig. 24 in order to operate. The R-X characteristic is a composite of three circles whose centers are A, B, and C in Fig. 24A. The circle whose center is A is produced from the comparison of faulted phase restraint and operating voltage for a single-line-to-ground fault; whereas the "B" and "C" circles result from sound-phase restraint comparison with operating voltage. Note that part (A) of Fig. 24 applies for the case of a low source impedance vs line impedance; parts (B) and (C) represent increasing amounts of source impedance, or conversely shorter line lengths. The solid-line characteristic is based on current distribution factors for a balance point fault with all breakers closed. As the fault moves toward the relay these distribution factors increase, with the relay approaching the dashed-line characteristic. In the case of Fig. 24C, the dashed-line characteristic is not shown, as it essentially coincides with the solid-line characteristic. Regardless of system conditions, the relay reaches Z_C positive-sequence ohms for a fault at the compensator angle. The fact that the circle diameter expands with increasing source impedance is beneficial, since this provides increased fault resistance accommodation for the shorter line applications. By this we mean that it takes a greater $\frac{3R_G}{K_1+K_2+pK_0}$ component to yield a Z phasor which is outside the operate zone. In Fig. 24C only the faulted phase characteristic is shown, since the other two fall well out of the first quadrant.

One might conclude from Fig. 24 that the relay is not directional since its characteristic includes the origin. This conclusion would be erroneous, since the characteristic equations assume faults in the trip direction per Fig. 14 and do not apply for reversed faults. The relay is directional. In Fig. 24 the second and third quadrants are essentially theoretical since a "negative resistance" is only possible due to out-of-phase infeed. The fourth quadrant is pertinent for series capacitor applications. So we are normally only interested in the first quadrant.

General Characteristics

Impedance settings in ohms reach can be made in steps of 3 percent. The maximum sensitivity angle, which is set for 75 degrees at the factory, may be set for any value from 60 degrees to 82 degrees. A change in the maximum sensitivity angle will produce a slight change in reach for any given setting of the relay. Referring to Fig. 11, note that the compensator secondary voltage output V, is largest when V leads the primary current, I, by 90°. This 90° relationship is approached, if the compensator loading resistor is open-circuited. The effect of the loading resistor, when connected, is to produce an internal drop in the compensator, which is out-of-phase with the induced voltage, IT_A, IT_B or IT_C. Thus the net voltage, V, is phase-shifted to change the compensator maximum sensitivity angle. As a result of this phase shift the magnitude of V is reduced, as shown in Fig. 11. The tap markings are based upon a 75° compensator angle setting. If the resistors R1, R2, R3, and R4 are adjusted for some other maximum sensitivity angle the nominal reach is different than that indicated by the taps. The reach Z_θ, varies with the maximum sensitivity angle, θ, as follows:

$$Z_\theta = \frac{TS \sin \theta (1 + M)}{\sin 75°}$$

TAP PLATE MARKINGS

T_A, T_B, T_C (Positive Sequence)

For 1.0-31 Ohms range- 1.2, 1.5, 2.1, 3.0, 4.5, 6.3, 8.7

For .2-4.35 Ohms range- .87, 1.16, 1.45, 2.03, 2.9, 4.06, 5.8

For .2-4.35 Ohms range- .23, .307, .383, .537, .69, .92, 1.23

T_O (Zero Sequence)

For 1.0-31 Ohms range- 3.60, 4.5, 6.3, 9.0, 13.5, 18.9, 26.1

For .75-20 Ohms range- 2.61, 3.48, 4.35, 6.1, 8.2, 12.2, 17.4

For .2-4.35 Ohms range- 0.69, 0.92, 1.15, 1.61, 2.07 2.76, 3.69

	(S_A and S_C)		
	1	2	3
± Values between taps (M_A and M_C)	.03	.09	.06

TIME CURVES AND BURDEN DATA

Operating Time

The speed of operation is shown in Fig. 21. The curves indicate the time in milliseconds required for the relay to provide an output for tripping after the occurance of a fault at any point on a line within the relay setting.

Current Circuit Rating in Amperes (All Ranges, All Settings)

Continuous — 10 Amperes

1 Second — 240 Amperes

Burden

The potential burden at 69 volts varies from a maximum of 1.4 volt-amperes at S=1 setting to a minimum of 0.42 volt-amperes based on 69 volts line to neutral per phase. Current burden varies from a maximum of 4.5 volt-amperes at 5 amperes for a maximum T-setting to a minimum of 0.60 volt-amperes for a minimum T-setting. This burden applies to each phase and residual current circuit. D.C. current burden is .07 amperes at all rated voltages.

Trip Circuit Constants

1 Ampere I.C.S. 0.1 ohms d-c resistance

Thyristor (SDG Only)

The thyristor is a three-terminal semiconductor device. In the reverse, or non-conducting direction, the device exhibits the very low leakage characteristics of a silicon rectifier. In the forward, or conducting directions conduction can be initiated by the application of a control pulse to the control terminal or "gate". If a gate signal is not applied, the device will not conduct at below rated forward blocking voltage. With the application of a gate signal, however, the device switches rapidly to a conducting state characterized by a very low voltage drop and a high current-carrying capability. Once a conduction has been initiated, the gate terminal no longer has any effect. In order to turn the thyristor off the anode-cathode current must be reduced to a value less than the holding current.

It should be noted that the SDG differs from mechanically operated contacts. A certain minimum trip current must flow before the thyristor will latch on. However, voltage will be applies to the load for the duration of each pulse. Pulses are applied to the gate circuit at a rate of four every one milliseconds.

Current Rating Per Circuit:

Ambient Temperature	25°C	50°C	75°C
For 50 ms. (3 cycle breaker)	60 A	49 A	37 A
For 83 ms. (5 cycle breaker)	54 A	44 A	33 A
Continuous	6.5 A	4.5 A	3 A

Trip Circuit Requirements:

$$\frac{\text{Vdc}}{R_{\text{LOAD OHMS}}} = .25 \text{ amp or more}$$

$$\frac{L_{\text{HENRYS}}}{R_{\text{LOAD OHMS}}} = .02 \text{ or less}$$

Thyristor

Max. forward leakage current at rated voltage = 125°C 8 MA d-c

Max. reverse leakage current at rated voltage = 125° C 8 MA d-c

Max. forward voltage drop at 10 amps = 25° C 1.6 volts

CALCULATIONS AND SELECTION OF SETTINGS

Relay reach is set on the tap plate. Maximum sensitivity angle, θ, is set for 75° (current lagging voltage) in the factory. This adjustment need not be disturbed for line angles of 65° or higher. For line angles below 65°, set θ for a 60° maximum sensitiv-

ity angle, by adjusting R_1, R_2, R_3 & R_4, for zone 1 application only. Set zone 1 reach to be 85% of the line, if S=1 is used; 75% if S=2 or 3.

Assume a desired balance point which is 85% of the total length of the line. The general formulas for setting the ohms reach of the relay are:

$$Z_1 = Z_{1L} \frac{0.85\ Rc}{R_V} ; \quad Z_0 = Z_{0L} \frac{0.85\ Rc}{R_V}$$

The terms used in this formula and hereafter are defined as follows:

Z_0 = Zero sequence ohmic reach.

Z_1 = Positive sequence ohmic reach

$Z_{1,0}$ = TS (1 + M) = the tap plate setting.

T = Compensator tap value.

S = Auto-transformer tap value.

θ = Maximum sensitivity angle setting of the relay.

±M = Compensator tertiary tap value. (This is a per unit value and is determined by the sum of the values between the "L" and the "R" leads. The sign is positive when "L" is above "R" and acts to raise the Z setting. The sign is negative when "R" is above "L" and acts to lower the "Z" setting).

Z_{1L} = Positive sequence ohms per phase of the total line section, referred to primary.

Z_{0L} = Zero-sequence ohms per phase of the total line section, referred to primary.

R_c = Current transformer ratio.

R_V = Potential transformer ratio.

The following procedure should be followed in order to obtain an optimum setting of the relay.

Zone 1 Setting (SDG, SDG-1, SDG-2 Relays)

1. a. Establish the desired values of Z_1 and Z_0 as above (available from transmission line data) and desired maximum sensitivity angle, $\theta°$.

   b. Determine the desired tap plate value Z' using the formula:

$$Z_1 = Z_1 \frac{\text{Sin } 75°}{\text{Sin } \theta°} \text{ and } Z_0 = Z_0 \frac{\text{Sin } 75°}{\text{Sin } \theta°}$$

When $\theta = 75°$, $Z_1 = Z_1$ and $Z_0 = Z_0$

2. Now refer to Table II or IV giving preferred zone 1 settings for the SDG relays. If the desired reach exceeds the relay range for S=1, use S=2 & Table III or V (set for 75% of line).

   a. Locate a table value for relay reach nearest to the desired Z' value (it will always be within 1.5% of the desired value.)

   b. From this table read off the "S", "T" and "M" settings. The "M" column includes additional information for the "L" and "R" lead setting for the specified "M" value. If the desired settings cannot be found on this table proceed to Table III or V to find the desired setting. The relay reach must now be reduced from 85 to 75 percent to avoid overreach on two phase to ground faults on high fault resistance faults.

   c. Recheck relay settings for Z_1' and Z_0' using equation:

   Z = TS (1 + M)

   For example, assume the desired reach, Z_1 is 7 ohms at 60° (Step 1a) and Z_0 is 21 ohms at 60°.

   Next step is (1b). Making correction of maximum sensitivity angle of the relay to match the characteristic angle of the line (60°) that is different from factory setting of 75°, we find the relay tap setting

   $Z_1' = 7 \times 1.11 = 7.77$ ohms

   $Z_0' = 21 \times 1.11 = 23.31$ ohms

   This procedure is followed when R_1, R_2, R_3, R_4 settings are changed, otherwise follow alternative procedure below.

   Step (2a). In Table IV we find 7.65 to be the nearest value to 7.77 ohms.

   $100 \times \frac{7.65}{7.77} = 98.8\%$ or 1.2% from the desired value

For the Z_0 selection find the nearest value to 23.31 ohms using the same S setting as above. 23.0 ohms is the nearest value.

$100 \times \frac{23.0}{23.31} = 98.8\%$ or 1.2% within the desired value

Step (2b). From Table IV read off:

S = 1
T = 8.7
M = -.12
T_0 = 26.1
M_0 = -.12

The "R" – lead should be connected over "L" – lead, with "L" lead connected to "O" – tap and "R" – lead to tap "09". (The sum of the values between L & R is 0.12)

Step (2c). Recheck Settings.

$Z_1 = TS(1 \pm M) = 1 \times 8.7(.88) = 7.65$ and

$Z_0' = 1 \times 26.1(.88) = 23.0$

$Z_1 = Z_1' \frac{\text{Sin } 60°}{\text{Sin } 75°} = 7.65 \times .900 = 6.90$ ohms at 60°

$Z_0 = Z_0^1 \frac{\text{Sin } 60°}{\text{Sin } 75°} = 23.0 \times .900 = 20.7$ ohms at 60°

Alternative Calculations and Settings

If it is desired to avoid recalibration of the relay maximum sensitivity setting the following procedure should be followed.

Follow Step 1a as above.

Change Step 1b to compute desired reach according with equation:

$$Z' = \frac{Z}{\text{Cos } (75-\theta)}$$

Then $Z_1 = \frac{7}{\text{Cos } (75-60)} = \frac{7}{.965} = 7.25w$

$Z_0 = \frac{21}{\text{Cos } (75-60)} = \frac{21}{.965} = 21.75w$

Step 2(a) as above From Table IV we find 7.25-value and 21.75 ohm-values as the exact values.

Step 2(b) From Table IV read off

S = 1
T = 6.3 T_0 = 18.9
M = +.15 M_0 = +.15

Step 2(c) Recheck settings:

$Z_1 = Z_1 \cos (75°-\theta) = 7.25 \times 965 = 7$ ohms

$Z_0 = Z_0 \cos (75-\theta) = 21.75 \times 965 = 21$ ohms

Zone 2 & 3 Settings

For zone 2 and 3 settings use a procedure similar to that for zone 1 described above. Tables II to V give the required settings. There is no need to recalibrate relay for, zone 2 or 3 application for difference in maximum torque angle.

Note: The S setting must be the same for both the positive and zero-sequence reach.

SETTING THE RELAY

The SDG relays require settings for the four compensators (T_A, T_B, T_C, and T_O), the three auto-transformer primaries (S_A, S_B, and S_C), and the four compensator tertiaries (M_A, M_B, M_C, and M_O). All of these settings are made with taps on the tap plate, and relay should be deenergized.

Compensator (T_A, T_B, T_C, T_0, and M_A, M_B, M_C, M_0)

Each set of compensator primary T_A, T_B, T_C, and T_O, taps terminates in inserts which are grouped on a socket and form approximately three-quarters of a circle around a center insert which is the common connection for all of the taps. Electrical connections between common insert and tap inserts are made with a link that is held in place with two connector screws, one in the common and one in the tap. A compensator tap setting is made by loosening the connector screw in the center. Before removing the screw open switches 12 through 19 to bypass the current around the relay. Remove the connector screw in the tap end of the link, swing the link around until it is in position over the insert for the desired tap setting, replace the connector screw to bind the link to this insert, and retighten the connector screw in the center. Since the link and connector screws carry operating current, be sure that the screws are turned to bind

snugly. Compensator secondary tap connections are made through two leads identified as L and R for each compensator. These leads come out of the tap plate each through a small hole, one on each side of the vertical row of "M" tap inserts. The lead connectors are held in place on the proper tap by connector screws.

Values for which an "M" setting can be made are from -.18 to +.18 in steps of .03. The value of a setting is the sum of the numbers that are crossed when going from the R lead position to the L lead position. The sign of the "M" value is determined by which lead is in the higher position on the tap plate. The sign is positive (+) if the L lead is higher and negative (-) if the R lead is higher.

An "M" setting may be made in the following manner. Remove the connector screws so that the L and R leads are free. Refer to Table II through Table V to determine the desired "M" value. Neither lead connector should make electrical contact with more than one tap at a time.

Line Angle Adjustment

Maximum sensitivity angle is set for 75° (current lagging voltage) in the factory. This adjustment need not be disturbed for line angles of 65° or higher. For line angles below 65° set for 60° maximum sensitivity angle by adjusting the compensator loading resistors R_1, R2, R_3, R_4. Refer to repair calibration under "Maximum Torque Angle Adjustment," when a change in maximum sensitivity angle is desired. For zone 2 and 3 application no need to recalibrate relay.

In general, the change in maximum torque angle adjustment, if desired, can be avoided. In this case the tap plate setting of the relay is adjusted to compensate for difference in the maximum torque angle of the relay (75°) and the characteristic angle of the line 8, according to the following equation:

$$Z_{1,0} = \frac{Z_{1,0}}{\text{Cos}\,(75°-\theta)}$$

Here $Z_{1,0}$ - Tap Plate Setting.

$Z_{1,0}$ - Desired Ohmic Reach.

TABLE II

.2-4.35 OHMS RELAY RANGE

PREFERRED ZONE 1 IMPEDANCE SETTINGS

POSITIVE SEQUENCE (Z_1) S = 1								ZERO SEQUENCE (Z_0) S = 1								M		CONNECT		
T	.230	.307	.383	.537	.69	.92	1.23	T_0	.69	.921	1.15	1.61	2.07	2.76	3.69	+M	−M	"L" LEAD TO TAP	"R" LEAD TO TAP	
	.272	.362	.452	.632	.815	1.09	1.45		.815	1.09	1.36	1.90	2.44	3.26	4.40	+.18		.06	0	
	.264	.352	.441	.617	.794	1.06	1.41		.794	1.06	1.32	1.85	2.38	3.18	4.25	+.15		.06	.03	"L" OVER "R"
	.258	.344	.430	.601	.772	1.03	1.38		.772	1.03	1.29	1.80	2.32	3.10	4.15	+.12		.09	0	
	.251	.335	.418	.585	.754	1.00	1.34		.754	1.00	1.25	1.76	2.26	3.00	4.04	+.09		.09	.03	
	.244	.325	.405	.570	.732	.975	1.30		.732	.975	1.22	1.71	2.20	2.92	3.92	+.06		.06	.09	
	.237	.316	.396	.555	.710	.950	1.27		.710	.950	1.18	1.66	2.13	2.84	3.80	+.03		.03	0	
	.230	.307	.383	.537	.69	.920	1.23		.69	.921	1.15	1.61	2.07	2.76	3.69	0	0	0	0	
	.223	.298	.370	.520	.670	.892	1.19		.670	.892	1.12	1.56	2.00	2.68	3.58		−.03	0	.03	
	.216	.288	.360	.505	.650	.865	1.15		.650	.865	1.08	1.52	1.95	2.60	3.46		−.06	.09	.06	
	.209	.280	.348	.488	.627	.840	1.12		.627	.840	1.05	1.47	1.88	2.51	3.36		−.09	.03	.09	"R" OVER "L"
	.202	.270	.336	.472	.607	.810	1.08		.607	.810	1.01	1.42	1.82	2.43	3.25		−.12	0	.09	
	.195	.260	.324	.456	.587	.782	1.05		.587	.782	.980	1.37	1.76	2.35	3.14		−.15	.03	.06	
	.188	.252	.314	.440	.565	.755	1.01		.565	.755	.940	1.32	1.70	2.26	3.02		−.18	0	.06	

TABLE III

.2-4.35 OHM RELAY RANGE

PREFERRED ZONE 2 & 3 IMPEDANCE SETTINGS

POSITIVE SEQUENCE SETTINGS (Z_1)										ZERO SEQUENCE SETTINGS (Z_0)										M		CONNECT		
S = 2							S = 3			S = 2							S = 3					"L" LEAD TO TAP	"R" LEAD TO TAP	
T	.230	.307	.383	.537	.69	.92	1.23	.92	1.23	T_0	.69	.921	1.15	1.61	2.07	2.76	3.69	2.76	3.69	+M	−M			
	.544	.724	.905	1.26	1.63	2.17	2.90	3.26	4.40		1.63	2.17	2.72	3.80	4.90	6.50	8.70	9.80	12.1	+.18		.06	0	"L" OVER "R"
	.528	.704	.880	1.23	1.59	2.12	2.82	3.18	4.25		1.59	2.12	2.65	3.70	4.76	6.35	8.48	9.55	12.7	+.15		.06	.03	
	.516	.688	.860	1.20	1.55	2.06	2.76	3.10	4.15		1.55	2.06	2.58	3.60	4.65	6.20	8.25	9.30	12.4	+.12		.09	0	
	.502	.670	.835	1.17	1.51	2.00	2.68	3.00	4.04		1.51	2.00	2.50	3.50	4.52	6.00	8.05	9.05	12.1	+.09		.09	.03	
	.488	.650	.810	1.13	1.46	1.95	2.60	2.92	3.92		1.46	1.95	2.44	3.41	4.40	5.85	7.80	8.80	11.8	+.06		.06	.09	
	.474	.632	.790	1.10	1.42	1.90	2.53		3.80		1.42	1.90	2.37	3.32	4.26	5.70	7.60		11.4	+.03		.03	0	
	.460	.614	.766	1.07	1.38	1.84	2.46		3.69		1.38	1.84	2.30	3.22	4.14	5.52	7.38		11.1	0	0	0	0	
	.446	.596	.740	1.04	1.34	1.78	2.40		3.58		1.34	1.78	2.24	3.12	4.02	5.35	7.15		10.7		−.03	0	.03	"R" OVER "L"
	.432	.576	.716	1.01	1.30	1.73	2.32		3.46		1.30	1.73	2.16	3.02	3.90	5.16	6.94		10.4		−.06	.09	.06	
	.418	.560	.695	.975	1.25	1.67	2.24		3.36		1.25	1.67	2.09	2.94	3.78	5.00	6.70		10.1		−.09	.03	.09	
	.404	.540	.674	.940	1.21	1.62	2.17				1.21	1.62	2.02	2.83	3.66	4.85	6.50		9.8		−.12	0	.09	
	.390	.520	.650	.910	1.17	1.56	2.10				1.17	1.56	1.95	2.74	3.55	4.67	6.27		9.4		−.15	.03	.06	
	.376	.504	.625	.880	1.13	1.50	2.08				1.13	1.50	1.79	2.64	3.40	4.50	6.05		9.1		−.18	0	.06	

TABLE IV

1.1-31 OHMS RELAY RANGE

PREFERRED ZONE 1 IMPEDANCE SETTINGS

	POSITIVE SEQUENCE (Z_1') S = 1							ZERO SEQUENCE (Z_0) S = 1								M		CONNECT		
																		"L" LEAD TO TAP	"R" LEAD TO TAP	
T	1.2	1.5	2.1	3.0	4.5	6.3	8.7	T_0	3.6	4.5	6.3	9.0	13.5	18.9	26.1	+M	−M			
	1.42	1.77	2.48	3.54	5.3	7.43	10.2		4.25	5.30	7.45	10.6	15.9	22.2	30.8	+.18		.06	.0	"R" OVER "L"
	1.38	1.73	2.42	3.45	5.17	7.25	10.0		4.15	5.17	7.25	10.4	15.5	21.7	30.0	+.15		.06	.03	
	1.34	1.68	2.36	3.36	5.04	7.05	9.75		4.05	5.04	7.05	10.1	15.1	21.2	29.3	+.12		.09	0	
	1.31	1.64	2.29	3.27	4.90	6.89	9.50		3.94	4.90	6.89	9.81	14.7	20.6	28.4	+.09		.09	.03	
	1.27	1.59	2.22	3.18	4.77	6.70	9.25		3.82	4.77	6.70	9.54	14.3	20.0	27.7	+.06		.06	.09	
	1.24	1.55	2.16	3.09	4.64	6.50	8.95		3.71	4.64	6.50	9.27	13.9	19.5	26.9	+.03		.03	0	
	1.20	1.5	2.10	3.00	4.50	6.30	8.70		3.6	4.50	6.30	9.0	13.5	18.9	26.1	0	0	0	0	
	1.16	1.45	2.04	2.91	4.36	6.10	8.45		3.50	4.36	6.10	8.73	13.1	18.3	25.2		−.03	0	.03	"R" OVER "L"
	1.13		1.97	2.82	4.23	5.90	8.15		3.38		5.90	8.46	12.7	17.7	24.5		−.06	.09	.06	
	1.09		1.91	2.73	4.10	5.74	7.90		3.27		5.74	8.19	12.3	17.2	23.7		−.09	.03	.09	
	1.06		1.85	2.64	3.96	5.55	7.65		3.16		5.55	7.92	11.9	16.6	23.0		−.12	0	.09	
	1.02		1.77	2.55	3.82	5.35			3.06		5.35	7.65	11.5	16.0			−.15	.03	.06	
	0.99				3.69				2.95				11.1				−.18	0	.06	

TABLE V

1.1-31 OHMS RELAY RANGE

PREFERRED ZONE 2 & 3 IMPEDANCE SETTINGS

T	POSITIVE SEQUENCE SETTINGS (Z_1)									ZERO SEQUENCE SETTINGS (Z_1)										M		CONNECT		
	S = 2							S = 3		S = 2								S = 3				"L" LEAD TO TAP	"R" LEAD TO TAP	
	1.2	1.5	2.1	3.0	4.5	6.3	8.7	6.3	8.7	T_0	3.6	4.5	6.3	9.0	13.5	18.9	26.1	18.9	26.1	+M	−M			
	2.84	3.54	4.96	7.08	10.62	14.9	20.5	22.3	30.8		8.50	10.6	14.9	21.2	31.8	44.5	61.5	66.6	92.5	+.18		.06	0	"L" OVER "R"
	2.76	3.46	4.84	6.90	10.35	14.5	20.0	21.6	30.0		8.30	10.34	14.5	20.7	31.0	43.5	60.0	65.1	90.0	+.15		.06	.03	
	2.68	3.36	4.72	6.72	10.08	14.1	19.5	21.2	29.3		8.10	10.08	14.1	20.2	30.2	42.4	58.5	63.6	87.5	+.12		.09	0	
	2.62	3.28	4.58	6.54	9.81	13.8	19.0		28.4		7.88	9.80	13.8	19.6	29.4	41.2	56.8		85.2	+.09		.09	.03	
	2.54	3.18	4.44	6.36	9.54	13.4	18.5		27.7		7.64	9.54	13.4	19.1	28.6	40.0	55.3		83.0	+.06		.06	.09	
	2.48	3.10	4.32	6.18	9.27	13.0	17.9		27.0		7.42	9.28	13.0	18.5	27.8	39.0	53.8		80.5	+.03		.03	0	
	2.4	3.0	4.20	6.0	9.0	12.6	17.4		26.1		7.20	9.0	12.6	18.0	27.0	37.8	52.2		78.3	0	0	0	0	
	2.32	2.90	4.08	5.82	8.73	12.2	16.9		25.2		7.00	8.72	12.2	17.5	26.2	36.6	50.5		75.8		−.03	0	.03	"R" OVER "L"
	2.26		3.95	5.64	8.46	11.8	16.3		24.5		6.76		11.8	16.9	25.4	35.4	49.0		73.5		−.06	.09	.06	
	2.18		3.82	5.46	8.19	11.5	15.8		23.7		6.54		11.5	16.4	24.6	34.4	47.5		71.0		−.09	.03	.09	
	2.12		3.70	5.28	7.92	11.1	15.3		23.0		6.32		11.1	15.8	23.8	33.2	45.8		68.8		−.12	0	.09	
	2.04		3.54	5.10	7.65	10.7			22.7		6.12		10.7	15.3	23.0	32.0					−.15	.03	.06	
	1.98				7.38										22.2						−.18	0	.06	

INSTALLATION

The relays should be mounted on switchboard panels or their equivalent in a location free from dirt, moisture, excessive vibration and heat. Mount the relay by means of the mounting stud for the type FT projection case or by means of the four mounting holes on the flange for the semi-flush type FT case. Either the stud or the mounting screws may be utilized for grounding the relay. The electrical connections may be made directly to the terminals by means of screws for steel panel mounting or to the terminal stud furnished with the relay for thick panel mounting. The terminal stud may be easily removed or inserted by locking two nuts on the stud and then turning the proper nut with a wrench.

For detailed information on the FT case refer to I.L. 41-076.

EXTERNAL CONNECTIONS

Figure 22 shows typical connection for single zone protection using an SDG relay.

ACCEPTANCE TEST

Acceptance tests consists of:

1. A visual inspection.
2. "Push-button" - check.
3. An electrical test to make certain that the relay measures the balance point impedance accurately.

1. Visual Inspection

Give a visual check to the relay to make sure there are no loose connections, broken resistors or broken wires.

.2-4.35 ohm relay	.75-20 ohm relay	1.0-31.0 ohm relay
all T= = 1.23	all T = 5.8	all T = 8.7
T_0 = 3.69	T_0 = 17.4	T_0 = 26.1
all S = 1	all S = 1	all A = 1
all M = +.18	all M = +.18	all M = +.18

2. Push-Button Check

Using the test connections of Fig. 23. Connect the a-c voltages as per test no. 1. No current connections are required. Connect the rated d-c voltages as shown. Open circuit the connections to terminal no. 7. Set $V_{BN} = V_{CN} = 70$ Volts. Depress the white pushbutton. The pushbutton should light. If the pushbutton does not light, connect a d-c voltmeter or a 25 watt lamp as per Fig. 23. The voltmeter should have a minimum deflection of at least 5 volts. If there is a deflection but the lamp does not light this indicates a fault in the pushbutton circuit. If there is no indication proceed with the electrical test to isolate the fault in the pushbutton circuit or the relay.

3. Electrical Tests

Distance Unit

Tripping is indicated for the SDG relay when the 25 watt lamp shown on Fig. 23 turns on and for SDG-1, -2, -3, & -4 relays when DC voltmeter indicates a minimum deflection of 5 volts for balance point condition. Refer to Fig. 23 for all test connections.

For .2-4.35 Ohm Relay

A. Use connections for test No. 5 and set V_{AN} voltage = 20 volts. $V_{BN} = V_{CN} = 70$ volts. Set the phase shifter for 75° current lagging voltage.

B. The relay current required to make the trip should be between 8.0-8.6 amp.

C. Use connections for Test No. 6 and set V_{BN} voltage = 20 volts. $V_{AN} = V_{CN} = 20$ volts. Set the phase shifter as above. The relay trip current should be 8.0-8.6 amps.

D. Use connections for Test No. 7 and set V_{CN} = 20 volts $V_{AN} = V_{BN} = 70$ volts. Set the phase shifter as above. The SDG relay trip current should be 8.0-8.6 amp.

For 1.0-31.0 ohm relay and .75-20 ohm Relay

A. Use connections for test #5 and set $V_{AN} = V_{BN} = V_{CN} = 70$ volts. Set the phase shifter for 75° current lagging voltage. The relay trip current should be 3.95-4.20 amperes for 1-31 ohm relays and 5.95-6.30 amp for .75-20 ohm relays.

B. Use connections for test #6 and set $V_{AN} = V_{BN} = V_{CN} = 70$ volts, and set the phase shifter as above. The relay trip current should be 3.95-4.20 amperes for 1-31 ohm relays and 5.95-6.30 amp. for .75-20 ohm relays.

C. Use test connections for test #7 and set V_{AN} = V_{BN} = V_{CN} = 70 volts. Set the phase shifter as above. The relay trip current should be 3.95-4.20 amperes for 1-31 ohm relays and 5.95-6.30 amp. for .75-20 ohm relays.

If the electrical response is outside the limits a more complete series of tests outlined in the section titled "Calibration" may be performed to determine which component is faulty or out of calibration.

If it is desired to check relay response at some other settings use following equation for the trip value of current.

$$I = \frac{3V_{LN}}{(2+p)Z_1}, \text{ Where } p = \frac{Z_0}{Z_1}$$

Z_0 = Zero sequence reach

Z_1 = Positive sequench reach (in above cases p = 3)

WARNING If testing required trip current over 15 amp. over prolonged periods, it is recommended that a heavy short lead be connected from terminal 19 to the center tap of T_O-socket. Also connect a jumper lead from terminal 16 to terminal 1 on the large printed circuit board for SDG-1 and SDG-3 relays and terminal 2 to terminal 4 for SDG-relay on the large printed circuit board. (Lower set of terminals rear view).

MAXIMUM TORQUE ANGLE

Maximum torque angle check is optional. In general, this check is complicated for SDG, SDG-1 and SDG-2 relays by the presence of transient blocking circuit, and the two-phase-to-ground fault desensitizer circuit.

The presence of transient blocking circuit requires that check for maximum torque angle should be made going from non-tripping to tripping condition at each end of the tripping range of the relay under test. Since the lab method of testing as used here presents artificial voltage conditions under certain voltage and phase angle condition two-phase-to-ground desensitizer will distort phase angle response; hence, it is required to disable the 2ϕ-G circuit by jumpering terminal for SDG-1 and SDG-2 #10 to #1 on large printed circuit board (for SDG-relay jumper #10 terminal to #4).

Phase A Check

Use connection #5. Relay tap settings should be the same as before. For all ranges set V_{AN} = 20 volts, VBN-VCN = 70 volts.

Set current for 1-30 ohm relay for 1.54 amp, for .75-20 ohm relay for 2.30 amp and for .2-4.35 ohm relay for 11 amp. Set phase-shifter for 75°-current lagging V_{AN}-voltage. Turn phase-shifter toward 0° after relays have dropped out reverse phase-shifter rotation and note the angle (ϕ1) at which relay is fully tripped. Then rotate the phase-shifter past the 75° until relay resets again. Then rotate phase shifter toward 75° again until relay is fully tripped. Note the angle again (ϕ2).

Maximum

Maximum torque angle is equal then to

$$\frac{\phi_1 + \phi_2}{2} = 75° (\pm 3°)$$

Any other T setting may be used, except use 130% current of the trip current at 75° angle.

Phase B Check

Use connection #6. Set V_{CN} = 20 volts. V_{AN} = V_{BN} = 70 volts. Otherwise follow the same procedure as for Phase A.

When check is completed, remove the jumper.

TWO-PHASE-TO-GROUND DESENSITIZER CHECK

Use connection #5, except no current connection is required for this test.

AB - Combination

Set V_{CN} = 70 V. V_{AN} = V_{BN} = 20 volts. Check d-c voltage on small P.C. board located just behind R1-R4 potentiometer terminal "10" (positive) located behind R1-potentiometer (second from the bottom) and relay terminal "2". It should measure 11.5-13.5 volts.

Set V_{CN} = 75 V. V_{AN} = V_{BN} = 10 volts. The DC voltage should measure 16.5-18.5 volts.

BC - Combination

Same check as for AB-except first set V_{AN} = 70V. $V_{BN} = V_{CN}$ = 20 volts and then V_{AN} = 75V. $V_{BN} = V_{CN}$ = 10 volts.

CA - Combination

Same check as for AB-except first set V_{BN} = 70V. $V_{CN} = V_{AN}$ = 20 volts and then V_{BN} = 75V, $V_{CN} = V_{AN}$ = 10 volts.

Overcurrent Unit

Check operation of the overcurrent unit by using test connection #5 of the Fig. 23. Set V_{AN} = 0, $V_{BN} = V_{CN}$ = 70 volts. The .2-4.35 ohm relay should operate at .75-.83 ampere, and the 1-31.0 ohms relay and .75-20 ohms relay should operate at .37-.420 amperes. If not, check adjustment of R45 for SDG relay and R48 for SDG-1 and SDG-3 relays.

Frequency Verifier

Use connection #5. Set V_{AN} = 0 volts, $V_{BN} = V_{CN}$ = 70 volts. Output of the Frequency Verifier is observed at test point TP6—for SDG Relay or TP10—for SDG-1 and SDG-2 relays. Use oscilloscope or DC voltmeter to observe the output. If oscilloscope is used, the output should be a positive pulse having 4.0 to 4.3 millisecond width at the base. If voltmeter is used the voltage at the test point should be approx. one helf of the voltage across the power zener (Z_1). This voltage is controlled by value of R38-resistor and C11-capacitor for SDG-relay or R43 and C10-for SDG-1 and SDG-2 relays. Smaller value of these components will increase the pulse width, and increase the voltage magnitude at test point.

Indicating Contactor Switch (ICS) (SDG Only)

With the SDG relay tripping, pass sufficient d-c current through the trip circuit to close the contacts of the ICS. This value of current should be not less than 1.0 ampere or greater than 1.2 amperes, for the 1 ampere ICS. The current should not be greater than the particular ICS tap setting being used for the 0.1-2.0 ampere ICS. The operation indicator target should drop freely.

The contact gap should be approximately 0.047" for the 0.2-2.0 ampere unit and 0.070" for the 1.0 ampere unit between the bridging moving contact and the adjustable stationary contacts. The bridging moving contact should touch both stationary contacts simultaneously.

ROUTINE MAINTENANCE

The relays should be inspected periodically, at such time intervals as may be dictated by experience, to insure that the relays have retained their calibration and are in proper operating condition.

"In-Service Test" (If relay is set for S = 1 only)

In-service testing is performed as follows:

1. Open relay trip circuit by opening red handle switch No. 11.
2. Open relay voltage terminal 7.
3. Press white pushbutton. Pushbutton light should light.

This test checks out the operation of the magnitude comparator and output circuitry.

REPAIR CALIBRATION

Use the following procedure for calibrating the relay if the relay has been taken apart for repairs or the adjustments disturbed.

For easier access to the parts, the relay should be tested without the case.

Part A Preliminary Settings

1. Set R9, R10, R11 resistors if they are adjustable type (located in front) using the following procedure: (To set resistors loosen the adjustable band and carefully move the band to a different setting. Retighten the band so not to damage resistance wires.)
   a. Remove the printed circuit board(s) (PCB) in the rear of the relay.
   b. Using a bridge type instrument, set the adjustable band next to the fixed terminal having the wire connection to measure 1600 (±35) ohms
   c. Set the second adjustable band from the same fixed terminal to measure a total 6000 (±100) ohms.
2. Set R_1-R_2-R_3-R4 potentiometers fully counter-clockwise for maximum resistance.
3. Set relay for S=1, M=+18 ("L" lead over "R" lead), all T=8.7, T_0=26.1 for the 1.0-31.0 ohm relays and for the .2-4.35 ohms relay all T=1.23

and T_0=3.69, or all T=5.8, T_0=17.4 for .75-20 ohms relay.

Part B Voltage Circuit Tests

1. Apply 3 phase balanced voltages as per test 1 of Fig. 23, except no current is applied.

2. Set $V_{AN} = V_{BN} = V_{CN}$ = 70 volts a-c. Measure following a-c voltages:

   From relay terminal 6 to S_A = 1 Tap
   70 (±1) volts

   From relay terminal 6 to S_A = 2 Tap
   140 (±2) volts

   From relay terminal 6 to S_A = 3 Tap
   221 (±3) volts

   From relay terminal 6 to R_A lead
   39.2 (±5) volts

   Repeat the same measurements for S_B, S_C, and R_B, R_C-leads.

3. Disconnect R_0-lead from M_0=0 Tap and measure the voltage from relay terminal "4" to the R_0-lead. It should be below 0.5 volts ac.

4. Apply rated d-c voltage to the relay. Check the d-c voltage across the lower set of plug-in terminals (rear view) "5" and "1" for the SDG-1, -2, -3, & -4 relays and terminals "6" and "4" for the SDG-relay. It should measure 20 (±2) volts. (Notice 250 V. d-c relay requires external resistor).

5. Plug in the lower and upper boards.

Part C Potentiometer Adjustments

NOTE: All potentiometers are the locked type and should be unlocked before adjustment and locked after adjustment is complete.

1. Set R1, R2, R3, R4, R5, R6, R7, R8 for maximum setting (counter-clockwise).

2. Measure the voltages with a Rectox type voltmeter across the specified terminals of the small upper terminal board located in the rear. All the following measurements are done on the small upper board. Terminal numbers refer to this board only.

R5-Adjustment

Measure the voltage across terminals 2 & 3. Adjust R5 until voltages across 4 & 2 and 4 & 3 are equal (±.1 volt) to each other and are within 1.0 volt of voltage across 2 & 3. If oscilloscope is available observe voltage across R9 and set R5 so that all peaks on the 360Hz ripple are equal.

R6-Adjustment

Measure the voltage across terminals 6 & 8. Adjust R6 until voltages across terminals 7 & 6 and 7 & 8 are equal (±.1 volt) to each other and are within 1.0 volt of voltage across 6 & 8. If oscilloscope is available observe voltage across R10 and set R6 so that all peaks are equal.

R-7 Adjustment

Measure the voltage across terminals 17 & 18. Adjust R7 until voltages across terminals 15 & 18 and 15 & 17 are equal (±0.1 volt) to each other and are within 1.0 volt of voltage across 17 & 18. If oscilloscope is available observe voltage across R11 and set R7 so that all peaks are equal.

R8-Adjustment

Reduce V_{AN} to zero and measure the voltage across terminals 11 & 12. Adjust R8 until voltages across terminals 14 & 11 and 14 & 12 are equal (±0.1 volt) to each other and are within 1.0 volt of voltage across 11 & 12. If oscilloscope is available observe voltage across R12 and set R8 so that all valleys are equal.

Maximum Torque Angle Adjustment

Disconnect all R & L-leads and Jumper Relay Terminals 5 and 6.

R-1 Adjustment

For the 1.0-31.0 ohm relay use the #1 test connection of Fig. 23. Apply 5.08 amp. a-c current to the relay. Set V_{AN} = 45 volts and $V_{BN} = V_{CN}$ = 0 volts. Set the phase shifter for 75° current lagging voltage. For the .75-20 ohm relay apply 7.6 amps.

For .20-4.35 ohm relay use the same procedure as above except set the current for 15.65 amp. and V_{AN} = 20.0 volts.

Insert an a-c voltmeter of 0-3 volts range between R_A-and L_A-leads. Adjust R1-potentiometer for a minimum ("null"-reading) and lock R1 in place. Vary current slightly to achieve lower "null" reading.

R2-Adjustment

Use #2 test connections of Fig. 23. Set V_{BN} = 45 volts and $V_{AN} = V_{CN} = 0$ volts. Set I_B = 5.08 amps. 75° lagging V_{BN}. (Modify voltage and current settings for the .2-4.35 ohm and .75-20 ohms relays as above). Measure the voltage between R_B & L_B leads. Adjust R2-potentiometer for a minimum ("null"-reading) and lock R2 in place.

R3-Adjustment

Use the #3 test connections of Fig. 23. Set V_{CN} = 45 volts and $V_{AN} = V_{BN} = 0$ volts. I_C = 5.08 amp. 75° lagging V_{CN}. (Modify voltage and current for the .2-4.35 ohm and .75-20 ohms relays as above).

Measure the voltage between R_C and L_C leads Adjust R3-potentiometer for a minimum ("null"-reading) and lock R3 in place.

R4-Adjustments

Remove jumper from relay terminals 5 and 6. Use the #4 test connections of Fig. 23. Connect all "L"-and "R"-leads back to previous setting. Set $V_{CN} = 0$ and $V_{AN} = V_{BN}$ = 70 volts. Set I_C = 2.34 amp. 75° lagging V_{CN}. (For the .2 to 4.35 relay set $V_{CN} = 0$ and $V_{BN} = V_{AN}$ = 45 volt. I_C = 9.9 amperes). Measure the voltage between R_0 and the lowest M_0-tap marked "0". Adjust the R-4 potentiometer for minimum voltage ("null"-reading) and lock R4 in place. For 0.75-20 ohms relay set $V_{CN} = 0$, $V_{AN} = V_{BN}$ = 70 volts, I_C = 3.51 amps.

Part D.M-Taps Check

Use a Rectox type voltmeter

M_A-Taps — Use test connection #1 of Fig. 23. Pass 10 amp. current through the relay. The voltage should read the following:

1.5 (±2) volts	For	between 0 tap and .03 tap
6.0 (±2) volts	1-30	between 0 tap and .09 tap
9.0 (±2) volts	Ohms	between 0 tap and .06 tap

1.0 (±.1) volts	For	between 0 tap and .03 tap
4.0 (±.1) volts	.75-20	between 0 tap and .09 tap
6.0 (±.1) volts	Ohms	between 0 tap and .06 tap

M_B-Taps-Use test connection #2 and repeat above.

M_C-Taps-Use test connection #3 and repeat above.

M0-Taps-Use test connection #4 and repeat above.

For .2-4.35 ohm relay

NOTE: Provide a jumper from terminal 19 to center tap of the T_0 tap block for the SDG, SDG-1, and -3 relays.

M_A-Taps-Use test connection #1 of Fig. 23. Pass 20 amp. of current through relay. The voltage should read the following:

.425 (±.05 volts)	between "0" tap and ".03" tap
1.70 (±.1 volts)	between "0" tap and ".09" tap
2.55 (±.1 volts)	between "0" tap and ".06" tap

M_B-Taps-Use test connection #2 and repeat above.

M_C-Taps-Use test connection #3 and repeat above.

M_0-Taps-Use test connection #4 and repeat above.

Part E Impedance Tests

Tripping is indicated for the SDG relay when the 25 watt lamp shown on Fig. 23 turns on and for SDG-1, -2, -3 & -4 relays when DC voltmeter indicates minimum deflection of 5 volts for balance point condition, but should rise over 18 v.d.c. when current is increased. Refer to Fig. 23 for all test connections.

For .2-4.35 Ohm Relay

A. Use connections for test No. 5 and set V_{AN} voltage = 20 volts. $V_{BN} = V_{CN}$ = 70 volts. Set the phase shifter for 75° current lagging voltage.

B. The relay current required to make the trip should be between 8.0-8.6 amp.

C. Use connections for Test No. 6 and set V_{BN} voltage = 20 volts. $V_{AN} = V_{BN}$ = 70 volts. Set the phase shifter as above. The SDG relay trip current should be 8-8.6 amp.

D. Use connections for Test No. 7 and set VCN = 20 volts. $V_{AN} = V_{BN}$ = 70 volts. Set the phase shifter as above. The SDG relay trip current should be 8.0-8.6 amp.

For 1.0-31.0 Ohm Relay

A. Use connections for test #5 and set V_{AN} = V_{BN} = V_{CN} = 70 volts. Set phase shifter for 75° current lagging voltage. The relay trip current should be 3.95-4.20 amperes. (5.95-6.30 amp. for .75-20 ohm relay)

B. Use connections for test #6 and set V_{AN} = V_{BN} = V_{CN} = 70 volts, and set the phase shifter as above. The relay trip current should be 3.95-4.20 amperes. (5.95-6.30 amp. for .75-20 ohm relay)

C. Use test connections for test #7 and set V_{AN} = V_{BN} = V_{CN} = 70 volts. Set the phase shifter as above. The relay trip current should be 3.95-4.20 amperes. (5.95-6.30 amp. for .75-20 ohm relay)

If it is desired to check relay response at some other settings use following equation for the trip value of current.

$$I = \frac{3V_{LN}}{(2+p)\,Z_1}, \text{ Where } p = \frac{Z_0}{Z_1}$$

Z_0 = Zero sequence reach

Z_1 = Positive sequence reach (in above cases p = 3)

WARNING: If testing requires trip current over 15 amp. over prolonged periods, it is recommended that a heavy short lead be connected from terminal 19 to the center tap of T_0-socket. Also connect a jumper lead from terminal 16 to terminal 1 on the large printed circuit board for SDG-1 and SDG-3 relays and terminal 2 to terminal 4 for SDG-relay.

(Lower set of terminals rear view).

Let V_{AN} = V_{BN} = V_{CN} = 70 volts.

Change all the S-setting to S = 3 and repeat the impedance test. Trip current for the 1.0-31.0 ohm relay should be 2.66-2.87 amp. and 9.4-10.0 amp. for the .2-4.35 ohm relay and 4.0-4.30 amp for .75-20 ohms relay.

LOW-VOLTAGE BALANCE POINT CALIBRATION

When performing this test on SDG, SDG-1, or SDG-3 relays that have 1.0-30.0 ohms reach or .75-20.0 ohms reach disable I_0-circuit by jumpering terminal 16 to 1 on large printed circuit board for SDG-1 and SDG-3 relays and terminals 2 and 4 for SDG-Relay.

SDG – SDG-1 – SDG-2 Relays

1. Use connection #5. Set V_{AN} = 2.5V, V_{BN} = V_{CN} = 70V. Set phase shifter for current lagging voltage by 75°. Check pick-up current. Note it.

2. Use connection #6. Set V_{BN} = 2.5V. V_{AN} = V_{CN} = 70V. Check pick-up current. Note it.

3. Use connection #7. Set V_{CN} = 2.5V. V_{AN} = V_{BN} = 70V. Check pick-up current. Note it.

The pick-up currents for each test should be within the following limits.

.2-4.35 ohms	1.05-1.15 amp.
.75-20.0 ohms	.208-.232 amp.
1.0-31.0 ohms	.140-.155 amp.

If the currents are outside their limits the following procedure should be followed. Set V_{AN} = V_{BN} = V_{CN} = 70 volts as close to each other as possible. Use connection #5. No current is applied. Measure DC-voltage across R9, R10, R11-resistors. Readjust potentiometers P5, P6, P7 until the voltages across R9, R10, R11 are as close to each other as possible. These voltages should be in 20-25 volts range. In most cases only slight adjustment of P5, P6 or P7 will be required. Then recheck pickup current again. If the pickup currents are close together but outside the specified limits, change R_X-resistor to lower value for lower pickup current, and conversely increase it for higher values of pickup. Note the P5, P6, P7 are interacting. Hence, recheck all three voltages after each adjustment. If difficulties in balancing at 2.5 volts persist, use the same test as for SDG-3 and SDG-4 below.

SDG-3 and SDG-4

Same procedure as above except use 5 volts instead of 2.5 volts as low-voltage check point the pickup currents should be as below:

.2-4.35 ohms	2.10-2.30 amp.
.75-20.0 ohms	.416-.464 amp.
1.0-30.0 ohms	.280-.310 amp.

Use the same P5-P6-P7 adjustment procedure as above.

Indicating Contactor Switch (when used)

With the relay tripped, pass sufficient d-c current through the trip circuit to close the contacts of ICS. This value of current should be not less than 1.0 ampere, nor greater than 1.2 amperes for the 1 ampere ICS. The current should not be greater than the particular ICS Setting being used for the 0.2-2.0 amperes ICS. The operation indicator target should drop freely.

The contact gap should be approximately 0.047'' for the 0.2-2.0 ampere unit and 0.070'' for the 1.0 ampere unit between the bridging moving contact and the adjustable stationary contacts. The bridging moving contact should touch both stationary contacts simultaneously.

RENEWAL PARTS

Repair work can be done most satisfactorily at the factory. However, interchangeable parts can be furnished to the customers who are equipped for doing repair work. When ordering parts, always give the complete nameplate data, and component style number given in the electrical parts list.

ELECTRICAL PARTS LIST

Circuit Symbol	Description	Westinghouse Style Number
Printed Circuit Board (SDG-1, -2)		836A777H01
(SDG-3 & 4) (Fig. 26)		836A777H03
	DIODES	
D1 to D24	B2N9	837A692H04
D37-D38-D62-D67-D70	1N3283	837A692H02
	CONTACT STRIP	
		187A637H02
Printed Circuit Board		670B499H01
(SDG) (Fig. 27A) -125V.D.C.		670B499H01
(SDG-1 & 3) (Fig. 27B)		670B499H02
(SDG-2 & 4) (Fig. 27C)		670B499H03
(SDG) (Fig. 27A) 48V.D.C.		670B499H04
	CAPACITORS	
C13-C14-C15	.5 MFD.	187A624H03
	DIODES	
D54-D55	1N4385	184A855H14
	RESISTORS	
R52 (125 V.D.C.)	2.2K	763A127H11
R56	700 Ohms 2W	763A127H28
R52 (48 V.D.C.)	21 Ohms 3W	763A127H33
Large Printed Circuit Board (SDG) (Fig.)28)		411C213H01
	CAPACITORS	
C5-C7	2 MFD.	184A662H07
C6	.25 MFD.	187A624H02
C8-C10-C19-C20	.02 MFD.	187A624H09
C12	2.2 MFD.	187A508H19
C9	.10 MFD.	187A624H01
C11	.56 MFD.	764A278H08
	DIODES	
D40 to D49-D51-D52 D57-D59-D60-D61 D64 to D66-D87	1N4385	184A855H14
D50	M4L2053	629A370H04
D29-D30-D32 D33-D35-D36	1N3283	837A692H02
D72	CER69	188A342H06
D26-D27	B2N9	837A692H04
D53	1N3283	837A692H02
	TUNNEL DIODES	
TD3, TD58	1N3713	836A602H01
TD4-TD5	1N2928	836A602H02

Circuit Symbol	Description	Westinghouse Style Number
Printed Circuit Board (SDG) (Fig. 28) Cont.		
	ZENER DIODES	
Z3	1R200	629A369H01
Z4	1N759A	837A693H01
Z5	1N3805A	185A089H05
	POTENTIOMETER	
R45	2.5K Ohm-¼W.	629A430H03
	RESISTORS	
R17	100 Ohm-½W.	629A531H08
R18	56 Ohm-½W.	629A531H02
R19	1.5K Ohm-½W.	629A531H36
R20-R21-R46	2.7K Ohm-½W.	629A531H42
R24	22K Ohm-½W.	629A531H64
R25-R26	68K Ohm-½W.	629A531H76
R28	2.7K Ohm-½W.	629A531H42
R29-R30	39K Ohm-½W.	629A531H70
R31-R37-R36	470K Ohm-½W.	629A531H24
R32-R33	1K Ohm-½W.	629A531H32
R34	6.2K Ohm-½W.	629A531H51
R35	20K Ohm-½W.	629A531H63
R38	8.2K Ohm-½W.	629A531H54
R65	5.6K Ohm-½W.	629A531H50
R43	2K Ohm-½W.	629A531H39
R48	3.3K Ohm-½W.	629A531H44
R49	2K Ohm-½W.	836A503H33
R27	30K Ohm-½W.	629A531H67
R42	47K Ohm-1 W.	629A371H17
R44	1K Ohm	629A531H32
R55	2K Ohm	629A531H39
R53-R54	2K Ohm-½W.	836A503H33
R57	2K Ohm-1 W.	187A643H34
	TRANSISTORS	
Q2-Q5-Q6	2N1132	184A638H20
Q3-Q4	2N336	184A638H06
Q1-Q8	2N697	184A638H18
Q7	2N3417	848A851H02
	SWITCHES	
QS2-QS3	2N886	185A517H03
	TRANSFORMER	
T1	—	629A453H02

ELECTRICAL PARTS LIST

Circuit Symbol	Description	Westinghouse Style Number
Printed Circuit Board (SDG) (Fig. 28) (Cont.)		
	TRANSISTOR RADIATOR	
		188A002H01
Printed Circuit Board (SDG-1) (Fig. 29)		411C822G01
	(SDG-2)	411C830G01
	(SDG-3)	411C831G01
	(SDG-4)	411C832G01
	CAPACITORS	
C5	2 MFD.	184A662H07
C6	.10 MFD.	187A624H01
C7-C9-C19-C20	.02 MFD.	187A624H09
C8	.10 MFD.	187A624H01
C10	.56 MFD.	764A278H08
C11	2.2 MFD.	187A508H19
	DIODES	
D26-D27	B2N9	837A692H04
D40-D43 to D53-D56-D58-D59-D64 to D66-D87 to D90	1N4385	184A855H14
D72	CER69	188A342H06
D29-D30-D32 D33-D35-D36	1N3283	837A692H02
D39-D5	1N3283	837A692H02
	TUNNEL DIODES	
TD1-TD3	1N2928	836A602H02
TD2-TD4 (D57)	1N3713	836A602H01
	ZENER DIODES	
Z3	1N9578	186A797H06
Z4	1N3686B	185A212H06
Z5	1N759A	837A693H01
Z6	1N3805A	185A089H05
	POTENTIOMETERS	
R48	2.5K	629A430H03
	RESISTORS	
R57	2K Ohm-1W.	187A643H34
R17	100 Ohm-½W.	629A531H08
R18	56 Ohm-½W.	629A531H02
R30-R65	4.7K Ohm-½W.	629A531H48
R22-R26	22K Ohm-½W.	629A531H64
R23	27K Ohm-½W.	629A531H66
R24	4.7K Ohm-½W.	629A531H48
R19	1.5K Ohm-½W.	629A531H36
R28-R37-R38	1K Ohm-½W.	629A531H32
R31-R32-R51	2.7K Ohm-½W.	629A531H42

Circuit Symbol	Description	Westinghouse Style Number
Printed Circuit Board (SDG-1) (Fig. 29) (Cont.)		
(SDG-2)		
(SDG-3)		
(SDG-4)		
	RESISTORS	
R33-R34	68K Ohm-½W.	629A531H76
R35-R36	39K Ohm-½W.	629A531H70
R39	6.2K Ohm-½W.	629A531H51
R21	30K Ohm-½W.	629A531H67
R40	20K Ohm-½W.	629A531H63
R41	1.5K Ohm-½W.	836A503H30
R42-R68	470K Ohm-½W.	629A531H24
R43	8.2K Ohm-½W.	629A531H54
R44	2K Ohm-½W.	836A503H33
R46	47 Ohm-1 W.	629A371H17
R47	2K Ohm-½W.	629A531H39
R49	3.3K Ohm-½W.	629A531H44
R50	1K Ohm-½W.	629A531H32
R54-R66	5.6K Ohm-½W.	629A531H50
R55	2K Ohm-½W.	629A531H39
R58-R59	2K Ohm-½W.	836A503H33
	TRANSISTORS	
Q1-Q5-Q7-Q13	2N697	184A638H18
Q2-Q6-Q10-Q11	2N1132	184A638H20
Q8-Q9	2N336	184A638H06
Q3	2N3391	848A851H01
Q12	2N3417	848A851H02
	SWITCHES	
QS1	2N1881	184A640H08
QS2-QS3	2N886	185A517H03
	TRANSISTOR RADIATOR	
		188A002H01
Printed Circuit Board SDG-SDG-1-2 (2 ϕ - Ground)		670B739
	TRANSISTORS	
Q17	2N697	184A638H18
Q18	2N1132	184A638H20
	DIODES	
D73 to D80 D82-D84 to D86	1N4385	184A855H14
	RESISTOR	
R13 to R15	15K-5W.	763A129H09
R20 (SDG-1 or -2)	4.7K-½W.	629A531H48
R40 (SDG)	4.7K-½W.	629A531H48

INDEX TO FIGURES

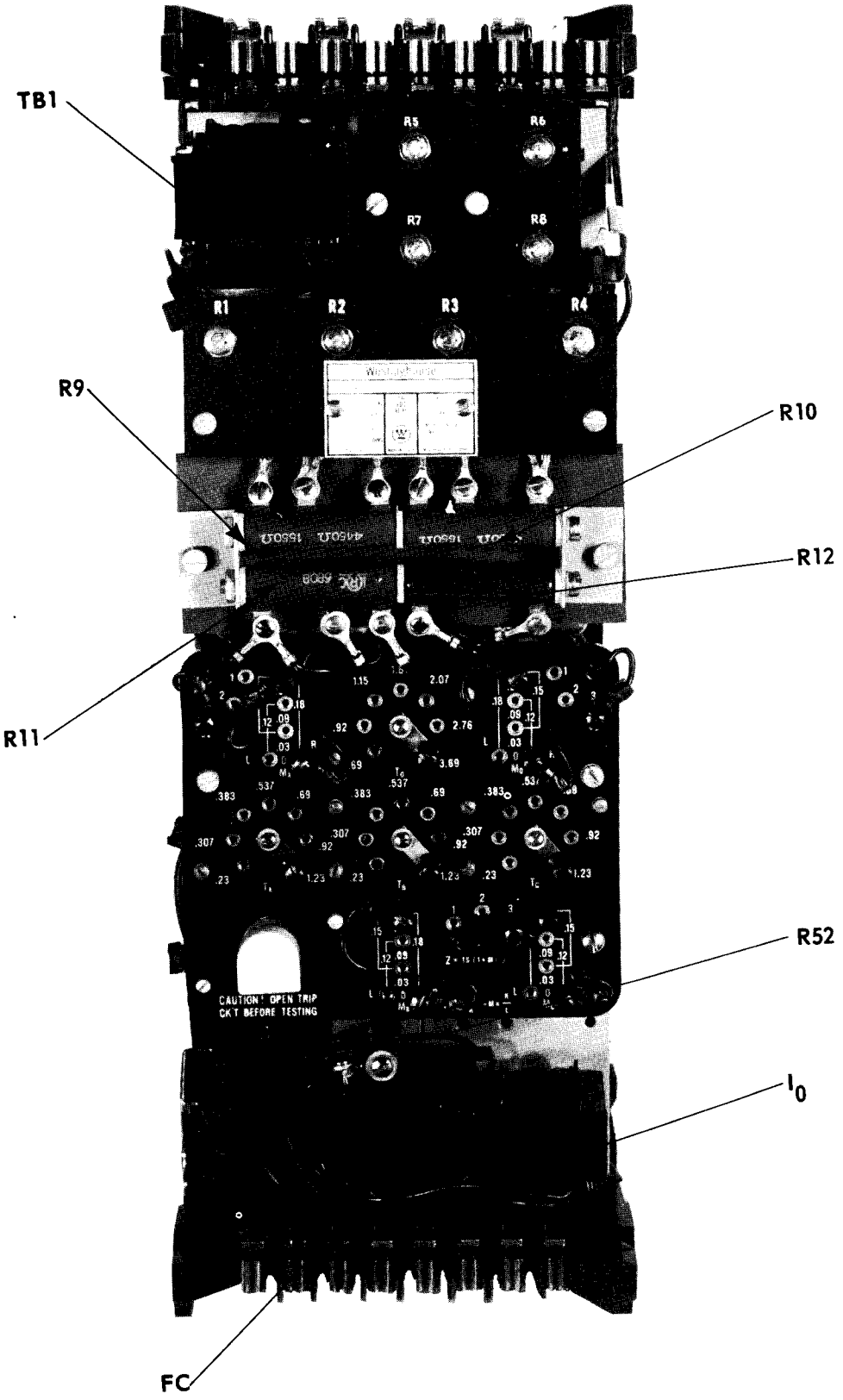


Fig. 1. Type SDG-1 Relay Without Case (Front View)

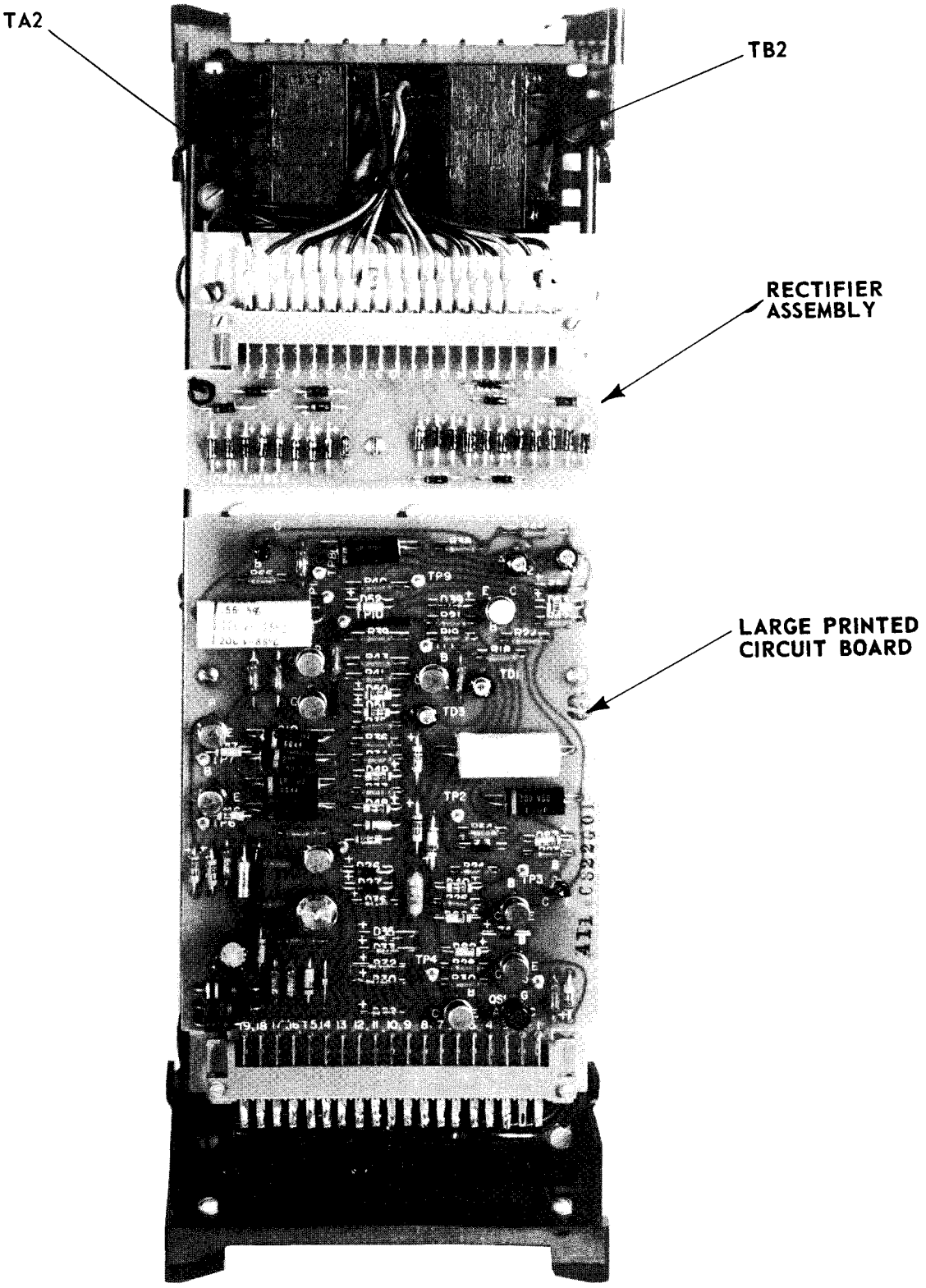


Fig. 2. Type SDG-1 Relay Without Case (Rear View)

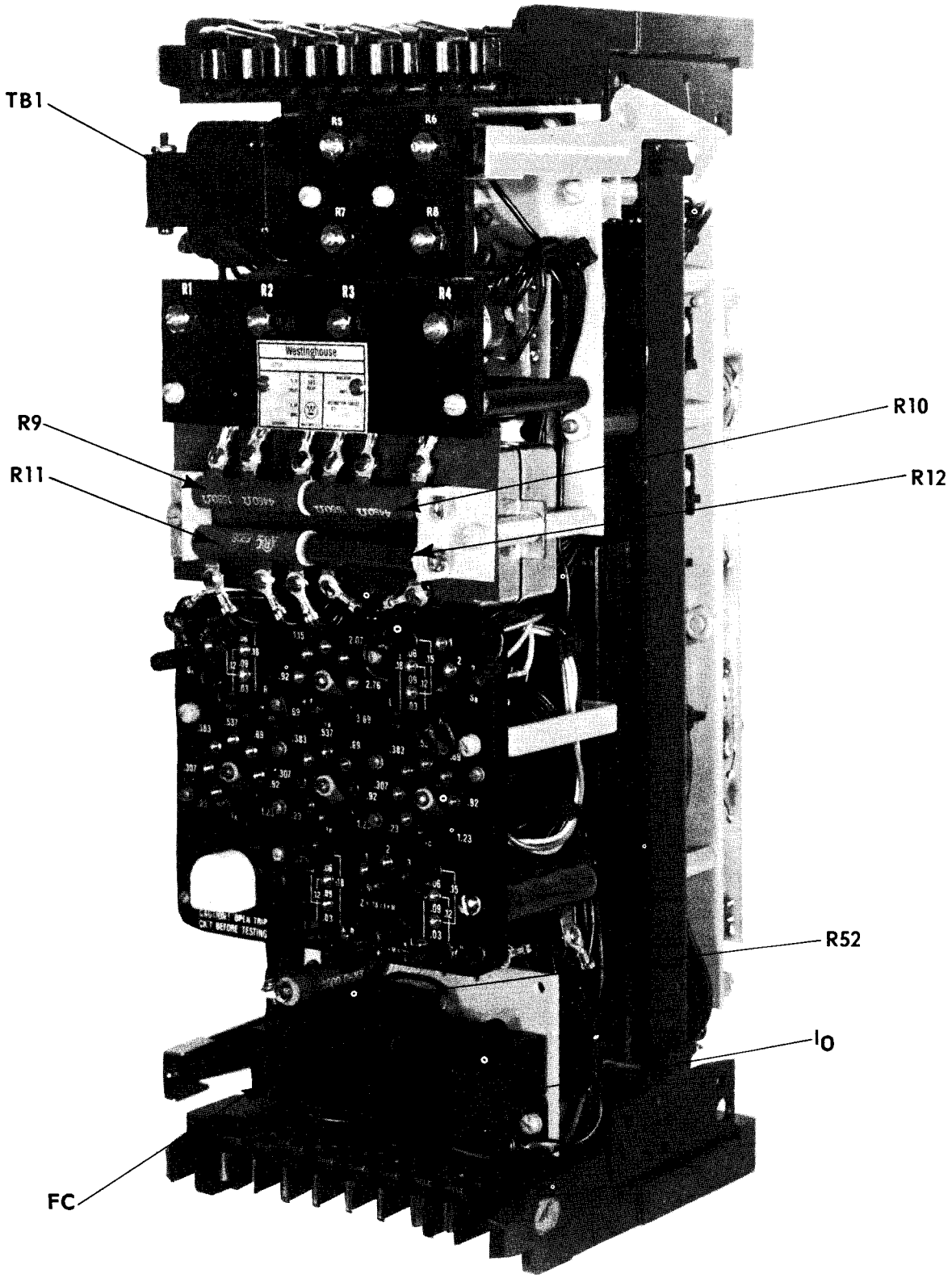


Fig. 3. Type SDG-1 Relay Without Case (Side View)

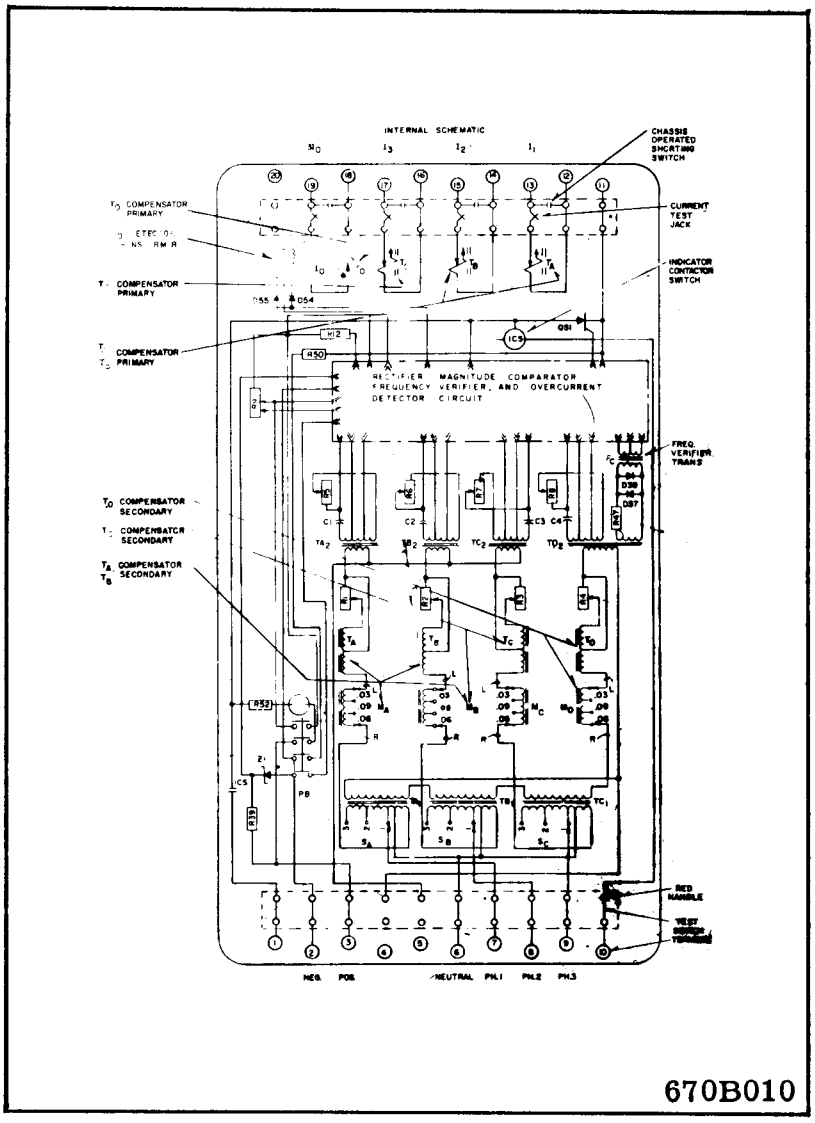


Fig. 4. Internal Schematic of the Type SDG Relay in FT-42 Case

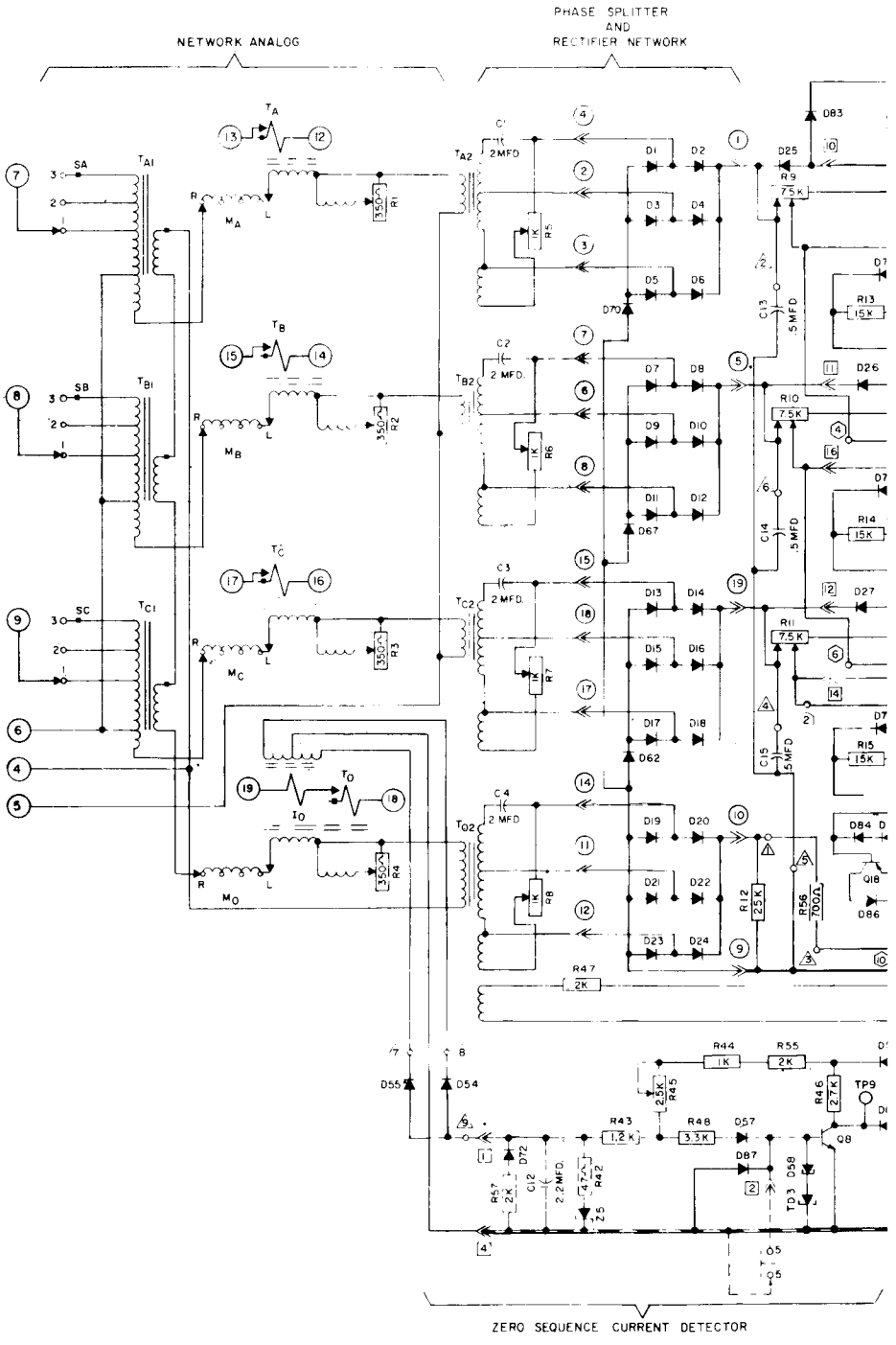


Fig. 5. Detailed Internal

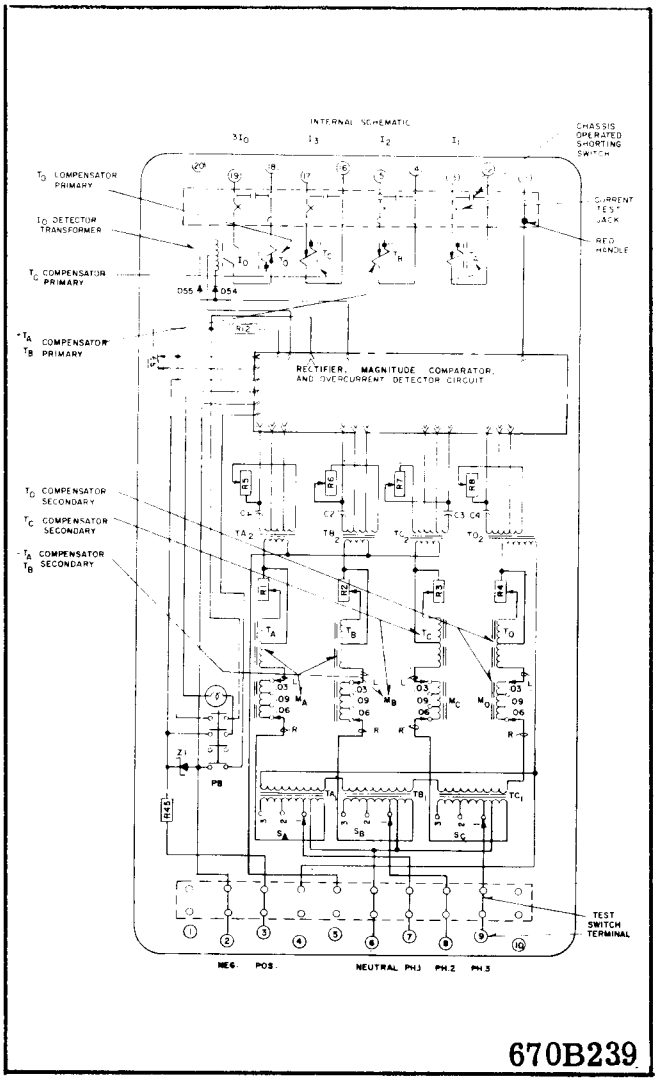


Fig. 8. Internal Schematic of the Type SDG-3 Relay in FT-42 Case

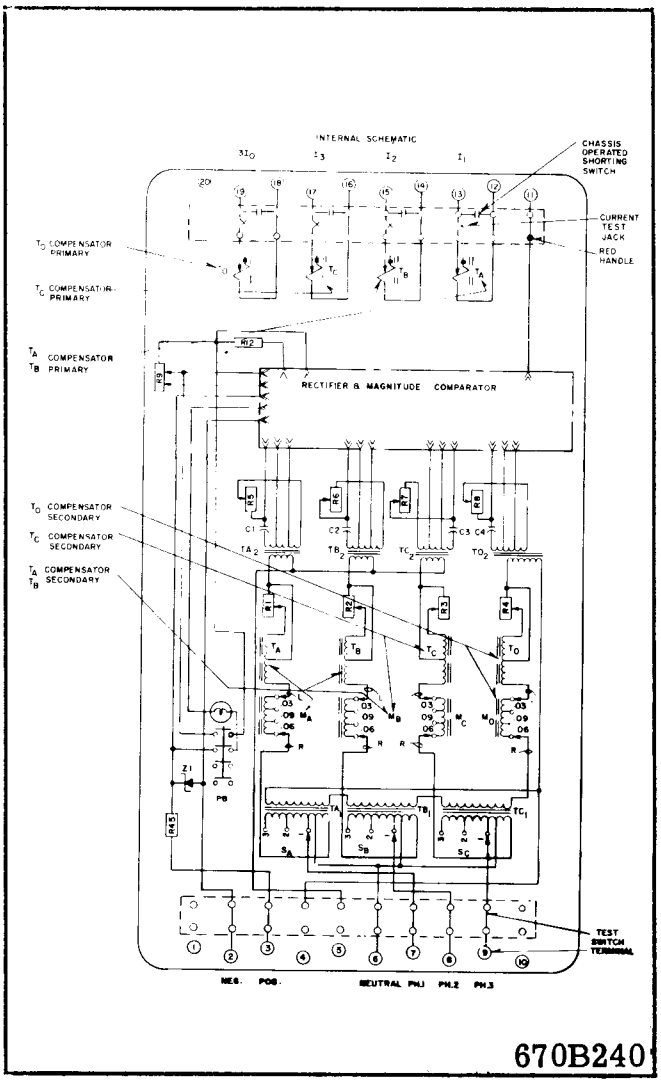
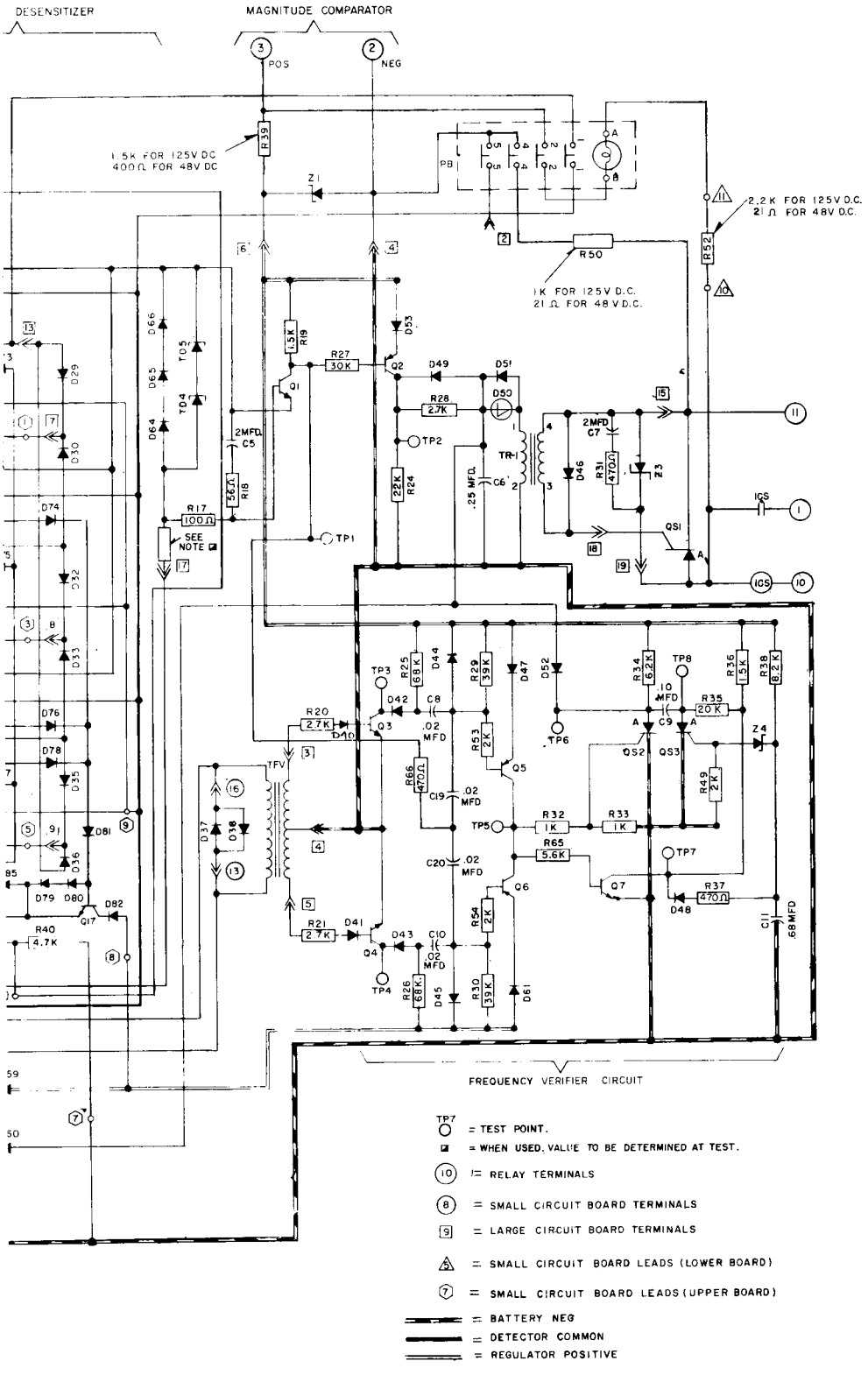


Fig. 9. Internal Schematic of the Type SDG-4 Relay in FT-42 Case



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Schematic of SDG Relay

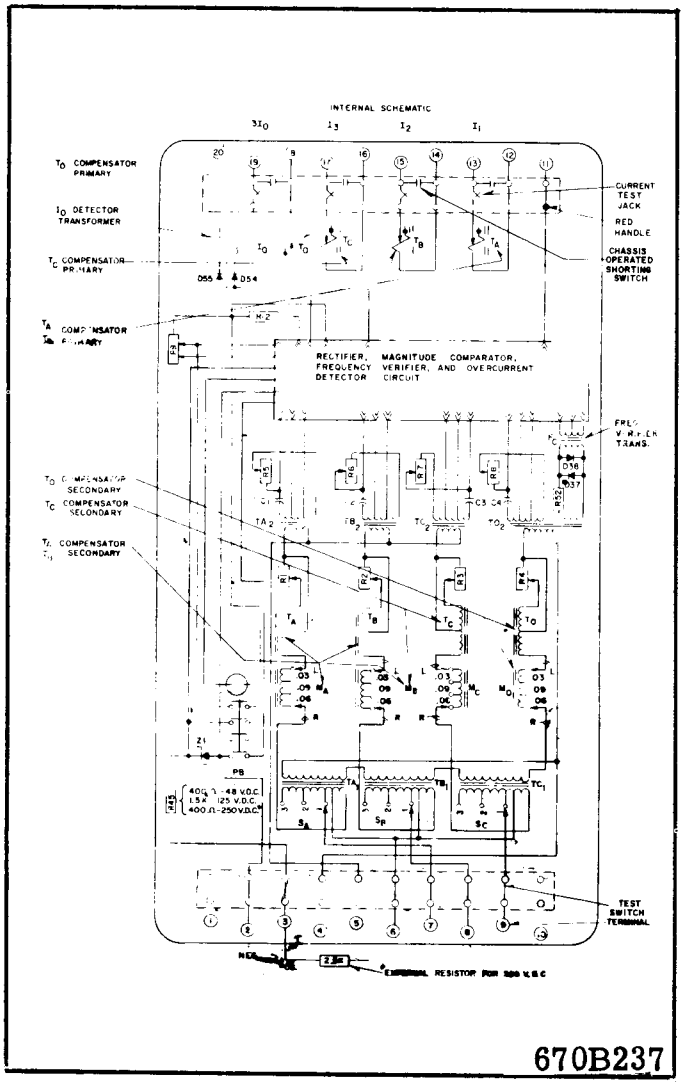


Fig. 6. Internal Schematic of the Type SDG-1 Relay in FT-42 Case

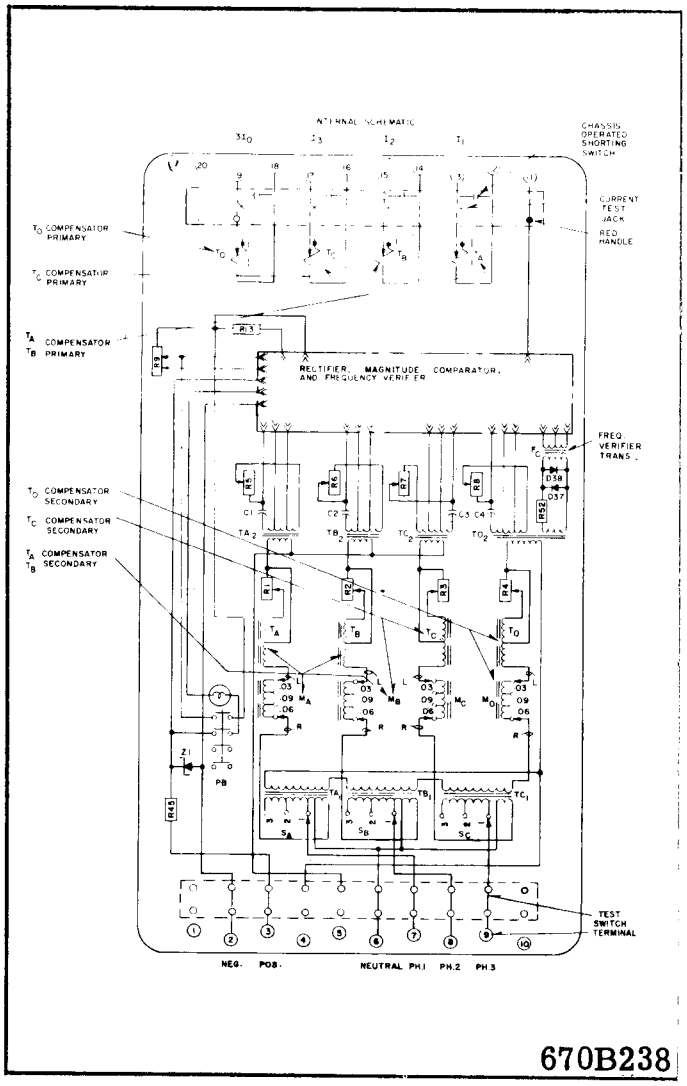


Fig. 7. Internal Schematic of the Type SDG-2 Relay in FT-42 Case

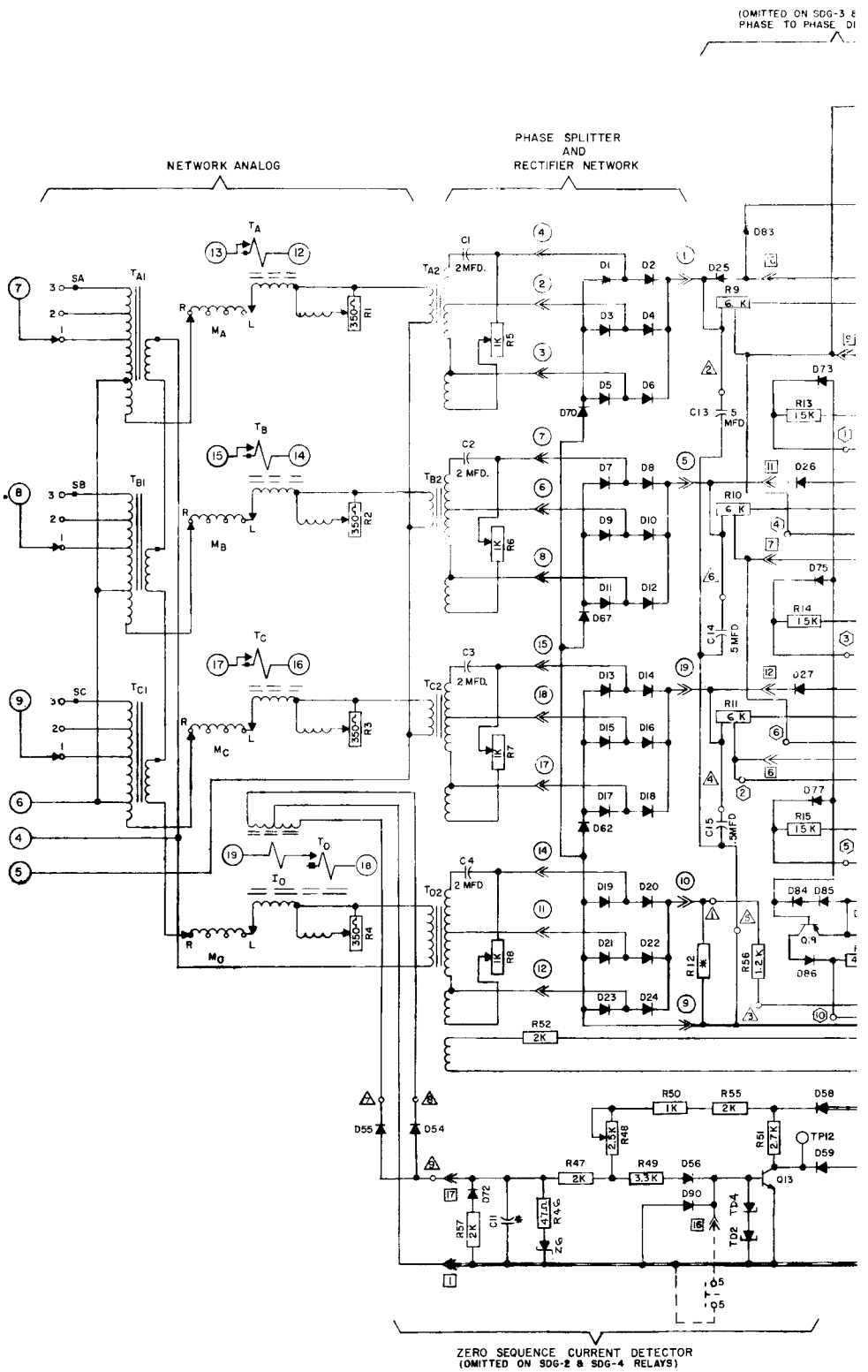


Fig. 10 Detailed Internal Schematic o

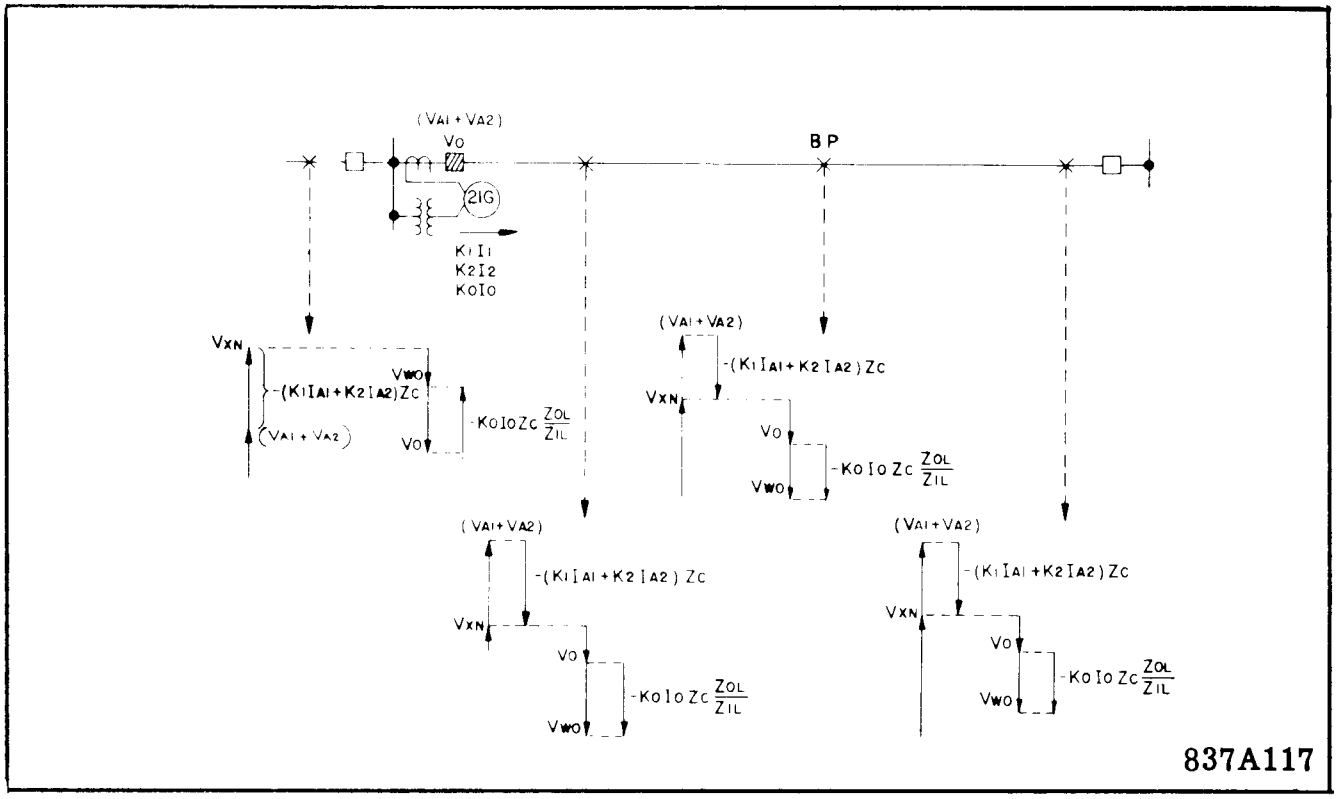


Fig. 14. Relay Voltages for A-to-Ground Faults at Selected Points

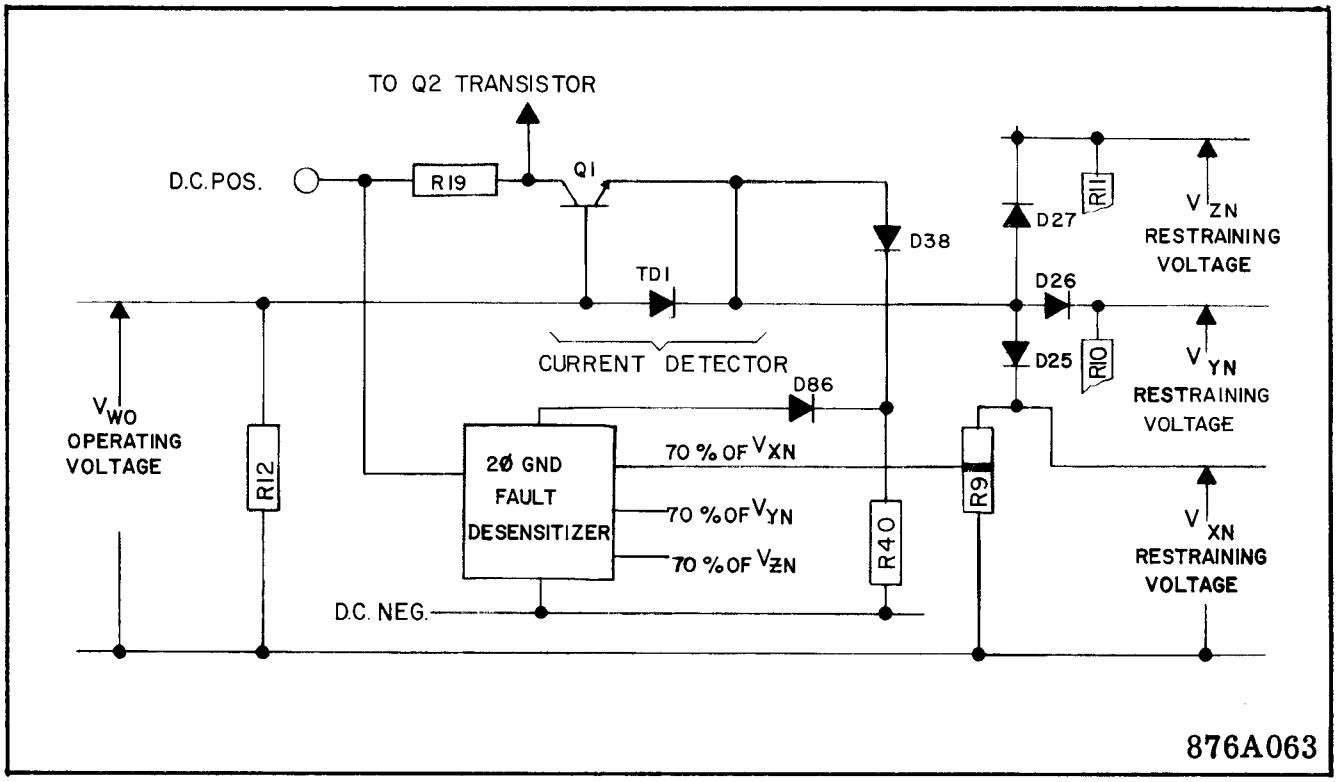
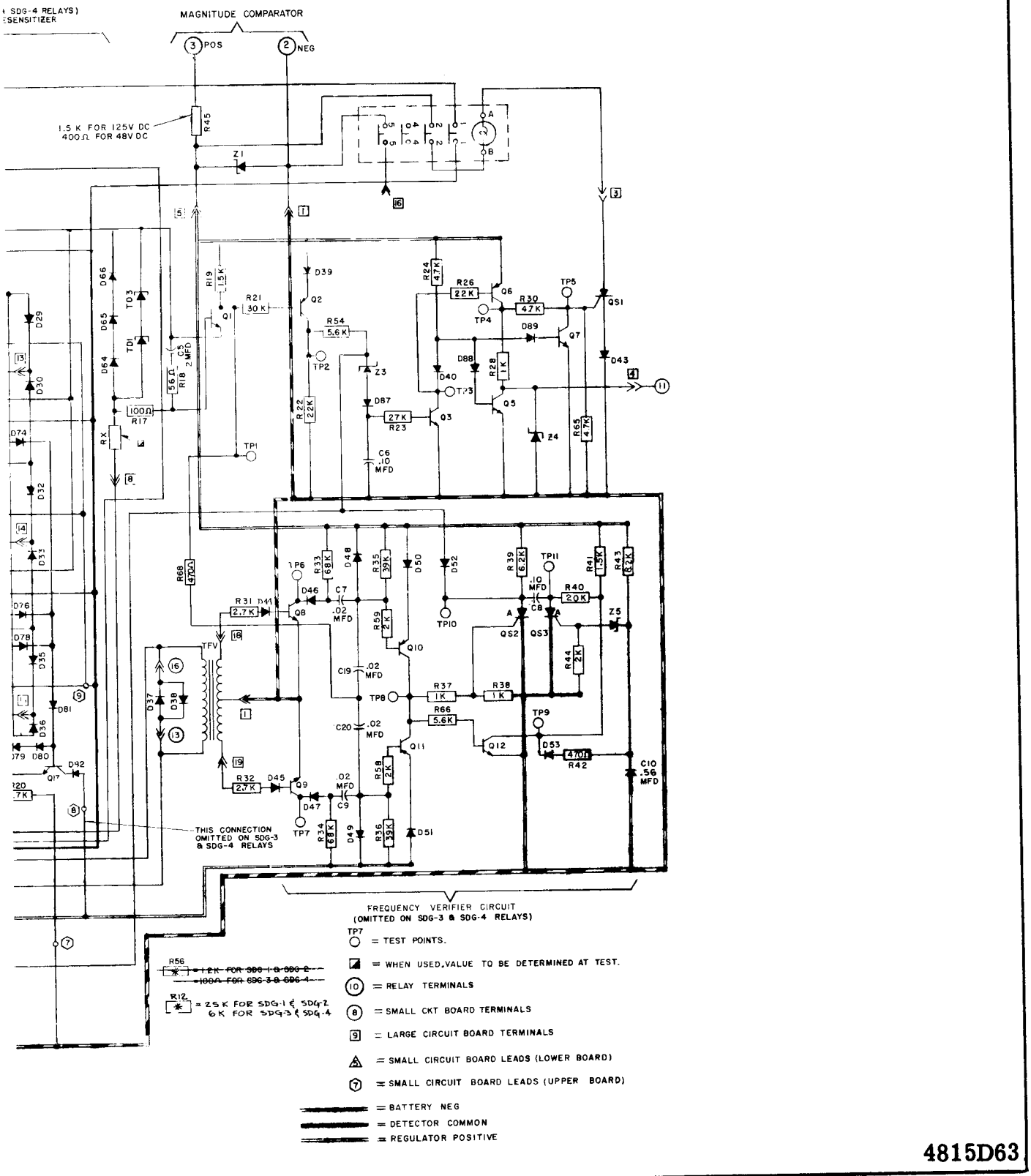


Fig. 15. Magnitude Comparator Circuit



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f the SDG-1, 2, 3, & 4 Relays

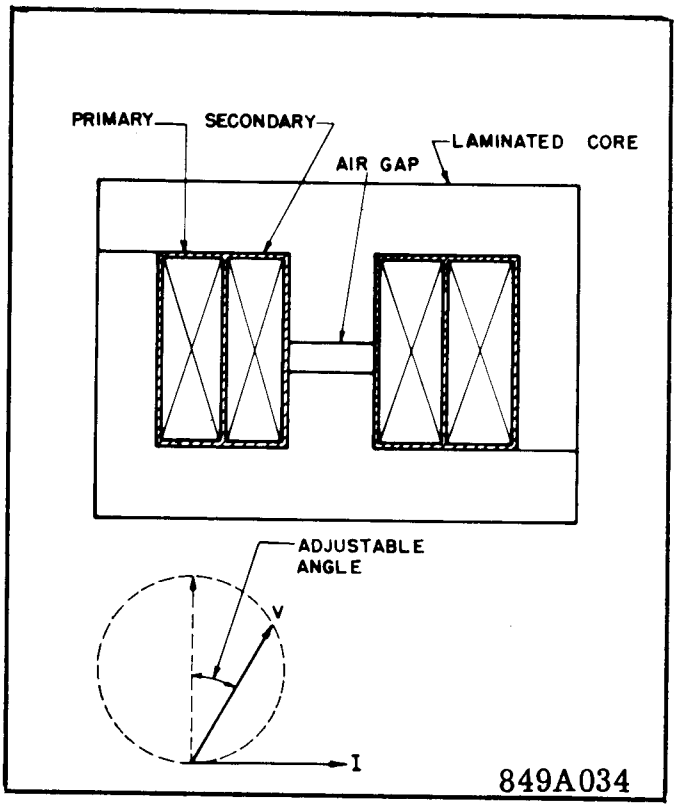


Fig. 11. Compensator Construction

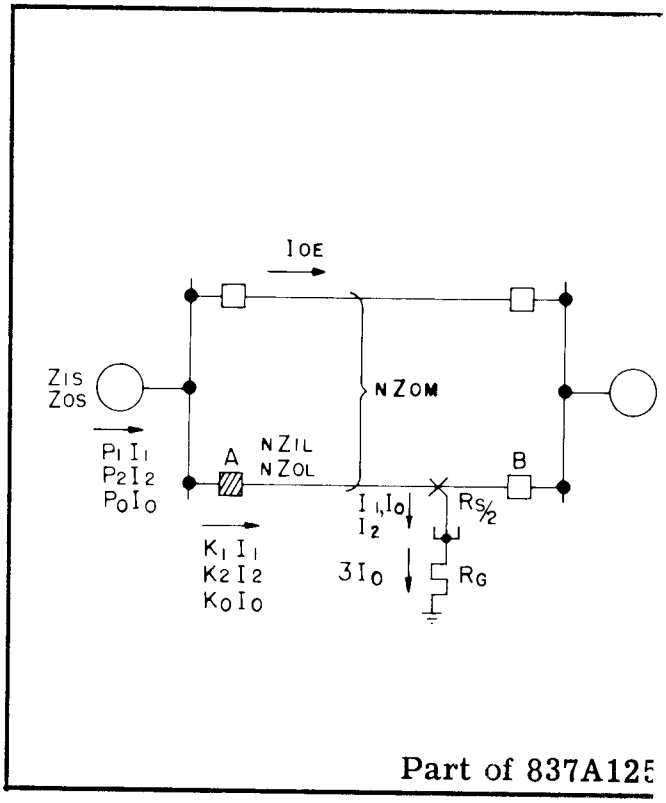


Fig. 12. Definition of Terms

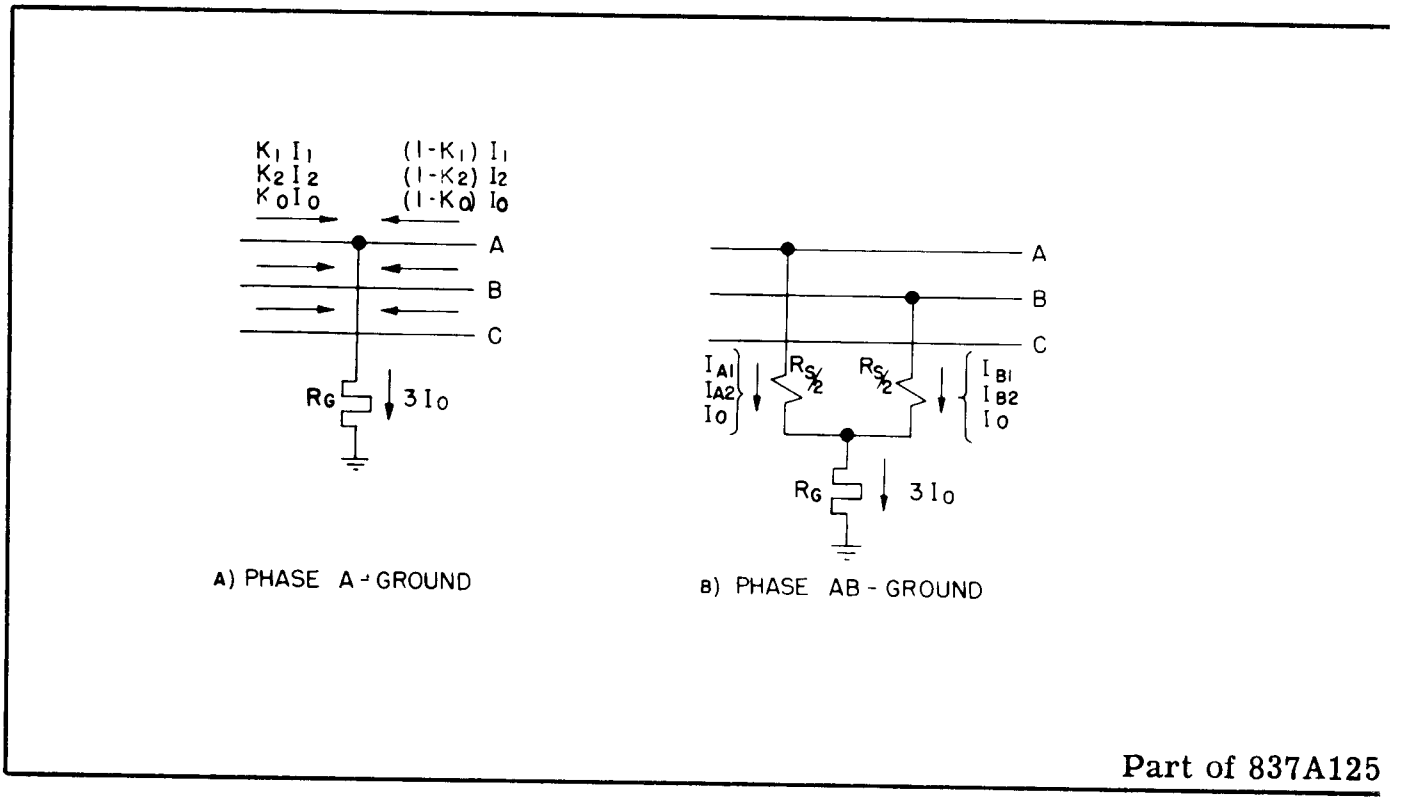


Fig. 13. Fault Resistance

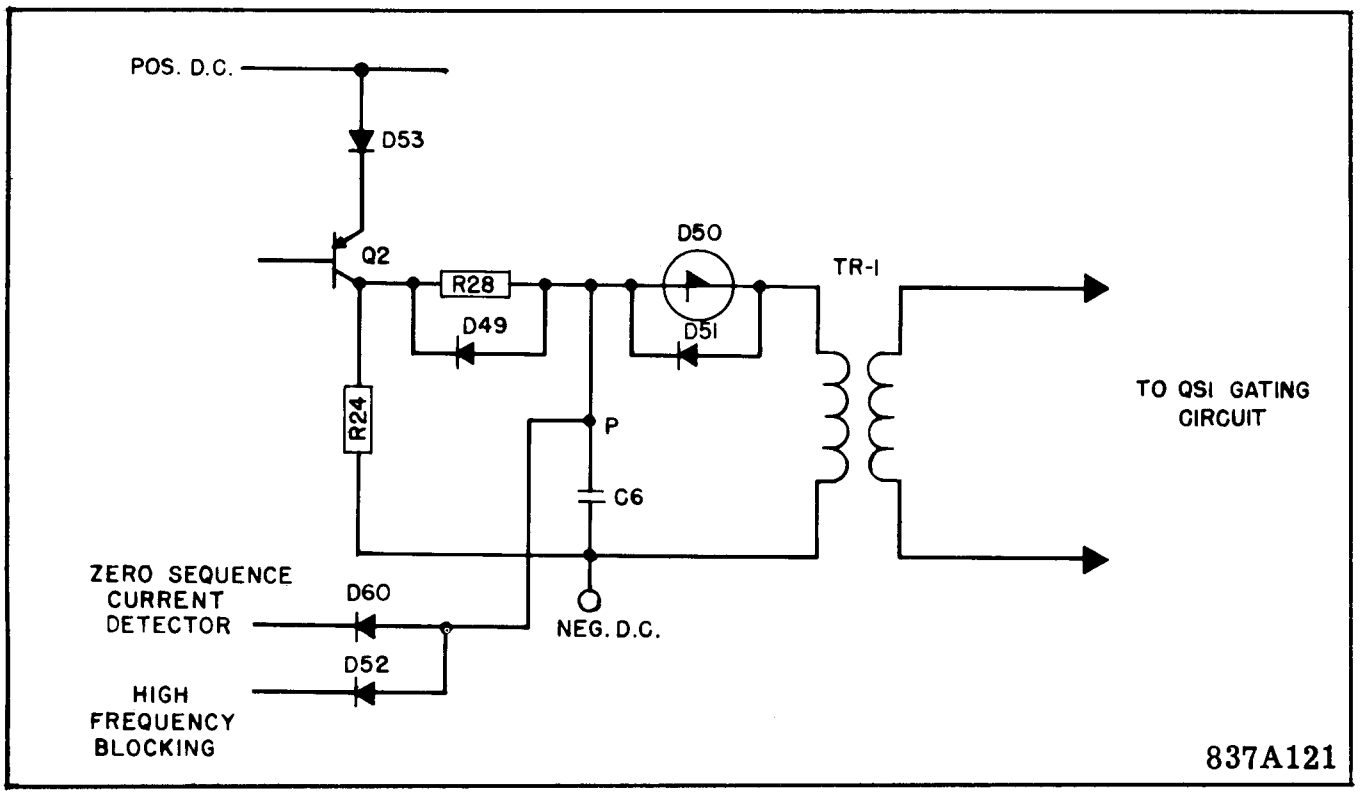


Fig. 16. Triggering Circuit

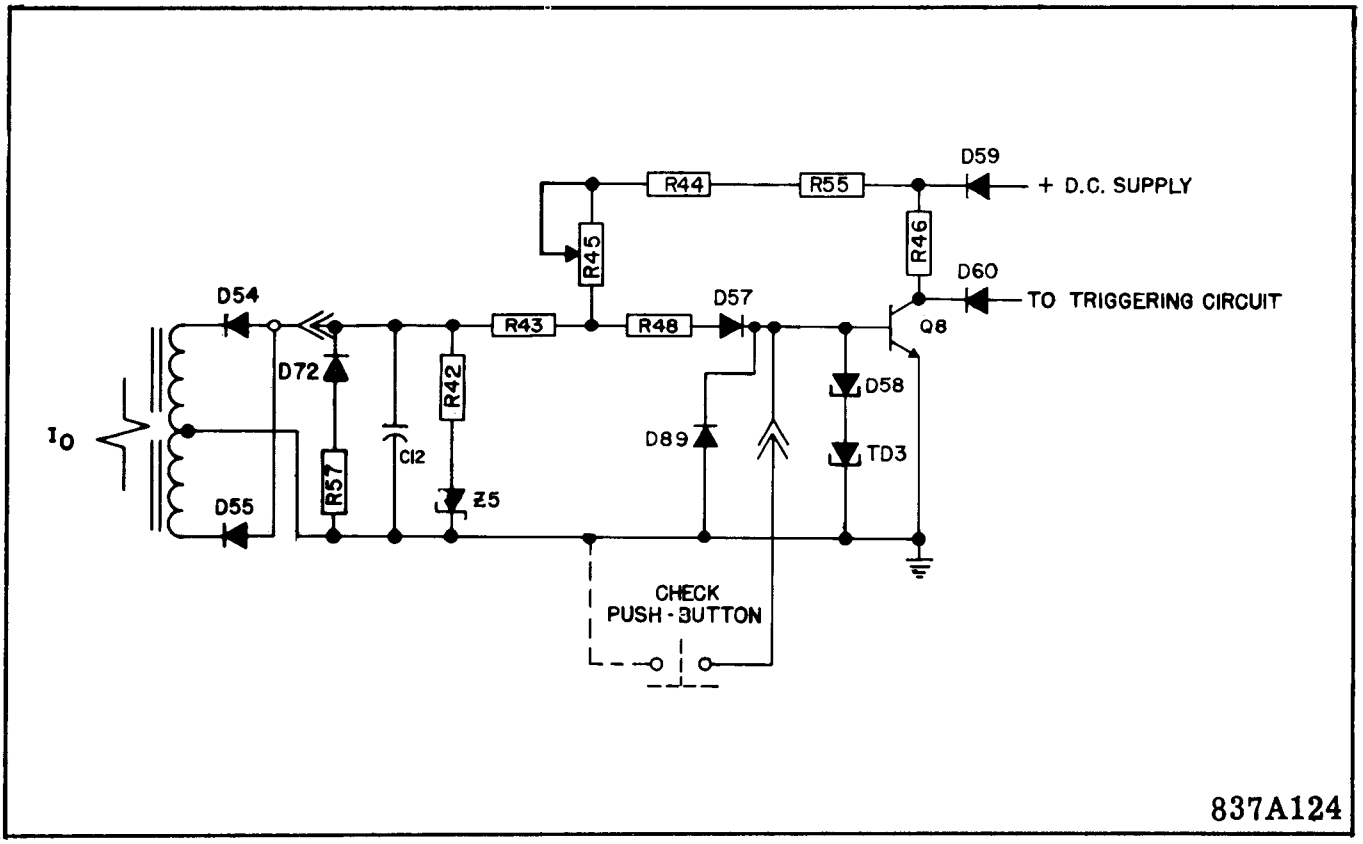


Fig. 17. Zero Sequence Current Detector Circuit

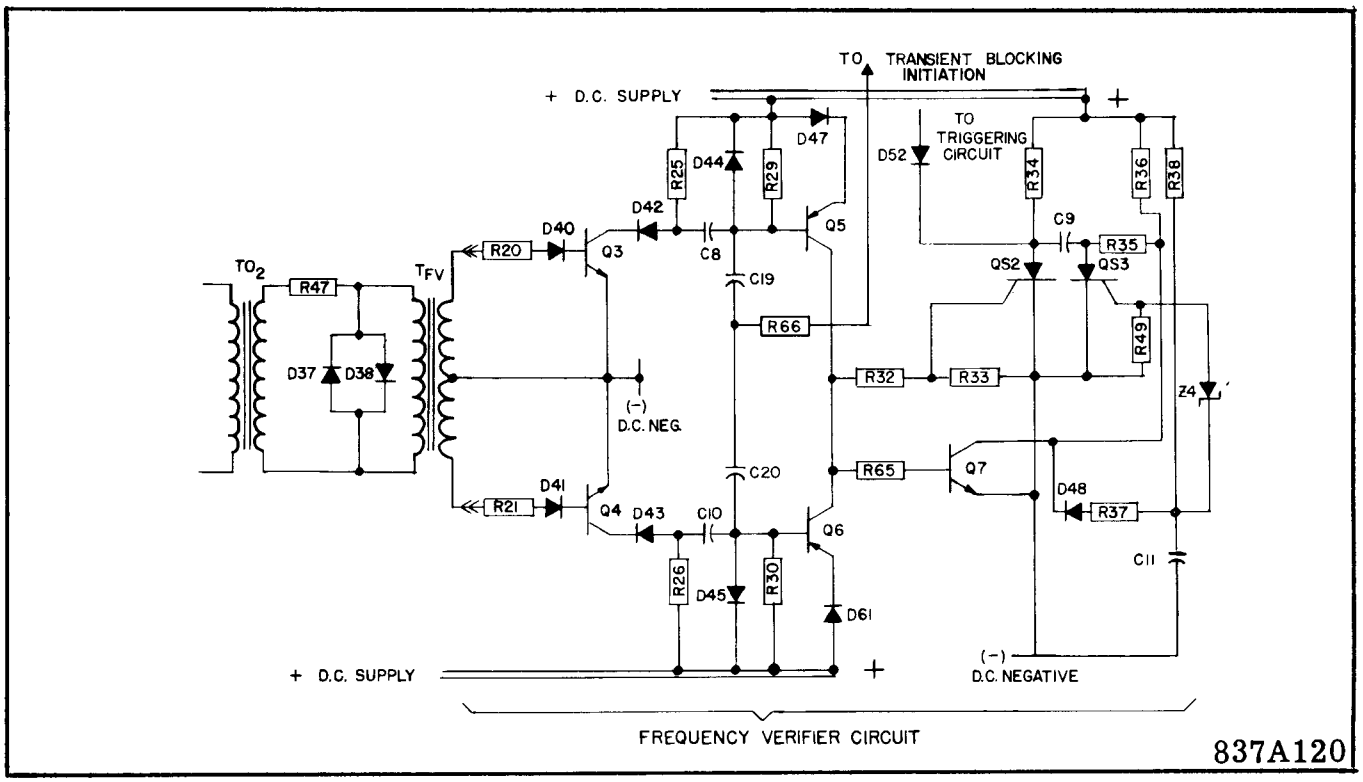


Fig. 18. Frequency Verifier Circuit

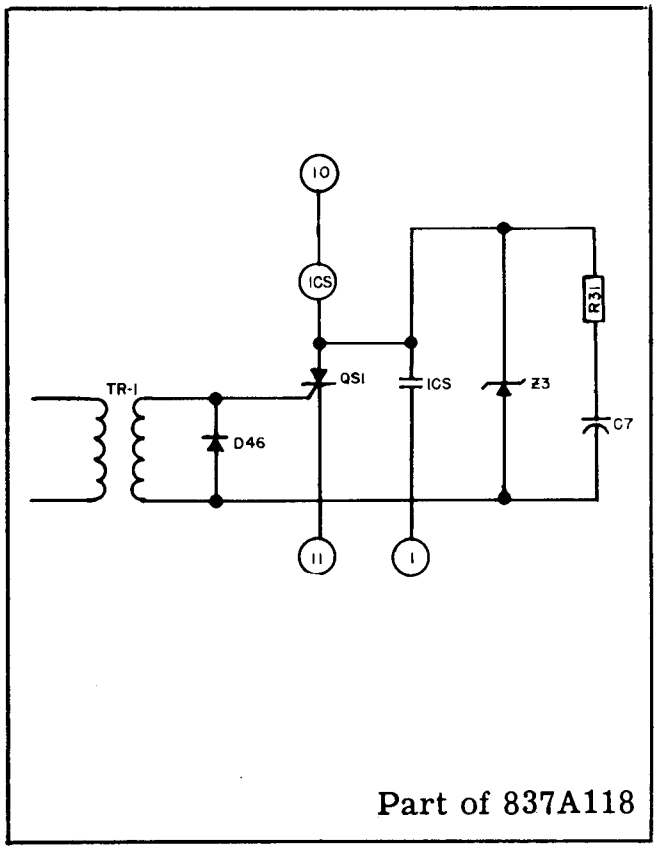


Fig. 19. Output Circuit of the SDG Relay

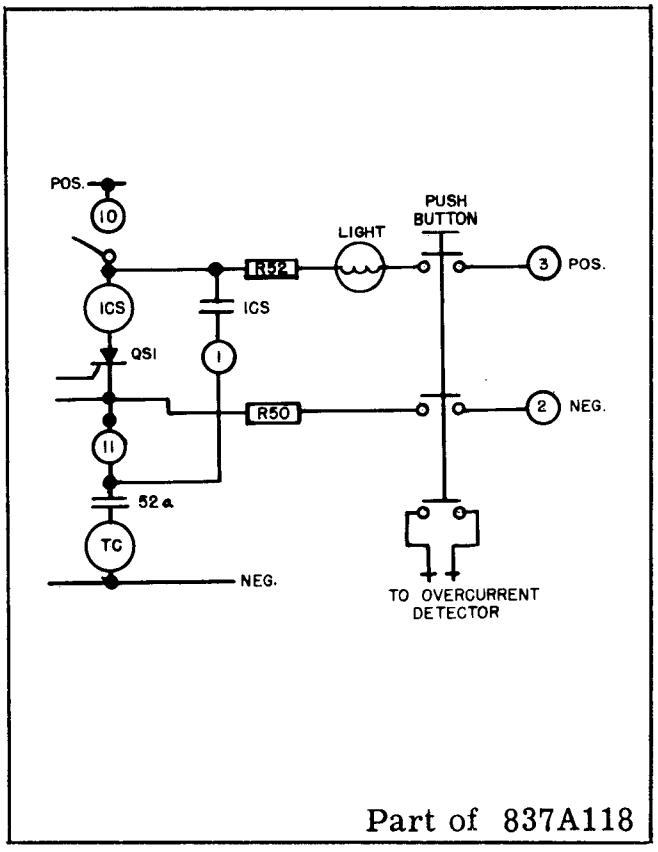


Fig. 20. Push Button "In Service Check" in the SDG Relay

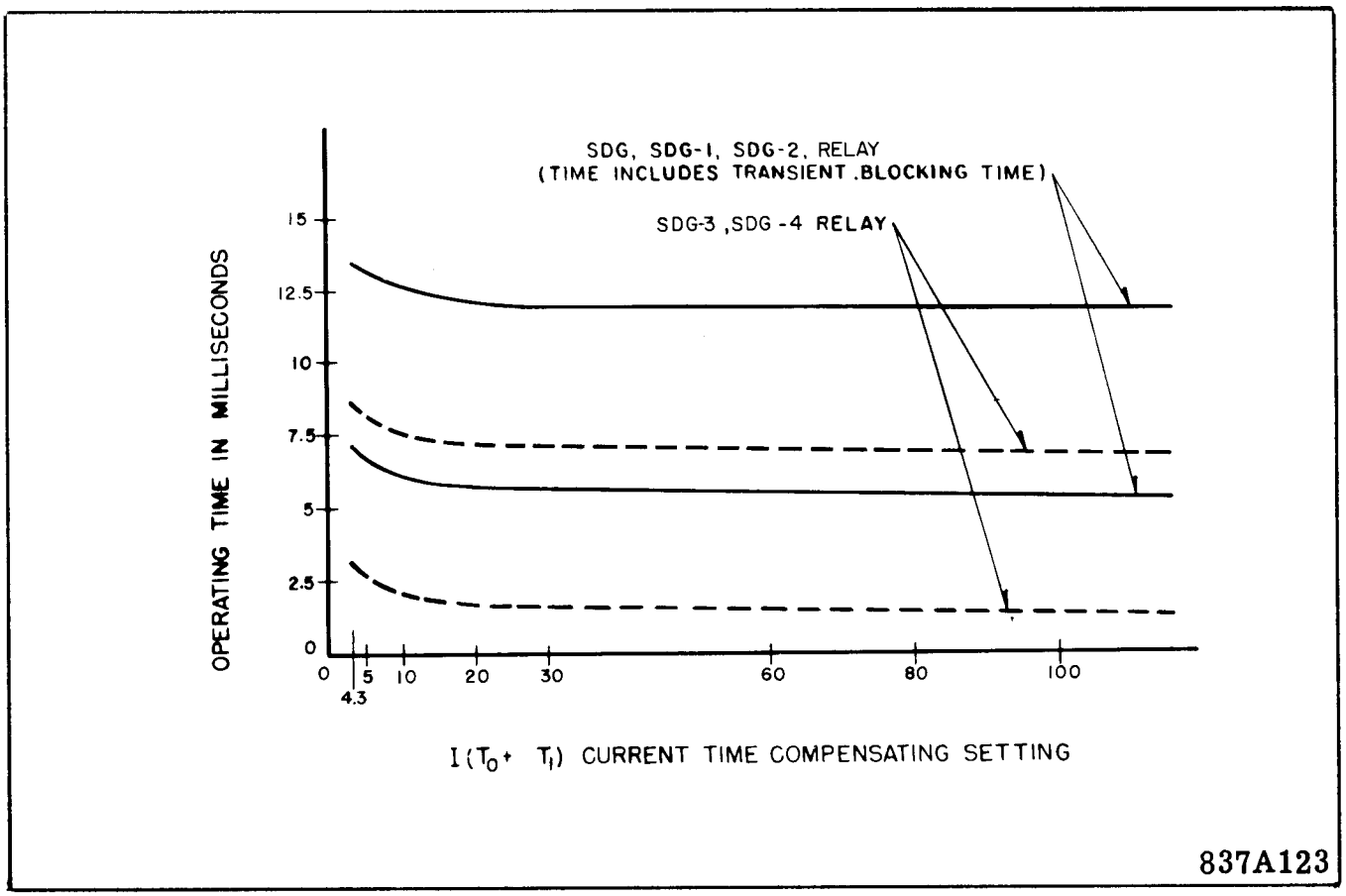


Fig. 21. Typical Operating Time Curves of the Type SDG-Line Relay

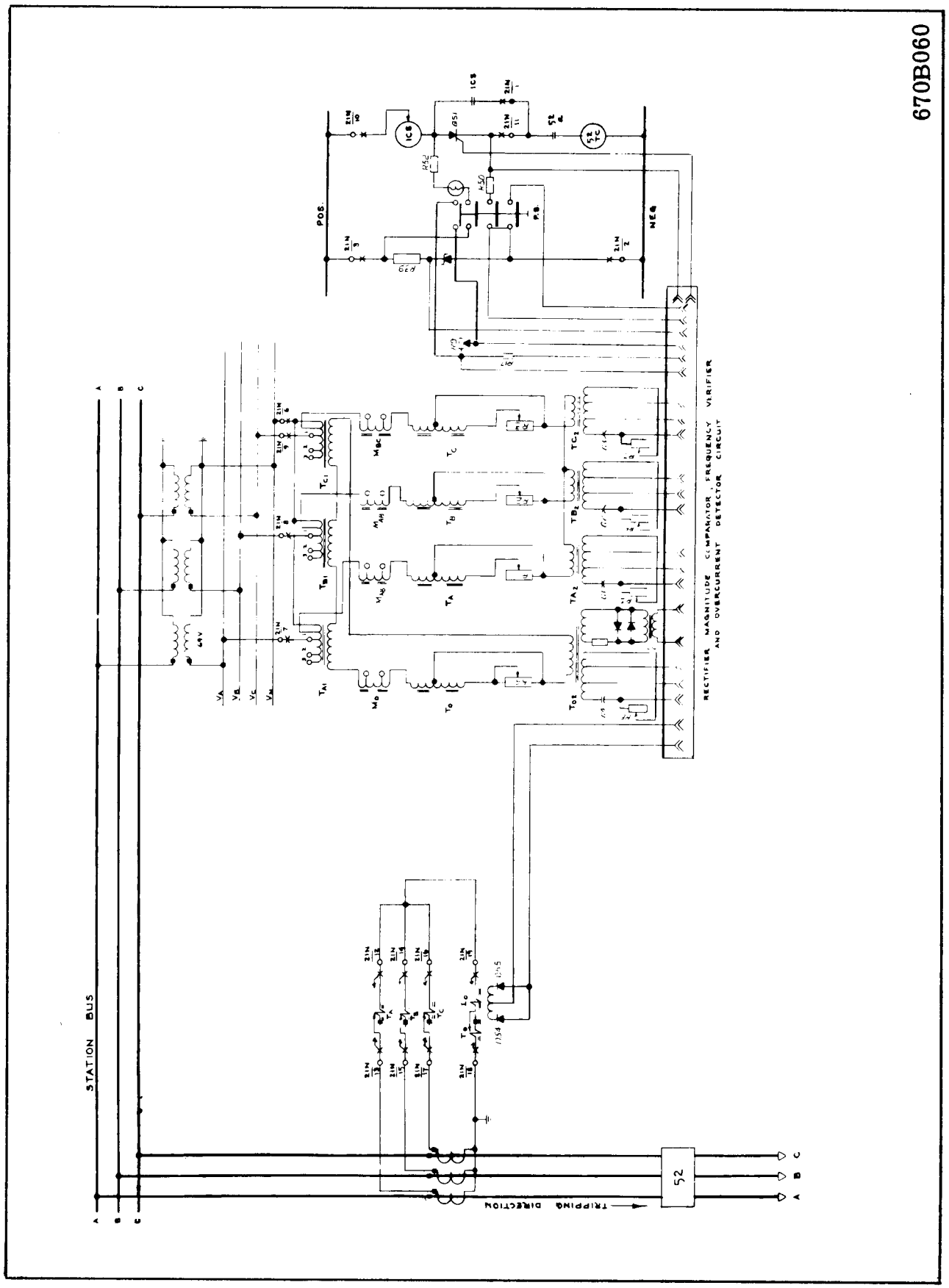
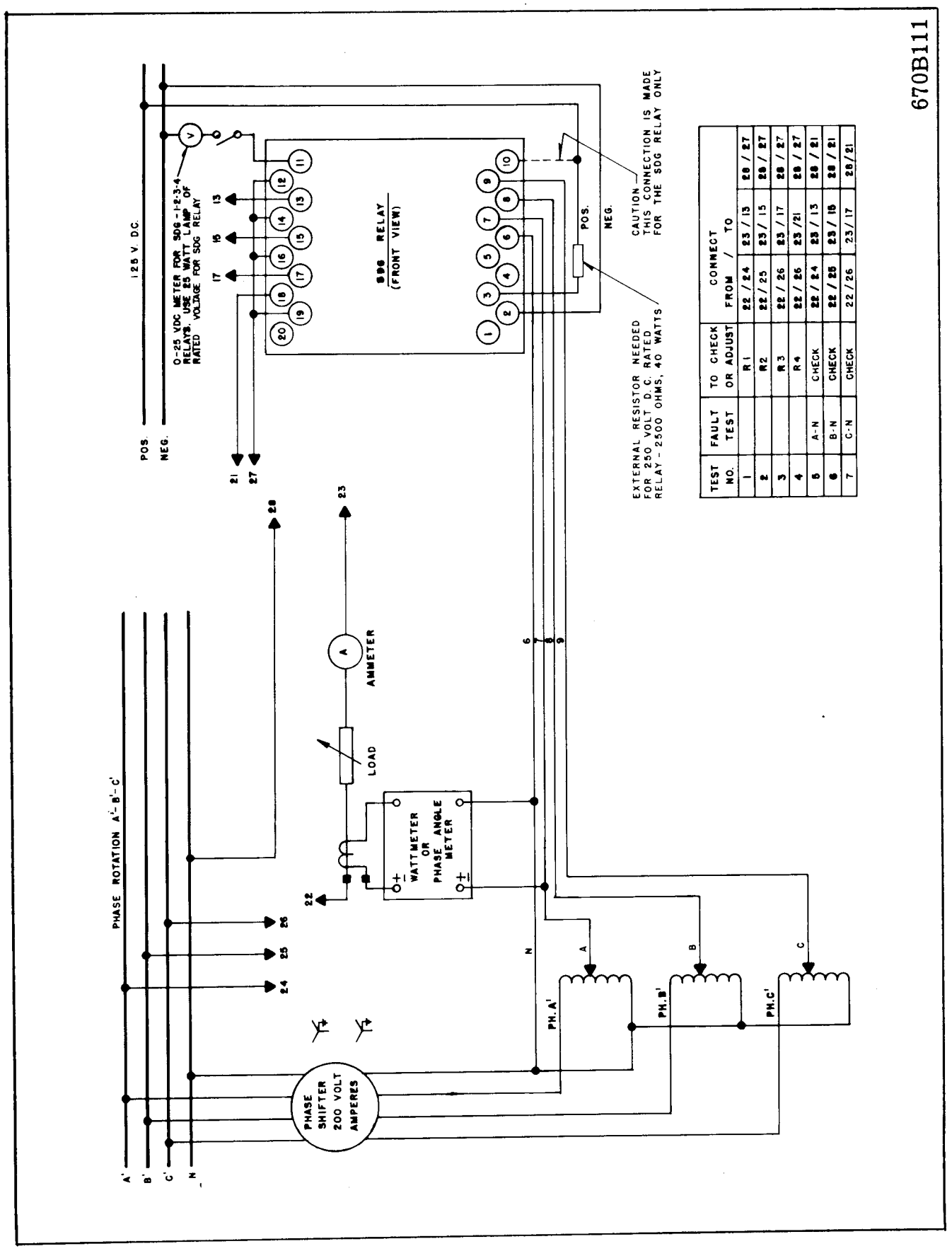
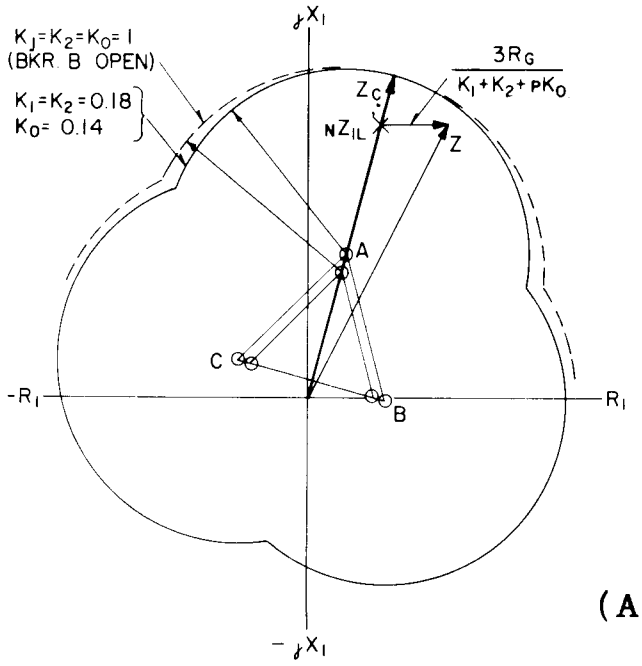


Fig. 22. External Connections for the SDG Relay



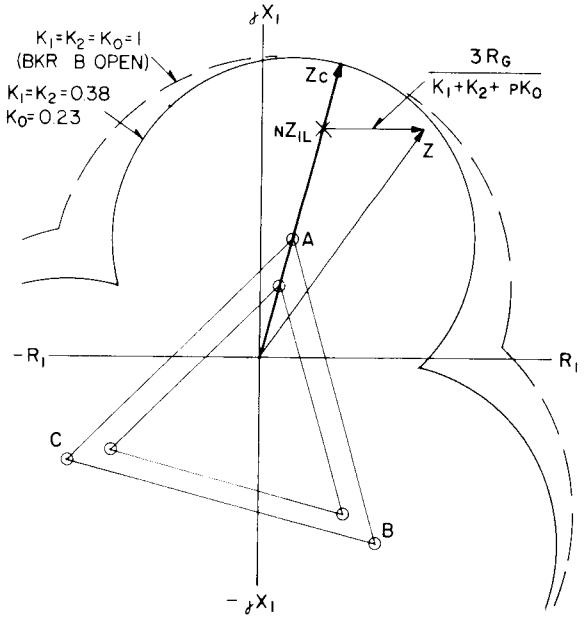
TEST NO.	FAULT TEST	TO CHECK OR ADJUST	CONNECT FROM / TO		
1		R1	22 / 24	23 / 13	28 / 27
2		R2	22 / 25	23 / 15	28 / 27
3		R3	22 / 26	23 / 17	28 / 27
4		R4	22 / 26	23 / 21	28 / 27
5	A-N	CHECK	22 / 24	23 / 13	28 / 21
6	B-N	CHECK	22 / 25	23 / 15	28 / 21
7	C-N	CHECK	22 / 26	23 / 17	28 / 21

Fig. 23. Test Connections for the SDG Line Relays



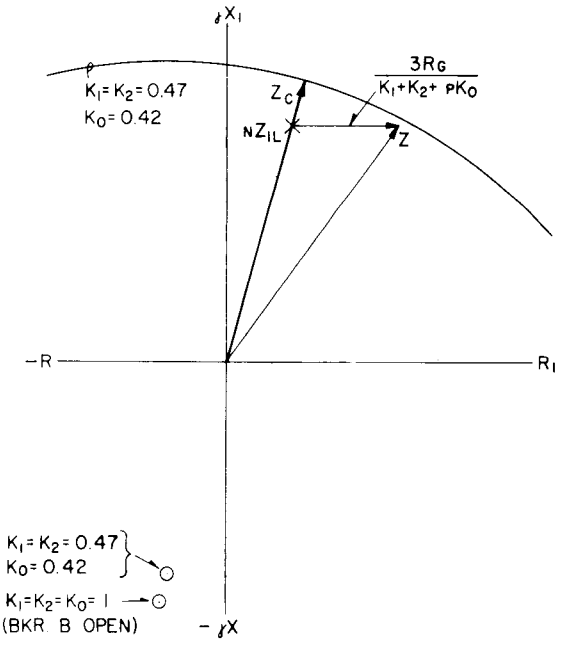
(A) 837A116

a) Long Line



(B) 837A114

b) Medium-length Line



(C) 837A115

c) Short Line

Fig. 24. Impedance Circles for the SDG Line Relays

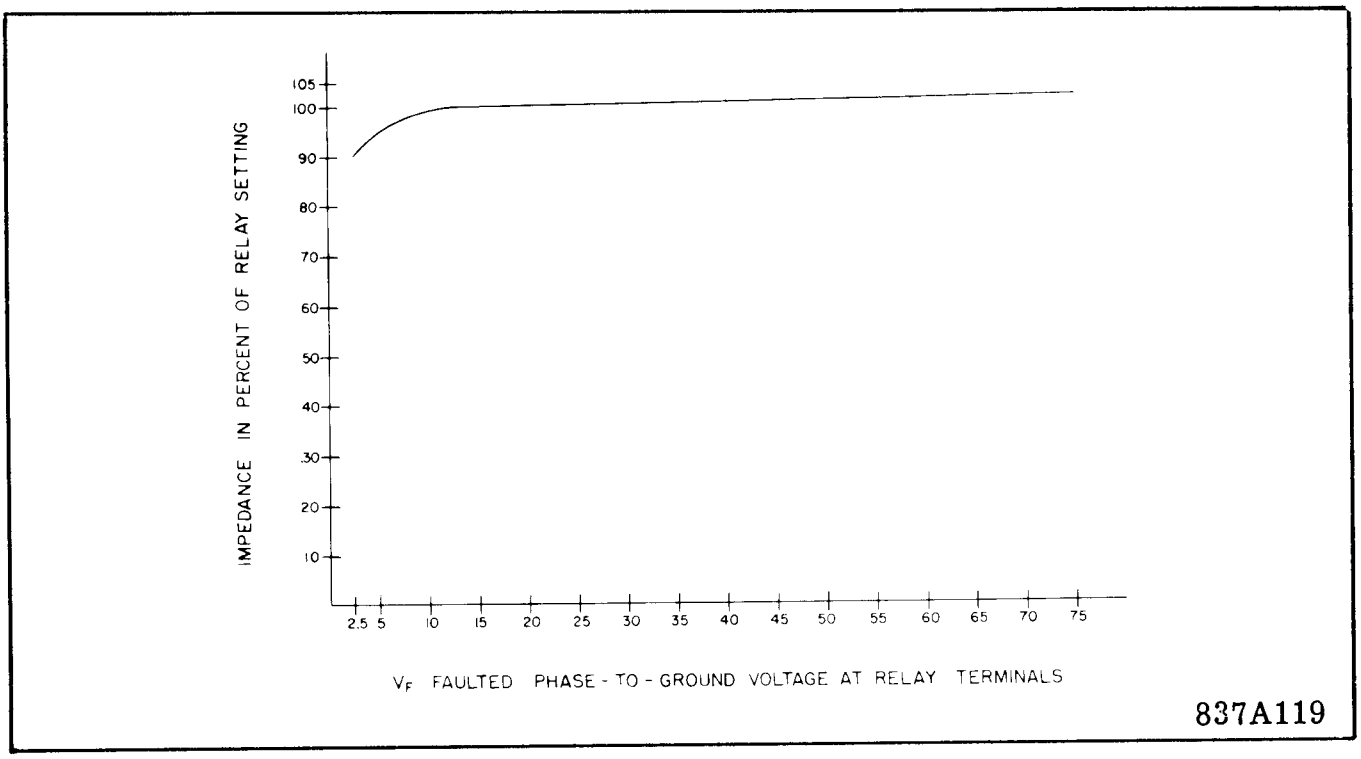


Fig. 25. Impedance Curve for the SDG Line Relays

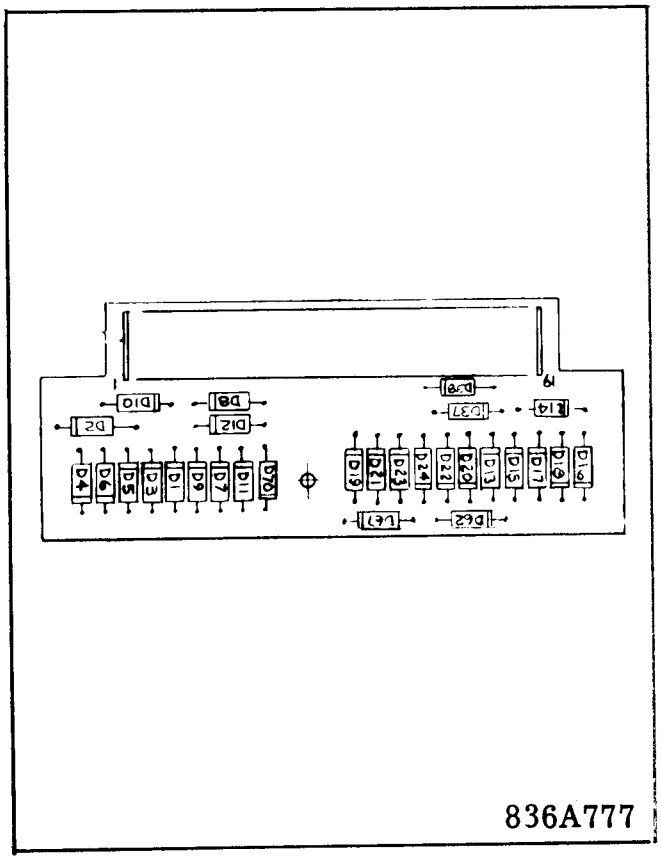


Fig. 26. Printed Circuit Board Assembly for SDG, SDG-1, 2, 3, & 4 Relays

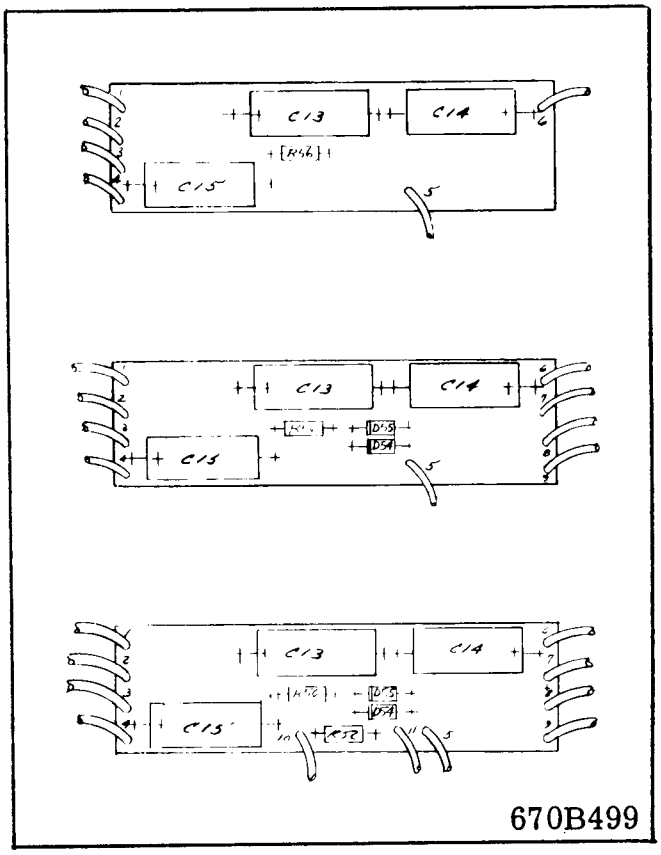


Fig. 27. Printed Circuit Board Assembly for SDG, SDG-1, 2, 3, & 4 Relays

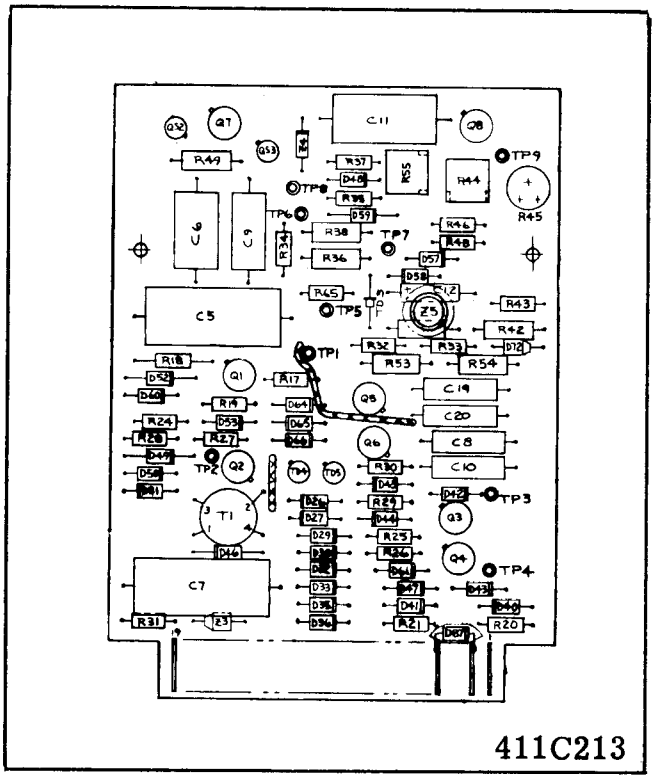


Fig. 28. Printed Circuit Board Assembly for SDG Relay

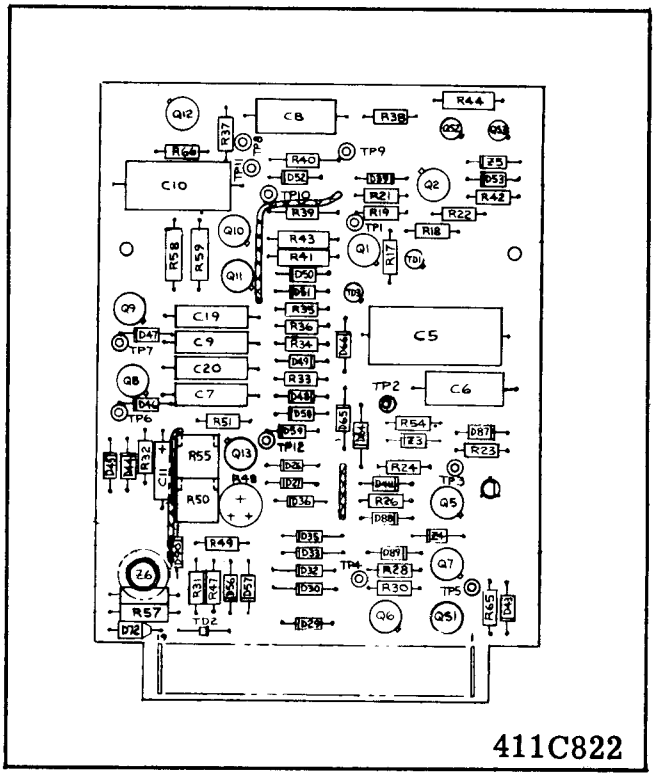


Fig. 29. Printed Circuit Board Assembly for SDG-1 Relay

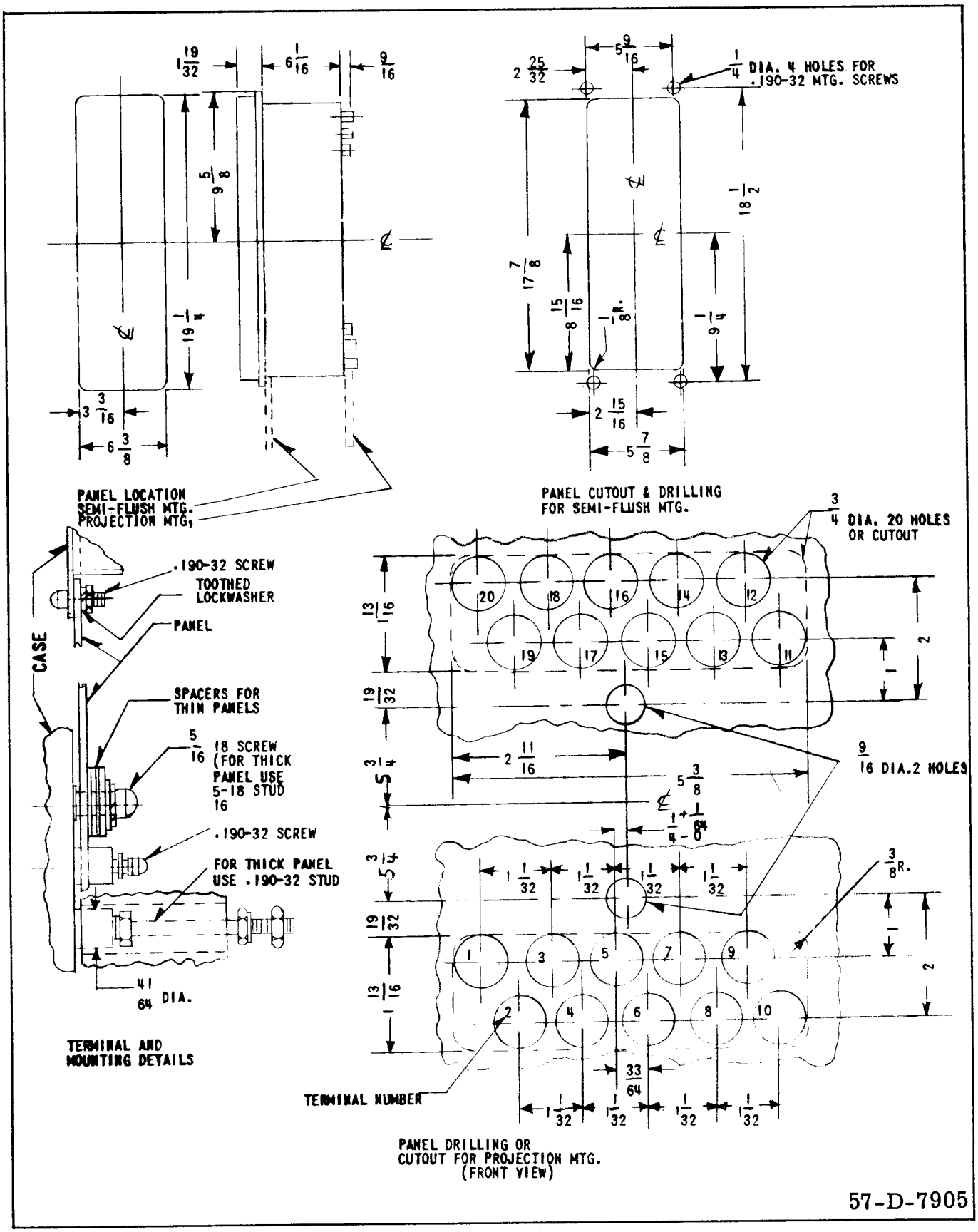


Fig. 30. Outline and Drilling Plan for the Type SDG Line Relays in the FT-42 Case

APPENDIX I

MUTUAL IMPEDANCE EFFECT

Where mutual compensation is desired, a type IK auxiliary current transformer (Fig. 32) maybe used with a step down current ratio of $\left|\frac{Z_{OM}}{Z_{OL}}\right| = C^1$ Z_{OM} is the zero sequence mutual impedance and Z_{OL} is the zero sequence self impedance of the line. Zone 1 maybe set to cover 85% of the line.

The "parallel line" leads on the IK-transformer are set for factor C^1, as defined above. These leads are set so that the difference between the taps is nearest to the desired C^1-value.

The external terminals of the IK-transformer numbered 3 and 4 are connected across the SDG-relay terminals 19 and 18 as shown in the external schematic figure 22. The external terminals 5 and 6 are connected in series with the residual CT circuit of the parallel line.

The IK transformer is set as outlined below. Before the proper tap settings are made, the cover of the transformer should be completely open. Complete opening of the cover assures continuity in the residual current transformer circuits and isolates the IK transformer windings from the residual circuits.

The taps are set so that difference between the two taps is equal to the desired setting of C^1. For instance, C^1 setting equal to 8, is set as follows:

Connect leads coming out of opening marked "parallel line" Fig. 32 to the terminals marked "C^1". Black lead (which is of the same polarity as the plus marked external terminal) is connected to terminal marked ".2" and the white lead to the terminal marked "1.0". The difference between the two taps 1.0 − .2 = .8, is the desired "C^1" setting. Physically, this is done as follows:

Remove the top nut from the desired terminal, place the lug of the proper lead on the terminal and replace the locking nut. Make sure that nut holds the lug snugly against the terminal to avoid the possibility of developing a loose or high resistance connection.

The leads coming out of opening marked "protective relay" and "protected line" are connected to the terminals "0" and "1.0" in the row marked "C" observing the same polarity marking as above. This connection is the same for all "C^1" values less or equal to 1.

After the setting is completed the cover should be closed to restore the connection between the transformer winding and the external terminals.

General Considerations

In considering mutual zero-sequence impedance effects it is well to consider that the mutual impedance works to reduce fault-current level when the currents flow in the same direction in the coupled lines. The converse is true when the currents flow in opposite directions. For example, in Fig. 33(a), the currents are flowing in the same direction from the left, causing the relay at A to underreach. If, however, $|Z_{OS}| >> |Z_{OU}|$ then for a balance point fault (e.g. 85% from A to B), the current I_{OM} reverses as in Fig. 33(b). Here the fault current K_0I_0 is larger than for a similar situation except with $Z_{OM} = 0$; so a relay set for 85% of the line actually reaches farther due to mutual effects assuming no mutual compensation. Of course, as the fault moves closer to B, a point is reached where I_{OM} reverses, so that relay A will never overreach to see a bus fault at B.

If mutual compensation is used in Fig. 33(b) for relay A, it will have the undesirable effect of reducing the operating current and hence the reach. We see then, that mutual compensation eliminates the undesirable effect of mutual impedance if, and only if, both K_0I_0 and I_{OM} are flowing from the local bus into the lines.

For the usual case of Fig. 33(a) mutual compensation may be used to maintain zone 1 reach at 85% of the line regardless of whether the adjacent line is in or not. Without compensation, if the relay is set for 85% of the zero-sequence self-impedance, it will cover at least 70% (but less than 85% except for the Fig. 33(b) case) of the line with the adjacent line closed. Two things work to minimize the underreach: first, as the fault moves closer to bkr. A, I_{OM} decreases and K_0I_0 increases; secondly, as the fault moves within the balance point, the restraint voltages are overcompensated, reducing the restraint. The amount of underreach varies with system impedances, but one can expect to cover at least 70% of the line, with an 85% nominal setting.

Mutual compensation of zone 2 is of more value: 1) Since I_{OM} is flowing in the same direction as K_0I_0 for the entire length for end-zone faults, and 2) we need to make sure of 100% protected line coverage.

We have already seen in Fig. 33(b) that mutual compensation is not always efficacious, we must also consider the adjacent-line faults of Fig. 34. In Fig. 34(a) we can be greatly overcompensated so that relay A operates due to the compensation current $I_{OM}(\frac{Z_{OM}}{Z_{OL}})$. The SCC relay will minimize the possibility of SDG-line overreach for the case in Fig. 34(b).

In Fig. 34(c) bkr. C is open so that the same conditions exist for relay A whether or not mutual compensation is used. In this case, adjacent line current flows in the opposite direction to that of K_0I_0 for the entire length. The zone-1-relay phase compensation at bkr. A is less than half of the proper amount to reach the fault, but the ground compensation may be in excess of the apparent zero-sequence impedance to the fault. The worst case occurs when there is no current source at U. Fortunately, zone 1 at A cannot overreach; however, zone 2 at A can see this fault if source U is weak. Fortunately zone 1 at D will also see the fault so bkr. A zone 2 need not be delayed to coordinate with bkr. D-zone 2.

Note in both Fig. 34(b) and (c) that the system condition which can cause trouble with relays A and C is a poor source at U. This is also the condition yielding the greatest zone 1 underreach for protected line faults.

As mentioned earlier we can get at least 70% zone 1 coverage without mutual compensation. The advantages of tolerating a reduced reach with the parallel line in service (vs. 85% coverage with mutual compensation) are:

1. Type SCC current comparer not required.
2. No overreach tendencies for adjacent line faults-(Fig. 34(b))
3. Simplified current circuit (where we have zone 1 only).

Zone 2 should definitely be mutually compensated unless the mutual impedance effects are negligible. The SCC current comparer need not be applied for zone 2 supervision even though the zone 2 relay at A will operate for close-in faults (Fig. 34(a) since bkr. C is opened at high speed. In rare cases, after bkr. C opens (Fig. 34(c), zone 2 at A will remain operated (poor source at U), requiring time coordination with zone 2 at D.

Type SCC Current Comparer

The SCC relay prevents the SDG relay types from tripping for close-in adjacent line faults, where the mutual compensating current may reach many times the protected line current, as in Fig. 35(a). It is a static magnitude-comparison circuit. It operates on protected line current K_0I_0 and restrains on $0.4\left|K_0I_0 - dI_{OM}\right| = 0.4\left|K_0I_0 - \frac{Z_{OM}}{Z_{OL}} I_{OM}\right|$. That is, it restrains on the difference between the protected line current and the mutual compensation current.

Fig. 35 illustrates the SCC relay operation for various conditions. It is in balance in Fig. 35(b). In Figs. 35(c), (d) and (e) it operates to permit distance relay trip.

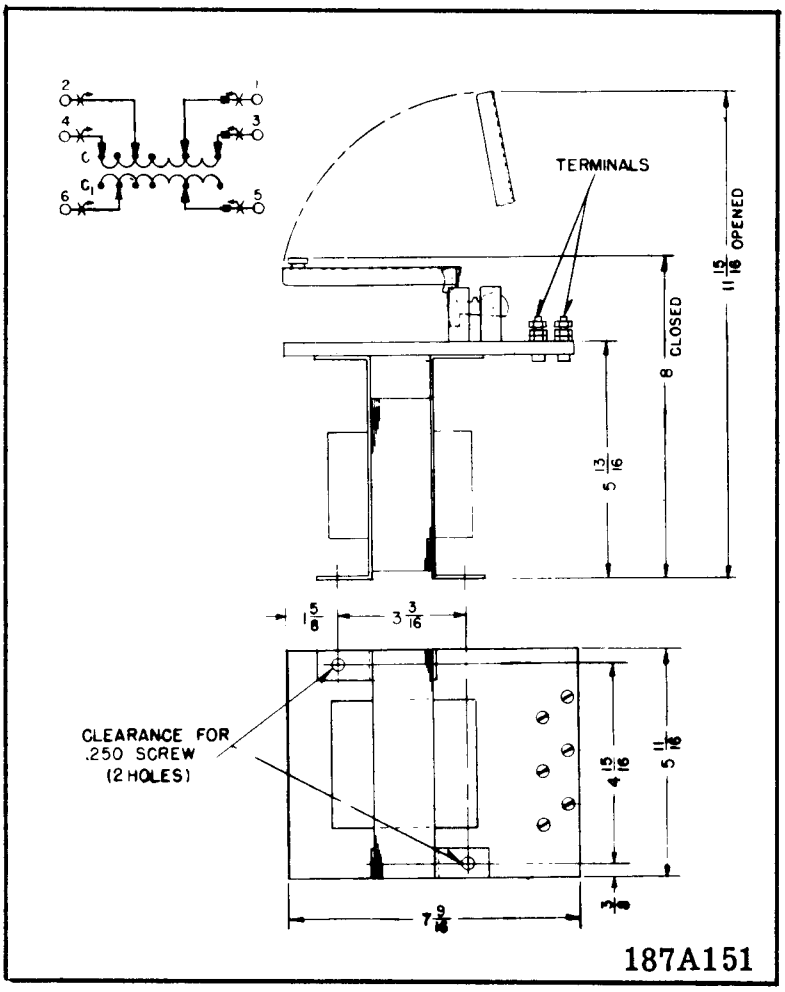


Fig. 31. Outline and Drilling Plan for the Type IK Transformer

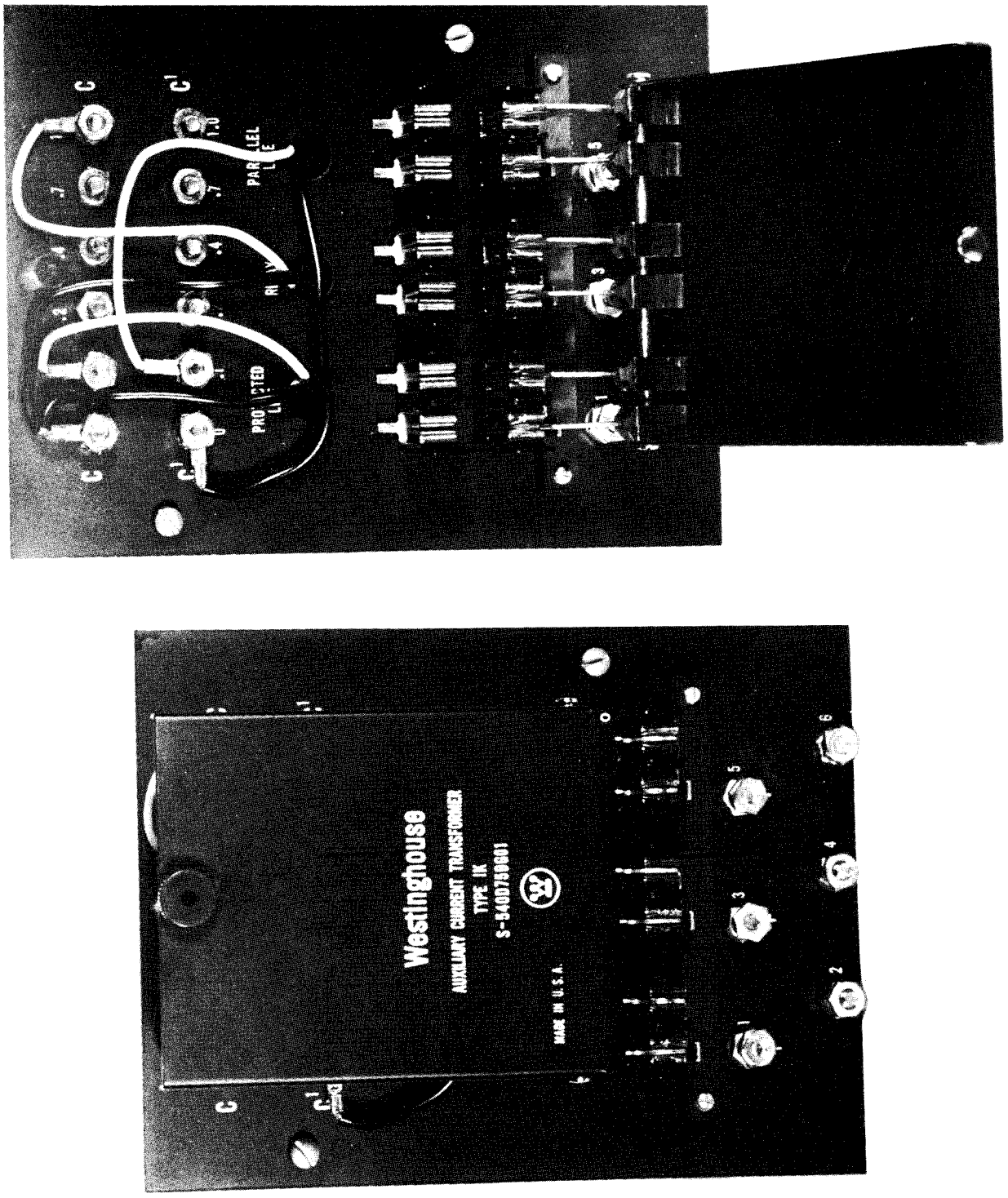


Fig. 32. Type IK Transformer

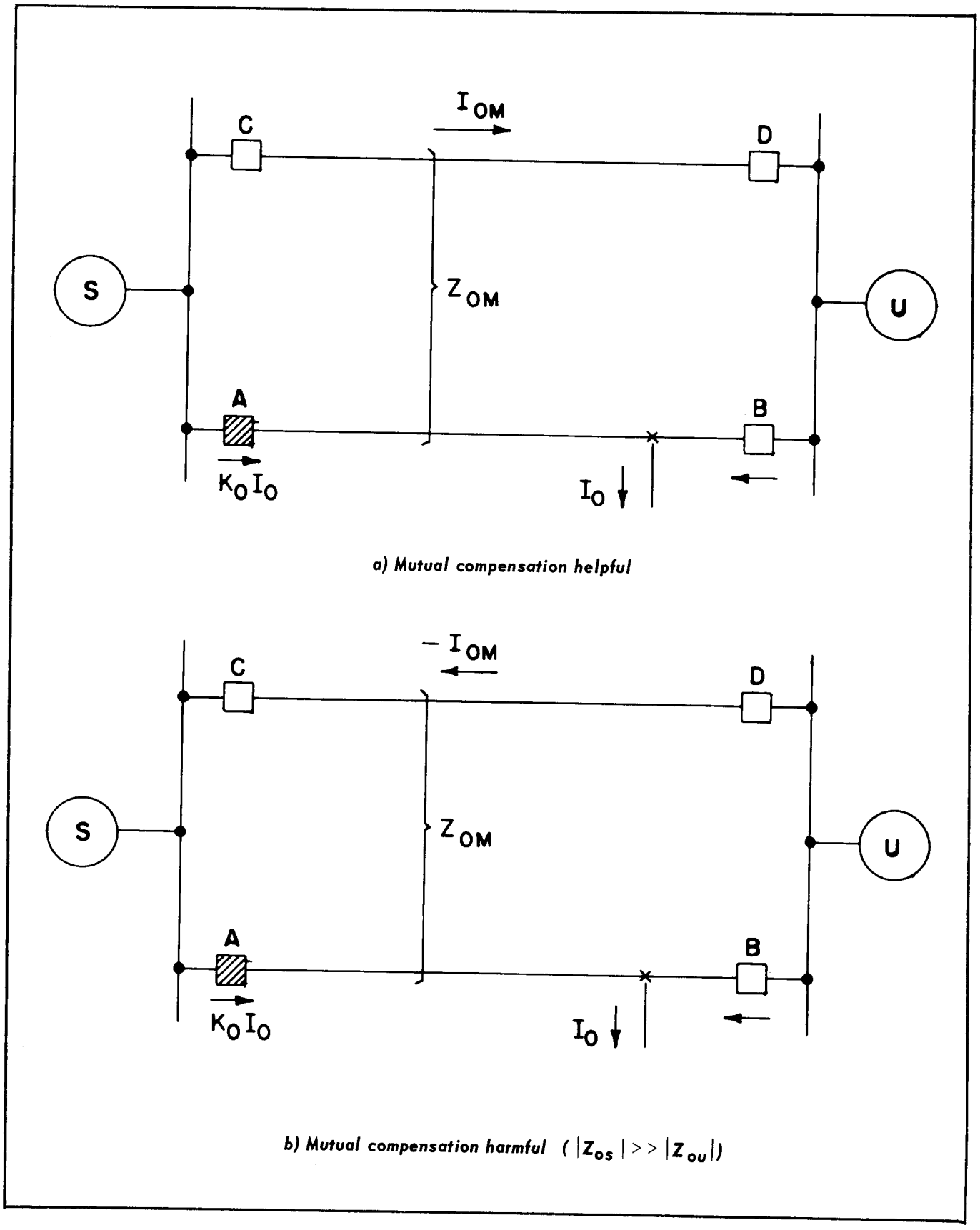


Fig. 33. Zero-Sequence Currents for Zone 1 Balance-Point Fault With Mutual Coupling

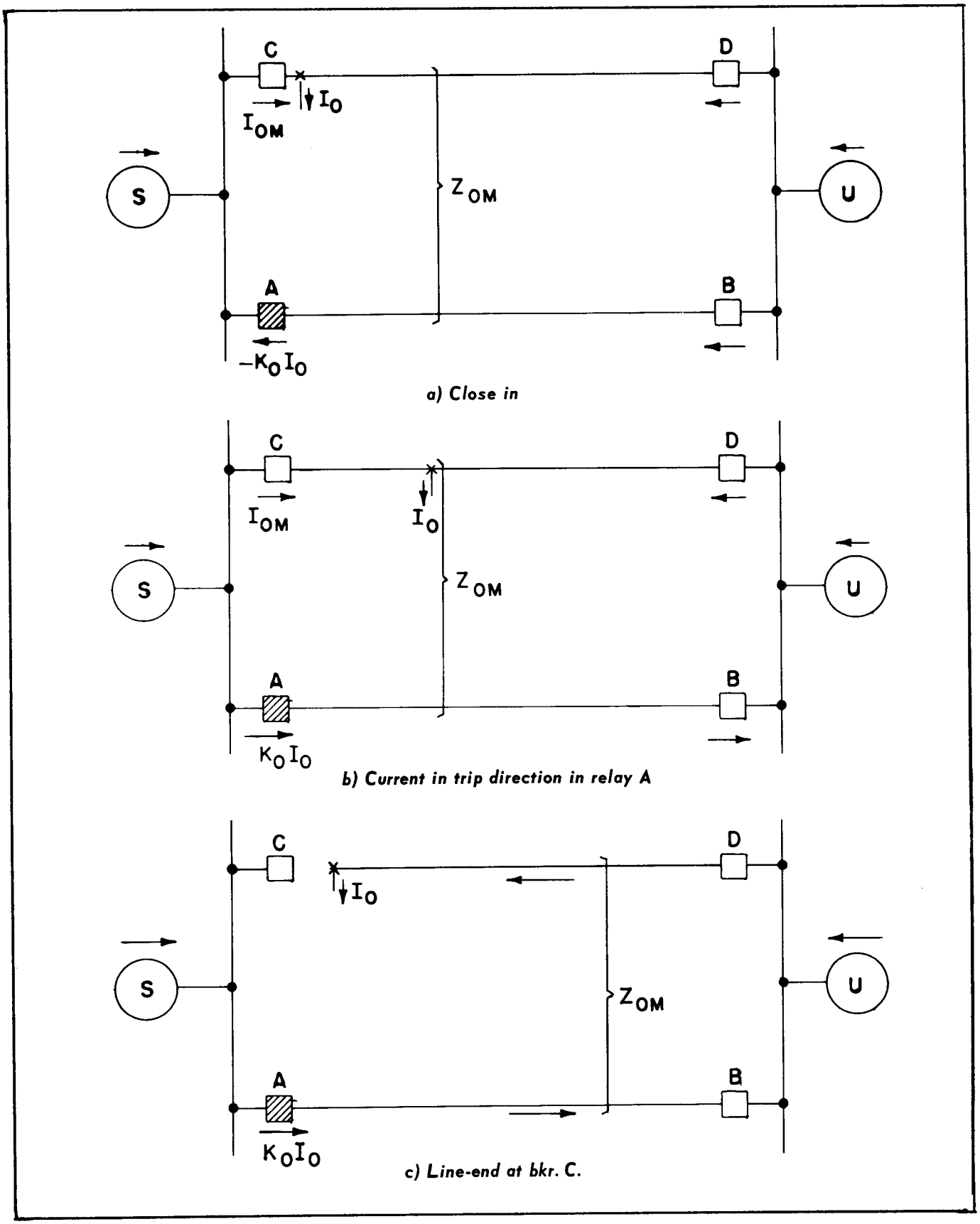


Fig. 34. Zero-Sequence Currents for Adjacent-Line Faults With Mutual Coupling

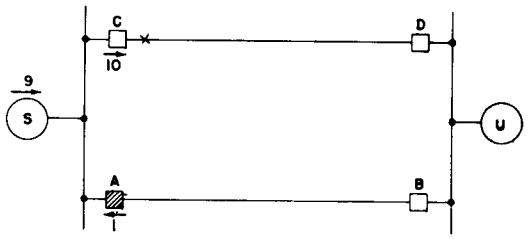
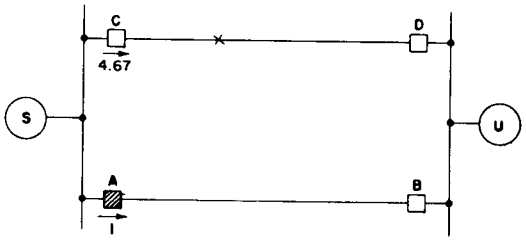
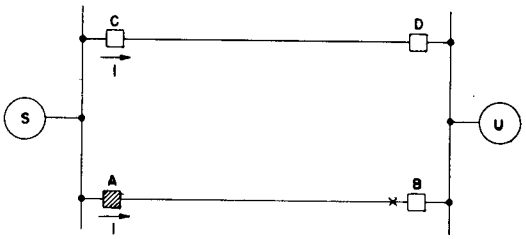
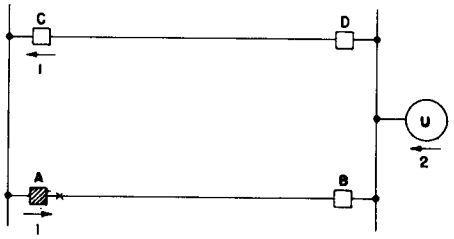
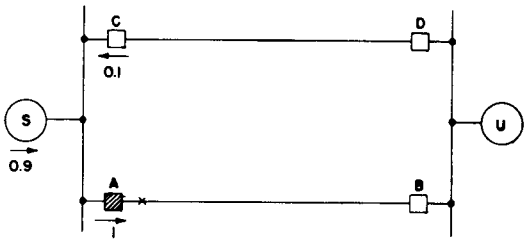
SCC OPER.		K_oI_o	$0.75\,I_{om}$	$0.4\,\lvert K_oI_o - 0.75\,I_{om}\rvert$
a) No		−1	7.5	3.4
b) Bal.		1	3.5	1.0
c) Yes		1	0.75	0.1
d) Yes		1	−0.75	0.7
e) Yes		1	−0.08	0.43

Fig. 35. Type SCC Relay Operation

INSTALLATION • OPERATION • MAINTENANCE

INSTRUCTIONS

TYPE SDG LINE GROUND-DISTANCE RELAY

APPLICATION

These instructions cover the five basic types listed in Table I. This line of relays provides single-zone ground-distance protection. The relay reaches the preset amount for single-line-to-ground faults and as much as 20% less for double-line-to-ground faults.

TABLE I

Relay	I_0 Fault Det.	Freq. Verifier	Phase to Phase Desensitizer	Output	Application
SDG	X	X	X	Thyristor	Zone 1
SDG-1	X	X	X	Transistor	Zone 1 or Pilot Trip (Note 1)
SDG-2	–	X	X	Transistor	Zone 1 or Pilot Trip (Note 1)
SDG-3	X	–	–	Transistor	Timed Trip
SDG-4	–	–	–	Transistor	Blocking Start

NOTE 1: Also suitable for timed trip.

The potential supply must be wye-grounded. The broken delta potential connection is provided inside the relay.

As shown in Table I the SDG is equipped with a thyristor trip output; use this type where a single-zone is needed in conjunction with an otherwise electromechanical system. For all-static-systems use the transistor output types, utilizing the thyristor trips in the type SRU output package.

The frequency-verifier circuit should be utilized for all high-speed trip applications to avoid undesired trips due to high-frequency transients. This circuit is not needed for timed trips (e.g. zone 2), but the SDG-1 or SDG-2 may be utilized instead of the SDG-3 in the interests of standardization.

Relays with I_0 current detector are used to prevent tripping due to potential circuit trouble; the SDG-2 requires SI or SI-1 current-detector supervision.

The phase-phase desensitizer is used to eliminate a possible 15% overreach on two-line-to-ground faults. This circuit is needed for zone 1 applications where the relay reaches 85% towards the far bus.

A type IK auxiliary current transformer may be used to compensate for zero-sequence mutual induction. Otherwise, this transformer is not needed. For the case of two parallel two-terminal lines and an 85% self impedance relay, zone 1 will reach at least 70% to the far end; accordingly, there is not much gain in mutual compensation of zone 1. However, zone 2 may be mutually compensated since its reach is affected more than zone 1. Where zone 1 is mutually compensated, a type SCC current-comparer relay is required to supervise distance relay tripping. See Appendix 1 for details.

FUNDAMENTALS OF DISTANCE MEASUREMENT ON GROUND FAULTS

The SDG distance relay operates on both single and double line-to-ground faults.* In either case, neglecting fault resistance, the faulted phase-to-ground voltages(s) at the relay consists of the line drop:

$$V_{LG} = \text{Faulted phase-to-ground relay voltage}$$

$$= K_1 I_1 n Z_{1L} + K_2 I_2 n Z_{1L} + K_0 I_0 n Z_{0L} + I_{0E} n Z_{0M} \quad (1)$$

Where K_1, K_2, K_0 are current distribution factors for the pos., neg., and zero sequence networks, respectively

I_1, I_2, I_0 are the pos., neg., and zero sequence currents in the fault.

$^{n}Z_{1L}$, $^{n}Z_{0L}$ are the pos. and zero sequence line impedances to the fault

I_{0E} is the adjacent line zero sequence current.

Z_{0M} zero sequence mutual impedance.

See Fig. 12 for further definition of terms. For an A to ground fault eq. (1) would be written in terms of the phase A quantities.

$$V_{AG} = K_1 I_{A1} {}^{n}Z_{1L} + K_2 I_{A2} {}^{n}Z_{1L} + I_{0E} {}^{n}Z_{0M} \quad (2)$$

Eq. (2) also applies for an AB to ground fault; an additional expression applies for the phase B quantities for an AB to ground fault.

Hence, a distance ground relay made to respond to single phase-to-ground faults will also respond in the same way to double line-to-ground faults. This is true except for the effect of ground resistance, RG. The different nature of these effects can be sensed from Fig. 13. In Fig. 13 the ground current $3I_0$ flowing through R_G is essentially in phase with the total faulted phase current. This is so, since $I_{A1} = I_{A2} = I_0$. This is not true for a 2L-G fault. The current $3I_0$ is out of phase with $K_1 I_{A1}$ and $K_2 I_{A2}$ (also out of phase with $K_1 I_{B1}$ and $K_2 I_{B2}$). As a result the drop across R_G produces an apparent reactance term to the distance relay, causing it to under-reach on one phase and over-reach on the other faulted phase. The SDG relay contains a desensitizer circuit to prevent over-reach on 2L-G faults, by reducing the reach of the relay.

$$V_{XN} = (V_{A1} + V_{A2}) - Z_C (K_A I_{A1} + K_2 I_{A2}) \quad (3)$$

$$V_{YN} = (V_{B1} + V_{B2}) - Z_C (K_1 I_{B1} + K_2 I_{B2}) \quad (4)$$

$$V_{ZN} = (V_{C1} + V_{C2}) - Z_C (K_1 I_{C1} + K_2 I_{C2}) \quad (5)$$

The restraint voltages are obtained by the use of compensators with an impedance Z_C, set to match the desired positive sequence line impedance reach. Only positive and negative sequence voltages appear in eq. (3) to (5). The zero sequence voltage is filtered out by not grounding the neutral of the set of Y-connected auxiliary transformers (T_{A2}, T_{B2} and T_{C2}) which are used to feed the restraint portion of the magnitude comparison circuit. These same connections render the zero sequence current flowing in the phase compensators ineffective. So the restraint voltages duplicate the delta voltage conditions at the fault when the fault is Z_C ohms from the relay (i.e. at the balance point). Zero sequence quantities are not required to duplicate the system voltage triangle at the balance point since zero sequence voltage cancels out of the line to line voltages.

The operating voltage is:

$$V_{W0} = V_0 - \frac{Z_{0L}}{Z_{1L}} \times Z_C \left(K_0 I_0 + I_{0E} \frac{Z_{0M}}{Z_{0L}}\right) \quad (6)$$

Here V_0 is the relay zero sequence voltage: it is compensated by using a compensator impedance $\frac{Z_{0L}}{Z_{1L}} Z_C$, representing the zero sequence line impedance to the desired balance point. For mutual coupled lines this compensator can be fed with not only the protected line current but also with a portion of the mutual current I_{0E} (See Fig. 12). The operating voltage V_{W0} duplicates the system zero sequence voltage for a fault at the balance point.

Since the faulted phase-to-ground voltage is zero at the fault (neglecting fault resistance), the operating and faulted phase restraint voltage will be equal for a balance point fault. This can be seen by manipulating the fault voltage expression, remembering that the relay compensated voltages are a replica of the fault-point voltages:

V_{LGF} = Faulted phase to ground voltage at fault

$$= V_{1F} + V_{2F} + V_{0F} = 0 \quad (7)$$

$$V_{1F} + V_{2F} = -V_{0F} \quad (8)$$

$$\left| V_{1F} + V_{2F} \right| = \left| V_{0F} \right| \quad (9)$$

Eq. (9) states that the magnitude of the sum of the pos. and neg. sequence voltage equals the magnitude of the zero sequence voltage at the fault. This holds regardless of how many phases are grounded. Eq. (9) is the keystone of the SDG system.

This balance point condition is shown in Fig. 14 for an A-G fault. The bus voltages ($V_{A1} + V_{A2}$) and V_0 are shown along with the compensator voltages, which modify the bus voltages to produce restraint voltage V_{XN} and operating voltage V_{WO}.

For this condition V_{YN} and V_{ZN} are also produced but these will be larger in magnitude since these are derived from the sound phases. Since these voltages exceed V_{XN}, they are irrelevant.

In Fig. 14 for a fault beyond the balance point, V_{XN} exceeds V_{WO}; the reverse is true for the fault within the balance point. Note that for all these faults in the trip direction that the phase compensation acts to reduce the bus positive and negative sequence voltages; whereas, the zero sequence compensation is added to V_0. The reverse is true for a fault behind the relay. For this reason the SDG is inherently directional.

One other aspect of Fig. 14 bears amplification. Note for the fault within the balance point that the phase compensation is almost enough to reverse V_{XN} polarity. It is possible for such a reversal to occur, and it is possible if very little zero sequence flows for the phase compensation to overtake the operating voltage and restrain the relay. Thus, the relay may fail to see a close-in fault if the zero sequence current is quite small. Any time this extreme occurs the phase distance relay will operate. The phase-distance relay will clear the fault when:

$$Z_1 > \frac{V_0/I_0}{K_1+K_2+pK_0}$$

where Z_1 is positive-sequence relay reach

V_0 = zero sequence bus voltage for close-in fault

I_0 = total zero-sequence fault current for close-in fault

K_1, K_2, K_0 pos.-, neg.- & zero-sequence current-distribution factors for close-in fault.

p = ratio of zero-sequence to positive-sequence line impedance.

CONSTRUCTION AND OPERATION

The type SDG relay consists of: four air gap transformers, three auto-transformers for reach adjustment, four phase splitter-transformers, one isolating transformer which couples the zero sequence network a-c output to the static frequency verifier circuit, one zero sequence current-to-voltage transformer, four phase-splitter and rectifier networks, a double line-to-ground fault desensitizer, one voltage regulating zener diode, a thyristor for the tripping function (if used), and printed circuit assemblies.

The large printed circuit assembly contains a magnitude comparator, frequency check circuit, the trigger circuit for the thyristor tripping unit, and the zero sequence current detector.

Compensators (T_A, T_B, T_C, T_O)

The compensators, which are designated T_A, T_B, T_C and T_O are two-winding air-gap transformers. Each current winding has seven taps which terminate at the tap block. A voltage is induced in the secondary which is proportional to the primary tap and current magnitude. This proportionality is established by the cross sectional area of the laminated steel core, the length of an air gap which is located in the center of the coil, and the tightness of the laminations. All of these factors which influence the secondary voltage have been precisely set at the factory. The clamps which hold the lamination should not be disturbed by either tightening or loosening the clamp screws.

The secondary winding has a single tap which divides the winding into two sections. One section is connected subtractively in series with the relay terminal voltage. Thus a voltage which is proportional to the phase current is subtracted vectorially from the relay terminal voltage. The second section is connected to an adjustable loading resistor (R_1, R_2, R_3, R_4) and provides a means of adjusting the phase angle between primary current and the induced secondary voltage. The phase angle may be set for any value between 60° and 90° by adjusting this resistor. The factory setting is for a maximum sensitivity angle of 75° current lagging voltage.

A tertiary winding M has four taps which may be connected to directly modify the T setting by any value from −18 to +18 percent in steps of 3 percent. The sign of M is negative when the R lead is above the L lead. M is positive when L is in a tap location which is above the tap location of the R lead. The M setting is determined by the sum of per unit values between the R and L lead. The actual per unit values which appear on the tap plate between taps are 0, .03, .09 and .06.

Auto-Transformer (T_{A1}, T_{B1}, T_{C1})

The auto-transformers T_{A1}, T_{B1}, T_{C1} have three taps on their main winding S which are numbered 1, 2 and 3 on the tap block.

The three secondary windings of the auto-transformers are connected in a "broken delta", thus serving as a source of zero sequence voltage

for the operating circuit. The primary to secondary turn ratio is 3:1, thus producing the proper zero sequence voltage magnitude as required by the theory of relay operation. Using S=2 or S=3 settings reduces zero sequence voltage in the same proportion as the line-to-neutral voltages.

The auto-transformer makes it possible to expand the basic range of T ohms by a multiplier of S.

Phase-Splitter Transformer (T_{A2}, T_{B2}, T_{C2}, T_{O2})

The phase splitter transformer provides isolation between the a-c analog network and the magnitude comparer circuitry located on the printed circuit board, and couples the restraint and operating outputs to the phase splitter network. The tap connection on the secondary winding serves as part of the phase splitting circuit that converts a single-phase input into a three-phase output, thus minimizing the ripple of the rectified output.

Isolating Transformer (I_O)

The isolating transformer I_O serves two purposes: First it isolates the a-c circuit from the d-c circuit, and second, it produces a secondary voltage in the presence of zero sequence current.

Isolating Transformer (T_{FV})

The isolating transformer T_{FV} serves two purposes: First, it isolates the a-c circuit from the d-c circuit and second, it steps up the clipped a-c signal to make the frequency check circuit sensitive to low level input signals.

Double Line-to-Ground Fault Desensitizer

The double line-to-ground fault desensitizer in Figs. 5 & 10 consists of the three networks. Each network consists of a resistor and a minimum voltage network. In this network the largest restraint voltage is blocked by a combination of two restraining voltages. If any two restraining voltages become smaller than the third restraint voltage, transistors Q17 and Q18 are turned on the prevent Q1 and Q2 transistors from turning on. When operating voltage becomes larger than the highest restraint the relay is allowed to trip. The desensitizer effect is limited to S=1 setting only and is not effective on the S=2 or S=3 setting. If S=2 or S=3 setting is used for zone 1 the setting should be reduced to 75% of the protected line to avoid overreach on double-line-to-ground faults.

Magnitude Comparator Circuit (Fig. 15)

The magnitude comparator circuit consists of a minimum voltage network of the voltage balance type in which operating current is caused to flow through a current detector whenever one of the phase restraint voltages becomes smaller than the operating voltage.

Resistors (R9, R10, R11) provide a return path for the operating current.

The current detector consists of a tunnel-diode TD1 and a transistor Q1. When the tunnel diode is switched to the high voltage state, the transistor is turned on. The use of the tunnel diode secures a sharp turn on characteristic for the triggering network.

When transistor Q1 is turned on it in turn switches transistor Q2 on, when transistor Q2 is "on" the collector voltage is raised to high positive voltage that starts the operation of the triggering circuit.

Triggering Circuit for SDG Relay (Fig. 16)

The triggering circuit consists of a four-layer diode D50, resistor R28, diode D51, and pulse transformer TR-1. When Q2 transistor is turned on capacitor C6 starts charging to the breakdown voltage of the four layer diode D50.

After breakdown of D50, capacitor C6 discharges through the primary of the TR-1 transformer thus producing a gating impulse that fires the output thyristor QS1 Diode D49 provides a quick discharge of C6 after Q2 is turned off through R24. Diode D51 protects D50 from reverse polarity. The triggering circuit is supervised by the residual overcurrent unit and frequency verifier circuit through diodes D52 and D60. D52 diode bypasses the charging capacitor C6 during the 4 ms. period the frequency verifier output is held at ground potential. D60 performs the same function in the absence of residual current.

Zero Sequence Current Detector (Fig. 17)

To prevent operation of the magnitude comparator during a blown potential fuse or similar condition a zero sequence current detector supervises the operation of the triggering network by preventing capacitor C6 in the triggering circuit from charging, keeping the point "P" at negative potential through the diode D60.

The detector employs a tunnel diode (TD3) as a level detector. The tunnel diode is biased through resistor R45 to the high voltage state so that enough voltage is maintained across the base-to-emitter junction of Q8 transistor to keep it conducting.

In the presence of the residual current a current derived negative voltage through transformer I_0 appears across resistor R41, switching TD3 to the low voltage state, thus turning transistor Q8 off and raising its collector to the positive DC voltage supply level, blocking D60 from discharging the C6 capacitor.

Frequency Verification (Fig. 18)

During certain switching conditions, such as energization of a transmission line, residual currents and voltages may exist of higher frequencies than 60 cycles per second. The frequency verifier prevents relay operation when the operating voltage period is less than 4.3 ms. The frequency verification circuit consists of two functional parts: zero-crossing and commutator circuits. The zero-crossing circuit consists of transistors Q3, Q4, Q5, and Q6. The zero-crossing circuit is used to allow operation in the presence of higher frequencies of small magnitude superimposed on a fundamental of 60 cps. During the positive or negative half cycles of the operating voltage V_{WO}, Q3 or Q4 transistors are driven into saturation by the output of the T_{FV} transformer. Transistors Q5 or Q6 conduct until capacitors C8 or C10 respectively are fully charged. While either capacitor charges, a voltage output in the form of very narrow pulse is developed across R32 & R33 resistors during the start of each half cycle. This pulse triggers QS2 control switch. When transistors Q3 or Q4 are not conducting, C8 and C10 capacitors discharge respectively through D45 or D44 and the parallel combination of R26 and R30 or R25 and R29.

While QS2 is "on" its anode is only about 0.7 volt above negative, thus preventing capacitor C6 in the triggering circuit from charging for 4.3 milliseconds. The time delay of 4.3 milliseconds is controlled by the resistor R38, the capacitor C11 and the reference Zener diode Z4. After 4.3 milliseconds of delay the control switch QS3 fires applying the voltage of capacitor C9 across QS2, turning it off. This raises the potential of the QS2 anode, leaving the triggering circuit free to operate. After the next zero crossing pulse, QS2 switch is turned on again, the QS3 switch is turned off by capacitor C9. Charge and commutator action is repeated all over again. Transistor Q7 when turned on by the same voltage that fires the gate of QS2, discharges timing capacitor C11, thus starting the timing cycle with close to zero charge on the capacitor. If the period of the V_{WO} voltage is less than 4.3 ms. the Q7 transistor discharges the timing capacitor thus preventing the turning off of QS3 switch. This keeps QS2 switch on to prevent operation of the triggering circuit. Capacitors C19 and C20 serve as coupling capacitors to start transient blocking whenever Q1 operates, this prevents tripping if V_{WO} – voltage stays at operating level for less than 4 msec.

Output Circuit (Fig. 19)

The output circuit or SDG relay consists of the secondary of the pulse transformer TR-1, diode D46, capacitor C7, resistor R31, and Zener diode Z3. The output of the SDG relay is a thyristor which is gated into conduction by a pulse transformer. The transformer is pulsed as described under "Triggering Circuit Operation". Zener diode Z3, resistor R31 and capacitor C7 form a network protecting the thyristor unit from voltage surges coming through the d-c supply. The function of diode D46 is to short out negative pulses coming from the TR-1 pulse transformer.

In the SDG-1, -2, -3, & -4 relays the output circuitry consists of transistors Q3, Q5, & Q6 and other associated components.

Upon the operation of the Q2-transistor in the magnitude comparator circuit, transistor Q3 is driven into conduction by the positive voltage developed across resistor R22. Transistor Q3, in turn, shunts the base drive current of transistor Q5, to turn Q5 off. At the same time the turned on Q3-transistor provides a base current path to transistor Q6 turning it on. An output voltage consequently is developed through transistor Q6, resistor R28, across Q5 and appears at relay terminal 11. In absence of the output from the magnitude and parator circuit the Q5 transistor is biased to conduct through resistor R24 and no output appears at relay terminal 11.

Q7 and QS1 form the pushbutton light circuit that operates an indicating light during a pushbutton check-out procedure.

Pushbutton Check Circuit (Fig. 20)

The pushbutton check circuit is used for in-service operational check-out of the output thyristor.

Depressing the pushbutton provides an internal d-c supply to the thyristor switch and operates the overcurrent circuit. This action must be preceded by the opening of the relay trip circuit (red handle) and relay voltage switch (7). The opening of the voltage switch produces operating voltage conditions in the magnitude comparator that gates the thyristor switch. Operation of the thyristor switch is indicated by the lighting of the bulb built into the pushbutton. A similar circuit is provided in the SDG-1, -2, -3, & -4 relays (See Fig. 10).

CHARACTERISTICS

Distance Characteristics

Fig. 24 shows the relay characteristic in the complex plane is $Z = nZ_{1L} + \frac{3R_G}{F}$ for single line to ground faults where factor $F = K_1 + K_2 + pK_0$, where K_1, K_2, K_0 are positive, negative and zero sequence current distribution factors and p = ratio of zero sequence to positive sequence line impedance. Impedance nZ_{1L} is the positive-sequence line impedance from the relay to the fault. The apparent impedance Z must fall within the characteristic shown in Fig. 24 in order to operate. The R-X characteristic is a composite of three circles whose centers are A, B, and C in Fig. 24A. The circle whose center is A is produced from the comparison of faulted phase restraint and operating voltage for a single-line-to-ground fault; whereas the "B" and "C" circles result from sound-phase restraint comparison with operating voltage. Note that part (A) of Fig. 24 applies for the case of a low source impedance vs line impedance; parts (B) and (C) represent increasing amounts of source impedance, or conversely shorter line lengths. The solid-line characteristic is based on current distribution factors for a balance point fault with all breakers closed. As the fault moves toward the relay these distribution factors increase, with the relay approaching the dashed-line characteristic. In the case of Fig. 24C, the dashed-line characteristic is not shown, as it essentially coincides with the solid-line characteristic. Regardless of system conditions, the relay reaches Z_C positive-sequence ohms for a fault at the compensator angle. The fact that the circle diameter expands with increasing source impedance is beneficial, since this provides increased fault resistance accommodation for the shorter line applications. By this we mean that it takes a greater $\frac{3R_G}{K_1+K_2+pK_0}$ component to yield a Z phasor which is outside the operate zone. In Fig. 24C only the faulted phase characteristic is shown, since the other two fall well out of the first quadrant.

One might conclude from Fig. 24 that the relay is not directional since its characteristic includes the origin. This conclusion would be erroneous, since the characteristic equations assume faults in the trip direction per Fig. 14 and do not apply for reversed faults. The relay is directional. In Fig. 24 the second and third quadrants are essentially theoretical since a "negative resistance" is only possible due to out-of-phase infeed. The fourth quadrant is pertinent for series capacitor applications. So we are normally only interested in the first quadrant.

General Characteristics

Impedance settings in ohms reach can be made in steps of .3 percent. The maximum sensitivity angle, which is set for 75 degrees at the factory, may be set for any value from 60 degrees to 82 degrees. A change in the maximum sensitivity angle will produce a slight change in reach for any given setting of the relay. Referring to Fig. 11, note that the compensator secondary voltage output V, is largest when V leads the primary current, I, by 90°. This 90° relationship is approached, if the compensator loading resistor is open-circuited. The effect of the loading resistor, when connected, is to produce an internal drop in the compensator, which is out-of-phase with the induced voltage, IT_A, IT_B or IT_C. Thus the net voltage, V, is phase-shifted to change the compensator maximum sensitivity angle. As a result of this phase shift the magnitude of V is reduced, as shown in Fig. 11. The tap markings are based upon a 75° compensator angle setting. If the resistors R1, R2, R3, and R4 are adjusted for some other maximum sensitivity angle the nominal reach is different than that indicated by the taps. The reach Z_θ, varies with the maximum sensitivity angle, θ, as follows:

$$Z_\theta = \frac{TS \sin \theta (1 + M)}{\sin 75°}$$

TAP PLATE MARKINGS

T_A, T_B, T_C (Positive Sequence)

For 1.0-31 Ohms range- 1.2, 1.5, 2.1, 3.0, 4.5, 6.3, 8.7

For .2-4.35 Ohms range- .87, 1.16, 1.45, 2.03, 2.9, 4.06, 5.8

For .2-4.35 Ohms range- .23, .307, .383, .537, .69, .92, 1.23

T_0 (Zero Sequence)

For 1.0-31 Ohms range- 3.60, 4.5, 6.3, 9.0, 13.5, 18.9, 26.1

For .75-20 Ohms range- 2.61, 3.48, 4.35, 6.1, 8.2, 12.2, 17.4

For .2-4.35 Ohms range- 0.69, 0.92, 1.15, 1.61, 2.07 2.76, 3.69

	(S_A and S_C)		
	1	2	3
± Values between taps (M_A and M_C)	.03	.09	.06

TIME CURVES AND BURDEN DATA

Operating Time

The speed of operation is shown in Fig. 21. The curves indicate the time in milliseconds required for the relay to provide an output for tripping after the occurance of a fault at any point on a line within the relay setting.

Current Circuit Rating in Amperes (All Ranges, All Settings)

Continuous – 10 Amperes

1 Second – 240 Amperes

Burden

The potential burden at 69 volts varies from a maximum of 1.4 volt-amperes at S=1 setting to a minimum of 0.42 volt-amperes based on 69 volts line to neutral per phase. Current burden varies from a maximum of 4.5 volt-amperes at 5 amperes for a maximum T-setting to a minimum of 0.60 volt-amperes for a minimum T-setting. This burden applies to each phase and residual current circuit. D.C. current burden is .07 amperes at all rated voltages.

Trip Circuit Constants

1 Ampere I.C.S. 0.1 ohms d-c resistance

Thyristor (SDG Only)

The thyristor is a three-terminal semiconductor device. In the reverse, or non-conducting direction, the device exhibits the very low leakage characteristics of a silicon rectifier. In the forward, or conducting directions conduction can be initiated by the application of a control pulse to the control terminal or "gate". If a gate signal is not applied, the device will not conduct at below rated forward blocking voltage. With the application of a gate signal, however, the device switches rapidly to a conducting state characterized by a very low voltage drop and a high current-carrying capability. Once a conduction has been initiated, the gate terminal no longer has any effect. In order to turn the thyristor off the anode-cathode current must be reduced to a value less than the holding current.

It should be noted that the SDG differs from mechanically operated contacts. A certain minimum trip current must flow before the thyristor will latch on. However, voltage will be applies to the load for the duration of each pulse. Pulses are applied to the gate circuit at a rate of four every one milliseconds.

Current Rating Per Circuit:

Ambient Temperature	25°C	50°C	75°C
For 50 ms. (3 cycle breaker)	60 A	49A	37A
For 83 ms. (5 cycle breaker)	54A	44A	33A
Continuous	6.5A	4.5A	3A

Trip Circuit Requirements:

$$\frac{\text{Vdc}}{R_{\text{LOAD OHMS}}} = .25 \text{ amp or more}$$

$$\frac{L_{\text{HENRYS}}}{R_{\text{LOAD OHMS}}} = .02 \text{ or less}$$

Thyristor

Max. forward leakage current at rated voltage = 125°C 8 MA d-c

Max. reverse leakage current at rated voltage = 125° C 8 MA d-c

Max. forward voltage drop at 10 amps = 25° C 1.6 volts

CALCULATIONS AND SELECTION OF SETTINGS

Relay reach is set on the tap plate. Maximum sensitivity angle, θ, is set for 75° (current lagging voltage) in the factory. This adjustment need not be disturbed for line angles of 65° or higher. For line angles below 65°, set θ for a 60° maximum sensitiv-

ity angle, by adjusting R_1, R_2, R_3 & R_4, for zone 1 application only. Set zone 1 reach to be 85% of the line, if S=1 is used; 75% if S=2 or 3.

Assume a desired balance point which is 85% of the total length of the line. The general formulas for setting the ohms reach of the relay are:

$$Z_1 = Z_{1L} \frac{0.85\ Rc}{R_V}\ ;\ Z_0 = Z_{0L} \frac{0.85\ Rc}{R_V}$$

The terms used in this formula and hereafter are defined as follows:

Z_0 = Zero sequence ohmic reach.

Z_1 = Positive sequence ohmic reach

$Z_{1,0}$ = TS (1 + M) = the tap plate setting.

T = Compensator tap value.

S = Auto-transformer tap value.

θ = Maximum sensitivity angle setting of the relay.

±M = Compensator tertiary tap value. (This is a per unit value and is determined by the sum of the values between the "L" and the "R" leads. The sign is positive when "L" is above "R" and acts to raise the Z setting. The sign is negative when "R" is above "L" and acts to lower the "Z" setting).

Z_{1L} = Positive sequence ohms per phase of the total line section, referred to primary.

Z_{0L} = Zero-sequence ohms per phase of the total line section, referred to primary.

R_c = Current transformer ratio.

R_V = Potential transformer ratio.

The following procedure should be followed in order to obtain an optimum setting of the relay.

Zone 1 Setting (SDG, SDG-1, SDG-2 Relays)

1. a. Establish the desired values of Z_1 and Z_0 as above (available from transmission line data) and desired maximum sensitivity angle, $\theta°$.

   b. Determine the desired tap plate value Z' using the formula:

$$Z_1 = Z_1 \frac{\text{Sin } 75°}{\text{Sin } \theta°} \text{ and } Z_0 = Z_0 \frac{\text{Sin } 75°}{\text{Sin } \theta°}$$

When $\theta = 75°$, $Z_1 = Z_1$ and $Z_0 = Z_0$

2. Now refer to Table II or IV giving preferred zone 1 settings for the SDG relays. If the desired reach exceeds the relay range for S=1, use S=2 & Table III or V (set for 75% of line).

   a. Locate a table value for relay reach nearest to the desired Z' value (it will always be within 1.5% of the desired value.)

   b. From this table read off the "S", "T" and "M" settings. The "M" column includes additional information for the "L" and "R" lead setting for the specified "M" value. If the desired settings cannot be found on this table proceed to Table III or V to find the desired setting. The relay reach must now be reduced from 85 to 75 percent to avoid overreach on two phase to ground faults on high fault resistance faults.

   c. Recheck relay settings for Z_1' and Z_0' using equation:

   Z = TS (1 + M)

   For example, assume the desired reach, Z_1 is 7 ohms at 60° (Step 1a) and Z_0 is 21 ohms at 60°.

   Next step is (1b). Making correction of maximum sensitivity angle of the relay to match the characteristic angle of the line (60°) that is different from factory setting of 75°, we find the relay tap setting

   $Z_1' = 7 \times 1.11 = 7.77$ ohms

   $Z_0' = 21 \times 1.11 = 23.31$ ohms

   This procedure is followed when R_1, R_2, R_3, R_4 settings are changed, otherwise follow alternative procedure below.

   Step (2a). In Table IV we find 7.65 to be the nearest value to 7.77 ohms.

   $100 \times \frac{7.65}{7.77} = 98.8\%$ or 1.2% from the desired value

For the Z_0 selection find the nearest value to 23.31 ohms using the same S setting as above. 23.0 ohms is the nearest value.

$100 \times \frac{23.0}{23.31} = 98.8\%$ or 1.2% within the desired value

Step (2b). From Table IV read off:

S = 1
T = 8.7
M = -.12
T_0 = 26.1
M_0 = -.12

The "R" – lead should be connected over "L" – lead, with "L" lead connected to "O" – tap and "R" – lead to tap "09". (The sum of the values between L & R is 0.12)

Step (2c). Recheck Settings.

$Z_1 = TS(1 \pm M) = 1 \times 8.7(.88) = 7.65$ and

$Z_0' = 1 \times 26.1(.88) = 23.0$

$Z_1 = Z_1' \frac{\text{Sin } 60°}{\text{Sin } 75°} = 7.65 \times .900 = 6.90$ ohms at 60°

$Z_0 = Z_0' \frac{\text{Sin } 60°}{\text{Sin } 75°} = 23.0 \times .900 = 20.7$ ohms at 60°

Alternative Calculations and Settings

If it is desired to avoid recalibration of the relay maximum sensitivity setting the following procedure should be followed.

Follow Step 1a as above.

Change Step 1b to compute desired reach according with equation:

$$Z' = \frac{Z}{\text{Cos } (75-\theta)}$$

$$\text{Then } Z_1 = \frac{7}{\text{Cos } (75-60)} = \frac{7}{.965} = 7.25w$$

$$Z_0 = \frac{21}{\text{Cos } (75-60)} = \frac{21}{.965} = 21.75w$$

Step 2(a) as above From Table IV we find 7.25-value and 21.75 ohm-values as the exact values.

Step 2(b) From Table IV read off

S = 1
T = 6.3 T_0 = 18.9
M = +.15 M_0 = +.15

Step 2(c) Recheck settings:

$Z_1 = Z_1 \cos (75°-\theta) = 7.25 \times 965 = 7$ ohms

$Z_0 = Z_0 \cos (75-\theta) = 21.75 \times 965 = 21$ ohms

Zone 2 & 3 Settings

For zone 2 and 3 settings use a procedure similar to that for zone 1 described above. Tables II to V give the required settings. There is no need to recalibrate relay for, zone 2 or 3 application for difference in maximum torque angle.

Note: The S setting must be the same for both the positive and zero-sequence reach.

SETTING THE RELAY

The SDG relays require settings for the four compensators (T_A, T_B, T_C, and T_O), the three auto-transformer primaries (S_A, S_B, and S_C), and the four compensator tertiaries (M_A, M_B, M_C, and M_O). All of these settings are made with taps on the tap plate, and relay should be deenergized.

Compensator (T_A, T_B, T_C, T_0, and M_A, M_B, M_C, M_0)

Each set of compensator primary T_A, T_B, T_C, and T_O, taps terminates in inserts which are grouped on a socket and form approximately three-quarters of a circle around a center insert which is the common connection for all of the taps. Electrical connections between common insert and tap inserts are made with a link that is held in place with two connector screws, one in the common and one in the tap. A compensator tap setting is made by loosening the connector screw in the center. Before removing the screw open switches 12 through 19 to bypass the current around the relay. Remove the connector screw in the tap end of the link, swing the link around until it is in position over the insert for the desired tap setting, replace the connector screw to bind the link to this insert, and retighten the connector screw in the center. Since the link and connector screws carry operating current, be sure that the screws are turned to bind

snugly. Compensator secondary tap connections are made through two leads identified as L and R for each compensator. These leads come out of the tap plate each through a small hole, one on each side of the vertical row of "M" tap inserts. The lead connectors are held in place on the proper tap by connector screws.

Values for which an "M" setting can be made are from -.18 to +.18 in steps of .03. The value of a setting is the sum of the numbers that are crossed when going from the R lead position to the L lead position. The sign of the "M" value is determined by which lead is in the higher position on the tap plate. The sign is positive (+) if the L lead is higher and negative (-) if the R lead is higher.

An "M" setting may be made in the following manner. Remove the connector screws so that the L and R leads are free. Refer to Table II through Table V to determine the desired "M" value. Neither lead connector should make electrical contact with more than one tap at a time.

Line Angle Adjustment

Maximum sensitivity angle is set for 75° (current lagging voltage) in the factory. This adjustment need not be disturbed for line angles of 65° or higher. For line angles below 65° set for 60° maximum sensitivity angle by adjusting the compensator loading resistors R_1, R2, R_3, R_4. Refer to repair calibration under "Maximum Torque Angle Adjustment," when a change in maximum sensitivity angle is desired. For zone 2 and 3 application no need to recalibrate relay.

In general, the change in maximum torque angle adjustment, if desired, can be avoided. In this case the tap plate setting of the relay is adjusted to compensate for difference in the maximum torque angle of the relay (75°) and the characteristic angle of the line 8, according to the following equation:

$$Z_{1,0} = \frac{Z_{1,0}}{\text{Cos}\,(75°-\theta)}$$

Here $Z_{1,0}$ - Tap Plate Setting.

$Z_{1,0}$ - Desired Ohmic Reach.

TABLE II

.2-4.35 OHMS RELAY RANGE

PREFERRED ZONE 1 IMPEDANCE SETTINGS

POSITIVE SEQUENCE (Z_1) S = 1								ZERO SEQUENCE (Z_0) S = 1								M		CONNECT		
																		"L" LEAD TO TAP	"R" LEAD TO TAP	
T	.230	.307	.383	.537	.69	.92	1.23	T_0	.69	.921	1.15	1.61	2.07	2.76	3.69	+M	−M			
	.272	.362	.452	.632	.815	1.09	1.45		.815	1.09	1.36	1.90	2.44	3.26	4.40	+.18		.06	0	
	.264	.352	.441	.617	.794	1.06	1.41		.794	1.06	1.32	1.85	2.38	3.18	4.25	+.15		.06	.03	"L" OVER "R"
	.258	.344	.430	.601	.772	1.03	1.38		.772	1.03	1.29	1.80	2.32	3.10	4.15	+.12		.09	0	
	.251	.335	.418	.585	.754	1.00	1.34		.754	1.00	1.25	1.76	2.26	3.00	4.04	+.09		.09	.03	
	.244	.325	.405	.570	.732	.975	1.30		.732	.975	1.22	1.71	2.20	2.92	3.92	+.06		.06	.09	
	.237	.316	.396	.555	.710	.950	1.27		.710	.950	1.18	1.66	2.13	2.84	3.80	+.03		.03	0	
	.230	.307	.383	.537	.69	.920	1.23		.69	.921	1.15	1.61	2.07	2.76	3.69	0	0	0	0	
	.223	.298	.370	.520	.670	.892	1.19		.670	.892	1.12	1.56	2.00	2.68	3.58		−.03	0	.03	"R" OVER "L"
	.216	.288	.360	.505	.650	.865	1.15		.650	.865	1.08	1.52	1.95	2.60	3.46		−.06	.09	.06	
	.209	.280	.348	.488	.627	.840	1.12		.627	.840	1.05	1.47	1.88	2.51	3.36		−.09	.03	.09	
	.202	.270	.336	.472	.607	.810	1.08		.607	.810	1.01	1.42	1.82	2.43	3.25		−.12	0	.09	
	.195	.260	.324	.456	.587	.782	1.05		.587	.782	.980	1.37	1.76	2.35	3.14		−.15	.03	.06	
	.188	.252	.314	.440	.565	.755	1.01		.565	.755	.940	1.32	1.70	2.26	3.02		−.18	0	.06	

TABLE III

.2-4.35 OHM RELAY RANGE

PREFERRED ZONE 2 & 3 IMPEDANCE SETTINGS

POSITIVE SEQUENCE SETTINGS (Z_1)									ZERO SEQUENCE SETTINGS (Z_0)									M		CONNECT		
S = 2							S = 3		S = 2								S = 3			"L" LEAD TO TAP	"R" LEAD TO TAP	
T	.230	.307	.383	.537	.69	.92	1.23	.92	1.23	T_0	.69	.921	1.15	1.61	2.07	2.76	3.69	2.76	3.69	+M	−M	
	.544	.724	.905	1.26	1.63	2.17	2.90	3.26	4.40		1.63	2.17	2.72	3.80	4.90	6.50	8.70	9.80	12.1	+.18		.06	0	"L" OVER "R"
	.528	.704	.880	1.23	1.59	2.12	2.82	3.18	4.25		1.59	2.12	2.65	3.70	4.76	6.35	8.48	9.55	12.7	+.15		.06	.03	
	.516	.688	.860	1.20	1.55	2.06	2.76	3.10	4.15		1.55	2.06	2.58	3.60	4.65	6.20	8.25	9.30	12.4	+.12		.09	0	
	.502	.670	.835	1.17	1.51	2.00	2.68	3.00	4.04		1.51	2.00	2.50	3.50	4.52	6.00	8.05	9.05	12.1	+.09		.09	.03	
	.488	.650	.810	1.13	1.46	1.95	2.60	2.92	3.92		1.46	1.95	2.44	3.41	4.40	5.85	7.80	8.80	11.8	+.06		.06	.09	
	.474	.632	.790	1.10	1.42	1.90	2.53		3.80		1.42	1.90	2.37	3.32	4.26	5.70	7.60		11.4	+.03		.03	0	
	.460	.614	.766	1.07	1.38	1.84	2.46		3.69		1.38	1.84	2.30	3.22	4.14	5.52	7.38		11.1	0	0	0	0	
	.446	.596	.740	1.04	1.34	1.78	2.40		3.58		1.34	1.78	2.24	3.12	4.02	5.35	7.15		10.7		−.03	0	.03	"R" OVER "L"
	.432	.576	.716	1.01	1.30	1.73	2.32		3.46		1.30	1.73	2.16	3.02	3.90	5.16	6.94		10.4		−.06	.09	.06	
	.418	.560	.695	.975	1.25	1.67	2.24		3.36		1.25	1.67	2.09	2.94	3.78	5.00	6.70		10.1		−.09	.03	.09	
	.404	.540	.674	.940	1.21	1.62	2.17				1.21	1.62	2.02	2.83	3.66	4.85	6.50		9.8		−.12	0	.09	
	.390	.520	.650	.910	1.17	1.56	2.10				1.17	1.56	1.95	2.74	3.55	4.67	6.27		9.4		−.15	.03	.06	
	.376	.504	.625	.880	1.13	1.50	2.08				1.13	1.50	1.79	2.64	3.40	4.50	6.05		9.1		−.18	0	.06	

TABLE IV

1.1-31 OHMS RELAY RANGE

PREFERRED ZONE 1 IMPEDANCE SETTINGS

	POSITIVE SEQUENCE (Z_1) S = 1							ZERO SEQUENCE (Z_0) S = 1								M		CONNECT		
T	1.2	1.5	2.1	3.0	4.5	6.3	8.7	T_0	3.6	4.5	6.3	9.0	13.5	18.9	26.1	+M	−M	"L" LEAD TO TAP	"R" LEAD TO TAP	
	1.42	1.77	2.48	3.54	5.3	7.43	10.2		4.25	5.30	7.45	10.6	15.9	22.2	30.8	+.18		.06	.0	"L" OVER "R"
	1.38	1.73	2.42	3.45	5.17	7.25	10.0		4.15	5.17	7.25	10.4	15.5	21.7	30.0	+.15		.06	.03	
	1.34	1.68	2.36	3.36	5.04	7.05	9.75		4.05	5.04	7.05	10.1	15.1	21.2	29.3	+.12		.09	0	
	1.31	1.64	2.29	3.27	4.90	6.89	9.50		3.94	4.90	6.89	9.81	14.7	20.6	28.4	+.09		.09	.03	
	1.27	1.59	2.22	3.18	4.77	6.70	9.25		3.82	4.77	6.70	9.54	14.3	20.0	27.7	+.06		.06	.09	
	1.24	1.55	2.16	3.09	4.64	6.50	8.95		3.71	4.64	6.50	9.27	13.9	19.5	26.9	+.03		.03	0	
	1.20	1.5	2.10	3.00	4.50	6.30	8.70		3.6	4.50	6.30	9.0	13.5	18.9	26.1	0	0	0	0	
	1.16	1.45	2.04	2.91	4.36	6.10	8.45		3.50	4.36	6.10	8.73	13.1	18.3	25.2		−.03	0	.03	"R" OVER "L"
	1.13		1.97	2.82	4.23	5.90	8.15		3.38		5.90	8.46	12.7	17.7	24.5		−.06	.09	.06	
	1.09		1.91	2.73	4.10	5.74	7.90		3.27		5.74	8.19	12.3	17.2	23.7		−.09	.03	.09	
	1.06		1.85	2.64	3.96	5.55	7.65		3.16		5.55	7.92	11.9	16.6	23.0		−.12	0	.09	
	1.02		1.77	2.55	3.82	5.35			3.06		5.35	7.65	11.5	16.0			−.15	.03	.06	
	0.99				3.69				2.95				11.1				−.18	0	.06	

TABLE V

1.1-31 OHMS RELAY RANGE

PREFERRED ZONE 2 & 3 IMPEDANCE SETTINGS

T	POSITIVE SEQUENCE SETTINGS (Z_1')									ZERO SEQUENCE SETTINGS (Z_1')										M		CONNECT		
	S = 2							S = 3		S = 2								S = 3				"L" LEAD TO TAP	"R" LEAD TO TAP	
	1.2	1.5	2.1	3.0	4.5	6.3	8.7	6.3	8.7	T_0	3.6	4.5	6.3	9.0	13.5	18.9	26.1	18.9	26.1	+M	−M			
	2.84	3.54	4.96	7.08	10.62	14.9	20.5	22.3	30.8		8.50	10.6	14.9	21.2	31.8	44.5	61.5	66.6	92.5	+.18		.06	0	"L" OVER "R"
	2.76	3.46	4.84	6.90	10.35	14.5	20.0	21.6	30.0		8.30	10.34	14.5	20.7	31.0	43.5	60.0	65.1	90.0	+.15		.06	.03	
	2.68	3.36	4.72	6.72	10.08	14.1	19.5	21.2	29.3		8.10	10.08	14.1	20.2	30.2	42.4	58.5	63.6	87.5	+.12		.09	0	
	2.62	3.28	4.58	6.54	9.81	13.8	19.0		28.4		7.88	9.80	13.8	19.6	29.4	41.2	56.8		85.2	+.09		.09	.03	
	2.54	3.18	4.44	6.36	9.54	13.4	18.5		27.7		7.64	9.54	13.4	19.1	28.6	40.0	55.3		83.0	+.06		.06	.09	
	2.48	3.10	4.32	6.18	9.27	13.0	17.9		27.0		7.42	9.28	13.0	18.5	27.8	39.0	53.8		80.5	+.03		.03	0	
	2.4	3.0	4.20	6.0	9.0	12.6	17.4		26.1		7.20	9.0	12.6	18.0	27.0	37.8	52.2		78.3	0	0	0	0	
	2.32	2.90	4.08	5.82	8.73	12.2	16.9		25.2		7.00	8.72	12.2	17.5	26.2	36.6	50.5		75.8		−.03	0	.03	"R" OVER "L"
	2.26		3.95	5.64	8.46	11.8	16.3		24.5		6.76		11.8	16.9	25.4	35.4	49.0		73.5		−.06	.09	.06	
	2.18		3.82	5.46	8.19	11.5	15.8		23.7		6.54		11.5	16.4	24.6	34.4	47.5		71.0		−.09	.03	.09	
	2.12		3.70	5.28	7.92	11.1	15.3		23.0		6.32		11.1	15.8	23.8	33.2	45.8		68.8		−.12	0	.09	
	2.04		3.54	5.10	7.65	10.7			22.7		6.12		10.7	15.3	23.0	32.0					−.15	.03	.06	
	1.98				7.38										22.2						−.18	0	.06	

INSTALLATION

The relays should be mounted on switchboard panels or their equivalent in a location free from dirt, moisture, excessive vibration and heat. Mount the relay by means of the mounting stud for the type FT projection case or by means of the four mounting holes on the flange for the semi-flush type FT case. Either the stud or the mounting screws may be utilized for grounding the relay. The electrical connections may be made directly to the terminals by means of screws for steel panel mounting or to the terminal stud furnished with the relay for thick panel mounting. The terminal stud may be easily removed or inserted by locking two nuts on the stud and then turning the proper nut with a wrench.

For detailed information on the FT case refer to I.L. 41-076.

EXTERNAL CONNECTIONS

Figure 22 shows typical connection for single zone protection using an SDG relay.

ACCEPTANCE TEST

Acceptance tests consists of:

1. A visual inspection.
2. "Push-button" - check.
3. An electrical test to make certain that the relay measures the balance point impedance accurately.

1. Visual Inspection

Give a visual check to the relay to make sure there are no loose connections, broken resistors or broken wires.

.2-4.35 ohm relay	.75-20 ohm relay	1.0-31.0 ohm relay
all T= = 1.23	all T = 5.8	all T = 8.7
T_0 = 3.69	T_0 = 17.4	T_0 = 26.1
all S = 1	all S = 1	all A = 1
all M = +.18	all M = +.18	all M = +.18

2. Push-Button Check

Using the test connections of Fig. 23. Connect the a-c voltages as per test no. 1. No current connections are required. Connect the rated d-c voltages as shown. Open circuit the connections to terminal no. 7. Set $V_{BN} = V_{CN}$ = 70 Volts. Depress the white pushbutton. The pushbutton should light. If the pushbutton does not light, connect a d-c voltmeter or a 25 watt lamp as per Fig. 23. The voltmeter should have a minimum deflection of at least 5 volts. If there is a deflection but the lamp does not light this indicates a fault in the pushbutton circuit. If there is no indication proceed with the electrical test to isolate the fault in the pushbutton circuit or the relay.

3. Electrical Tests

Distance Unit

Tripping is indicated for the SDG relay when the 25 watt lamp shown on Fig. 23 turns on and for SDG-1, -2, -3, & -4 relays when DC voltmeter indicates a minimum deflection of 5 volts for balance point condition. Refer to Fig. 23 for all test connections.

For .2-4.35 Ohm Relay

A. Use connections for test No. 5 and set V_{AN} voltage = 20 volts. $V_{BN} = V_{CN}$ = 70 volts. Set the phase shifter for 75° current lagging voltage.

B. The relay current required to make the trip should be between 8.0-8.6 amp.

C. Use connections for Test No. 6 and set V_{BN} voltage = 20 volts. $V_{AN} = V_{CN}$ = 20 volts. Set the phase shifter as above. The relay trip current should be 8.0-8.6 amps.

D. Use connections for Test No. 7 and set V_{CN} = 20 volts $V_{AN} = V_{BN}$ = 70 volts. Set the phase shifter as above. The SDG relay trip current should be 8.0-8.6 amp.

For 1.0-31.0 ohm relay and .75-20 ohm Relay

A. Use connections for test #5 and set $V_{AN} = V_{BN} = V_{CN}$ = 70 volts. Set the phase shifter for 75° current lagging voltage. The relay trip current should be 3.95-4.20 amperes for 1-31 ohm relays and 5.95-6.30 amp for .75-20 ohm relays.

B. Use connections for test #6 and set $V_{AN} = V_{BN} = V_{CN}$ = 70 volts, and set the phase shifter as above. The relay trip current should be 3.95-4.20 amperes for 1-31 ohm relays and 5.95-6.30 amp. for .75-20 ohm relays.

C. Use test connections for test #7 and set $V_{AN} = V_{BN} = V_{CN} = 70$ volts. Set the phase shifter as above. The relay trip current should be 3.95-4.20 amperes for 1-31 ohm relays and 5.95-6.30 amp. for .75-20 ohm relays.

If the electrical response is outside the limits a more complete series of tests outlined in the section titled "Calibration" may be performed to determine which component is faulty or out of calibration.

If it is desired to check relay response at some other settings use following equation for the trip value of current.

$$I = \frac{3V_{LN}}{(2+p)Z_1}, \text{ Where } p = \frac{Z_0}{Z_1}$$

Z_0 = Zero sequence reach

Z_1 = Positive sequench reach (in above cases p = 3)

WARNING If testing required trip current over 15 amp. over prolonged periods, it is recommended that a heavy short lead be connected from terminal 19 to the center tap of T_Q-socket. Also connect a jumper lead from terminal 16 to terminal 1 on the large printed circuit board for SDG-1 and SDG-3 relays and terminal 2 to terminal 4 for SDG-relay on the large printed circuit board. (Lower set of terminals rear view).

MAXIMUM TORQUE ANGLE

Maximum torque angle check is optional. In general, this check is complicated for SDG, SDG-1 and SDG-2 relays by the presence of transient blocking circuit, and the two-phase-to-ground fault desensitizer circuit.

The presence of transient blocking circuit requires that check for maximum torque angle should be made going from non-tripping to tripping condition at each end of the tripping range of the relay under test. Since the lab method of testing as used here presents artificial voltage conditions under certain voltage and phase angle condition two-phase-to-ground desensitizer will distort phase angle response; hence, it is required to disable the 2ϕ-G circuit by jumpering terminal for SDG-1 and SDG-2 #10 to #1 on large printed circuit board (for SDG-relay jumper #10 terminal to #4).

Phase A Check

Use connection #5. Relay tap settings should be the same as before. For all ranges set $V_{AN} = 20$ volts, VBN-VCN = 70 volts.

Set current for 1-30 ohm relay for 1.54 amp, for .75-20 ohm relay for 2.30 amp and for .2-4.35 ohm relay for 11 amp. Set phase-shifter for 75°-current lagging V_{AN}-voltage. Turn phase-shifter toward 0° after relays have dropped out reverse phase-shifter rotation and note the angle (ϕ1) at which relay is fully tripped. Then rotate the phase-shifter past the 75° until relay resets again. Then rotate phase shifter toward 75° again until relay is fully tripped. Note the angle again (ϕ2).

Maximum

Maximum torque angle is equal then to

$$\frac{\phi_1 + \phi_2}{2} = 75° (\pm 3°)$$

Any other T setting may be used, except use 130% current of the trip current at 75° angle.

Phase B Check

Use connection #6. Set $V_{CN} = 20$ volts. $V_{AN} = V_{BN} = 70$ volts. Otherwise follow the same procedure as for Phase A.

When check is completed, remove the jumper.

TWO-PHASE-TO-GROUND DESENSITIZER CHECK

Use connection #5, except no current connection is required for this test.

AB - Combination

Set $V_{CN} = 70$ V. $V_{AN} = V_{BN} = 20$ volts. Check d-c voltage on small P.C. board located just behind R1-R4 potentiometer terminal "10" (positive) located behind R1-potentiometer (second from the bottom) and relay terminal "2". It should measure 11.5-13.5 volts.

Set $V_{CN} = 75$ V. $V_{AN} = V_{BN} = 10$ volts. The DC voltage should measure 16.5-18.5 volts.

BC - Combination

Same check as for AB-except first set V_{AN} = 70V. $V_{BN} = V_{CN}$ = 20 volts and then V_{AN} = 75V. $V_{BN} = V_{CN}$ = 10 volts.

CA - Combination

Same check as for AB-except first set V_{BN} = 70V. $V_{CN} = V_{AN}$ = 20 volts and then V_{BN} = 75V, $V_{CN} = V_{AN}$ = 10 volts.

Overcurrent Unit

Check operation of the overcurrent unit by using test connection #5 of the Fig. 23. Set V_{AN} = 0, $V_{BN} = V_{CN}$ = 70 volts. The .2-4.35 ohm relay should operate at .75-.83 ampere, and the 1-31.0 ohms relay and .75-20 ohms relay should operate at .37-.420 amperes. If not, check adjustment of R45 for SDG relay and R48 for SDG-1 and SDG-3 relays.

Frequency Verifier

Use connection #5. Set V_{AN} = 0 volts, $V_{BN} = V_{CN}$ = 70 volts. Output of the Frequency Verifier is observed at test point TP6—for SDG Relay or TP10—for SDG-1 and SDG-2 relays. Use oscilloscope or DC voltmeter to observe the output. If oscilloscope is used, the output should be a positive pulse having 4.0 to 4.3 millisecond width at the base. If voltmeter is used the voltage at the test point should be approx. one helf of the voltage across the power zener (Z_1). This voltage is controlled by value of R38-resistor and C11-capacitor for SDG-relay or R43 and C10-for SDG-1 and SDG-2 relays. Smaller value of these components will increase the pulse width, and increase the voltage magnitude at test point.

Indicating Contactor Switch (ICS) (SDG Only)

With the SDG relay tripping, pass sufficient d-c current through the trip circuit to close the contacts of the ICS. This value of current should be not less than 1.0 ampere or greater than 1.2 amperes, for the 1 ampere ICS. The current should not be greater than the particular ICS tap setting being used for the 0.1-2.0 ampere ICS. The operation indicator target should drop freely.

The contact gap should be approximately 0.047" for the 0.2-2.0 ampere unit and 0.070" for the 1.0 ampere unit between the bridging moving contact and the adjustable stationary contacts. The bridging moving contact should touch both stationary contacts simultaneously.

ROUTINE MAINTENANCE

The relays should be inspected periodically, at such time intervals as may be dictated by experience, to insure that the relays have retained their calibration and are in proper operating condition.

"In-Service Test" (If relay is set for S = 1 only)

In-service testing is performed as follows:

1. Open relay trip circuit by opening red handle switch No. 11.
2. Open relay voltage terminal 7.
3. Press white pushbutton. Pushbutton light should light.

This test checks out the operation of the magnitude comparator and output circuitry.

REPAIR CALIBRATION

Use the following procedure for calibrating the relay if the relay has been taken apart for repairs or the adjustments disturbed.

For easier access to the parts, the relay should be tested without the case.

Part A Preliminary Settings

1. Set R9, R10, R11 resistors if they are adjustable type (located in front) using the following procedure: (To set resistors loosen the adjustable band and carefully move the band to a different setting. Retighten the band so not to damage resistance wires.)
   a. Remove the printed circuit board(s) (PCB) in the rear of the relay.
   b. Using a bridge type instrument, set the adjustable band next to the fixed terminal having the wire connection to measure 1600 (±35) ohms
   c. Set the second adjustable band from the same fixed terminal to measure a total 6000 (±100) ohms.
2. Set R_1-R_2-R_3-R4 potentiometers fully counterclockwise for maximum resistance.
3. Set relay for S=1, M=+18 ("L" lead over "R" lead), all T=8.7, T_0=26.1 for the 1.0-31.0 ohm relays and for the .2-4.35 ohms relay all T=1.23

and T_0=3.69, or all T=5.8, T_0=17.4 for .75-20 ohms relay.

Part B Voltage Circuit Tests

1. Apply 3 phase balanced voltages as per test 1 of Fig. 23, except no current is applied.

2. Set $V_{AN} = V_{BN} = V_{CN}$ = 70 volts a-c. Measure following a-c voltages:

   From relay terminal 6 to S_A = 1 Tap
   70 (±1) volts

   From relay terminal 6 to S_A = 2 Tap
   140 (±2) volts

   From relay terminal 6 to S_A = 3 Tap
   221 (±3) volts

   From relay terminal 6 to R_A lead
   39.2 (±5) volts

   Repeat the same measurements for S_B, S_C, and R_B, R_C-leads.

3. Disconnect R_0-lead from M_0=0 Tap and measure the voltage from relay terminal "4" to the R_0-lead. It should be below 0.5 volts ac.

4. Apply rated d-c voltage to the relay. Check the d-c voltage across the lower set of plug-in terminals (rear view) "5" and "1" for the SDG-1, -2, -3, & -4 relays and terminals "6" and "4" for the SDG-relay. It should measure 20 (±2) volts. (Notice 250 V. d-c relay requires external resistor).

5. Plug in the lower and upper boards.

Part C Potentiometer Adjustments

NOTE: All potentiometers are the locked type and should be unlocked before adjustment and locked after adjustment is complete.

1. Set R1, R2, R3, R4, R5, R6, R7, R8 for maximum setting (counter-clockwise).

2. Measure the voltages with a Rectox type voltmeter across the specified terminals of the small upper terminal board located in the rear. All the following measurements are done on the small upper board. Terminal numbers refer to this board only.

R5-Adjustment

Measure the voltage across terminals 2 & 3. Adjust R5 until voltages across 4 & 2 and 4 & 3 are equal (±.1 volt) to each other and are within 1.0 volt of voltage across 2 & 3. If oscilloscope is available observe voltage across R9 and set R5 so that all peaks on the 360Hz ripple are equal.

R6-Adjustment

Measure the voltage across terminals 6 & 8. Adjust R6 until voltages across terminals 7 & 6 and 7 & 8 are equal (±.1 volt) to each other and are within 1.0 volt of voltage across 6 & 8. If oscilloscope is available observe voltage across R10 and set R6 so that all peaks are equal.

R-7 Adjustment

Measure the voltage across terminals 17 & 18. Adjust R7 until voltages across terminals 15 & 18 and 15 & 17 are equal (±0.1 volt) to each other and are within 1.0 volt of voltage across 17 & 18. If oscilloscope is available observe voltage across R11 and set R7 so that all peaks are equal.

R8-Adjustment

Reduce V_{AN} to zero and measure the voltage across terminals 11 & 12. Adjust R8 until voltages across terminals 14 & 11 and 14 & 12 are equal (±0.1 volt) to each other and are within 1.0 volt of voltage across 11 & 12. If oscilloscope is available observe voltage across R12 and set R8 so that all valleys are equal.

Maximum Torque Angle Adjustment

Disconnect all R & L-leads and Jumper Relay Terminals 5 and 6.

R-1 Adjustment

For the 1.0-31.0 ohm relay use the #1 test connection of Fig. 23. Apply 5.08 amp. a-c current to the relay. Set V_{AN} = 45 volts and $V_{BN} = V_{CN}$ = 0 volts. Set the phase shifter for 75° current lagging voltage. For the .75-20 ohm relay apply 7.6 amps.

For .20-4.35 ohm relay use the same procedure as above except set the current for 15.65 amp. and V_{AN} = 20.0 volts.

Insert an a-c voltmeter of 0-3 volts range between R_A-and L_A-leads. Adjust R1-potentiometer for a minimum ("null"-reading) and lock R1 in place. Vary current slightly to achieve lower "null" reading.

R2-Adjustment

Use #2 test connections of Fig. 23. Set V_{BN} = 45 volts and $V_{AN} = V_{CN} = 0$ volts. Set I_B = 5.08 amps. 75° lagging V_{BN}. (Modify voltage and current settings for the .2-4.35 ohm and .75-20 ohms relays as above). Measure the voltage between R_B & L_B leads. Adjust R2-potentiometer for a minimum ("null"-reading) and lock R2 in place.

R3-Adjustment

Use the #3 test connections of Fig. 23. Set V_{CN} = 45 volts and $V_{AN} = V_{BN} = 0$ volts. I_C = 5.08 amp. 75° lagging V_{CN}. (Modify voltage and current for the .2-4.35 ohm and .75-20 ohms relays as above).

Measure the voltage between R_C and L_C leads Adjust R3-potentiometer for a minimum ("null"-reading) and lock R3 in place.

R4-Adjustments

Remove jumper from relay terminals 5 and 6. Use the #4 test connections of Fig. 23. Connect all "L"-and "R"-leads back to previous setting. Set $V_{CN} = 0$ and $V_{AN} = V_{BN}$ = 70 volts. Set I_C = 2.34 amp. 75° lagging V_{CN}. (For the .2 to 4.35 relay set $V_{CN} = 0$ and $V_{BN} = V_{AN}$ = 45 volt. I_C = 9.9 amperes). Measure the voltage between R_0 and the lowest M_0-tap marked "0". Adjust the R-4 potentiometer for minimum voltage ("null"-reading) and lock R4 in place. For 0.75-20 ohms relay set $V_{CN} = 0$, $V_{AN} = V_{BN}$ = 70 volts, I_C = 3.51 amps.

Part D.M-Taps Check

Use a Rectox type voltmeter

M_A-Taps — Use test connection #1 of Fig. 23. Pass 10 amp. current through the relay. The voltage should read the following:

1.5 (±2) volts	For	between 0 tap and .03 tap
6.0 (±2) volts	1-30	between 0 tap and .09 tap
9.0 (±2) volts	Ohms	between 0 tap and .06 tap

1.0 (±.1) volts	For	between 0 tap and .03 tap
4.0 (±.1) volts	.75-20	between 0 tap and .09 tap
6.0 (±.1) volts	Ohms	between 0 tap and .06 tap

M_B-Taps-Use test connection #2 and repeat above.

M_C-Taps-Use test connection #3 and repeat above.

M0-Taps-Use test connection #4 and repeat above.

For .2-4.35 ohm relay

NOTE: Provide a jumper from terminal 19 to center tap of the T_0 tap block for the SDG, SDG-1, and -3 relays.

M_A-Taps-Use test connection #1 of Fig. 23. Pass 20 amp. of current through relay. The voltage should read the following:

.425 (±.05 volts)	between "0" tap and ".03" tap
1.70 (±.1 volts)	between "0" tap and ".09" tap
2.55 (±.1 volts)	between "0" tap and ".06" tap

M_B-Taps-Use test connection #2 and repeat above.

M_C-Taps-Use test connection #3 and repeat above.

M_0-Taps-Use test connection #4 and repeat above.

Part E Impedance Tests

Tripping is indicated for the SDG relay when the 25 watt lamp shown on Fig. 23 turns on and for SDG-1, -2, -3 & -4 relays when DC voltmeter indicates minimum deflection of 5 volts for balance point condition, but should rise over 18 v.d.c. when current is increased. Refer to Fig. 23 for all test connections.

For .2-4.35 Ohm Relay

A. Use connections for test No. 5 and set V_{AN} voltage = 20 volts. $V_{BN} = V_{CN}$ = 70 volts. Set the phase shifter for 75° current lagging voltage.

B. The relay current required to make the trip should be between 8.0-8.6 amp.

C. Use connections for Test No. 6 and set V_{BN} voltage = 20 volts. $V_{AN} = V_{BN}$ = 70 volts. Set the phase shifter as above. The SDG relay trip current should be 8-8.6 amp.

D. Use connections for Test No. 7 and set VCN = 20 volts. $V_{AN} = V_{BN}$ = 70 volts. Set the phase shifter as above. The SDG relay trip current should be 8.0-8.6 amp.

For 1.0-31.0 Ohm Relay

A. Use connections for test #5 and set $V_{AN} = V_{BN} = V_{CN} = 70$ volts. Set phase shifter for 75° current lagging voltage. The relay trip current should be 3.95-4.20 amperes. (5.95-6.30 amp. for .75-20 ohm relay)

B. Use connections for test #6 and set $V_{AN} = V_{BN} = V_{CN} = 70$ volts, and set the phase shifter as above. The relay trip current should be 3.95-4.20 amperes. (5.95-6.30 amp. for .75-20 ohm relay)

C. Use test connections for test #7 and set $V_{AN} = V_{BN} = V_{CN} = 70$ volts. Set the phase shifter as above. The relay trip current should be 3.95-4.20 amperes. (5.95-6.30 amp. for .75-20 ohm relay)

If it is desired to check relay response at some other settings use following equation for the trip value of current.

$$I = \frac{3V_{LN}}{(2+p)Z_1}, \text{ Where } p = \frac{Z_0}{Z_1}$$

Z_0 = Zero sequence reach

Z_1 = Positive sequence reach (in above cases p = 3)

WARNING: If testing requires trip current over 15 amp. over prolonged periods, it is recommended that a heavy short lead be connected from terminal 19 to the center tap of T_0-socket. Also connect a jumper lead from terminal 16 to terminal 1 on the large printed circuit board for SDG-1 and SDG-3 relays and terminal 2 to terminal 4 for SDG-relay.

(Lower set of terminals rear view).

Let $V_{AN} = V_{BN} = V_{CN} = 70$ volts.

Change all the S-setting to S = 3 and repeat the impedance test. Trip current for the 1.0-31.0 ohm relay should be 2.66-2.87 amp. and 9.4-10.0 amp. for the .2-4.35 ohm relay and 4.0-4.30 amp for .75-20 ohms relay.

LOW-VOLTAGE BALANCE POINT CALIBRATION

When performing this test on SDG, SDG-1, or SDG-3 relays that have 1.0-30.0 ohms reach or .75-20.0 ohms reach disable I_0-circuit by jumpering terminal 16 to 1 on large printed circuit board for SDG-1 and SDG-3 relays and terminals 2 and 4 for SDG-Relay.

SDG – SDG-1 – SDG-2 Relays

1. Use connection #5. Set V_{AN} = 2.5V, $V_{BN} = V_{CN}$ = 70V. Set phase shifter for current lagging voltage by 75°. Check pick-up current. Note it.

2. Use connection #6. Set V_{BN} = 2.5V. $V_{AN} = V_{CN}$ = 70V. Check pick-up current. Note it.

3. Use connection #7. Set V_{CN} = 2.5V. $V_{AN} = V_{BN}$ = 70V. Check pick-up current. Note it.

The pick-up currents for each test should be within the following limits.

.2-4.35 ohms	1.05-1.15 amp.
.75-20.0 ohms	.208-.232 amp.
1.0-31.0 ohms	.140-.155 amp.

If the currents are outside their limits the following procedure should be followed. Set $V_{AN} = V_{BN} = V_{CN}$ = 70 volts as close to each other as possible. Use connection #5. No current is applied. Measure DC-voltage across R9, R10, R11-resistors. Readjust potentiometers P5, P6, P7 until the voltages across R9, R10, R11 are as close to each other as possible. These voltages should be in 20-25 volts range. In most cases only slight adjustment of P5, P6 or P7 will be required. Then recheck pickup current again. If the pickup currents are close together but outside the specified limits, change R_X-resistor to lower value for lower pickup current, and conversely increase it for higher values of pickup. Note the P5, P6, P7 are interacting. Hence, recheck all three voltages after each adjustment. If difficulties in balancing at 2.5 volts persist, use the same test as for SDG-3 and SDG-4 below.

SDG-3 and SDG-4

Same procedure as above except use 5 volts instead of 2.5 volts as low-voltage check point the pickup currents should be as below:

.2-4.35 ohms	2.10-2.30 amp.
.75-20.0 ohms	.416-.464 amp.
1.0-30.0 ohms	.280-.310 amp.

Use the same P5-P6-P7 adjustment procedure as above.

Indicating Contactor Switch (when used)

With the relay tripped, pass sufficient d-c current through the trip circuit to close the contacts of ICS. This value of current should be not less than 1.0 ampere, nor greater than 1.2 amperes for the 1 ampere ICS. The current should not be greater than the particular ICS Setting being used for the 0.2-2.0 amperes ICS. The operation indicator target should drop freely.

The contact gap should be approximately 0.047" for the 0.2-2.0 ampere unit and 0.070" for the 1.0 ampere unit between the bridging moving contact and the adjustable stationary contacts. The bridging moving contact should touch both stationary contacts simultaneously.

RENEWAL PARTS

Repair work can be done most satisfactorily at the factory. However, interchangeable parts can be furnished to the customers who are equipped for doing repair work. When ordering parts, always give the complete nameplate data, and component style number given in the electrical parts list.

ELECTRICAL PARTS LIST

Circuit Symbol	Description	Westinghouse Style Number
Printed Circuit Board (SDG-1, -2)		836A777H01
(SDG-3 & 4) (Fig. 26)		836A777H03
	DIODES	
D1 to D24	B2N9	837A692H04
D37-D38-D62-D67-D70	1N3283	837A692H02
	CONTACT STRIP	
		187A637H02
Printed Circuit Board		670B499H01
(SDG) (Fig. 27A) -125V.D.C.		670B499H01
(SDG-1 & 3) (Fig. 27B)		670B499H02
(SDG-2 & 4) (Fig. 27C)		670B499H03
(SDG) (Fig. 27A) 48V.D.C.		670B499H04
	CAPACITORS	
C13-C14-C15	.5 MFD.	187A624H03
	DIODES	
D54-D55	1N4385	184A855H14
	RESISTORS	
R52 (125 V.D.C.)	2.2K	763A127H11
R56	700 Ohms 2W	763A127H28
R52 (48 V.D.C.)	21 Ohms 3W	763A127H33
Large Printed Circuit Board (SDG) (Fig.)28)		411C213H01
	CAPACITORS	
C5-C7	2 MFD.	184A662H07
C6	.25 MFD.	187A624H02
C8-C10-C19-C20	.02 MFD.	187A624H09
C12	2.2 MFD.	187A508H19
C9	.10 MFD.	187A624H01
C11	.56 MFD.	764A278H08
	DIODES	
D40 to D49-D51-D52 D57-D59-D60-D61 D64 to D66-D87	1N4385	184A855H14
D50	M4L2053	629A370H04
D29-D30-D32 D33-D35-D36	1N3283	837A692H02
D72	CER69	188A342H06
D26-D27	B2N9	837A692H04
D53	1N3283	837A692H02
	TUNNEL DIODES	
TD3, TD58	1N3713	836A602H01
TD4-TD5	1N2928	836A602H02

Circuit Symbol	Description	Westinghouse Style Number
Printed Circuit Board (SDG) (Fig. 28) Cont.		
	ZENER DIODES	
Z3	1R200	629A369H01
Z4	1N759A	837A693H01
Z5	1N3805A	185A089H05
	POTENTIOMETER	
R45	2.5K Ohm-¼W.	629A430H03
	RESISTORS	
R17	100 Ohm-½W.	629A531H08
R18	56 Ohm-½W.	629A531H02
R19	1.5K Ohm-½W.	629A531H36
R20-R21-R46	2.7K Ohm-½W.	629A531H42
R24	22K Ohm-½W.	629A531H64
R25-R26	68K Ohm-½W.	629A531H76
R28	2.7K Ohm-½W.	629A531H42
R29-R30	39K Ohm-½W.	629A531H70
R31-R37-R36	470K Ohm-½W.	629A531H24
R32-R33	1K Ohm-½W.	629A531H32
R34	6.2K Ohm-½W.	629A531H51
R35	20K Ohm-½W.	629A531H63
R38	8.2K Ohm-½W.	629A531H54
R65	5.6K Ohm-½W.	629A531H50
R43	2K Ohm-½W.	629A531H39
R48	3.3K Ohm-½W.	629A531H44
R49	2K Ohm-½W.	836A503H33
R27	30K Ohm-½W.	629A531H67
R42	47K Ohm-1 W.	629A371H17
R44	1K Ohm	629A531H32
R55	2K Ohm	629A531H39
R53-R54	2K Ohm-½W.	836A503H33
R57	2K Ohm-1 W.	187A643H34
	TRANSISTORS	
Q2-Q5-Q6	2N1132	184A638H20
Q3-Q4	2N336	184A638H06
Q1-Q8	2N697	184A638H18
Q7	2N3417	848A851H02
	SWITCHES	
QS2-QS3	2N886	185A517H03
	TRANSFORMER	
T1	—	629A453H02

ELECTRICAL PARTS LIST

Circuit Symbol	Description	Westinghouse Style Number
Printed Circuit Board (SDG) (Fig. 28) (Cont.)		
	TRANSISTOR RADIATOR	
		188A002H01
Printed Circuit Board (SDG-1) (Fig. 29)		411C822G01
(SDG-2)		411C830G01
(SDG-3)		411C831G01
(SDG-4)		411C832G01
	CAPACITORS	
C5	2 MFD.	184A662H07
C6	.10 MFD.	187A624H01
C7-C9-C19-C20	.02 MFD.	187A624H09
C8	.10 MFD.	187A624H01
C10	.56 MFD.	764A278H08
C11	2.2 MFD.	187A508H19
	DIODES	
D26-D27	B2N9	837A692H04
D40-D43 to D53-D56-D58-D59-D64 to D66-D87 to D90	1N4385	184A855H14
D72	CER69	188A342H06
D29-D30-D32 D33-D35-D36	1N3283	837A692H02
D39-D5	1N3283	837A692H02
	TUNNEL DIODES	
TD1-TD3	1N2928	836A602H02
TD2-TD4 (D57)	1N3713	836A602H01
	ZENER DIODES	
Z3	1N9578	186A797H06
Z4	1N3686B	185A212H06
Z5	1N759A	837A693H01
Z6	1N3805A	185A089H05
	POTENTIOMETERS	
R48	2.5K	629A430H03
	RESISTORS	
R57	2K Ohm-1W.	187A643H34
R17	100 Ohm-½W.	629A531H08
R18	56 Ohm-½W.	629A531H02
R30-R65	4.7K Ohm-½W.	629A531H48
R22-R26	22K Ohm-½W.	629A531H64
R23	27K Ohm-½W.	629A531H66
R24	4.7K Ohm-½W.	629A531H48
R19	1.5K Ohm-½W.	629A531H36
R28-R37-R38	1K Ohm-½W.	629A531H32
R31-R32-R51	2.7K Ohm-½W.	629A531H42

Circuit Symbol	Description	Westinghouse Style Number
Printed Circuit Board (SDG-1) (Fig. 29) (Cont.) **(SDG-2)** **(SDG-3)** **(SDG-4)**		
	RESISTORS	
R33-R34	68K Ohm-½W.	629A531H76
R35-R36	39K Ohm-½W.	629A531H70
R39	6.2K Ohm-½W.	629A531H51
R21	30K Ohm-½W.	629A531H67
R40	20K Ohm-½W.	629A531H63
R41	1.5K Ohm-½W.	836A503H30
R42-R68	470K Ohm-½W.	629A531H24
R43	8.2K Ohm-½W.	629A531H54
R44	2K Ohm-½W.	836A503H33
R46	47 Ohm-1 W.	629A371H17
R47	2K Ohm-½W.	629A531H39
R49	3.3K Ohm-½W.	629A531H44
R50	1K Ohm-½W.	629A531H32
R54-R66	5.6K Ohm-½W.	629A531H50
R55	2K Ohm-½W.	629A531H39
R58-R59	2K Ohm-½W.	836A503H33
	TRANSISTORS	
Q1-Q5-Q7-Q13	2N697	184A638H18
Q2-Q6-Q10-Q11	2N1132	184A638H20
Q8-Q9	2N336	184A638H06
Q3	2N3391	848A851H01
Q12	2N3417	848A851H02
	SWITCHES	
QS1	2N1881	184A640H08
QS2-QS3	2N886	185A517H03
	TRANSISTOR RADIATOR	
		188A002H01
Printed Circuit Board SDG-SDG-1-2 (2 ϕ - Ground)		670B739
	TRANSISTORS	
Q17	2N697	184A638H18
Q18	2N1132	184A638H20
	DIODES	
D73 to D80 D82-D84 to D86	1N4385	184A855H14
	RESISTOR	
R13 to R15	15K-5W.	763A129H09
R20 (SDG-1 or -2)	4.7K-½W.	629A531H48
R40 (SDG)	4.7K-½W.	629A531H48

INDEX TO FIGURES

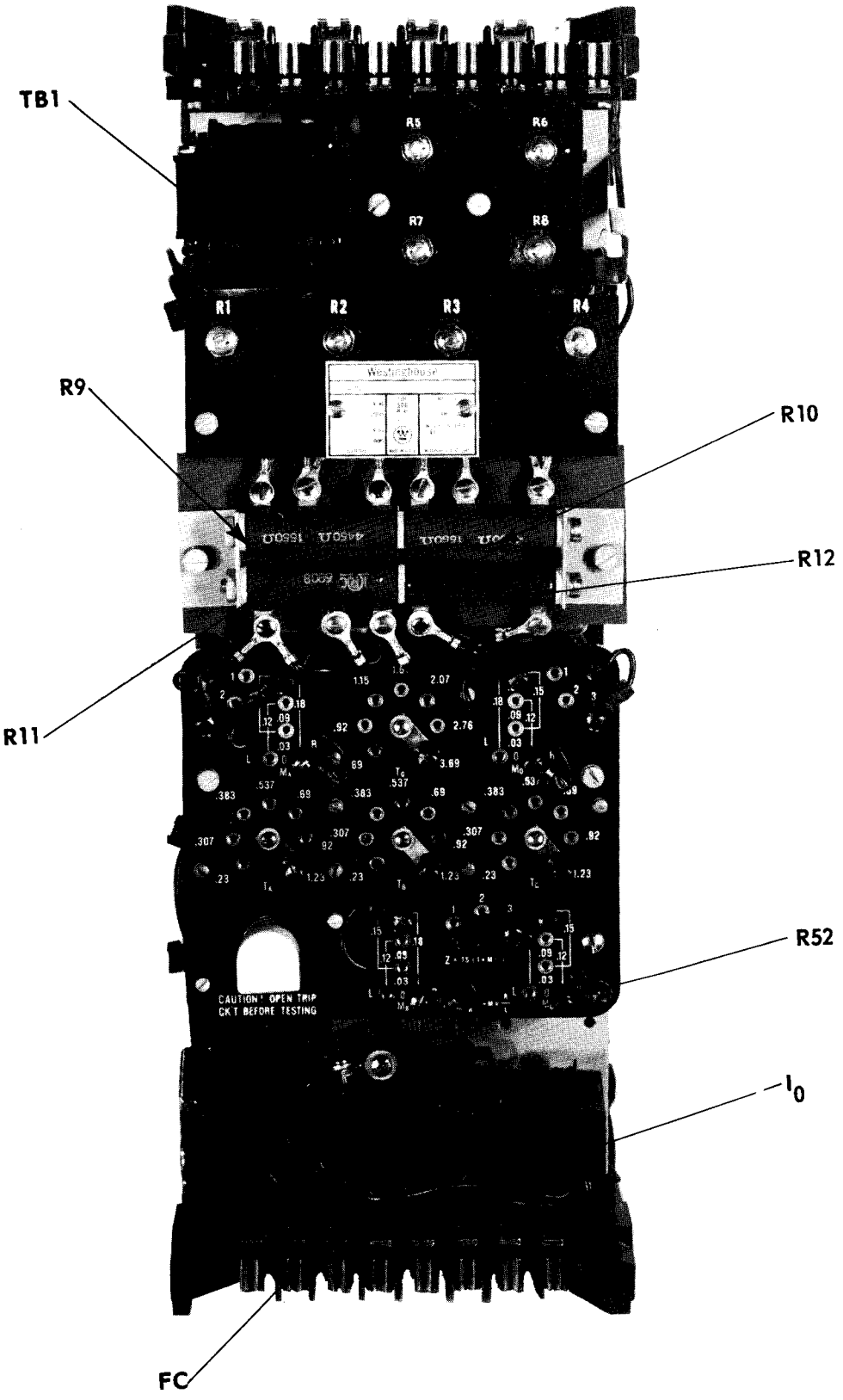


Fig. 1. Type SDG-1 Relay Without Case (Front View)

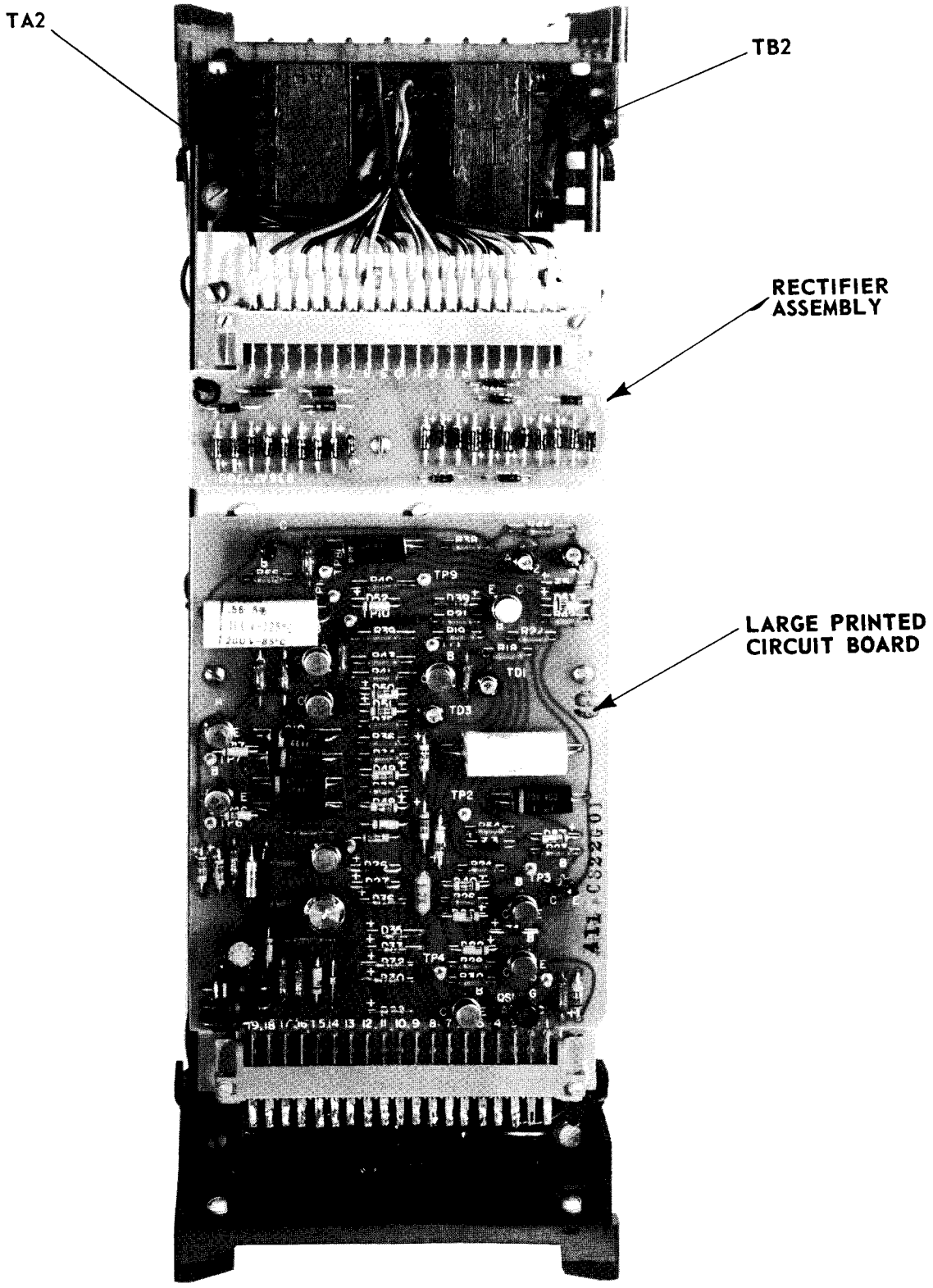


Fig. 2. Type SDG-1 Relay Without Case (Rear View)

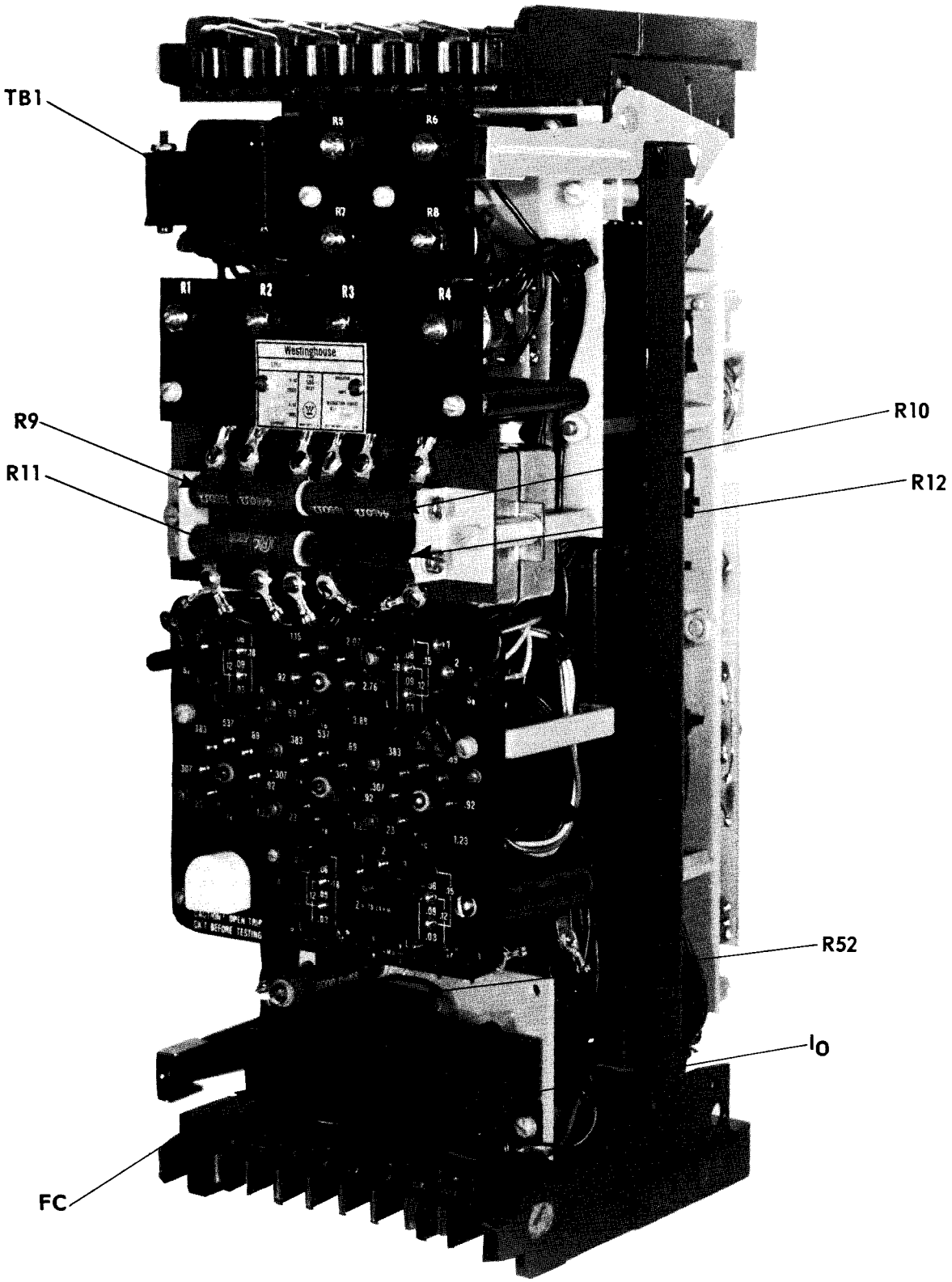


Fig. 3. Type SDG-1 Relay Without Case (Side View)

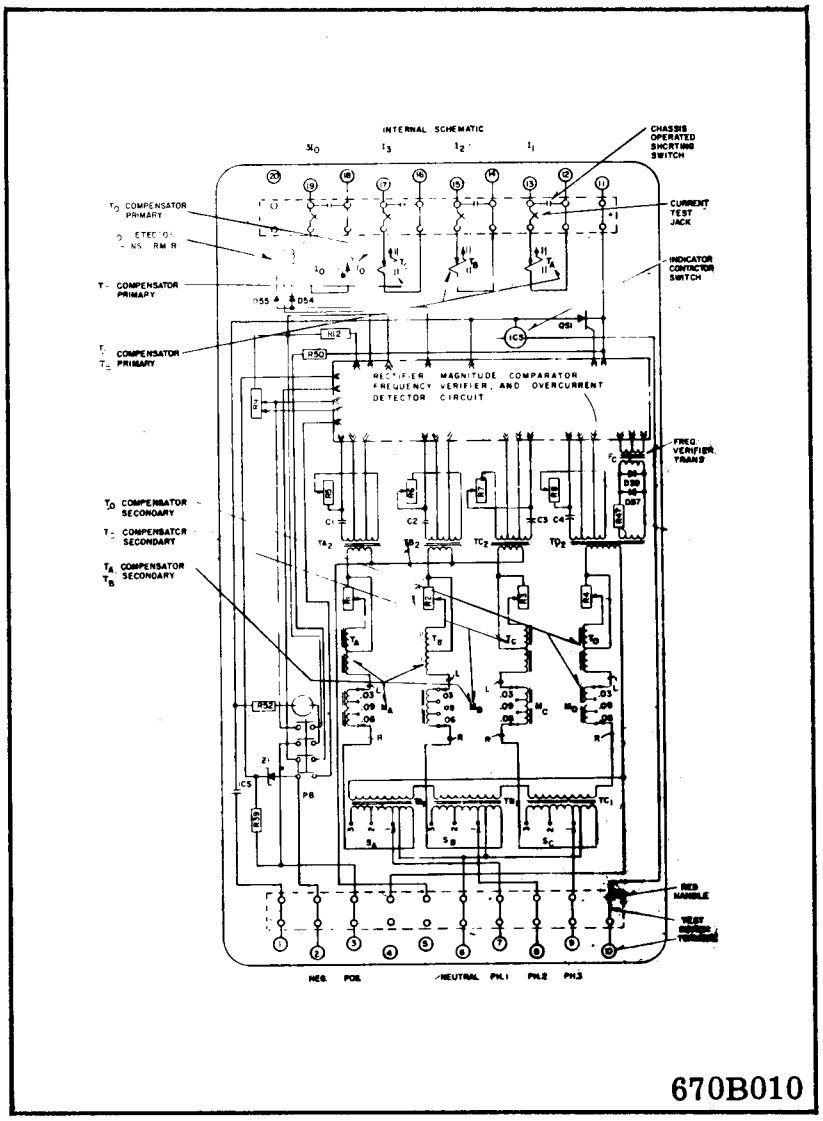


Fig. 4. Internal Schematic of the Type SDG Relay in FT-42 Case

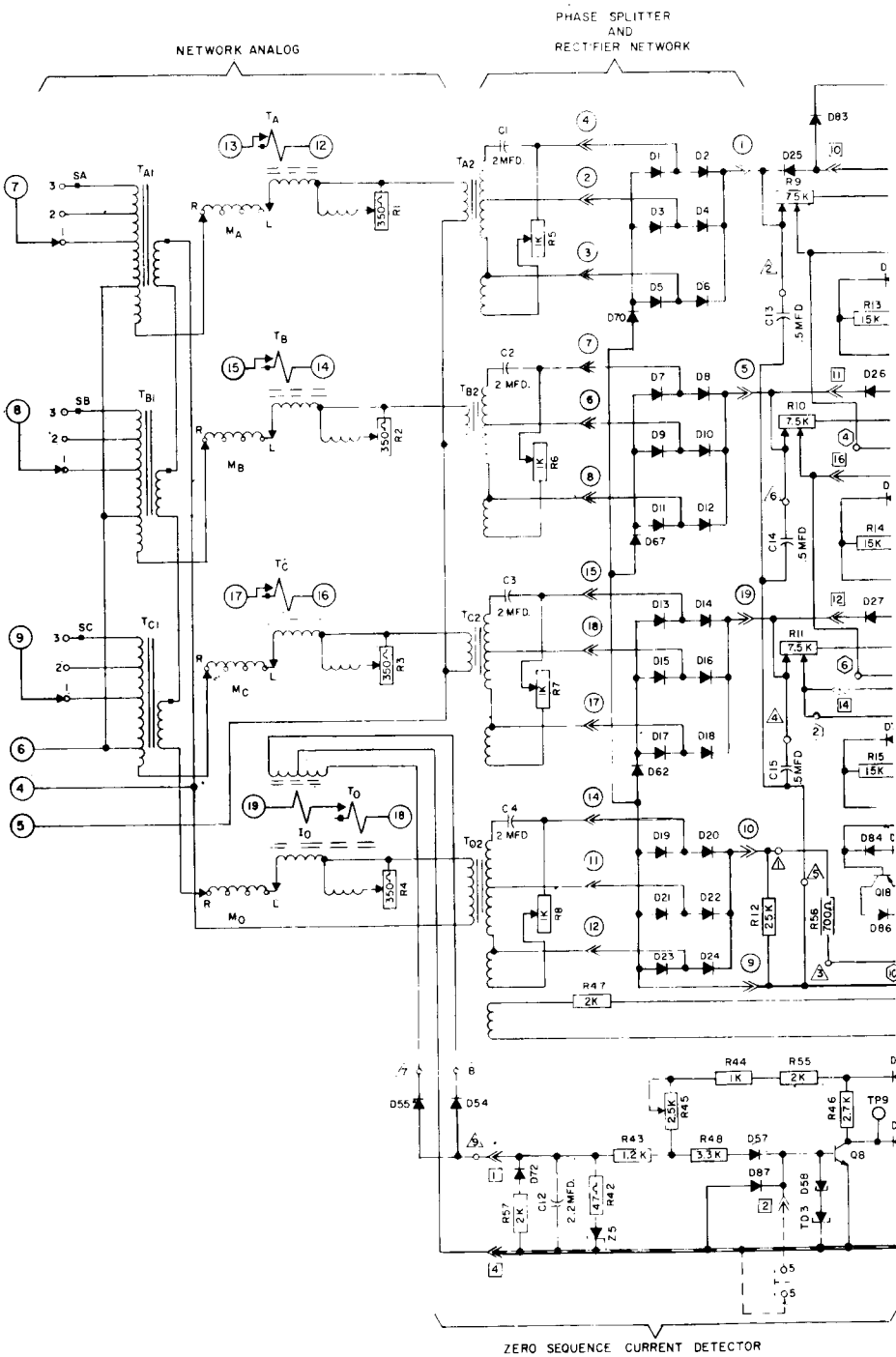


Fig. 5. Detailed Internal

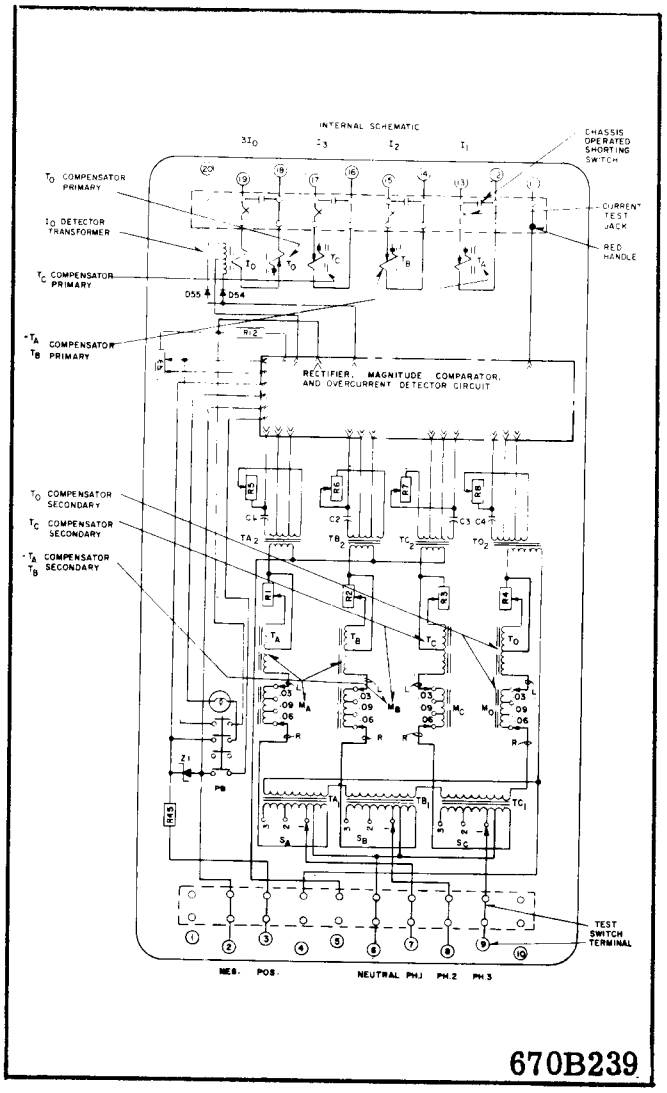


Fig. 8. Internal Schematic of the Type SDG-3 Relay in FT-42 Case

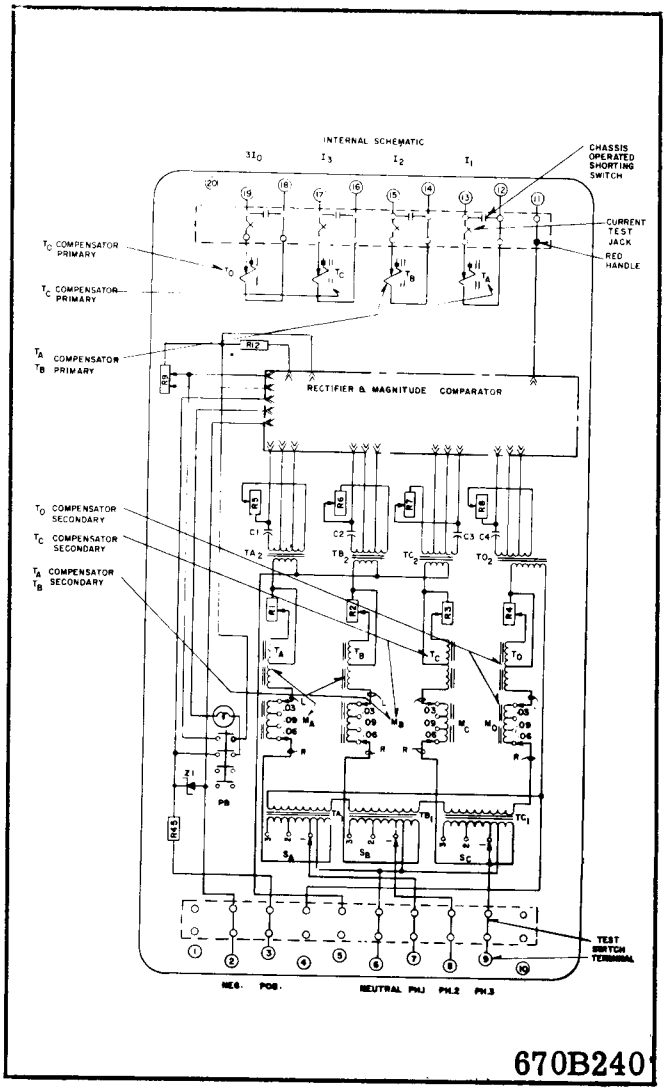
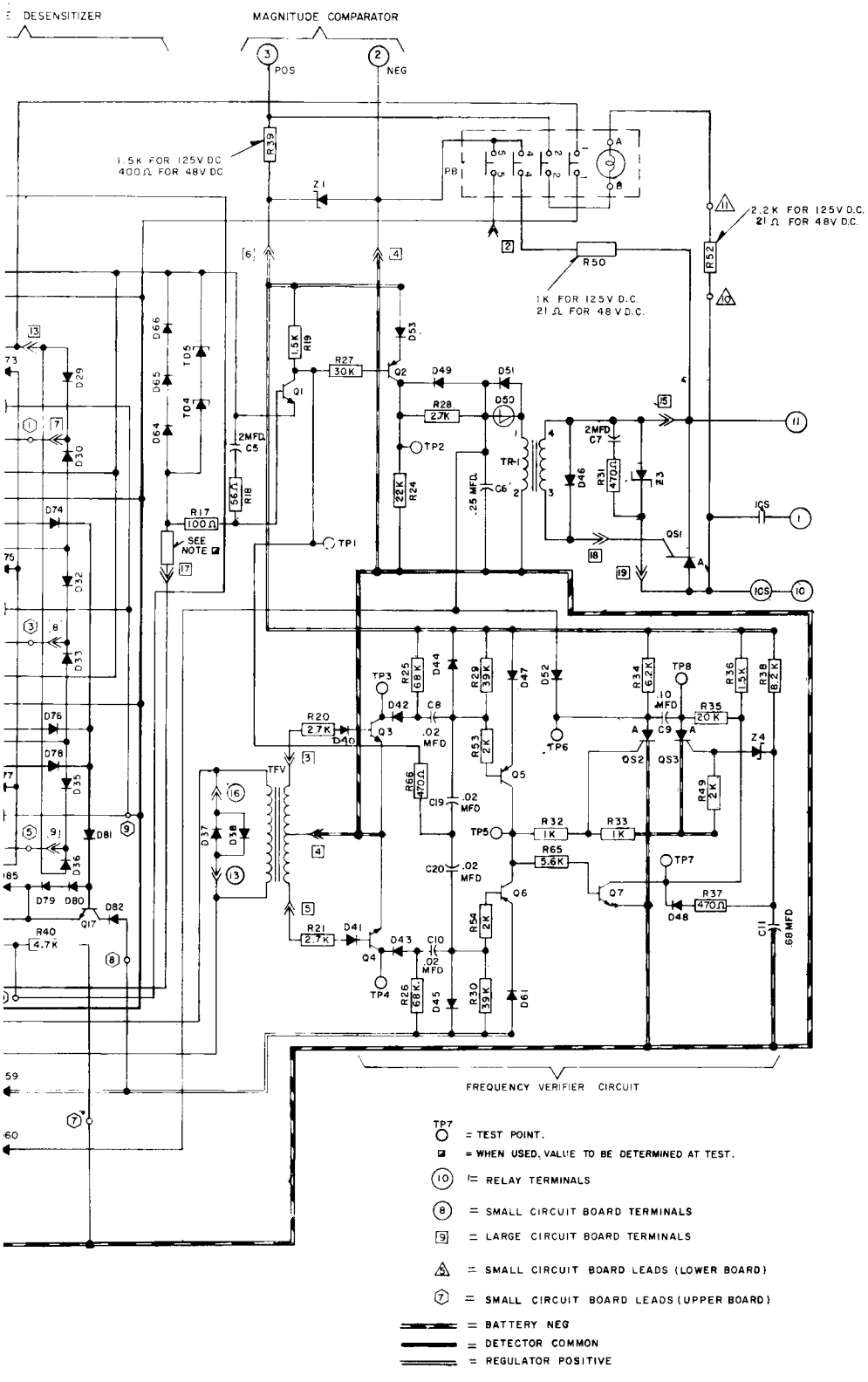


Fig. 9. Internal Schematic of the Type SDG-4 Relay in FT-42 Case



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Schematic of SDG Relay

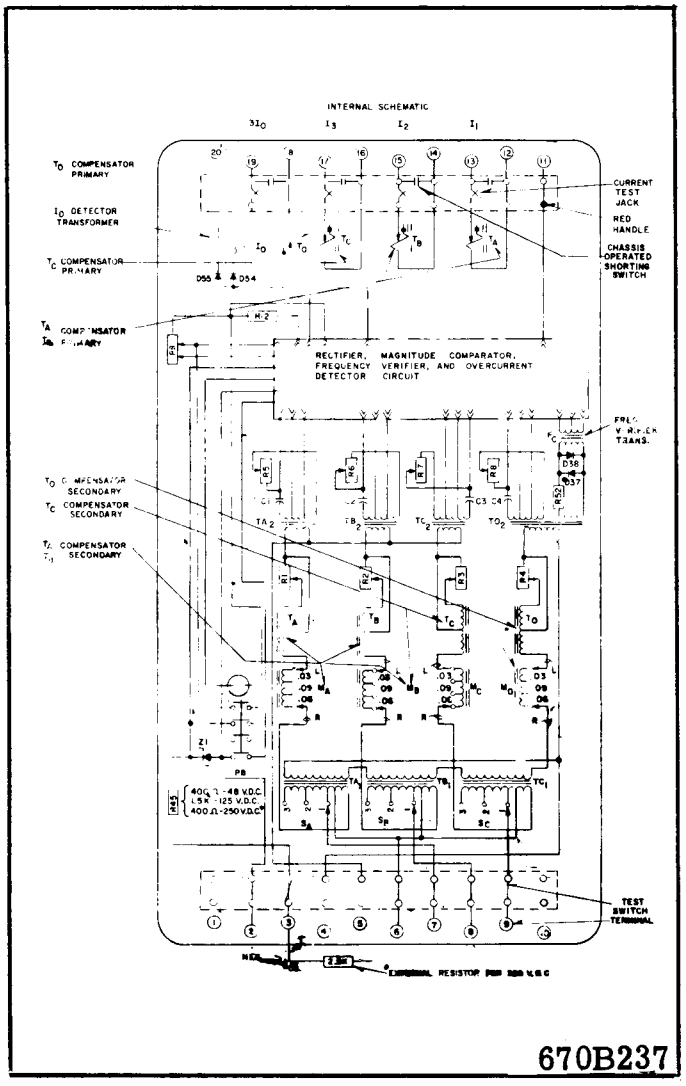


Fig. 6. Internal Schematic of the Type SDG-1 Relay in FT-42 Case

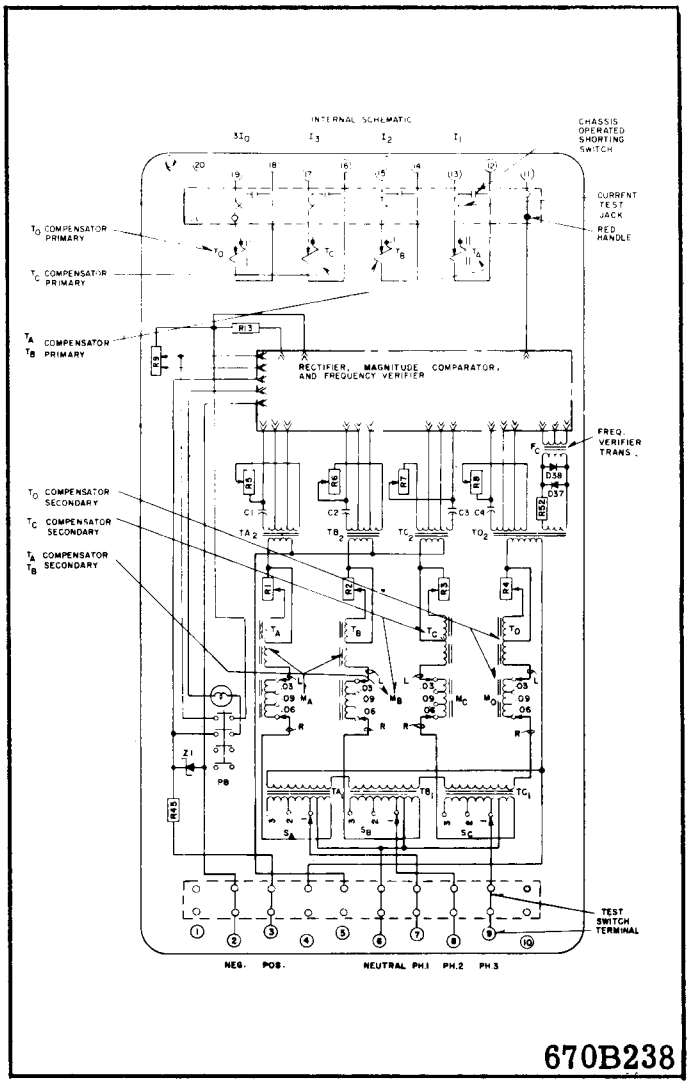


Fig. 7. Internal Schematic of the Type SDG-2 Relay in FT-42 Case

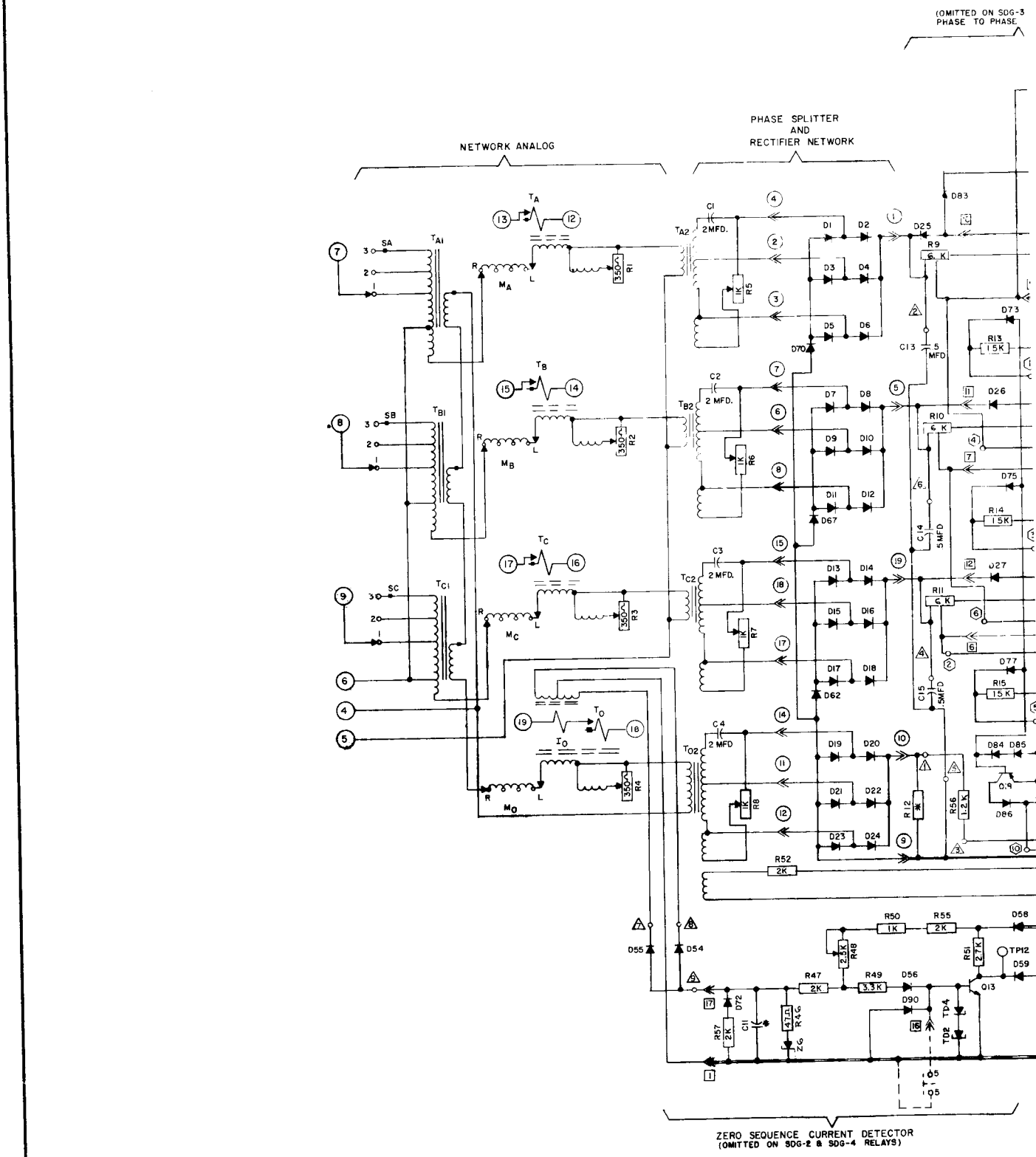


Fig. 10 Detailed Internal Schematic

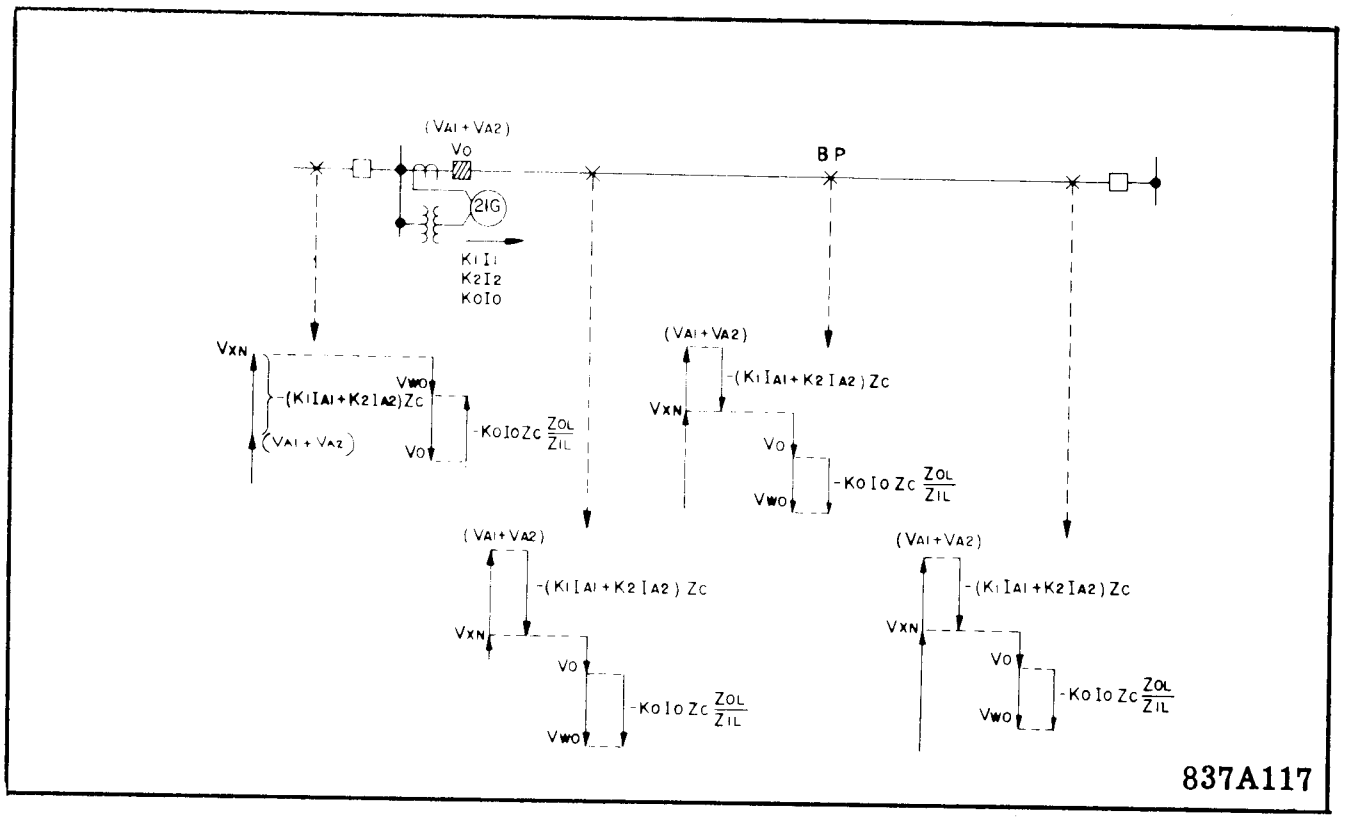


Fig. 14. Relay Voltages for A-to-Ground Faults at Selected Points

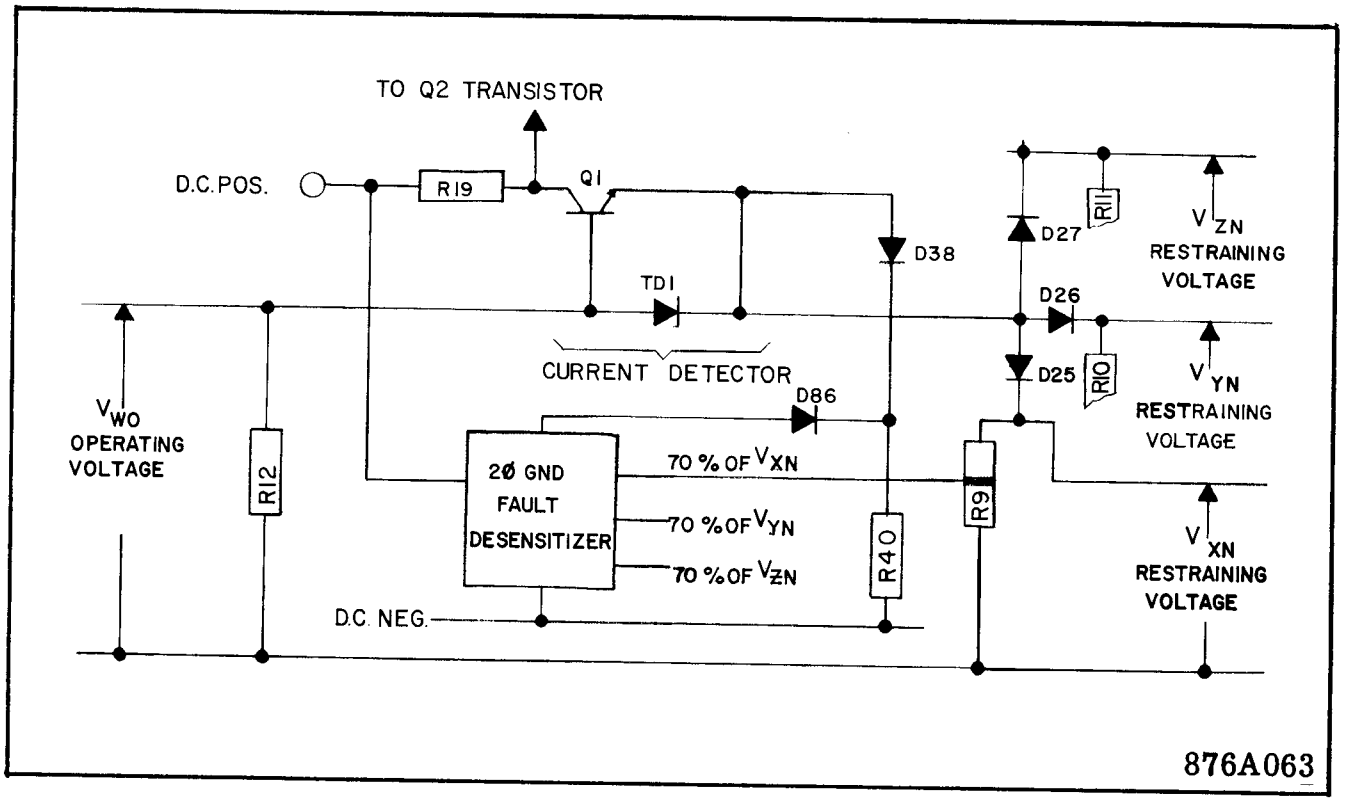
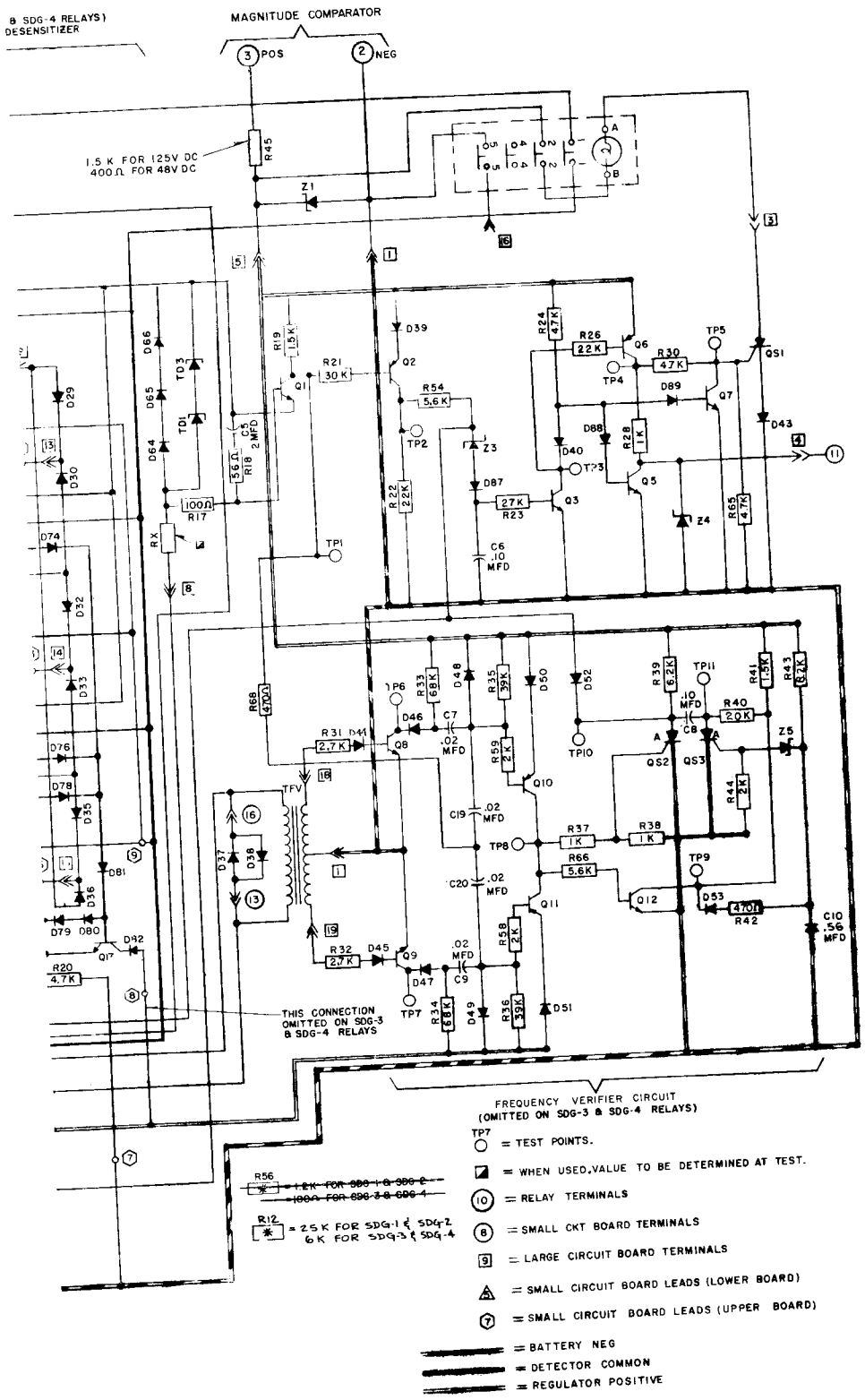


Fig. 15. Magnitude Comparator Circuit



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of the SDG-1, 2, 3, & 4 Relays

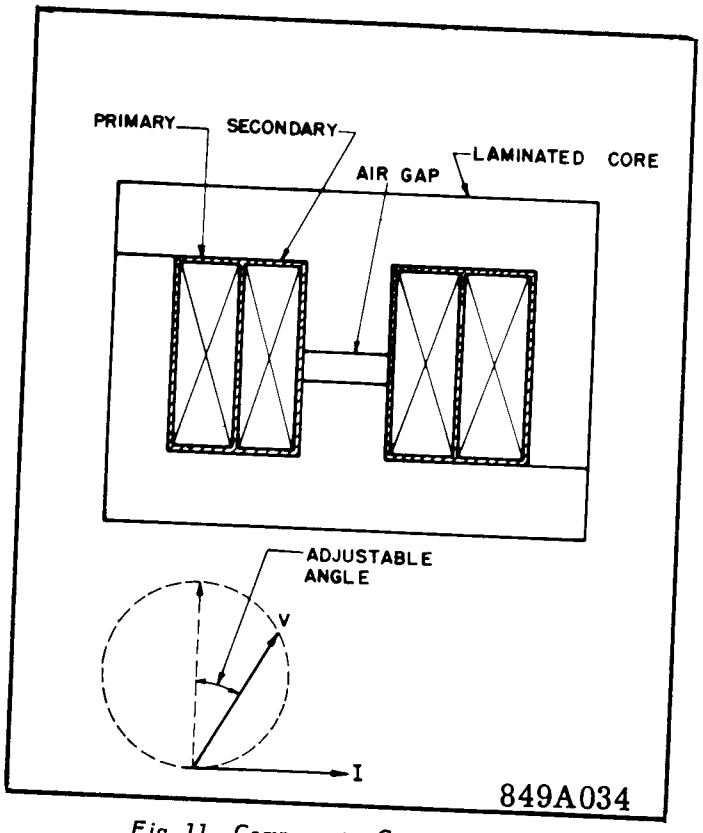


Fig. 11. Compensator Construction

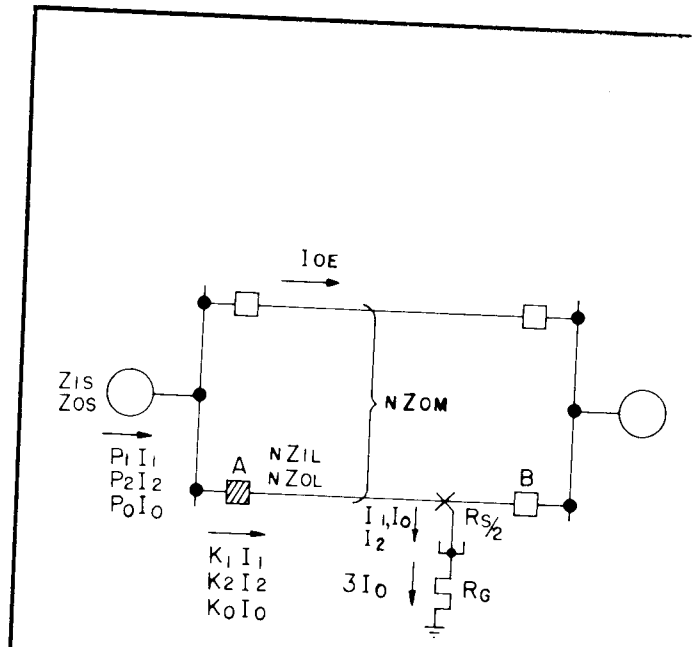


Fig. 12. Definition of Terms

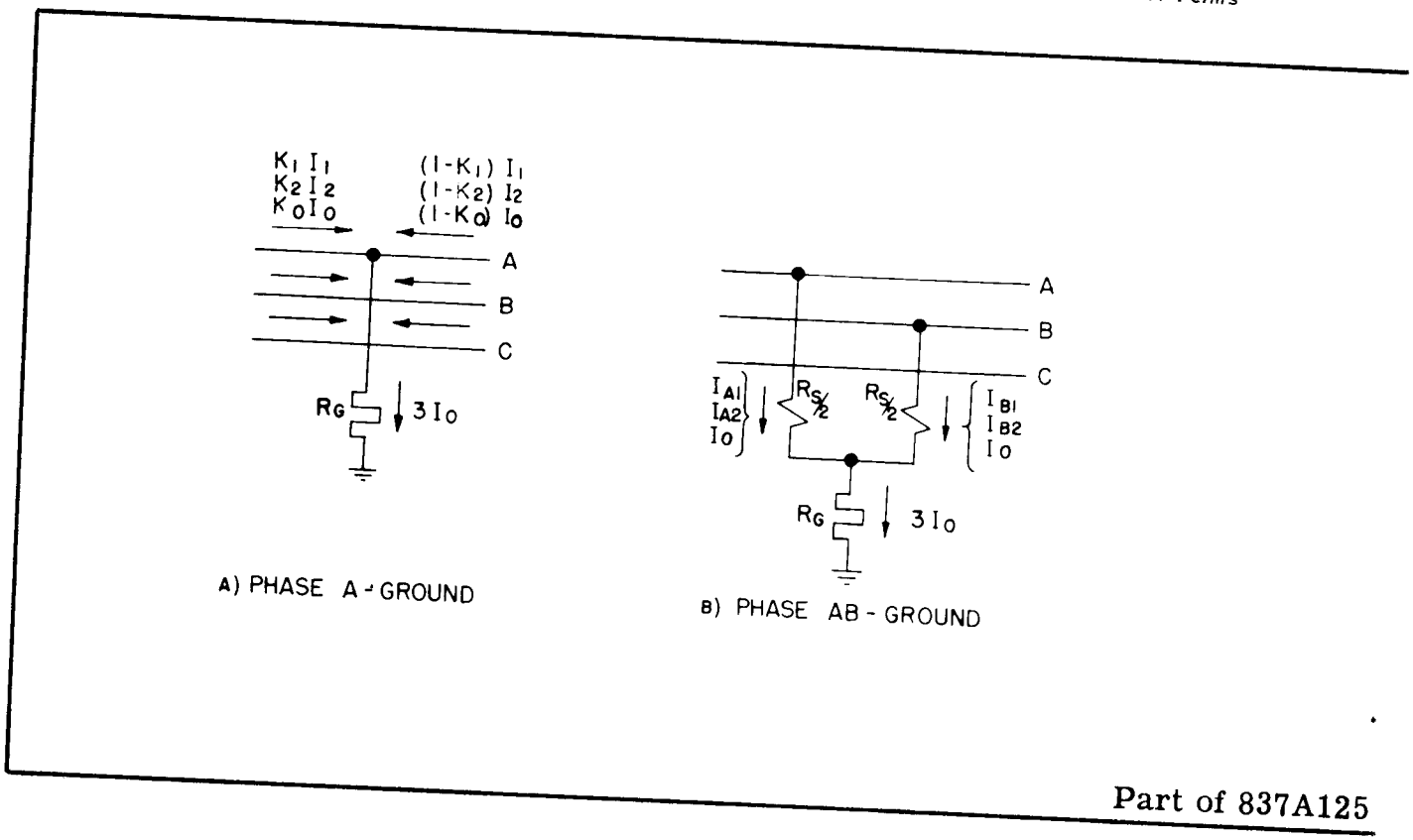


Fig. 13. Fault Resistance

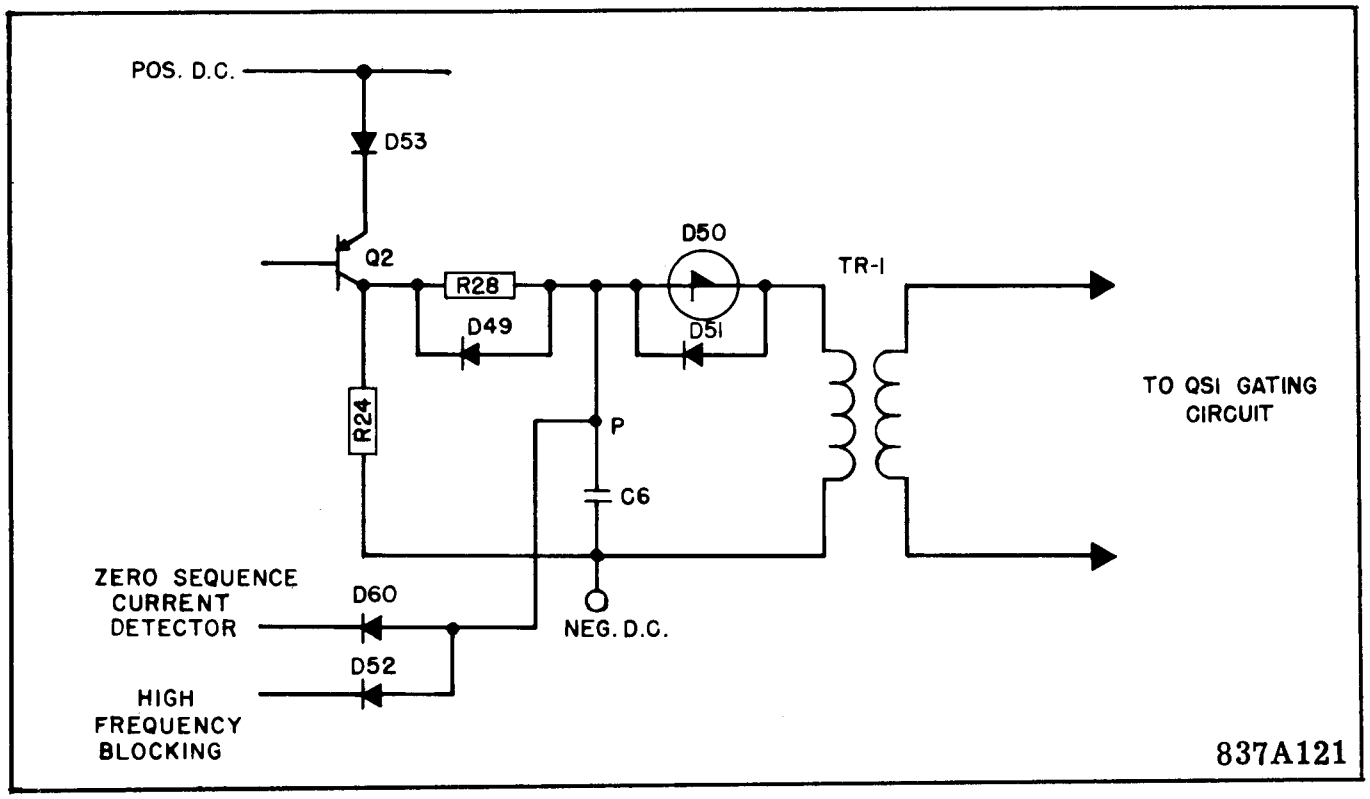


Fig. 16. Triggering Circuit

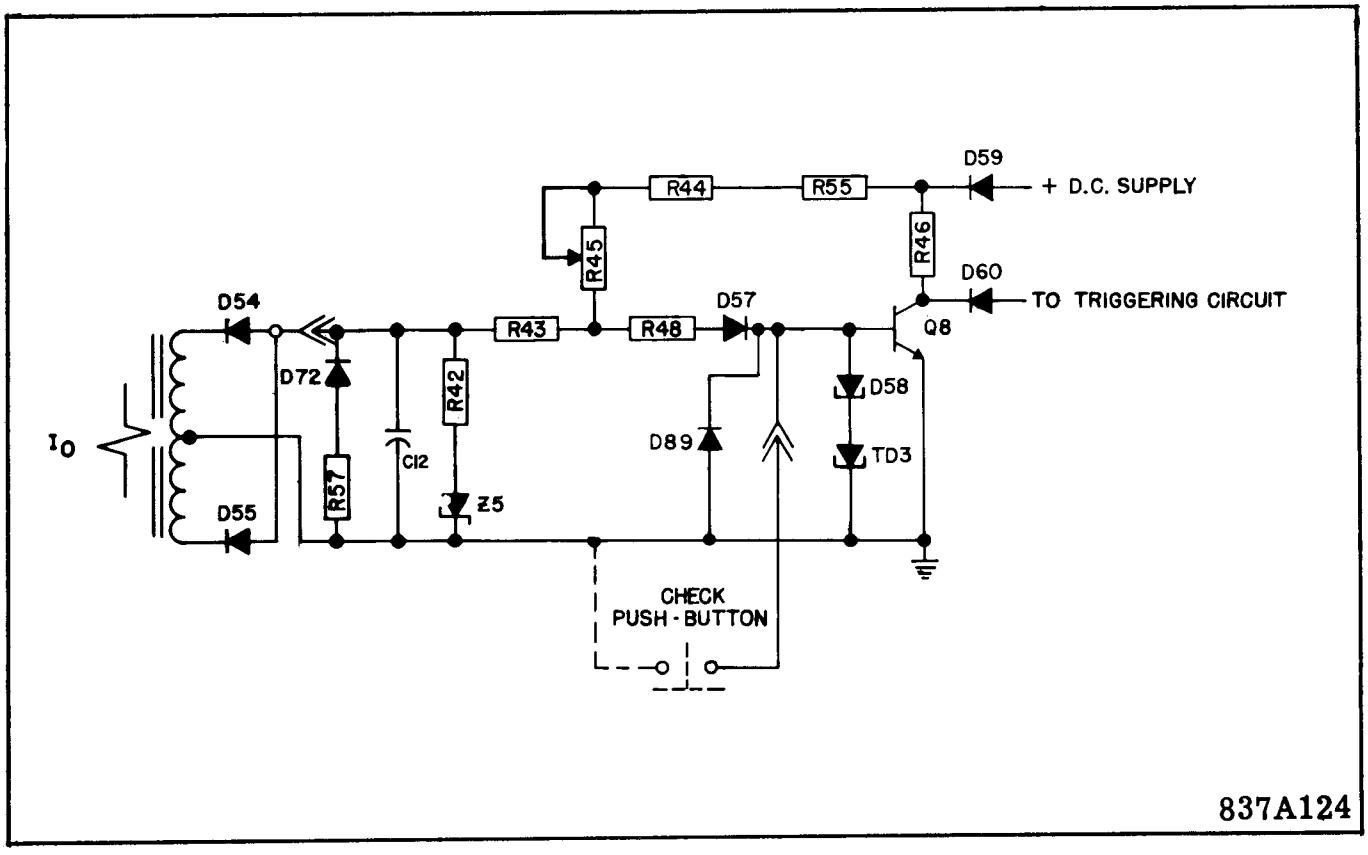


Fig. 17. Zero Sequence Current Detector Circuit

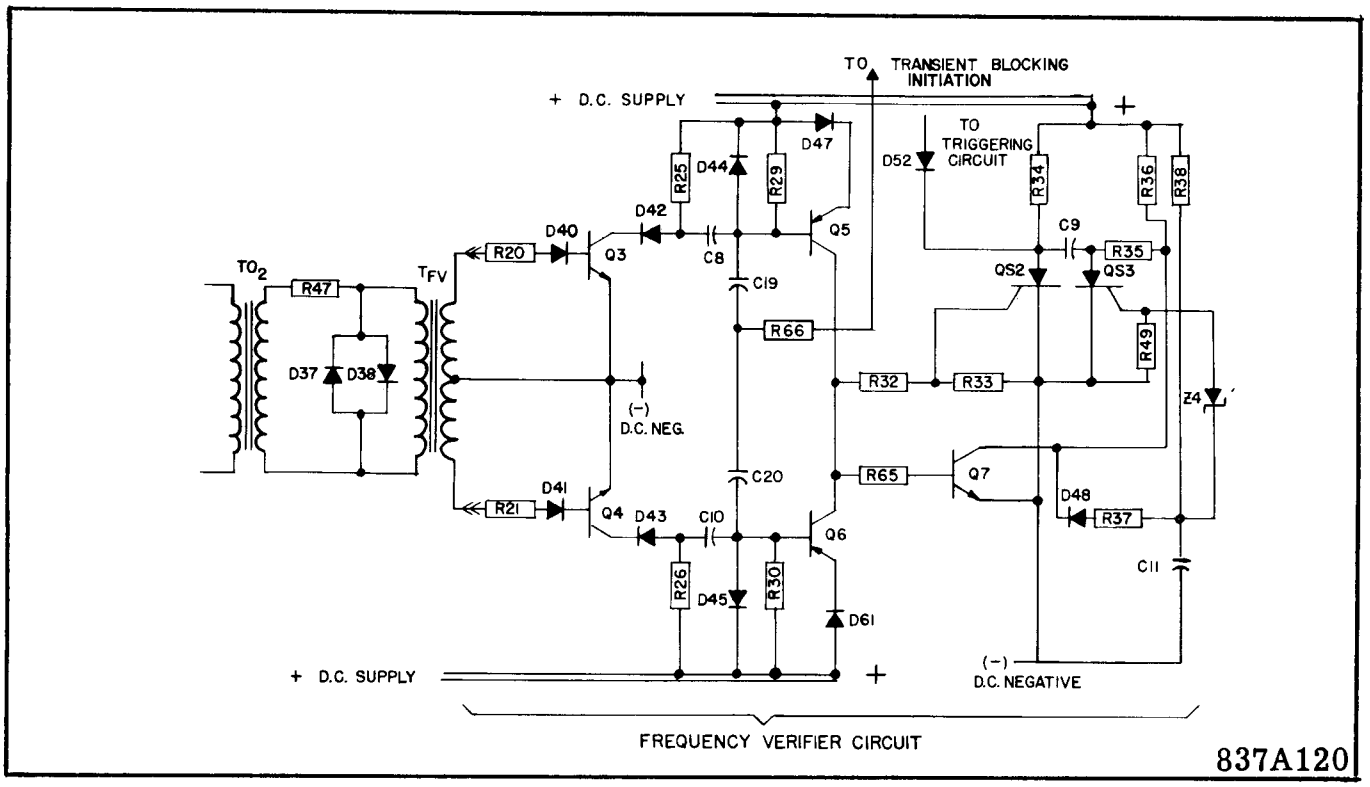


Fig. 18. Frequency Verifier Circuit

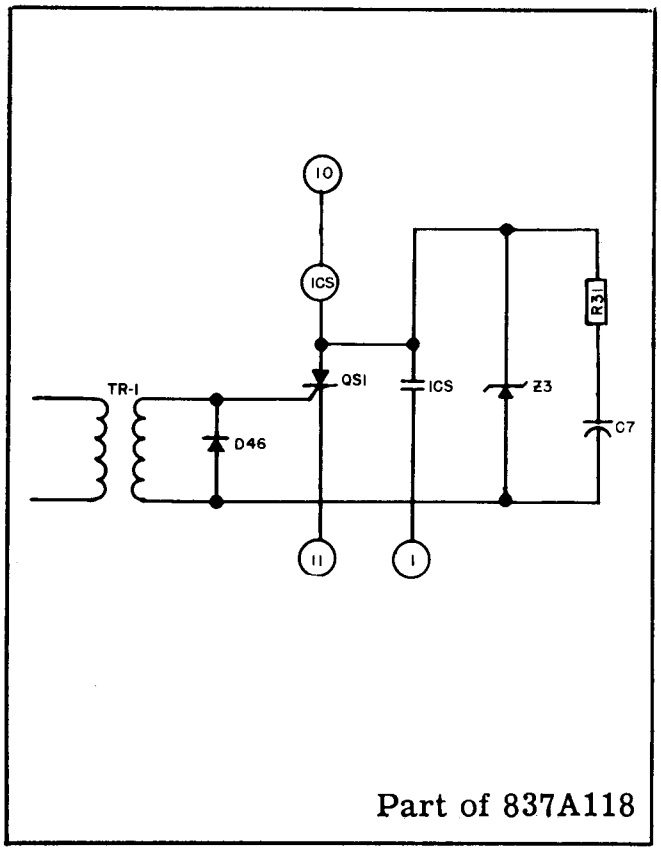


Fig. 19. Output Circuit of the SDG Relay

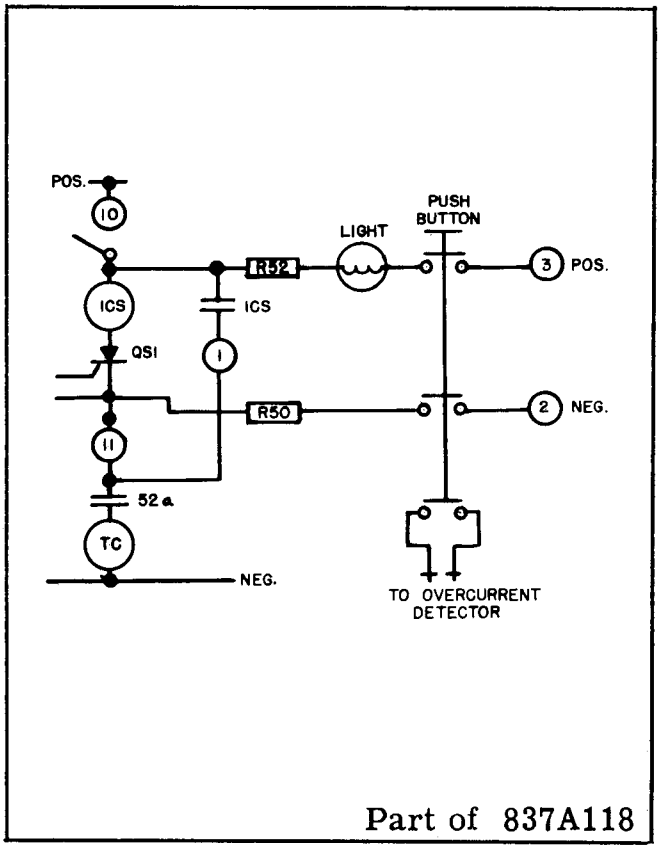


Fig. 20. Push Button "In Service Check" in the SDG Relay

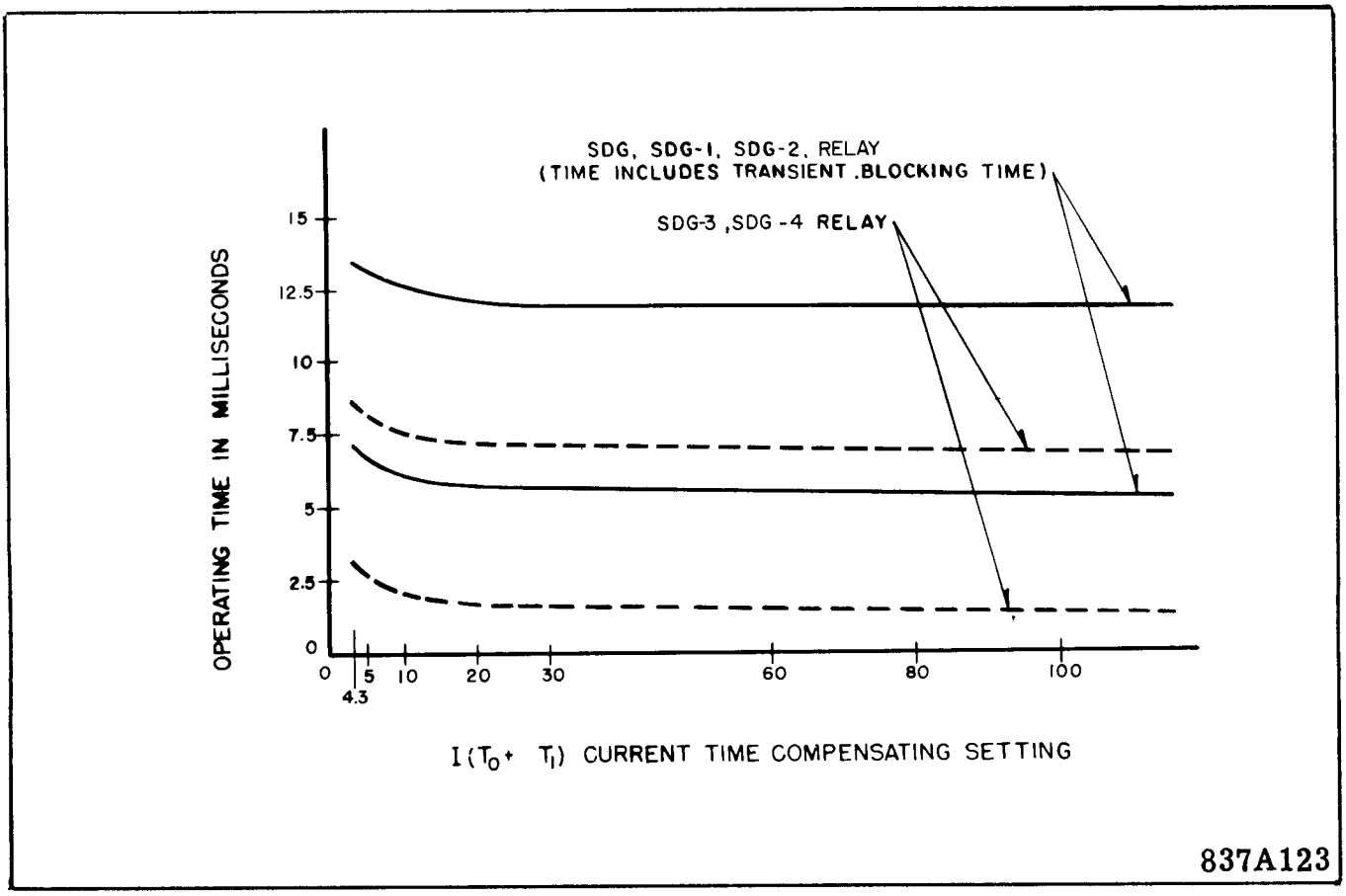


Fig. 21. Typical Operating Time Curves of the Type SDG-Line Relay

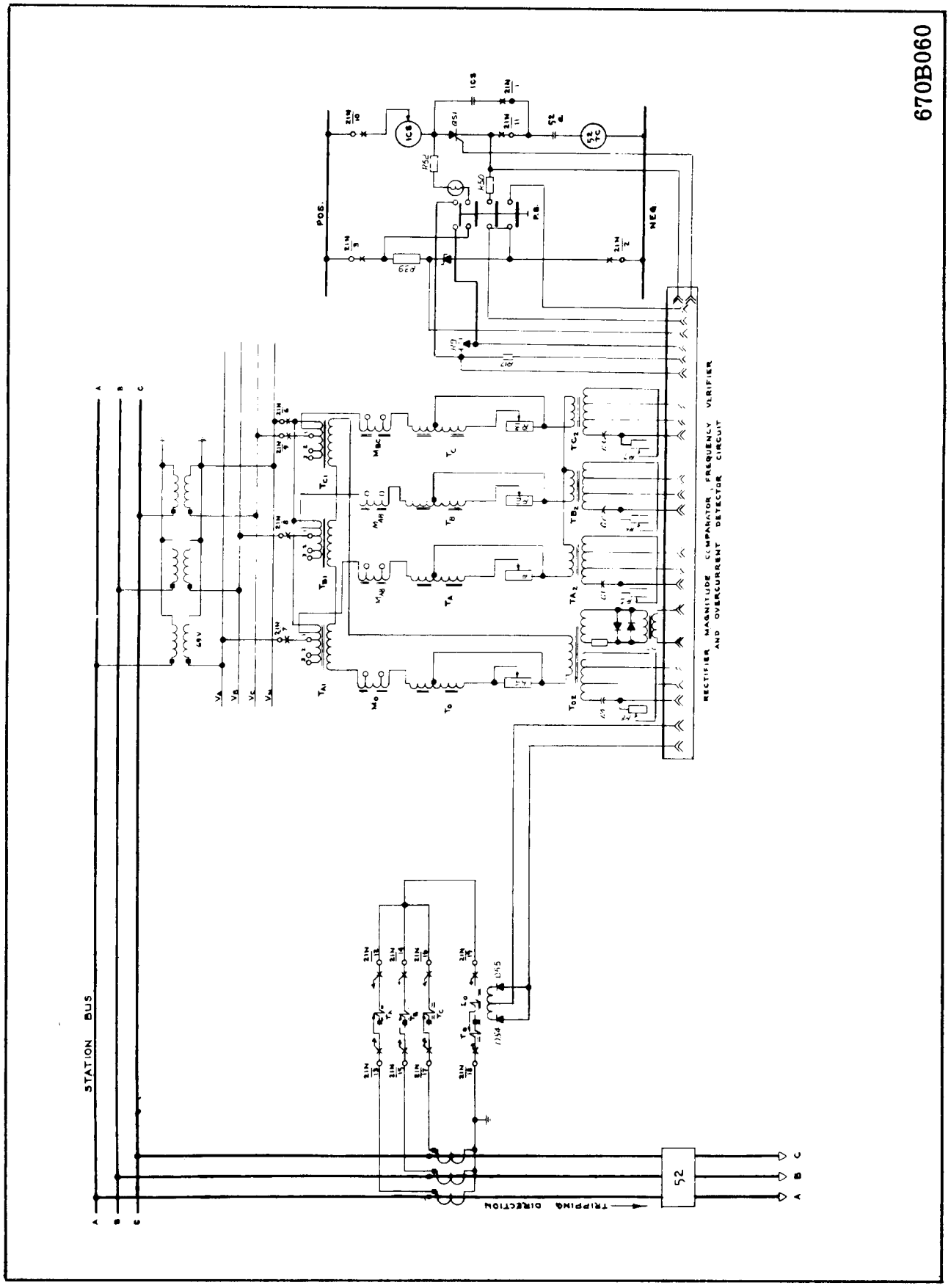
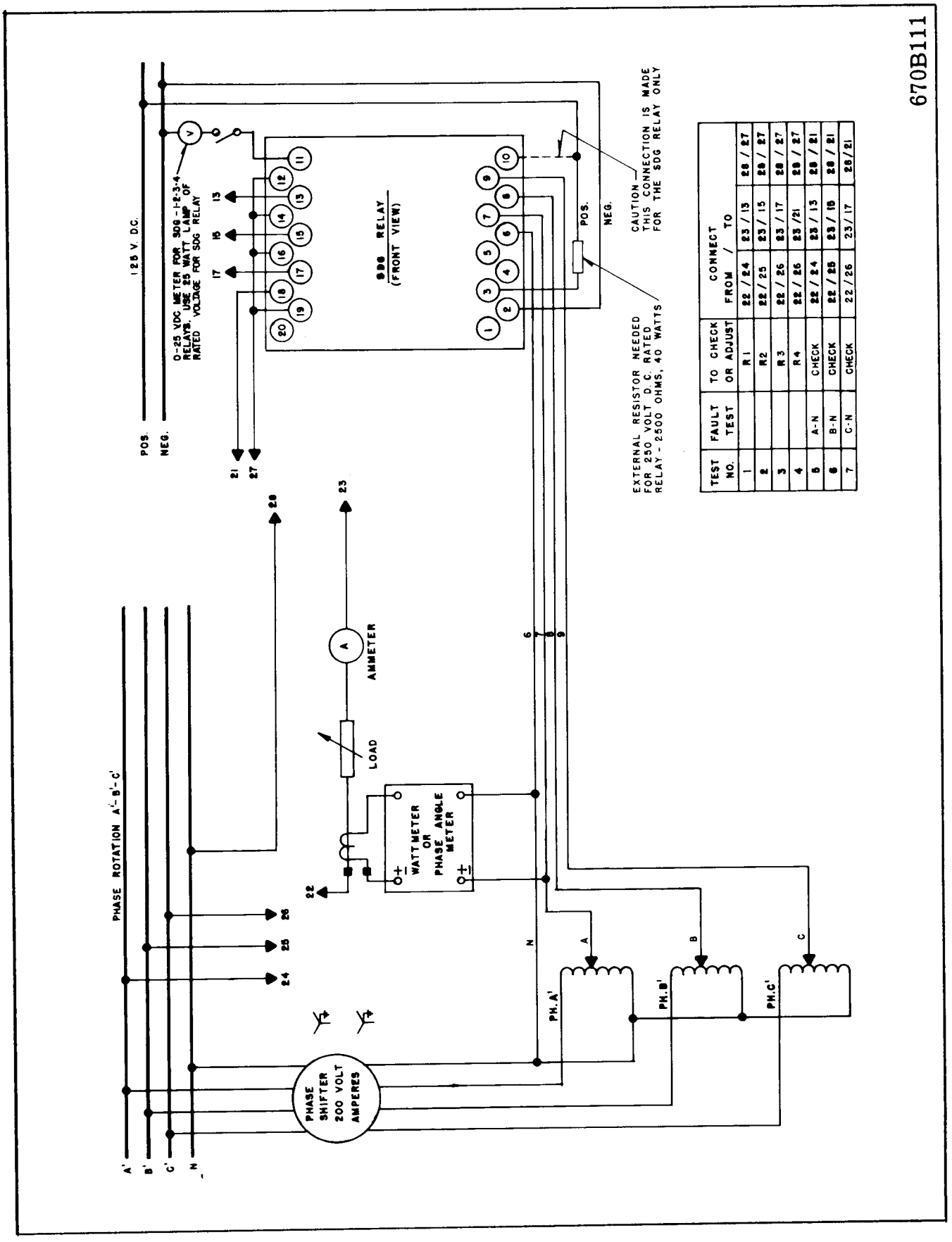
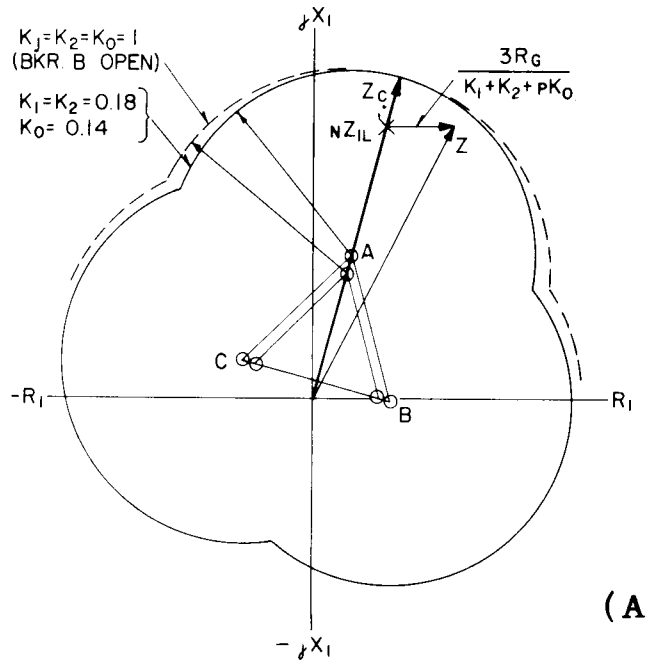


Fig. 22. External Connections for the SDG Relay



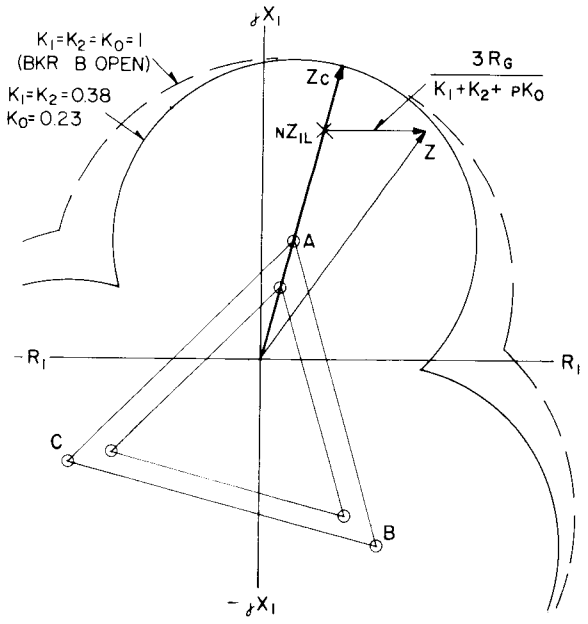
TEST NO.	FAULT TEST	TO CHECK OR ADJUST	CONNECT FROM	TO	
1		R1	22 / 24	23 / 13	28 / 27
2		R2	22 / 25	23 / 15	28 / 27
3		R3	22 / 26	23 / 17	28 / 27
4		R4	22 / 26	23 /21	28 / 27
5	A-N	CHECK	22 / 24	23 / 13	28 / 21
6	B-N	CHECK	22 / 25	23 / 19	28 / 21
7	C-N	CHECK	22 / 26	23 / 17	28/21

Fig. 23. Test Connections for the SDG Line Relays



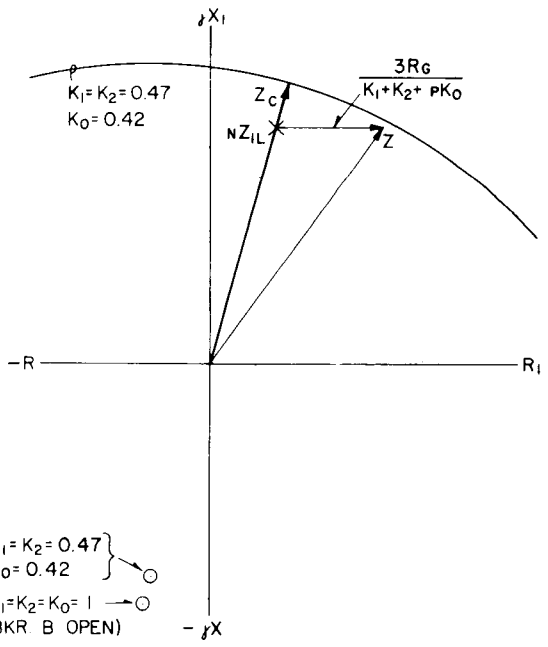
(A) 837A116

a) Long Line



(B) 837A114

b) Medium-length Line



(C) 837A115

c) Short Line

Fig. 24. Impedance Circles for the SDG Line Relays

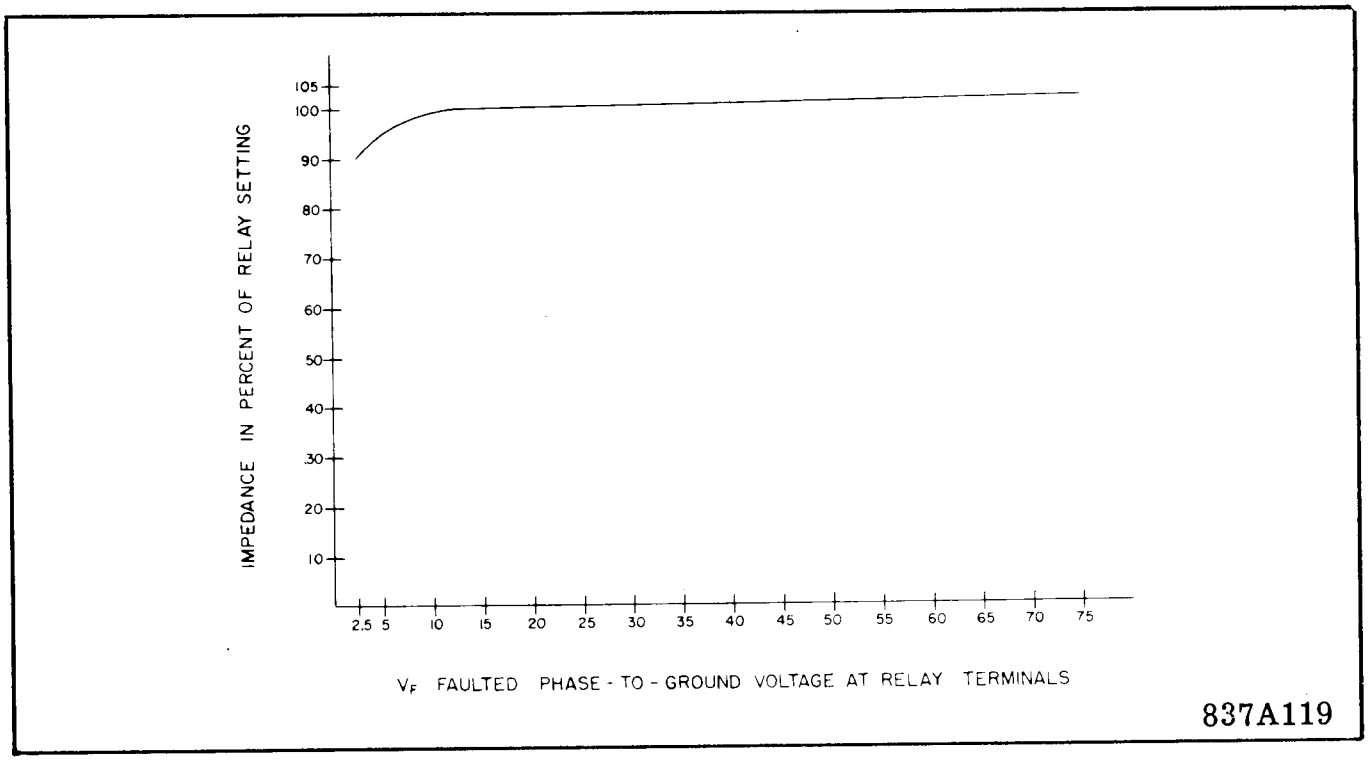


Fig. 25. Impedance Curve for the SDG Line Relays

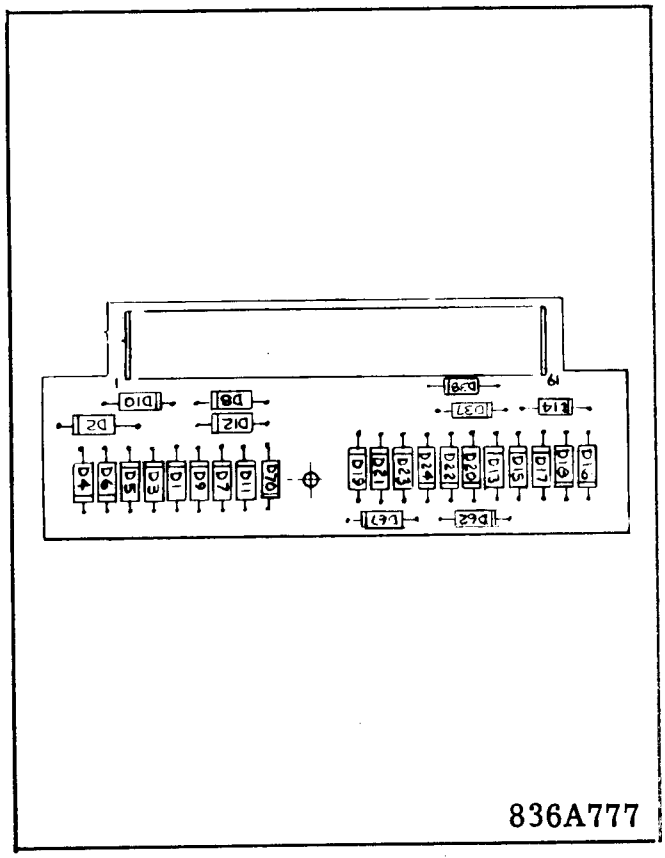


Fig. 26. Printed Circuit Board Assembly for SDG, SDG-1, 2, 3, & 4 Relays

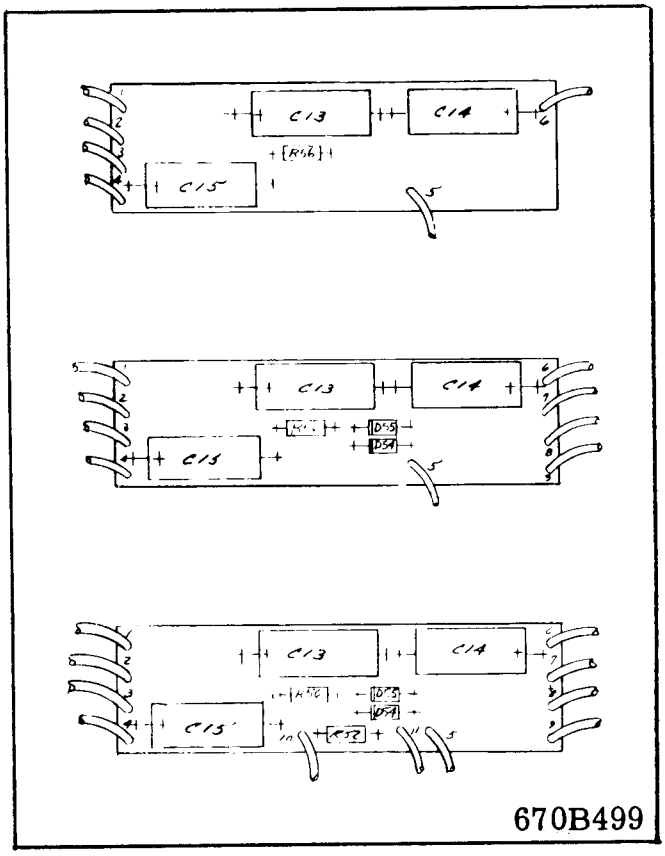


Fig. 27. Printed Circuit Board Assembly for SDG, SDG-1, 2, 3, & 4 Relays

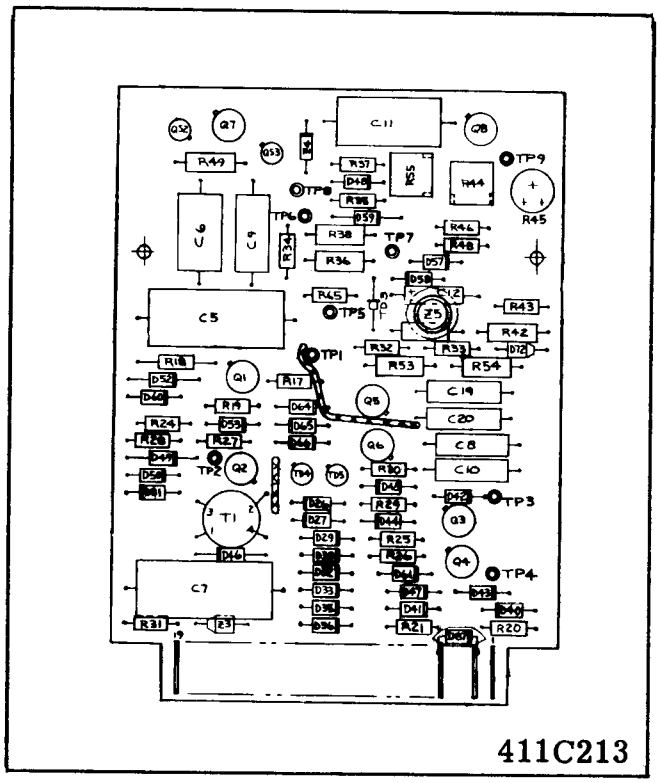


Fig. 28. Printed Circuit Board Assembly for SDG Relay

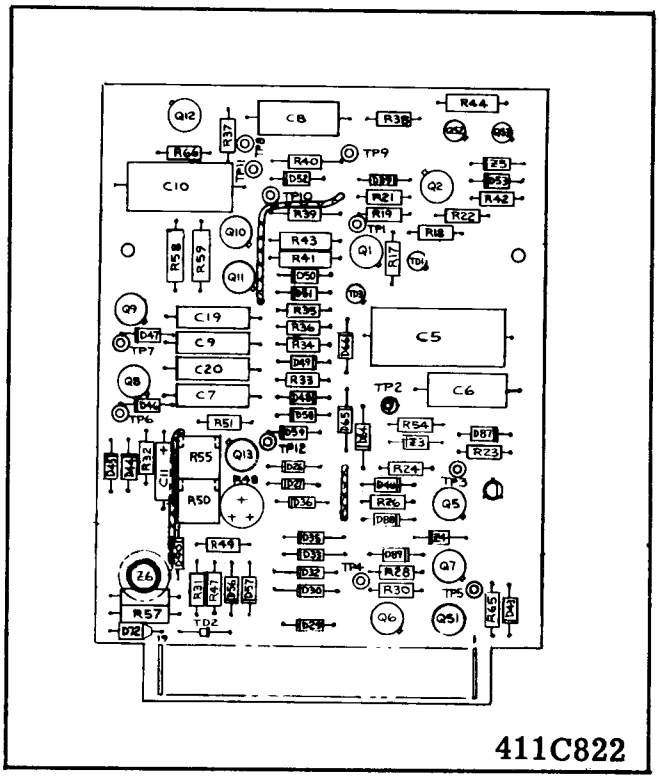


Fig. 29. Printed Circuit Board Assembly for SDG-1 Relay

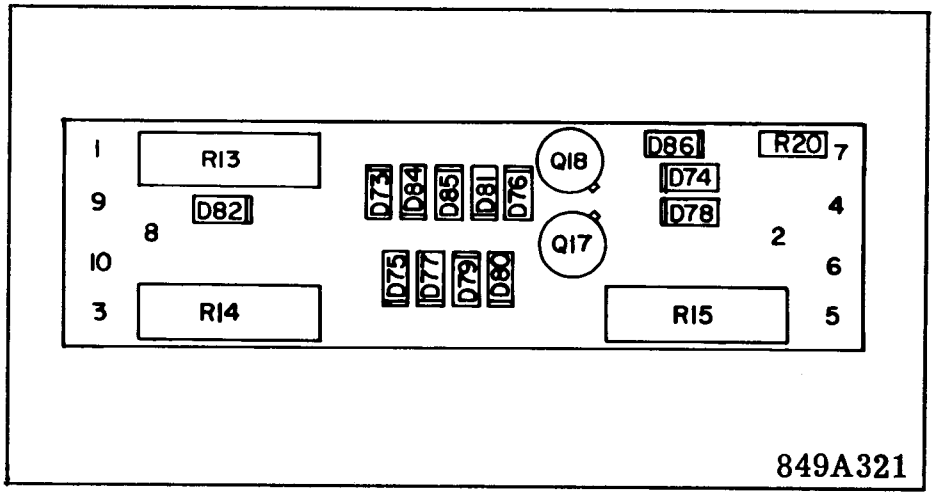


Fig. 29A. Printed Circuit Board Assembly for SDG1, 2, 3 and 4 Relays.

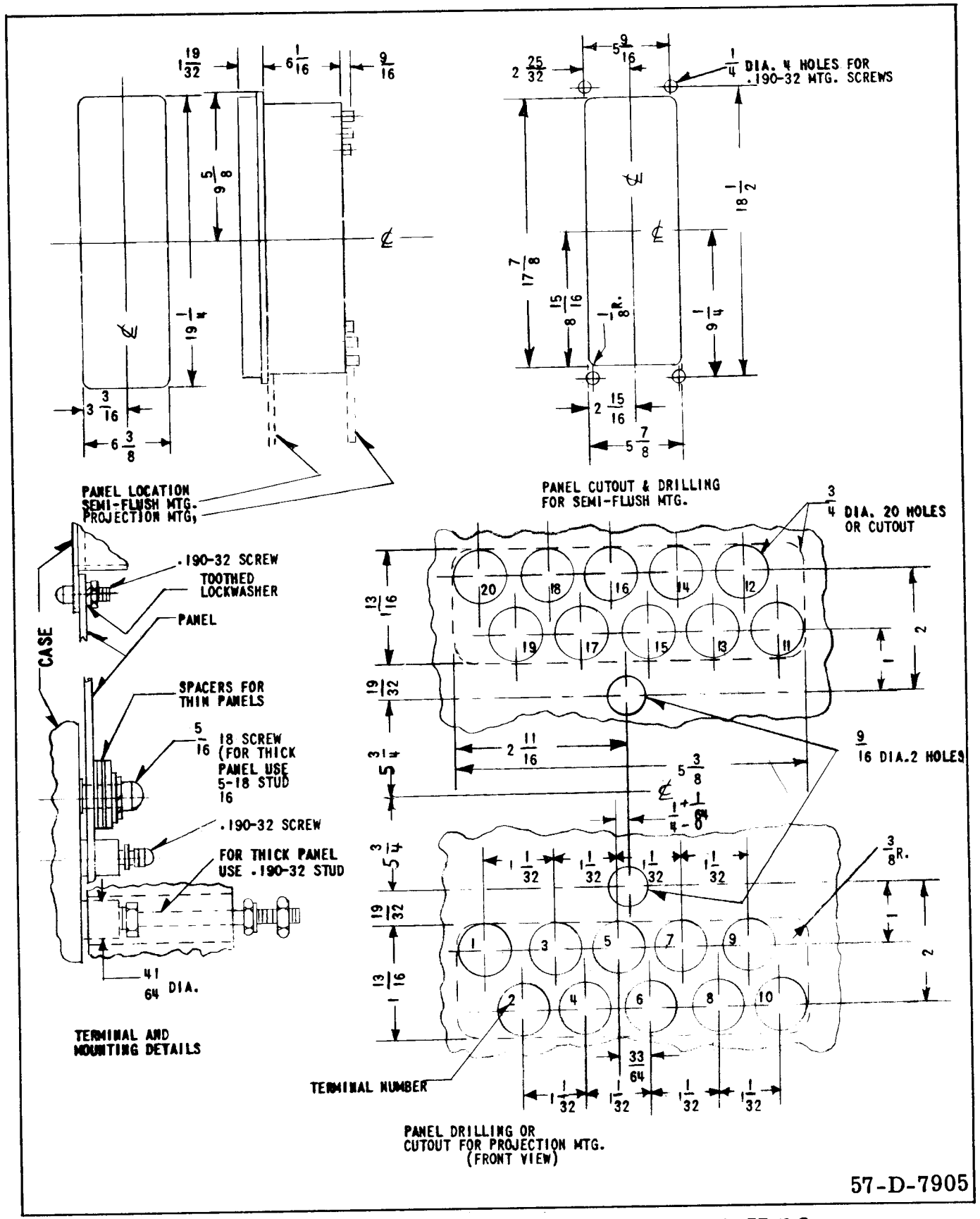


Fig. 30. Outline and Drilling Plan for the Type SDG Line Relays in the FT-42 Case

APPENDIX I

MUTUAL IMPEDANCE EFFECT

Where mutual compensation is desired, a type IK auxiliary current transformer (Fig. 32) maybe used with a step down current ratio of $\left|\frac{Z_{OM}}{Z_{OL}}\right| = C^1$ Z_{OM} is the zero sequence mutual impedance and Z_{OL} is the zero sequence self impedance of the line. Zone 1 maybe set to cover 85% of the line.

The "parallel line" leads on the IK-transformer are set for factor C^1, as defined above. These leads are set so that the difference between the taps is nearest to the desired C^1-value.

The external terminals of the IK-transformer numbered 3 and 4 are connected across the SDG-relay terminals 19 and 18 as shown in the external schematic figure 22. The external terminals 5 and 6 are connected in series with the residual CT circuit of the parallel line.

The IK transformer is set as outlined below. Before the proper tap settings are made, the cover of the transformer should be completely open. Complete opening of the cover assures continuity in the residual current transformer circuits and isolates the IK transformer windings from the residual circuits.

The taps are set so that difference between the two taps is equal to the desired setting of C^1. For instance, C^1 setting equal to 8, is set as follows:

Connect leads coming out of opening marked "parallel line" Fig. 32 to the terminals marked "C^1". Black lead (which is of the same polarity as the plus marked external terminal) is connected to terminal marked ".2" and the white lead to the terminal marked "1.0". The difference between the two taps 1.0 − .2 = .8, is the desired "C^1" setting. Physically, this is done as follows:

Remove the top nut from the desired terminal, place the lug of the proper lead on the terminal and replace the locking nut. Make sure that nut holds the lug snugly against the terminal to avoid the possibility of developing a loose or high resistance connection.

The leads coming out of opening marked "protective relay" and "protected line" are connected to the terminals "0" and "1.0" in the row marked "C" observing the same polarity marking as above. This connection is the same for all "C^1" values less or equal to 1.

After the setting is completed the cover should be closed to restore the connection between the transformer winding and the external terminals.

General Considerations

In considering mutual zero-sequence impedance effects it is well to consider that the mutual impedance works to reduce fault-current level when the currents flow in the same direction in the coupled lines. The converse is true when the currents flow in opposite directions. For example, in Fig. 33(a), the currents are flowing in the same direction from the left, causing the relay at A to underreach. If, however, $|Z_{OS}| > > |Z_{OU}|$ then for a balance point fault (e.g. 85% from A to B), the current I_{OM} reverses as in Fig. 33(b). Here the fault current K_0I_0 is larger than for a similar situation except with $Z_{OM} = 0$; so a relay set for 85% of the line actually reaches farther due to mutual effects assuming no mutual compensation. Of course, as the fault moves closer to B, a point is reached where I_{OM} reverses, so that relay A will never overreach to see a bus fault at B.

If mutual compensation is used in Fig. 33(b) for relay A, it will have the undesirable effect of reducing the operating current and hence the reach. We see then, that mutual compensation eliminates the undesirable effect of mutual impedance if, and only if, both K_0I_0 and I_{OM} are flowing from the local bus into the lines.

For the usual case of Fig. 33(a) mutual compensation may be used to maintain zone 1 reach at 85% of the line regardless of whether the adjacent line is in or not. Without compensation, if the relay is set for 85% of the zero-sequence self-impedance, it will cover at least 70% (but less than 85% except for the Fig. 33(b) case) of the line with the adjacent line closed. Two things work to minimize the underreach: first, as the fault moves closer to bkr. A, I_{OM} decreases and K_0I_0 increases; secondly, as the fault moves within the balance point, the restraint voltages are overcompensated, reducing the restraint. The amount of underreach varies with system impedances, but one can expect to cover at least 70% of the line, with an 85% nominal setting.

Mutual compensation of zone 2 is of more value: 1) Since I_{OM} is flowing in the same direction as K_0I_0 for the entire length for end-zone faults, and 2) we need to make sure of 100% protected line coverage.

We have already seen in Fig. 33(b) that mutual compensation is not always efficacious; we must also consider the adjacent-line faults of Fig. 34. In Fig. 34(a) we can be greatly overcompensated so that relay A operates due to the compensation current $I_{OM}(\frac{Z_{OM}}{Z_{OL}})$. The SCC relay will minimize the possibility of SDG-line overreach for the case in Fig. 34(b).

In Fig. 34(c) bkr. C is open so that the same conditions exist for relay A whether or not mutual compensation is used. In this case, adjacent line current flows in the opposite direction to that of K_0I_0 for the entire length. The zone-1-relay phase compensation at bkr. A is less than half of the proper amount to reach the fault, but the ground compensation may be in excess of the apparent zero-sequence impedance to the fault. The worst case occurs when there is no current source at U. Fortunately, zone 1 at A cannot overreach; however, zone 2 at A can see this fault if source U is weak. Fortunately zone 1 at D will also see the fault so bkr. A zone 2 need not be delayed to coordinate with bkr. D-zone 2.

Note in both Fig. 34(b) and (c) that the system condition which can cause trouble with relays A and C is a poor source at U. This is also the condition yielding the greatest zone 1 underreach for protected line faults.

As mentioned earlier we can get at least 70% zone 1 coverage without mutual compensation. The advantages of tolerating a reduced reach with the parallel line in service (vs. 85% coverage with mutual compensation) are:

1. Type SCC current comparer not required.
2. No overreach tendencies for adjacent line faults-(Fig. 34(b))
3. Simplified current circuit (where we have zone 1 only).

Zone 2 should definitely be mutually compensated unless the mutual impedance effects are negligible. The SCC current comparer need not be applied for zone 2 supervision even though the zone 2 relay at A will operate for close-in faults (Fig. 34(a) since bkr. C is opened at high speed. In rare cases, after bkr. C opens (Fig. 34(c), zone 2 at A will remain operated (poor source at U), requiring time coordination with zone 2 at D.

Type SCC Current Comparer

The SCC relay prevents the SDG relay types from tripping for close-in adjacent line faults, where the mutual compensating current may reach many times the protected line current, as in Fig. 35(a). It is a static magnitude-comparison circuit. It operates on protected line current K_0I_0 and restrains on $0.4\left|K_0I_0 - dI_{OM}\right| = 0.4\left|K_0I_0 - \frac{Z_{OM}}{Z_{OL}} I_{OM}\right|$. That is, it restrains on the difference between the protected line current and the mutual compensation current.

Fig. 35 illustrates the SCC relay operation for various conditions. It is in balance in Fig. 35(b). In Figs. 35(c), (d) and (e) it operates to permit distance relay trip.

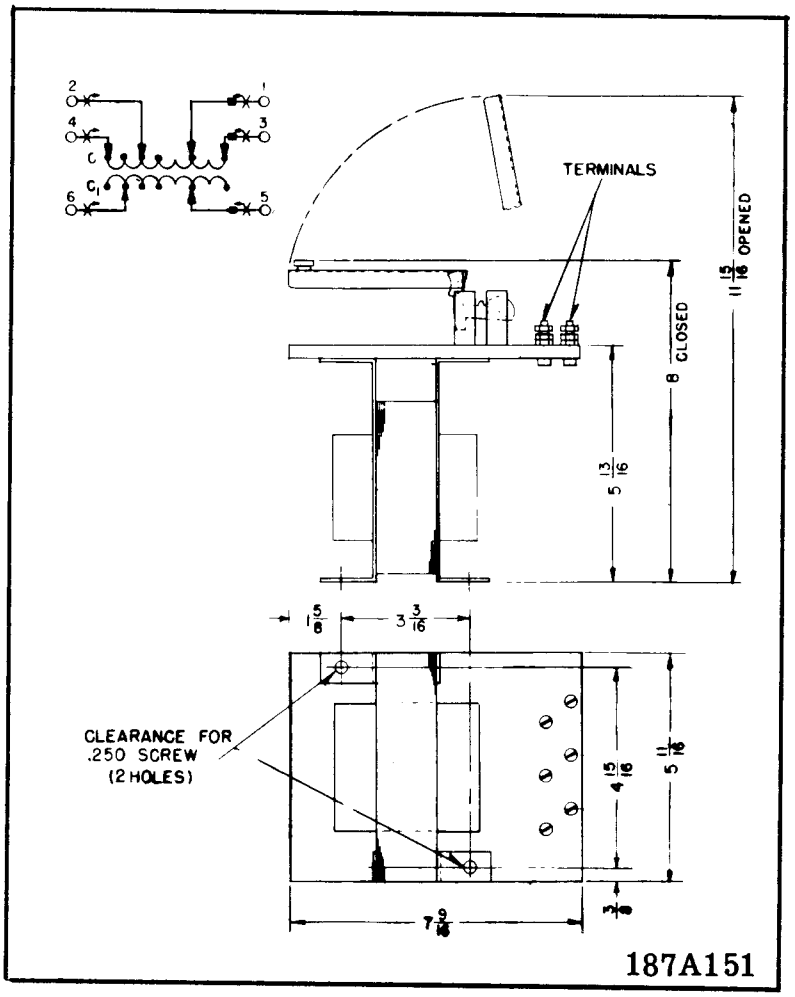


Fig. 31. Outline and Drilling Plan for the Type IK Transformer

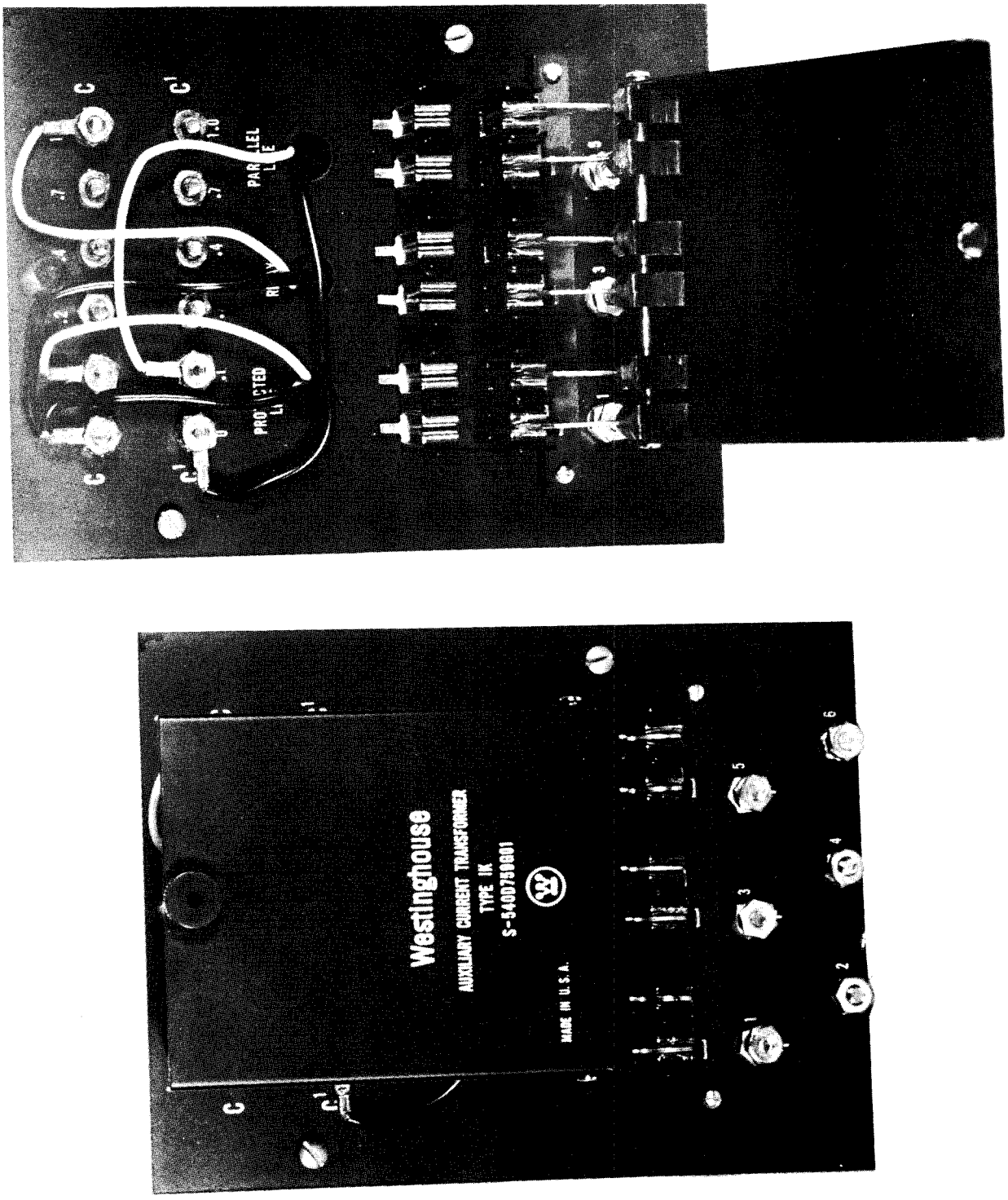
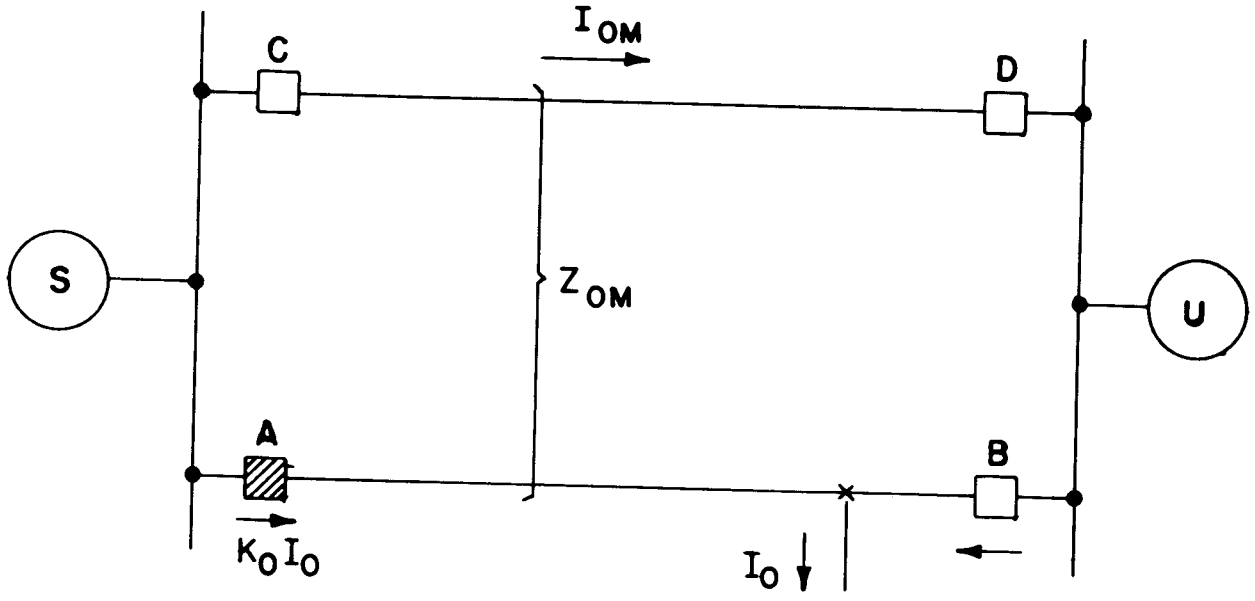
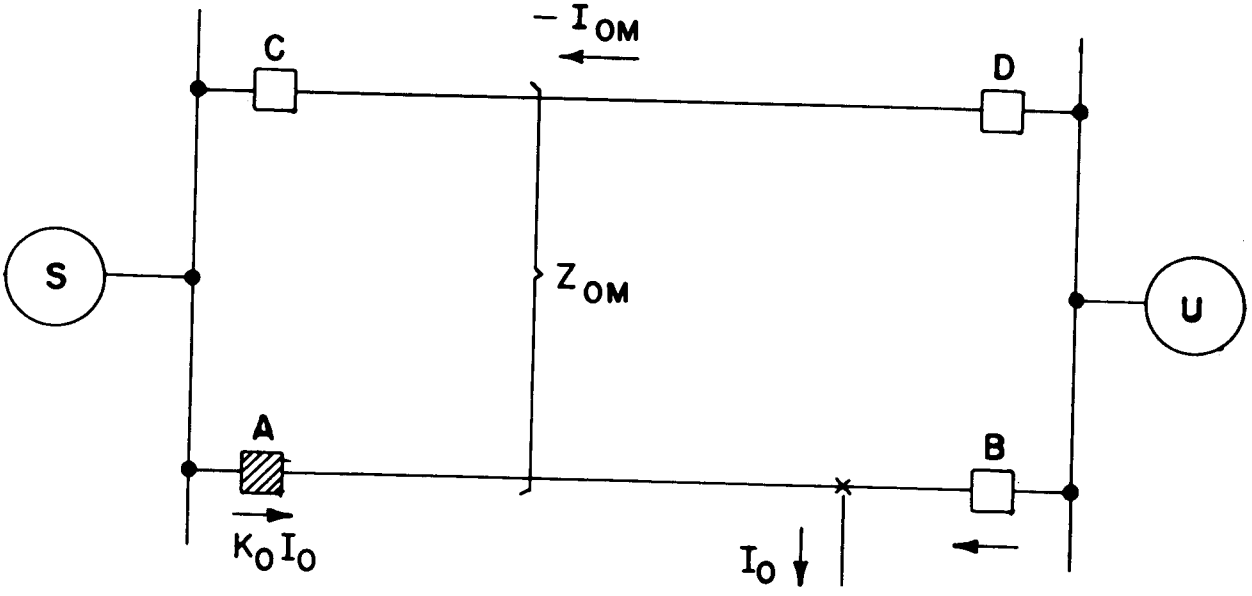


Fig. 32. Type IK Transformer



a) Mutual compensation helpful



b) Mutual compensation harmful ($|Z_{os}| >> |Z_{ou}|$)

Fig. 33. Zero-Sequence Currents for Zone 1 Balance-Point Fault With Mutual Coupling

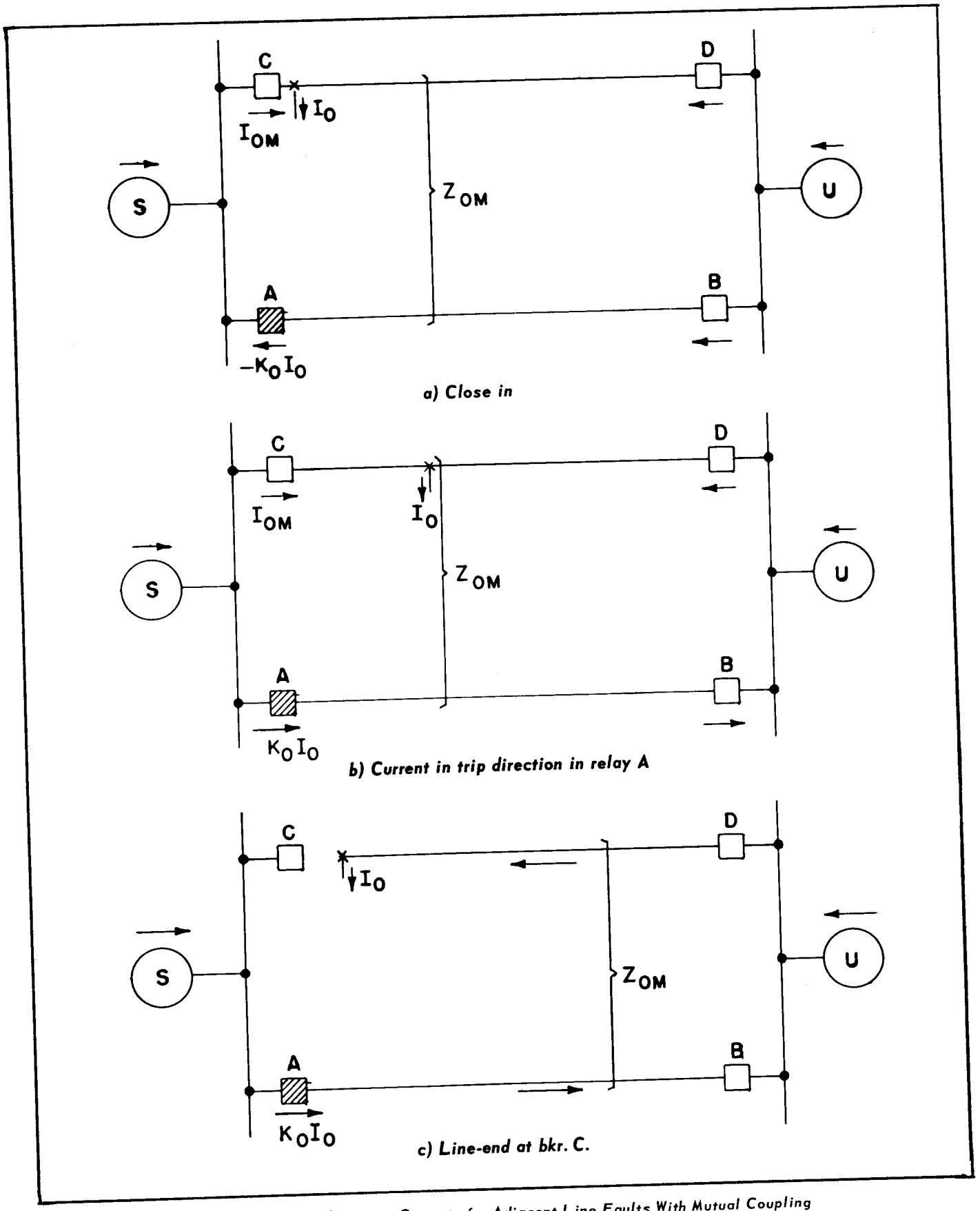
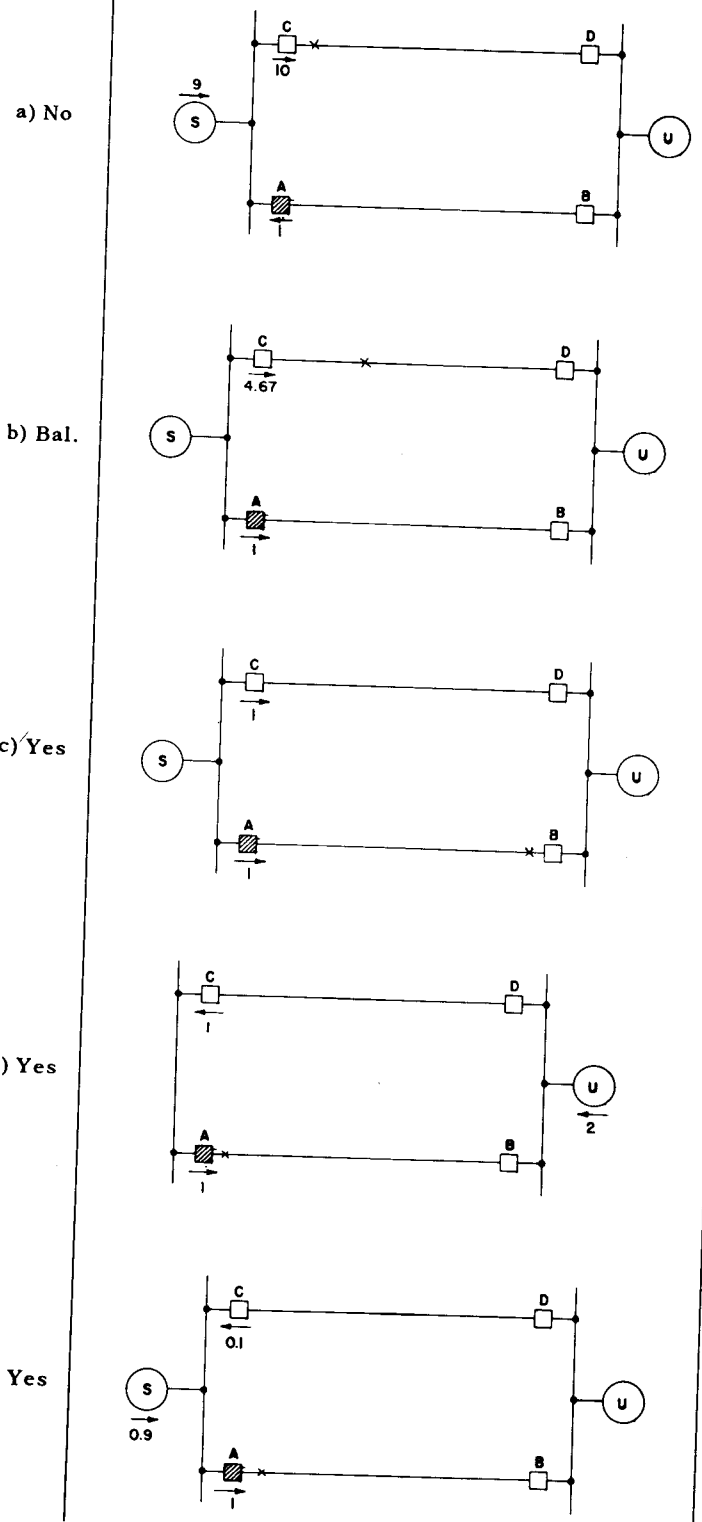


Fig. 34. Zero-Sequence Currents for Adjacent-Line Faults With Mutual Coupling



SCC OPER.	K_oI_o	$0.75\,I_{om}$	$0.4\,\lvert K_oI_o - 0.75\,I_{om}\rvert$
a) No	−1	7.5	3.4
b) Bal.	1	3.5	1.0
c) Yes	1	0.75	0.1
d) Yes	1	−0.75	0.7
e) Yes	1	−0.08	0.43

Fig. 35. Type SCC Relay Operation