INSTALLATION • OPERATION • MAINTENANCE

INSTRUCTIONS

Model 67 TEST
Manual Test Module

DESCRIPTION

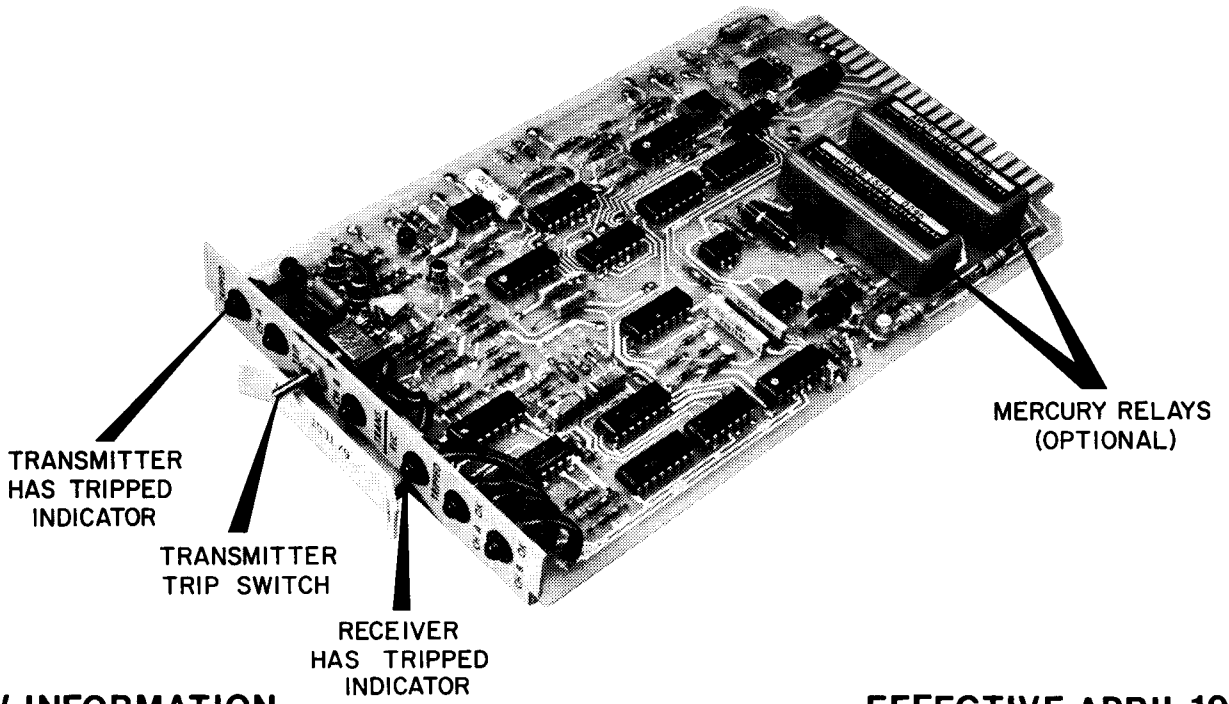
The Model 67 TEST Manual Test Module is an on-line unit designed to test the operation of the DIT-1 Protective Relaying System without removing it from service. The relaying system will not generate a trip if only one of its two subchannels is tested at a time, and so the subchannels are tested individually and successively. If an operational trip should arise during the test, the system is automatically preempted to transmit the valid signal.

Unless augmented with other equipment, the module requires two operators, one at either end of the system, with voice communication. Testing is accomplished by successively keying each of the two subchannels at the transmitter. The acknowledgement from the operator at the receiving end either concludes the test or indicates trouble.

The operator at the receiving end can be replaced with a three-frequency tone transmitter arranged to transmit, say, a mark to designate reception of a trip signal in subchannel A and a space to acknowledge a trip signal in subchannel B. The output of a three-frequency tone receiver, located at the transmitting end, can be arranged to light lamps or to give other appropriate indication of the reception of the test signal. The system may be tested, similarly, from the receiving end. In this case, the three-frequency tone transmitter keys the input of the Model 67 TEST through a three-frequency tone receiver at the transmitting end. Operation of the protective relaying system is then monitored by observing the supervisory lamps on the test module at the receiving end.

The Model 67 TEST will enable testing of the system from the input to the transmitter at the sending end to the input of the logic card at the receiving end. This provides a complete test of transmitter, communication circuit, and the receiving terminal. Testing additional elements, including trip-keying input to the Model 67A INTER and the remote trip-output relay can be provided. It is suggested that the factory be contacted for details.

The concepts of the design of the Model 67 TEST are outlined in the block diagram of Figure 2. The module has two main sections, a transmitter shown at the top of the illustration and a receiver, shown below, both of which use a 250-Hz oscillator for their timing functions.



NEW INFORMATION

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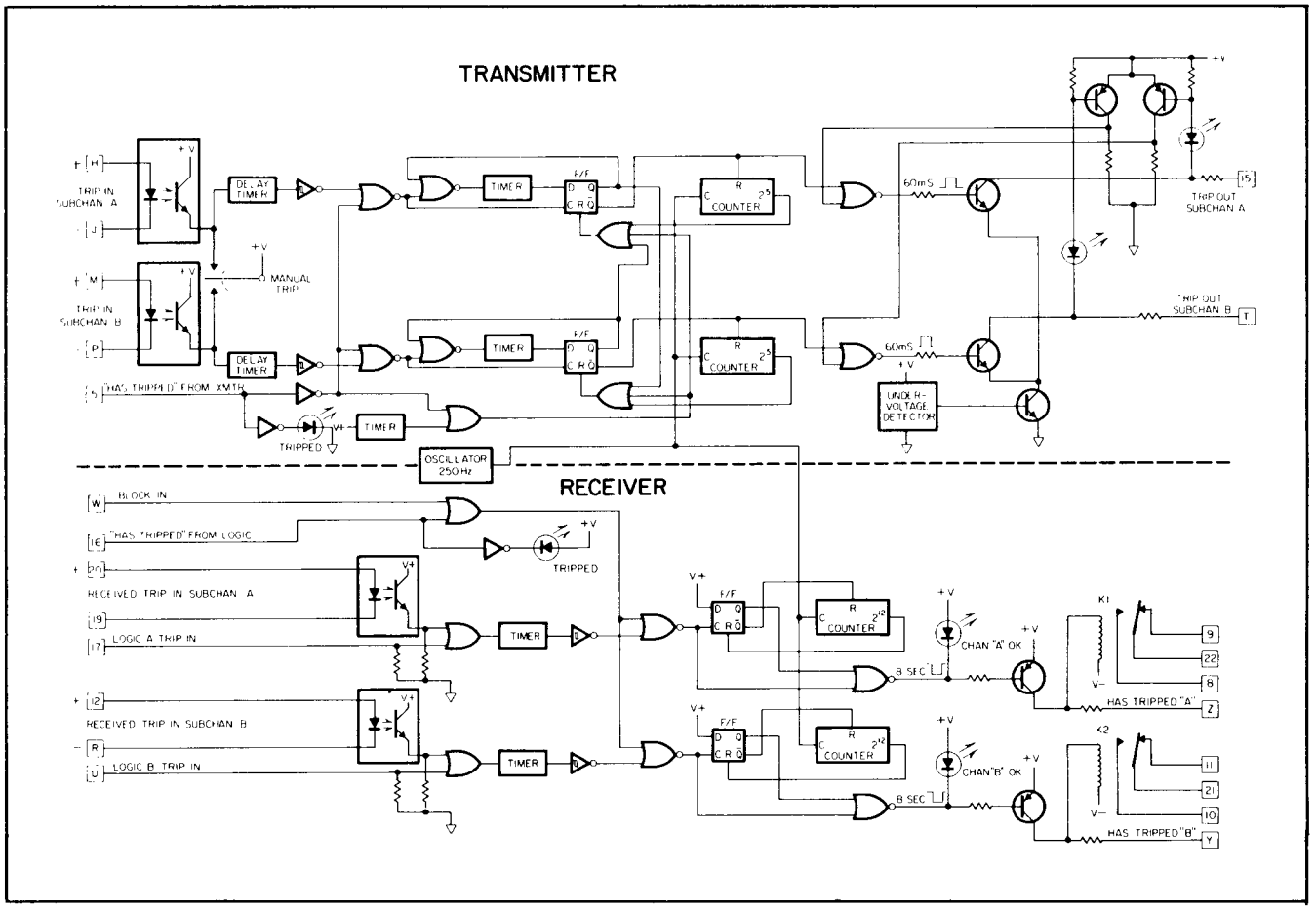


Figure 2. Block diagram, Model 67 TEST.

TRANSMITTER

The transmitter uses two Schmitt trigger circuits, shown at the upper left of Figure 2, which are keyed either by a center-off toggle switch, located on the front panel, or by optical isolators provided for remote keying of the unit. The two Schmitt triggers drive two lockout circuits which prevent whichever subchannel has not been keyed from being keyed during the time that the opposite subchannel is keyed. This prevents subchannels from being keyed simultaneously and so prevents the possibility of an accidental false trip.

The output of the Schmitt trigger also drives a one-shot timing circuit, the output of which drives the keying circuit of the Model 67 Transmitter through a pull-down transistor. The timing circuit limits the trip signal to about 65 ms, irrespective of how long the input keying signal is sustained.

The two pull-down transistors which key the transmitter are interconnected with each other so that if one of them is in the conducting mode the other is turned off. This arrangement provides for component redundancy to prevent a false trip from being generated because of failure of a single component.

An undervoltage-protection circuit prevents the transmitter from keying when an undervoltage condition exists.

RECEIVER

The receiver may receive the transmitted trip signal from either the logic module of the DIT-1 or from the tripping circuit on the Model 67 Interface card. Trip signals from the logic module are received by direct connection to that module. Connections for receiving trip signals through the interface card are made through optical-isolator inputs provided at the receiver. When a trip signal is received, it passes through a timer which requires that the trip be sustained for at least 15 ms for it to illuminate the CHANNEL OK indicator lamp. Once the lamp has been triggered, it will remain on for approximately 8 seconds. Both indicators may be on at the same time as when, for example, the operator at the transmitter keys both subchannels rapidly in succession.

The output of the receiver section of the Model 67 TEST is a solid-state-logic output. Plug-in relays, with mercury-wetted Form-C contacts, are provided at circuit positions K1 and K2.

SPECIFICATIONS

TRANSMITTER

Inputs: The test may be originated either with a toggle switch on the front panel, or through optical isolators provided for subchannels A and B. Optical isolators require 12 V, 40 mA trip current for 15 ms minimum.

Output: Pull-down transistors to common will carry up to 50 mA, each.

RECEIVER

Input: The receiver will respond either to CMOS logic level inputs from the logic card of the system or to inputs impressed on optical isolators for each subchannel. In the latter case the input signal must be 12 V, 40 mA for 15 ms, minimum.

Output: Two PNP pull-up transistors, one for each subchannel, will carry up to 50 mA, each.

Optional plug-in relays for each subchannel with mercury-wetted Form-C contacts provide an output signal by movement of their contacts.

GENERAL

Modules with solid-state-logic output require +12 Vdc, 50 mA. Modules with relay output require +12 Vdc, 75 mA and -12 Vdc, 25 mA. All operating power may be obtained from a Series 6000 power supply.

Temperature Range: The unit will operate in ambient temperatures in the range from -20 to +55°C.

Size: The module occupies a circuit card 4.713 inches high by 8 inches deep by one inch. It requires two one-half-inch module spaces in the DIT-1 Chassis.

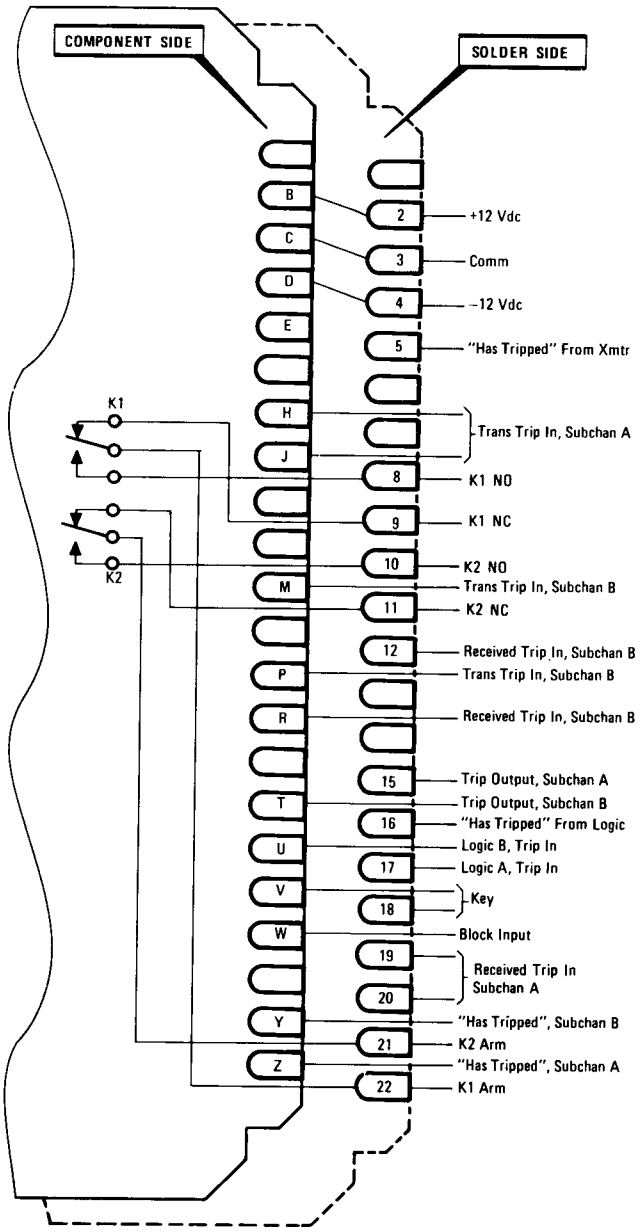
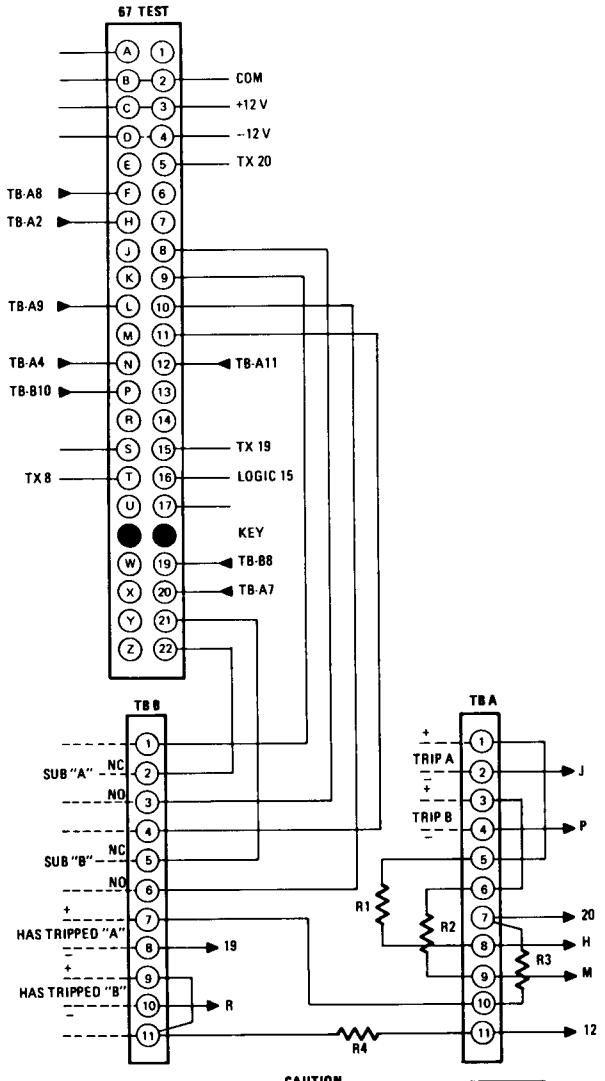


Figure 3. Edge-connector terminal assignments.

INSTALLATION

When supplied as a unit of a complete System, the Model 67 TEST will be mounted in the card chassis, interconnected as part of the system, and no special procedures for installation should be necessary. For retrofit into an earlier system, for a change in an existing system, or for other cases including routine maintenance, the following notes will be helpful.

Figure 3 shows terminal connections to the circuit card. Reference to the schematic will make the meaning of the designations clearer. A suitable mating connector, which will mount in the Chassis, is TRW/Cinch Part 251-22-30-261, Part HA-38545.



DC VOLTAGE	24 V	48 V	125 V
R1, R2, R3, R4	500 Ω	1.5 K	4.5 K
Part No.	H-1100-308	H-1220-35	H-1100-690

Figure 4. External connections to Model 67 TEST.

Figure 4 details the interconnections necessary between the Model 67 TEST and other elements of the DIT-1 System. Terminal blocks A and B can be arbitrarily chosen from any of the unused blocks at the back of the Chassis. Blocks selected should be as close as possible to the edge connector into which the Model 67 TEST is plugged, and wires should not be cabled with others in the chassis.

An arc-suppression network is provided at K1 and K2 for the contacts of both relays. Placement of Jumpers A or B (for each relay) will be determined whether the normally closed or the normally open contacts are protected. Additional protection may be needed depending on the nature of the load.

THEORY OF OPERATION

TRANSMITTER

The transmitter can be keyed either with S1, Figure 5, from the mark and space outputs of a three-frequency tone receiver, or from some other source. For the latter case, optical isolators IC1 and IC2 are the inputs, and these duplicate the action of S1.

When S1 is moved to trip subchannel A, flip-flop IC14B is triggered. This will remove the reset to counter IC17, which is driven by the 250-Hz oscillator using IC12 and IC13C. The output of the counter at Pin 3 delivers a pulse 2^5 counts later, so that after about 60 ms the flip-flop is reset. This circuit is a clocked, digital monostable pulse generator. When S1 is moved to trip subchannel B, the same action occurs with flip-flop IC14A and counter IC16.

The clocked digital monostable pulse generators are cross connected so that one is reset while the other is activated. Thus, when IC14B (subchannel A) is activated for a trip, IC14A (subchannel B) is reset through IC15B. After the trip signal has stopped, a few tenths of a second are required, because of the time constants of the circuit, before a trip signal can be effective on the D input of the flip-flop of the previously inactive channel. This delay is introduced to minimize the possibility of tripping both channels simultaneously by rapid movement of S1.

If the system is required for transmission of an operating trip while a test us underway, a "has tripped" signal from the Model 67 TRANS, which is a logic low, is received at Terminal 5. This signal, through IC10D and IC15C, resets both flip-flops to cancel the test. Simultaneously, the TRIPPED lamp, DS1, is illuminated through IC11F. The use of a logic low for the "has tripped" signal is a protective measure.

When power is first turned on, both flip-flops are reset through IC15C as the logic high from the power supply moves C10 high. This high is then removed as C10 charges through R54.

The outputs of the two monostable pulse generators feed through NOR gates IC13D and IC13A to the output transistors Q5 and Q6, one for each subchannel, which drive the trip-logic inputs at Terminals 19 and 8 of the Model 67 Transmitter. Q5 and Q6 also illuminate lamps DS2 and DS3 to indicate a test trip visually. As further protection against false tripping, the current through the lamps is sensed at the bases of transistors Q4 and Q3, the collectors of which are cross connected to the inputs of

NOR gates IC13D and IC13A. Thus, if the output of Trip A is activated (logic low) the current through DS2 will turn on Q3, place a logic high at IC13A-2 which will, in turn, turn off output transistor Q6 which otherwise could carry an erroneous subchannel-B trip signal.

Undervoltage protection for the transmitter is provided with Q8 and CR15. If V+ falls below the voltage level of the 9.1-V zener, Q8 is shut off and the source of current to the two output transistors, through Q7, is cut off.

RECEIVER

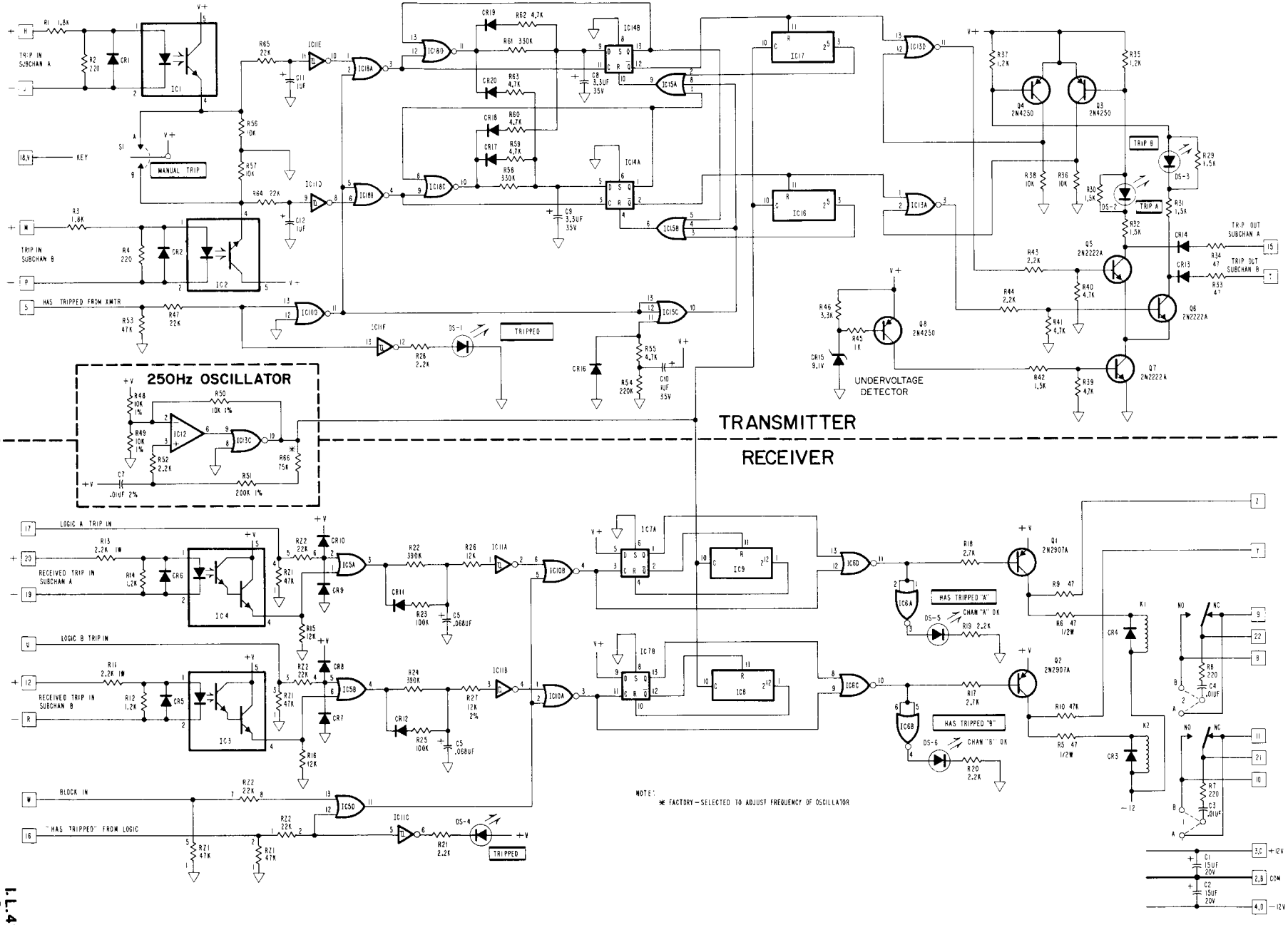
The receiver for the test signals is shown on the lower portion of Figure 5. While not identical, there is considerable similarity between the circuits of the transmitter and those of the receiver.

Received-trip signals can be taken from the Model 67 Logic card at Terminals 17 and U of the Model 67 TEST. They can be accepted from the Model 67 Interface card through the two optical isolators connected to Terminals 20 and 19 (Trip A) and Terminals 12 and R (Trip B). Receipt of trip signals is blocked whenever a block signal from the Model 67 Logic appears at Terminal W, or a logic signal for "has tripped", at Terminal 16, will prevent the receiver from indicating a valid, completed test when the system has actually been preempted to transmit a true operational trip signal.

As in the transmitter, there are two clocked, digital monostable pulse generators. IC7A and IC9 are in subchannel A; IC7B and IC8 are in subchannel B. The counters for the receiver, however, count 2^{12} counts, corresponding to about 8 seconds for a 250-Hz clock. The output from NOR gate IC6D or IC6C, therefore, will be held for about 8 seconds, even through the trip signal lasts for only about 60 ms. The output of each NOR gate drives a PNP pull-up transistor, as well as lamps DS5 and DS6 through inverting gates IC6A and IC6B. The transistors may be used to drive incandescent lamps on an external panel, or they may drive optional relays K1 and K2 whose contacts may be used as required. Jumpers A and B, associated with each relay, provide protection for either pair of the Form-C contact set.

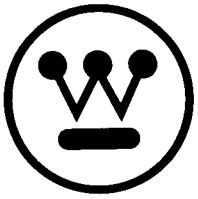
PARTS LIST

CIRCUIT SYMBOL	DESCRIPTION	PART NUMBER
	MODEL 67 TEST, ASSEMBLY HB-45760	
C1, 2	Capacitor, tantalum, 15 μF, 20%, 20 V, Kemet T324D156M020AS, or eq.	H-1007-716
C3, 4	Capacitor, ceramic disc, 0.01 μF, 20%, 500 V, Erie 811000Z5U0103M, or eq.	H-1007-83
C5, 6	Capacitor, MPC, 0.068 μF, 5%, 250 V, Siemens Type MKM, or eq.	H-1007-1407
C7	Capacitor, poly., 0.01 μF, 2%, 100 V, Wesco 32P, or eq.	H-5115-35
C8, 9	Capacitor, tantalum, 3.3 μF, 20%, 35 V, Kemet T324C335M035AS, or eq.	H-1007-1260
C10	Capacitor, tantalum, 1 μF, 10%, 35 V, Kemet T110A105K035AS, or eq.	H-1007-1156
C11, 12	Capacitor, ceramic, 1.0 μF, +80 -20%, 50 V, Sprague 5C0223105D8500C5, or eq.	H-1007-1153
CR1 thru 14 16 thru 20	Diode, silicon, Type 1N914B/1N4448	HA-26482
CR15	Diode, zener, silicon, 9.1 V, Type 1N960B	HA-41014
DS1 thru 6	Optodevice, LED, red, Texas Inst. TIL220, or eq.	HA-38939
IC1, 2	Photo isolator, GE Type 4N35, or eq.	HA-47104
IC3, 4	Photo-Darlington opto isolator, Litronix IL-CA2-30, or eq.	HA-41084
IC5	Quad, 2-input OR gate, RCA CD4071BE, or eq.	H-0615-24
IC6, 10, 13, 18	Quad, 2-input NOR gate, RCA CD4001AE, or eq.	H-0615-3
IC7, 14	Dual, D-type flip-flop, RCA CD4013AE, or eq.	H-0615-1
IC8, 9, 16, 17	12-Stage, ripple-carry, counter-divider, RCA CD4040AE, or eq.	H-0615-21
IC11	Hex Schmitt trigger, Motorola MC145848CP, or eq.	H-0615-60
IC12	Linear opamp., National LM741CN, or eq.	H-0620-52
IC15	Triple, 3-input AND gate, RCA CD-4075BE, or eq.	H-0615-33
K1, 2	Relay, mercury-wetted SPDT, break-before-make, non-bridging, Adams & Westlake AWCB-16541, or eq.	HA-24311
Q1, 2	Transistor, silicon, PNP, Type 2N2907A	HA-37439
Q3, 4, 9	Transistor, silicon, PNP, Type 2N4250	HA-39964
Q5, 6, 7	Transistor, silicon, NPN, Type 2N2222A	HA-37445
R1 thru 47 52 thru 65	Resistor, fixed, composition, 5%, ¼ W, value on schematic, Allen Bradley CB, or eq.	H-1009-(xxx)
R48, 49, 50	Resistor, metal-film, precision 10 K, 1%, 1/8W, Type RN55D, Spec HA-38301	H-1510-775
R51	Same as R48, 100 K	H-1510-737
RZ1	Resistor network, 47K, 2%, 7R/P, CTS 750-81-R47K, or eq.	HA-47880
RZ2	Resistor network, 47K, 2%, 4R/P, CTS 750-83-R47K, or eq.	HA-47879
——	Bar, shorting	HA-42904
——	Schematic	H- 45764



POWER CONNECTION TABLE			
IC NO.	TYPE	PINS	
		V +	COM
1	4N35	5	—
2	4N35	5	—
3	EL-CA2-30	5	—
4	EL-CA2-30	5	—
5	4071	14	7
6	4001	14	7
7	4013	14	7
8	4040	8	16
9	4040	8	16
10	4001	14	7
11	MC-14584	14	7
12	T41	7	4
13	4001	14	7
14	4013	14	7
15	4075	14	7
16	4040	8	16
17	4040	8	16
18	4001	14	7

Figure 5. Schematic of circuit, Model 67 TEST.



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