INSTALLATION • OPERATION • MAINTENANCE

INSTRUCTIONS

TYPE STU UNBLOCK RELAY
FOR USE WITH SOLID STATE RELAY

CAUTION: It is recommended that the user of this equipment become thoroughly acquainted with the information in these instructions before energizing this relay. Failure to observe this precaution may result in damage to the equipment. If the equipment is mounted in a cabinet, the cabinet must be bolted down to the floor or otherwise secured before swinging out the equipment rack to prevent its tipping over.

APPLICATION

The type STU relay is a completely solid-state carrier unblock auxiliary relay for use with solid-state relays and a type TCF frequency shift channel to prevent tripping for faults external to the line section to which it is applied and to permit instantaneous and simultaneous tripping for internal faults. The relay is arranged to respond to indications of fault direction, distance and power provided by the phase and ground distance, and overcurrent relays thereby controlling the transmission of an unblocking or trip signal and the initiation of high speed tripping for internal faults. Either two or three terminal line applications may be used.

CONSTRUCTION

The STU relay is mounted on a standard 19" wide panel, 8-3/4" high (5 rack units) with edge slots for mounting on a standard relay rack or panel. All components not on printed circuit boards are mounted on the panel and extend to the rear. For the outline and drilling plan, refer to Fig. 8.

All of the circuitry suitable for printed circuit board mounting is contained in an enclosure that projects from the rear of the panel and is accessible by opening the door on the front. The dotted lines enclosing separate areas of Fig. 1 indicate that the components thus enclosed are all on the same printed circuit board.

The printed circuit boards slide into position in slotted guides at the top and bottom of the enclosure, and the board terminals engage a terminal block at the rear of the compartment. Each board and terminal block are keyed so that if a board is placed in the wrong compartment, it cannot be inserted into the terminal block. The printed circuit boards are labeled from left to right respectively: Protective Relay Interface, Timing, Channel, Arming, Output and Test.

SUPERSEDES I. L. 41-959
* Denotes change from superseded issue.

EFFECTIVE AUGUST 1969

A board extender (Style No. 644B315G01) is available for facilitating circuit voltage measurements or major adjustments. After withdrawing any one of the circuit boards, the extender is inserted in that compartment. The board then is inserted into the terminal block on the front of the extender. This restores all circuit connections; and all components, test points and printed circuit terminals are readily accessible.

* Most of the relay operates from a zener regulated 20 volts d-c supply (Z1 on Fig. 1) which is mounted on a heatsink at the rear of the panel. The 20 volt zener and a portion of the relay works from a 45 volt d-c input supply. External connections to the relay are made through a 32 terminal circuit receptacle, J101 in Fig. 1.

SYSTEM OPERATION

The type STU unblock relay is used in a directional unblock relay scheme for power line protection. High-speed tripping is obtained for two or three terminal line applications for faults anywhere in the protected line. The signals to which the STU relay responds are obtained from the receiver of the TCF frequency shift channel and the output of the local protective relays.

Since distance relays may operate on a loss of a-c potential, the STU relay provides alarm and lockout of tripping 3000 milliseconds after this condition occurs. The 3000/100 MS timer picks up and the output from NOT 1 drops out an AL loss of potential alarm mounted elsewhere in the relaying system. This also prevents output from A 2 since there is no signal from NOT 1.

The output of A 2 initiates keying of the local transmitter through operation of OR 2, by shifting the transmitter from the blocking frequency to the unblocking or trip frequency. In 10 milliseconds after a primary pilot trip operation, the 10/150-400 millisecond timer picks up and also maintains the unblocking frequency keying for 150 to 400 milliseconds after a loss of the trip signal. This time is adjustable to allow for the breaker failure timer setting at the remote terminal.

In addition, the 52b contact initiates the trip frequency transmission 30 milliseconds after the local circuit breaker opens and until such time as the circuit breaker is reclosed. The 30/0 millisecond timer delays the transmission of trip frequency to obtain coordination for bus fault tripping of the local circuit breaker where tripping of the remote breaker would be incorrect and might cause undesired interruption to tapped transformer terminals. Transmission of the trip or unblocking frequency is necessary to permit tripping of the remote terminal should the remote circuit breaker be closed into a fault or should a fault develop in the protected line while the local circuit breaker is open.

<u>Internal Fault</u>

* The operation of any or all the protective relays PR-1, PR-2 or PR-3 for an Internal Fault perform the following (refer to the block diagram, Fig. 2):

1. Energizes the 3 second timer and A2 thereby giving an output from A2 for up to 3 seconds.

2. "Arms" A6 or puts it in a "ready" condition for up to 3 seconds by removing a blocking bias voltage.

3. Energize the transient blocking circuit at OR 4 up to 3 seconds.

4. Key the TCF transmitter for 3 seconds through OR 2 to shift the frequency from a blocking to an unblocking or trip condition.

For an internal fault, the TCF Receivers will produce a "1" output unblock signal to energize A1 thereby producing a "1" input from the channel to A3. This together with the signal from PR-1, PR-2 or PR-3 at A3 will cause tripping 2 milliseconds later. This operation will be completed before the transient blocking becomes effective.

External Fault

If no unblocking or trip signal is received from the remote terminal when PR-1, PR-2, or PR-3 operates (as for an External Fault), there will be no tripping output from A1. If tripping does not take place within 25 milliseconds after the protective relays operate, the transient blocking circuit energized through OR 4 will desensitize A6 to prevent possible undesired tripping during transients occurring at the clearing (elsewhere) of an external fault.

The above procedure also holds true if the TCF unblocking or trip signals are received from the remote terminals and the protective relays do not operate. This also is an external fault.

Sequential Faults

Occasionally an External Fault will be followed by an internal fault before the former is cleared. In order to prevent a long delay in clearing such an internal fault, a "transient unblocking" feature is included. Although transient blocking has been set up by the initial external fault, the presence of an Internal Fault will cause an output from A3 which will energize the transient unblocking circuit. After 25 milliseconds, A6 will be resensitized and tripping will be permitted.

RELAY OPERATION

The complete detailed relay circuit is shown on the internal schematic, Fig. 1. The operation of the logic elements shown on Fig. 2, and the individual circuit components will be described in the following paragraphs.

Protective Relay Interface Board

The Protective Relay printed circuit board contains the required circuits for interface with the protective relays, PR-1, PR-2 and PR-3, These logic blocks are the protective relay input OR 1 and its associated Buffer B3, for surge protection, the 3000/100 millisecond time delay for loss of a-c potential, and A2.

Under normal conditions, J101 terminals 30, 31 and 32, the inputs to the STU relay from PR-1, PR-2 and PR-3 respectively, are held at negative (zero volts) thereby holding transistor Q101, the output of B3, non-conductive. With Q101 off, transistors Q102 and Q109 have base drive holding them both conductive. Since Q109 is turned on, this represents a "0" output from A2. Transistor Q107 is normally on representing a "1" signal from NOT 1 to the AL loss of potential alarm elsewhere in the relaying system.

When one or more of the protective relays, PR-1, PR-2 or PR-3 operate and positive 20 volts d-c is applied to J101 terminals 30, 31 or 32, then transistor Q101 will conduct and immediately turn off Q102 and Q109. Transistor Q109 is the output stage of A2, and for A2 to assume a "1" output, both transistors Q101 (output of buffer B3) and Q108 (output of NOT 1) must be conducting thereby holding Q109 non-conductive. Therefore, immediately following reception of a protective relay "1" signal, A2 will yield a "1" output.

Transistors Q102 to Q105 are associated with the 3000/100 millisecond time delay, and Q106 to Q108 with NOT 1. Normally, transistors Q102, Q104, Q107 and Q108 are conducting and Q103 and Q105 non-conductive. Therefore, capacitor C102 in the three (3) second timer is fully discharged through transistor Q104. Since Q108 is conducting, this represents a "1" input to A2 from NOT 1.

Since distance relays may operate on loss of a-c potential, the 3000/100 millisecond timer provides alarm and blocks A2 three (3) seconds after loss of primary protection and blown a-c potential fuse. As mentioned above, output from any or all the protective relays turns off transistor Q102. Therefore, providing the timer disable switch between J101 terminals 12 and 13 is closed, transistor Q103 has base drive to cause it to conduct and turn off transistor Q104. When this occurs, capacitor C102 will begin to charge from positive 20 volt d-c through resistors R114 and R116 and, in 3000 milliseconds, reaches a sufficient potential to breakdown zener diode Z103 and cause transistor Q105 to conduct. With Q105 conducting, base drive is removed from transistors Q106 and Q108 to make them non-conductive. Therefore, with Q108 off, the "1" input from NOT 1 becomes a "0" and blocks A2. In addition, since Q106 is off, no base drive is available for Q107 so it becomes non-conductive and provides a "0" signal to the AL alarm for indication of loss of a-c potential. Upon loss of the protective relay signal, transistor Q104 will turn on and permit capacitor C102 to discharge in 100 milliseconds below the breakdown of zener diode Z103 and turn off transistor Q105.

Timing Board

The Timing printed circuit board contains two time delays necessary for proper operation of the relaying system: one, the 30/0 millisecond timer used for coordination with bus fault and remote breaker tripping; and, two, the 10/150-400 millisecond signal continuing timer used for coordination with the breaker failure timer.

Under normal conditions, transistor Q201, the output of Buffer circuit B4, and the input to the 30/0 timer, is non-conductive thereby preventing a path for base current to turn on transistor Q202. As a result, printed circuit terminal #14 is held at negative (zero volts) representing a "0" output from this timer.

After the local circuit breaker opens, positive 125 volt d-c is applied through the now closed 52b contact to J101 terminal No. 20. When this occurs, transistor Q201 has base drive and immediately becomes conductive. As a result, capacitor C202 starts charging to negative through resistor R207 and the collector-emitter circuit of Q201, and in 30 milliseconds, C202 assumes a low enough potential below positive 20 Vdc to breakdown zender diode Z203 and provide a path for base drive to make transistor Q202 conductive. Therefore, with Q202 conducting, this represents a "1" signal to OR 2 to shift the transmitter from a blocking to an unblocking or trip frequency. Upon breaker reclosing, the 52b contact opens turning transistor Q201 off thus permitting capacitor C102 to rapidly discharge for immediate dropout.

The 10/150-400 millisecond time delay operates similar to the 30/0 MS timer. After a primary pilot trip operation, capacitors C203 and C204 will charge in milliseconds through diode D202, resistor R212 and the collector-emitter circuit of transistor Q203 to a low enough potential to cause breakdown of zener diode Z204 and conduction of transistor Q204. Once Q204 turns on, a "1" signal to OR 2 keys the transmitter to the trip frequency for the duration of the pilot trip signal. After loss of the pilot trip signal, capacitors C203 and C204 will discharge in 150 to 400 milliseconds (adjustable by resistor R214) and turn Q204 off. This 150 to 400 MS dropout time holds the unblocking or trip frequency on to provide coordination with the breaker failure timer. Normal dropout time is factory calibrated at 300 milliseconds.

Channel Interface Board

The channel printed circuit board contains A2 and its associated Buffers B1 and B2 for interface with the TCF Receiver, and OR 2 for interface with the TCF Transmitter.

Under normal conditions and for three-terminal line applications, both J101 terminals 8 (TCF RCVR-1) and 7 (TCF RCVR-2) are held at negative (zero volts) thereby allowing no base drive for transistors Q151 and Q152 thus holding them non-conductive. As a result, transistor Q153 has base drive, so it is normally conducting and represents a "0" output from A1.

When both of the TCF Receivers receive the unblocking or trip frequency from the other terminals, they will produce a positive 20 Vdc potential at J101 terminals 8 and 7. When this occurs, both transistors Q151 and Q152 have base drive and start conducting. In turn, with both Q151 and Q152 on, base drive is removed from transistor Q153 which them stops conducting and represents a "1" output signal from A1. If only one of the TCF Receivers yield a trip output, then transistor Q153 still will receive base drive from the other input transistor in the STU and a "0" signal will be received from A1.

In the case of two-terminal line applications, either J101 terminal 8 or 7 must be connected to J101 terminal 4 to simulate having a constant signal of "1" at one of the A1 inputs. Under this condition, transistor Q153 will still be normally conducting thus representing a "0" output from A1. When the J101 terminal (either 8 or 7) not connected to J101 terminal 4 receives a positive 20 Vdc signal from the TCF, transistor Q153 will lose its base drive and turn off to produce a "1" output from A1.

Under normal conditions, the inputs to OR 2 printed circuit terminals #14, 15 and 16 on the Channel Board are held at negative (0 volts) thereby preventing any base drive from turning on transistors Q154, and thus Q155. When one or more of these printed circuit terminals receive a positive d-c signal, "1", base drive will turn on transistor Q154 which in turn will make transistor Q155 conduct and apply positive 45 Vdc to the TCF transmitter to cause it to shift from the block to the unblock or trip frequency. As can be seen from Fig. 2, in order for the TCF transmitter to be keyed, OR 2 must receive a positive going "1" signal from A2, the 30/0 timer or the 10/150-400 timer.

Arming Board

The Arming printed circuit board contains the logic blocks which combine the information from the protective relays and the channel receiver and in turn provides the proper interfaces for this information to be translated to the Output Board for transient block, arm, transient unblock and pilot trip.

Normally, there is a "0" signal to OR 4 from A1 (printed circuit terminal #12) and from A2 (printed circuit terminal #14) thereby resulting in a "0" signal at printed circuit terminal #9, the output of OR 4. When either or both A1 and A2 yield a "1" output signal to the inputs of OR 4, current is allowed to flow through resistor R287 and diode D264 (for an A1 output) or resistor R288 and diode D265 (for an A2 output). In this case, therefore, a "1" is received from OR 4 to energize the transient block circuitry in the Output Board.

Likewise, both inputs into A3 are normally "0". The input transistors of A3 are Q255 for A1 and Q254 for A2. Normally both Q255 and Q254 have no base drive and, as a result, they are both non-conductive. Therefore, the output transistor of A3, Q256, has base drive and is turned on thus allowing Q254 to conduct and provide a proper interface with the Output Board. If a "1" signal is received from both A1 and A2, then both transistors Q255 and Q254 become conductive thereby removing base drive to Q256 to turn it off. This causes Q257 to stop conducting and allow the 2/0 timer and the transient unblock circuits in the Output Board to function. If either Q255 or Q254 remains non-conductive, then transistor Q257 will stay on and a "0" output will be received from A3.

The Arm circuit is energized from A2 and under normal conditions with a "0" output from A2, there is no base drive from transistor Q258, so it is non-conductive. As a result, with Q258 off, base drive holds transistor Q259 conducting thereby keeping the Output Board "disarmed". As soon as A2 assumes a "1" output state, base drive turns transistor Q258 on and thereby Q259 turns off and arms A6 on the Output Board.

Output Board

The Output Board contains all the logic required for final tripping, transient blocking and transient unblocking. In reference to Fig. 2, a "1" signal from OR 4 represents a transient blocking signal. A "1" output from A3 is a pilot tripping signal in two milliseconds but prior to tripping, it is a transient unblocking signal in the event that transient blocking has already occurred.

The 2/0 millisecond time delay circuit is used to prevent tripping from improper signals of short duration. Normally, printed circuit terminal #6 is held at positive 20 Vdc thereby preventing capacitor C306, associated with the

2/0 MS timer, from charging. Under conditions for tripping, transistor Q257 in A3 (Arming Board) will turn off and allow capacitor C306 to charge to negative through resistors R318 (Output Board) and R279 (Arming Board). After the factory calibrated time (by S1) of two milliseconds, the voltage across C306, which is applied to the base emitter circuit of transistor Q305 in A6, is sufficient to cause Q305 to operate and thereby turn transistor Q306 off providing it is armed.

The 2/0 millisecond timer has no intentional reset time delay. If a tripping condition is indicated for some time less than two (2) milliseconds, such as during a reversal of fault power flow, as soon as transistor Q257 in A3 again conducts, capacitor C306 will rapidly discharge through the collector emitter circuitry of Q257, diode D261 and resistor R318. This rapid resetting of the 2/0 timer prevents possible "notching up" of the charge on C306 during momentary and intermittent interruptions under normal conditions.

The A6 circuit block consists of transistors Q305 and Q306 and the associated components. Under normal conditions, transistor Q305 is non-conducting and Q306 fully conducting. The base of Q306 is held well below its emitter potential by means of the arming circuitry voltage divider consisting of resistors R324, R335, diode D308 and transistor Q259. With this bias, transistor Q306 is held in saturation and is desensitized so that even if a tripping voltage were applied to Q305, transistor Q306 would not turn off. This desensitizing circuit is an arrangement to prevent inadvertent operation of A6 caused by surges on the d-c system. As long as Q306 is conducting, its collector is at a high enough potential above negative d-c so that transistor Q307 in the tripping amplifier cannot turn on.

Upon occurrence of an internal fault, transistor Q259 in the Arming Board turns off thereby removing the desensitizing bias from Q306 by open-circuiting the path of current through diode D308 and resistor R335. This causes A6 to become "armed" and in a ready condition for a tripping operation. After a two (2) millisecond time delay, the potential across capacitor C306 is sufficient to cause Q305 to conduct and thus turn off Q306. When Q306 is no longer conducting, the potential of its collector circuit drops to a relatively low value and allows sufficient voltage to appear across the base-emitter circuit of transistor Q307 in the trip amplifier, causing it to become conductive. In turn, transistors Q308 and Q309 turn on and apply a pilot trip voltage output.

The transient blocking circuit is energized only when there is an output from OR 4. An output from OR 4 consists of a positive potential which immediately turns on transistor Q302 thus dropping its collector potential (at TP 303) to a very low value. Therefore, the positive voltage is removed from the base of transistor Q303 turning it off. When this occurs, capacitor C305 charges in 25 milliseconds to a potential which is sufficient to cause the breakdown of zener diode Z303 and provide a path for base current to turn on transistor Q304. With Q304 on, a conducting path through resistors R324, R323, diode D306 and the collector-emitter circuit of Q304 is provided in order to hold a desensitizing bias on transistor Q306 in A6. Thus, the transient blocking circuitry allows 25 milliseconds after the operation of either a protective relay or the reception of a TCF trip signal for a "1" to be received from A6. If tripping does not occur in this time, as during an external fault, operation of the transient blocking circuit will hold A6 desensitized in order to prevent undesirable operation during transients associated with power reversals on the protected line or at the clearing of an external fault.

If an internal fault occurs before the external fault is cleared, it is desirable to obtain high-speed tripping. The transient unblocking circuitry permits this since transistor Q257 in A3 will turn off and remove the positive 20 Vdc potential on printed circuit terminal #10. This allows capacitor C301 to charge to negative through diode D301, resistor R314 and the collector-emitter circuit of transistor Q304, which has been turned on due to transient blocking. In 25 milliseconds, C301 will charge to a sufficient potential to turn on transistor Q301 and permit base drive for transistor Q303. This will immediately turn on Q303 which allows a path for rapid discharge of capacitor C305. When this occurs, zener diode Z303 will not breakdown, and Q304 will stop conducting thereby interrupting the desensitizing circuit from the base of transistor Q306. Therefore A6 will be able to assume a "1" output and provide tripping after a delay of only 25 milliseconds.

Test Board

The Test Board contains two potentiometers, S1 and S2, used for factory time delay adjustments. Also, six test points are easily accessible from the front of this board for facilitating system tests of the STU Relay.

Potentiometer S1 is the 2/0 millisecond time delay adjustment, and S2 is the 25/0 transient unblocking time delay adjustment. These potentiometers are used only for factory calibration of the STU Relay.

Listed below are the six test points on the Test Board. Test points 1 to 5 are red, and test point 6 is black.

1. Pilot Trip
2. Transient Block
3. Arm - Received Protective Relay
4. Received Channel
5. Transmitter Key
6. Negative DC

CHARACTERISTICS

Input Voltage	45 volts D-C
Current Drain	100 milliamperes maximum
Pilot Trip Output	10 milliamperes at positive 20 Vdc
Min. Operate Time	2 milliseconds
Keying Voltage	Positive 45 volt D-C
Blown A-C Fuse Detection Timer	3 seconds
Ambient Temperature Range	-20°C to +55°C around chassis

Dimensions	panel height: 8-3/4" or 5 R.U. panel width: 19" panel depth: 6"
Weight	approximately 9 pounds

SETTINGS

Normally, there are no settings to be made on the STU unblock relay. All various time delay circuits are factory adjusted to the stated time in Fig. 2. However, if conditions require, the dropout time of the 10/150-400 millisecond timer may be changed from the factory setting of 300 MS to any value between 150 and 400 MS as explained under the Calibration section.

INSTALLATION

The STU Relay is generally supplied on a relay rack as part of a complete relay system assembly. The location must be free from dust, excessive humidity, vibration, corrosive fumes or heat. The maximum ambient temperature around the chassis must not exceed 55°C.

The outline and drilling plan of the STU Relay is shown in Fig. 8.

ADJUSTMENT AND MAINTENANCE

A. Acceptance Test

The operation of the STU Unblock Relay can be checked by taking voltage measurements at the six (6) test points on the Test Board. Energize the STU Relay with 45 Vdc and measure the positive d-c voltages on test points 1 to 5 with respect to negative d-c, test point 6, under the following conditions:

Note: In reference to Fig. 1, use the timer disable switch (between J101 terminals 12 and 13) closed unless otherwise noted in tests below.

1. Normal Condition.	Test Point 1 - 0 Vdc Test Point 2 - 19 Vdc Test Point 3 - less than 0.5 Vdc Test Point 4 - less than 0.5 Vdc Test Point 5 - 0 Vdc
2. Protective Relay Operation. (Open timer disable switch) (Apply positive 20 Vdc to J101 terminal 30)	Test Point 1 - 0 Vdc Test Point 2 - less than 0.5 Vdc Test Point 3 - 19 Vdc Test Point 4 - less than 0.5 Vdc Test Point 5 - 45 Vdc
3. Channel Receiver Operation. (Apply positive 20 Vdc to J101 terminals 8 and 9)	Test Point 1 - 0 Vdc Test Point 2 - less than 0.5 Vdc Test Point 3 - less than 0.5 Vdc Test Point 4 - 7 Vdc Test Point 5 - 0 Vdc

4. Protective Relay and Channel Operation. (Apply pos. 20 Vdc to J101 terminals 8 and 9. Then apply pos. 20 Vdc to J101, terminal 30)

Test Point 1 - immed. 20 Vdc, in 3 sec. 0 Vdc

Test Point 2 - immed. 19 Vdc, in 3 sec. less than 0.5 Vdc

Test Point 3 - immed. 19 Vdc, in 3 sec. less than 0.5 Vdc

Test Point 4 - immed. 7 Vdc, in 3 sec. 7 Vdc

Test Point 5 - immed. 45 Vdc, in 3 sec. 0 Vdc

B. Recommended Routine Maintenance

Periodic checks of the relaying system are desirable to indicate impending failure so that the equipment can be taken out of service for correction. Any accumulated dust should be removed at regular maintenance intervals.

The proper adjustments to insure correct operation of this relay have been made at the factory and should not be disturbed after receipt by the customer. If the adjustments or if the components or printed circuit boards which affect calibration have been changed, then recalibration per the Calibration section following will have to be made on the circuits in question.

C. Calibration

1. 10/150-400 T.D. (Timing Board)

The dropout of the 10/150-400 millisecond signal continuing timer may be adjusted from 150 to 400 MS to allow for various settings of the breaker failure timer. By comparing the Pilot Trip voltage of the relay with the timer output voltage at printed circuit terminal 16 (Timing Board) under dropout conditions, the time delay between a change of the input voltage and the output voltage can be adjusted from 150 to 400 milliseconds. For more dropout time, potentiometer R214 on the Timing Board should be turned clockwise, and for less time it should be turned counter-clockwise. Factory setting of the dropout time is 300 milliseconds. Pickup time can be calibrated in the same manner except for more time, increase resistor R212 and for less time, decrease R212. Pickup time should be 10 milliseconds. Location of potentiometer R214 and resistor R212 can be seen on the Timing Board component location, Fig. 4.

2. 30/0 T.D. (Timing Board)

The pickup time of the 30/0 millisecond timer can be calibrated by comparing the input voltage to Buffer B4 with the output voltage at printed circuit terminal 14, Timing Board, under pickup conditions. Pickup time should be 30 milliseconds. Increase resistor R207 (Timing Board) for more time or decrease R207 for less time. Location of resistor R207 can be seen in Fig. 4.

3. 3000/100 T.D. (P. R. Interface Board)

The 3000/100 millisecond time delay can be calibrated by comparing the time duration for a voltage change between the timer input, the output of Buffer B3, and the timer output, printed circuit terminal 14 (P. R. Interface Bd.) under pickup and dropout conditions. Normal pickup time is 3000 milliseconds. For more pickup time, increase resistor R116 and for less time, decrease R116. Dropout time can be calibrated by using a higher value of resistor R115 for more time or a lower value for less time. Normal dropout calibration time is 100 milliseconds. Location of resistors R115 and R116 can be seen on the Protective Relay Board component location, Fig. 3.

4. 2/0 MS Timer (Output Board)

In order to calibrate the 2/0 millisecond time delay, connect a jumper across capacitor C305 on the Output Board. Then compare the voltage at test point TP 255 on the Arming Board with the voltage at test point TP 306 on the Output Board under a trip condition. If the time delay between a change in both voltages is not two milliseconds, turn potentiometer S1 on the Test Board clockwise for more time and counter-clockwise for less time. Location of components and test points may be seen in Figs. 6 and 7. After calibration, remove the jumper from capacitor C305 and insure that the locking clamp on S1 is tight.

5. Transient Unblocking 25/0 Time Delay (Output Board)

In order to calibrate the transient unblocking time delay, the STU Relay must be in a transient block state. After putting the relay in a block state, compare the voltage at test point TP 255, Arming Board, with the voltage at Test Point 1, Test Board. If the time delay between a voltage change at the input (TP 255) and output (TP 1) is not 25 milliseconds, then turn potentiometer S2 (Test Board) clockwise for more time and counter-clockwise for less time. Location of TP 255 can be seen in Fig. 6, Arming Board component location.

6. Transient Blocking 25/0 Time Delay (Output Board)

To calibrate the transient blocking time delay, compare the voltage at test point TP 303 on the Output Board with test point 2, Test Board. Apply a transient block signal and if the time delay between a voltage change at the input (TP 303) and output (Test Point 2) is not 25 milliseconds, then turn potentiometer R316 clockwise for more time and counter-clockwise for less time. Location of the potentiometer R316 and test point TP 303 can be seen in Fig. 7.

D. Electrical Checkpoints - Trouble Shooting

The components of the STU Unblock Relay are operated well within their ratings and normally will give long and trouble-free service. However, if a relay has given indication of trouble in service or during routine checks, the voltages tabulated in Table I should be checked to determine the faulty circuit.

Test point voltages for the P. R. Interface, Timing, Channel, Arming, Output and Test printed circuit boards in the STU Unblock Relay are listed in Table I under various system conditions. The exact values will vary from one relay to another but, in general, will be within ±10% between relays. A Board Extender is helpful in checking test point voltages.

RENEWAL PARTS

Repair work can be done most satisfactorily at the factory. However, interchangeable parts can be furnished to the customers who are equipped for doing repair work. When ordering parts, always give the complete nameplate data and identify the part by its designation on the internal schematic drawing Fig. 1, as well as all information in the Electrical Parts List.

TABLE I

ELECTRICAL CHECKPOINTS - TROUBLE SHOOTING VOLTAGES

All test point voltages are positive D-C taken with respect to negative, Test Point No. 6 on the Test Board

TEST CONDITIONS

TEST POINTS	NORMAL STAND-BY	PROTECTIVE RELAY OPER. (3 SEC. TIMER DISABLED)	PROTECTIVE RELAY & CHANNEL RCVR. OPER. (3 SEC. TIMER DISABLED)	PROTECTIVE RELAY & CHANNEL RCVR. OPER. (3 SEC. TIMER USED) (VOLTAGES AFTER 3 SEC)
PROTECTIVE RELAY BD.				
TP 101	12.5 Vdc	less than 0.5	less than 0.5	less than 0.5
TP 102	6.5	6.5	6.5	less than 0.5
TP 103	less than 0.5	less than 0.5	less than 0.5	17
TP 104	6	6	6	less than 0.5
TP 105	less than 0.5	less than 0.5	less than 0.5	20
TP 106	20	20	20	0
TP 107	less than 0.5	less than 0.5	less than 0.5	9
PCT -5	less than 0.5	20	20	6.5
PCT -15	less than 0.5	7	7	less than 0.5
TIMING BD.				
TP 201	20	20	20	20
TP 202	20	20	less than 0.5	20
PCT -14	0	0	0	20
PCT -16	0	0	20	0
CHANNEL BD.				
TP 151	15	15	less than 0.5	less than 0.5
TP 152	15	15	less than 0.5	less than 0.5
TP 153	45	less than 0.5	less than 0.5	45
PCT -10	less than 0.5	less than 0.5	7	7
PCT -18	0	45	45	0

- PCT INDICATES PRINTED CIRCUIT TERMINAL

TABLE I (CONT.)

TEST POINTS	NORMAL STAND-BY	PROTECTIVE RELAY OPER. (3 SEC. TIMER DISABLED)	PROTECTIVE RELAY & CHANNEL RCVR. OPER. (3 SEC. TIMER DISABLED)	PROTECTIVE RELAY & CHANNEL RCVR. OPER. (3 SEC. TIMER USED) (VOLTAGES AFTER 3 SEC.)
		TEST CONDITIONS		
<u>ARMING BD.</u>				
TP 253	10	10	less than 0.5	less than 0.5
TP 254	less than 0.5	less than 0.5	20	less than 0.5
TP 255	20	20	0	20
TP 256	6.5	less than 0.5	less than 0.5	6.5
PCT -1	10	less than 0.5	less than 0.5	10
PCT -19	less than 0.5	19	19	less than 0.5
<u>OUTPUT BD.</u>				
TP 301	20	20	20	20
TP 302	0	0	0	0
TP 303	2	less than 0.5	less than 0.5	less than 0.5
TP 304	2	7.5	2	7.5
TP 305	19	19	5.5	19
TP 306	0	0	13	0
TP 307	20	20	less than 0.5	20
TP 308	0	0	20	0
PCT -14	19	less than 0.5	19	less than 0.5
<u>TEST BD.</u>				
TEST PT. - 1	0	0	20	0
TEST PT. - 2	19	less than 0.5	19	less than 0.5
TEST PT. - 3	less than 0.5	19	19	19
TEST PT. - 4	less than 0.5	less than 0.5	7	7
TEST PT. - 5	0	45	45	0
TEST PT. - 6	0 (REF)	0 (REF)	0 (REF)	0 (REF)

ELECTRICAL PARTS LIST

CIRCUIT SYMBOL	PROTECTIVE RELAY INTERFACE BD. (S# 201C050G01) DESCRIPTION	WESTINGHOUSE DESIGNATION
D101-D102	DIODE 1N645A	837A692H03
D103-D105		
D104	DIODE 1N457A	184A855H07
Z101	ZENER DIODE 1N3686B	185A212H06
Z102-Z103	ZENER DIODE 1N957B	186A797H06
Z104	ZENER DIODE 1N3688B	862A288H01
Q101-Q102	TRANSISTOR 2N3417	848A851H02
Q103-Q106		
Q108-Q109		
Q104-Q105	TRANSISTOR 2N697	184A638H18
Q107	TRANSISTOR 2N3645	849A441H01
C101	CAPACITOR 0.047 MFD., 200 VOLTS, ±5%	849A437H04
C102	CAPACITOR 68 MFD., 35 VOLTS, ±20%	187A508H02
C103	CAPACITOR 0.27 MFD., 200 VOLTS, ±10%	188A669H05
R101-R102	RESISTOR 4.7K OHMS, ½ WATT, ±2%	629A531H48
R103	RESISTOR 82K OHMS, ½ WATT, ±2%	629A531H78
R104-R122	RESISTOR 10K OHMS, ½ WATT, ±2%	629A531H56
R105-R123	RESISTOR 6.8K OHMS, ½ WATT, ±2%	629A531H52
R106-R108	RESISTOR 22K OHMS, ½ WATT, ±5%	184A763H59
R111-R114		
R131		
R107-R109	RESISTOR 10K OHMS, ½ WATT, ±5%	184A763H59
R110-R112		
R113-R117		
R118-R120		
R121-R126		
R127-R130		
R132		
R115	RESISTOR 6.8K OHMS, ½ WATT, ±5%	184A763H47
R116	RESISTOR 56K OHMS, ½ WATT, ±5%	184A763H69
R119-R128	RESISTOR 12K OHMS, ½ WATT, ±5%	184A763H53
R124	RESISTOR 27K OHMS, ½ WATT, ±2%	629A531H66
R125	RESISTOR 150 OHMS, 3 WATT, ±5%	762A679H01
R133	RESISTOR 4.7K OHMS, ½ WATT, ±5%	184A763H43

\- INDICATES TYPICAL VALUE

ELECTRICAL PARTS LIST

CIRCUIT SYMBOL	TIMING BD. (S# 201C046G01) DESCRIPTION	WESTINGHOUSE DESIGNATION
D201-D202	DIODE 1N457A	184A855H07
Z201	ZENER DIODE 1N3686B	185A212H06
Z202-Z203 Z204	ZENER DIODE 1N957B	186A797H06
Q201	TRANSISTOR 2N3417	848A851H02
Q202-Q203	TRANSISTOR 2N1132	184A638H20
Q204	TRANSISTOR 2N697	184A638H18
C201	CAPACITOR 0.047 MFD., 200 VOLTS, ±5%	849A437H04
C202	CAPACITOR 4.7 MFD., 35 VOLTS, ±10%	184A661H12
C203-C204	CAPACITOR 6.8 MFD., 35 VOLTS, ±5%	184A661H21
* R201	RESISTOR 47K OHMS, 1 WATT, ±5%	187A643H67
R202	RESISTOR 4.7K OHMS, ½ WATT, ±2%	629A531H48
R203	RESISTOR 82K OHMS, ½ WATT, ±2%	629A531H78
R204	RESISTOR 10K OHMS, ½ WATT, ±2%	629A531H56
R205	RESISTOR 6.8K OHMS, ½ WATT, ±2%	629A531H52
R206	RESISTOR 2.2K OHMS, ½ WATT, ±5%	184A763H35
R207	RESISTOR 15K OHMS, ½ WATT, ±5%	184A763H55
R208-R216	RESISTOR 33K OHMS, ½ WATT, ±5%	184A763H63
R209	RESISTOR 22K OHMS, ½ WATT, ±5%	184A763H59
R210-R211 R215	RESISTOR 10K OHMS, ½ WATT, ±5%	184A763H51
R212	RESISTOR 1.5K OHMS, ½ WATT, ±5%	184A763H31
R213	RESISTOR 68K OHMS, ½ WATT, ±5%	184A763H71
R214	POTENTIOMETER 50K OHMS	629A430H01
	* CHANNEL BD. (S# 201C013G01)	
D151-D152 D153	DIODE 1N457A	184A855H07
Z151-Z153	ZENER DIODE 1N3686B	185A212H06
Z152-Z154	ZENER DIODE 1N957B	186A797H06
Z155	ZENER DIODE UZ 5875	837A693H04
Z156	ZENER DIODE 1N3688A	862A288H01
Q151-Q152 Q153	TRANSISTOR 2N3417	848A851H02
Q154	TRANSISTOR 2N699	184A638H19
Q155	TRANSISTOR 2N3064	184A638H24
C151-C152	CAPACITOR 0.047 MFD., 200 VOLTS, ±5%	849A437H04
R151-R152 R157-R158	RESISTOR 4.7K OHMS, ½ WATT, ±2%	629A531H48
R153-R159	RESISTOR 82K OHMS, ½ WATT, ±2%	629A531H78
R154-R160	RESISTOR 10K OHMS, ½ WATT, ±2%	629A531H56
R155-R161	RESISTOR 6.8K OHMS, ½ WATT, ±2%	629A531H52
R156-R162	RESISTOR 22K OHMS, ½ WATT, ±5%	184A763H59
R163-R164	RESISTOR 10K OHMS, ½ WATT, ±5%	184A763H51

ELECTRICAL PARTS LIST

* CIRCUIT SYMBOL	CHANNEL BD. (S# 201C013G01) (CONTINUED) DESCRIPTION	WESTINGHOUSE DESIGNATION
R165-R166		
R167		
R168	RESISTOR 15K OHMS, 1 WATT, ±5%	187A643H55

CIRCUIT SYMBOL	ARMING BD. (S# 201C022G01) DESCRIPTION	WESTINGHOUSE DESIGNATION
D259-D260	DIODE 1N457A	184A855H07
D261-D263		
D264-D265		
Q254-Q255	TRANSISTOR 2N3417	848A851H02
Q256-Q258		
Q259		
Q257	TRANSISTOR 2N3645	849A441H01
R266-R267	RESISTOR 10K OHMS, ½ WATT, ±5%	184A763H51
R270-R271		
R275-R276		
R281-R282		
R284-R285		
R287-R288		
R268-R272	RESISTOR 22K OHMS, ½ WATT, ±5%	184A763H59
R273-R274		
R277-R278		
R283		
R279	RESISTOR 27K OHMS, ½ WATT, ±2%	629A531H66

CIRCUIT SYMBOL	OUTPUT BD. (S# 201C024G01) DESCRIPTION	WESTINGHOUSE DESIGNATION
D301-D302	DIODE 1N457A	184A855H07
D303-D304		
D305-D306		
D308		
D307	DIODE 1N645A	837A692H03
Z301-Z303	ZENER DIODE 1N957B	186A797H06
Z304-Z305		
Z306	ZENER DIODE 1N3688A	862A288H01
Q301-Q305	TRANSISTOR 2N3645	849A441H01
Q306-Q307		
Q309		
Q302-Q303	TRANSISTOR 2N3417	848A851H02
Q304-Q308		

ELECTRICAL PARTS LIST

C301	CAPACITOR 1.0 MFD., 35 VOLTS, ±10%	837A241H15
C302-C303 C306-C309	CAPACITOR 0.22 MFD., 50 VOLTS, ±10%	762A703H01
C305	CAPACITOR 4.7 MFD., 35 VOLTS, ±10%	184A661H12
C307-C308	CAPACITOR 0.047 MFD., 200 VOLTS, ±5%	849A437H04
C310	CAPACITOR 0.10 MFD., 200 VOLTS, ±10%	188A669H03
C311	CAPACITOR 1.5 MFD., 35 VOLTS, ±10%	187A508H09
R301-R303 R304-R306 R310-R311 R315-R320 R323-R324 R326-R330 R335	RESISTOR 10K OHMS, ½ WATT, ±5%	184A763H51
R302	RESISTOR 120K OHMS, ½ WATT, ±5%	184A763H77
R305	RESISTOR 47 OHMS, ½ WATT, ±5%	187A290H17
R307-R314 R319-R321 R325	RESISTOR 22K OHMS, ½ WATT, ±5%	184A763H59
R309-R317	RESISTOR 1K OHMS, ½ WATT, ±5%	184A763H27
R312	RESISTOR 470 OHMS, ½ WATT, ±5%	184A763H19
R313	RESISTOR 470K OHMS, ½ WATT, ±5%	184A763H91
R316	POTENTIOMETER 15K OHMS	629A430H08
R318-R322 R328	RESISTOR 4.7K OHMS, ½ WATT, ±5%	184A763H43
R327	RESISTOR 6.8K OHMS, ½ WATT, ±5%	184A763H47
R329	RESISTOR 18K OHMS, ½ WATT, ±5%	184A763H57
R331	RESISTOR 10K OHMS, ½ WATT, ±2%	629A531H56
R332	RESISTOR 6.8K OHMS, ½ WATT, ±2%	629A531H52
R333	RESISTOR 27K OHMS, ½ WATT, ±2%	629A531H66
R334	RESISTOR 150 OHMS, 3 WATT, ±5%	762A679H01

CIRCUIT SYMBOL	TEST BD. (S# 899C711G01) DESCRIPTION	WESTINGHOUSE DESIGNATION
S1	POTENTIOMETER 1K OHMS	185A086H28
S2	POTENTIOMETER 50K OHMS	185A086H22

CIRCUIT SYMBOL	CHASSIS MOUNTED COMPONENTS DESCRIPTION	WESTINGHOUSE DESIGNATION
Z1	ZENER DIODE 1N2984B	762A631H01
R1	RESISTOR 300 OHMS, 25 WATT, ±5%	1202847

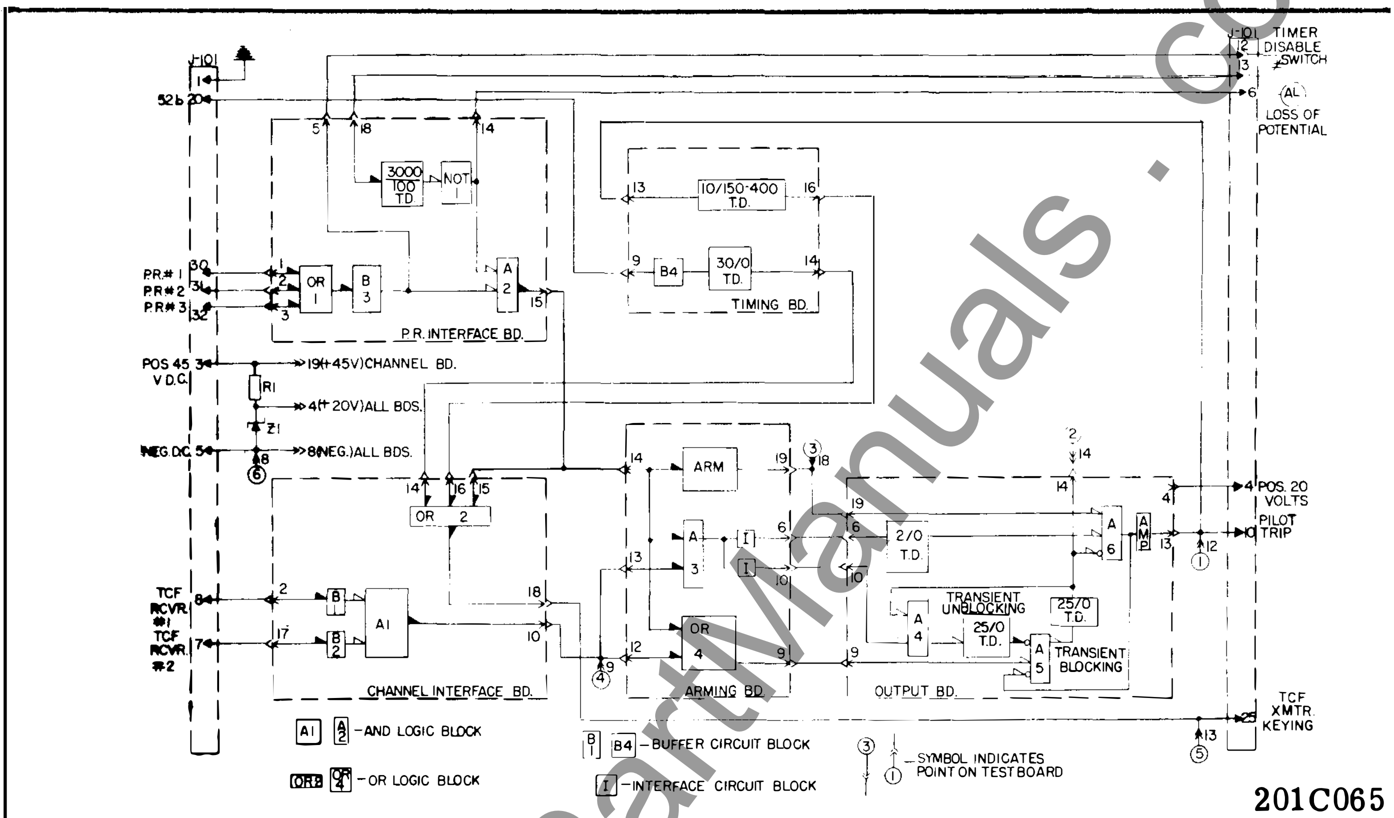


Fig. 2 Logic Block Diagram for the Type STU Relay

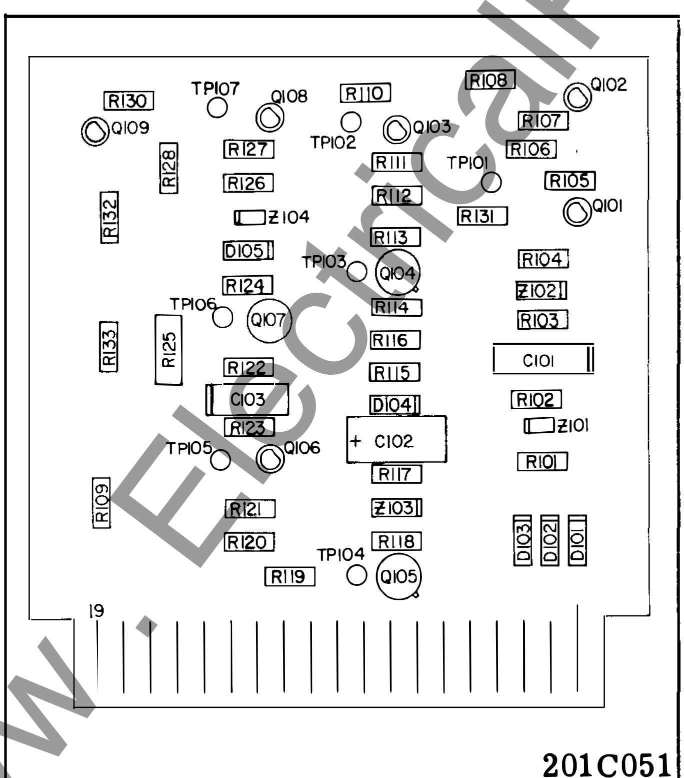


Fig. 3 Component Location of the Protective Relay Board for the Type STU Relay.

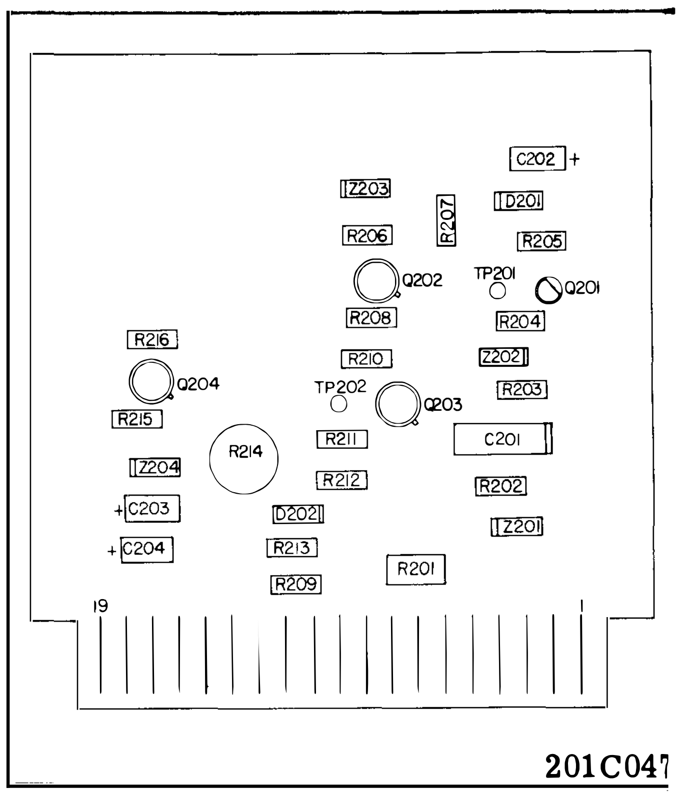
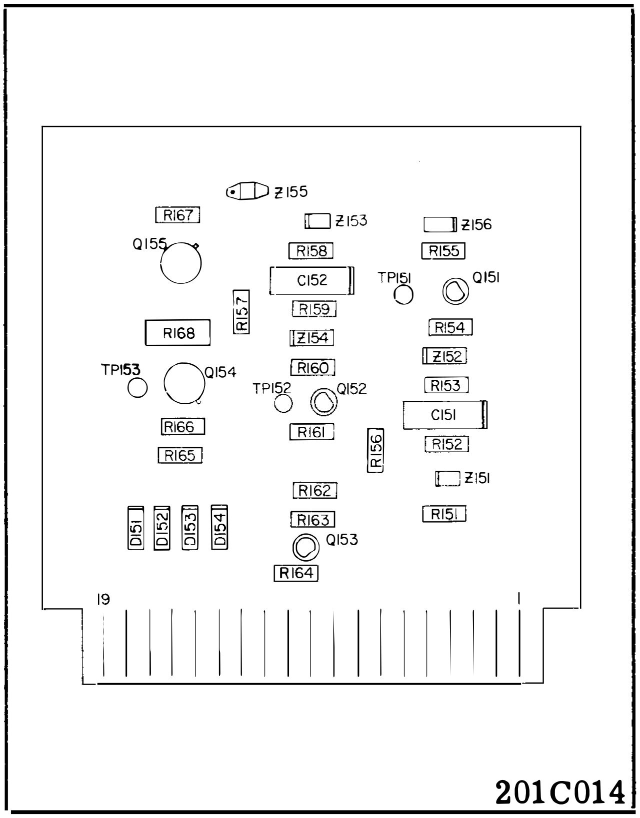


Fig. 4 Component Location of the Timing Board for the Type STU Relay.



* Fig. 5 Component Location of the Channel Board for the Type STU Relay.

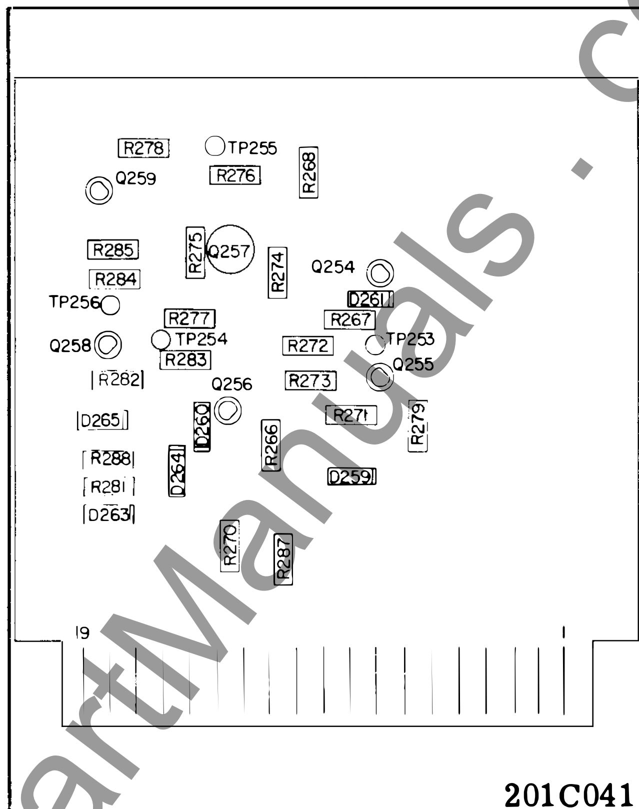


Fig. 6 Component Location of the Arming Board for the Type STU Relay.

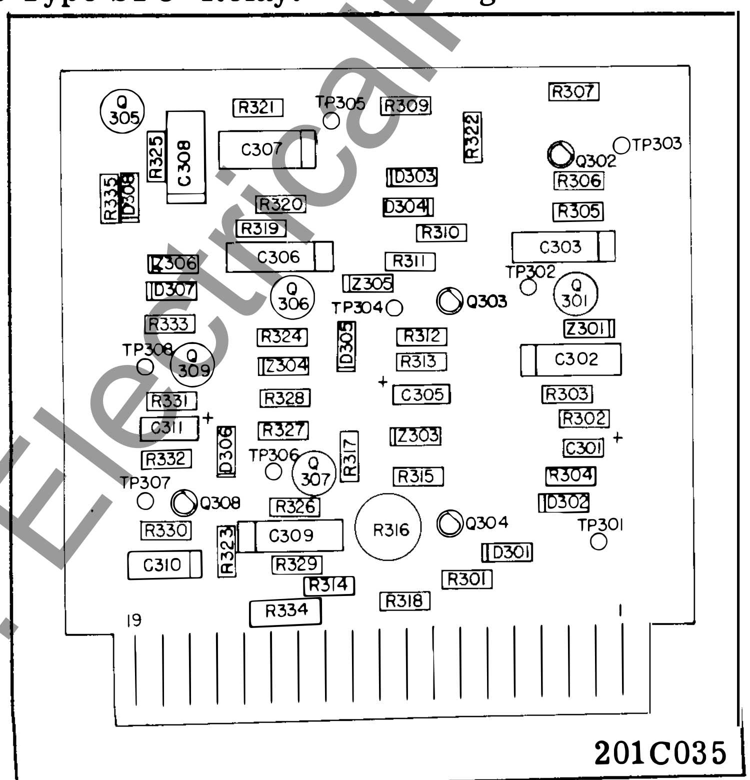
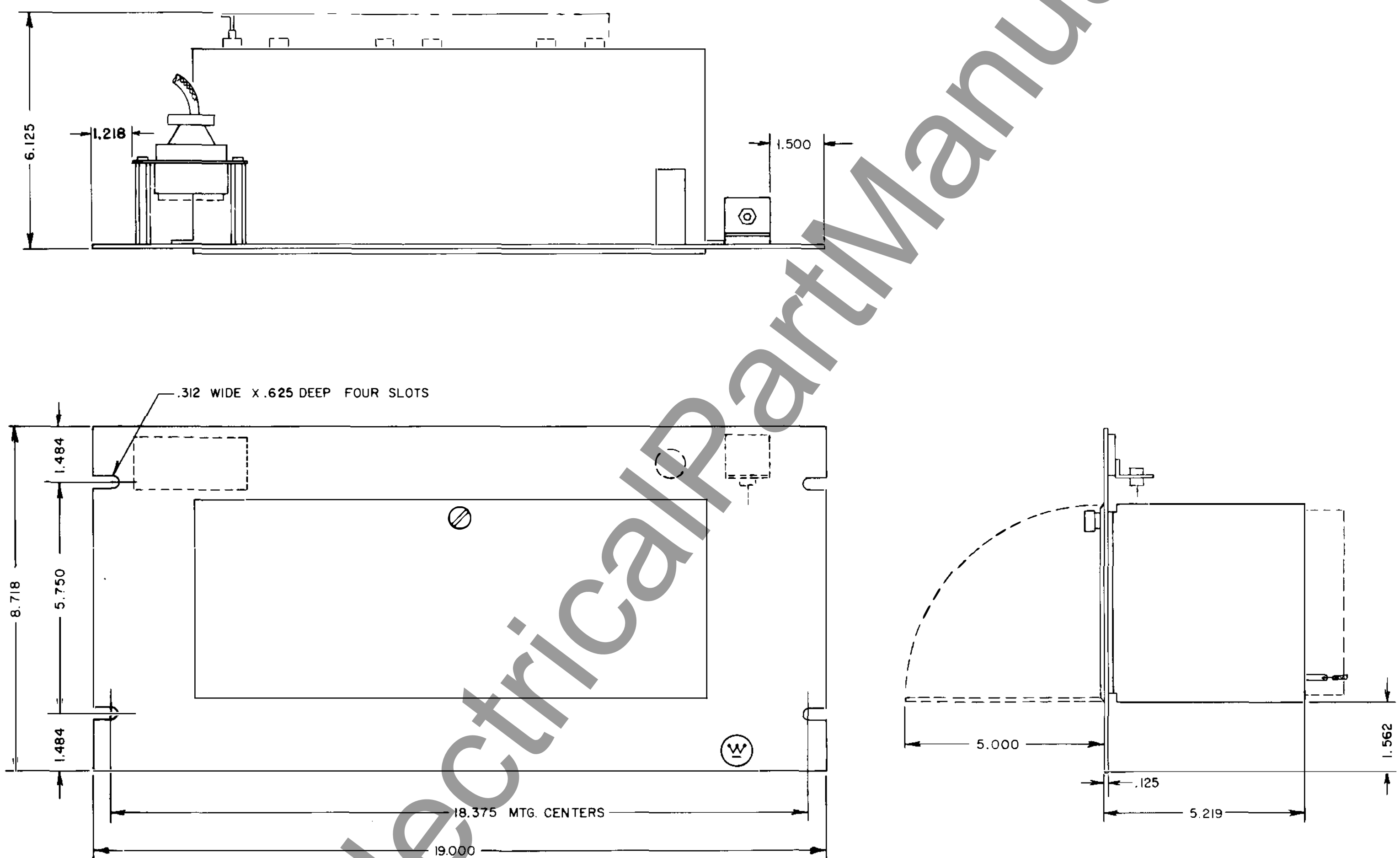


Fig. 7 Component Location of the Output Board for the Type STU Relay.



899C756

Fig. 8 Outline and Drilling Plan for the STU Relay.

WESTINGHOUSE ELECTRIC CORPORATION
RELAY-INSTRUMENT DIVISION **NEWARK, N. J.**
Printed in U.S.A.

INSTALLATION • OPERATION • MAINTENANCE

INSTRUCTIONS

TYPE STU UNBLOCK RELAY
FOR USE WITH SOLID STATE RELAY

CAUTION: It is recommended that the user of this equipment become thoroughly acquainted with the information in these instructions before energizing this relay. Failure to observe this precaution may result in damage to the equipment. If the equipment is mounted in a cabinet, the cabinet must be bolted down to the floor or otherwise secured before swinging out the equipment rack to prevent its tipping over.

APPLICATION

The type STU relay is a completely solid-state carrier unblock auxiliary relay for use with solid-state relays and a type TCF frequency shift channel to prevent tripping for faults external to the line section to which it is applied and to permit instantaneous and simultaneous tripping for internal faults. The relay is arranged to respond to indications of fault direction, distance and power provided by the phase and ground distance, and overcurrent relays thereby controlling the transmission of an unblocking or trip signal and the initiation of high speed tripping for internal faults. Either two or three terminal line applications may be used.

CONSTRUCTION

The STU relay is mounted on a standard 19" wide panel, 8-3/4" high (5 rack units) with edge slots for mounting on a standard relay rack or panel. All components not on printed circuit boards are mounted on the panel and extend to the rear. For the outline and drilling plan, refer to Fig. 8.

All of the circuitry suitable for printed circuit board mounting is contained in an enclosure that projects from the rear of the panel and is accessible by opening the door on the front. The dotted lines enclosing separate areas of Fig. 1 indicate that the components thus enclosed are all on the same printed circuit board.

The printed circuit boards slide into position in slotted guides at the top and bottom of the enclosure, and the board terminals engage a terminal block at the rear of the compartment. Each board and terminal block are keyed so that if a board is placed in the wrong compartment, it cannot be inserted into the terminal block. The printed circuit boards are labeled from left to right respectively: Protective Relay Interface, Timing, Channel, Arming, Output and Test.

NEW INFORMATION EFFECTIVE MARCH 1968

A board extender (Style No. 644B315G01) is available for facilitating circuit voltage measurements or major adjustments. After withdrawing any one of the circuit boards, the extender is inserted in that compartment. The board then is inserted into the terminal block on the front of the extender. This restores all circuit connections; and all components, test points and printed circuit terminals are readily accessible.

Most of the relay operates from a zener regulated 20 volts d-c supply (Z1 on Fig. 3) which is mounted on a heatsink at the rear of the panel. The 20 volt zener and a portion of the relay works from a 45 volt d-c input supply. External connections to the relay are made through a 32 terminal circuit receptacle, J101 in Fig. 1.

SYSTEM OPERATION

The type STU unblock relay is used in a directional unblock relay scheme for power line protection. High-speed tripping is obtained for two or three terminal line applications for faults anywhere in the protected line. The signals to which the STU relay responds are obtained from the receiver of the TCF frequency shift channel and the output of the local protective relays.

Since distance relays may operate on a loss of a-c potential, the STU relay provides alarm and lockout of tripping 3000 milliseconds after this condition occurs. The 3000/100 MS timer picks up and the output from NOT 1 drops out an AL loss of potential alarm mounted elsewhere in the relaying system. This also prevents output from A 2 since there is no signal from NOT 1.

The output of A 2 initiates keying of the local transmitter through operation of OR 2, by shifting the transmitter from the blocking frequency to the unblocking or trip frequency. In 10 milliseconds after a primary pilot trip operation, the 10/150-400 millisecond timer picks up and also maintains the unblocking frequency keying for 150 to 400 milliseconds after a loss of the trip signal. This time is adjustable to allow for the breaker failure timer setting at the remote terminal.

In addition, the 52b contact initiates the trip frequency transmission 30 milliseconds after the local circuit breaker opens and until such time as the circuit breaker is reclosed. The 30/0 millisecond timer delays the transmission of trip frequency to obtain coordination for bus fault tripping of the local circuit breaker where tripping of the remote breaker would be incorrect and might cause undesired interruption to tapped transformer terminals. Transmission of the trip or unblocking frequency is necessary to permit tripping of the remote terminal should the remote circuit breaker be closed into a fault or should a fault develop in the protected line while the local circuit breaker is open.

Internal Fault

The operation of any or all the protective relays PR-1, PR-2 or PR-3 for an Internal Fault perform the following (refer to the block diagram, Fig. 4):

1. Energizes the 3 second timer and A2 thereby giving an output from A2 for up to 3 seconds.

2. "Arms" A6 or puts it in a "ready" condition for up to 3 seconds by removing a blocking bias voltage.

3. Energize the transient blocking circuit at OR 4 up to 3 seconds.

4. Key the TCF transmitter for 3 seconds through OR 2 to shift the frequency from a blocking to an unblocking or trip condition.

For an internal fault, the TCF Receivers will produce a "1" output unblock signal to energize A1 thereby producing a "1" input from the channel to A3. This together with the signal from PR-1, PR-2 or PR-3 at A3 will cause tripping 2 milliseconds later. This operation will be completed before the transient blocking becomes effective.

External Fault

If no unblocking or trip signal is received from the remote terminal when PR-1, PR-2, or PR-3 operates (as for an External Fault), there will be no tripping output from A1. If tripping does not take place within 25 milliseconds after the protective relays operate, the transient blocking circuit energized through OR 4 will desensitize A6 to prevent possible undesired tripping during transients occurring at the clearing (elsewhere) of an external fault.

The above procedure also holds true if the TCF unblocking or trip signals are received from the remote terminals and the protective relays do not operate. This also is an external fault.

Sequential Faults

Occasionally an External Fault will be followed by an internal fault before the former is cleared. In order to prevent a long delay in clearing such an internal fault, a "transient unblocking" feature is included. Although transient blocking has been set up by the initial external fault, the presence of an Internal Fault will cause an output from A3 which will energize the transient unblocking circuit. After 25 milliseconds, A6 will be resensitized and tripping will be permitted.

RELAY OPERATION

The complete detailed relay circuit is shown on the internal schematic, Fig. 1. The operation of the logic elements shown on Fig. 2, and the individual circuit components will be described in the following paragraphs.

Protective Relay Interface Board

The Protective Relay printed circuit board contains the required circuits for interface with the protective relays, PR-1, PR-2 and PR-3, These logic blocks are the protective relay input OR 1 and its associated Buffer B3, for surge protection, the 3000/100 millisecond time delay for loss of a-c potential, and A2.

Under normal conditions, J101 terminals 30, 31 and 32, the inputs to the STU relay from PR-1, PR-2 and PR-3 respectively, are held at negative (zero volts) thereby holding transistor Q101, the output of B3, non-conductive. With Q101 off, transistors Q102 and Q109 have base drive holding them both conductive. Since Q109 is turned on, this represents a "0" output from A2. Transistor Q107 is normally on representing a "1" signal from NOT 1 to the AL loss of potential alarm elsewhere in the relaying system.

When one or more of the protective relays, PR-1, PR-2 or PR-3 operate and positive 20 volts d-c is applied to J101 terminals 30, 31 or 32, then transistor Q101 will conduct and immediately turn off Q102 and Q109. Transistor Q109 is the output stage of A2, and for A2 to assume a "1" output, both transistors Q101 (output of buffer B3) and Q108 (output of NOT 1) must be conducting thereby holding Q109 non-conductive. Therefore, immediately following reception of a protective relay "1" signal, A2 will yield a "1" output.

Transistors Q102 to Q105 are associated with the 3000/100 millisecond time delay, and Q106 to Q108 with NOT 1. Normally, transistors Q102, Q104, Q107 and Q108 are conducting and Q103 and Q105 non-conductive. Therefore, capacitor C102 in the three (3) second timer is fully discharged through transistor Q104. Since Q108 is conducting, this represents a "1" input to A2 from NOT 1.

Since distance relays may operate on loss of a-c potential, the 3000/100 millisecond timer provides alarm and blocks A2 three (3) seconds after loss of primary protection and blown a-c potential fuse. As mentioned above, output from any or all the protective relays turns off transistor Q102. Therefore, providing the timer disable switch between J101 terminals 12 and 13 is closed, transistor Q103 has base drive to cause it to conduct and turn off transistor Q104. When this occurs, capacitor C102 will begin to charge from positive 20 volt d-c through resistors R114 and R116 and, in 3000 milliseconds, reaches a sufficient potential to breakdown zener diode Z103 and cause transistor Q105 to conduct. With Q105 conducting, base drive is removed from transistors Q106 and Q108 to make them non-conductive. Therefore, with Q108 off, the "1" input from NOT 1 becomes a "0" and blocks A2. In addition, since Q106 is off, no base drive is available for Q107 so it becomes non-conductive and provides a "0" signal to the AL alarm for indication of loss of a-c potential. Upon loss of the protective relay signal, transistor Q104 will turn on and permit capacitor C102 to discharge in 100 milliseconds below the breakdown of zener diode Z103 and turn off transistor Q105.

Timing Board

The Timing printed circuit board contains two time delays necessary for proper operation of the relaying system: one, the 30/0 millisecond timer used for coordination with bus fault and remote breaker tripping; and, two, the 10/150-400 millisecond signal continuing timer used for coordination with the breaker failure timer.

Under normal conditions, transistor Q201, the output of Buffer circuit B4, and the input to the 30/0 timer, is non-conductive thereby preventing a path for base current to turn on transistor Q202. As a result, printed circuit terminal #14 is held at negative (zero volts) representing a "0" output from this timer.

After the local circuit breaker opens, positive 125 volt d-c is applied through the now closed 52b contact to J101 terminal No. 20. When this occurs, transistor Q201 has base drive and immediately becomes conductive. As a result, capacitor C202 starts charging to negative through resistor R207 and the collector-emitter circuit of Q201, and in 30 milliseconds, C202 assumes a low enough potential below positive 20 Vdc to breakdown zender diode Z203 and provide a path for base drive to make transistor Q202 conductive. Therefore, with Q202 conducting, this represents a "1" signal to OR 2 to shift the transmitter from a blocking to an unblocking or trip frequency. Upon breaker reclosing, the 52b contact opens turning transistor Q201 off thus permitting capacitor C102 to rapidly discharge for immediate dropout.

The 10/150-400 millisecond time delay operates similar to the 30/0 MS timer. After a primary pilot trip operation, capacitors C203 and C204 will charge in milliseconds through diode D202, resistor R212 and the collector-emitter circuit of transistor Q203 to a low enough potential to cause breakdown of zener diode Z204 and conduction of transistor Q204. Once Q204 turns on, a "1" signal to OR 2 keys the transmitter to the trip frequency for the duration of the pilot trip signal. After loss of the pilot trip signal, capacitors C203 and C204 will discharge in 150 to 400 milliseconds (adjustable by resistor R214) and turn Q204 off. This 150 to 400 MS dropout time holds the unblocking or trip frequency on to provide coordination with the breaker failure timer. Normal dropout time is factory calibrated at 300 milliseconds.

Channel Interface Board

The channel printed circuit board contains A2 and its associated Buffers B1 and B2 for interface with the TCF Receiver, and OR 2 for interface with the TCF Transmitter.

Under normal conditions and for three-terminal line applications, both J101 terminals 8 (TCF RCVR-1) and 7 (TCF RCVR-2) are held at negative (zero volts) thereby allowing no base drive for transistors Q151 and Q152 thus holding them non-conductive. As a result, transistor Q153 has base drive, so it is normally conducting and represents a "0" output from A1.

When both of the TCF Receivers receive the unblocking or trip frequency from the other terminals, they will produce a positive 20 Vdc potential at J101 terminals 8 and 7. When this occurs, both transistors Q151 and Q152 have base drive and start conducting. In turn, with both Q151 and Q152 on, base drive is removed from transistor Q153 which them stops conducting and represents a "1" output signal from A1. If only one of the TCF Receivers yield a trip output, then transistor Q153 still will receive base drive from the other input transistor in the STU and a "0" signal will be received from A1.

In the case of two-terminal line applications, either J101 terminal 8 or 7 must be connected to J101 terminal 4 to simulate having a constant signal of "1" at one of the A1 inputs. Under this condition, transistor Q153 will still be normally conducting thus representing a "0" output from A1. When the J101 terminal (either 8 or 7) not connected to J101 terminal 4 receives a positive 20 Vdc signal from the TCF, transistor Q153 will lose its base drive and turn off to produce a "1" output from A1.

Under normal conditions, the inputs to OR 2 printed circuit terminals #14, 15 and 16 on the Channel Board are held at negative (0 volts) thereby preventing any base drive from turning on transistors Q154, and thus Q155. When one or more of these printed circuit terminals receive a positive d-c signal, "1", base drive will turn on transistor Q154 which in turn will make transistor Q155 conduct and apply positive 45 Vdc to the TCF transmitter to cause it to shift from the block to the unblock or trip frequency. As can be seen from Fig. 2, in order for the TCF transmitter to be keyed, OR 2 must receive a positive going "1" signal from A2, the 30/0 timer or the 10/150-400 timer.

Arming Board

The Arming printed circuit board contains the logic blocks which combine the information from the protective relays and the channel receiver and in turn provides the proper interfaces for this information to be translated to the Output Board for transient block, arm, transient unblock and pilot trip.

Normally, there is a "0" signal to OR 4 from A1 (printed circuit terminal #12) and from A2 (printed circuit terminal #14) thereby resulting in a "0" signal at printed circuit terminal #9, the output of OR 4. When either or both A1 and A2 yield a "1" output signal to the inputs of OR 4, current is allowed to flow through resistor R287 and diode D264 (for an A1 output) or resistor R288 and diode D265 (for an A2 output). In this case, therefore, a "1" is received from OR 4 to energize the transient block circuitry in the Output Board.

Likewise, both inputs into A3 are normally "0". The input transistors of A3 are Q255 for A1 and Q254 for A2. Normally both Q255 and Q254 have no base drive and, as a result, they are both non-conductive. Therefore, the output transistor of A3, Q256, has base drive and is turned on thus allowing Q254 to conduct and provide a proper interface with the Output Board. If a "1" signal is received from both A1 and A2, then both transistors Q255 and Q254 become conductive thereby removing base drive to Q256 to turn it off. This causes Q257 to stop conducting and allow the 2/0 timer and the transient unblock circuits in the Output Board to function. If either Q255 or Q254 remains non-conductive, then transistor Q257 will stay on and a "0" output will be received from A3.

The Arm circuit is energized from A2 and under normal conditions with a "0" output from A2, there is no base drive from transistor Q258, so it is non-conductive. As a result, with Q258 off, base drive holds transistor Q259 conducting thereby keeping the Output Board "disarmed". As soon as A2 assumes a "1" output state, base drive turns transistor Q258 on and thereby Q259 turns off and arms A6 on the Output Board.

Output Board

The Output Board contains all the logic required for final tripping, transient blocking and transient unblocking. In reference to Fig. 2, a "1" signal from OR 4 represents a transient blocking signal. A "1" output from A3 is a pilot tripping signal in two milliseconds but prior to tripping, it is a transient unblocking signal in the event that transient blocking has already occurred.

The 2/0 millisecond time delay circuit is used to prevent tripping from improper signals of short duration. Normally, printed circuit terminal #6 is held at positive 20 Vdc thereby preventing capacitor C306, associated with the

2/0 MS timer, from charging. Under conditions for tripping, transistor Q257 in A3 (Arming Board) will turn off and allow capacitor C306 to charge to negative through resistors R318 (Output Board) and R279 (Arming Board). After the factory calibrated time (by S1) of two milliseconds, the voltage across C306, which is applied to the base emitter circuit of transistor Q305 in A6, is sufficient to cause Q305 to operate and thereby turn transistor Q306 off providing it is armed.

The 2/0 millisecond timer has no intentional reset time delay. If a tripping condition is indicated for some time less than two (2) milliseconds, such as during a reversal of fault power flow, as soon as transistor Q257 in A3 again conducts, capacitor C306 will rapidly discharge through the collector emitter circuitry of Q257, diode D261 and resistor R318. This rapid resetting of the 2/0 timer prevents possible "notching up" of the charge on C306 during momentary and intermittent interruptions under normal conditions.

The A6 circuit block consists of transistors Q305 and Q306 and the associated components. Under normal conditions, transistor Q305 is non-conducting and Q306 fully conducting. The base of Q306 is held well below its emitter potential by means of the arming circuitry voltage divider consisting of resistors R324, R335, diode D308 and transistor Q259. With this bias, transistor Q306 is held in saturation and is desensitized so that even if a tripping voltage were applied to Q305, transistor Q306 would not turn off. This desensitizing circuit is an arrangement to prevent inadvertent operation of A6 caused by surges on the d-c system. As long as Q306 is conducting, its collector is at a high enough potential above negative d-c so that transistor Q307 in the tripping amplifier cannot turn on.

Upon occurrence of an internal fault, transistor Q259 in the Arming Board turns off thereby removing the desensitizing bias from Q306 by open-circuiting the path of current through diode D308 and resistor R335. This causes A6 to become "armed" and in a ready condition for a tripping operation. After a two (2) millisecond time delay, the potential across capacitor C306 is sufficient to cause Q305 to conduct and thus turn off Q306. When Q306 is no longer conducting, the potential of its collector circuit drops to a relatively low value and allows sufficient voltage to appear across the base-emitter circuit of transistor Q307 in the trip amplifier, causing it to become conductive. In turn, transistors Q308 and Q309 turn on and apply a pilot trip voltage output.

The transient blocking circuit is energized only when there is an output from OR 4. An output from OR 4 consists of a positive potential which immediately turns on transistor Q302 thus dropping its collector potential (at TP 303) to a very low value. Therefore, the positive voltage is removed from the base of transistor Q303 turning it off. When this occurs, capacitor C305 charges in 25 milliseconds to a potential which is sufficient to cause the breakdown of zener diode Z303 and provide a path for base current to turn on transistor Q304. With Q304 on, a conducting path through resistors R324, R323, diode D306 and the collector-emitter circuit of Q304 is provided in order to hold a desensitizing bias on transistor Q306 in A6. Thus, the transient blocking circuitry allows 25 milliseconds after the operation of either a protective relay or the reception of a TCF trip signal for a "1" to be received from A6. If tripping does not occur in this time, as during an external fault, operation of the transient blocking circuit will hold A6 desensitized in order to prevent undesirable operation during transients associated with power reversals on the protected line or at the clearing of an external fault.

If an internal fault occurs before the external fault is cleared, it is desirable to obtain high-speed tripping. The transient unblocking circuitry permits this since transistor Q257 in A3 will turn off and remove the positive 20 Vdc potential on printed circuit terminal #10. This allows capacitor C301 to charge to negative through diode D301, resistor R314 and the collector-emitter circuit of transistor Q304, which has been turned on due to transient blocking. In 25 milliseconds, C301 will charge to a sufficient potential to turn on transistor Q301 and permit base drive for transistor Q303. This will immediately turn on Q303 which allows a path for rapid discharge of capacitor C305. When this occurs, zener diode Z303 will not breakdown, and Q304 will stop conducting thereby interrupting the desensitizing circuit from the base of transistor Q306. Therefore A6 will be able to assume a "1" output and provide tripping after a delay of only 25 milliseconds.

Test Board

The Test Board contains two potentiometers, S1 and S2, used for factory time delay adjustments. Also, six test points are easily accessible from the front of this board for facilitating system tests of the STU Relay.

Potentiometer S1 is the 2/0 millisecond time delay adjustment, and S2 is the 25/0 transient unblocking time delay adjustment. These potentiometers are used only for factory calibration of the STU Relay.

Listed below are the six test points on the Test Board. Test points 1 to 5 are red, and test point 6 is black.

1. Pilot Trip
2. Transient Block
3. Arm - Received Protective Relay
4. Received Channel
5. Transmitter Key
6. Negative DC

CHARACTERISTICS

Input Voltage	45 volts D-C
Current Drain	100 milliamperes maximum
Pilot Trip Output	10 milliamperes at positive 20 Vdc
Min. Operate Time	2 milliseconds
Keying Voltage	Positive 45 volt D-C
Blown A-C Fuse Detection Timer	3 seconds
Ambient Temperature Range	-20°C to +55°C around chassis

Dimensions	panel height: 8-3/4" or 5 R.U. panel width: 19" panel depth: 6"
Weight	approximately 9 pounds

SETTINGS

Normally, there are no settings to be made on the STU unblock relay. All various time delay circuits are factory adjusted to the stated time in Fig. 2. However, if conditions require, the dropout time of the 10/150-400 millisecond timer may be changed from the factory setting of 300 MS to any value between 150 and 400 MS as explained under the Calibration section.

INSTALLATION

The STU Relay is generally supplied on a relay rack as part of a complete relay system assembly. The location must be free from dust, excessive humidity, vibration, corrosive fumes or heat. The maximum ambient temperature around the chassis must not exceed 55°C.

The outline and drilling plan of the STU Relay is shown in Fig. 8.

ADJUSTMENT AND MAINTENANCE

A. Acceptance Test

The operation of the STU Unblock Relay can be checked by taking voltage measurements at the six (6) test points on the Test Board. Energize the STU Relay with 45 Vdc and measure the positive d-c voltages on test points 1 to 5 with respect to negative d-c, test point 6, under the following conditions:

Note: In reference to Fig. 1, use the timer disable switch (between J101 terminals 12 and 13) closed unless otherwise noted in tests below.

1. Normal Condition.	Test Point 1 - 0 Vdc Test Point 2 - 19 Vdc Test Point 3 - less than 0.5 Vdc Test Point 4 - less than 0.5 Vdc Test Point 5 - 0 Vdc
2. Protective Relay Operation. (Open timer disable switch) (Apply positive 20 Vdc to J101 terminal 30)	Test Point 1 - 0 Vdc Test Point 2 - less than 0.5 Vdc Test Point 3 - 19 Vdc Test Point 4 - less than 0.5 Vdc Test Point 5 - 45 Vdc
3. Channel Receiver Operation. (Apply positive 20 Vdc to J101 terminals 8 and 9)	Test Point 1 - 0 Vdc Test Point 2 - less than 0.5 Vdc Test Point 3 - less than 0.5 Vdc Test Point 4 - 7 Vdc Test Point 5 - 0 Vdc

4. Protective Relay and Channel Operation. (Apply pos. 20 Vdc to J101 terminals 8 and 9. Then apply pos. 20 Vdc to J101, terminal 30)

Test Point 1 - immed. 20 Vdc, in 3 sec. 0 Vdc

Test Point 2 - immed. 19 Vdc, in 3 sec. less than 0.5 Vdc

Test Point 3 - immed. 19 Vdc, in 3 sec. less than 0.5 Vdc

Test Point 4 - immed. 7 Vdc, in 3 sec. 7 Vdc

Test Point 5 - immed. 45 Vdc, in 3 sec. 0 Vdc

B. Recommended Routine Maintenance

Periodic checks of the relaying system are desirable to indicate impending failure so that the equipment can be taken out of service for correction. Any accumulated dust should be removed at regular maintenance intervals.

The proper adjustments to insure correct operation of this relay have been made at the factory and should not be disturbed after receipt by the customer. If the adjustments or if the components or printed circuit boards which affect calibration have been changed, then recalibration per the Calibration section following will have to be made on the circuits in question.

C. Calibration

1. 10/150-400 T.D. (Timing Board)

The dropout of the 10/150-400 millisecond signal continuing timer may be adjusted from 150 to 400 MS to allow for various settings of the breaker failure timer. By comparing the Pilot Trip voltage of the relay with the timer output voltage at printed circuit terminal 16 (Timing Board) under dropout conditions, the time delay between a change of the input voltage and the output voltage can be adjusted from 150 to 400 milliseconds. For more dropout time, potentiometer R214 on the Timing Board should be turned clockwise, and for less time it should be turned counter-clockwise. Factory setting of the dropout time is 300 milliseconds. Pickup time can be calibrated in the same manner except for more time, increase resistor R212 and for less time, decrease R212. Pickup time should be 10 milliseconds. Location of potentiometer R214 and resistor R212 can be seen on the Timing Board component location, Fig. 4.

2. 30/0 T.D. (Timing Board)

The pickup time of the 30/0 millisecond timer can be calibrated by comparing the input voltage to Buffer B4 with the output voltage at printed circuit terminal 14, Timing Board, under pickup conditions. Pickup time should be 30 milliseconds. Increase resistor R207 (Timing Board) for more time or decrease R207 for less time. Location of resistor R207 can be seen in Fig. 4.

3. 3000/100 T.D. (P. R. Interface Board)

The 3000/100 millisecond time delay can be calibrated by comparing the time duration for a voltage change between the timer input, the output of Buffer B3, and the timer output, printed circuit terminal 14 (P. R. Interface Bd.) under pickup and dropout conditions. Normal pickup time is 3000 milliseconds. For more pickup time, increase resistor R116 and for less time, decrease R116. Dropout time can be calibrated by using a higher value of resistor R115 for more time or a lower value for less time. Normal dropout calibration time is 100 milliseconds. Location of resistors R115 and R116 can be seen on the Protective Relay Board component location, Fig. 3.

4. 2/0 MS Timer (Output Board)

In order to calibrate the 2/0 millisecond time delay, connect a jumper across capacitor C305 on the Output Board. Then compare the voltage at test point TP 255 on the Arming Board with the voltage at test point TP 306 on the Output Board under a trip condition. If the time delay between a change in both voltages is not two milliseconds, turn potentiometer S1 on the Test Board clockwise for more time and counter-clockwise for less time. Location of components and test points may be seen in Figs. 6 and 7. After calibration, remove the jumper from capacitor C305 and insure that the locking clamp on S1 is tight.

5. Transient Unblocking 25/0 Time Delay (Output Board)

In order to calibrate the transient unblocking time delay, the STU Relay must be in a transient block state. After putting the relay in a block state, compare the voltage at test point TP 255, Arming Board, with the voltage at Test Point 1, Test Board. If the time delay between a voltage change at the input (TP 255) and output (TP 1) is not 25 milliseconds, then turn potentiometer S2 (Test Board) clockwise for more time and counter-clockwise for less time. Location of TP 255 can be seen in Fig. 6, Arming Board component location.

6. Transient Blocking 25/0 Time Delay (Output Board)

To calibrate the transient blocking time delay, compare the voltage at test point TP 303 on the Output Board with test point 2, Test Board. Apply a transient block signal and if the time delay between a voltage change at the input (TP 303) and output (Test Point 2) is not 25 milliseconds, then turn potentiometer R316 clockwise for more time and counter-clockwise for less time. Location of the potentiometer R316 and test point TP 303 can be seen in Fig. 7.

D. Electrical Checkpoints - Trouble Shooting

The components of the STU Unblock Relay are operated well within their ratings and normally will give long and trouble-free service. However, if a relay has given indication of trouble in service or during routine checks, the voltages tabulated in Table I should be checked to determine the faulty circuit.

Test point voltages for the P. R. Interface, Timing, Channel, Arming, Output and Test printed circuit boards in the STU Unblock Relay are listed in Table I under various system conditions. The exact values will vary from one relay to another but, in general, will be within ±10% between relays. A Board Extender is helpful in checking test point voltages.

RENEWAL PARTS

Repair work can be done most satisfactorily at the factory. However, interchangeable parts can be furnished to the customers who are equipped for doing repair work. When ordering parts, always give the complete nameplate data and identify the part by its designation on the internal schematic drawing Fig. 1, as well as all information in the Electrical Parts List.

TABLE I

ELECTRICAL CHECKPOINTS - TROUBLE SHOOTING VOLTAGES

All test point voltages are positive D-C taken with respect to negative, Test Point No. 6 on the Test Board

TEST POINTS	NORMAL STAND-BY	TEST CONDITIONS PROTECTIVE RELAY OPER. (3 SEC. TIMER DISABLED)	PROTECTIVE RELAY & CHANNEL RCVR. OPER. (3 SEC. TIMER DISABLED)	PROTECTIVE RELAY & CHANNEL RCVR. OPER. (3 SEC. TIMER USED) (VOLTAGES AFTER 3 SEC)
PROTECTIVE RELAY BD.				
TP 101	12.5 Vdc	less than 0.5	less than 0.5	less than 0.5
TP 102	6.5	6.5	6.5	less than 0.5
TP 103	less than 0.5	less than 0.5	less than 0.5	17
TP 104	6	6	6	less than 0.5
TP 105	less than 0.5	less than 0.5	less than 0.5	20
TP 106	20	20	20	0
TP 107	less than 0.5	less than 0.5	less than 0.5	9
PCT -5	less than 0.5	20	20	6.5
PCT -15	less than 0.5	7	7	less than 0.5
TIMING BD.				
TP 201	20	20	20	20
TP 202	20	20	less than 0.5	20
PCT -14	0	0	0	20
PCT -16	0	0	20	0
CHANNEL BD.				
TP 151	15	15	less than 0.5	less than 0.5
TP 152	15	15	less than 0.5	less than 0.5
TP 153	45	less than 0.5	less than 0.5	45
PCT -10	less than 0.5	less than 0.5	7	7
PCT -18	0	45	45	0

- PCT INDICATES PRINTED CIRCUIT TERMINAL

TABLE I (CONT.)

TEST POINTS	TEST CONDITIONS NORMAL STAND-BY	PROTECTIVE RELAY OPER. (3 SEC. TIMER DISABLED)	PROTECTIVE RELAY & CHANNEL RCVR. OPER. (3 SEC. TIMER DISABLED)	PROTECTIVE RELAY & CHANNEL RCVR. OPER. (3 SEC. TIMER USED) (VOLTAGES AFTER 3 SEC.)
<u>ARMING BD.</u>				
TP 253	10	10	less than 0.5	less than 0.5
TP 254	less than 0.5	less than 0.5	20	less than 0.5
TP 255	20	20	0	20
TP 256	6.5	less than 0.5	less than 0.5	6.5
PCT -1	10	less than 0.5	less than 0.5	10
PCT -19	less than 0.5	19	19	less than 0.5
<u>OUTPUT BD.</u>				
TP 301	20	20	20	20
TP 302	0	0	0	0
TP 303	2	less than 0.5	less than 0.5	less than 0.5
TP 304	2	7.5	2	7.5
TP 305	19	19	5.5	19
TP 306	0	0	13	0
TP 307	20	20	less than 0.5	20
TP 308	0	0	20	0
PCT -14	19	less than 0.5	19	less than 0.5
<u>TEST BD.</u>				
TEST PT. - 1	0	0	20	0
TEST PT. - 2	19	less than 0.5	19	less than 0.5
TEST PT. - 3	less than 0.5	19	19	19
TEST PT. - 4	less than 0.5	less than 0.5	7	7
TEST PT. - 5	0	45	45	0
TEST PT. - 6	0 (REF)	0 (REF)	0 (REF)	0 (REF)

ELECTRICAL PARTS LIST

CIRCUIT SYMBOL	PROTECTIVE RELAY INTERFACE BD. (S# 201C050G01) DESCRIPTION	WESTINGHOUSE DESIGNATION
D101-D102 D103-D105	DIODE 1N645A	837A692H03
D104	DIODE 1N457A	184A855H07
Z101	ZENER DIODE 1N3686B	185A212H06
Z102-Z103	ZENER DIODE 1N957B	186A797H06
Z104	ZENER DIODE 1N3688B	862A288H01
Q101-Q102 Q103-Q106 Q108-Q109	TRANSISTOR 2N3417	848A851H02
Q104-Q105	TRANSISTOR 2N697	184A638H18
Q107	TRANSISTOR 2N3645	849A441H01
C101	CAPACITOR 0.047 MFD., 200 VOLTS, ±5%	849A437H04
C102	CAPACITOR 68 MFD., 35 VOLTS, ±20%	187A508H02
C103	CAPACITOR 0.27 MFD., 200 VOLTS, ±10%	188A669H05
R101-R102	RESISTOR 4.7K OHMS, ½ WATT, ±2%	629A531H48
R103	RESISTOR ·82K OHMS, ½ WATT, ±2%	629A531H78
R104-R122	RESISTOR 10K OHMS, ½ WATT, ±2%	629A531H56
R105-R123	RESISTOR 6.8K OHMS, ½ WATT, ±2%	629A531H52
R106-R108 R111-R114 R131	RESISTOR 22K OHMS, ½ WATT, ±5%	184A763H59
R107-R109 R110-R112 R113-R117 R118-R120 R121-R126 R127-R130 R132	RESISTOR 10K OHMS, ½ WATT, ±5%	184A763H59
R115	RESISTOR 6.8K OHMS, ½ WATT, ±5%	184A763H47
R116	RESISTOR 56K OHMS, ½ WATT, ±5%	184A763H69
R119-R128	RESISTOR 12K OHMS, ½ WATT, ±5%	184A763H53
R124	RESISTOR 27K OHMS, ½ WATT, ±2%	629A531H66
R125	RESISTOR 150 OHMS, 3 WATT, ±5%	762A679H01
R133	RESISTOR 4.7K OHMS, ½ WATT, ±5%	184A763H43

· - INDICATES TYPICAL VALUE

ELECTRICAL PARTS LIST

CIRCUIT SYMBOL	TIMING BD. (S# 201C046G01) DESCRIPTION	WESTINGHOUSE DESIGNATION
D201-D202	DIODE 1N457A	184A855H07
Z201	ZENER DIODE 1N3686B	185A212H06
Z202-Z203 Z204	ZENER DIODE 1N957B	186A797H06
Q201	TRANSISTOR 2N3417	848A851H02
Q202-Q203	TRANSISTOR 2N1132	184A638H20
Q204	TRANSISTOR 2N697	184A638H18
C201	CAPACITOR 0.047 MFD., 200 VOLTS, ±5%	849A437H04
C202	CAPACITOR 4.7 MFD., 35 VOLTS, ±10%	184A661H12
C203-C204	CAPACITOR 6.8 MFD., 35 VOLTS, ±5%	184A661H21
R201	RESISTOR 68K OHMS, 1 WATT, ±5%	187A643H71
R202	RESISTOR 4.7K OHMS, ½ WATT, ±2%	629A531H48
R203	RESISTOR 82K OHMS, ½ WATT, ±2%	629A531H78
R204	RESISTOR 10K OHMS, ½ WATT, ±2%	629A531H56
R205	RESISTOR 6.8K OHMS, ½ WATT, ±2%	629A531H52
R206	RESISTOR 2.2K OHMS, ½ WATT, ±5%	184A763H35
R207	RESISTOR 15K OHMS, ½ WATT, ±5%	184A763H55
R208-R216	RESISTOR 33K OHMS, ½ WATT, ±5%	184A763H63
R209	RESISTOR 22K OHMS, ½ WATT, ±5%	184A763H59
R210-R211 R215	RESISTOR 10K OHMS, ½ WATT, ±5%	184A763H51
R212	RESISTOR 1.5K OHMS, ½ WATT, ±5%	184A763H31
R213	RESISTOR 68K OHMS, ½ WATT, ±5%	184A763H71
R214	POTENTIOMETER 50K OHMS	629A430H01
D151-D152 D153	DIODE 1N457A	184A855H07
Z151-Z153	ZENER DIODE 1N3686B	185A212H06
Z152-Z154	ZENER DIODE 1N957B	186A797H06
Q151-Q152 Q153	TRANSISTOR 2N3417	848A851H02
Q154	TRANSISTOR 2N699	184A638H19
Q155	TRANSISTOR 2N3064	184A638H24
C151-C152	CAPACITOR 0.047 MFD., 200 VOLTS, ±5%	849A437H04
R151-R152 R157-R158	RESISTOR 4.7K OHMS, ½ WATT, ±2%	629A531H48
R153-R159	RESISTOR 82K OHMS, ½ WATT, ±2%	629A531H78
R154-R160	RESISTOR 10K OHMS, ½ WATT, ±2%	629A531H56
R155-R161	RESISTOR 6.8K OHMS, ½ WATT, ±2%	629A531H52
R156-R162	RESISTOR 22K OHMS, ½ WATT, ±5%	184A763H59
R163-R164	RESISTOR 10K OHMS, ½ WATT, ±5%	184A763H51

ELECTRICAL PARTS LIST

CIRCUIT SYMBOL	CHANNEL BD. (S# 201C013G01) DESCRIPTION	WESTINGHOUSE DESIGNATION
R165-R166 R167 R168	RESISTOR 15K OHMS, 1 WATT, ±5%	187A643H55

CIRCUIT SYMBOL	ARMING BD. (S# 201C022G01) DESCRIPTION	WESTINGHOUSE DESIGNATION
D259-D260 D261-D263 D264-D265	DIODE 1N457A	184A855H07
Q254-Q255 Q256-Q258 Q259	TRANSISTOR 2N3417	848A851H02
Q257	TRANSISTOR 2N3645	849A441H01
R266-R267 R270-R271 R275-R276 R281-R282 R284-R285 R287-R288	RESISTOR 10K OHMS, ½ WATT, ±5%	184A763H51
R268-R272 R273-R274 R277-R278 R283	RESISTOR 22K OHMS, ½ WATT, ±5%	184A763H59
R279	RESISTOR 27K OHMS, ½ WATT, ±2%	629A531H66

CIRCUIT SYMBOL	OUTPUT BD. (S# 201C024G01) DESCRIPTION	WESTINGHOUSE DESIGNATION
D301-D302 D303-D304 D305-D306 D308	DIODE 1N457A	184A855H07
D307	DIODE 1N645A	837A692H03
Z301-Z303 Z304-Z305	ZENER DIODE 1N957B	186A797H06
Z306	ZENER DIODE 1N3688A	862A288H01
Q301-Q305 Q306-Q307 Q309	TRANSISTOR 2N3645	849A441H01
Q302-Q303 Q304-Q308	TRANSISTOR 2N3417	848A851H02

ELECTRICAL PARTS LIST

C301	CAPACITOR 1.0 MFD., 35 VOLTS, ±10%	837A241H15
C302-C303 C306-C309	CAPACITOR 0.22 MFD., 50 VOLTS, ±10%	762A703H01
C305	CAPACITOR 4.7 MFD., 35 VOLTS, ±10%	184A661H12
C307-C308	CAPACITOR 0.047 MFD., 200 VOLTS, ±5%	849A437H04
C310	CAPACITOR 0.10 MFD., 200 VOLTS, ±10%	188A669H03
C311	CAPACITOR 1.5 MFD., 35 VOLTS, ±10%	187A508H09
R301-R303 R304-R306 R310-R311 R315-R320 R323-R324 R326-R330 R335	RESISTOR 10K OHMS, ½ WATT, ±5%	184A763H51
R302	RESISTOR 120K OHMS, ½ WATT, ±5%	184A763H77
R305	RESISTOR 47 OHMS, ½ WATT, ±5%	187A290H17
R307-R314 R319-R321 R325	RESISTOR 22K OHMS, ½ WATT, ±5%	184A763H59
R309-R317	RESISTOR 1K OHMS, ½ WATT, ±5%	184A763H27
R312	RESISTOR 470 OHMS, ½ WATT, ±5%	184A763H19
R313	RESISTOR 470K OHMS, ½ WATT, ±5%	184A763H91
R316	POTENTIOMETER 15K OHMS	629A430H08
R318-R322 R328	RESISTOR 4.7K OHMS, ½ WATT, ±5%	184A763H43
R327	RESISTOR 6.8K OHMS, ½ WATT, ±5%	184A763H47
R329	RESISTOR 18K OHMS, ½ WATT, ±5%	184A763H57
R331	RESISTOR 10K OHMS, ½ WATT, ±2%	629A531H56
R332	RESISTOR 6.8K OHMS, ½ WATT, ±2%	629A531H52
R333	RESISTOR 27K OHMS, ½ WATT, ±2%	629A531H66
R334	RESISTOR 150 OHMS, 3 WATT, ±5%	762A679H01

CIRCUIT SYMBOL	TEST BD. (S# 899C711G01) DESCRIPTION	WESTINGHOUSE DESIGNATION
S1	POTENTIOMETER 1K OHMS	185A086H28
S2	POTENTIOMETER 50K OHMS	185A086H22

CIRCUIT SYMBOL	CHASSIS MOUNTED COMPONENTS DESCRIPTION	WESTINGHOUSE DESIGNATION
Z1	ZENER DIODE 1N2984B	762A631H01
R1	RESISTOR 300 OHMS, 25 WATT, ±5%	1202847

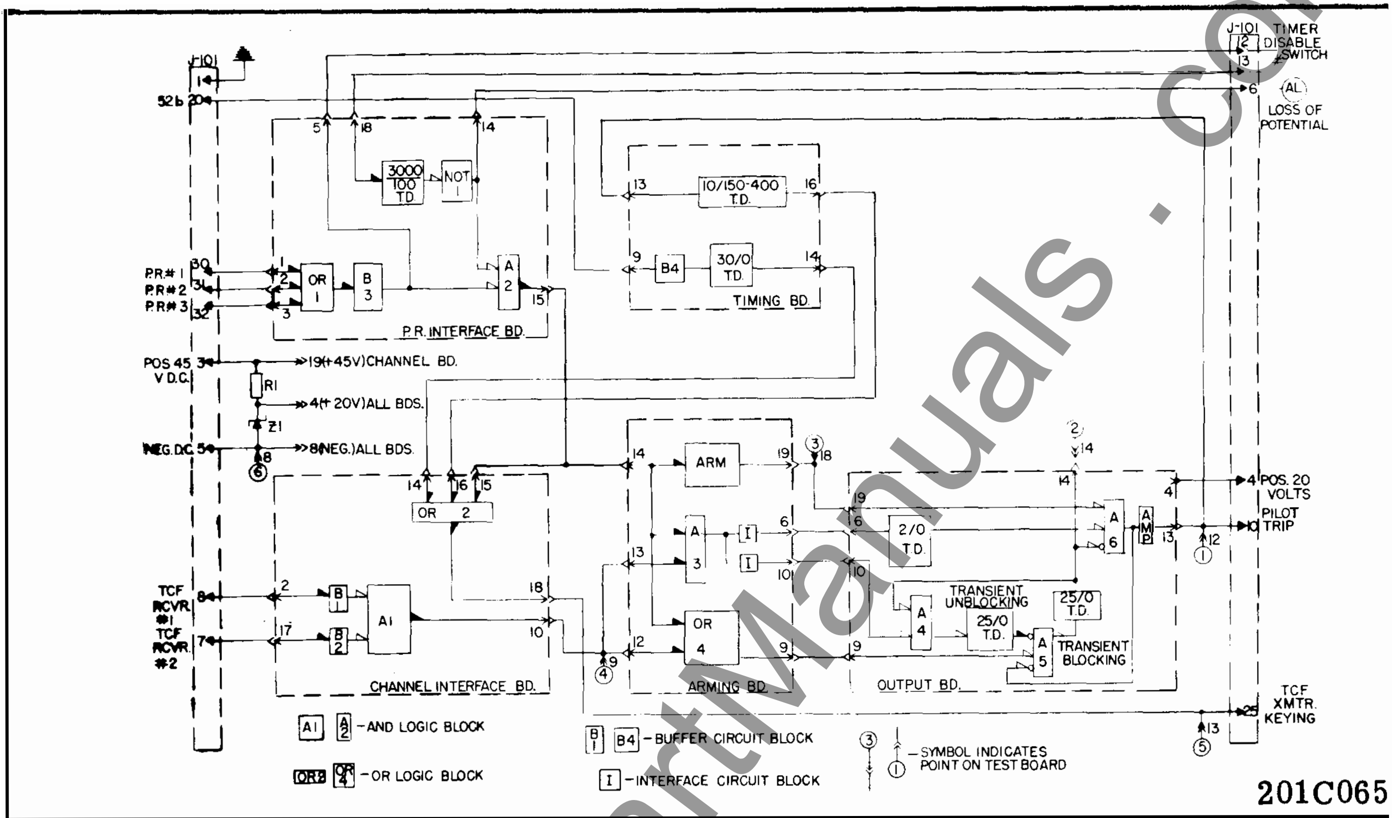


Fig. 2 Logic Block Diagram for the Type STU Relay

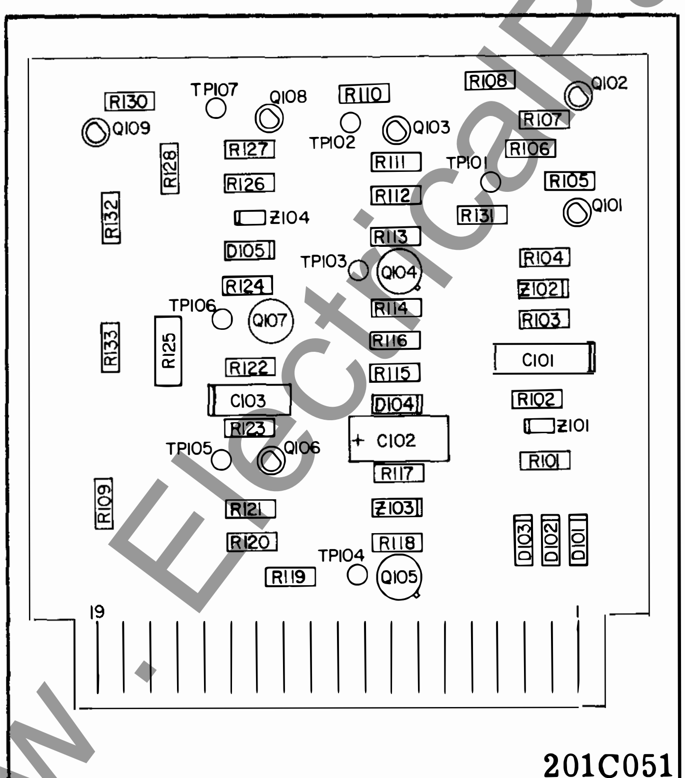


Fig. 3 Component Location of the Protective Relay Board for the Type STU Relay.

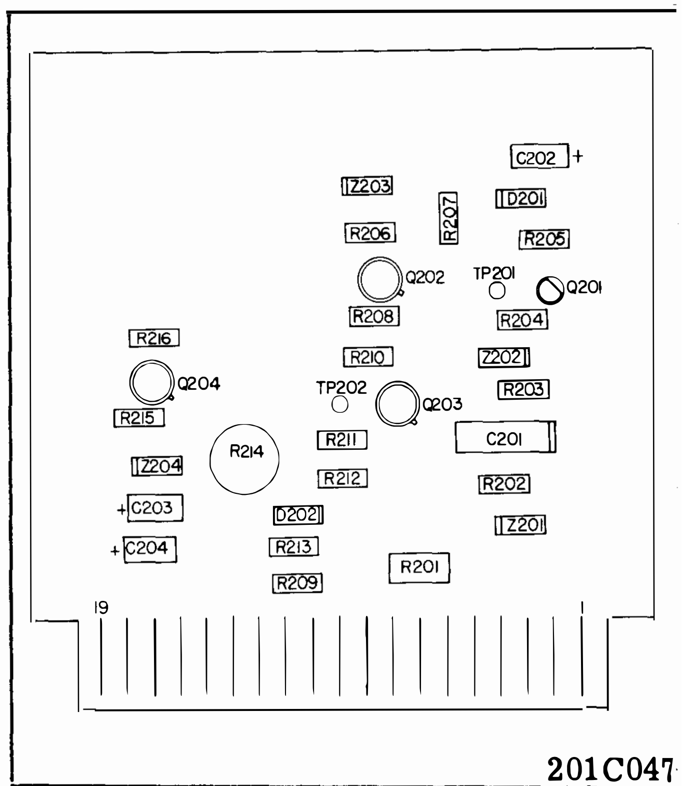


Fig. 4 Component Location of the Timing Board for the Type STU Relay.

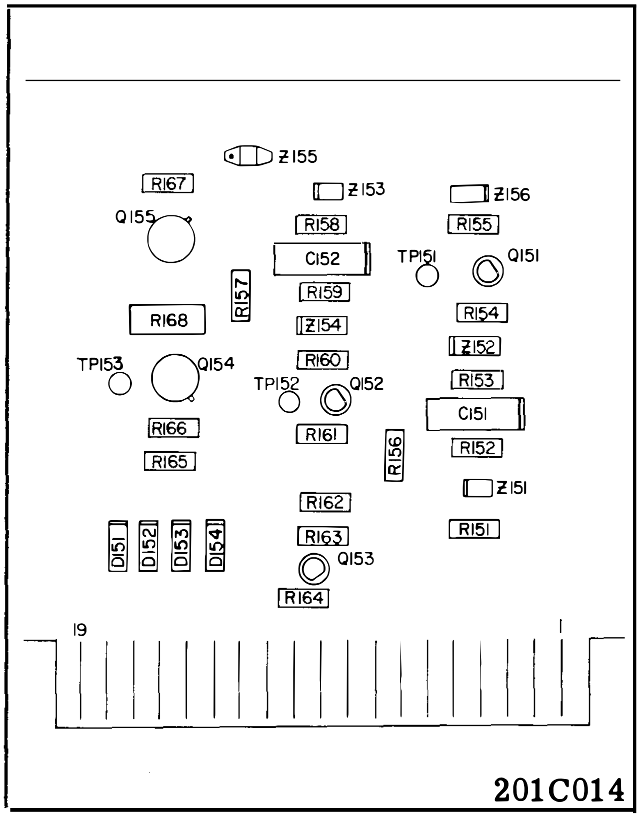


Fig. 5 Component Location of the Channel Board for the Type STU Relay.

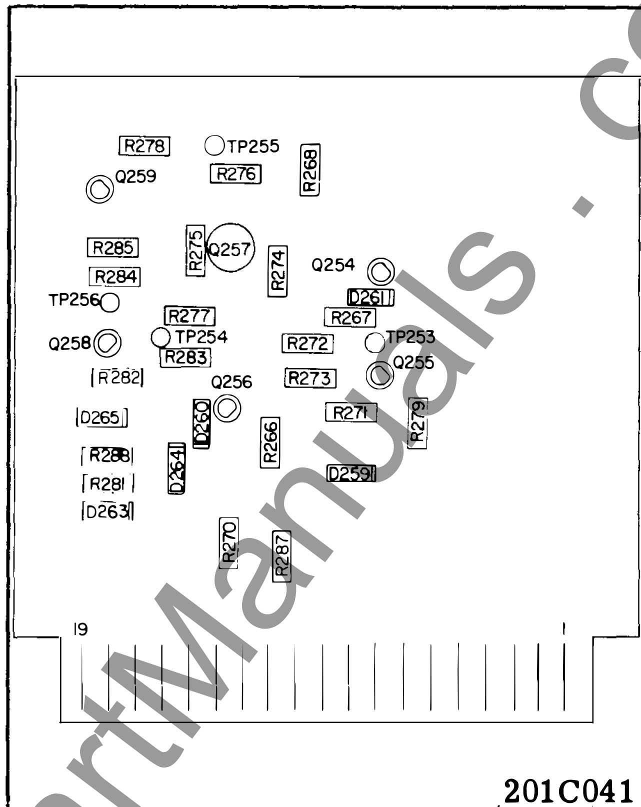


Fig. 6 Component Location of the Arming Board for the Type STU Relay.

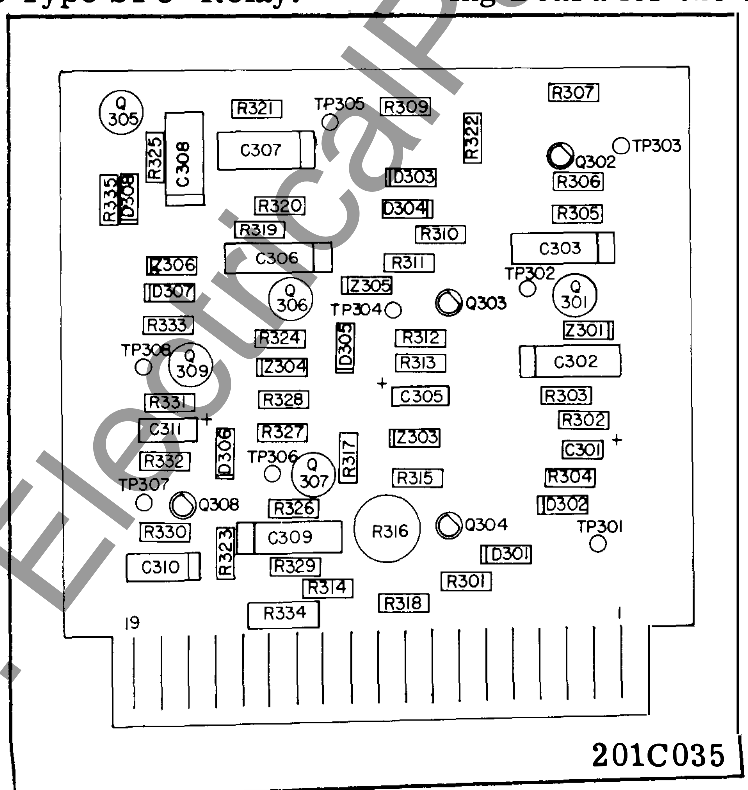


Fig. 7 Component Location of the Output Board for the Type STU Relay.

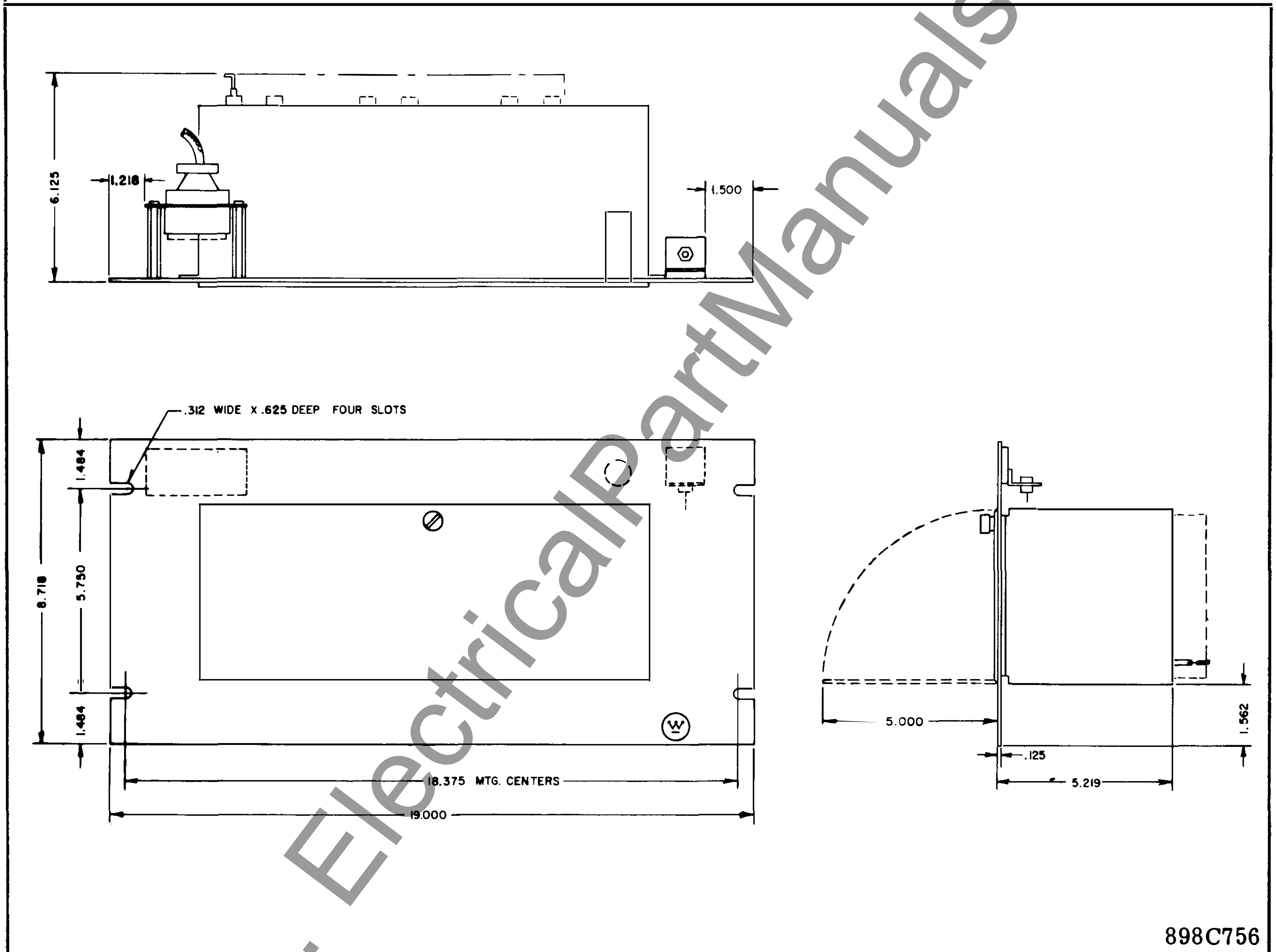


Fig. 8 Outline and Drilling Plan for the STU Relay.

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