INSTALLATION • OPERATION • MAINTENANCE

INSTRUCTIONS

TYPE STU-12 TRANSFER TRIP RELAY FOR A WEAK FEED TERMINAL

CAUTION: It is recommended that the user of this equipment become acquainted with the information in either these instructions or the system instruction leaflet 40-205.1 before energizing this relay. Failure to observe this precaution may result in damage to the equipment. Before putting the relay into service, operate the relay to check the electrical connections.

Do not remove or insert printed circuit boards while the STU-12 relay is energized.

APPLICATION

The type STU-12 relay is a solid state directional comparison permissive overreaching transfer trip auxiliary relay for use with solid state or electromechanical distance relays, and a frequency shift type TCF carrier or TA-3 tone channel. This relay will prevent tripping for faults external to the protected line section to which it is applied and permit high speed simultaneous tripping for internal faults. The relay will respond to indications of fault direction and distance provided by the phase and ground distance relays thereby, controlling the transmission of a trip signal and the initiation of high speed tripping for internal faults.

The relay described in this instruction may be applied to two or three terminal lines to provide high-speed simultaneous clearing of all line terminals, even though one or more of these fails to deliver a meaningful amount of fault current. A forward reaching relay of at least one terminal must operate for the internal fault.

CONSTRUCTION

The STU-12 relay is mounted on a standard 19'' wide panel 5-¼'' high (3 rack units) with edge slots for mounting on a standard relay rack or panel. For the outline and drilling plan refer to Fig. 43.

A hinged and removable door on the front of the chassis covers the printed circuit boards. The photograph in Fig. 1 shows the front view of the relay with the door open. A sealing post at the top center in front may be used to lock and seal the relay when in service.

The rear panel consists of a hinged door which may be opened to expose various components mounted inside. Mounted on the hinged door are two AR type auxiliary relays and, when used, two AL telephone type relays. The AR relay is a small high-speed attracted armature type of unit. An insulated member, fastened to the free end of the armature, draws down four moving contact springs to close or open the contacts when the relay coil is energized. This relay is available for inspection by removing the locking screw and swinging the hinged door outward. In the AL relays, an electromagnet attracts a right-angle iron bracket which in turn operates a set of make or break contacts.

Four power supply resistors are mounted in the rear housing of the chassis. In addition, one 32 terminal connector, J1, and two, (4) terminal, terminal blocks are mounted on the rear of the panel. The photo in Fig. 2 shows the rear view of the STU-12 relay with the top cover off and rear door open.

All of the circuitry suitable for mounting on printed circuit boards is contained in an enclosure behind the front door. The printed circuit boards slide into position in slotted guides at the top and bottom of the enclosure, and engage a terminal block at the rear of the compartment. Each board and terminal block are keyed so that they cannot be accidently inserted into the wrong slot location. A handle mounted on the front end of the board is used for identification, and for removing and inserting the circuit. In addition the handles also serve as a bumper with the front door to prevent the board from becoming disconnected from its terminal block. The boards may be removed for replacement purposes or for use in conjunction with a board extender (Style No. 849A534G01) which permits access to the boards test points and terminals for making measurements while the relay is energized

SUPERSEDES I.L. 41-959.71
*Denotes change from superseded issue.

EFFECTIVE MARCH 1972

Fifteen (15) printed circuit boards are used in the STU-12 chassis. The location and title of the printed circuit boards are shown on the relay component location drawing, Fig. 3.

Printed Circuit Boards

Following is a description of all the printed circuit boards used in the STU-12 relay. Refer to the functional relay logic shown in Fig. 4, 5, 6, and 7. The internal schematics associated with the printed circuit boards contain a detailed NOR/NAND logic diagram to simplify understanding of the transistor logic.

For those users not generally acquainted with logic circuit notation or with device symbols of those components used in the STU-12 drawings, it is recommended that a copy of Westinghouse instruction leaflet. I.L. 41-000-1 entitled SYMBOLS FOR SOLID STATE PROTECTIVE RELAYING be consulted.

Power Supply Board

The Power Supply board located in slot A contains two 20 volt transistor regulators: These voltage regulators will operate from a nominal battery supply of 48 or 125 volts dc by varying resistors RA, RB, RC and RD mounted in the rear of the chassis. The location of components on this board is shown in Fig. 8, and the internal schematic is Fig. 9.

Weak Feed Logic 1 Board

The Weak Feed (W.F.) Logic-1 board located in slot B contains logic to provide tripping and keying by the forward reaching relays (21NP(67N) or 21P and to provide indication of loss of ac potential if either 21S or 21NS(67NS) inadvertantly operates for a sustained period of greater than 500 milliseconds.

In relays for use with electromechanical systems a relay driver is provided on this board to energize the Loss of Potential AL telephone relay mounted in the rear of the chassis. A contact bounce circuit is also provided to override bounce in the contacts of 21P or 21NP(67N).

Location of components on this board is shown in Fig. 10. Two internal schematics are used: Fig. 11-for use with electro-mechanical systems and Fig. 12 for use with solid state systems.

Weak Feed Logic-2 Board

The Weak Feed (W.F.) Logic-2 board located in slot C contains some of the logic to control echo keying. This board provides interface with the undervoltage relay (27). There are two buffered inputs, one for IA/IC, another for 21S- which work into an AND circuit, whose output will block echo keying and trip. A memory circuit on this board provides echo-key blocking after the 10/0 timer operates even if 21S and IA/IC reset.

Location of components on this board is shown in Fig. 13, and the internal schematic in Fig. 14.

Weak Feed Logic-3 Board

The Weak Feed (W.F.) Logic-3 board located in slot D contains some of the logic to set up breaker tripping at the weak source terminal. An output from the 4 input AND on this board is one of the conditions required for trip. Other logic, including the 0/50 millisecond timer, is used to supervise tripping.

A contact bounce circuit is required for electromechanical systems to override bounce which could delay tripping.

Location of components on this board is shown in Fig. 15. Two internal schematics are used: Fig. 16-for electromechanical systems and Fig. 17-for solid state systems.

Weak Feed Locic-4 Board

The Weak Feed (W.F.) Logic 4 board located in slot E contains logic to both provide or block echo keying. An output from the 3 input AND on this board will start echo keying, but if an output is received from the 4 input OR, the 4/80 millisecond timer will pickup and block echo keying.

The memory circuit comprised of an AND and OR is used to block echo keying when the breaker is open and the undervoltage relay (27) operates.

Location of components for this board is shown in Fig. 18, and the internal schematic is in Fig. 19.

Channel Interface Boards

The Channel Interface boards located in Slot F

From : Greentree Office
WIN : 235-4761
Date : September 12, 1972
Subject: INSTRUCTION LEAFLETS-RELAYS

Industry Services Divisions
DISTRICT ENGINEERING SERVICE MANAGERS

file

Attached is one (1) copy each of the three (3) I.L.'s covering Newark relays as follows:

I.L. 41-776.4C - Type SBFU Static Circuit Breaker Failure Relay

I.L. 41-496.4B - Type SDGU-1-2-3-4-5-6-7 Solid State Ground Distance Relay

I.L. 41-959.71A - Type STU-12 Transfer Trip Relay for a Weak Feed Terminal

If any additional copies are required for local distribution, please order direct from Newark Sales. (WIN 326-2584) These are not stocked at Trafford Printing.

L. M. Kram
L. M. Kram

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Enclosures (3)

(Channel 1) and Slot G (Channel 2-when used) contain the buffered interface logic for connection with the channel equipment and provide the outputs to work into the Channel Trip and Supv. boards. In addition, the TA-3 Channel Interface board contains buffered outputs.

An interlock feature is also included in order to convert from a 2 to 3 terminal line relay and conversely. CHANNEL TWO INTERFACE board in slot G must be used in the relay for THREE TERMINAL applications, but MUST BE REMOVED for TWO TERMINAL LINE systems.

A conversion kit may be ordered to change a 2 TERM LINE relay to 3 TERM LINE. This kit includes instructions, nameplate and a CHANNEL INTERFACE BOARD.

The location of components for both the TA-3 and TCF-CHANNEL INTERFACE boards is shown in Fig. 20. Internal schematics are shown in Fig. 21 for the TA-3 CHANNEL and Fig. 22 for the TCF CHANNEL.

Channel Trip Boards

The CHANNEL TRIP board located in slot H contains the connecting logic between the channel trip signals and the remainder of the relay logic. A buffered output for channel 1 and 2 trip is included on this board.

The TONE CHANNEL TRIP board also has additional logic comprised of two AND's and an OR for a guard return function. This logic is inherent to the TCF channel equipment, therefore it is not required in this relay.

Location of components on this board is shown in Fig. 23. Two internal schematics are used; TONE CHANNEL TRIP BOARD - Fig. 24, TCF CHANNEL TRIP BOARD - Fig. 25.

Channel Supervision Board - TCF Channel

The Channel Supervision board for a TCF Channel is located in slot I and contains the connecting logic between the supervisory functions of the channel equipment and the remainder of the relay logic. Both LOW SIGNAL CLAMP outputs work into an OR, as do both CHECK TRIP outputs.

For electromechanical systems, a relay driver is used for energizing a loss of channel AL telephone relay.

The location of components for this board is shown in Fig. 29, and the internal schematic in Fig. 30.

Channel Supervision Board - Tone Channel

The Channel Supervision board for a TONE channel is located in slot I and contains the connecting logic between the supervisory functions of the channel equipment and the remainder of the relay logic. A 150/100 millisecond time delay and associated logic is used to monitor the LOW SIGNAL CLAMP outputs for loss of channel. For electromechanical systems, a relay driver is used for energizing a Loss of Channel AL telephone relay. the NOISE outputs work into OR logic on this board.

Location of components for this board is shown in Fig. 26. Two internal schematics are used; Fig. 27 for electromechanical systems and Fig. 28 for solid state systems.

Transmitter Key Board

The Transmitter Key board located in slot J contains OR logic to combine all inputs required to key the transmitter, and interface circuitry to key the particular channel equipment. A relay driver circuit is connected to the output of the OR in order to operate an AR relay mounted in the rear of the chassis.

For use with the TCP channel, interface with the transmitter is a positive going (0 to 20 volt) buffered output represented by transistors Q4 and Q5 is shown on the internal schematic, Fig. 32. When the relay is used with tone channels, the transmitter interface is a negative going output similar to the relay driver and is shown by transistor Q6 on internal schematic, Fig. 33.

Location of components for the XMTR KEY board is shown in Fig. 31.

Checkback Board

The Checkback board located in slot K contains

logic used to functionally test the channel in both directions. The circuit consists of two AND circuits and a 2500/2500 millisecond time delay and is operated from the CHANNEL SUPV board. This logic is required as part of the channel checkback scheme.

The location of components for this board is shown in Fig. 34, and the internal schematic in Fig. 35.

Timing Board

The timing board located in slot L contains logic, a buffered input, and three time delays used in conjunction with the remainder of the relay.

After a pilot trip operation, the 0/30 millisecond timer maintains the transmitter keying for 30 milliseconds. The 180/0 millisecond timer delays keying of the transmitter for 180 milliseconds after opening of the local breaker. Input to this timer is a 48/125 V DC buffer circuit.

The 2500/0 millisecond timer and associated logic is used to permit transient blocking for 2.5 seconds if a trip output is obtained from the channel receiver. This circuit is also controlled by the 52b contact input.

The location of components on this board is shown in Fig. 36, and the internal schematic in Fig. 37.

Arming Board

The Arming Board located in slot M contains the connecting logic between the Channel, Protective Relay, Elec-Mech and Timing boards for the OUTPUT board. Logic on this board interfaces with and sets up arming of the trip AND, the transient blocking and unblocking timers and the 4/0 millisecond trip timer.

In addition, two time delays, 0/1000 and 0/100 milliseconds, are included on this board. The 0/1000 MS timer holds transient blocking on for an additional 1000 MS to protect against fault power reversals due to unequal breaker reclosing times into a permanent external fault. After a pilot trip operation, the 0/100 MS timer picks up and immediately resets the 0/1000 MS timer to de-energize the transient blocking timer. The 100 MS dropout time is greater than the time it takes to reset the distance relays, remove the input to the 0/1000 MS timer, therefore transient blocking will remain off, after the pilot trip signal is removed.

The location of components for this board is shown in Fig. 38 and the internal schematic in Fig. 39.

Output Board

The Output board located in slot N contains the final logic of the relay. This board utilizes the intelligence supplied by the Arming board to set up either a pilot trip output for internal faults, transient blocking on external faults or transient unblocking for sequential faults.

Three timers are used on this board: a 4/0 millisecond timer to delay the pilot trip output and two 18/0 millisecond timers for transient blocking and unblocking. NOTE: Relays may be supplied with the transient blocking time calibrated for 25 milliseconds instead of 18 MS to coordinate with the time delay of the channel equipment. The pilot trip output is comprised of and AND circuit whose output works into a logic inverting amplifier. There are two final pilot trip output: a buffered positive going (0 to 20 volt) output and a relay driver to activate an AR relay mounted in the rear of the chassis. Fig. 40 shows location of components on this board, and Fig. 41 shows the internal schematic and detailed logic.

Test Board

The Test board located in slot 0 is used for facilitating test measurements and routine checks of the relay. This board consists of 10 test terminals mounted on a panel attached to a printed circuit board.

OPERATION

The type STU-12 transfer trip relay for a weak feed terminal is used in a directional comparison permissive overreaching transfer trip relay system for power line protection. High speed tripping is obtained for two or three terminal line application where line terminals may be weak or strong, providing one of the terminals is a strong source.

System Operation

In a directional comparison transfer trip system, a continuous guard signal is normally transmitted

from each line terminal and received at all other terminals. The channel transmitters are keyed to the trip frequency by the STU-12 to remove blocking at the remote terminals during an internal fault. At the weak feed terminal, the STU-12 operates on the "echo-trip" principle; that is, a trip request must be received from one of the remote terminals before the local transmitter can key a trip signal back to the remote terminal. In addition to receiving a remote trip request at the weak source terminal, either voltage relay (27 or 59N) and neither reverse-reaching relay must operate to key the local transmitter. Pilot tripping is initiated at the weak terminal if either voltage relay operates and neither reverse reaching phase or ground relay operates and a trip request is received from all remote terminals.

If a weak source terminal can be become a strong source then forward reaching phase and ground relays can be applied to the system as in the transfer trip normal system.

Some features included in the system are a functional test channel checkback scheme, loss of A-C potential circuit for reverse reaching relays, channel logic to force a guard return, and coordination for bus fault tripping, breaker failure and fault power reversal. The description of the preceding features and some special weak feed coordination is further explained under the Relay Operation section.

Refer to system I.L. 40-205.1 on the transfer trip system for further system operation.

Relay Operation

Refer to the logic diagrams shown in Fig. 4,5,6, and 7 to understand the operation of the STU-12 transfer trip relay.

1. Normal Condition

   In Fig. 4,5,6, and 7 the logic voltage "0" and "1" states shown refer to the normal operating condition of the STU-12 relay.

2. Internal Fault

   For an internal fault, providing the terminal is weak feed, one of the voltage relays (27 or 59N) Will operate and cause the input that is not negated on the 4 input AND on WEAK FEED LOGIC-3 board to become a logic "1". This will satisfy this AND and course a logic "1" output from the line driver which does the following:

   a. Produce a logic "1" at Test Term 3 (Protective Relay.)

   b. Pickup the 0/1000 MS timer on the ARMING BD. and produce a logic "0" at terminal 5 of the OUTPUT BD. This will start the transient blocking timer.

   c. Arm the trip AND on the OUTPUT BD through the one input OR on the ARMING BD.

   d. Satisfy one input of the trip AND on the ARMING BD.

   Both of the channel transmitters will be keyed at the remote terminals, thus causing both of the receiver trip outputs of the local channel 1 and 2 receivers to become a logic "1". This make TEST TERM 4 (CHANNEL TRIP) a logic "1" signal through logic on the CHANNEL INTERFACE and CHANNEL TRIP BDS. This "1" output will satisfy the trip AND on the ARMING BD. causing energization of the 4/0 MS timer on the OUTPUT BD. Four milliseconds later the trip AND on the OUTPUT BD. will be satisfied and produce a PILOT TRIP.

In addition, a voltage relay operation will cause drop out the 0/6 MS timer on the WEAK FEED LOGIC 4 board and satisfy one of the inputs on the three input AND on the board. Since a trip request will be received from the remote terminal (s); that is, then the receiver trip outputs become a logic "1"; to satisfy the three input AND to key the local transmitter.

Also, when a receiver trip output (logic "1") is received as an input to the STU-12 the 2500/0 MS timer on the TIMING BD. will be energized to start transient blocking. This will not affect the initial pilot trip, since it is an internal fault, and once the local breaker opens, then the 52b contact will block the output of this AND on the TIMING BD.

The 52b contact of the breaker provides an input to the 0/50 timer on the WEAK FEED LOGIC-3 board. The output of this timer blocks tripping when the breaker is open. Tripping will remain blocked 50 milliseconds after closing the breaker at the Weak Feed terminal to allow time for the undervoltage relay (27) to reset

If the STU-12 is applied at a terminal that can be a strong feed terminal, then distance relays 21P or 21NP (67N) would respond to the internal fault.

Operation of either of these relays would cause the STU-12 to key the transmitter to the trip frequency and also to set up trip. Logic for strong feed operation is on WEAK FEED LOGIC-1 board.

Once a pilot trip signal is obtained for an internal fault, the 0/100 MS timer on the ARMING BD. will rapidily reset the 1000 millisecond dropout timer of the 0/1000 MS timer. Therefore; when reclosing into a permanent internal fault, the only time delay will be the 4/0 MS timer.

3. External Fault

For an external fault forward from the weak source terminal but behind the remote terminals, one of the forward reaching relays of the remote terminal of a three terminal line will not see the fault. As a result, no receiver trip signal will be received from that remote terminal. At the local terminal, if either voltage relay (27 or 59N) operates, then, through logic on WEAK FEED LOGIC 3 board, the four input AND is satisfied to produce a logic "1" at TEST TERM 3 (Protective Relay). The trip AND on the ARMING BD will not be satisfied because both receiver trip signals were not received. However, the 0/1000 MS timer will pickup to cause the 18/0 MS transient blocking timer on the OUTPUT BD to start timing. IN 18 milliseconds, TEST TERM 2 (TRANSIENT BLOCKING) will become a negative logic "1" to block the trip AND of the OUTPUT BD. thereby preventing possible undersirable tripping during transients occuring at the clearing of an external fault.

If an external fault occurs behind the weak feed terminal of the protected line, then either the undervoltage (27) or overvoltage relay (59N) will operate. Also, either reverse reaching relay (21S or 21NS) will also see this fault and operate to block the 4 input AND on the WEAK FEED LOGIC 3 board. The forward reaching relays at the remote terminal (s) may also see this fault and key to the trip frequency. Therefore a trip request (received receiver trip signal) would be received at the weak feed terminal. This would satisfy one input of the trip AND on the ARMING BD. and also start the 2500/0 ms. timer on the TIMING BD. Since the other input to the trip AND is not satisfied, the output of the 2500/0 ms. timer will activate the 0/1000 ms. timer on the ARMING BD. and set up transient blocking 18 milliseconds latter to block trip. No tripping will occur at the remote terminals since operation of 21S or 21NS at weak feed terminal will prevent echo keying by pickingup the 4/80 ms. timer on WEAK FEED LOGIC 4 board.

The 0/6 MS timer on WEAK FEED LOGIC 4 board is used to delay echo keying for 6 milliseconds to allow adequate time for 21S or 21NS to operate for an external fault. The overcurrent fault detector (IA/IC) supervices 21S and must operate along with 21S to block keying and trip.

If the terminal was strong rather than weak feed, then for a forward external fault, the forward reaching relay 21P or 21NP (67N) would operate to set up transient blocking. For a reverse fault, these relays would not see the fault, but transient blocking would be set up with the received trip signals.

Transient blocking is also established to insure against any misoperation due to fault power reversals caused by unequal circuit breakers clearing time on a parallel line. The 1000 millisecond reset time of the 0/1000 MS timer on the ARMING BD. prevents misoperations when reclosing into an external fault where fault power flow reversals occur. In addition, the 1000 millisecond reset time also prevents transient, blocking from resetting when short holes appears in the input.

4. Sequential Fault

Occasionally an external fault will be followed by an internal fault before the former is cleared. In order to prevent a long delay in clearing a sequential fault a transient unblocking 18/0 MS timer is included. Although transient blocking has been initiated by the external fault, the presence of an internal fault will produce a negative logic "1" signal from the trip AND on the ARMING BD., since a trip request will be received from the remote terminal. This "1" signal will energize the 4/0 MS timer and satisfy the AND to energize the 18/0 MS transient unblocking timer on the OUTPUT BD. In 18 milliseconds the transient blocking timer will reset the transient blocking timer thus satisfying the TRIP AND on the OUTPUT BD. and causing a pilot trip output.

5. Loss of Potential

Distance relays may tend to operate if the input from the potential device is momentarily interrupted. Since tripping of circuit breakers is undesirable for this loss of ac potential the STU-12 relay will lockout tripping and provide alarm. This is accomplished by the 500/500 MS timer on WEAK FEED LOGIC-1 board. In 500 milliseconds after a reverse reaching relay (21NS-67NS or 21S) operation, providing both receiver trip signals are not present, a logic "1" signal will be produced at TEST TERM 7 (Loss of Potential). This "1" signal will lockout

the three input AND on W.F. Logic 1 board, thereby simulating "not" distance relay (21P or 21NP-67N) operation. Output of the 500/500 MS timer will also provide a buffered "1" signal at the J1 connector.

For electromechanical systems, an AL telephone relay will drop out for indication purposes.

6. Channel Transmitter Control

The transmitter may be keyed to the trip frequency by any one of the following six inputs:

a. 0/30 MS timer after pilot trip.

b. 180/0 MS timer from 52b contact.

c. 21P or 21NP (67N) forward reaching relay operation – strong feed keying

d. 27 or 59N – voltage relay operation – weak feed keying.

e. Check back circuit from channel logic.

f. Contact bounce for 21P or 21NP (67N) operation – electromechanical systems only.

When the transmitter is keyed, TEST TERM 5 (XMTR KEY) becomes a logic "1" signal, the keying AR picks up, and the interface with the transmitter becomes a logic "1" as described under the operation of the XMTR KEYING BD.

The weak feed keying control logic is contained primarily on WEAK FEED LOGIC BDS. 2 and 4. Keying at the weak terminal will take place when either voltage relay (27N and 59N) and neither reverse reaching relay (21NS or 21S) operates and a trip request is received from either remote terminal. There is a 6 millisecond delay (0/6 MS timer) on echo keying to allow time for blocking to become effective for an external fault, thereby preventing false keying.

Operation of 21S and its supervising overcurrent fault detector IA/IC will satisfy the two input AND on WEAK FEED LOGIC 2 BD. If the undervoltage relay 27 has operated and the breaker is not open then an output will be obtained from the three input AND. This output will start the 10/0 MS timer and also satisfy the four input OR on WEAK FEED LOGIC 4 BD. to block echo keying. After 10 milliseconds, the output of the 10/0 timer will seal in the three input AND to provide continuous echo key block when 21S resets after memory action subsides for a zero voltage fault. This AND can only be reset by the undervoltage relay (27) or by the opening of the breaker. The purpose of the breaker resetting this is to break the 21S seal in for bus faults, where bus side pots are used.

If 21NS or 67NS operates, it also will block echo keying by applying an input to the four input OR on WEAK FEED LOGIC 4 board. Also, echo keying is blocked by the 2 input OR and AND memory circuit on the same board. This circuit will cause blocking when the breaker is open (52b closed) and the undervoltage relay (27) operates. The purpose of this is to prevent tripping of the remote terminals when closing the line into a fault on the weak-terminal bus, when using bus-side pots. Relay 21S could not operate for this case since their was no voltage prior to the fault.

To block echo keying, an output must be received from the four input OR an WEAK FEED LOGIC 4 board for 4 milliseconds to pickup the the 4/80 timer and block the echo keying three input AND. The 4 ms time delay will prevent blocking for transient 21S operation on an internal fault. There is an 80 millisecond delay on removal of blocking to insure that the fault detectors at the remote terminal have reset.

Strong feed keying control is obtained through logic on WEAK FEED LOGIC 1 board. Operation of 21P or 21NP (67N) will satisfy the three input AND on this board providing loss of potential has not occurred and echo keying is not blocked. A A logic "1" output from this AND will cause transmitter keying.

After a pilot trip operation the 0/30 MS timer on the TIMING BD. will maintain keying of the trip frequency for 30 milliseconds in order to insure that the remote breaker has tripped before the transmitter returns to normal condition.

After the local circuit breaker opens, the 52b contact will energize the 180/0 MS timer on the TIMING BD. and initiate trip frequency transmission after 180 milliseconds and until such time as the circuit breaker is reclosed. This 180 millisecond delay allows coordination for bus fault tripping of the local breaker, where tripping of the remote breaker would be incorrect and might cause undesired interruption to tapped transformer terminals. Transmission of the trip frequency is necessary to permit tripping of the remote terminal should the remote circuit breaker be closed into a fault, or should a fault develop in the protected line while while the local circuit breaker is open.

7. Channel Logic

   a. TCF frequency shift carrier channel
      Refer to CAHNNEL-INTERFACE, TRIP, and SUPERVISION BDS. in logic drawings Fig. 4 and 5.

Two TCF CHANNEL INTERFACE boards are shown: Both boards must be used for three terminal line systems utilizing two receivers. However, for two terminal line applications, the interface board in board slot G must not be used in the relay. An interlock shown on the Channel 2 interface board connects the Channel 2 trip output as one output to the Channel trip AND on the CHANNEL TRIP BD.

For three terminal line applications, both receiver trips signals are required to produce a logic "1" signal at TEST TERMINAL 4. This output will satisfy one input of the ARMING BD. trip AND, block operation of the 500/500 MS loss of potential timer, and produce a buffered "1" output. Either receiver trip signal will produce a "1" signal at terminal 12 of the CHANNEL TRIP BD. to start transient blocking.

For two terminal line applications, the one receiver trip signal will produce a "1" output at TEST TERMINAL 4 (CHANNEL TRIP), and terminal 12 of the CHANNEL TRIP BD.

Operation of either or both low signal clamp inputs ("1" to "0") will cause a "1" signal at TEST TERMINAL 6 (LOSS OF CHANNEL) for use in the channel checkback scheme. For electromechanical systems, an AL telephone relay will dropout for indication of loss of channel. In addition, operation of either Check Trip output will produce a "1" output at terminal 7 of the CHANNEL SUPERVISION BD. This signal is used for the channel checkback scheme.

   b. Frequency shift tone channel
      Refer to CHANNEL INTERFACE, TRIP and SUPERVISION BDS. in logic drawings Fig. 6 and 7.

Two TONE CHANNEL INTERFACE boards are shown; Both boards must be used for three terminal line systems utilizing two receivers. However, for two terminal line applications, the interface board in board slot G must not be used in the relay. An interlock shown on the channel 2 interface board connects the channel 2 trip output as one input to three input channel trip AND on the CHANNEL TRIP BD.

For three terminal line applications, both receiver trip signals and no low signal clamps are required to produce a logic "1" signal at TEST TERMINAL 4 (CHANNEL TRIP). This output will satisfy one input of the ARMING BD. trip AND, block operation of the 500/500 MS loss of potential timer, and produce a buffered output. Either receiver trip signal will produce a "1" signal at terminal 12 of the CHANNEL TRIP BD. to start transient blocking and to energize an AND circuit on the CHANNEL SUPERVISION BD.

For two terminal line applications, the one receiver trip signal will produce a "1" output at TEST TERMINAL 4, and terminal 12 of the CHANNEL TRIP BD.

When a Tone Channel is used with the STU-12 transfer trip relay, the Tone receiver must be internally strapped to clamp to no trip output when a low signal condition occurs. Therefore, tripping will not be allowed under loss of channel.

Either LOW signal clamp operation ("1" to "0") will pickup the 150/100 MS timer and produce a "1" signal at TEST TERMINAL 6 (LOSS OF CHANNEL) for use in channel checkback as well as blocking Channel Trip. For electromechanical systems, an AL telephone relay will dropout for indication of loss of channel. Both low signal clamp outputs on the CHANNEL INTERFACE BDS. are buffered and separately brought out to the J1 connector.

One AND circuit on the CHANNEL SUPERVISION BD. is used for channel checkback. When a receiver trip signal from either channel is received, a logic "1" will be produced at terminal 3 of the CHANNEL SUPERVISION BD. providing both low signal clamps have not operated.

When the noise output operates on either one or both channel receivers, a logic "1" output is produced from the noise OR on the CHANNEL SUPERVISION BD. to block the trip AND of the ARMING BD. Therefore, the STU-12 relay will not trip on receipt of the channel noise. Both noise outputs on the CHANNEL INTERFACE BD. are buffered, connected together, and brought out to the J1 connector.

A guard return circuit is included on the CHANNEL TRIP BD. and is comprised of two AND's and an OR. The principle of guard return, is to insure that after a loss of channel condition is cleared up, the receiver trip signal will return in the "0" logic

state, not "1". When a low signal clamp operation ("1" to "0") is received from the tone channel, then the 150/100 MS timer picks up and applies a "1" signal to one input of each of the two guard AND's on the CHANNEL TRIP BD. Now, if either or both receiver trip signals are "1" or become a "1" within the 100 millisecond dropout time of the 150/100 MS timer, then a "1" output will be produced at the output of the guard return AND and the OR it works into. Terminal 5 of the CHANNEL TRIP BD. will become a "1" and hold the 150/100 MS timer picked up by applying a "1" input to the 3 input loss of channel OR on the CHANNEL SUPERVISION BD. By inspecting the logic it can be seen that both receiver trip signals (one for two terminal applications) must return to guard, logic "0" to, make the channel operative after a loss of channel condition.

8. Channel Checkback Test

   A. TCF frequency shift carrier channel
      Refer to logic drawings, Fig. 4 and 5. Information in this section does not cover the the complete test, but only that portion concerning the STU-12 relays.

At the local terminal, the carrier transmitter will be disconnected from the line thus causing a loss of channel condition at the remote terminal. This will cause the loss of channel OR on the CHANNEL SUPERVISION BD. (Remote Terminal) to assume a "1", and satisfy the two input AND (preceding the 2500/2500 MS timer) and in 2500 milliseconds pickup the 2500/2500 MS timer on the CHECKBACK BD. The "1" output of the 2500/2500 MS timer will satisfy one input of the AND following it. Next, a test switch will be operated at the local terminal and the following will happen: a protective relay signal (for example, 21P) will be simulated, the transmitter will be reconnected to the line to restore the channel, and the local transmitter will be keyed to the trip frequency. At the remote terminal the TCF receiver logic will not give a trip output since the channel was not restored to the guard frequency. However, there will be a "1" signal obtained from the CHECK TRIP output of the receiver. This check trip output will satisfy the other input to the AND on the CHECKBACK BD. causing the transmitter to be keyed to the trip frequency. Since the check trip signal also applies a "1" input to the negated input of the AND energizing the 2500/2500 MS timer, it will no longer be satisfied and the timer will dropout causing keying to stop in 2.5 seconds. However, within the 2.5 seconds of keying, the STU-12 relay at the local terminal will trip because of reception of both a received trip signal and a simulated protective relay signal.

   B. Frequency shift tone channel
      Refer to logic drawings, Fig. 6 and 7
      Information in this section does not cover the complete test, but only that portion concerning the STU-12 relay.

At the local terminal, the tone transmitter will be disconnected from the line thus causing a loss of channel condition at the remote terminal. This will cause the loss of channel OR on the CHANNEL SUPERVISION BD. (remote terminal) to assure a "1" output to pickup the 150/100 MS timer. This satisfies the two input AND on the Check Back Bd. and in 2500 milliseconds the 2500/2500 MS timer will pick up. The "1" output of the 2500/2500 MS timer will satisfy one input of the AND following it. Next, a test switch will be operated at the local terminal and the following will happen: a protective relay signal (for example, 21P) will be simulated, the transmitter will be reconnected to the line to restore the channel, and the local transmitter will be keyed to trip frequency. At the remote terminal, the tone receiver trip signal will be a "1" thus causing the three input AND on the CHANNEL SUPERVISION BD. to operate and produce a "1" at terminal 3 of this board. This "1" will satisfy the other input to the AND on the CHECKBACK BD. causing the transmitter to be keyed to the trip frequency. Since at the same time, the input to the 2500/2500 MS timer is lost, then the keying signal to local terminal will only last 2.5 seconds. However, within this time of keying, the STU-12 relay will trip because of the reception of both a received trip signal and a simulated protective relay signal.

9. Electromechanical Systems

When the STU-12 relay is used with electromechanical protective relays, two contact bounce circuits are used. The contact bounce circuit will produce a logic "1" output immediately upon reception of an input logic "1" signal. This output will last for approximately 20 milliseconds. The contact bounce circuits on the W.F. Logic 1 and 3 boards permit transmitter keying and an input to set up tripping respectively. These circuits prevent additional delay in tripping due to a bouncing elecmech protective relay contact.

Two telephone alarm relays are mounted in the rear of the chassis — one for indication of loss of a-c potential, another for indication of loss of channel. Both of these AL's are normally picked up.

CHARACTERISTICS

Control Voltage:	48 V DC (42 to 56 volts) 125 V DC (105 to 140 volts)
Current Drain:	SOLID STATE SYSTEMS Normal — 160 MA Pilot Trip - 270 MA Maximum - 310 MA ELEC-MECH SYSTEMS Normal - 200 MA Pilot Trip - 310 MA Maximum - 350 MA
Temperature Range:	-20 C to +55 C around chassis
Inputs:	
52b Contact -	48/125 Control Voltage Buffered 48V - 1.5 MA MAX CURRENT 125V - 2.5 MA MAX CURRENT
Protective Relays: 21NS(67NS), 21S, 21NP(67N), 21P, 59N, 27, IA/IC	SOLID STATE SYSTEMS 15 to 20 V DC Buffered 2 MA MAC CURRENT ELEC-MECH SYSTEMS 48/125 Control Voltage Buffered 48 V - 1.5 MA MAX CURRENT 125 V - 2.5 MA MAX CURRENT
All Other Inputs are:	15 to 20 V DC, buffered and require 2 MA MAX CURRENT
Outputs:	
Transmitter Key:	
TCF Frequency Shift Carrier Channel	15 to 20 V DC Buffered 10 MA MAX CURRENT
Frequency Shift Tone	"0" State - Open Circuit "1" State - Short Circuit to Battery Neg. 140 V DC MAX Voltage 40 MA MAX CURRENT

All Other Outputs are 15 to 20 V DC Buffered and provide 10 MA MAX CURRENT.

Time:	
Trip Time (4/0)	4.0 to 4.5 Milliseconds (adjustable from 2.0 to 6.0 MS)
Transient Block and Transient Unblock Time (18/0):	17 to 20 milliseconds (adjustable from 12 to 30 MS) (Relays may be ordered with a transient blocking time of 24 to 27 milliseconds)
Low Signal Lock-out Time:	130 to 180 Milliseconds
Loss of Potential Time (500/500)	400 to 600 Milliseconds
Dimensions:	relay height-5.25"(3 rack units) relay width - 19" relay depth - 14"
Weight:	approximately 15 lbs.

SETTINGS

No setting is required on the STU-12 relay.

INSTALLATION

The STU-12 relay is generally supplied in a cabinet or on a relay rack as part of a complete system. The location must be free from dust, excessive humidity, vibration, corrosive fumes or heat. The maximum temperature around the chassis must not exceed 55 C.

The outline and drilling plan of the STU-12 relay is shown in Fig. 43.

ADJUSTMENTS & MAINTENANCE

Acceptance Check

It is recommended that an acceptance check be applied to the STU-12 relay to verify that the circuits are functioning properly. The following procedure can be used for this purpose.

Connect the STU-12 relay to the test circuit of Fig. 42. Apply rated dc to J1 terminals 3 and 4 as shown, and use an auxiliary 20 volt regulator or the internal 20 volts of the STU-12 relay for the inputs to the switches. On STU-12 relays for use with the electro-mechanical protective relays, rated positive dc must be applied to the protective relay switches.

Note that the low signal switches for channel 1 and 2 are normally closed and all other switches are open.

Since the STU-12 relay varies in logic depending on the channel equipment, insure that it is checked per the proper channel. When reference is made to AL relay, this refers to STU-12 relays for use only with electro-mechanical systems utilizing elec-mech protective relays.

When reference is made to TEST TERMINAL, this means one of the 10 test terminals on the TEST BD. in board slot O. All voltages are to be measured with respect to negative, TEST TERMINAL 10. Voltage measurements may vary by +10%. Information in this acceptance test applies to a relay with a transient blocking time of 18 MS. For relays with a transient blocking time of 25 MS., limits are 24 to 27 milliseconds.

A. Normal Condition

TEST TERMINAL 1: 0 Volts
" " 2: 20 Volts
" " 3: 0 Volts
" " 4: 0 Volts
" " 5: 0 Volts
" " 6: 0 Volts
" " 7: 0 Volts
" " 8: 20 Volts
" " 9: 20 Volts

Keying AR — Not picked up
Trip AR — Not picked up
Loss of Channel AL — Picked up (Elec-Mech System)
Loss of Potential AL—Picked up (Elec-Mech System)

B. Channel Logic - 2 Term Line Relay Only
(For 3 Term Line relays, disregard this section and continue on section C)

1. TCF Carrier Channel
   a. Channel Trip-2500/0 MS timer (TIMING BD.), 0/1000 MS timer
      Close Trip-1 switch
      Test Term 2: Voltage drop from 20 to 0 volts in 18 to 20 milliseconds, then rise from 0 to 20 volts in 3100 to 4100 milliseconds.
      Test Term 4: Voltage rise from 0 to 20 volts
      Open Trip-1 switch
   b. Loss of Channel
      Open LOW SIGNAL - 1 switch
      Test Term 6: Voltage rise from 0 to 20 volts
      Loss of Channel AL will drop out
      Close LOW SIGNAL - 1 switch
2. Tone Channel
   a. Channel Trip - 2500/0 MS timer (TIMING BD.) 0/1000 MS timer (ARMING BD.), transient blocking timer
      Close Trip-1 switch
      Test Term 2: Voltage drop from 20 to 0 volts in 18 to 20 milliseconds, then rise from 0 to 20 volts in 3100 to 4100 milliseconds.
      Test Term 4: Voltage rise from 0 to 20 volts
      Open Trip-1 switch
   b. Loss of channel-150/100 MS timer (CHANNEL SUPERVISION BD.)
      Open LOW SIGNAL-1 switch
      Test Term 6: Voltage rise from 0 to 20 volts in 130 to 180 milliseconds
      Loss of Channel AL will drop out
      Close LOW SIGNAL - 1 switch
      Test Term 6: Voltage drop from 20 to 0 volts in 75 to 125 milliseconds.
   c. Guard Return
      Open LOW SIGNAL-1 switch, then close Trip-1 switch
      Test Term 4: Voltage must remain at zero
      Close LOW SIGNAL - 1 switch
      Test Term 6: Voltage must remain at 20 zero
      Open Trip-1 switch
      Test Term 6: Voltage must drop from 20 to 0 volts

C. Channel Logic - 3 Term Line Relays Only
(For 2 Term Line relays, the preceding section was used and this part may be disregarded)

1. TCF Carrier Channel

   a. Channel 1-Trip 2500/0 MS timer (TIMING BD.), 0/1000 MS timer (ARMING BD.), transient blocking timer

   Close Trip - 1 switch

   Test Term 2: Voltage drop from 20 to 0 volts in 18 to 20 milliseconds then rise from 0 to 20 volts in 3100 to 4100 milliseconds

   Test Term 4: Voltage remains at zero

   Open Trip-1 switch

   b. Channel 2-Trip 2500/0 MS timer (TIMING BD.), 0/1000 MS timer (ARMING BD,), transient blocking timer

   Close Trip - 2 switch

   Test Term 2: Voltage drop from 20 to 0 volts in 18 to 20 milliseconds then rise from 0 to 20 volts in 3100 to 4100 milliseconds

   Test Term 4: Voltage must remain at zero

   Open Trip - 2 switch

   c. Channel 1 and 2 Loss of Channel

   Open LOW SIGNAL - 1 switch

   Test Term 6: Voltage rise from 0 to 20 volts

   Loss of Channel AL must drop out

   Close LOW SIGNAL - 1 switch, then open LOW SIGNAL - 2 switch

   Test Term 6: Voltage rise from 0 to 20 volts

   Loss of Channel AL must drop out

   Close LOW SIGNAL - 2 switch

   d. Channel 1 and 2 switches

   Test Term 4: Voltage rise from 0 to 20 volts

   Open Trip-1 and Trip-2 switches

2. Tone Channel

   a. Channel 1-Trip 2500/0 MS timer (TIMING BD.), 0/1000 MS timer (ARMING BD.), transient blocking timer

   Close Trip - 1 switch

   Test Term 2: Voltage drop from 20 to 0 volts in 18 to 20 milliseconds then rise from 0 to 20 volts in 3100 to 4100 milliseconds

   Test Term 4: Voltage remains at zero

   Open Trip - 1 switch

   b. Channel 2-Trip 2500/0 MS timer (TIMING BD.), 0/1000 MS timer (ARMING BD.) transient blocking timer

   Close trip - 2 switch

   Test Term 2: Voltage drop from 20 to 0 volts in 18 to 20 milliseconds then rise from 0 to 20 volts in 3100 to 4100 milliseconds

   Test Term 4: Voltage remains at zero

   Open Trip - 2 switch

   c. Guard Return - Channel 1 - Trip and Low Signal - 150/100 MS timer

   Open LOW SIGNAL - 1 switch

   Test Term 6: Voltage rise from 0 to 20 volts in 130 to 180 milliseconds

   Loss of Channel AL must drop out

   Close Trip - 1 switch, then close LOW SIGNAL - 1 switch

   Test Term 6: Voltage must remain at 20 volts

   Open Trip - 1 switch

   Test Term 6: Voltage must drop from 20 to 0 volts in 75 to 125 milliseconds

   d. Guard Return - Channel 2 - Trip and Low Signal - 150/100 MS timer

   Open LOW SIGNAL -2 switch

   Test Term 6: Voltage rise from 0 to 20 volts in 130 to 180 milliseconds

   Loss of Channel AL must drop out

   Close Trip - 1 switch, then close LOW SIGNAL - 1 switch

   Test Term 6: Voltage must remain at 20 volts

   Open Trip - 1 switch

   Test Term 6: Voltage must drop from 20 to 0 volts in 75 to 125 milliseconds

   e. Channel 1 and 2 - Trip and Low Signal

   Close Trip-1 and Trip-2 switches

   Test Term 4: Voltage rise from 0 to 20 volts

Open LOW SIGNAL - 1 switch

Test Term 4: Voltage drop from 20 to 0 volts

Open Trip-1 and Trip-2 switches, then close LOW SIGNAL - 1 switch

D. Weak Feed Logic Operation

1. Weak Feed Trip

a. Voltage relay operation

Close 27 switch

Test Term 3: Voltage rise from 0 to 20 volts

Open 27 switch, then repeat above using 59N switch

b. Block of weak feed trip (W.F.Logic 3 BD.) 21NS, 21S and IA/IC, and 52b (0/50 timer)

Close 59N switch

Close 21NS switch

Test Term 3: Voltage drop from 20 to 0 volts

Open 21NS switch

Close 21S and IA/IC switches

Test Term 3: Voltage drop from 20 to 0 volts

Open 21S and IA/IC switches

Close 52b switch

Test Term 3: Voltage drop from 20 to 0 volts

Open 52b switch

Test Term 3: Voltage rise from 0 to 20 volts in 38 to 62 milliseconds (0/50 timer)

Open 59N switch

2. Weak Feed Keying

(For 2 Term line relays, remove the output BD. (Slot N) for these tests to prevent a Pilot Trip operation)

a. Voltage Relay operation

Close 27 Switch

Test Term 5: Voltage remains at zero

Close Trip-1 switch

Test Term 5: Voltage rise from 0 to 20 volts

Open 27 switch, then close 59N switch

Test Term 5: Voltage rise from 0 to 20 volts in 6 to 10 milliseconds (0/6 timer)

Open 59N and Trip-1 switch

b. Block of weak feed keying (W.F.Logic 2 & 4 BDS.) 21NS. 21S and IA/IC, 52b, 10/0 timer, 4/80 timer, 0/6 timer

Close Trip-1 switch

Close 59N switch

Test Term 5: Voltage rise from 0 to 20 volts

Close 21NS switch

Test Term 5: Voltage drop from 20 to 0 volts in 2.4 to 4.0 milliseconds (4/80 timer)

Open 21S switch

Test Term 5: Voltage rise, from 0 to 20 volts in 60 to 100 milliseconds (4/80 timer)

Open 59N switch, then close 27 switch

Close 21D switch, then IA/IC switch

Terminal 3 (W.F. Logic 2 BD.): Voltage rise from 0 to approx. 7 volts in 6 to 10 milliseconds (10/0 timer)

Test Term 5: Voltage drop from 20 to 0 volts

Open 21S and IA/IC switches

Test Term 5: Voltage must remain at zero.

Close 52b switch

Terminal 3 (W.F. Logic 2 BD.): Voltage must drop from 7 to 0 volts

Test Term 5: Voltage will rise from 0 to 20 volts

Open 52b switch

Test Term 5: Voltage must drop from 20 to 0 volts

Open 27 switch

(Re insert OUTPUT BD. into Slot N)

E. Strong Feed Operation

1. 21P or 21NP (67N) Keying and trip

Close 21P switch

Test Term 3 & 5: Voltage rise from 0 to 20 volts

Open 21P switch and repeat above fro 21NP switch

2. Loss of potential (500/500 timer - W.F. Logic 1 BD.)

Close 21S switch

Test Term 7: Voltage rise from 0 to 20 volts

in 400 to 600 milliseconds (500/500 timer)

Repeat above for 21NS switch

3. Block of Loss of Potential

Close Trip-1 and Trip-2 switches (Trip-2 switch not required for 2 Term Line relays)

Then close either 21S or 21NS switch

Test Term 7: Voltage must remain at zero

Open 21S (or 21NS,) Trip-1 and Trip-2 switches

4. Block of 21P (21NP) Keying and Trip

Close 21P switch

Then close 21S switch

Test Term 3: Voltage must drop from 20 to 0 volts in 0.5 sec.

Close 52b switch and 27 switch

Open 21S switch

Test Term 3: Voltage must remain at zero

Open 27 switch

Test Term 3: Voltage must rise from 0 to 20 volts

Open 52b and 21P switches

F. 52b Contact Operation - 180/0 MS timer (TIMING BD.)

Close 52b switch

Test Term 5: Voltage must rise from 0 to 20 volts in 180 to 230 milliseconds

Open 52b switch

G. Channel Checkback Operation

1. TCF Carrier Channel

2500/2500 MS timer (CHECKBACK BD.), check trip inputs

Open LOW SIGNAL - 1 switch

TP4 on CHECKBACK BD. voltage must drop from 8 to 0 volts in 2000 to 3000 milliseconds

Close CK-Trip-1 switch

Test Term 5: Voltage must rise from 0 to 20 volts immediately then drop from 20 to 0 volts in 2000 to 3000 milliseconds

XMTR KEY AR must pickup for 2 to 3 seconds

Close LOW SIGNAL-1 switch, then open CK Trip-1 switch

For relay used for 3 Term Line, also do the following:

Open LOW SIGNAL-2 switch and wait for 3 seconds, then close CK Trip-2 switch

Test Term 5: Voltage must rise from 0 to 20 immediately then drop from 20 to 0 volts in 2 to 3 seconds.

Close LOW SIGNAL-2 switch, then open CK Trip-2 switch

2. Tone Channel

2500/2500 MS timer (CHECKBACK BD.)

Open LOW SIGNAL-1 switch

TP4 on CHECKBACK BD.: Voltage must drop from 8 to 0 volts in 2000 to 3000 milliseconds

Close Trip-1 switch, then close LOW SIGNAL -1 switch

Test Term 5: Voltage must rise from 0 to 20 volts immediately then drop from 20 to 0 volts in 2000 to 3000 milliseconds

XMTR KEY AR must pick up for 2 to 3 seconds

Open Trip-1 switch

For relays used for 3 Term Line, also do the following:

Open both LOW SIGNAL-1 and LOW SIGNAL-2 switches then close Trip-2 switch. Wait for 3 seconds then close both LOW SIGNAL-1 and 2 switches

Test Term 5: Voltage must rise from 0 to 20 volts immediately after closing both the LOW SIGNAL switches then drop from 20 to 0 volts in 2 to 3 seconds

Open Trip-2 switch

H. Pilot Trip - 4/0 MS Timer (OUTPUT BD.)

Close 52b switch in order to prevent the 2500/0 MS timer from starting transient blocking

Close Trip-1 switch, and also, for 3 Term Line relays, close Trip-2 switch

Then, close 21P Switch

Test Term 1: Voltage must rise from 0 to 20 volts in 4.0 to 4.5 milliseconds

Trip AR must pickup

Open Trip-1 and Trip-2 switches

Test Term 1: Voltage must remain at 20 volts

Open 21P switch and Trip AR must drop out

Open 52b switch

I. Pilot Trip After Transient Unblocking 18/0 MS Timer (OUTPUT BD.)

Close 21P switch

Then, close Trip-1 switch, and also for 3 Term Line relays, close Trip-2 switch

Test Term 1: Voltage drop from 20 to 0 volts 18 to 20 milliseconds

Open 21P switch

Test Term 1: Voltage drop from 20 to 0 volts.

Open Trip-1 and Trip-2 switches

Repeat above tests except use switch 27 or 59N in place of 21P switch

J. Continue Key after pilot trip-0/30 MS Timer

Close 21P switch

Close Trip-1 switch and for 3 Term Line relays, also close Trip-2 switch

As soon as the voltage on Test Term 1 rises from 0 to 20 volts then the 0/30 MS timer will pickup

Then open 21P switch

Test Term 5: Voltage must drop from 20 to 0 volts in 24 to 30 milliseconds

Open Trip-1 and Trip-2 switches

K. Fast Reset of 0/1000 MS timer after pilot trip .0/100 MS timer (ARMING BD.)

For checking this 0/1000 MS timer, it will be necessary to use a jumper

Close 21P switch, then close Trip-1 switch and also for 3 Term Line relays close Trip-2 switch

Terminal 4 (ARMING BD.): Voltage must rise from 0 to 16 volts in less than 2 milliseconds after the voltage at Test Term 1 rises from 0 to 20 volts

In order to check the 100 millisecond reset time, it is necessary to connect a jumper from TP-8 to terminal 14 on the ARMING BD.

Open 21P switch

Terminal 4 (ARMING BD.): Voltage must drop from 16 to 0 volts in 70 to 170 milliseconds

Open Trip-1 and Trip-2 switches, and remove the jumper

L. Contact Bounce Circuits (Weak Feed (W.F.) Logic 1 and 3 BDS.)

This section is to be used only for those STU-12 relays which are for use with electromechanical protective relays

Close 21P switch

Terminal 2 (W.F. Logic 1 and 3 Bds.): Voltage must rise from 0 to 20 volts immediatly then drop back to zero in approximately 20 milliseconds

Open 21P switch

M. Noise Operation (tones only)

This section is to be used only for those STU-12 relays which are for use with a frequency shift tone channel.

Close NOISE-1 switch

Then close 21P switch and Trip-1 switch, and also for 3 Term Line relays close Trip-2 switch

Test Term 1: Voltage must remain at zero

Open Noise-1 switch

Test Term 1: Voltage must rise from 0 to 20 volts

Trip AR must pickup

Open 21P, Trip-1 and Trip-2 switches

For 3 Term Line relays, repeat above test using Noise-2 switch instead by Noise-1 switch.

Recommended Routine Maintenance

Periodic checks of the relaying system are desirable to indicate impeding failure so that the equipment can be taken out of service for correction. Any accumulated dust should be removed at regular maintenance intervals.

All contacts should be periodically cleaned. A contact burnisher, Style No. 182A836H01, is recommended. The use of abrassive material is not recommended because of the danger of embedding small particles in the face of the soft silver and thus imparing the contact.

CALIBRATION

The proper adjustments to insure correct operation of the relay have been made at the factory and should not be disturbed after receipt by the customer. However, if the adjustments or if the components or printed circuit boards which affect calibration have have changed, then the STU-12 relay should be rechecked per the acceptance check information.

All time delays are fixed except for the three timers on the OUTPUT BD.: 18/0 (25/0) MS transient blocking timer. These adjustable timers can be recalibrated as follows using an auxiliary timer or oscilloscope.

Transient Block 18/0 MS Timer – OUTPUT BD.

(NOTE: For relays having a transient blocking timer of 25/0 MS limits are 24 to 27 milliseconds.

Start timer on 21P switch (positive pulse)
End timer on Test Term 2 (negative pulse)

Close 21P switch and the voltage on Test Term 2 must drop from 20 to 0 volts in 18 to 20 milliseconds (24 to 27 MS)

This time can be adjusted by turning potentiometer R14 on the OUTPUT clockwise for more time or counter clockwise for less time. (After recalibrating this timer also recheck the calibration of the 4/0 MS timer.)

Pilot Trip 4/0 MS Timer – OUTPUT BD.

Start Timer on 21P switch (positive pulse)
End timer on Test Term 1 (positive pulse)

For this calibration, close 52b switch

Close Trip-1 switch, and also Trip-2 switch for 3 Term Line relays

Then close 21P switch and the voltage on Test Term 1 must rise from 0 to 20 volts in 4.0 to 4.5 milliseconds

This timer can be adjusted by turning potentiometer R20 on the OUTPUT BD.clockwise for more time and counter-clockwise for less time.

(After recalibrating this timer, also recheck calibration of the 18/0 MS transient block timer.)

Transient Unblocking 18/0 MS Timer-OUTPUT BD.

Start timer on Trip-1 switch (positive pulse)

End timer on Test Term 1 (positive pulse)

Close 21P switch, and also close Trip-2 switch for 3 Term Line relays

Then close Trip-1 switch and the voltage on Test Term 1 must rise from 0 to 20 volts in 18 to 20 milliseconds.

This time can be adjusted by turning potentiometer R1 on the OUTPUT BD. clockwise for more time and counter-clockwise for less time.

Tripping Relay (AR)

The type AR tripping relay unit has been properly adjusted at the factory to insure correct operation and should not be disturbed after receipt by the customer. If, however, the adjustments are disturbed in error, or it becomes necessary to replace some part in the field, use the following adjustment procedure. This procedure should not be used until it is apparent that the AR unit is not in proper working order, and then only if suitable tools are available for checking the adjustments.

a. Adjust the set screw at the top of the frame to obtain a 0.009 inch gap at the rear end of the armature air gap.

b. Adjust each contact spring to obtain 4 grams pressure at the very end of the spring. This pressure is measured when the spring moves away from the edge of the slot in the insulated crosspiece.

c. Adjust each stationary contact screw to obtain a contact gap of 0.020 inch. This will give 15-30 grams contact pressure.

Trouble Shooting

The components of the STU-12 relay are operated well within their ratings and normally will give long and trouble-free service. However, if a relay has given an indication of trouble in service or during routine check, then using "0" and "1" logic notation, the faulty printed circuit board can be traced to using the diagrams in Fig. 4, 5, 6, or 7. In turn, the faculty, component or circuit can be found using the individual schematic of the printed circuit boards which show the detailed transistor NOR/NAND logic-

Each NOR/NAND logic block represents a transistor on the schematic. The output of each individual logic block is the collector of the transistor which represents that block. The collector of each transistor is either connected to a test point or printed circuit terminal. A box around the transistor indicates that it is conducting for the normal condition of the relay.

Following is an explanation of the voltage levels for the "0" and "1" logic notation as shown for the normal relay condition in Figs. 4, 5, 6, and 7. This logic notation will also apply to the detailed logic on the printed circuit board internal schematics.

For positive logic – represented by logic blocks, with no arrows. "0" is equivalent to less than 0.5 volts with respect to negative, Test Term 10.

"1" is equivalent to 8 to 20 volts with respect to negative, Test Term 10)

For negative logic - represented by logic blocks with open arrow heads, "0" is equivalent to 8 to 20 volts with respect to negative, Test Term 10, except for the output of the relay driver, where a "0" is rated positive dc.

"1" is equivalent to less than 0.5 volts with respect to negative, Test Term 10.

A board extender, Style No. 849A534G01, is available for facilitating circuit voltage measurements. After withdrawing anyone of the circuit boards, the extender is inserted into that slot. The board is then inserted into the terminal block on the front of the extender to restore all circuit connections.

The Test Terminals on the Test Bd. in the board position to the extreme right are helpful in checking the overall relay operation. Following are the voltages that will occur at these Test Terminals under various conditions:

NOTE: All voltages referred to are taken with respect to negative, Test Terminal 10.

Test Terminal 1: Pilot Trip

Normal Condition – 0 volts
Internal Fault – 20 volts

For an internal fault, either a forward reaching relay (21P or 21NP(67N)) or a voltage relay (27 or 59N) operation and both receiver trip signals (one receiver trip signal for 2 Term Line relays are required.

Test Terminal 2: Transient Blocking & Unblocking

Normal Condition – 20 volts
External Fault – 0 volts

The following will simulate an external fault:

21P or 21NP (67N) operation
27 or 59N operation
either channel receiver trip operation

Test Terminal 3: Protective Relay

Normal Operation – 0 volts
21P or 21NP(67N) Operation - 20 volts
27 or 59N Operation - 20 volts

Test Terminal 4: Channel Trip

Normal Condition - 0 volts

Operation of Channel 1 and 2 receiver trip outputs-(for 2 Term Line relays, only 1 channel required)-20 volts

Test Terminal 5: XMTR Key

Normal Condition - 0 volts
21P or 21NP(67N) Operation - 20 volts
52b contact operation - 20 volts
Internal Fault (pilot trip signal) - 20 volts
27 or 59N and received trip signal 1 or 2 – 20 volts
Channel Checkback scheme—20 volts for 2.5 seconds

Test Terminal 6: Loss of Chennel

Normal Condition - 0 volts
Operation of either channel 1 or 2 Low signal clamp-20 volts.

Test Terminal 7: Loss of Potential

Normal Condition - 0 volts

21NS(67NS) or 21S operation—20 volts after 500 MS time delay

21NS(67NS) or 21S and both receiver trip signal operation (one receiver trip signal for 2 Term Line relays) - 0 volts

Test Terminal 8 and 9: Pos. 20 V DC

Normal Condition - 0 volts

Test Terminal 10: Negative DC

RENEWAL PARTS

Repair work can be done most satisfactorily at the factory. However, interchangeable parts can be furnished to the customers who are equipped for doing the repair work. When ordering parts, always give the complete nameplate data, and the component Style No. given in the Electrical Parts List.

ELECTRICAL PARTS LIST

CIRCUIT SYMBOL	REFERENCE	STYLE
POWER SUPPLY BOARD – S#202C465G01		
Capacitors		
C1, C2	6.8 MFD, 35 V, ±20%	184A661H10
Diodes		
D1, D2	1N645A	837A692H03
Resistors		
None on PCB	None	
Transistors		
Q1, Q2	2N3589	837A617H01
Zener Diodes		
Z1, Z3	1N3050A (180 V - 1W)	187A936H16
Z2, Z4	1N4747A (20 V - 1W)	849A487H01
Heat Sink for A1 & Q2		849A517H01
WEAK FEED – S#6262D69G01 – ELEC. MECH. SYSTEM **LOGIC 1 BOARD – S#6262D69G02 – SOLID STATE SYSTEM**		
Capacitors		
C1, C2	.047 mfd, 200 VDC	849A437H04
C3, C4	22 mfd, 35 V DC	184A661H16
C5	.27 mfd, 200 V DC	188A669H05
C6	.47 mfd, 35 V DC	837A241H21
Diodes		
D1, D2, D3, D4, D5	1N645A	837A692H03
Resistors		
R1, R2, R7, R8 △	4.7 K, ½ W, ±2%	629A531H48
R1, R2, R7, R8 #	47 K, ½ W, ±2%	629A531H72
R3, R9	4.7K, ½ W, ±2%	629A531H48
R4, R10, R27, R45	82K, ½ W, ±2%	629A531H78
R5, R11, R15, R18, R21, R24, R26, R30, R33, R37, R40, R43, R44	10 K, ½ W, ±2%	629A531H56
R6, R12, R16, R25, R31, R38	6.8K, ½ W, ±2%	629A531H52
R13, R14, R17, R29, R34, R35, R36, R39, R41	27K, ½ W, ±2%	629A531H66
R19	39K, ½ W, ±2%	629A531H70
R20, R23	470 ohms, ½ W, ±2%	629A531H24
R22	47 K, ½ W, ±2%	629A531H72
R28	150 Ohms, 3 W, ±5%	762A679H01
R32	1K, ½ W, ±2%	629A531H32
Transistors		
Q1, Q2, Q3, Q4, Q5, Q6, Q8, Q10, Q11	2N3417	848A851H02
Q7, Q12	2N3645	849A441H01
Q9	2N3589	837A617H01

△ – Solid State Systems

– Elec. Mech Systems

ELECTRICAL PARTS LIST

CIRCUIT SYMBOL	REFERENCE	STYLE
WEAK FEED LOGIC 1 BOARD (continued)		
Zener Diodes		
Z1, Z2, Z5, Z6, Z11	IN3688A	862A288H01
Z3, Z7	IN3686B	185A212H06
Z4, Z8, Z9, Z10	IN957B	186A797H06
Z12	IN3050B	187A936H17
WEAK FEED LOGIC 2 BOARD S#6262D57G01 – SOLID STATE SYSTEMS S#6262D57G02 – ELEC. MECH. SYSTEMS		
Capacitors		
C1, C2, C3	.047 mfd, 200 VDC	849A437H04
C4	.15 mfd, 35 VDC	837A241H13
Diodes		
D1, D2, D3, D4, D5	IN645A	837A692H03
Resistors		
R1, R6, R12 Δ	4.7K, ½W, ± 2%	629A531H48
R1, R6, R12 #	47K, ½W, ± 2%	629A531H72
R2, R7, R13	4.7K, ½W, ± 2%	629A531H48
R3, R8, R14	82K, ½W, ± 2%	629A531H78
R4, R9, R15, R20, R23, R28, R30, R33, R36	10K, ½W, ± 2%	629A531H56
R5, R11, R17, R21, R24, R29, R34, R37	6.8K, ½W, ± 2%	629A531H52
R10, R16, R18, R19, R22, R25, R26, R27, R35	27K, ½W, ± 2%	629A531H39
R31	2K, ½W, ± 2%	629A531H60
R32	15K, ½W, ± 2%	
Transistors		
Q1, Q2, Q3, Q4, Q5, Q6, Q8, Q9	2N3417	848A851H02
Q7	2N3645	849A441H01
Zener Diodes		
Z1, Z3, Z5	IN3686B	185A212H06
Z2, Z4, Z6	IN957B	186A797H06
WEAK FEED LOGIC 3 BOARD S#6262D65G01 – SOLID STATE SYSTEMS S#6262D65D02 – ELEC. MECH. SYSTEMS		
Capacitors		
C1	3.3 mfd, 35 VDC	862A530H01
C2, C3	.047 mfd, 200 VDC	849A437H04
C4	.47 mfd, 35 VDC	837A241H21
Diodes		
D1, D2, D3, D4, D5	IN645A	837A692H03

Δ – Solid State Systems

– Elec. Mech. Systems

ELECTRICAL PARTS LIST

CIRCUIT SYMBOL	REFERENCE	STYLE
WEAK FEED LOGIC 3 BOARD (continued)		
Resistors		
R1, R7, R14, R20, R21, R22, R24, R25, R30, R32	27K, ½W, ± 2%	629A531H66
R2, R5, R8, R13, R17, R26, R28, R31, R33, R35	10K, ½W, ± 2%	629A531H56
R3	30K, ½W, ± 2%	629A531H67
R4	470 ohm, ½W, ± 2%	629A531H24
R6, R9, R15, R23, R27	6.8K, ½W, ± 2%	629A531H52
R10, R16 Δ	4.7K, ½W, ± 2%	629A531H48
R10, R16 #	47K, ½W, ± 2%	629A531H72
R11, R17	4.7K, ½W, ± 2%	629A531H48
R12, R18, R29, R36	82 K, ½W, ± 2%	629A531H78
R34	15K, ½W, ± 2%	629A531H60
Transistors		
Q1, Q2, Q3, Q4, Q5, Q6, Q8	2N3417	848A851H02
Q7, Q9	2N3645	849A441H01
Zener Diodes		
Z1, Z3, Z5	IN957B	186A797H06
Z2, Z4	IN3686B	185A212H06
WEAK FEED LOGIC 4 BOARD S#6262D74G01 – SOLID STATE SYSTEM S#6262D74G02 – ELEC. MECH. SYSTEM		
Capacitors		
C1	.047 mfd, 200 VDC	849A437H04
C2	4.7 mfd, 35 VDC	184A661H12
C3	.47 mfd, 35 VDC	837A241H21
Diodes		
D1, D3, D4, D5, D6	IN645A	837A692H03
Resistors		
R1, R2, R5, R6, R12, R14, R15, R22, R29, R31, R32, R33	27K, ½W, ± 2%	629A531H66
R3, R7, R13, R20, R23, R26, R28, R34	10K, ½W, ± 2%	629A531H56
R4, R8, R16, R19, R21, R27, R30, R35	6.8K, ½W, ± 2%	629A531H52
R9 Δ	4.7K, ½W, ± 2%	629A531H48
R9 #	47K, ½W, ± 2%	629A531H72
R10	4.7K, ½W, ± 2%	629A531H48
R11	82K, ½W, ± 2%	629A531H78
R17	22K, ½W, ± 2%	629A531H64
R18	2.7K, ½W, ± 2%	629A531H42
R24	33K, ½W, ± 2%	629A531H68
R25	470 ohms, ½W, ± 2%	629A531H24
Transistors		
Q1, Q2, Q3, Q4, Q5, Q6, Q7, Q8	2N3417	848A851H02
Zener Diodes		
Z1	IN3686B	185A212H06
Z2, Z3, Z4	IN957B	186A797H06

Δ – Solid State System

– Elec. Mech. System

ELECTRICAL PARTS LIST

CIRCUIT SYMBOL	REFERENCE	STYLE
CHANNEL – S#202C530G01 – TCT INT. INTERFACE BOARD – S#202C469G01 – TA3 INT.		
Capacitors		
C1, C3, C5	.047 mfd, 200 V DC	849A437H04
C4, C6	.27 mfd, 200 V DC	188A669H05
Diodes		
D2, D3	1N645A	837A692H03
Resistors		
R1, R2, R9, R10, R17, R18	4.7 K, ½W, ± 2%	629A531H48
R3, R7, R11, R15, R19, R23	82 K, ½W, ± 2%	629A531H78
R4, R5, R12, R13, R20, R21, R26	10 K, ½W, ± 2%	629A531H56
R6, R14, R22, R27	6.8 K, ½W, ± 2%	629A531H52
R16, R24	150 ohm, 3W, ± 5%	762A679H01
R25	27 K, ½W, ± 2%	629A531H66
Transistors		
Q1, Q3, Q5, Q7	2N3417	848A851H02
Q2, Q4, Q6	2N3645	849A441H01
Zener Diodes		
Z1, Z4, Z7	1N3686B, 20 V, ± 5%	185A212H06
Z2, Z5, Z8	1N957B, 6.8 V, ± 5%	186A797H06
Z6, Z9, Z10	1N3688A, 24 V, ± 20%	862A288H01
CHANNEL – S#202C471G01 – TCF TRIP BOARD – S#202C472G01 – TONE		
Capacitors		
C1	0.27 mfd, 200 V	188A669H05
Diodes		
D1	1N645A	837A692H03
Resistors		
R1, R2, R5, R8, R11, R14, R17, R18, R21, R22, R25, R26, R29, R32, R33, R34, R37, R43	27 K, ½W, ± 2%	629A531H66
R3, R6, R9, R12, R15, R19, R23, R27, R30, R35, R38, R39	10K, ½W, ± 2%	629A531H56
R4, R7, R10, R13, R16, R20, R24, R28, R31, R36, R40	6.8 K, ½W ± 2%	629A531H52
R41	82 K, ½W, ± 2%	629A531H78
R42	150 ohm, 3 W, ± 5%	762A679H01

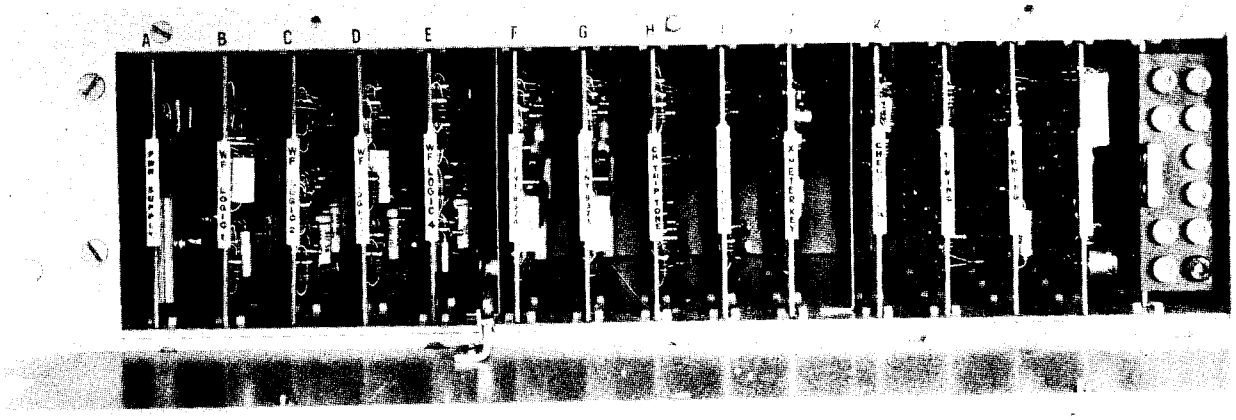


Fig. 1. Photograph (Front view with door open)

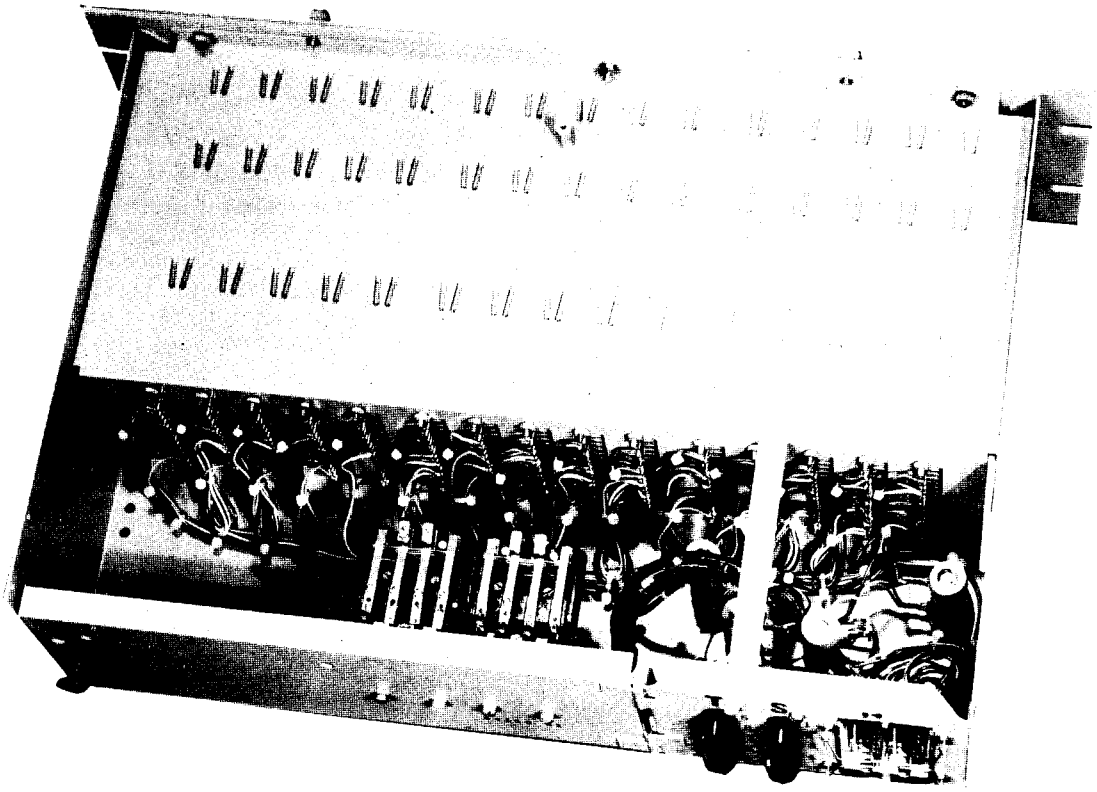
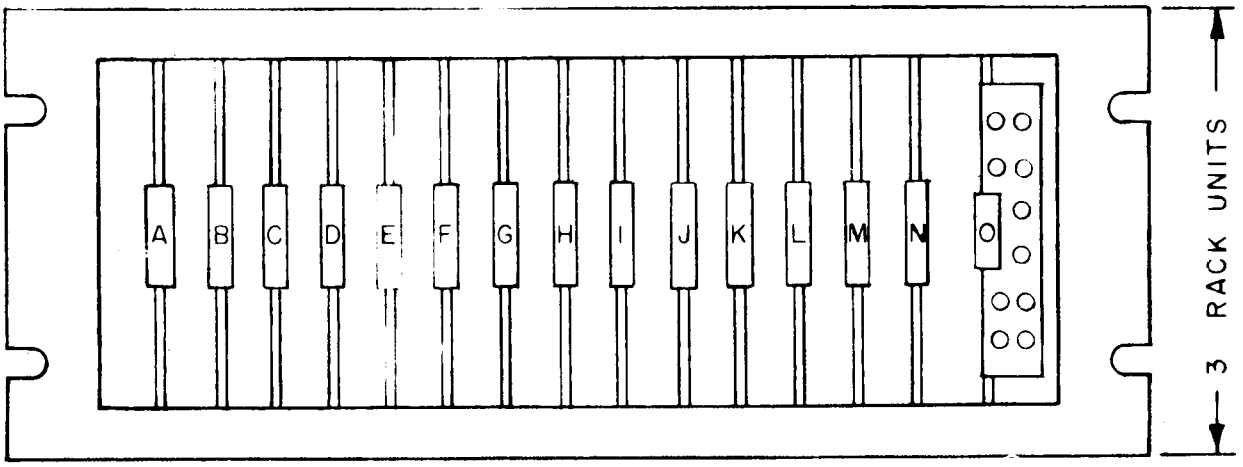


Fig. 2 Photograph (Rear view taken above relay with top cover off and door open)

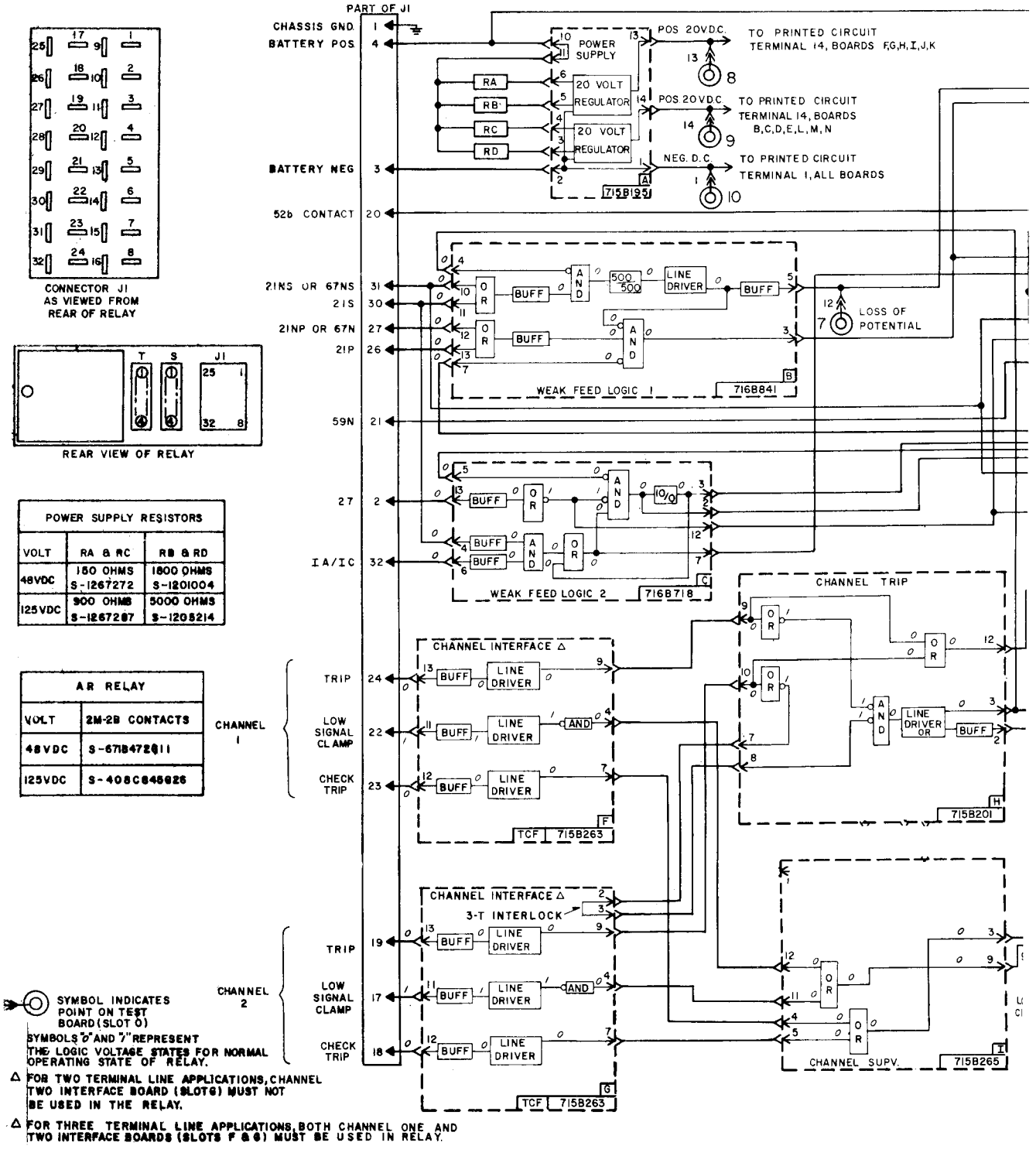


FRONT VIEW
(COVER REMOVED)

BOARD POSITION	BOARD DESCRIPTION
A	POWER SUPPLY
B	WEAK FEED LOGIC-1
C	WEAK FEED LOGIC-2
D	WEAK FEED LOGIC-3
E	WEAK FEED LOGIC-4
F	CHANNEL 1 INTERFACE
G	CHANNEL 2 INTERFACE
H	CHANNEL TRIP
I	CHANNEL SUPERVISION
J	CHANNEL TRANSMITTER KEY
K	CHECK BACK
L	TIMING
M	ARMING
N	OUTPUT
O	TEST

878A323

Fig. 3 Relay component location



CONNECTOR J1 AS VIEWED FROM REAR OF RELAY

REAR VIEW OF RELAY

POWER SUPPLY RESISTORS		
VOLT	RA & RC	RB & RD
48VDC	150 OHMS S-1267272	1800 OHMS S-1201004
125VDC	900 OHMS S-1267287	5000 OHMS S-1205214

AR RELAY	
VOLT	2M-2B CONTACTS
48VDC	S-671B472G11
125VDC	S-408C845G26

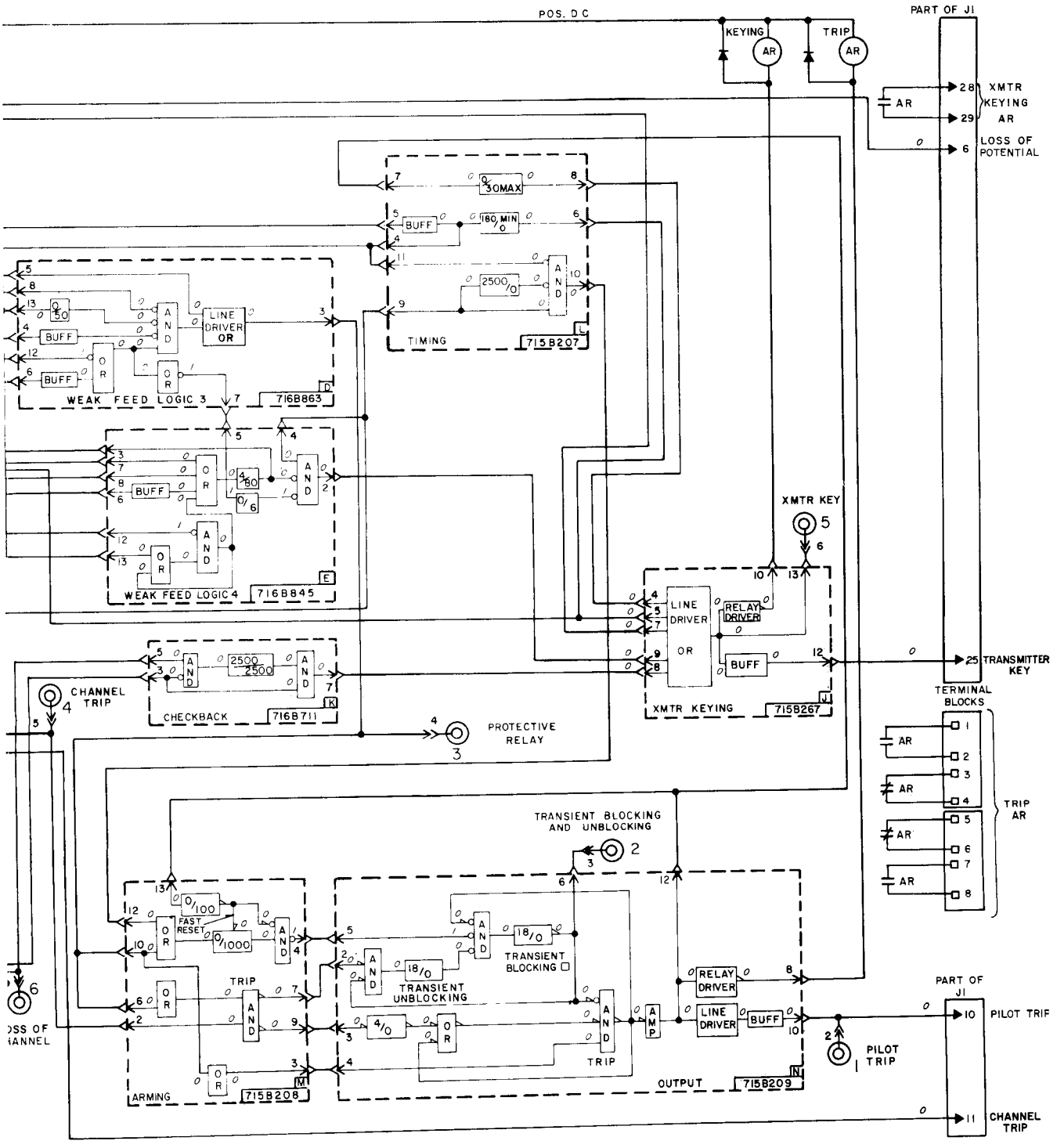
SYMBOL INDICATES POINT ON TEST BOARD (SLOT 0)

SYMBOLS "0" AND "1" REPRESENT THE LOGIC VOLTAGE STATES FOR NORMAL OPERATING STATE OF RELAY.

Δ FOR TWO TERMINAL LINE APPLICATIONS, CHANNEL TWO INTERFACE BOARD (SLOT G) MUST NOT BE USED IN THE RELAY.

Δ FOR THREE TERMINAL LINE APPLICATIONS, BOTH CHANNEL ONE AND TWO INTERFACE BOARDS (SLOTS F & G) MUST BE USED IN RELAY.

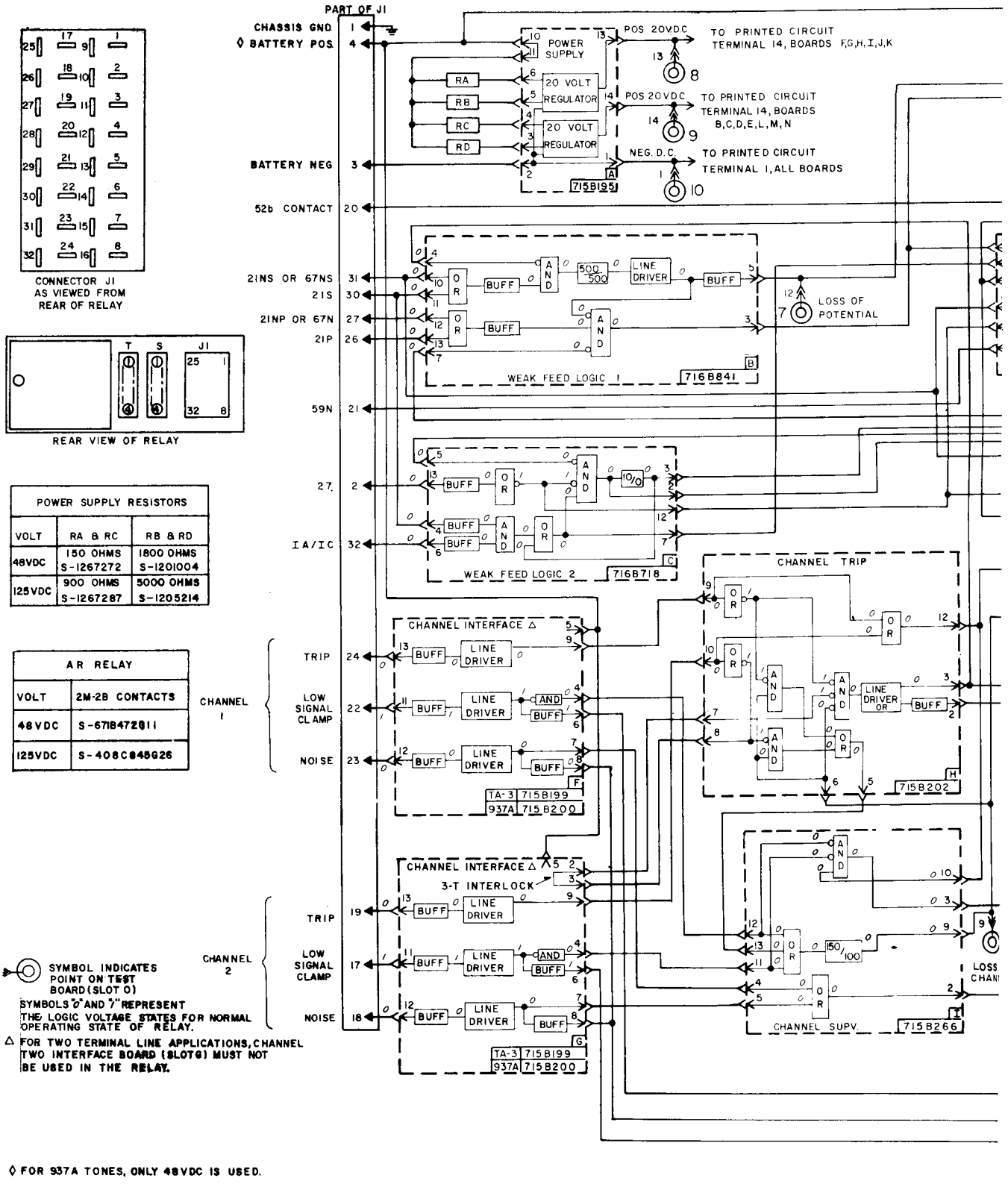
Fig. 5 STU-12 logic – for use with solid state protective



□:RELAY STYLES AVAILABLE WITH TRANSIENT BLOCK TIME OF 25 MILLISECONDS

6263D44

elays and a TCF carrier channel – for a weak feed terminal



CONNECTOR J1 AS VIEWED FROM REAR OF RELAY

REAR VIEW OF RELAY

POWER SUPPLY RESISTORS		
VOLT	RA & RC	RB & RD
48VDC	150 OHMS S-1267272	1800 OHMS S-1201004
125VDC	900 OHMS S-1267287	5000 OHMS S-1205214

AR RELAY	
VOLT	2M-2B CONTACTS
48VDC	S-67184726 11
125VDC	S-408C845G26

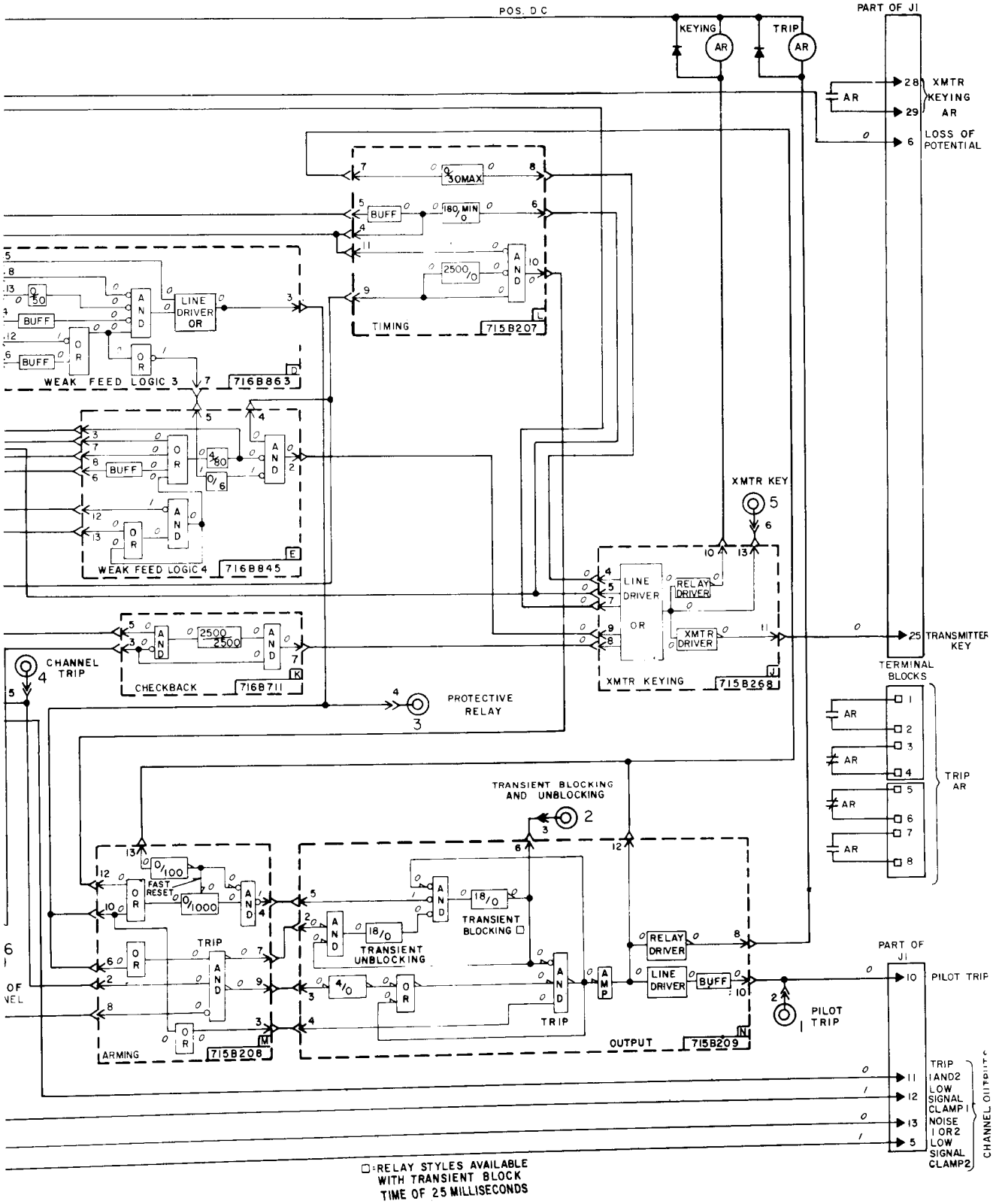
SYMBOL INDICATES POINT ON TEST BOARD (SLOT 0)

SYMBOLS "0" AND "1" REPRESENT THE LOGIC VOLTAGE STATES FOR NORMAL OPERATING STATE OF RELAY.

Δ FOR TWO TERMINAL LINE APPLICATIONS, CHANNEL TWO INTERFACE BOARD (SLOT G) MUST NOT BE USED IN THE RELAY.

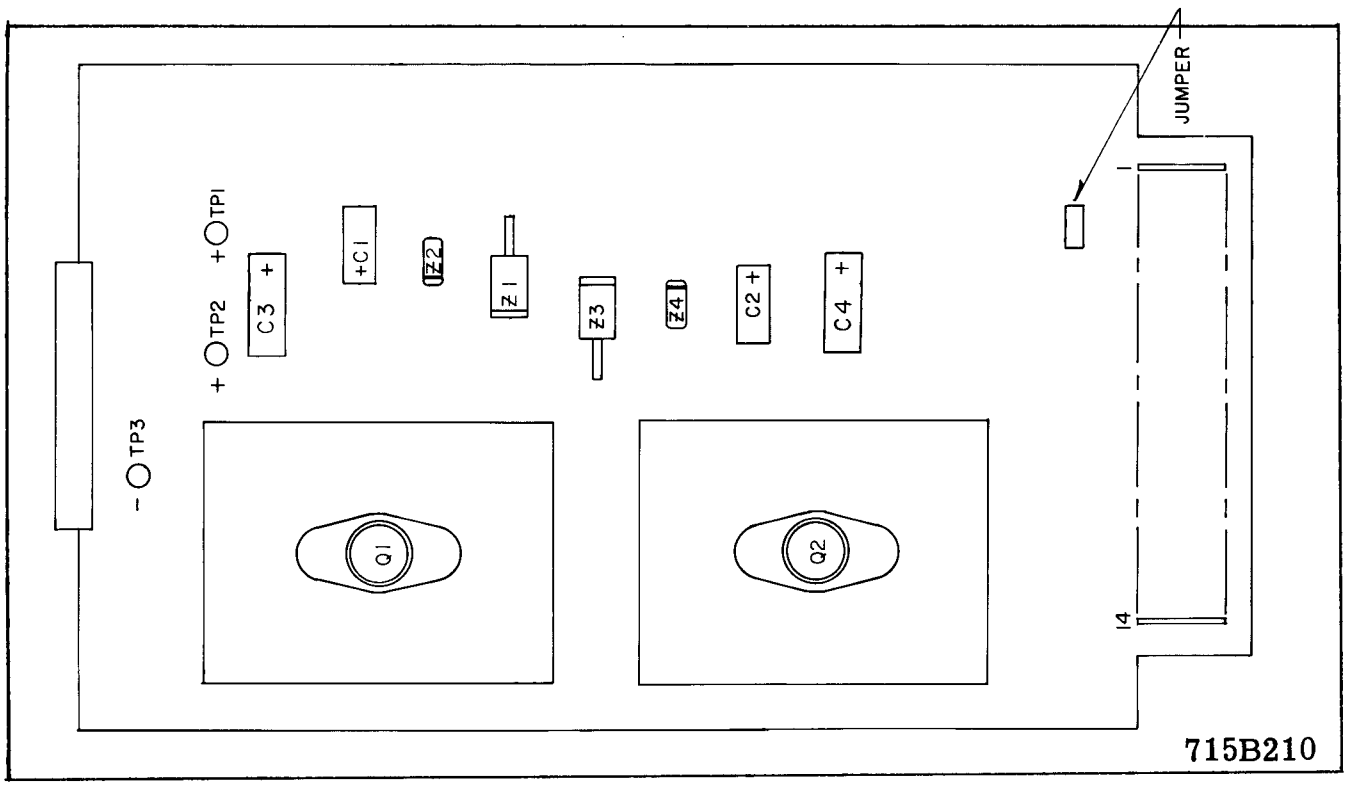
◊ FOR 937A TONES, ONLY 48VDC IS USED.

Fig. 7 STU-12 logic – for use with solid state protectiv

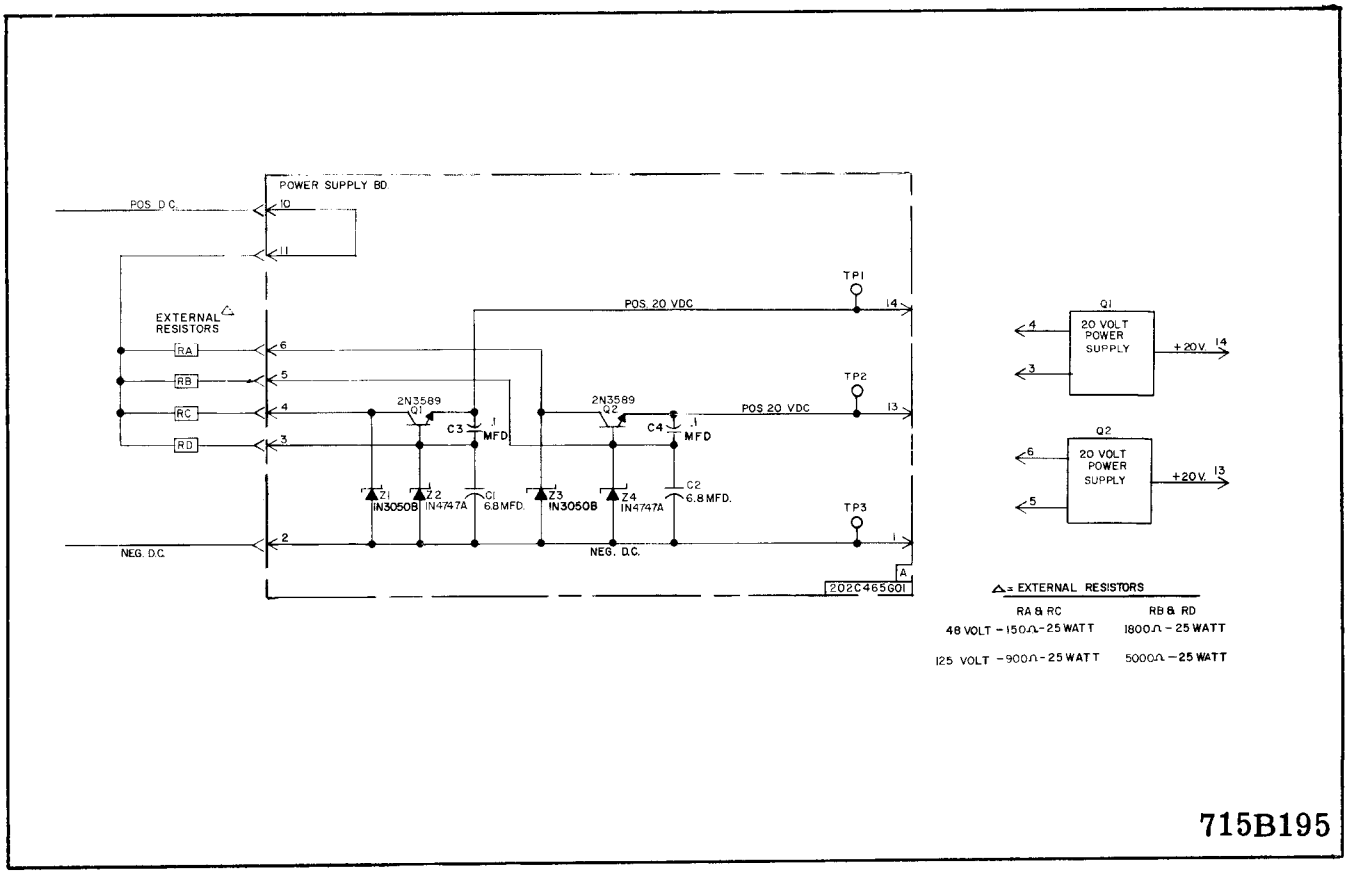


6263D46

...ays and a tone channel for a weak feed terminal



* *Fig. 8 Component Location Power Supply Board*



* *Fig. 9 Internal Schematic Power Supply Board*

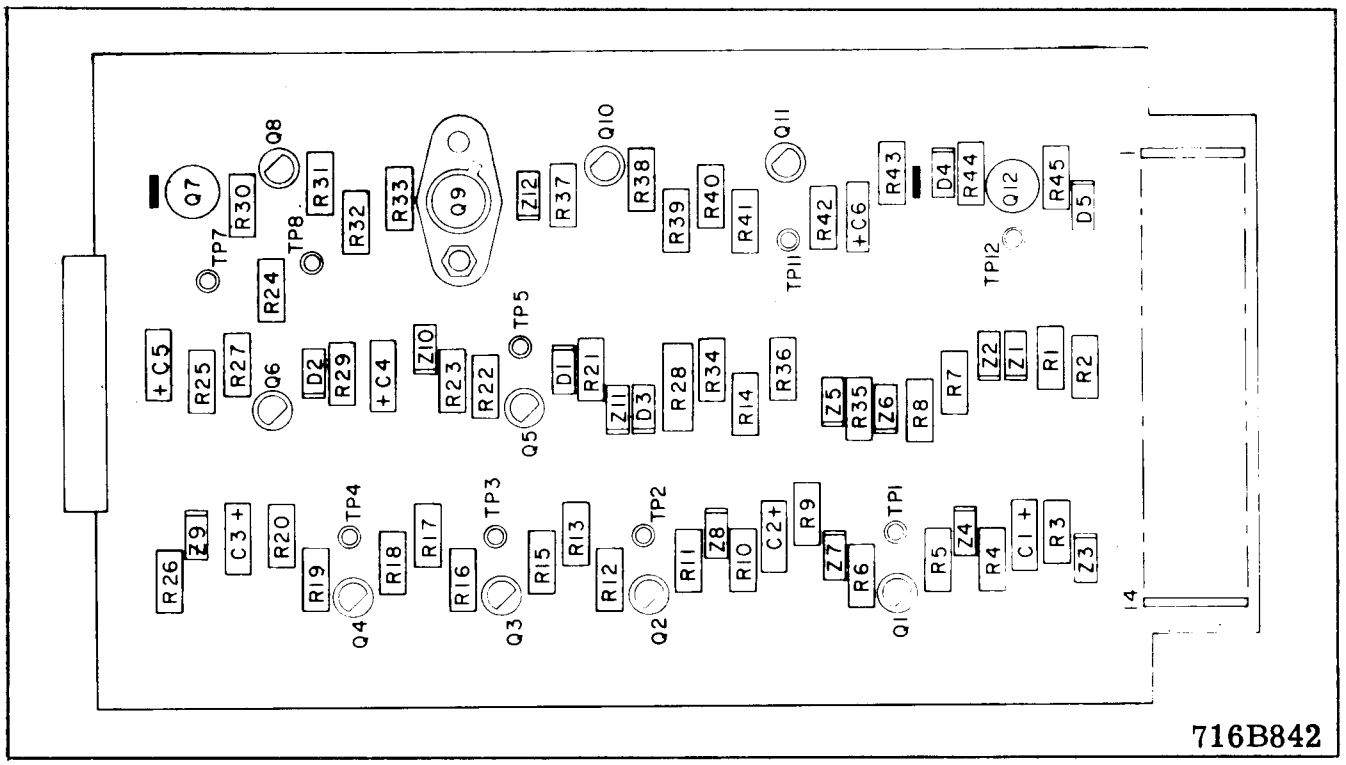


Fig. 10 Component Location – Weak Feed Logic 1 Board

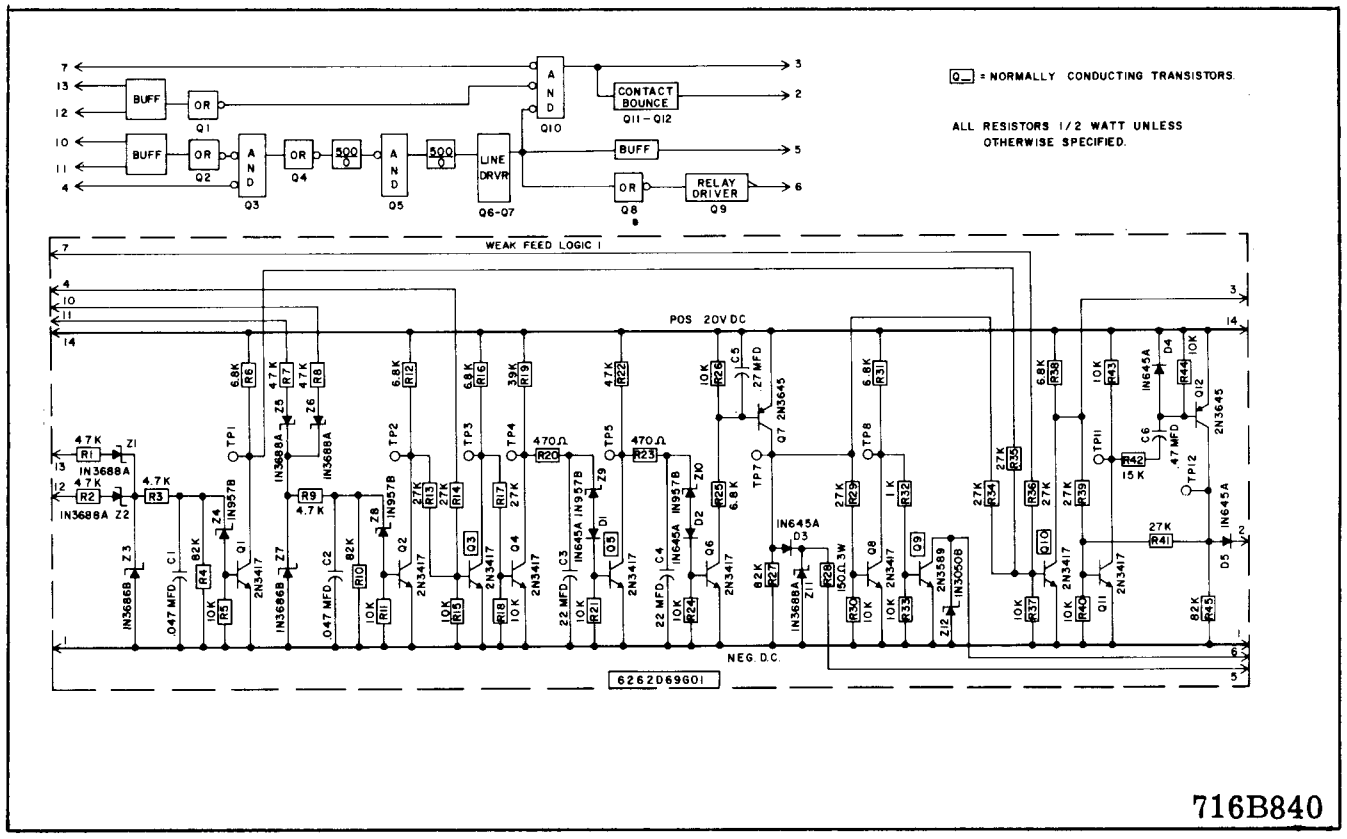


Fig. 11 Internal Schematic – Weak Feed Logic 1 Board for Elec. Mech. System

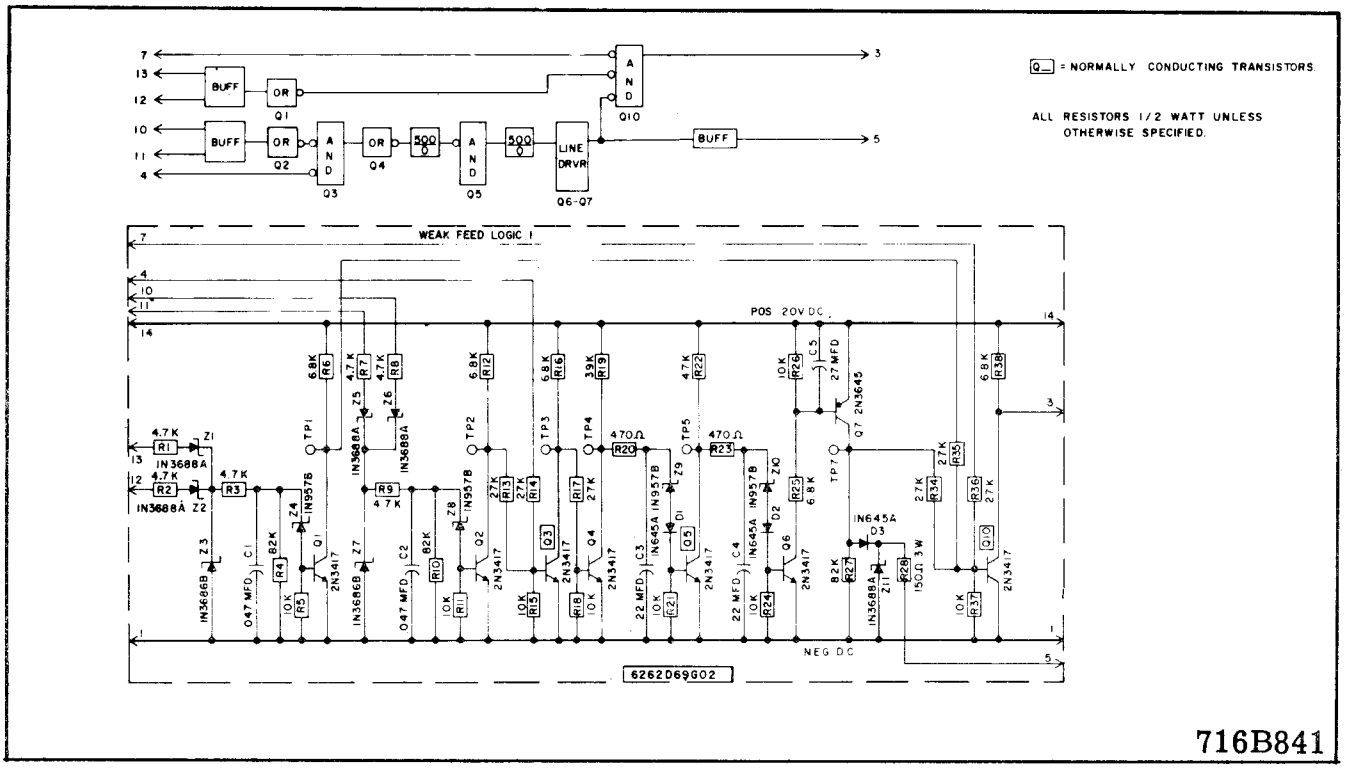


Fig. 12 Internal Schematic – Weak Feed Logic 1 Board for Solid State System

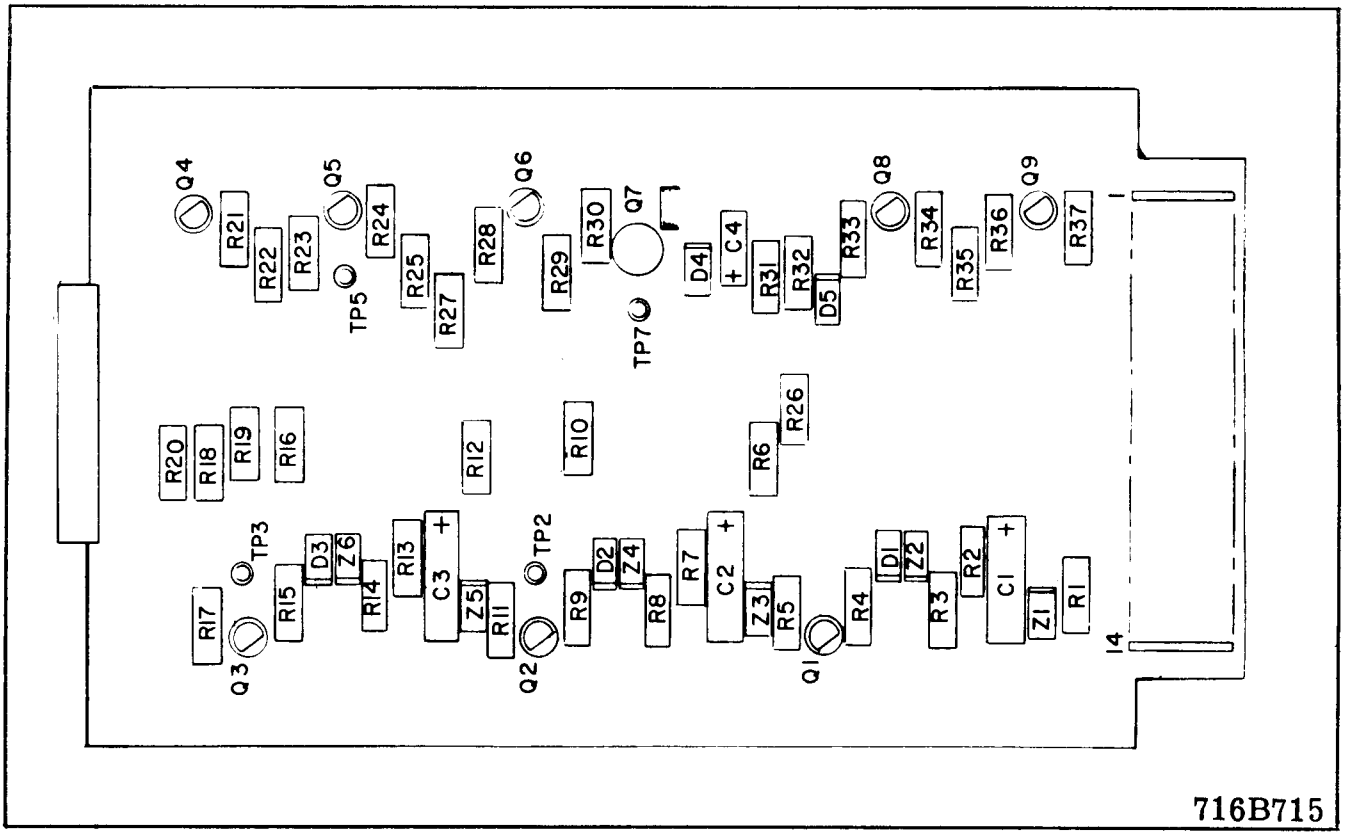


Fig. 13 Component Location – Weak Feed Logic 2 Board

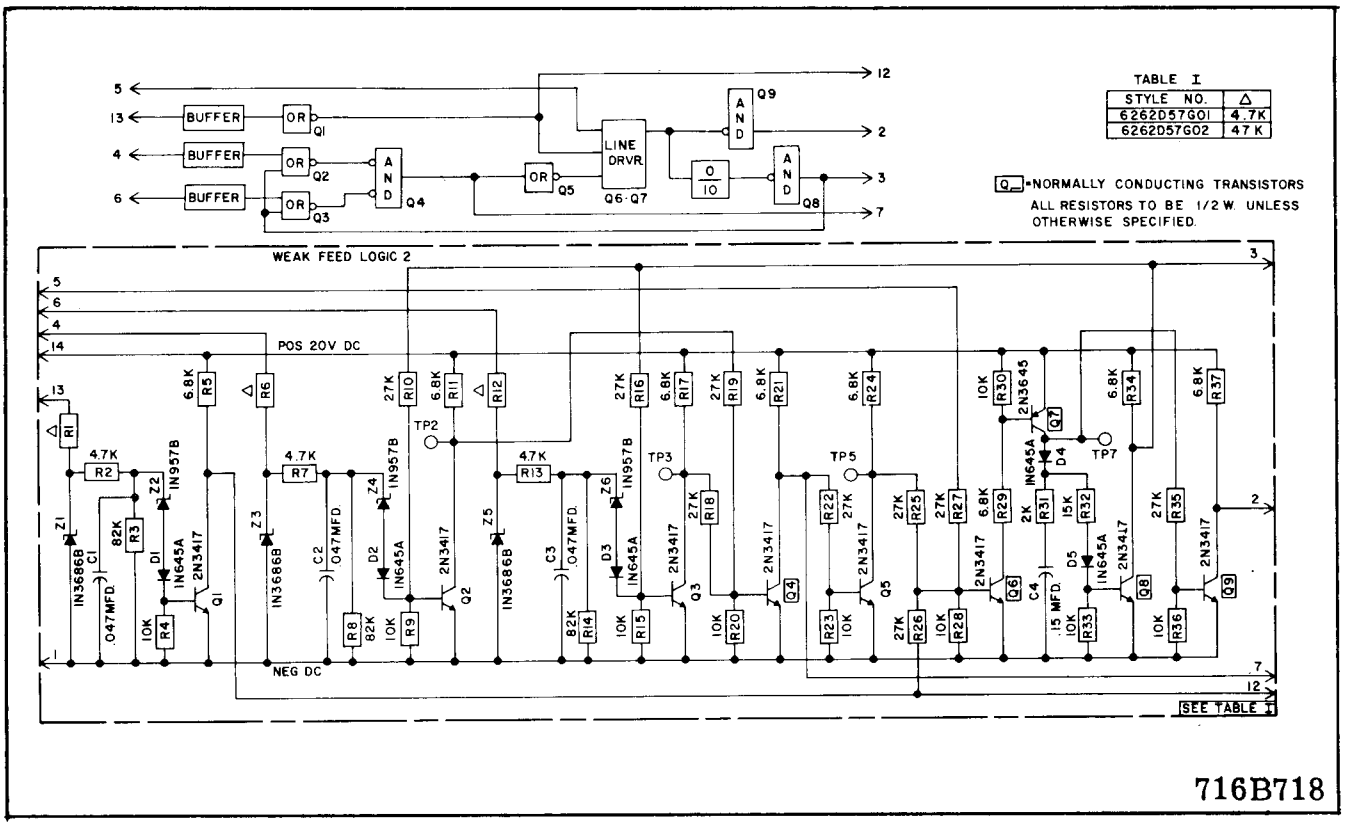


Fig. 14 Internal Schematic – Weak Feed Logic 2 Board

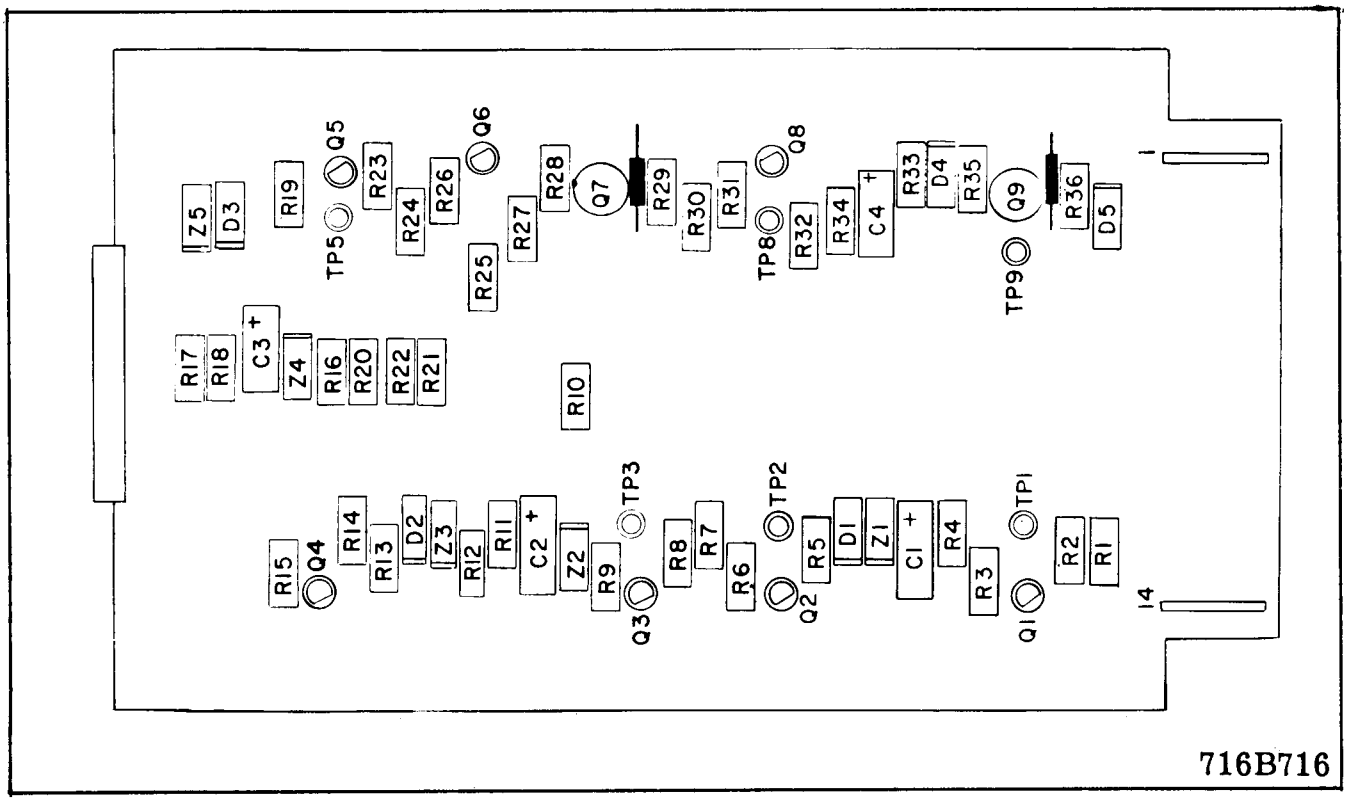


Fig. 15 Component Location – Weak Feed Logic 3 Board

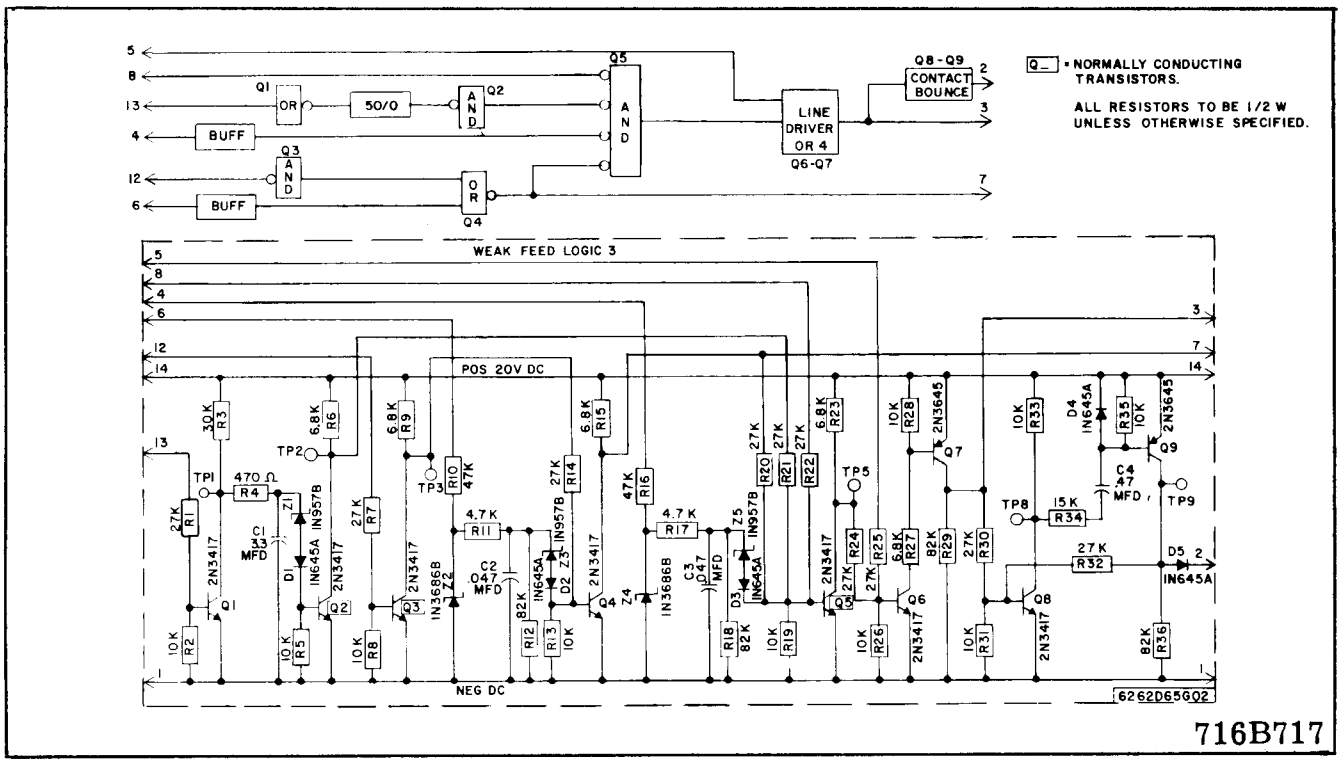


Fig. 16 Internal Schematic – Weak Feed Logic 3 Board for Elec. Mech. Systems

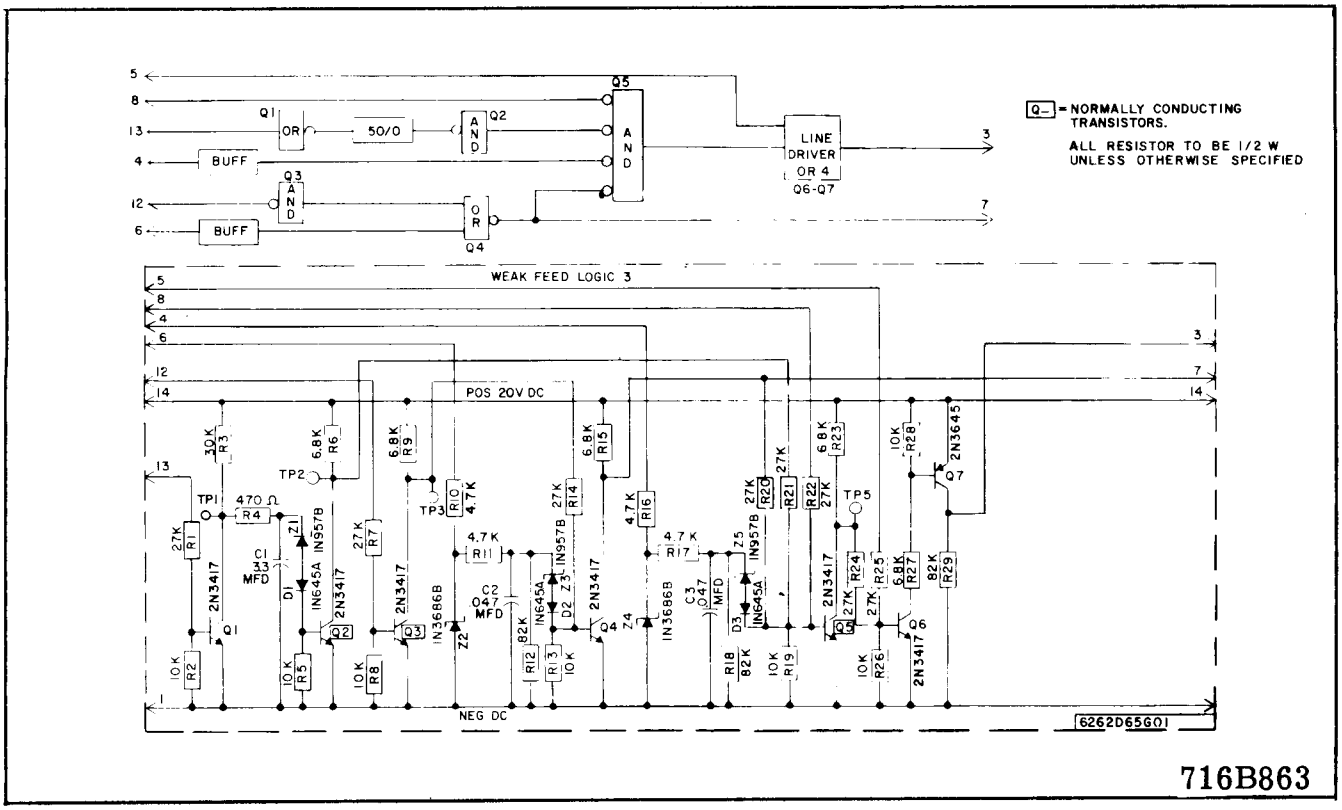


Fig. 17 Internal Schematic – Weak Feed Logic 3 Board for Solid State Systems

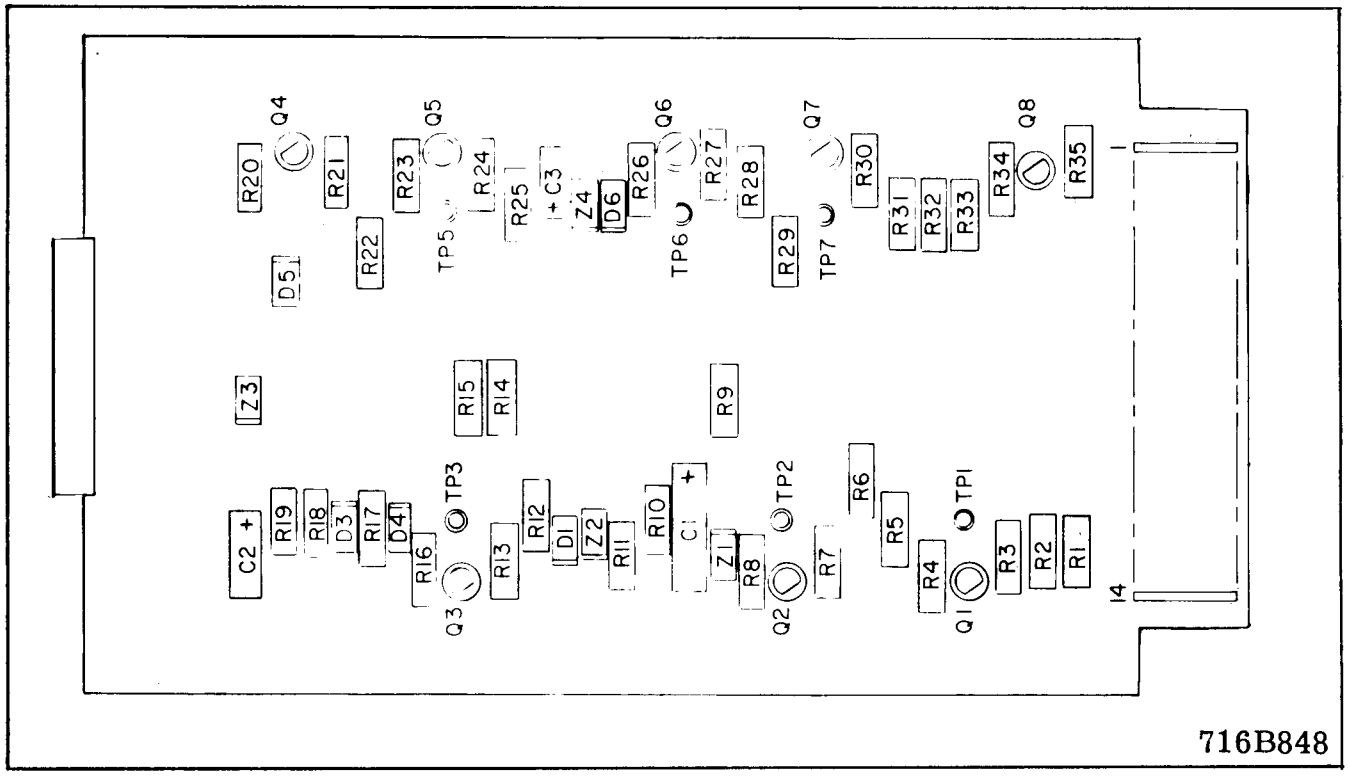


Fig. 18 Component Location – Weak Feed Logic 4 Board

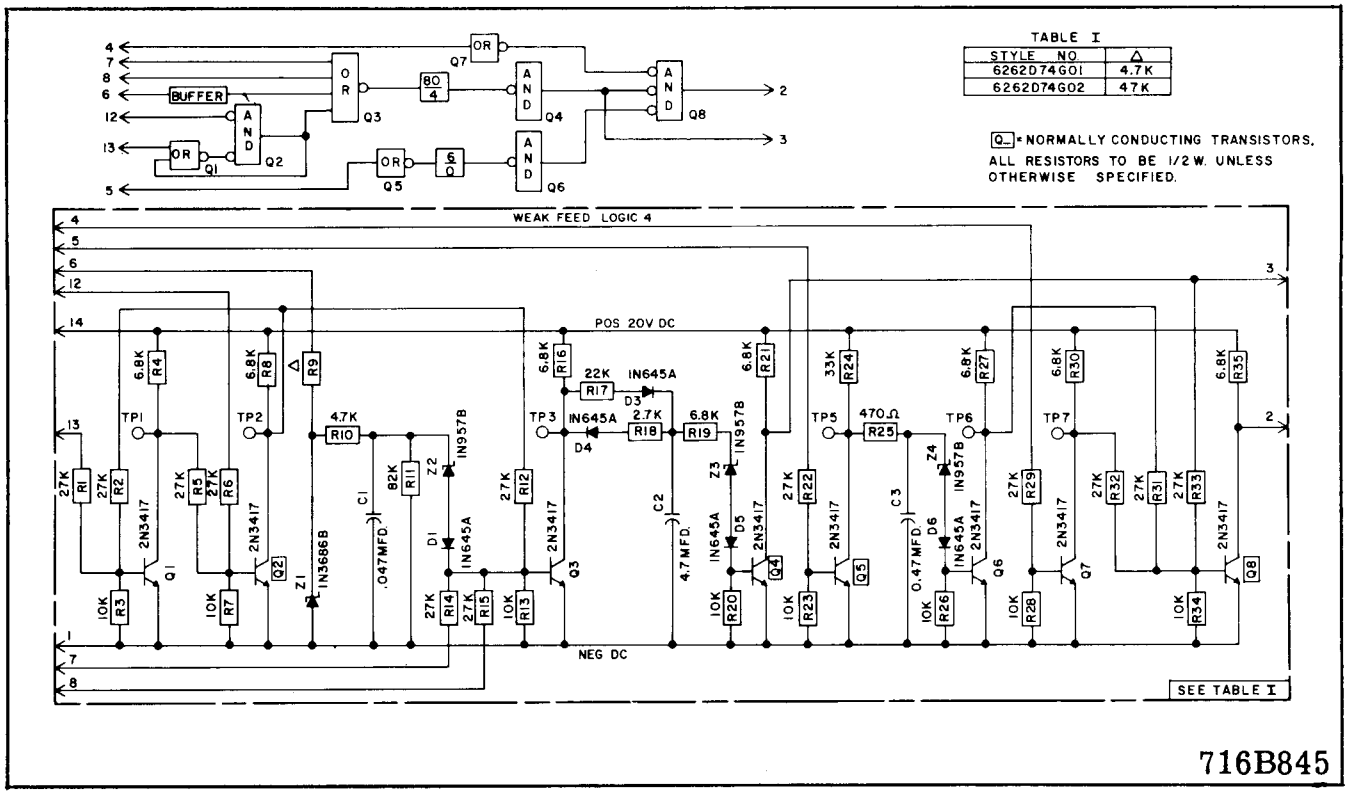


Fig. 19 Internal Schematic – Weak Feed Logic 4 Board

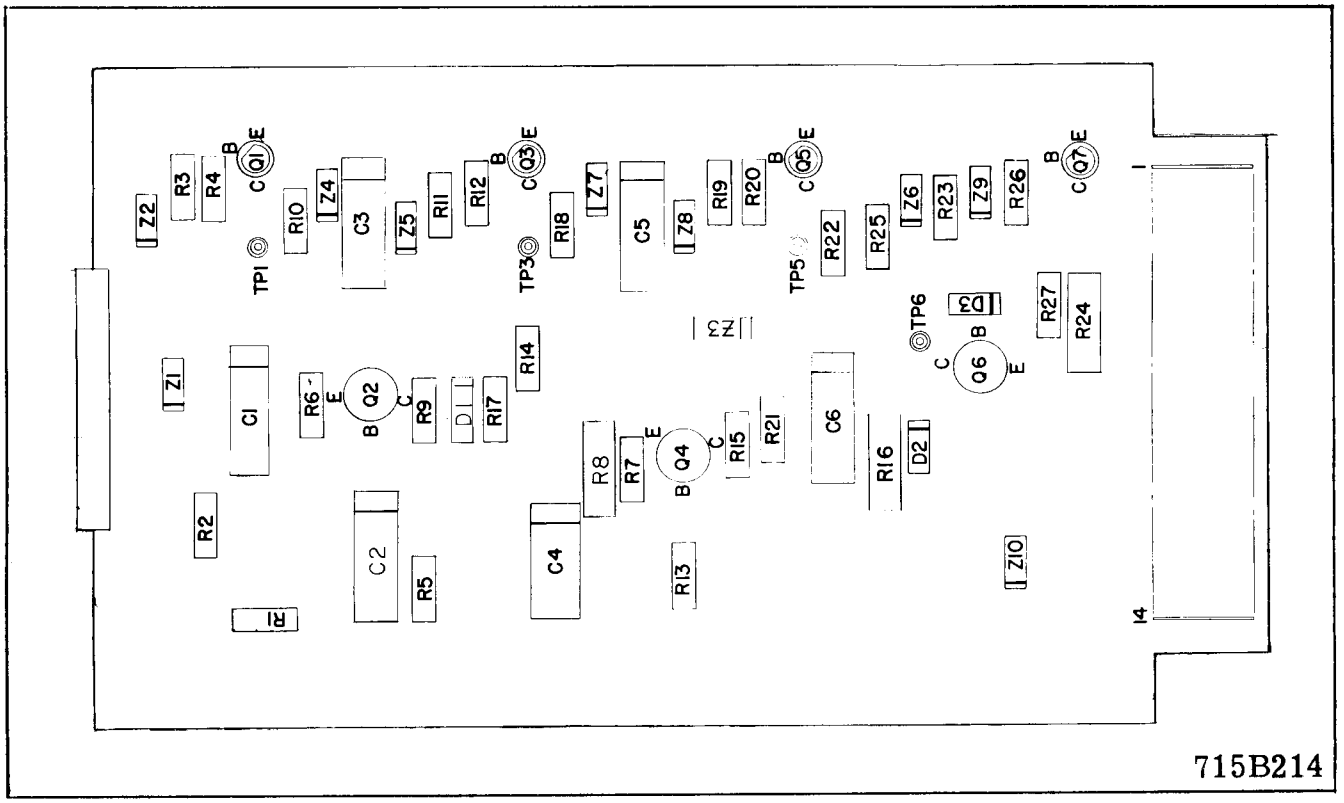


Fig. 20 Component Location Channel Interface Board

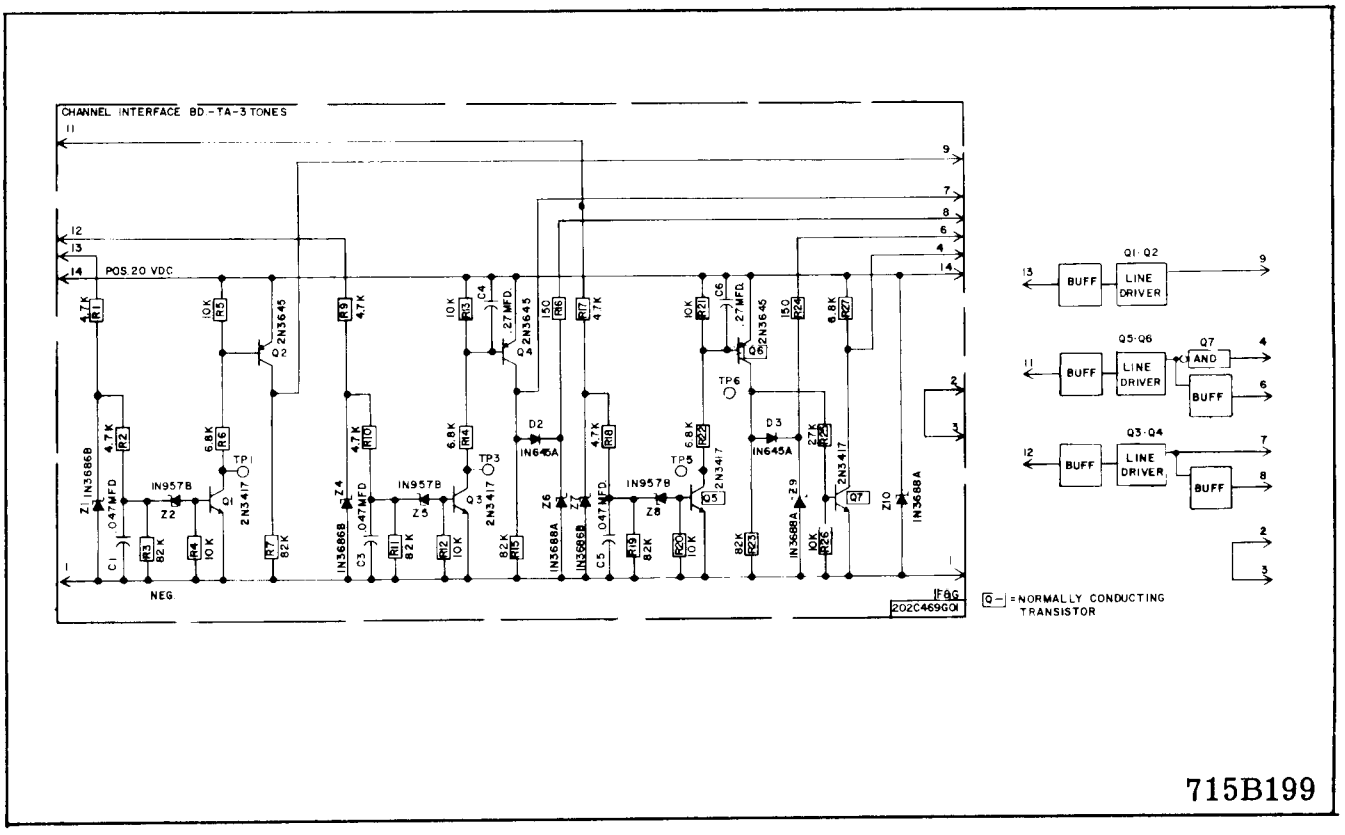


Fig. 21 Internal Schematic Channel Interface Board for TA-3 Tone

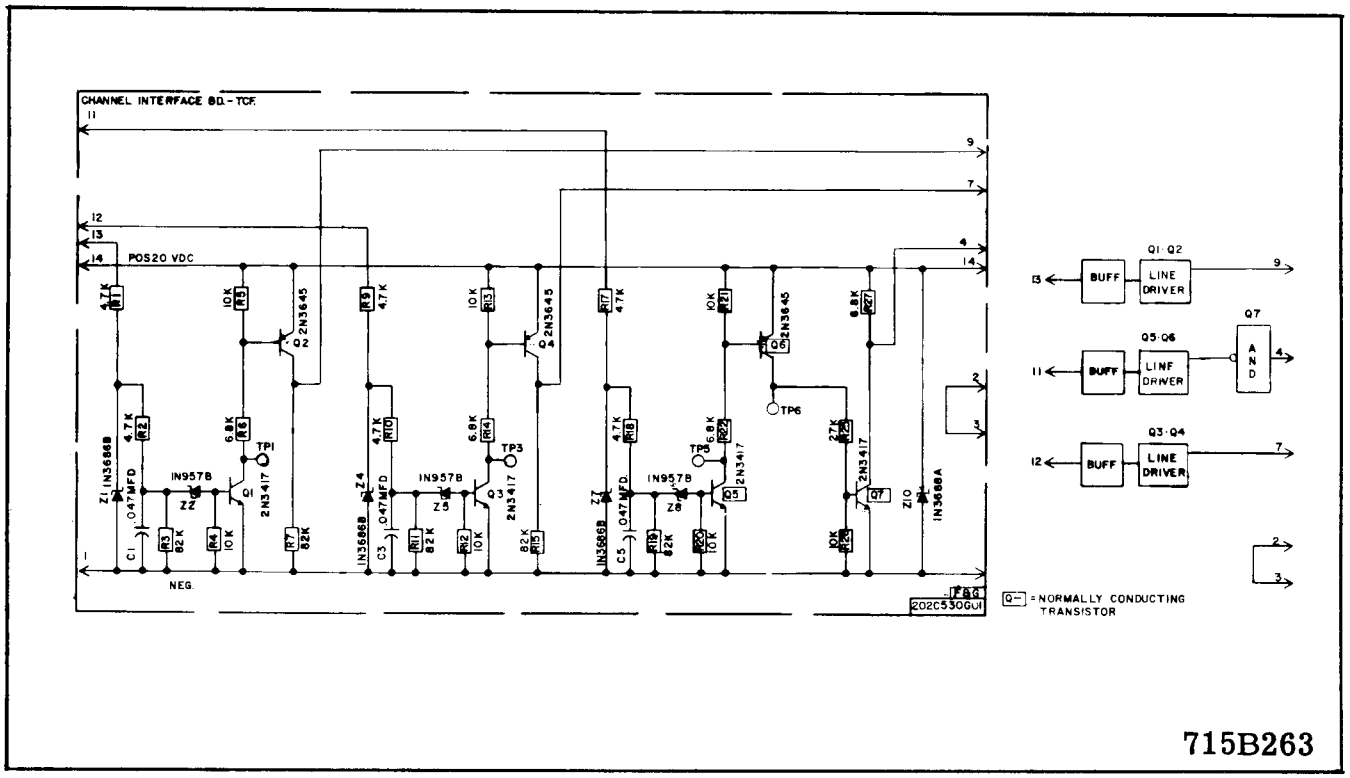


Fig. 22 Internal Schematic Channel Interface Board for TCF Carrier

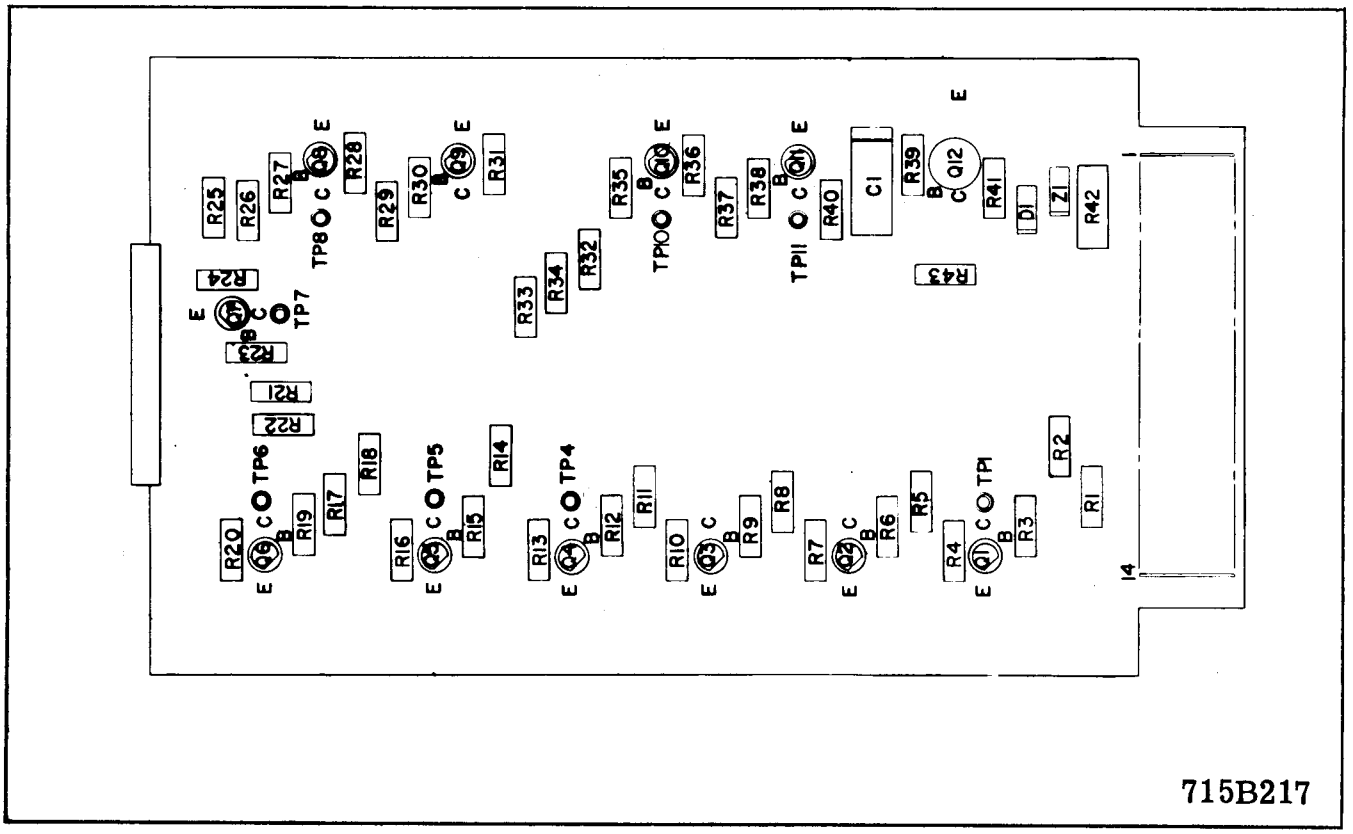


Fig. 23 Component Location Channel Trip Board

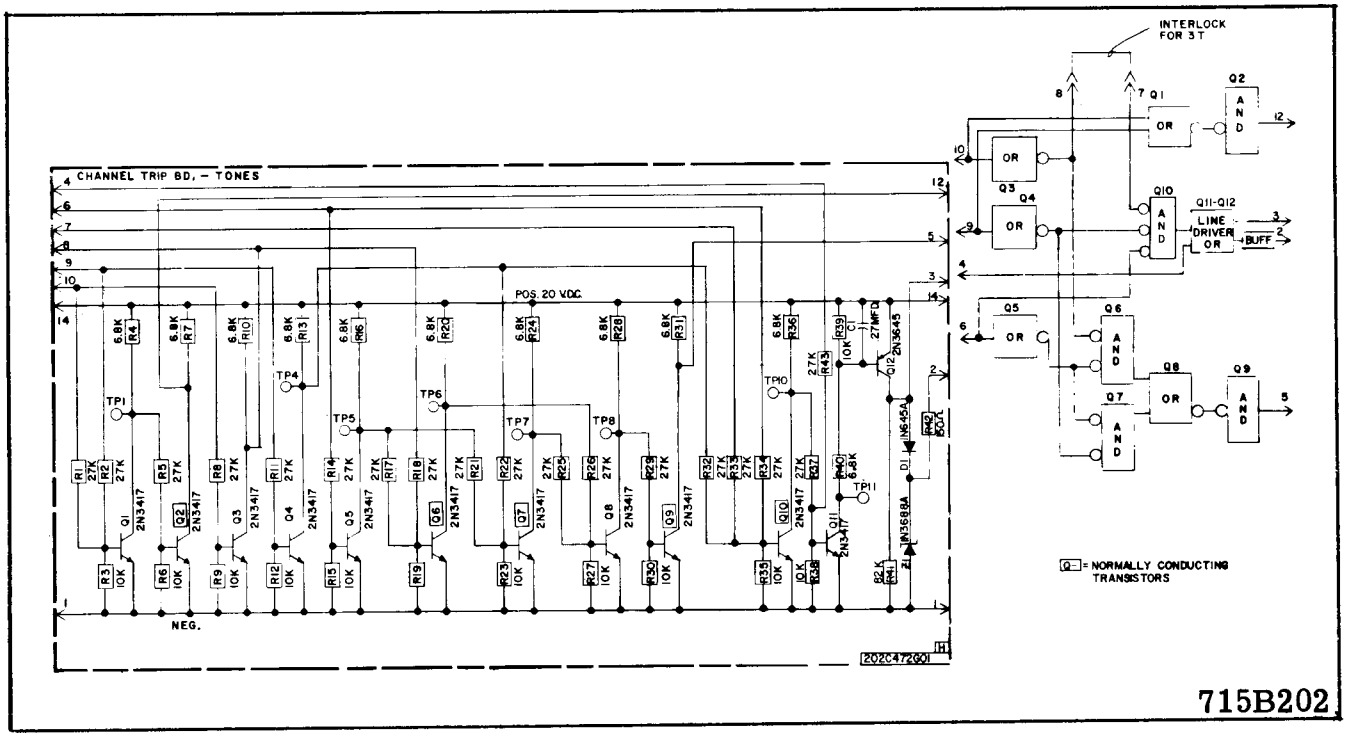


Fig. 24 Internal Schematic Channel Trip Board for Tones

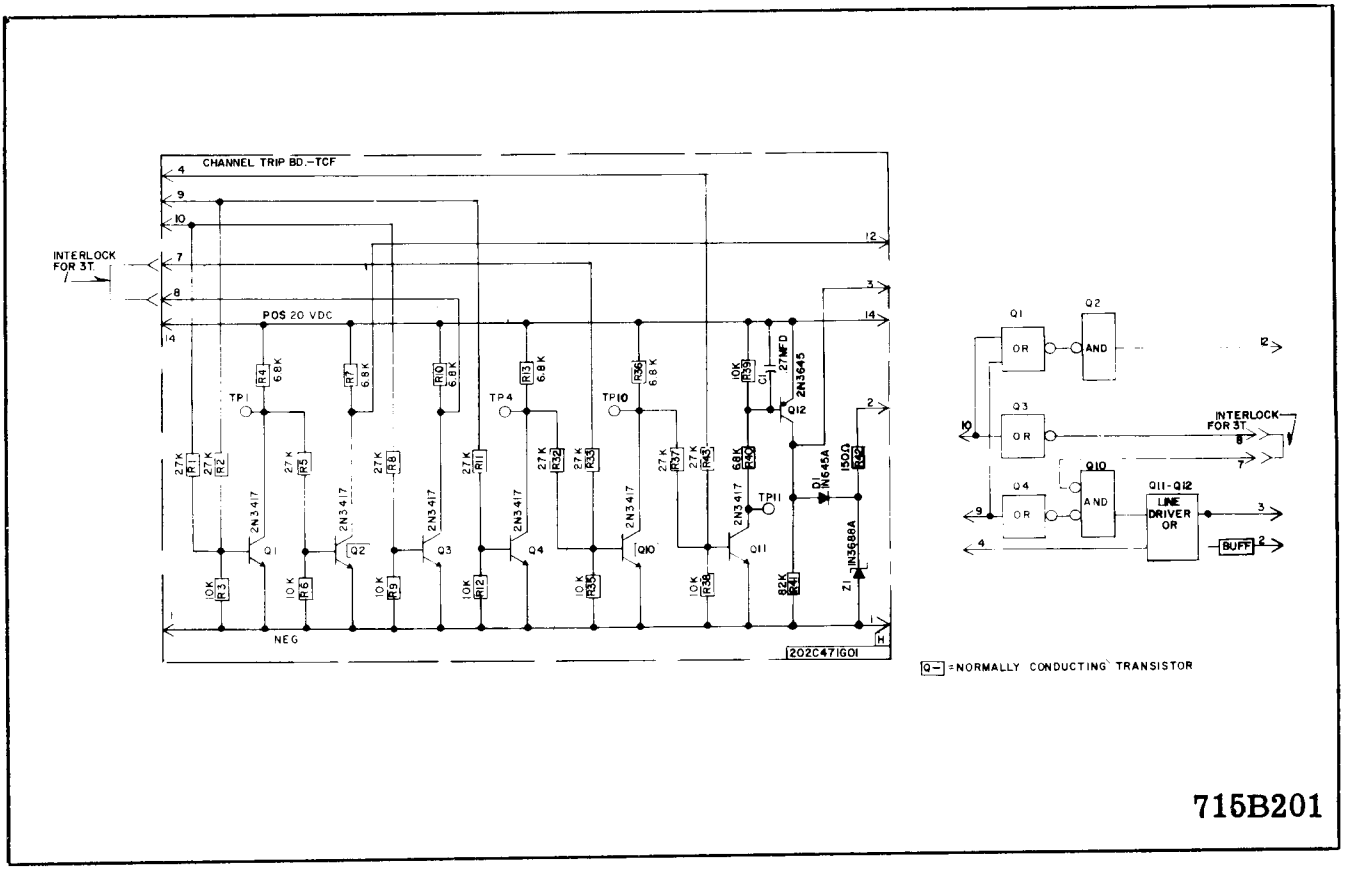


Fig. 25 Internal Schematic Channel Trip Board for TCF

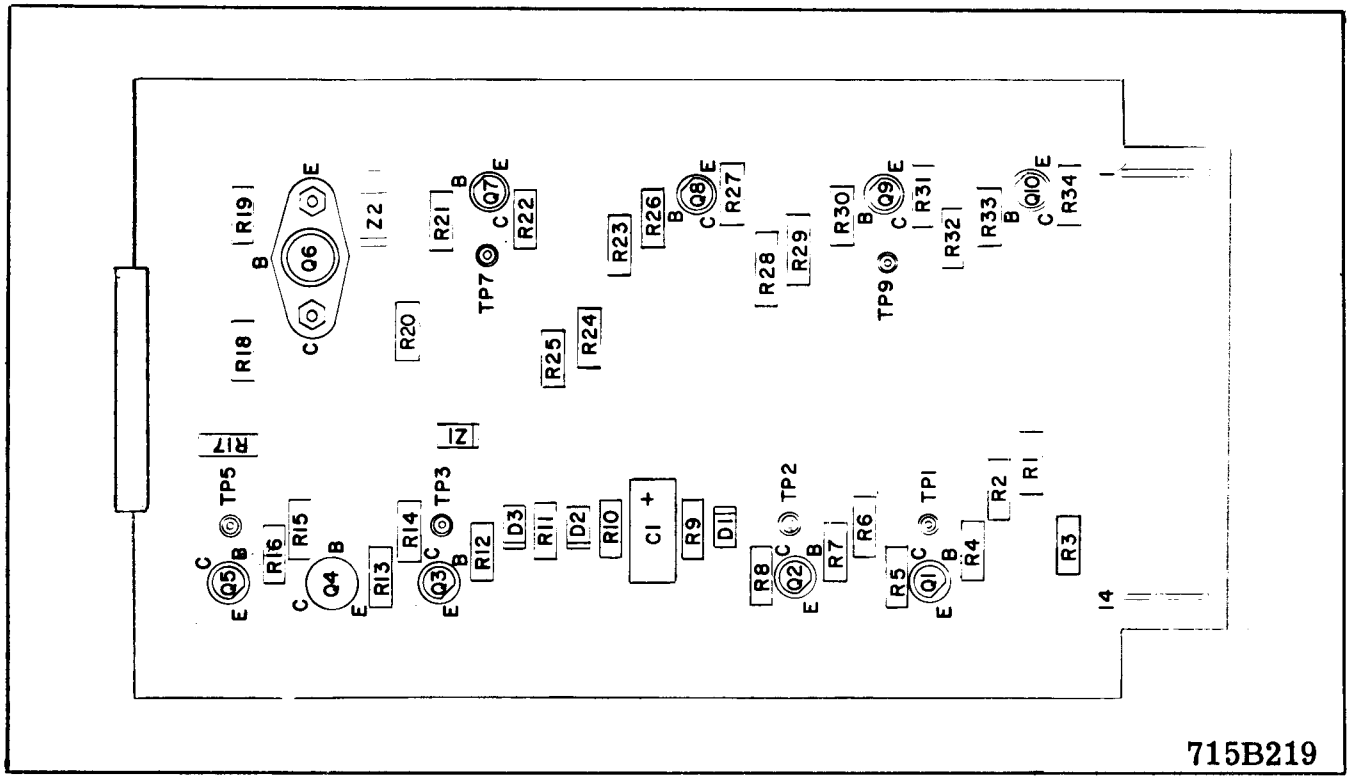


Fig. 26 Component Location Channel Supervision Board Tone Channel

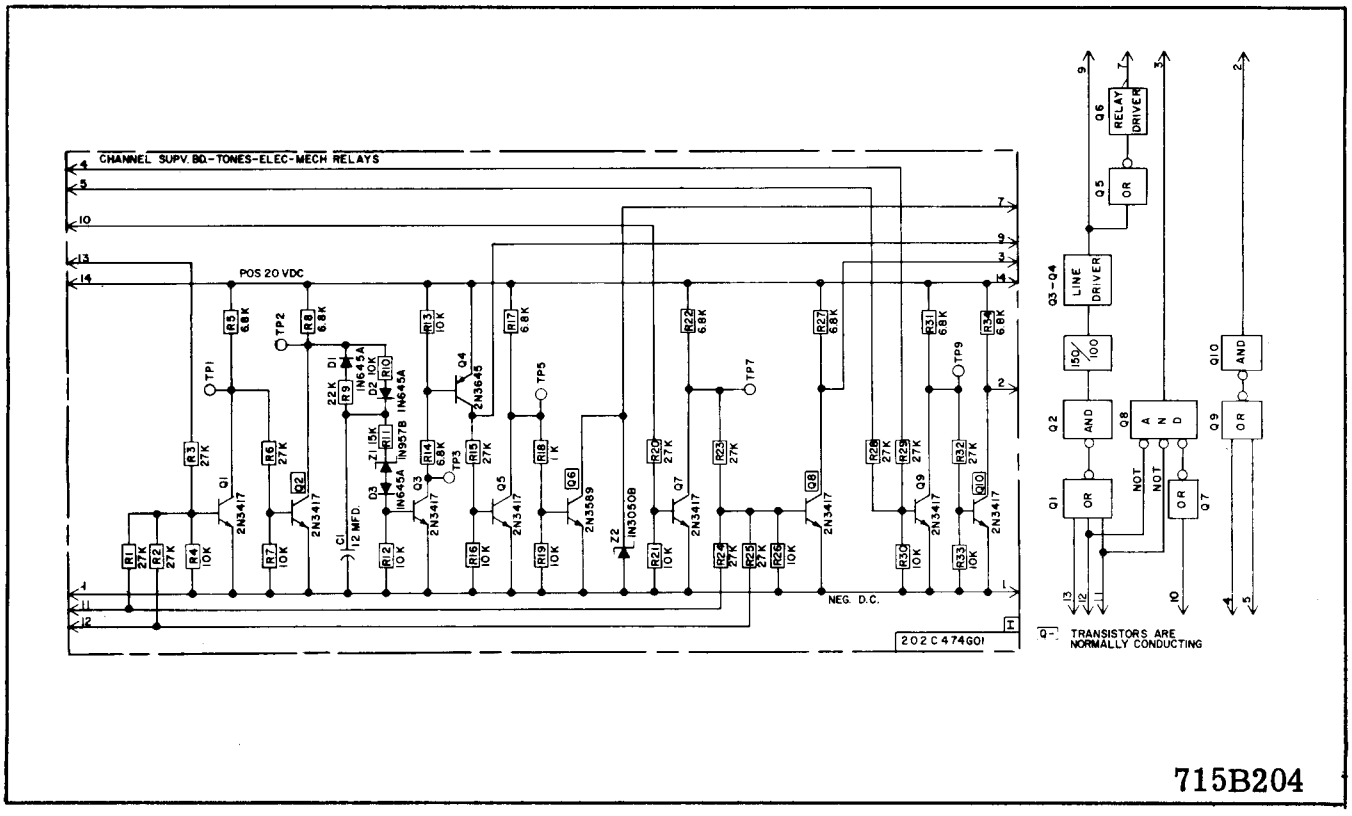


Fig. 27 Internal Schematic Channel Supervision Board for Tone Channel and Elec. Mech. System

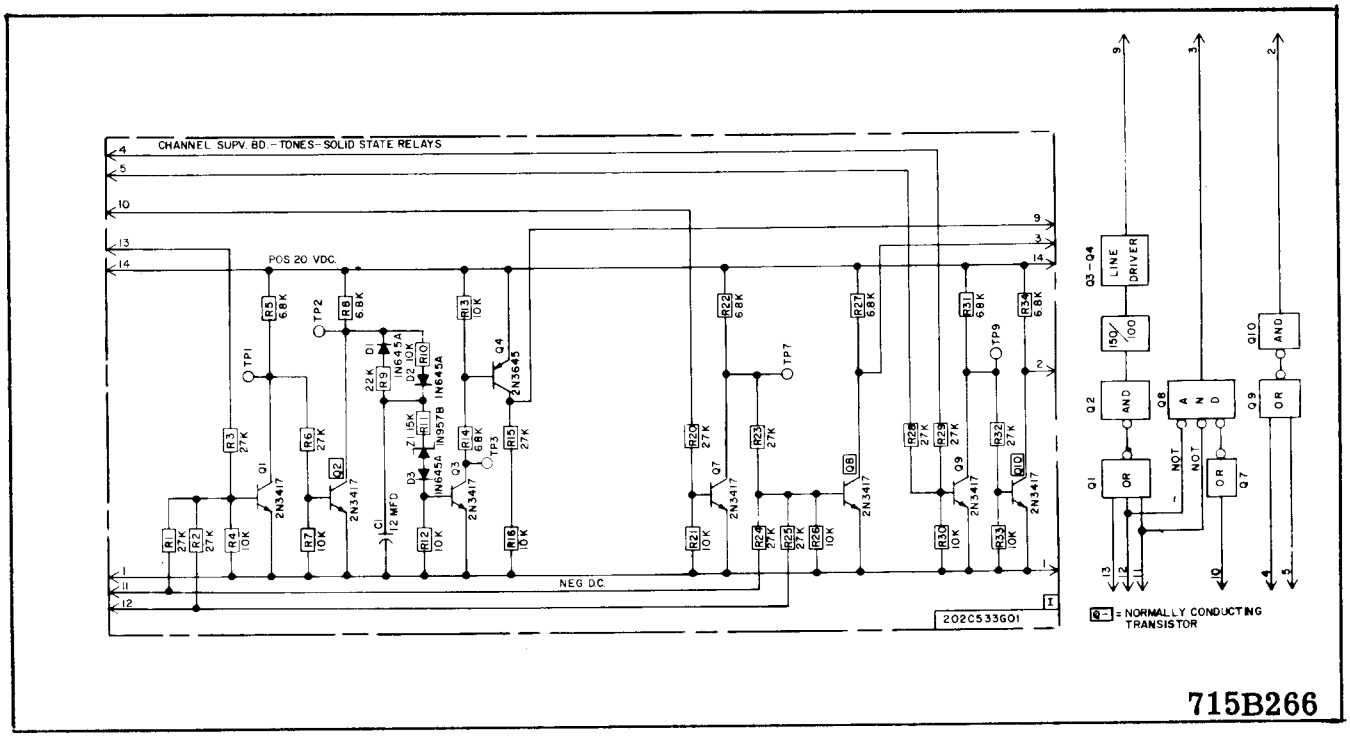


Fig. 28 Internal Schematic Channel Supervision Board for Tone Channel and Solid State System

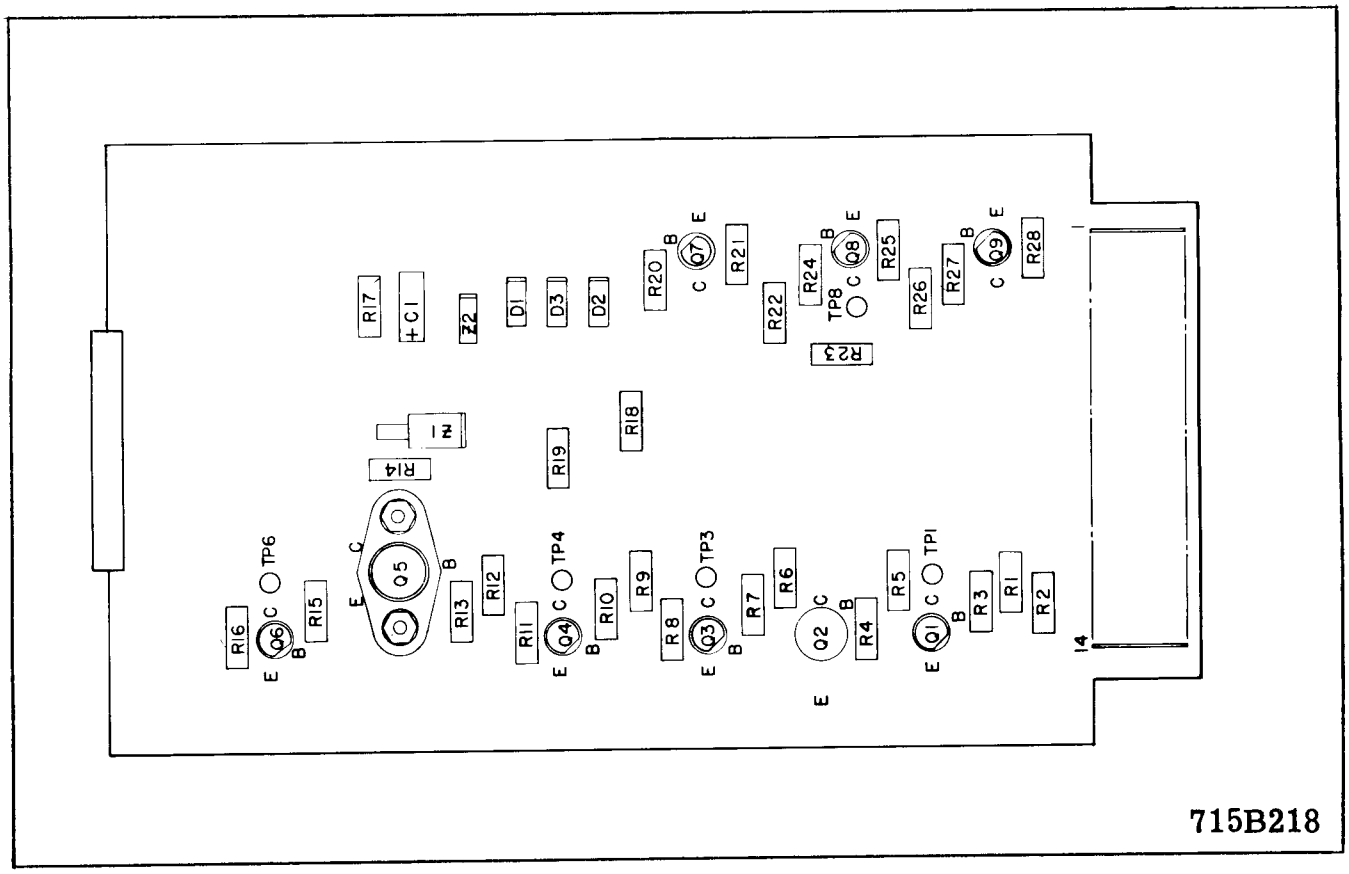


Fig. 29 Component Location Channel Supervision Board TCF Channel

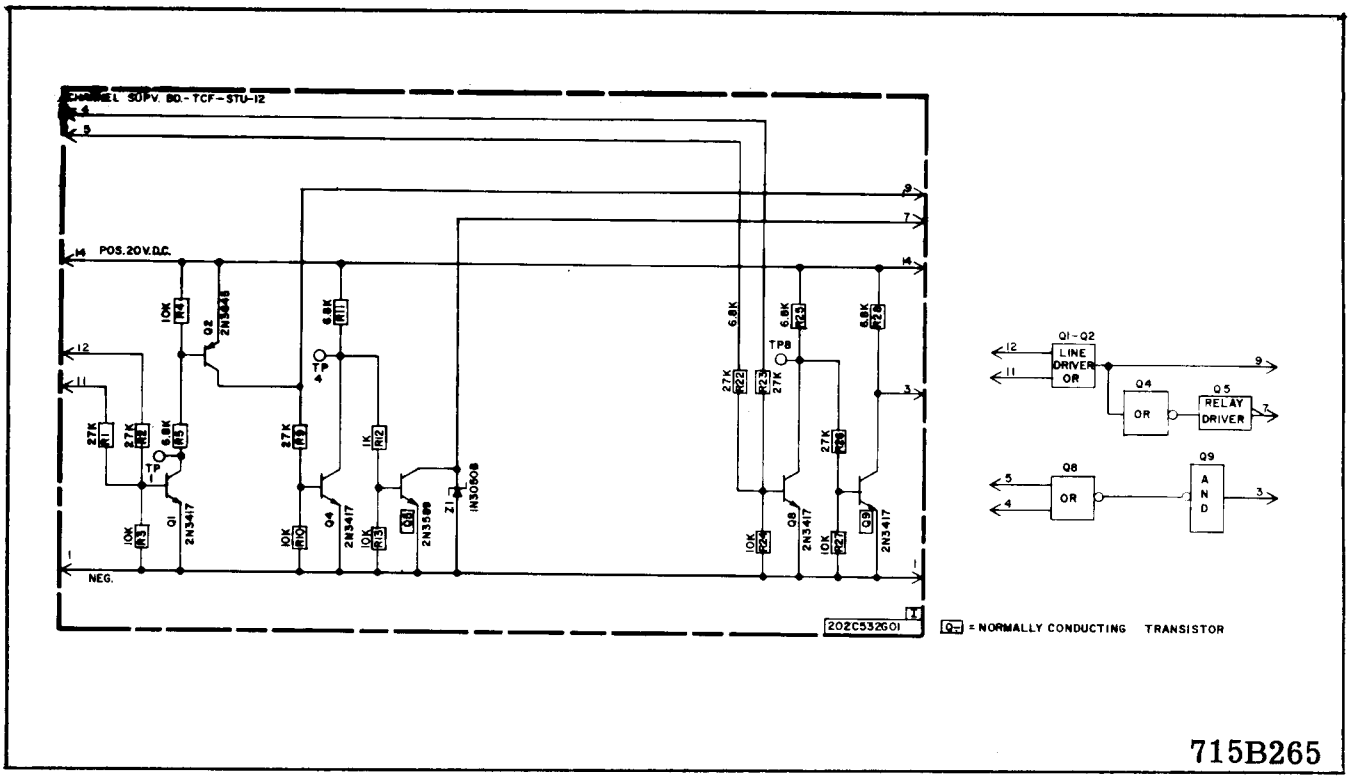


Fig. 30 Internal Schematic Channel Supervision Board for TCF Channel

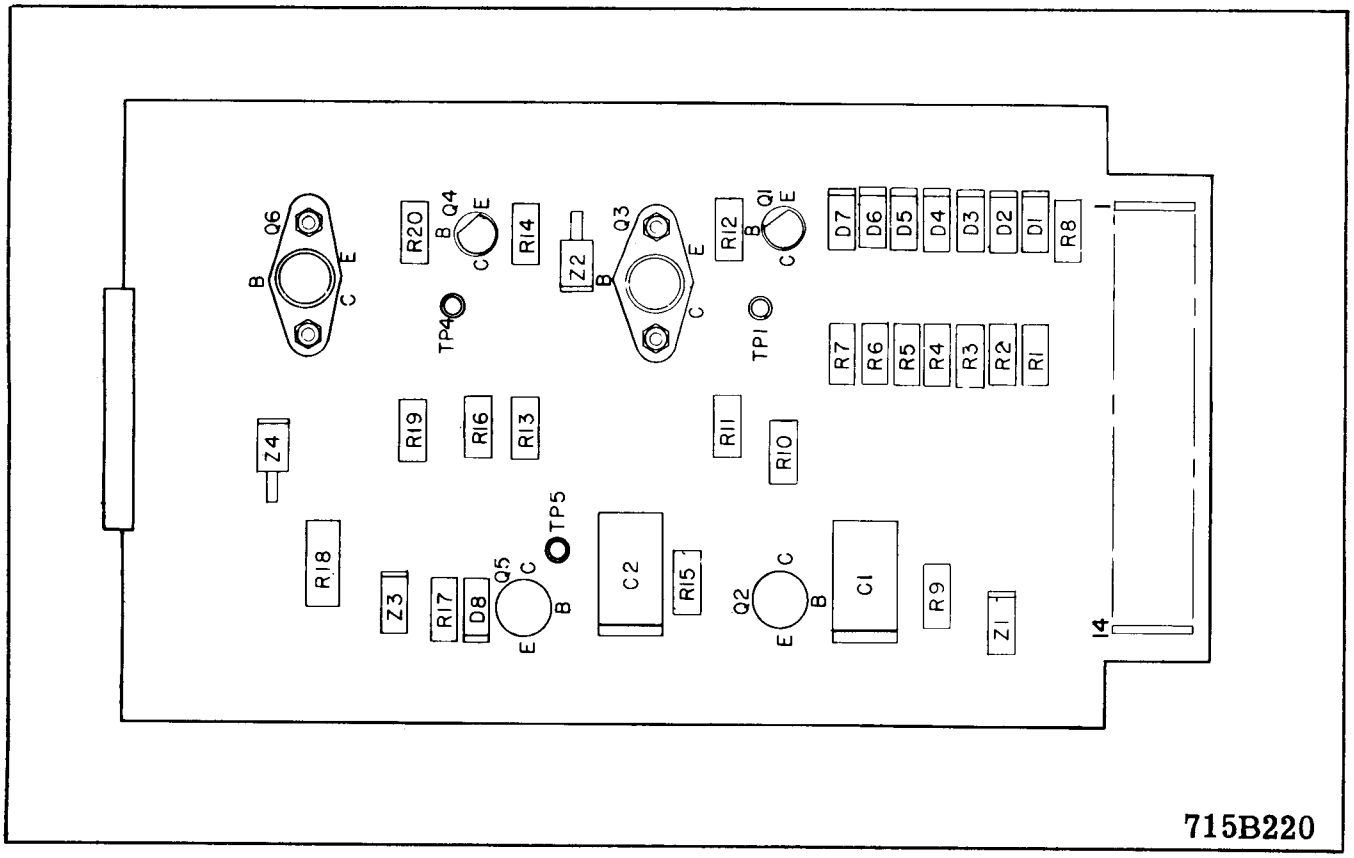


Fig. 31 Component Location Transmitter Key Board

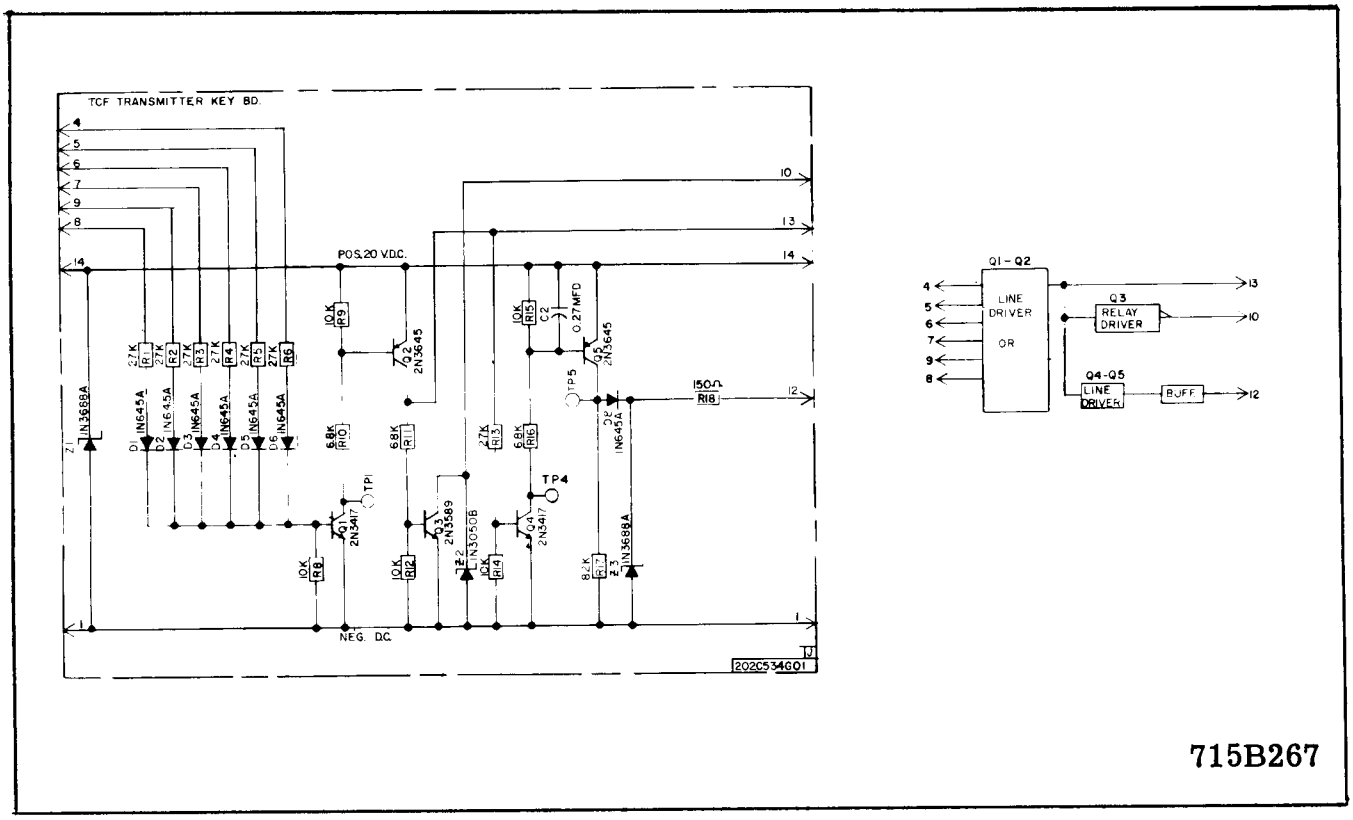


Fig. 32 Internal Schematic Transmitter Key Board for TCF Channel

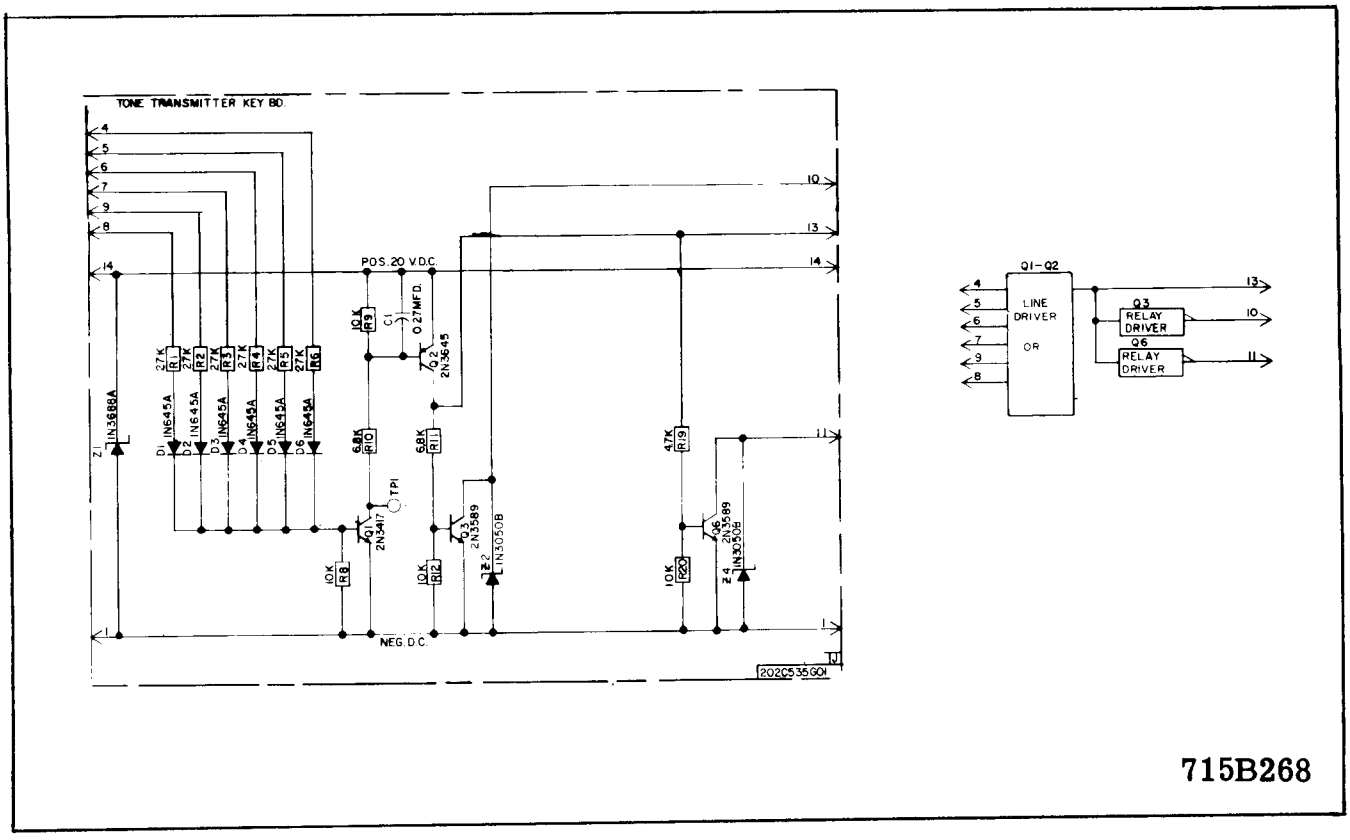


Fig. 33 Internal Schematic Transmitter Key Board for a Tone Channel

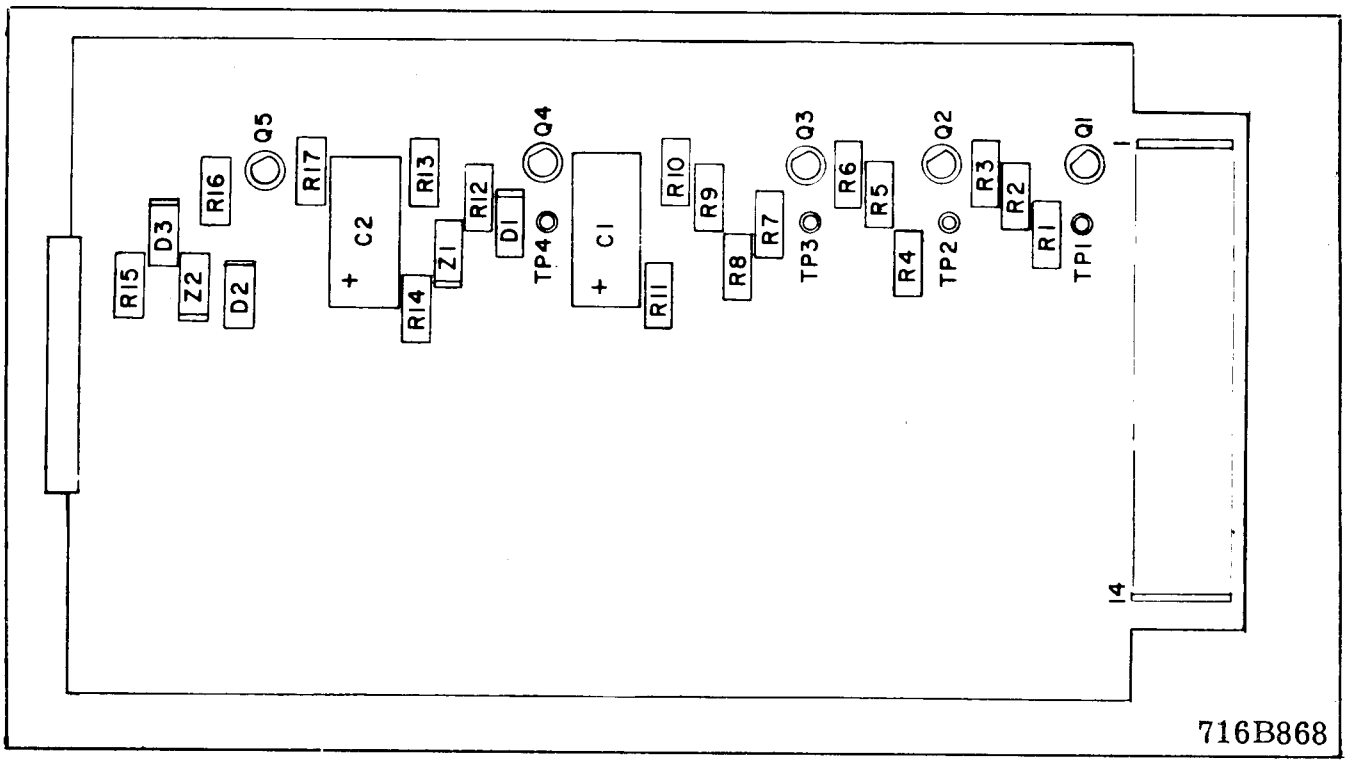


Fig. 34 Component Location Checkback Board

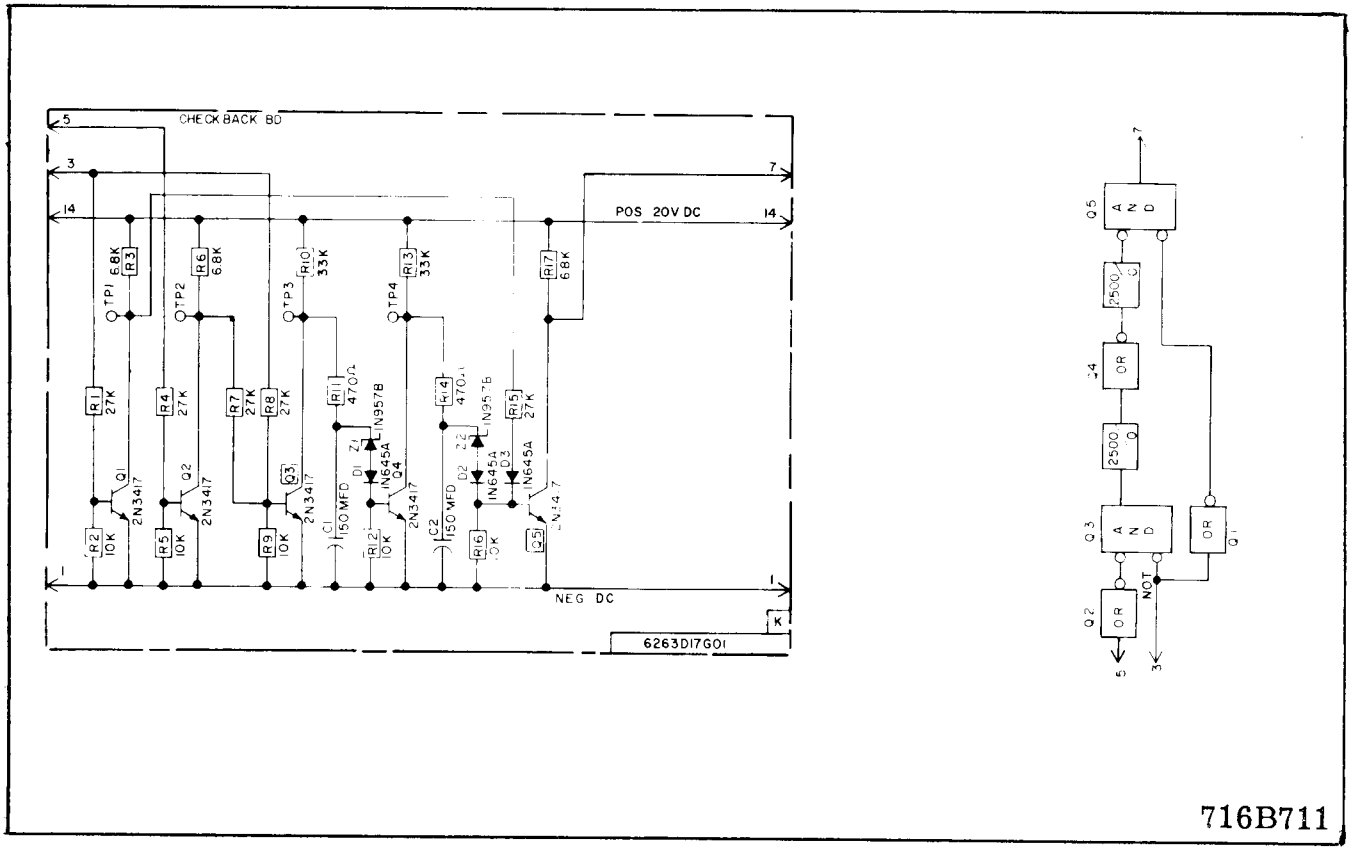


Fig. 35 Internal Schematic Checkback Board

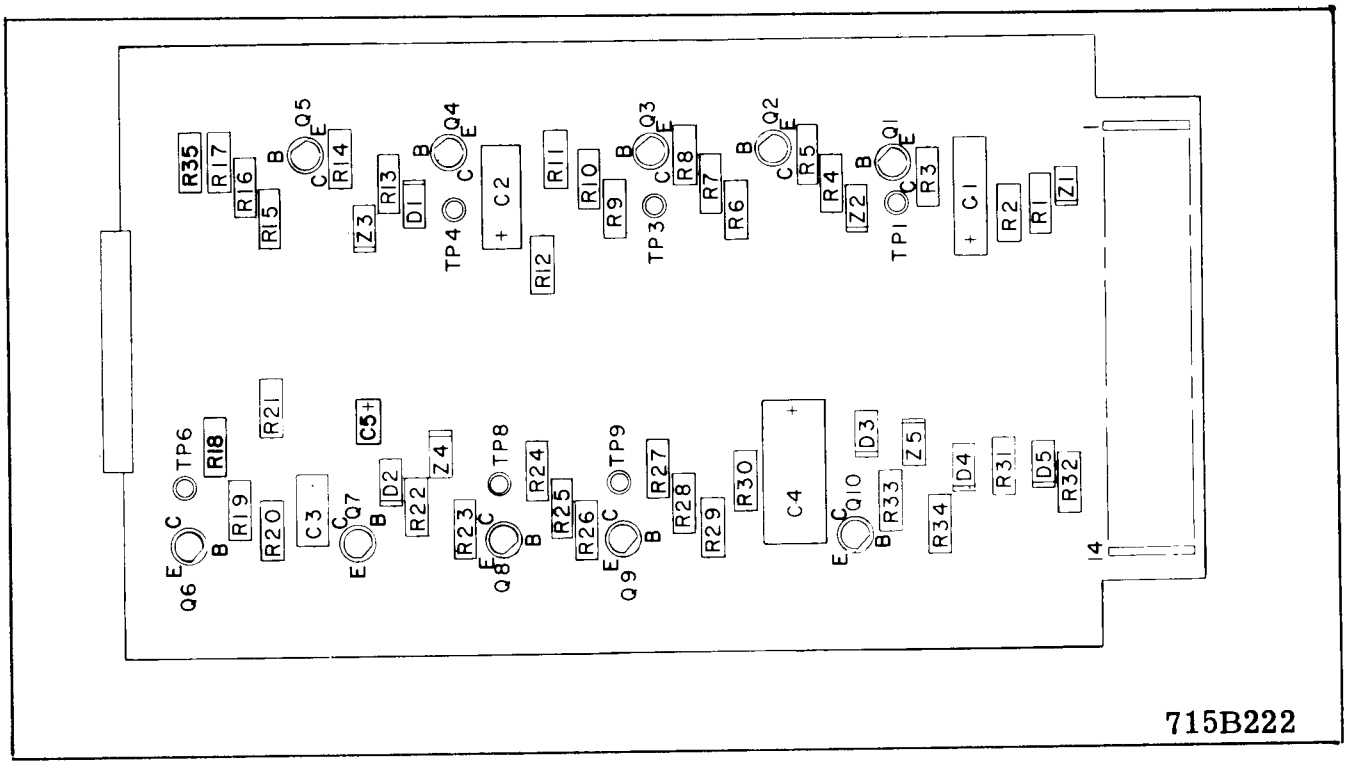


Fig. 36 Component Location Timing Board

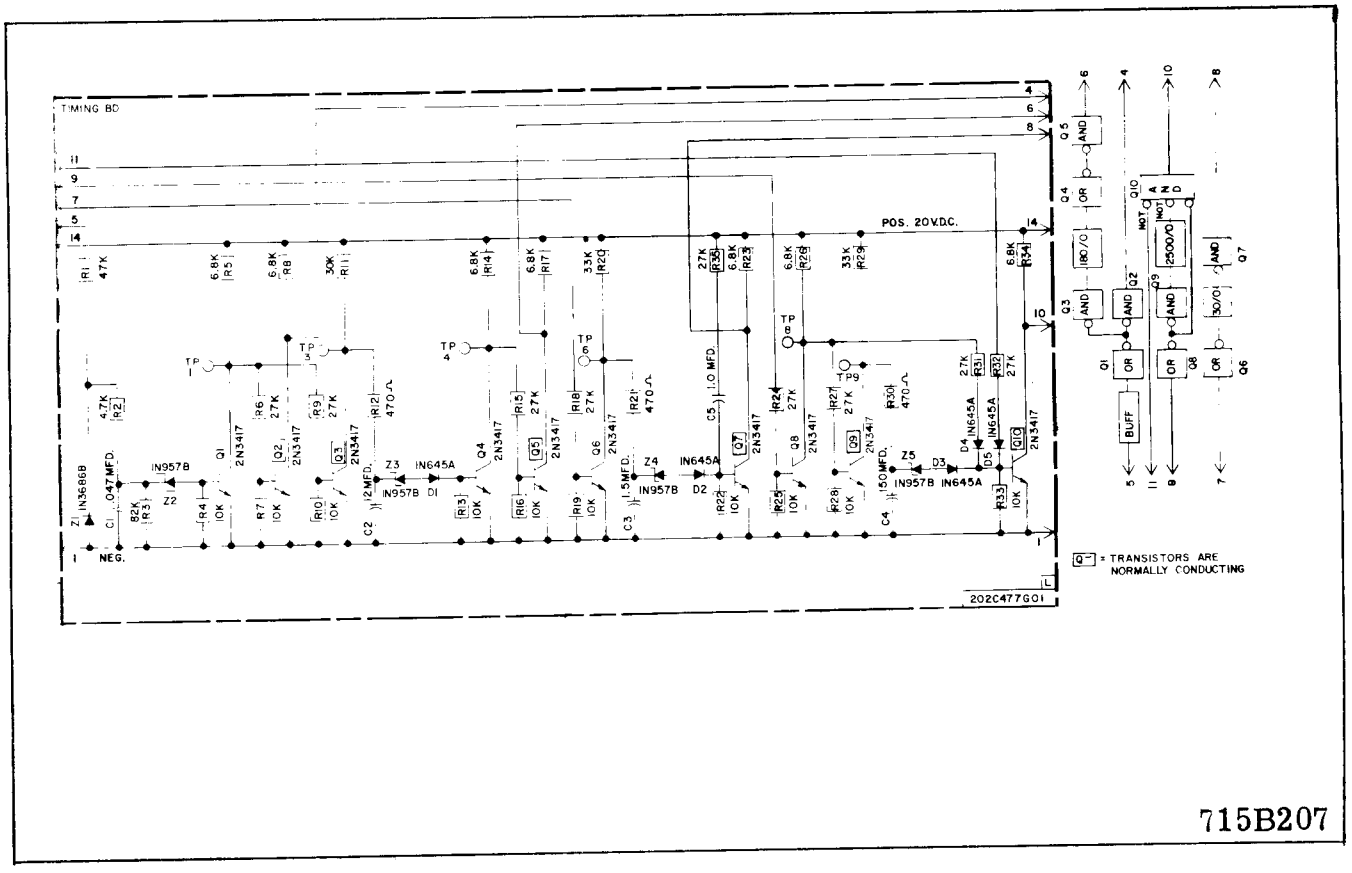


Fig. 37 Internal Schematic Timing Board

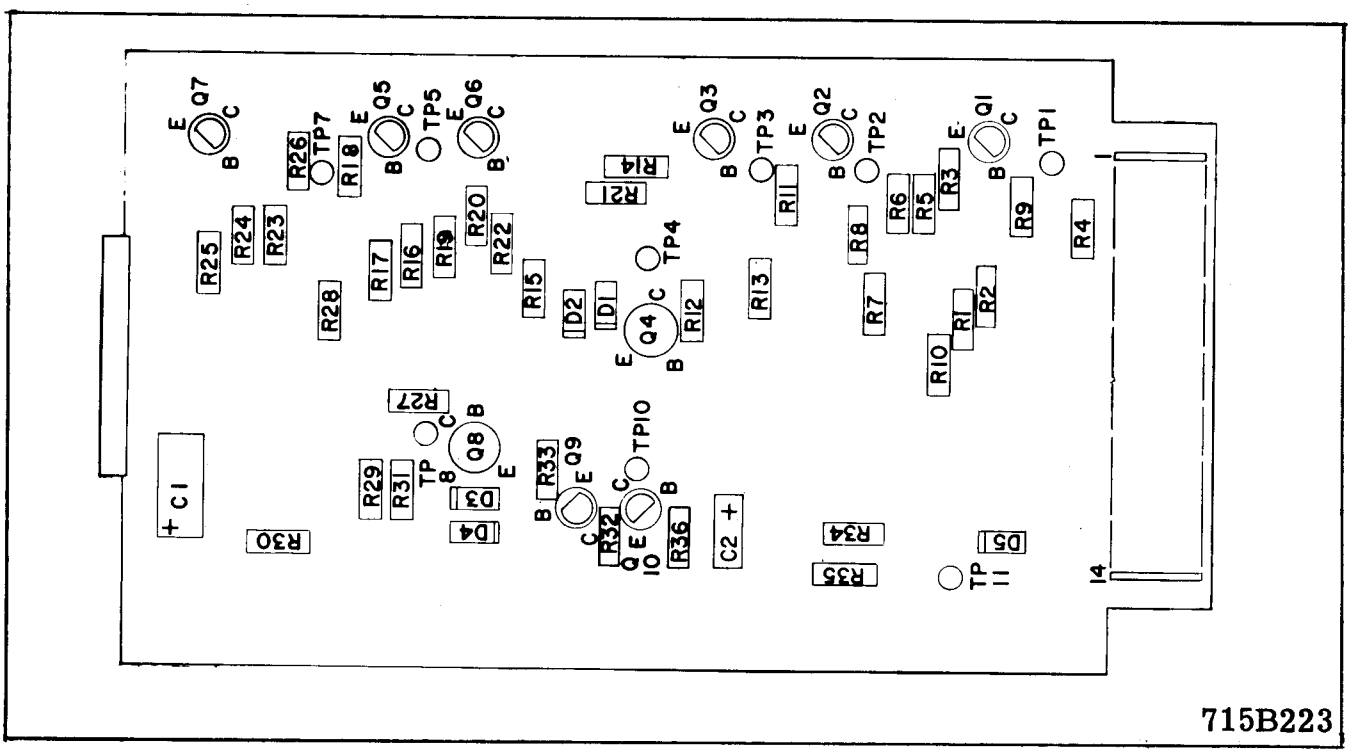


Fig. 38 Component Location Arming Board

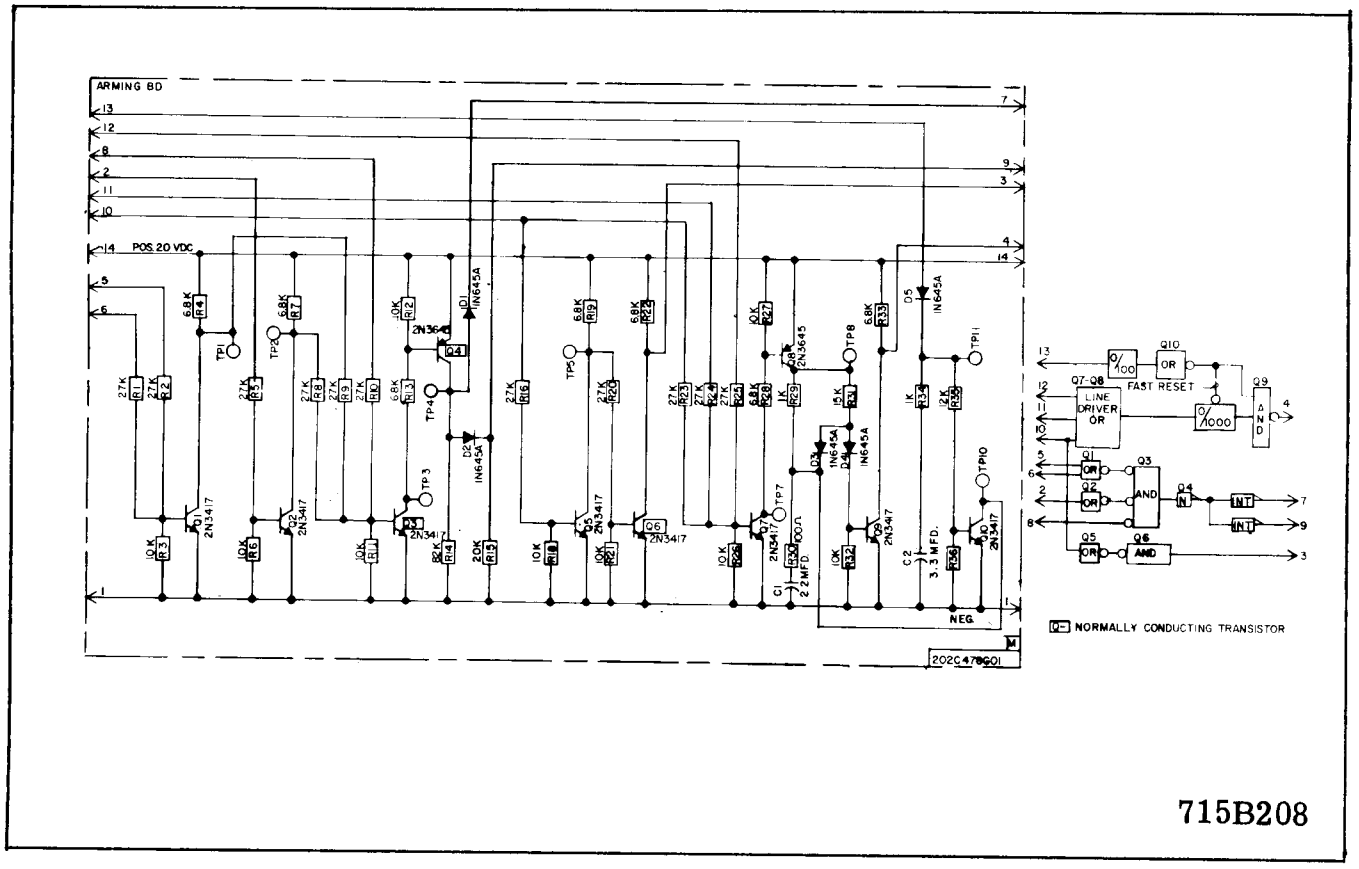
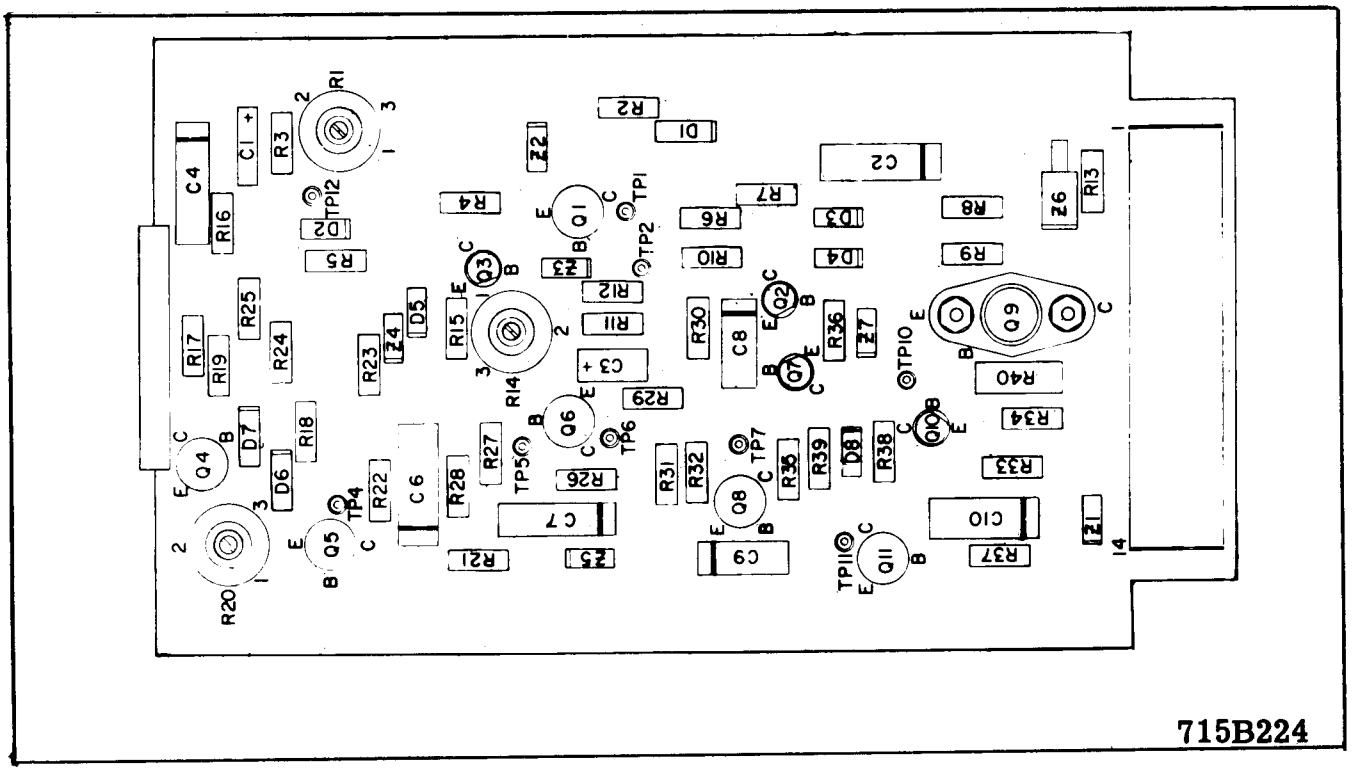
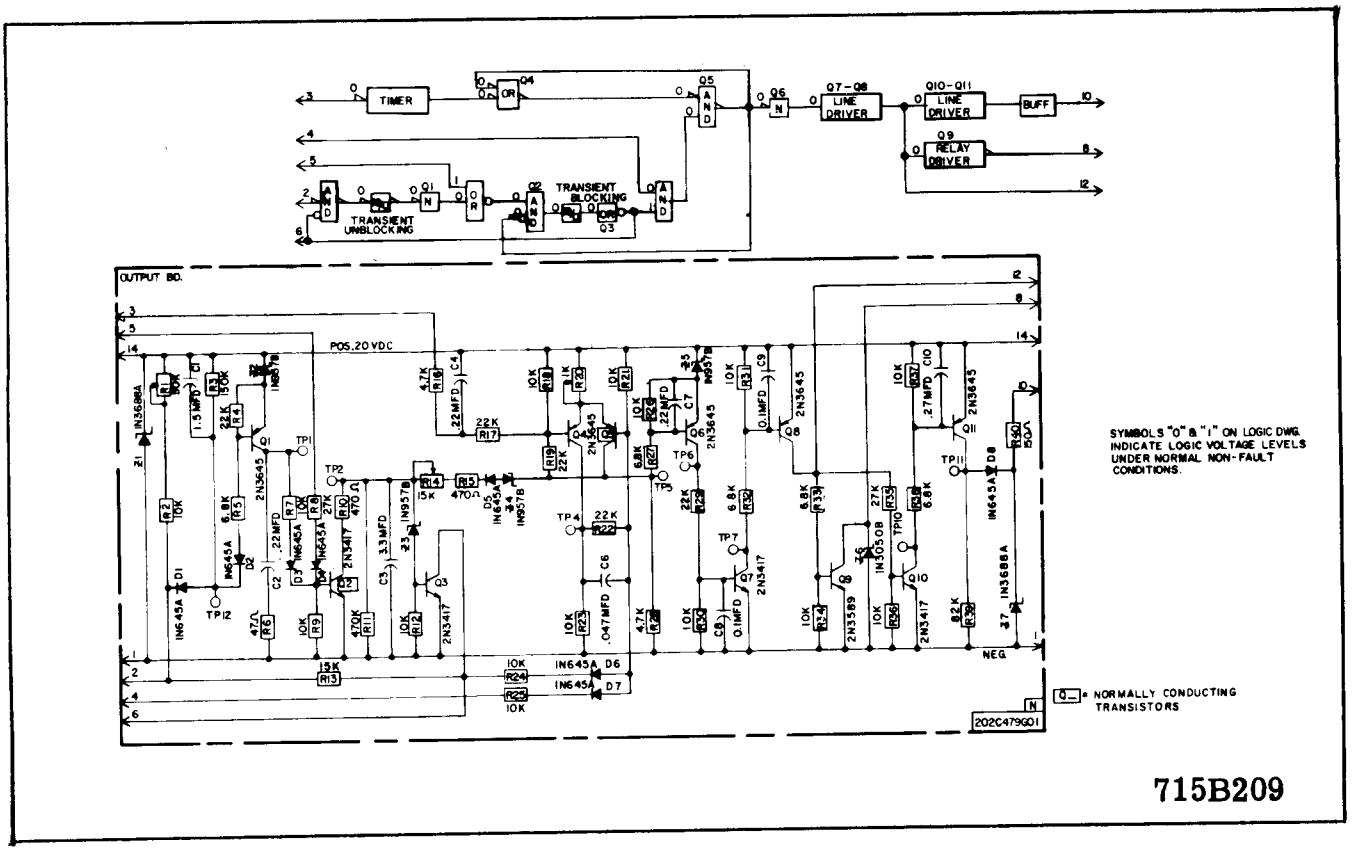
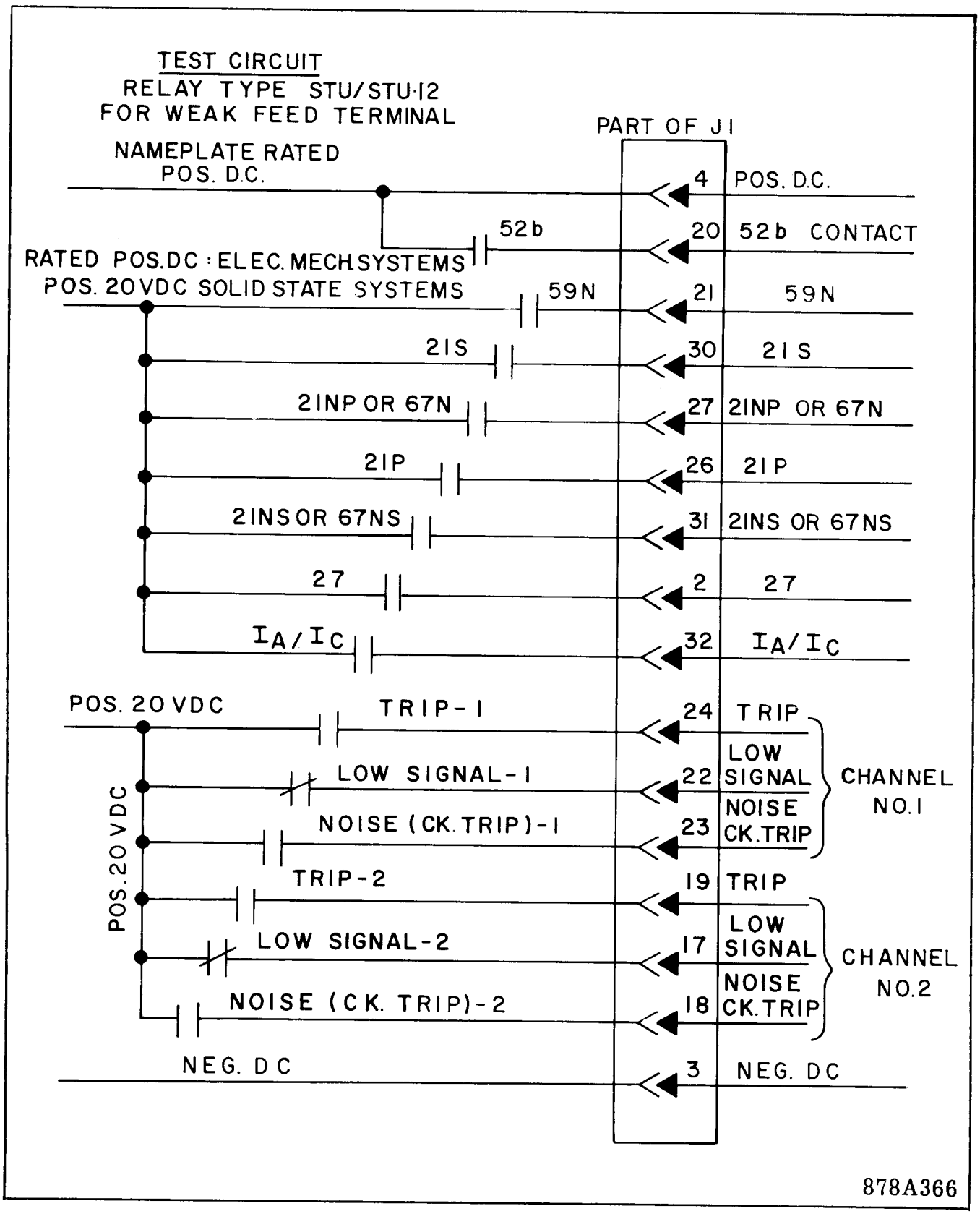
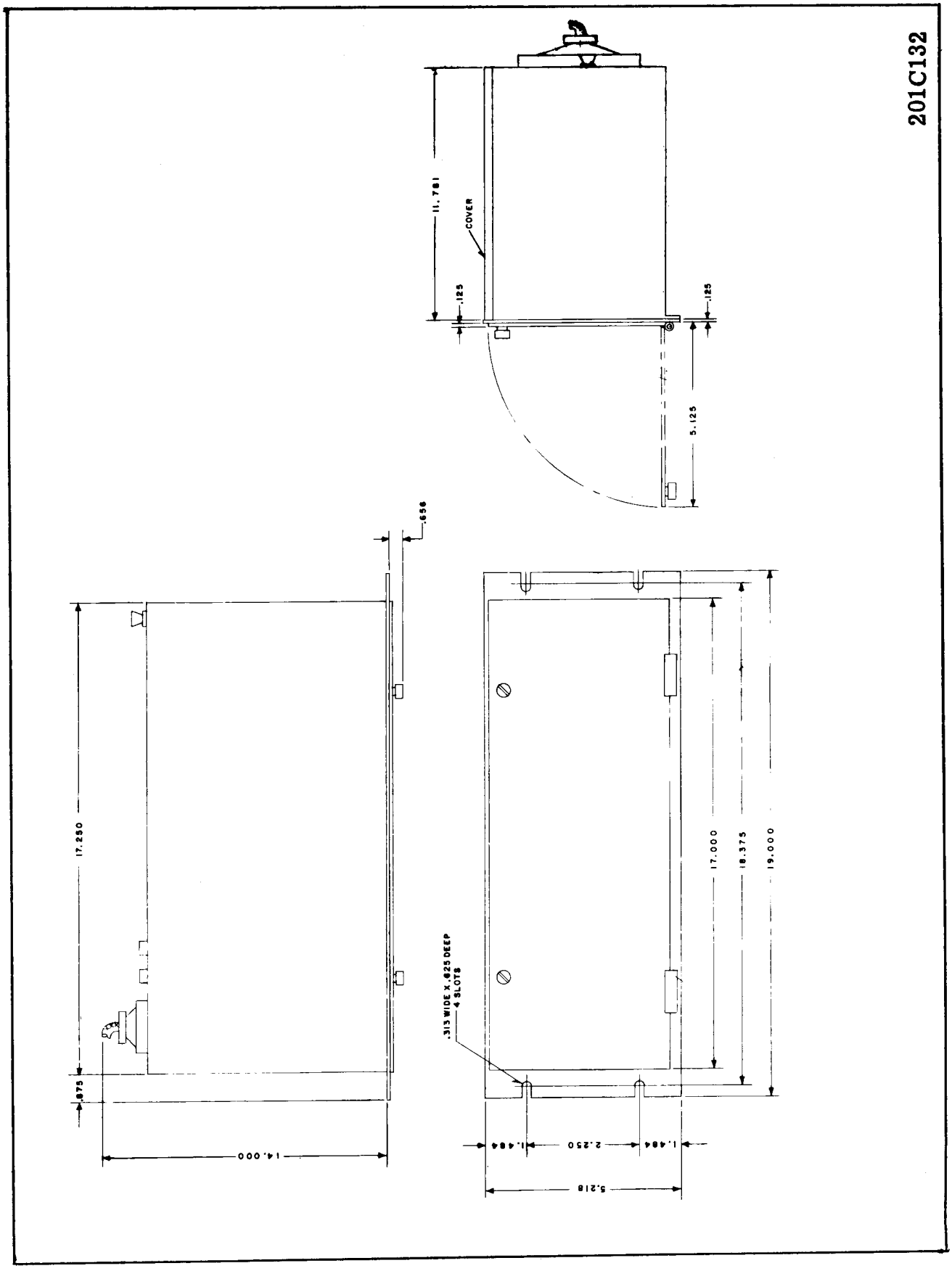


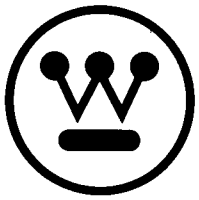
Fig. 39 Internal Schematic Arming Board


715B224


TIMER
TRANSIENT UNBLOCKING
TRANSIENT BLOCKING
LINE DRIVER
LINE DRIVER
BUFF
RELAY DRIVER
OUTPUT BD.
POS. 20 VDC
NEG
SYMBOLS "0" & "1" ON LOGIC DWG. INDICATE LOGIC VOLTAGE LEVELS UNDER NORMAL NON-FAULT CONDITIONS.
NORMALLY CONDUCTING TRANSISTORS
715B209


TEST CIRCUIT
RELAY TYPE STU/STU-12
FOR WEAK FEED TERMINAL
PART OF J1
NAMEPLATE RATED
POS. D.C.
4
POS. D.C.
52b
20
52b CONTACT
RATED POS.DC : ELEC. MECH. SYSTEMS
POS. 20VDC SOLID STATE SYSTEMS
59N
21
59N
21S
30
21S
21NP OR 67N
27
21NP OR 67N
21P
26
21P
21NS OR 67NS
31
21NS OR 67NS
27
2
27
IA/IC
32
IA/IC
POS. 20 VDC
TRIP-1
24
TRIP
LOW SIGNAL-1
22
LOW SIGNAL
NOISE (CK. TRIP)-1
23
NOISE CK. TRIP
CHANNEL NO.1
POS. 20 VDC
TRIP-2
19
TRIP
LOW SIGNAL-2
17
LOW SIGNAL
NOISE (CK. TRIP)-2
18
NOISE CK. TRIP
CHANNEL NO.2
NEG. DC
3
NEG. DC
878A366


201C132
11.781
COVER
.125
.125
5.125
.656
17.250
.875
14.000
.313 WIDE X .625 DEEP
4 SLOTS
17.000
18.375
19.000
1.484
2.250
1.484
5.218



WESTINGHOUSE ELECTRIC CORPORATION

RELAY-INSTRUMENT DIVISION

NEWARK, N. J.

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