INSTALLATION • OPERATION • MAINTENANCE

# INSTRUCTIONS

## TYPE STU UNBLOCK RELAY

CAUTION: It is recommended that the user of this equipment become acquainted with the information in either these instructions or the systems instruction leaflet 40-204 before energizing this relay. Failure to observe this precaution may result in damage to the equipment. Before putting the relay into service, operate the relay to check the electrical connections.

Do not remove or insert printed circuit boards while the STU relay is energized.

### APPLICATION

The type STU relay is a solid state directional comparison unblocking auxiliary relay for use with solid state or electromechanical distance relays, and a frequency shift type TCF carrier or TA-3 tone channel. This relay will prevent tripping for faults external to the protected line section to which it is applied and permit high speed simultaneous tripping for internal faults. The relay will respond to indications of fault direction and distance provided by the phase and ground distance relays, thereby controlling the transmission of an unblocking signal and the initiation of high speed tripping for internal faults. Either two or three terminal line applications may be used where all line terminals provide adequate fault current to operate the overreaching distance relays.

### CONSTRUCTION

The STU relay is mounted on a standard 19" wide panel 5-$\frac{1}{4}$" high (3 rack units) with edge slots for mounting on a standard relay rack or panel. For the outline and drilling plan, refer to Fig. 41.

A hinged and removable door on the front of the chassis covers the printed circuit boards. The photograph in Fig. 1 shows the front view of the relay with door open. A sealing post at the top center in front may be used to lock and seal the relay when in service.

The rear panel consists of a hinged door which may be opened to expose various components mounted inside. Mounted on the hinged door are two AR type auxiliary relays and, when used, two AL telephone type relays. The AR relay is a small high-speed attracted armature type of unit. An insulated member, fastened to the free end of the armature, draws down four moving-contact springs to close or open the contacts when the relay coil is energized. This relay is mounted on the rear hinged door, is available for inspection by removing the locking screw and swinging the hinged door outward. In the AL

relays, an electromagnet attracts a right-angle iron bracket which in turn operates a set of make or break contacts. Four power supply resistors are mounted in the rear housing of the chassis. In addition, one 32 terminal connector, J1, and two, four (4) terminal, terminal blocks are mounted on the rear of the panel. The photo in Fig. 2 shows the rear view of the STU relay with the top cover off and rear door open.

All of the circuitry suitable for mounting on printed circuit boards is contained in an enclosure behind the front door. The printed circuit boards slide into position in slotted guides at the top and bottom of the enclosure, and engage a terminal block at the rear of the compartment. Each board and terminal block are keyed so that they cannot be accidently inserted into the wrong slot location. A handle mounted on the front end of the board is used for identification, and for removing and inserting the circuit. In addition the handles also serve as a bumper with the front door to prevent the board from becoming disconnected from its terminal block. The boards may be removed for replacement purposes or for use in conjunction with a board extender (Style No. 849A534G01) which permits access to the boards test points and terminals for making measurements while the relay is energized.

Either 13 or 14 printed circuit boards are used in the STU chassis. The location and title of the printed circuit boards are shown on the relay component location drawing, Fig. 3.

## PRINTED CIRCUIT BOARDS

Following is a description of all the printed circuit boards used in the STU relay. Refer to the functional relay logic shown in Fig. 4, 5, 6, & 7. The internal schematics associated with the printed circuit boards contain a detailed NOR/NAND logic diagram to simplify understanding of the transistor logic.

For those users not generally acquainted with logic circuit notation or with device symbols of those components used in the STU drawings, it is recommended that a copy of Westinghouse instruction leaflet I.L. 41-000.1 entitled SYMBOLS FOR SOLID STATE PROTECTIVE RELAYING be consulted.

### Power Supply Board

The Power Supply board located in slot A contains two 20 volt transistor regulators: These voltage regulators will operate from a nominal battery supply of 48 or 125 volts dc by varing resistors RA, RB, RC, & RD mounted in the rear of the chassis.

The location of components on this board is shown in Fig. 8, and the internal schematic is Fig. 9.

### Protective Relay (P.R.) Interface Boards

The Protective Relay (P.R.) Interface board located in slot B contains the buffered interface logic for the distance relays and the functional test switch. Other logic associated with the protective relays is included.

Location of components on this board is shown in Fig. 10. Two internal schematics are used: Fig. 11 - For use with electromechanical distance relays and Fig. 12 - For use with solid state distance relays. The difference in the two schematics is the buffered distance relay input; 48/125 VDC input for electromechanical systems, 20 VDC input for solid state systems.

Loss of Potential Boards

The Loss of Potential board located in slot C contains a 500/0 millisecond time delay and logic to cause an alarm and voltage output if a distance relay inadvertantly operates on a blown ac potential fuse or has an sustained output for greater than 500 milliseconds. An input AND prevents operation of the timer if both channel trip signals are obtained.

In relays for use with electromechanical systems, a relay driver is provided on this board to energize the Loss of Potential AL telephone relay mounted in the rear of the chassis.

Location of components on this board is shown in Fig. 13. Two internal schematics are used: Fig. 14 - For use with electromechanical systems and Fig. 15 - For use with solid state systems.

ELEC-MECH (E.M.) Interface Board

The ELEC-MECH (E.M.) Interface board located in slot D is used only in systems using electromechanical distance relays. Upon receipt of a distance relay signal, this circuit of two timers (0/25 and 20/0 millisecond) and associated logic will immediately simulate a protective relay signal for 20 milliseconds, thereby overriding any contact bounce in the electromechanical relays.

Location of components on this board is shown in Fig. 16, and the internal schematic in Fig. 17.

Channel Interface Boards

The Channel Interface boards located in slot F (Channel 1) and slot G (Channel 2 - when used) contain the buffered interface logic for connection with the channel equipment and provide the outputs to work into the Channel Trip and Supv. boards. In addition, the TA-3 Channel Interface board contains buffered outputs.

An interlock feature is also included in order to convert from a 2 to 3 terminal line relay and conversely. CHANNEL TWO INTERFACE in slot G must be used in the relay for THREE TERMINAL LINE applications, but MUST BE REMOVED for TWO TERMINAL LINE systems.

A conversion kit may be ordered to change a 2 TERM LINE relay to 3 TERM LINE. This kit includes instructions, nameplate and a CHANNEL INTERFACE board. The location of components for both the TA-3 and TCF - CHANNEL INTERFACE boards is shown in Fig. 18. Internal schematics are shown in Fig. 19 for the TA-3 CHANNEL and Fig. 20 for the TCF CHANNEL.

Channel Trip Boards

The Channel Trip board located in slot H contains the connecting logic between the channel unblock trip signals and the remainder of the relay logic. A buffered output for channel 1 and 2 trip is included on this board.

The Tone Channel Trip board also has additional logic comprised of two AND'S and an OR for a block return function. This logic is inherent to the TCF channel equipment, therefore it is not required in this relay.

Location of components on this board is shown in Fig. 21. Two internal schematics are used: TONE CHANNEL TRIP BOARD - Fig. 22, TCF CHANNEL TRIP BOARD - Fig. 23.

Channel Supervision Boards - TCF Channel

The Channel Supv. Board for a TCF channel is located in slot I and contains the connecting logic between the supervisory functions of the channel equipment and the remainder of the relay logic. Both LOW SIGNAL CLAMP OUTPUTS work into an OR, as do both CHECK TRIP outputs.

In addition, there is a circuit comprised of an AND circuit and a 0/150 millisecond time delay to allow tripping when reclosing into a fault.

For electromechanical systems, a relay driver is used for energizing a loss of channel AL telephone relay.

Location of components for this board is shown in Fig. 26. Two internal schematics are used: Fig. 27 for electromechanical systems and Fig. 28 for solid state systems.

Channel Supervision Board - Tone Channel

The Channel Supv. board for a tone channel is located in slot I and contains the connecting logic between the supervisory functions of the channel equipment and the remainder of the relay logic. A 150/100 millisecond time delay and associated logic is used to monitor the LOW SIGNAL CLAMP outputs for loss of channel and to provide unblock time. For electromechanical systems, a relay driver is used for energizing a Loss of Channel AL telephone relay. The NOISE outputs work into OR logic on this board.

In addition, there is a circuit comprised of an AND circuit and a 0/150 millisecond time delay to allow tripping when reclosing into a fault.

Location of components for this board is shown in Fig. 24 and the internal schematic in Fig. 25.

Transmitter Key Boards

The transmitter Key board located in slot J contains OR logic to combine all inputs required to key the transmitter, and interface circuitry to key the particular channel equipment. A relay driver circuit is connected to the output of the OR in order to operate an AR relay mounted in the rear of the chassis.

For the channel interface with the TCF transmitter, a positive going (0 to 20 volt) buffered output represented by transistors Q4 and Q5 is shown on the internal schematic, Fig. 30. When the relay is used with tone channels, the transmitter interface is a negative going output similar to the relay driver and is shown by transistor Q6 on internal schematic, Fig. 31.

Location of components for the XMTR KEY board is shown in Fig. 29.

Checkback Board

The Checkback board located in slot K contains logic used to functionally test the channel in both directions. Two separate circuits are included on the board. One circuit comprised of a buffered input, AND circuit and a 2500/0 millisecond time delay is used for keying the transmitter for 2.5 seconds after the TEST switch is operated. The other circuit consisting of two AND circuits and a 2500/2500 millisecond time delay is operated from the CHANNEL SUPV. BD. and is required as part of the channel checkback scheme.

The location of components for this board is shown in Fig. 32 and the internal schematic in Fig. 33.

Timing Board

The Timing board located in slot L contains logic, a buffered input, and three time delays used in conjunction with the remainder of the relay.

After a pilot trip operation, the 0/30 millisecond timer maintains the transmitter keying for 30 milliseconds. The 180/0 millisecond timer delays keying of the transmitter for 180 milliseconds after opening of the local breaker. Input to this timer is a 48/125 VDC buffer circuit.

The 2500/0 millisecond timer and associated logic is used to permit transient blocking for 2.5 seconds if a unblock trip output is obtained from the channel receiver. This circuit is also controlled by the 52b contact input.

The location of components on this board is shown in Fig. 34, and the internal schematic in Fig. 35.

Arming Board

The Arming board located in slot M contains the connecting logic between the Channel, Protective Relay, Elec-Mech and Timing boards for the OUTPUT board. Logic on this board interfaces with, and sets up arming of the trip AND, the transient blocking and unblocking timers and the 4/0 millisecond trip timer.

In addition, two time delays, 0/1000 and 0/100 milliseconds, are included on this board. The 0/1000 MS timer holds transient blocking on for an additional 1000 MS to protect against fault power reversals due to unequal breaker reclosing times into a permanent external fault. After a pilot trip operation, the 0/100 MS timer picks up and immediately resets the 0/1000 MS timer to de-energize the transient blocking timer. The 100 MS dropout time is greater than the time it takes to reset the distance relays and remove the input to the 0/1000 MS timer, therefore transient blocking will remain off after the

pilot trip signal is removed.

The location of components for this board is shown in Fig. 36, and the internal schematic in Fig. 37.

Output Board

The Output board located in slot N contains the final logic of the relay. This board utilizes the intelligence supplied by the Arming board to set up either a pilot trip output for internal faults, transient blocking on external faults or transient unblocking for sequential faults.

Three timers are used on this board: a 4/0 millisecond timer to delay the pilot trip output and two 18/0 millisecond timers for transient blocking and unblocking. NOTE: Relays may be supplied with the transient block time calibrated for 25 milliseconds instead of 18 ms. to coordinate with the time delay of the channel equipment. The pilot trip output is comprised of and AND circuit whose output works into a logic inverting amplifier. There are two final pilot trip outputs; a buffered positive going (0 to 20 volt) output and a relay driver to activate an AR relay mounted in the rear of the chassis.

Fig. 38 shows location of components on this board, and Fig. 39 shows the internal schematic and detailed logic.

Test Board

The Test board located in slot O is used for facilitating test measurements and routine checks of the relay. This board consists of 10 test terminals mounted on a panel attached to a printed circuit board.

## OPERATION

The type STU unblock relay is used in a directional comparison unblocking relay system for power line protection. High speed tripping is obtained for two or three terminal line applications for faults anywhere on the protected line, providing all terminals contribute adequate fault current to operate the distance fault detectors.

System Operation

In a directional comparison unblocking system, a continuous blocking signal is normally transmitted from each line terminal and received at all other terminals. The phase or ground protective relays key the channel transmitters to the unblock frequency to remove blocking at the remote terminals during a fault. Tripping is accomplished when both the local protective relay operates, and the blocking signal has been removed. The unblocking signal does not have to be received to allow tripping.

Some features included in this system are a functional test channel checkback scheme, lockout of tripping after 500 milliseconds for abnormal protective relay operation, channel logic to force a block return, and coordination for bus fault tripping, breaker failure and fault power flow reversal. The description of the preceding features are further explained under the Relay

Operation section.

Refer to system I.L. 40-204 on the unblocking system for further system operation.

Relay Operation

Refer to the logic diagrams shown in Fig. 4, 5, 6, and 7 to understand the operation of the STU unblock relay.

1. Normal Condition

In Fig. 4, 5, 6, and 7 the logic voltage "0" and "1" states shown refer to the normal operating condition of the STU relay.

2. Internal Fault

For an internal fault, one or more of the protective distance relays will operate and perform the following:

a. Start the 500/0 MS loss of potential timer
b. Produce a logic "1" at TEST TERM 3 (Protective Relay)
c. Key the transmitter to the unblock frequency
d. Pickup the 0/1000 MS timer on the ARMING BD. and produce a logic "0" at terminal 5 of the OUTPUT BD. This will start the transient blocking timer.
e. Arm the trip AND on the OUTPUT BD. through the one input OR on the ARMING BD.
f. Satisfy one input of the trip AND on the ARMING BD.

The channel transmitter will also be keyed at the remote terminal, thus causing the unblock trip outputs of the local channel 1 and 2 receivers to become a logic "1". This will make TEST TERM 4 (CHANNEL TRIP) a logic "1" signal through logic on the CHANNEL INTERFACE and CHANNEL TRIP BDS. This "1" output will satisfy the trip AND on the ARMING BD. causing energization of the 4/0 MS timer on the OUTPUT BD. Four milliseconds later the trip AND on the OUTPUT BD. will be satisfied and produce a PILOT TRIP output before transient blocking becomes effective.

In addition, when a receiver unblock trip output (logic "1") is received as an input to the STU the 2500/0 MS timer on the TIMING BD. will be energized to start transient blocking. This will not affect the initial pilot trip, and once the local breaker opens, then the 52b contact will block the output of this AND on the TIMING BD.

Once a pilot trip signal is obtained for an internal fault, the 0/100 MS timer on the ARMING BD. will rapidily reset the 1000 millisecond dropout time of the 0/1000 MS timer. Therefore, when reclosing into a permanent internal fault, the only time delay will be the 4/0 MS timer.

3. External Fault

If no unblock trip signal is received from the remote terminal when the local

distance relays operate, then the trip AND on the ARMING BD. will not be satisfied and the 18/0 MS transient blocking timer will time out. TEST TERM 2 (Transient Blocking) will then become a negative logic "1" and block the trip AND of the OUTPUT BD. thereby preventing possible undesirable tripping during transients occuring at the clearing of an external fault.

If an external fault occurs behind the protected line such that the local distance relays do not operate, but either one or both of the channel receivers are keyed to the unblock frequency at the remote terminal then transient blocking will also be set up. When either channel unblock trip output assumes a logic "1" state, the 2500/0 MS timer on the TIMING BD. is energized and a logic "1" is obtained at TIMING BD. terminal 10 for 2.5 seconds. This output will activate the 0/1000 MS timer on the ARMING BD. and set up transient blocking 18 milliseconds later.

In addition, for external faults, transient blocking is established to insure against any misoperation due to fault power flow reversals caused by unequal circuit breaker clearing time on parallel lines. The 1000 millisecond reset time of the 0/1000 MS timer on the ARMING BD. prevents misoperations when reclosing into an external fault where fault power flow reversals occur on parallel lines due to unequal breaker reclosing times. In addition, the 1000 millisecond reset time also prevents transient blocking from resetting when short holes appear in the input.

4. Sequential Fault

Occasionally an external fault will be followed by an internal fault before the former is cleared. In order to prevent a long delay in clearing a sequential fault, a transient unblocking 18/0 MS timer is included. Although transient blocking has been initiated by the external fault, the presence of an internal fault will produce a negative logic "1" signal from the trip AND on the ARMING BD. This "1" signal will energize the 4/0 MS timer and satisfy the AND to energize the 18/0 MS transient unblocking timer on the OUTPUT BD. In 18 milliseconds the transient unblocking timer will drop out the transient blocking timer thus satisfying the trip AND on the OUTPUT BD. and causing a pilot trip output.

5. Loss of Potential

Distance relays may tend to operate if the input from the potential device is momentarily interrupted. Since tripping of circuit breakers is undesirable for this loss of ac potential, or any other abnormal protective relay operation, the STU relay will lockout tripping and provide alarm. This is accomplished by the 500/0 MS timer on the LOSS OF POTENTIAL BD. In 500 milliseconds after a distance relay operation, providing both receiver unblock trip signals are not present, a logic "1" signal will be produced at TEST TERM 7 (Loss of Potential). This "1" signal will block the AND on the PROTECTIVE RELAY INTERFACE BD. thereby simulating no distance relay signal. Output of the 500/0 MS timer will also provide a buffered "1" signal at the J1 connector.

For electromechanical systems, an AL telephone relay will drop out for indication purposes.

6. Channel Transmitter Control

The transmitter may be keyed to the unblock frequency by any one of the following six inputs:

a. Distance relay operation
b. 0/30 MS timer after pilot trip
c. 180/0 MS timer from 52b contact
d. Checkback circuit from test switch
e. Checkback circuit from channel logic
f. Output from E.M. Interface Bd. for electromechanical systems only.

When the transmitter is keyed, TEST TERM 5 (XMTR KEY) becomes a logic "1" signal, the keying AR picks up, and the interface with the transmitter becomes a logic "1" as described under the operation of the XMTR KEYING BD.

After a pilot trip operation the 0/30 MS timer on the TIMING BD. will maintain keying of the unblock frequency for 30 milliseconds in order to insure that the remote breaker has tripped before the transmitter returns to normal condition.

After the local circuit breaker opens, the 52b contact will close and energize the 180/0 MS timer on the TIMING BD. to cause initiation of the unblock frequency transmission after 180 milliseconds and until such time as the circuit breaker is reclosed. This 180 millisecond delay allows coordination for bus fault tripping of the local breaker, where tripping of the remote breaker would be incorrect and might cause undesired interruption to tapped transformer terminals. Transmission of the unblocking frequency is necessary to permit tripping of the remote terminal should the remote circuit breaker be closed into a fault, or should a fault develop in the protected line while the local circuit breaker is open.

7. Channel Logic

a. TCF frequency shift carrier channel.
Refer to CHANNEL-INTERFACE, TRIP, and SUPERVISION BDS. in logic logic drawings Fig. 4 and 5.

Two TCF CHANNEL INTERFACE boards are shown; both boards must be used for three terminal line systems utilizing two receivers. However, for two terminal line application, the interface board in board slot G must not be used in the relay. An interlock shown on the Channel 2 interface board connects the Channel 2 unblock trip output as one input to the channel trip AND on the CHANNEL TRIP BD.

For three terminal line application, both receiver unblock trip signals are required to produce a logic "1" signal at TEST TERM 4. This output will satisfy one input of the ARMING BD. trip AND, block operation of the 500/0 MS Loss of Potential timer, and produce a buffered "1" output. Either receiver unblock trip signal will produce a "1" signal at terminal 12 of the CHANNEL TRIP BD. to start transient blocking. For two terminal line applications, the one receiver unblock trip signal will produce a "1" output at TEST TERM 4 (CHANNEL TRIP), and terminal 12 of the CHANNEL TRIP BD.

Operation of either or both low signal clamp inputs ("1" to "0") will cause a "1" signal at TEST TERM 6 (Loss of Channel) for use in the channel checkback scheme. For electromechanical systems, an AL telephone relay will dropout for

indication of loss of channel. In addition, operation of either Check Trip output will produce a "1" output at terminal 7 of the CHANNEL SUPV. BD. This signal is used for the channel checkback scheme.

If the carrier channel is lost for an internal fault condition then the TCF receiver will convert to an unblock trip signal for 150 milliseconds to allow tripping before lockout. However, it is still desirable to have this system operative if reclosing into a permanent fault. This is accomplished by the 0/150 MS timer and AND circuit on the CHANNEL SUPV. BD. After the initial opening of the breaker, the 52b contact will close and pickup the 0/150 MS timer. Upon reclosure the 52b contact opens and starts dropout of the 0/150 timer, therefore with a loss of channel signal from the TCF, a "1" output will be obtained from the AND. This "1" produces a "1" at TEST TERM 4 to permit tripping if a distance relay operates.

b. Frequency shift tone channel.
Refer to CHANNEL INTERFACE, TRIP and SUPERVISION BDS. in logic drawings Fig. 6 and 7.

Two tone CHANNEL INTERFACE bds. are shown; both boards must be used for three terminal line systems utilizing two receivers. However, for two terminal line applications, the interface board in board slot G must not be used in the relay. An interlock shown on the Channel 2 interface board connects the Channel 2 unblock trip output as one input to the three input channel trip AND on the CHANNEL TRIP BD.

For three terminal line applications, both receiver unblock trip signals and no low signal clamp are required to produce a logic "1" signal at TEST TERM 4 (CHANNEL TRIP). This output will satisfy one input of the ARMING BD. trip AND, block operation of the 500/0 MS Loss of Potential timer, and produce a buffered output. Either receiver unblock trip signal will produce a "1" signal at terminal 12 of the CHANNEL TRIP BD. to start transient blocking and to energize an AND circuit on the CHANNEL SUPV. BD.

For two terminal line applications, the one receiver unblock trip signal will produce a "1" output at TEST TERM 4, and terminal 12 of the CHANNEL TRIP BD.

When a tone channel is used with the STU unblock relay, the tone receivers must be internally strapped to clamp to an unblock trip output when a low signal condition occurs. Therefore, if during an internal fault condition the channel is lost, tripping will be allowed until the 150/100 MS timer on the CHANNEL SUPV. BD. picks up and blocks the channel trip AND on the CHANNEL TRIP BD. However, it is still desirable to have this system operative if reclosing into a permanent fault. This is accomplished by the 0/150 MS timer and AND circuit on the CHANNEL SUPV. BD. After the initial opening of the breaker, the 52b contact will close and pickup the 0/150 MS timer. Upon reclosure the 52b contact opens and starts dropout of the 0/150 timer, therefore with a loss of channel signal from the tones, a "1" output will be obtained from the AND. This "1" produces a "1" at TEST TERM 4 to permit tripping if a distance relay operates.

Either low signal clamp operation ("1" to "0") will pickup the 150/100 MS timer and produce a "1" signal at TEST TERM 6 (LOSS OF CHANNEL) for use in

channel checkback as well as blocking channel trip. For electromechanical systems, an AL telephone relay will dropout for indication of loss of channel. Both low signal clamp outputs on the CHANNEL INTERFACE BDS. are buffered and separately brought out to the J1 connector.

One AND circuit on the CHANNEL SUPV. BD. is used for channel checkback. When a receiver trip signal from either channel is received, a logic "1" will be produced at terminal 3 of the CHANNEL SUPV. BD. providing both low signal clamps have not operated.

When the noise output operates on either one or both channel receivers, a logic "1" output is produced from the noise OR on the CHANNEL SUPV. BD. to block the trip AND of the ARMING BD. Therefore, the STU relay will not trip on receipt of channel noise. Both noise outputs on the CHANNEL INTERFACE BD. are buffered, connected together, and brought out to the J1 connector.

A block return circuit is included on the CHANNEL **TRIP** BD., and is comprised of two AND'S and an OR. The principle of block return is to insure that after a loss of channel condition is cleared up, the receiver unblock trip signal returns in the "0" logic state, not "1". When a low signal clamp operation ("1" to "0") is received from the tone channel, then the 150/100 MS timer picks up and applies a "1" signal to one input of each of the two block return AND'S on the CHANNEL TRIP BD. Now, if either or both receiver unblock trip signals are a "1" or become a "1" within the 100 millisecond dropout time of the 150/100 MS timer, then a "1" output will be produced at the output of the block return AND and the OR in works into. Terminal 5 of the CHANNEL TRIP BD. will become a "1" and hold the 150/100 MS timer picked up by applying a "1" input to the 3 input loss of channel OR on the CHANNEL SUPV. BD. By inspecting the logic, it can be seen that both receiver unblock trip signals (one for two terminal line applications) must return to block, logic "0", to make the channel operative after a loss of channel condition.

8. Channel Checkback Test

   a. TCF frequency shift carrier channel.
      Refer to logic drawings, Fig. 4 and 5. Information in this section does not cover the complete test, but only that portion concerning the STU relay.

At the local terminal, the carrier transmitter will be disconnected from the line thus causing a loss of channel condition at the remote terminal. This will cause the loss of channel OR on the CHANNEL SUPV. BD. (Remote Terminal) to assume a "1", and satisfy the two input AND (preceding the 2500/2500 MS timer), and in 2500 milliseconds pickup the 2500/2500 MS timer on the CHECKBACK BD. The "1" output of the 2500/2500 MS timer will satisfy one input of the AND following it. Next, the test switch will be operated at the local terminal and the following will happen: a protective relay signal will be simulated through the OR on the protective relay interface bd., the transmitter will be reconnected to the line to restore the channel, and the local transmitter will be keyed to the unblock frequency for 2500 milliseconds through the 2500/0 MS timer and AND circuit on the CHECKBACK BD. At the remote terminal, the TCF receiver logic will not give a trip output since the

channel was not restored to the blocking frequency. However, there will be a "1" signal obtained from the CHECK TRIP output of the receiver. This check trip output will satisfy the other input to the AND on the CHECKBACK BD. causing the transmitter to be keyed to the unblock frequency. Since the check trip signal also applies a "1" input to the negated input of the AND energizing the 2500/2500 MS timer, it will no longer be satisfied and the timer will drop out causing keying to stop in 2.5 seconds. However within the 2.5 seconds of keying, the STU relay at the local terminal will trip because of reception of both a received unblock trip signal and a simulated protective relay signal.

b. Frequency shift tone channel.
Refer to logic drawings, Fig. 6 and 7.
Information in this section does not cover the complete test, but only that portion concerning the STU relay.

At the local terminal, the tone transmitter will be disconnected from the line thus causing a loss of channel condition at the remote terminal. This will cause the loss of channel OR on the CHANNEL SUPV. BD. (Remote Terminal) to assume a "1" output to pick up the 150/100 MS timer. This satisfies the two input AND on the CHECKBACK BD. and in 2500 milliseconds the 2500/2500 MS timer will pick up. The "1" output of the 2500/2500 MS timer will satisfy one input of the AND following it. Next, the test switch will be operated at the local terminal and the following will happen: a protective relay signal will be simulated through the OR on the protective relay INT BD, the transmitter will be reconnected to the line to restore the channel, and the local transmitter will be keyed to the unblock frequency for 2500 milliseconds through the 2500 MS timer and AND circuit on the CHECKBACK BD. At the remote terminal, the tone receiver unblock trip signal will be a "1" thus causing the three input AND on the CHANNEL SUPV. BD. to operate and produce a "1" at terminal 3 of this board. This "1" will satisfy the other input to the AND on the CHECKBACK BD. causing the transmitter to be keyed to the unblock frequency. Since at the same time, the input to the 2500/2500 MS timer is lost, then the keying signal to the local terminal will only last 2.5 seconds. However, within this time of keying, the STU relay will trip because of the reception of both a received trip (unblock) signal and a simulated protective relay signal.

9. Electromechanical Interface

When the STU relay is used in an electromechanical system the ELEC-MECH (E.M.) INTERFACE BD. is used only for the purpose of preventing additional tripping delay because of contact bounce. When a distance relay operates, the 0/25 MS time delay on the E.M. INTERFACE BD. will immediately pickup to satisfy the AND thereby simulating a protective relay operation. The 25 millisecond drop-out time of the 0/25 MS timer will hold the "1" input to the AND in the event that bouncing contacts interrupt the timer input signal. The 20/0 timer will time out and remove the simulated protective relay signal after 20 milli-seconds.

## CHARACTERISTICS

| | |
|---|---|
| CONTROL VOLTAGE: | 48 V DC (42 to 56 volts)<br>125 V DC (105 to 140 volts) |
| CURRENT DRAIN: | SOLID STATE SYSTEMS |
| | Normal - 130 MA<br>Pilot Trip - 240 MA<br>Maximum - 280 MA |
| | ELEC-MECH SYSTEMS |
| | Normal - 170 MA<br>Pilot Trip - 280 MA<br>Maximum - 320 MA |
| TEMPERATURE RANGE: | -20°C to +55°C around chassis |
| INPUTS: | |
| 52b Contact - | 48/125 Control Voltage Buffered<br>48 V - 1.5 MA MAX Current<br>125 V - 2.5 MA MAX Current |
| DISTANCE RELAYS 1, 2, and 3: | |
| Solid State Systems - | 15 to 20 V DC Buffered<br>2 MA MAX Current |
| Elec-Mech Systems - | 48/125 Control Voltage Buffered<br>48 V - 1.5 MA MAX Current<br>125 V - 2.5 MA MAX Current |
| All Other Inputs Are Buffered and Require 2 MA MAX Current | 15 to 20 V DC |
| OUTPUTS: | |
| TRAMITTER KEY: | |
| TCF Frequency Shift Carrier Channel | 15 to 20 V DC Buffered<br>10 MA MAX Current |
| Frequency Shift Tone Channel | "0" State - Open Circuit<br>"1" State - Short Circuit to Battery Neg.<br><br>140 V DC MAX Voltage<br>40 MA MAX Current |

All other outputs are 15 to 20 V DC buffered and provide 10 MA MAX Current

## CHARACTERISTICS

| | |
|---|---|
| TIME: | |
| TRIP TIME (4/0) | 4.0 to 4.5 Milliseconds (adjustable from 2.0 to 6.0 MS) |
| TRANSIENT BLOCK and TRANSIENT UNBLOCK TIME (18/0) | 18 to 20 Milliseconds (adjustable from 12 to 30 MS) (Relay may be ordered with a transient blocking time of 24 to 27 milliseconds) |
| LOW SIGNAL LOCKOUT TIME 150/100 & 0/150 | 130 to 180 Milliseconds |
| LOSS OF POTENTIAL TIME (500/0) | 400 to 600 Milliseconds |
| DIMENSIONS: | Relay Height - 5.25" (3 rack units)<br>Relay Width - 19"<br>Relay Depth - 14" |
| WEIGHT: | Approximately 12 lbs. |

## SETTINGS

No setting is required on the STU relay.

## INSTALLATION

The STU relay is generally supplied in a cabinet or on a relay rack as part of a complete system. The location must be free from dust, excessive humidity, vibration, corrosive fumes or heat. The maximum temperature around the chassis must not exceed 55°C.

The outline and drilling plan of the STU relay is shown in Fig. 41.

## ADJUSTMENTS AND MAINTENANCE

### Acceptance Check

It is recommended that an acceptance check be applied to the STU relay to verify that the circuits are functioning properly. The following procedure can be used for this purpose.

Connect the STU relay to the test circuit of Fig. 40. Apply rated dc to J1 terminals 3 and 4 as shown, and use an auxiliary 20 volt regulator or the internal 20 volts of the STU relay for the inputs to the switches. On STU relays for use with electromechanical distance relays, rated positive dc must be applied to the PR 1, 2, and 3 switches. Note that the low signal switches for channels 1 and 2 are normally closed and all other switches are open.

Since the STU relay varies in logic depending on the channel equipment, insure that it is checked per the proper channel. When reference is made to AL relays, this refers to STU relays for use only with electromechanical systems utilizing ELEC-MECH distance relays.

When reference is made to TEST TERM, this means one of the 10 test terminals on the TEST BD. in board slot 0. All voltages are to be measured with respect to negative, TEST TERM 10. Voltage measurements may vary by ±10%. Information in this acceptance test applies to a relay with a transient blocking time of 18 MS for relays with a transient blocking time of 25 MS, limits are 24 to 27 milliseconds.

A. Normal Condition

TEST TERM 1: 0 Volts
" " 2: 20 Volts
" " 3: 0 Volts
" " 4: 0 Volts
" " 5: 0 Volts
" " 6: 0 Volts
" " 7: 0 Volts
" " 8: 20 Volts
" " 9: 20 Volts

Keying AR - not picked up

Trip AR - not picked up

Loss of Channel AL - picked up (Elec-Mech system)

Loss of Potential AL - picked up - (Elec-Mech System)

B. Channel Logic - 2 Term Line Relays Only

(For 3 term. line relays, disregard this section and continue on section C)

1. TCF Carrier Channel

a. Channel Trip - 2500/0 MS timer (TIMING BD.), 0/1000 MS timer (ARMING BD.), transient blocking timer

Close Trip-1 switch

TEST TERM 2: Voltage drop from 20 to 0 volts in 18 to 20 milliseconds, then rise from 0 to 20 volts in 3100 to 4100 milliseconds.

TEST TERM 4: Voltage rise from 0 to 20 volts.

Open Trip 1 switch

b. Loss of Channel

Open Low Signal - 1 Switch

TEST TERM 6: Voltage rise from 0 to 20 volts

Loss of Channel AL will drop out

Close LOW SIGNAL - 1 Switch

2. Tone Channel

a. Channel Trip - 2500/MS timer (TIMING BD.), 0/1000 MS timer (ARMING BD.), transient blocking timer

Close Trip-1 switch

TEST TERM 2: Voltage drop from 20 to 0 volts in 18 to 20 milliseconds, then rise from 0 to 20 volts in 3100 to 4100 milliseconds

TEST TERM 4: Voltage rise from 0 to 20 volts

Open Trip-1 switch

b. Loss of Channel - 150/100 MS timer (CH. SUPV. BD.)

Open LOW SIGNAL - 1 switch

TEST TERM 6: Voltage rise from 0 to 20 volts in 130 to 180 milliseconds

Loss of Channel AL will drop out

Close LOW SIGNAL - 1 switch

TEST TERM 6: Voltage drop from 20 to 0 volts in 75 to 125 milliseconds.

c. Block return

Open LOW SIGNAL - 1 switch, then close Trip-1 switch

TEST TERM 4: Voltage must remain at zero.

Close LOW SIGNAL - 1 switch

TEST TERM 6: Voltage must remain at 20 volts

Open Trip-1 switch

TEST TERM 6: Voltage must drop from 20 to 0 volts

C. Channel Logic - 3 Term Line Relays Only

(For 2 term line relays, the preceding section was used and this part may be disregarded)

1. TCF Carrier Channel

a. Channel 1 - Trip 2500/0 MS timer (TIMING BD.), 0/1000 MS timer (ARMING BD.), transient blocking timer

Close Trip-1 switch

TEST TERM 2: Voltage drop from 20 to 0 volts in 18 to 20 milliseconds then rise from 0 to 20 volts in 3100 to 4100 milliseconds.

TEST TERM 4: Voltage remains at zero

Open Trip - 1 switch

b. Channel 2 - Trip 2500/0 MS timer (TIMING BD.), 0/1000 MS timer (ARMING BD.), transient blocking timer.

Close Trip-2 switch

TEST TERM 2: Voltage drop from 20 to 0 volts in 18 to 20 milliseconds then rise from 0 to 20 volts in 3100 to 4100 milliseconds

TEST TERM 4: Voltage remains at zero

Open Trip - 2 switch

c. Channel 1 and 2 Loss of Channel

Open LOW SIGNAL - 1 switch

TEST TERM 6: Voltage rise from 0 to 20 volts

Loss of Channel AL must drop out.

Close LOW SIGNAL - 1 switch, then open LOW SIGNAL 2 switch

TEST TERM 6: Voltage rise from 0 to 20 volts

Loss of Channel AL must drop out

Close LOW SIGNAL - 2 switch

d. Channel 1 and 2 trip

Close Trip-1 and Trip-2 switches

TEST TERM 4: Voltage rise from 0 to 20 volts

Open Trip-1 and Trip-2 switches

2. Tone Channel

a. Channel 1 - Trip 2500/0 MS timer (TIMING BD.), 0/1000 MS timer (ARMING BD.), transient blocking timer

Close Trip-1 switch

TEST TERM 2: Voltage drop from 20 to 0 volts in 18 to 20 milliseconds then rise from 0 to 20 volts in 3100 to 4100 milliseconds.

TEST TERM 4: Voltage remain at zero.

Open Trip-1 switch

b. Channel 2 - Trip 2500/0 MS timer (TIMING BD.), 0/1000 MS timer (ARMING BD.), transient blocking timer.

Close Trip-2 switch

TEST TERM 2: Voltage drop from 20 to 0 volts in 18 to 20 milliseconds then rise from 0 to 20 volts in 3100 to 4100 milliseconds.

TEST TERM 4: Voltage remain at zero.

Open Trip-2 switch

c. Block Return - Channel 1 - Trip and Low Signal - 150/100 MS Timer

Open LOW SIGNAL - 1 switch

TEST TERM 6: voltage rise from 0 to 20 volts in 130 to 180 milliseconds.

Loss of Channel AL must drop out

Close TRIP-1 switch, then close LOW SIGNAL - 1 switch

TEST TERM 6: voltage must remain at 20 volts

Open TRIP-1 switch

TEST TERM 6: voltage must drop from 20 to 0 volts in 75 to 125 milliseconds.

d. Block Return - Channel 2 - Trip and Low Signal - 150/100 MS Timer

Open LOW SIGNAL - 2 switch

TEST TERM 6: voltage rise from 0 to 20 volts in 130 to 180 milliseconds

Loss of Channel AL must drop out

Close TRIP-1 switch, then close LOW SIGNAL - 1 switch

TEST TERM 6: voltage must remain at 20 volts

Open TRIP-1 switch

TEST TERM 6: voltage must drop from 20 to 0 volts in 75 to 125 milliseconds.

e. Channel 1 and 2 - TRIP and LOW SIGNAL

Close TRIP-1 and TRIP-2 switches

TEST TERM 4: voltage rise from 0 to 20 volts

Open LOW SIGNAL - 1 switch

TEST TERM 4: voltage drop from 20 to 0 volts

Open TRIP-1 and TRIP-2 switches, then close LOW SIGNAL-1 switch

D. Distance Relay Operation

a. Distance relay operation loss of potential 500/0 MS timer

Close PR-1 switch

TEST TERM 7: voltage rise from 0 to 20 volts in 400 to 600 milliseconds

Loss of Potential AL must drop out

TEST TERM 3 & 5: voltage rise from 0 to 20 volts immediately, and then drop from 20 to 0 volts in 400 to 600 milliseconds

XMTR KEY AR picks up immediately then drops out in 400 to 600 milliseconds

Open PR-1 switch

The same as the preceding must happen by closing either the PR-2 or PR-3 switch

b. Distance Relay Operation - no Loss of Potential

Close TRIP-1 and TRIP-2 switches
(TRIP-2 switch not required for 2 TERM LINE relays)

Close either PR-1, PR-2, or PR-3 switches

TEST TERM 7: voltage must remain at zero, the Loss of Potential timer must not pickup.

Open TRIP-1, TRIP-2, and PR switches.

E. Test Switch Operation - 2500/0 MS timer (CHECK BACK BD.)
0/1000 MS timer (ARMING BD.)
18/0 transient Blocking timer (OUTPUT BD.)

Close TEST Switch

TEST TERM 3: voltage must rise from 0 to 20 volts

TEST TERM 2: voltage must drop from 20 to 0 volts in 18 to 20 milliseconds

TEST TERM 5: voltage must rise from 0 to 20 volts immediately, then drop from 20 to 0 volts in 2000 to 3000 milliseconds

Also, XMTR KEY AR must pickup for 2 to 3 seconds

Open TEST Switch

TEST TERM 2: voltage must rise from 0 to 20 volts in 900 to 1300 milliseconds

F. 52b Contact Operation - 180/0 MS timer (TIMING BD.)

Close 52b switch

TEST TERM 5: voltage must rise from 0 to 20 volts in 180 to 230 milliseconds

Open 52b switch

G. Channel Checkback Operation

1. TCF Carrier Channel
2500/2500 MS timer (CHECKBACK BD.)
Check Trip Inputs

Open LOW SIGNAL - 1 switch

TP4 on CHECKBACK BD: voltage must drop from 8 to 0 volts in 2000 to 3000 milliseconds

Close CK TRIP-1 switch

TEST TERM 5: voltage must rise from 0 to 20 volts immediately, then drop from 20 to 0 volts in 2000 to 3000 milliseconds

XMTR KEY AR must pickup for 2 to 3 seconds

Close LOW SIGNAL - 1 switch, then open CK TRIP-1 switch

For relay used for 3 TERM LINE, also do the following

Open LOW SIGNAL-2 switch and wait for 3 seconds, then close CK TRIP-2 switch

TEST TERM 5: voltage must rise from 0 to 20 volts immediately, then drop from 20 to 0 volts in 2 to 3 seconds.

Close LOW SIGNAL - 2 switch, then open CK TRIP-2 switch

2. Tone Channel
2500/2500 MS timer (CHECKBACK BD.)

Open LOW SIGNAL - 1 switch

TP4 on CHECKBACK BD: voltage must drop from 8 to 0 volts in 2000 to 3000 milliseconds

Close TRIP-1 switch, then close LOW signal-1 switch

TEST TERM 5: voltage must rise from 0 to 20 volts immediately then drop from 20 to 0 volts in 2000 to 3000 milliseconds.

XMTR KEY AR must pickup for 2 to 3 seconds

Open TRIP-1 switch

For relays used for 3 TERM LINE, also do the following:

Open both LOW SIGNAL-1 and LOW SIGNAL-2 switches then close TRIP-2 switch. Wait for 3 seconds, then close both LOW SIGNAL 1 and LOW SIGNAL 2 switches.

TEST TERM 5: voltage must rise from 0 to 20 volts immediately after closing both the LOW SIGNAL switches, then drop from 20 to 0 volts in 2 to 3 seconds

Open TRIP-2 switch

H. PILOT TRIP 4/0 MS timer (OUTPUT BD.)

Close 52b switch in order to prevent the 2500/0 timer from starting transient blocking

Close TRIP-1 switch, and also, for 3 TERM LINE relays, close TRIP-2 switch

Then, close TEST switch

TEST TERM 1: voltage must rise from 0 to 20 volts in 4.0 to 4.5 milliseconds.

TRIP AR must pick up

Open TRIP-1 and TRIP-2 switches

TEST TERM 1: voltage must remain at 20 volts

Open TEST switch and TRIP AR must drop out.
Open 52b switch

I. Pilot Trip after Transient Unblocking 18/0 MS timer (OUTPUT BD)

Close TEST switch

Then, close TRIP-1 switch, and also for 3 TERM LINE relays, close TRIP-2 switch.

TEST TERM 1: voltage rise from 0 to 20 volts in 18 to 20 milliseconds

Open TEST switch

TEST TERM 1: voltage drop from 20 to 0 volts

Open TRIP-1 and TRIP-2 switches

J. Continue Key after Pilot Trip - 0/30 MS timer (TIMING BD.)

Close TEST switch, then wait until XMTR KEY AR drops out.

Then close TRIP-1 switch and for 3 TERM LINE relays, also close TRIP-2 switch

As soon as the voltage on TEST TERM 1 rises from 0 to 20 volts, then the 0/30 MS timer will pickup in less than 1 millisecond and the voltage at TEST TERM 5 will rise from 0 to 20 volts.

Then open TEST switch

TEST TERM 5: voltage must drop from 20 to 0 volts in 24 to 30 milliseconds.

Open TRIP-1 and TRIP-2 switches

K. Fast reset of 0/1000 MS timer after pilot trip. 0/100 MS timer (ARMING BD.)

For checking this 0/100 MS timer, it will be necessary to use a jumper.

Close TEST switch, then close TRIP-1 switch and also for 3 TERM LINE relays close TRIP-2 switch

Terminal 4 (ARMING BD.): voltage must rise from 0 to 16 volts in less than 2 milliseconds after the voltage at TEST TERM 1 rises from 0 to 20 volts.

In order to check the 100 millisecond reset time, it is necessary to connect a jumper from TP-8 to terminal 14 on the ARMING BD.

Open TEST switch

Terminal 4 (ARMING BD.) voltage must drop from 16 to 0 volts in 70 to 170 milliseconds

Open TRIP-1 and TRIP-2 switches, and remove the jumper.

L. Elec-Mech Interface 0/25 and 20/0 MS timers (Elec-Mech (E.M.)INTERFACE BD.)

This section is to be used only for those STU relays which are for use with electromechanical distance relays.

Close PR-1, PR-2 or PR-3 switches

Terminal 4 (E.M. INTERFACE BD.): voltage must rise from 0 to 11 volts immediately then drop back to zero in 16 to 24 milliseconds

Open PR-1, PR-2, and PR-3 switches

Terminal 4 (E.M. INTERFACE BD.): voltage must remain at zero

M. Unblock timer for Reclosure 0/150 MS timer (CH. SUPV. BD.)

Close 52b switch, and open LOW SIGNAL-1 switch. This will set up the AND on the CH. SUPV. BD.

Now, open 52b switch

TEST TERM 4: voltage must rise from 0 to 20 volts immediately, then drop back to zero in 130 to 180 milliseconds

Close LOW SIGNAL-1 switch

N. NOISE operation - (Tones Only)

This section is to be used only for those STU relays which are for use with a frequency shift tone channel.

Close NOISE-1 switch

Then close TEST switch and TRIP-1 switch, and also for 3 TERM LINE relays close TRIP-2 switch

TEST TERM 1: voltage must remain at zero

Open NOISE-1 switch

TEST TERM 1: voltage must rise from 0 to 20 volts

Trip AR must pickup

Open TEST, TRIP-1, and TRIP-2 switches

For 3 TERM LINE relays, repeat above test using NOISE-2 switch instead of NOISE-1 switch

Recommended Routine Maintenance

Periodic checks of the relay system are desirable to indicate impending failure so that the equipment can be taken out of service for correction. Any accumulated dust should be removed at regular maintenance intervals.

All contacts should be periodically cleaned. A contact burnisher, style No. 182A836H01, is recommened. The use of abrasive material is not recommended because of the danger of embedding small particles in the face of the soft silver and thus impairing the contact.

## CALIBRATION

The proper adjustments to insure correct operation of the relay have been made at the factory and should not be disturbed after receipt by the customer. However, if the adjustments or if the components or printed circuit boards which affect calibration have been changed, then the STU relay should be rechecked per the acceptance check information.

All time delays are fixed except for the three timers on the OUTPUT BD.:

18/0 MS trandient blocking timer, 18/0 MS transient unblocking timer, and the 4/0 MS trip timer. These adjustable timers can be recalibrated as follows using an auxiliary timer or oscilloscope.

Transient block 18/0 MS timer - OUTPUT BD.

(NOTE: For relays having a transient blocking timer of 25/0 MS limits are 24 to 27 milliseconds)

Start timer on TEST switch (positive pulse)
End timer on TEST TERM 2 (negative pulse)

Close TEST switch and the voltage on TEST TERM 2 must drop from 20 to 0 volts in 18 to 20 milliseconds (24 to 27 MS)

This time can be adjusted by turning potentiometer R14 on the OUTPUT BD. clockwise for more time or counter-clockwise for less time.

Pilot trip 4/0 MS time - OUTPUT BD.

Start timer on TEST SWITCH
End timer on TEST TERM 1

For this calibration, close 52b switch

Close TRIP-1 switch and also TRIP-2 switch for 3 TERM LINE relays.

Then close TEST switch and the voltage on TEST TERM 1 must rise from 0 to 20 volts in 4.0 to 4.5 milliseconds

This time can be adjusted by turning potentiometer R20 on the OUTPUT BD. clockwise for more time or counter-clockwise for less time.

Transient unblocking 18/0 MS timer - OUTPUT BD.

Start timer on TRIP-1 switch
End timer on TEST TERM 1

Close TEST switch, and also close TRIP-2 switch for 3 TERM LINE relays

Then close TRIP-1 switch and the voltage on TEST TERM 1 must rise from 0 to 20 volts in 18 to 20 milliseconds

This time can be adjusted by turning potentiometer R1 on the OUTPUT BD. clockwise for more time and counter-clockwise for less time.

Tripping Relay (AR)

The type AR tripping relay unit has been properly adjusted at the factory to insure correct operation and should not be disturbed after receipt by the customer. If, however, the adjustments are disturbed in error, or it becomes necessary to replace some part in the field, use the following adjustment procedure. This procedure should not be used until it is apparent that the AR unit is not in proper working order, and then only if suitable tools are

available for checking the adjustments.

a. Adjust the set screw at the top of the frame to obtain a 0.009 inch gap at the rear end of the armature air gap.

b. Adjust each contact spring to obtain 4 grams pressure at the very end of the spring. This pressure is measured when the spring moves away from the edge of the slot in the insulated crosspiece.

c. Adjust each stationary contact screw to obtain a contact gap of 0.020 inch. This will give 15-30 grams contact pressure.

Trouble Shooting

The components of the STU relay are operated well within their ratings and normally will give long and trouble-free service. However, if a relay has given an indication of trouble in service or during routine checks, then using "0" and "1" logic notation, the faulty, printed circuit board can be traced to using the diagrams in Fig. 4, 5, 6, or 7. In turn, the faulty component or circuit can be found using the individual schematics of the printed circuit boards, which show the detailed transistor NOR/NAND logic.

Each NOR/NAND logic block represents a transistor on the schematic. The output of each individual logic block is the collector of the transistor which represents that block. The collector of each transistor is either connected to a test point or printed circuit terminal. A box around the transistor indicates that it is conducting for the normal condition of the relay.

Following is an explanation of the voltage levels for the "0" and "1" logic notation as shown for the normal relay condition in Figures 4, 5, 6, and 7. This logic notation will also apply to the detailed logic on the printed circuit board internal schematics.

For positive logic - represented by logic blocks, with no arrows.

"0" is equivalent to less than 0.5 volts with respect to negative, TEST TERM 10.

"1" is equivalent to 8 to 20 volts with respect to negative, TEST TERM 10.

For negative logic - represented by logic blocks with open arrow heads

"0" is equivalent to 8 to 20 volts with respect to negative, TEST TERM 10, except for the output of the relay driver, where a "0" is rated positive dc.

"1" is equivalent to less than 0.5 volts with respect to negative, TEST TERM 10.

A board extender, style No. 849A534G01, is available for facilitating circuit voltage measurements. After withdrawing any one of the circuit boards, the

extender is inserted into that slot. The board is then inserted into the terminal block on the front of the extender to restore all circuit connections.

The TEST TERMINAL'S on the TEST BD. in the board position to the extreme right are helpful in checking the overall relay operation. Following are the voltages that will occur at these TEST TERM's under various conditions:

NOTE: All voltages referred to are taken from respect to negative, TEST TERM 10

TEST TERM 1: PILOT TRIP

Normal Condition - 0 volts

Internal Fault - 20 volts

For an internal fault, either a distance relay or test switch operation and both receiver trip signals (one receiver trip signal for 2 TERM LINE relays) are required.

TEST TERM 2: TRANSIET BLOCKING & UNBLOCKING

Normal Condition - 20 volts

External Fault - 0 volts

The following will simulate an external fault:

Distance relay operation
Test switch operation
Either channel receiver trip operation

TEST TERM 3: PROTECTIVE RELAY

Normal Condition - 0 volts

Distance relay operation - 20 volts

Test Switch Operation - 20 volts

TEST TERM 4: CHANNEL TRIP

Normal Condition - 0 volts

Operation of Channel 1 and 2 receiver trip

Outputs - (for 2 TERM Line Relays, only Channel 1 required) - 20 volts

TEST TERM 5: XMTR KEY

Normal Condition - 0 volts

Distance relay operation - 20 volts

52b contact operation - 20 volts

Internal Fault
(pilot trip signal) - 20 volts

Test Switch Operation - 20 volts for 2.5 seconds

Channel checkback scheme - 20 volts for 2.5 seconds

TEST TERM 6: LOSS OF CHANNEL

Normal Condition - 0 volts

Operation of either Channel 1 or 2
Low Signal Clamp - 20 volts

TEST TERM 7: LOSS OF POTENTIAL

Normal Condition - 0 volts

Distance Relay Operation - 20 volts after 500 MS time delay

Distance relay and both receiver trip signal
Operation (one receiver trip signal for 2 TERM LINE relays) - 0 volts

TEST TERM 8 and 9: POS. 20 V DC

Normal Condition: 18 to 21 volts

TEST TERM 10: NEGATIVE DC

## RENEWAL PARTS

Repair work can be done most satisfactorily at the factory. However, interchangeable parts can be furnished to the customers who are equipped for doing the repair work. When ordering parts, always give the complete nameplate data, and the component style no. given in the Electrical Parts List.

ELECTRICAL PARTS LIST

Power Supply Board (S# 202C465G01)

| Circuit Symbol | Reference | Style |
|---|---|---|
| | CAPACITORS | |
| C1, C2 | 6.8 MFD, 35 V, ±20% | 184A761H10 |
| | DIODES | |
| D1, D2 | 1N645A | 837A692H03 |
| | RESISTORS | |
| None on PCB | None | |
| | TRANSISTORS | |
| Q1, Q2 | 2N3589 | 837A617H01 |
| Heat Sink for Q1, Q2 | | 849A517H01 |
| | ZENER DIODE | |
| Z1, Z3 | 1N3050A (180 V - 1W) | 187A936H16 |
| Z2, Z4 | 1N4747A ( 20 V - 1W) | 849A487H01 |

Protective Relay (S# 202C466G01) - Solid State Systems
Interface Board (S# 202C475G01) - Elec-Mech Systems

| | | |
|---|---|---|
| | CAPACITORS | |
| C1, C2 | .047 MFD, 200 V DC | 849A437H04 |
| | DIODES | |
| D1, D2 | 1N645A | 837A692H03 |
| | RESISTORS | |
| R1, R2, R3 Δ | 4.7 K, ½W, ±2% | 629A531H48 |
| R1, R2, R3 # | 47 K, ½W, ±2% | 629A531H72 |
| R4, R15, R16 | 4.7 K, ½W, ±2% | 629A531H48 |
| R5, R17, R22 | 82 K, ½W, ±2% | 629A531H78 |
| R6, R9, R13, R19, R20 | 10 K, ½W, ±2% | 629A531H56 |
| R7, R10, R14, R21 | 6.8 K, ½W, ±2% | 629A531H52 |
| R8, R11, R12, R18 | 27 K, ½W, ±2% | 629A531H66 |
| | TRANSISTORS | |
| Q1, Q2, Q3, Q4 | 2N3417 | 848A851H02 |
| Q5 | 2N3645 | 849A441H01 |

ELECTRICAL PARTS LIST

Protective Relay (S# 202C466G01) - Solid State Systems
Interface Board (S# 202C475G01) - Elec-Mech Systems

| Circuit Symbol | Reference | Style |
|---|---|---|
| | ZENER DIODES | |
| Z1, Z2, Z3 | 1N3688A, 29 V, ±10% | 862A288H01 |
| Z4, Z6 | 1N3686B, 20 V, ±5% | 185A212H06 |
| Z5, Z7 | 1N957B, 6.8 V, ±5% | 186A797H06 |

Δ - Solid State Systems
\# - Elec-Mech Systems

Loss of Potential Board (S# 202C467G01) - Elec-Mech Systems
(S# 202C529G01) - Solid State Systems

| | | |
|---|---|---|
| | CAPACITORS | |
| C1 | 22 MFD, 35 V | 184A661H16 |
| C2 | .27 MFD, 200 V DC | 188A669H05 |
| | DIODES | |
| D1, D2 | 1N645A | 837A692H03 |
| | RESISTORS | |
| R1, R4, R5, R14 | 27 K, ½W, ±2% | 629A531H66 |
| R2, R6, R9, R10 R15, R18 | 10 K, ½W, ±2% | 629A531H56 |
| R3, R11, R16 | 6.8 K, ½W, ±2% | 629A531H52 |
| R7 Δ | 43 K, ½W, ±2% | 629A531H71 |
| R8 | 470 ohm, ½W, ±2% | 629A531H24 |
| R12 | 82 K, ½W, ±2% | 629A531H78 |
| R13 | 150 ohm, 3W, ±5% | 762A679H01 |
| R17 | 1 K, ½W, ±2% | 629A531H32 |
| | TRANSISTORS | |
| Q1, Q2, Q3, Q5 | 2N3417 | 848A851H02 |
| Q4 | 2N3645 | 849A441H01 |
| Q6 | 2N3589 | 837A617H01 |
| | ZENER DIODES | |
| Z1 | 1N957B, 6.8 V, ±5% | 186A797H06 |
| Z2 | 1N3688A, 24 V, ±10% | 862A288H01 |
| Z3 | 1N3050B, 180 V | 187A936H17 |

Loss of Potential Board (S# 202C467G01) - Elec-Mech Systems (continued)
(S# 202C529G01) - Solid State Systems

Δ - Indicates Typical Value

Elec-Mech Interface Board (S# 202C468G01)

| Circuit Symbol | Reference | Style |
|---|---|---|
| | CAPACITORS | |
| C1, C2 | 1.5 MFD, 35 V, ±5% | 187A508H18 |
| | DIODES | |
| D1, D2, D3, D4, D5 | 1N645A | 837A692H03 |
| | RESISTORS | |
| R1 | 27 K, ½W, ±2% | 629A531H66 |
| R2, R5, R9, R12 R14, R15 | 10 K, ½W, ±2% | 629A531H56 |
| R3 Δ | 30 K, ½W, ±2% | 629A531H67 |
| R4 | 22 ohm, ½W, ±5% | 187A290H09 |
| R6 | 12 K, ½W, ±2% | 629A531H58 |
| R7 Δ | 12 K, ½W, ±2% | 629A531H58 |
| R8 | 470 ohm, ½W, ±2% | 629A531H24 |
| R10, R11, R13 | 22 K, ½W, ±2% | 629A531H64 |
| R16 | 6.8 K, ½W, ±2% | 629A531H52 |
| | TRANSISTORS | |
| Q1, Q2, Q3, Q4, Q5 | 2N3417 | 848A851H02 |
| | ZENER DIODES | |
| Z1, Z2 | 1N957B | 186A797H06 |

Δ - Indicates Typical Value

Channel Interface Board (S# 202C530G01) - TCF Int.
(S# 202C469G01) - TA3 Int.

| | CAPACITORS | |
|---|---|---|
| C1, C3, C5 | .047 MFD, 200 V DC | 849A437H04 |
| C4, C6 | .27 MFD, 200 V DC | 188A669H05 |

ELECTRICAL PARTS LIST

Channel (S# 202C530G01) - TCF Int. (continued)
Interface Board (S# 202C469G01) - TA3 Int.

| Circuit Symbol | Reference | Style |
|---|---|---|
| | DIODES | |
| D2, D3 | 1N645A | 837A692H03 |
| | RESISTORS | |
| R1, R2, R9, R10 R17, R18 | 4.7 K, ½W, ±2% | 629A531H48 |
| R3, R7, R11, R15 R19, R23 | 82 K, ½W, ±2% | 629A531H78 |
| R4, R5, R12, R13 R20, R21, R26 | 10 K, ½W, ±2% | 629A531H56 |
| R6, R14, R22, R27 | 6.8 K, ½W, ±2% | 629A531H52 |
| R16, R24 | 150 ohm, 3 W, ±5% | 762A679H01 |
| R25 | 27 K, ½W, ±2% | 629A531H66 |
| | TRANSISTORS | |
| Q1, Q3, Q5, Q7 | 2N3417 | 848A851H02 |
| Q2, Q4, Q6 | 2N3645 | 849A441H01 |
| | ZENER DIODES | |
| Z1, Z4, Z7 | 1N3686B, 20 V, ±5% | 185A212H06 |
| Z2, Z5, Z8 | 1N957B, 6.8 V, ±5% | 186A797H06 |
| Z6, Z9, Z10 | 1N3688A, 24 V, ±20% | 862A288H01 |

Channel (S# 202C471G01) - TCF
Trip Board (S# 202C472G01) - Tone

| | | |
|---|---|---|
| | CAPACITORS | |
| C1 | 0.27 MFD, 200 V. | 188A669H05 |
| | DIODES | |
| D1 | 1N645A | 837A692H03 |
| | RESISTORS | |
| R1, R2, R5, R8, R11, R14, R17, R32, R33, R34, R37, R43 | 27 K, ½W, ±2% | 629A531H66 |
| R3, R6, R9, R12, R15 R19, R23, R27, R30, R35 R38, R39 | 10 K, ½W, ±2% | 629A531H56 |

ELECTRICAL PARTS LIST

Channel (S# 202C471G01) - TCF (continued)
Trip Board (S# 202C472G01) - Tone

| Circuit Symbol | Reference | Style |
|---|---|---|
| | **RESISTORS** | |
| R4, R7, R10, R13 R16, R20, R24, R28, R31, R36, R40 | 6.8 K, ½W, ±2% | 629A531H52 |
| R41 | 82 K, ½W, ±2% | 629A531H78 |
| R42 | 150 ohm, 3 W, ±5% | 762A679H01 |
| | **TRANSISTORS** | |
| Q1, Q2, Q3, Q4, Q5, Q6, Q7, Q8, Q9, Q10, Q11 | 2N3417 | 848A851H02 |
| Q12 | 2N3645 | 849A441H01 |
| | **ZENER DIODES** | |
| Z1 | 1N3688A, 24 V, ±10% | 862A288H01 |

TCF Channel (S# 202C473G01) - Elec-Mech Systems
Supv. Board (S# 202C531G01) - Solid State System

| | | |
|---|---|---|
| | **CAPACITORS** | |
| C1 | 6.8 MFD, 35 V, ±5% | 184A661H21 |
| | **DIODES** | |
| D1, D2, D3 | 1N645A | 837A692H03 |
| | **RESISTORS** | |
| R1, R2, R6, R9, R14, R18, R19, R22, R23, R26 | 27 K, ½W, ±2% | 629A531H66 |
| R3, R4, R7, R10, R13 R15, R20, R24, R27 | 10 K, ½W, ±2% | 629A531H56 |
| R5, R8, R11, R21, R25, R28 | 6.8 K, ½W, ±2% | 629A531H52 |
| R12 | 1 K, ½W, ±2% | 629A531H32 |
| R17 | 470 ohm, ½W, ±2% | 629A531H24 |
| R16 Δ | 43 K, ½W, ±2% | 629A531H71 |
| | **TRANSISTORS** | |
| Q1, Q3, Q4, Q6, Q7 Q8, Q9 | 2N3417 | 848A851H02 |

ELECTRICAL PARTS LIST

TCF Channel (S# 202C473G01) - Elec-Mech Systems (continued)
Supv. Board (S# 202C531G01) - Solid State System

| Circuit Symbol | Reference | Style |
|---|---|---|
| | TRANSISTORS | |
| Q2 | 2N3645 | 849A851H02 |
| Q5 | 2N3589 | 837A617H01 |
| | ZENER DIODES | |
| Z1 | 1N3050B, 180 V. | 187A936H17 |
| Z2 | 1N957B, 6.8 V, ±5% | 186A797H06 |

Δ - Indicates Typical Value

Tone Channel (S# 203C253G01) - Elec-Mech or
Supv. Board Solid State Systems

| | | |
|---|---|---|
| | CAPACITORS | |
| C1 | 12 MFD, 35 V, ±10% | 862A530H05 |
| C2 | 6.8 MFD, 35 V, ±5% | 184A661H21 |
| | DIODES | |
| D1, D2, D3, D4, D5, D6 | 1N645A | 837A692H03 |
| | RESISTORS | |
| R1, R2, R3, R6 R15, R20, R23, R24, R25, R28, R29, R32, R35, R39 | 27 K, ½W, ±2% | 629A531H66 |
| R4, R7, R12, R13 R16, R19, R21, R26, R30, R33, R36, R41 | 10 K, ½W, ±2% | 629A531H56 |
| R5, R8, R14, R22, R27, R31, R34, R42 | 6.8 K, ½W, ±2% | 629A531H52 |
| R9 Δ | 22 K, ½W, ±2% | 629A531H64 |
| R10 Δ | 10 K, ½W, ±2% | 629A531H56 |
| R11 | 15 K, ½W, ±2% | 629A531H60 |
| R17 | 5.6 K, ½W, ±2% | 629A531H50 |
| R18 | 1 K, ½W, ±2% | 629A531H32 |
| R37 Δ | 43 K, ½W, ±2% | 629H531H71 |
| R38 | 470 ohms, ½W, ±2% | 629A531H24 |
| R40 | 12 K, ½W, ±2% | 629A531H58 |

ELECTRICAL PARTS LIST

Tone Channel (S# 203C253G01) - Elec-Mech or Solid State Systems (continued)
Supv. Board

| Circuit Symbol | Reference | Style |
|---|---|---|
| | TRANSISTORS | |
| Q1, Q2, Q3, Q5 Q7, Q8, Q9, Q10, Q11, Q12 | 2N3417 | 848A851H02 |
| Q4 | 2N3645 | 849A441H01 |
| Q6 | 2N3589 | 837A617H01 |
| | ZENER DIODES | |
| Z1, Z3 | 1N957B, 6.8 V, ±5% | 186A797H06 |
| Z2 | 1N3050B, 180 V | 187A936H17 |

Δ - Indicates Typical Valve

Transmitter (S# 202C534G01) - TCF Ch.
Key Board (S# 202C535G01) - Tone Ch.

| | | |
|---|---|---|
| | CAPACITORS | |
| C1, C2 | 0.27 MFD, 200 V DC | 188A669H05 |
| | DIODES | |
| D1, D2, D3, D4, D5, D6, D7 | 1N645A | 837A692H03 |
| | RESISTORS | |
| R1, R2, R3, R4, R5, R6, R7, R13 | 27 K, ½W, ±2% | 629A531H66 |
| R8, R9, R12, R14, R15, R20 | 10 K, ½W, ±2% | 629A531H56 |
| R10, R11, R16 | 6.8 K, ½W, ±2% | 629A531H52 |
| R17 | 82 K, ½W, ±2% | 629A531H78 |
| R18 | 150 ohm, 3W, ±5% | 762A679H01 |
| R19 | 4.7 K, ½W, ±2% | 629A531H48 |
| | TRANSISTORS | |
| Q1, Q4 | 2N3417 | 848A851H02 |
| Q2, Q5 | 2N3645 | 849A441H01 |
| Q3, Q6 | 2N3589 | 837A617H01 |

ELECTRICAL PARTS LIST

Transmitter (S# 202C534G01) - TCF Ch. - (continued)
Key Board (S# 202C535G01) - Tone Ch.

| Circuit Symbol | Reference | Style |
|---|---|---|
| | ZENER DIODES | |
| Z1, Z3 | 1N3688A, 24 V, ±10% | 862A288H01 |
| Z2, Z4 | 1N3050B, 180 V | 187A936H17 |

Checkback Board (S# 202C476G01)

| | | |
|---|---|---|
| | CAPACITORS | |
| C1, C2, C4 | 150 MFD, 35 V | 849A007H01 |
| C3 | .047 MFD, 200 V DC | 849A437H04 |
| | DIODES | |
| D1, D2, D3, D4, D5, D6 | 1N645A | 837A692H03 |
| | RESISTORS | |
| R1, R4, R7, R8, R15, R23, R27 | 27 K, ½W, ±2% | 629A531H66 |
| R2, R5, R9, R12, R16, R21, R24, R28 | 10 K, ½W, ±2% | 629A531H56 |
| R3, R6, R17, R22 R29 | 6.8 K, ½W, ±2% | 629A531H52 |
| R10 Δ, R13 Δ, R25 Δ | 33 K, ½W, ±2% | 629A531H68 |
| R11, R14, R26 | 470 ohm, ½W, ±2% | 629A531H24 |
| R18, R19 | 4.7 K, ½W, ±2% | 629A531H48 |
| R20 | 82 K, ½W, ±2% | 629A531H78 |
| | TRANSISTORS | |
| Q1, Q2, Q3, Q4, Q5 Q6, Q7, Q8 | 2N3417 | 848A851H02 |
| | ZENER DIODES | |
| Z1, Z2, Z4, Z5 | 1N957B, 6.8 V, ±5% | 186A797H06 |
| Z3 | 1N3686B, 20 V, ±5% | 185A212H06 |

Δ - Indicates Typical Value

ELECTRICAL PARTS LIST

Timing Board (S# 202C477G01)

| Circuit Symbol | Reference | Style |
|---|---|---|
| | **CAPACITORS** | |
| C1 | .047 MFD, 200 V | 849A437H04 |
| C2 | 12 MFD, 35 V, ±10% | 862A530H05 |
| C3 | 1.5 MFD, 35 V, ±5% | 187A508H18 |
| C4 | 150 MFD, 30 V, ±10% | 849A007H01 |
| C5 | 1.0 MFD, 35 V, ±10% | 837A241H15 |
| | **DIODES** | |
| D1, D2, D3, D4, D5 | 1N645A | 837A692H03 |
| | **RESISTORS** | |
| R1, R2 | 4.7 K, ½W, ±2% | 629A531H48 |
| R3 | 82 K, ½W, ±2% | 629A531H78 |
| R4, R7, R10, R13 R16, R19, R22, R25, R28, R33 | 10 K, ½W, ±2% | 629A531H56 |
| R5, R8, R14, R17, R23, R26, R34 | 6.8 K, ½W, ±2% | 629A531H52 |
| R6, R9, R15, R18, R24, R27, R31, R32, R35 | 27 K, ½W, ±2% | 629A531H66 |
| R11 | 30 K, ½W, ±2% | 629A531H67 |
| R12, R21, R30 | 470 ohm, ½W, ±2% | 629A531H24 |
| R20 Δ, R29 Δ | 33 K, ½W, ±2% | 629A531H68 |
| | **TRANSISTORS** | |
| Q1, Q2, Q3, Q4, Q5, Q6, Q7, Q8, Q9, Q10 | 2N3417 | 848A851H02 |
| | **ZENER DIODES** | |
| Z1 | 1N3686B, 20 V, ±5% | 185A212H06 |
| Z2, Z3, Z4, Z5 | 1N957B, 6.8 V, ±5% | 186A797H06 |

Δ - Indicates Typical Value

ELECTRICAL PARTS LIST

Arming Board (S# 202C478G01)

| Circuit Symbol | Reference | Style |
|---|---|---|
| | CAPACITORS | |
| C1 | 22 MFD, 35 V, ±10% | 184A661H16 |
| C2 | 3.3 MFD, 35 V, ±5% | 862A530H01 |
| | DIODES | |
| D1, D2, D3, D4, D5 | 1N645A | 837A692H03 |
| | RESISTORS | |
| R1, R2, R5, R8, R9, R10, R16, R20, R23 R24, R25 | 27 K, ½W, ±2% | 629A531H66 |
| R3, R6, R11, R12, R18, R21, R26, R27, R32, R36 | 10 K, ½W, ±2% | 629A531H56 |
| R4, R7, R13, R19, R22, R28, R33 | 6.8 K, ½W, ±2% | 629A531H52 |
| R14 | 82 K, ½W, ±2% | 629A531H78 |
| R15 | 20 K, ½W, ±2% | 629A531H63 |
| R29, R34 | 1 K, ½W, ±2% | 629A531H32 |
| R30 | 100 ohm, ½W, ±2% | 629A531H08 |
| R31 | 15 K, ½W, ±2% | 629A531H60 |
| R35 | 12 K, ½W, ±2% | 629A531H58 |
| | TRANSISTORS | |
| Q1, Q2, Q3, Q5, Q6, Q7, Q9, Q10 | 2N3417 | 848A851H02 |
| Q4, Q8 | 2N3645 | 849A441H01 |

Δ - Indicates Typical Value

Output Board (S# 202C479G01)

| | CAPACITORS | |
|---|---|---|
| C1 | 1.5 MFD, 35 V, ±10% | 187A508H18 |
| C2, C4, C7 | 0.22 MFD, 100 V | 763A219H21 |
| C3 | 3.3 MFD, 35 V, ±10% | 862A530H01 |
| C6 | 0.047 MFD, 200 V. | 849A437H04 |
| C8, C9 | 0.1 MFD, 200 V | 188A669H03 |
| C10 | 0.27 MFD, 200 V | 188A669H05 |

ELECTRICAL PARTS LIST

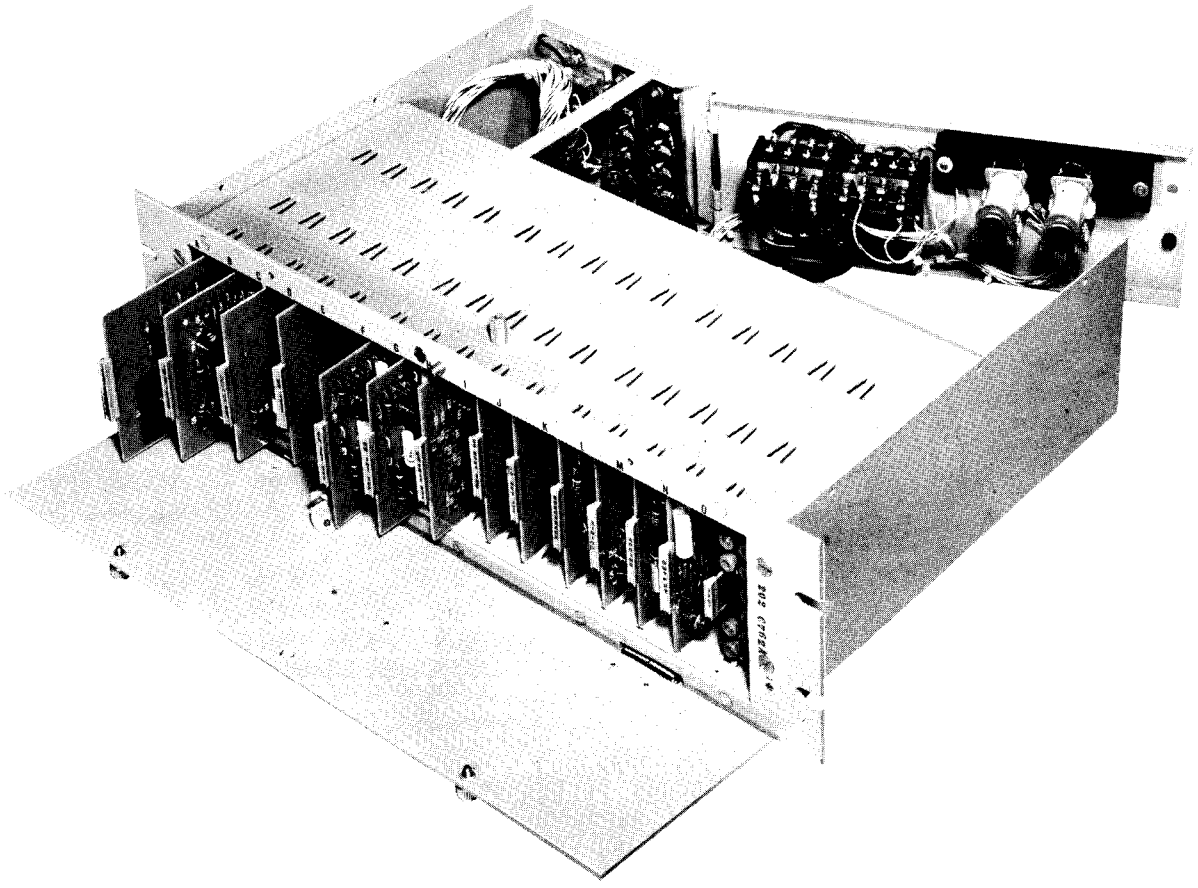
Output Board (S# 202C479G01) - (continued)

| Circuit Symbol | Reference | Style |
|---|---|---|
| | **DIODES** | |
| D1, D2, D3, D4, D5, D6, D7, D8 | 1N645A | 837A692H03 |
| | **POTENTIOMETERS** | |
| R1 | 50 K, $\frac{1}{4}$ W, ±20% | 629A430H01 |
| R14 | 15 K, $\frac{1}{4}$ W, ±20% | 629A430H08 |
| R20 | 1 K, $\frac{1}{4}$ W, ±20% | 629A430H02 |
| | **RESISTORS** | |
| R2, R7, R9, R12, R18, R21, R23, R24, R25, R26, R30, R31, R34, R36, R37 | 10 K, $\frac{1}{2}$W, ±2% | 629A531H56 |
| R3 | 150 K, $\frac{1}{2}$W, ±5% | 629A531H84 |
| R6 | 47 ohm, $\frac{1}{2}$W, ±5% | 187A290H17 |
| R8, R35 | 27 K, $\frac{1}{2}$W, ±2% | 629A531H66 |
| R10, R15 | 470 ohm, $\frac{1}{2}$W, ±2% | 629A531H24 |
| R11 | 470 K, $\frac{1}{2}$W, ±5% | 184A763H91 |
| R16, R28 | 4.7 K, $\frac{1}{2}$W, ±2% | 629A531H48 |
| R4, R17, R19, R22, R29 | 22 K, $\frac{1}{2}$W, ±2% | 629A531H64 |
| R5, R27, R32, R33, R38 | 6.8 K, $\frac{1}{2}$W, ±2% | 629A531H52 |
| R39 | 82 K, $\frac{1}{2}$W, ±2% | 629A531H78 |
| R40 | 150 ohm, 3W, ±5% | 762A679H01 |
| R13 | 15 K, $\frac{1}{2}$W, ±2% | 629A531H60 |
| | **TRANSISTORS** | |
| Q1, Q4, Q5, Q6, Q8, Q11 | 2N3645 | 849A441H01 |
| Q2, Q3, Q7, Q10 | 2N3417 | 848A851H02 |
| Q9 | 2N3589 | 837A617H01 |
| | **ZENER DIODES** | |
| Z1, Z7 | 1N3688A, 24 V, ±10% | 862A288H01 |
| Z2, Z3, Z4, Z5 | 1N957B, 6.8 V, ±5% | 186A797H06 |
| Z6 | 1N3050B, 180 V | 187A936H17 |

ELECTRICAL PARTS LIST

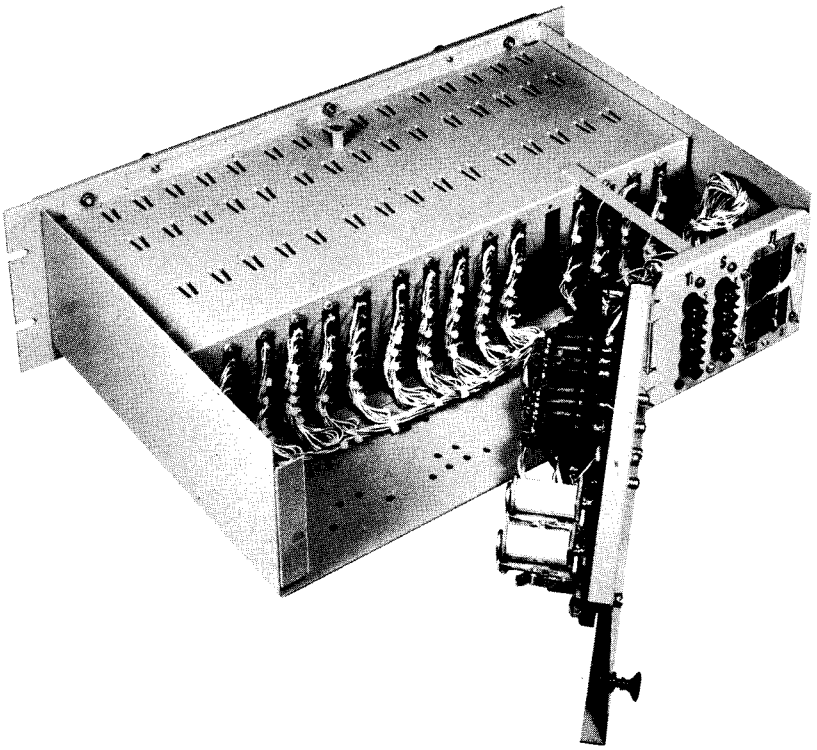
Test Board (S# 5490D87G01)

| Circuit Symbol | Reference | Style |
|---|---|---|
| Tip Jacks (red)<br>1, 2, 3, 4, 5, 6,<br>7, 8, 9 | | 187A332H01 |
| Tip Jacks (black)<br>10 | | 187A332H02 |



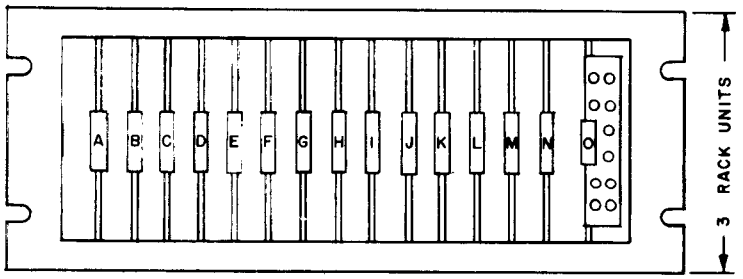
69-279

**Fig. 1 Photograph (Front View with Door open).**



69-280

Fig. 2 Photograph (rear view taken above relay with top cover off and door open).

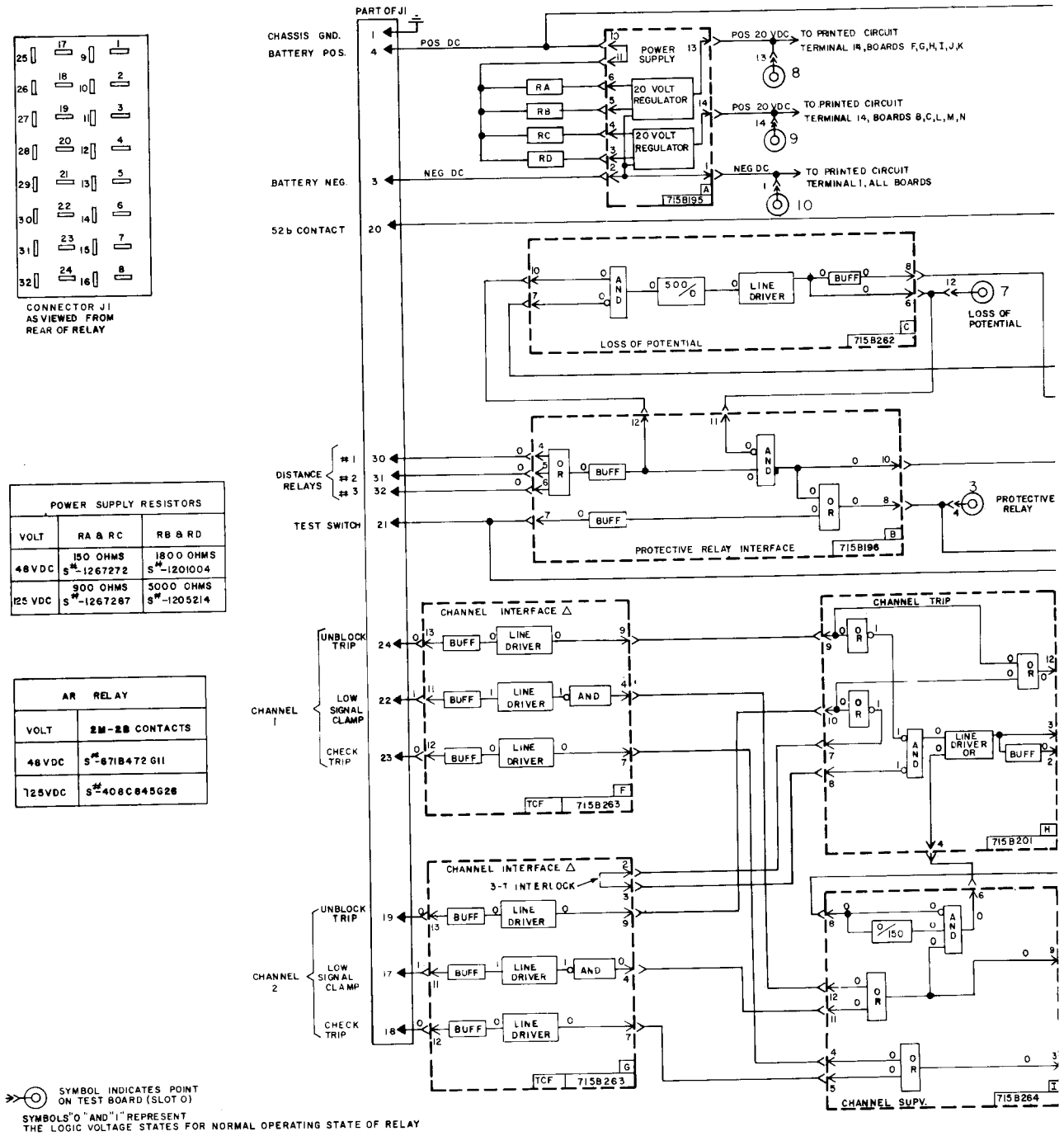



FRONT VIEW
(COVER REMOVED)

| BOARD POSITION | BOARD DESCRIPTION |
|---|---|
| A | POWER SUPPLY |
| B | PROTECTIVE RELAY INTERFACE |
| C | LOSS OF POTENTIAL |
| D | ELEC. MECH. INTERFACE |
| E | ——— |
| F | CHANNEL 1 INTERFACE |
| G | CHANNEL 2 INTERFACE |
| H | CHANNEL TRIP |
| I | CHANNEL SUPERVISION |
| J | CHANNEL TRANSMITTER KEY |
| K | CHECK BACK |
| L | TIMING |
| M | ARMING |
| N | OUTPUT |
| O | TEST |

876A611

Fig. 3 Relay Component Location.




CONNECTOR J1
AS VIEWED FROM
REAR OF RELAY

| POWER SUPPLY RESISTORS | | |
|---|---|---|
| VOLT | RA & RC | RB & RD |
| 48 VDC | 150 OHMS S#-1267272 | 1800 OHMS S#-1201004 |
| 125 VDC | 900 OHMS S#-1267267 | 3000 OHMS S#-1205214 |

| AR RELAY | |
|---|---|
| VOLT | 2M-2B CONTACTS |
| 48 VDC | S#-6718472 G11 |
| 125 VDC | S#-408C845G26 |

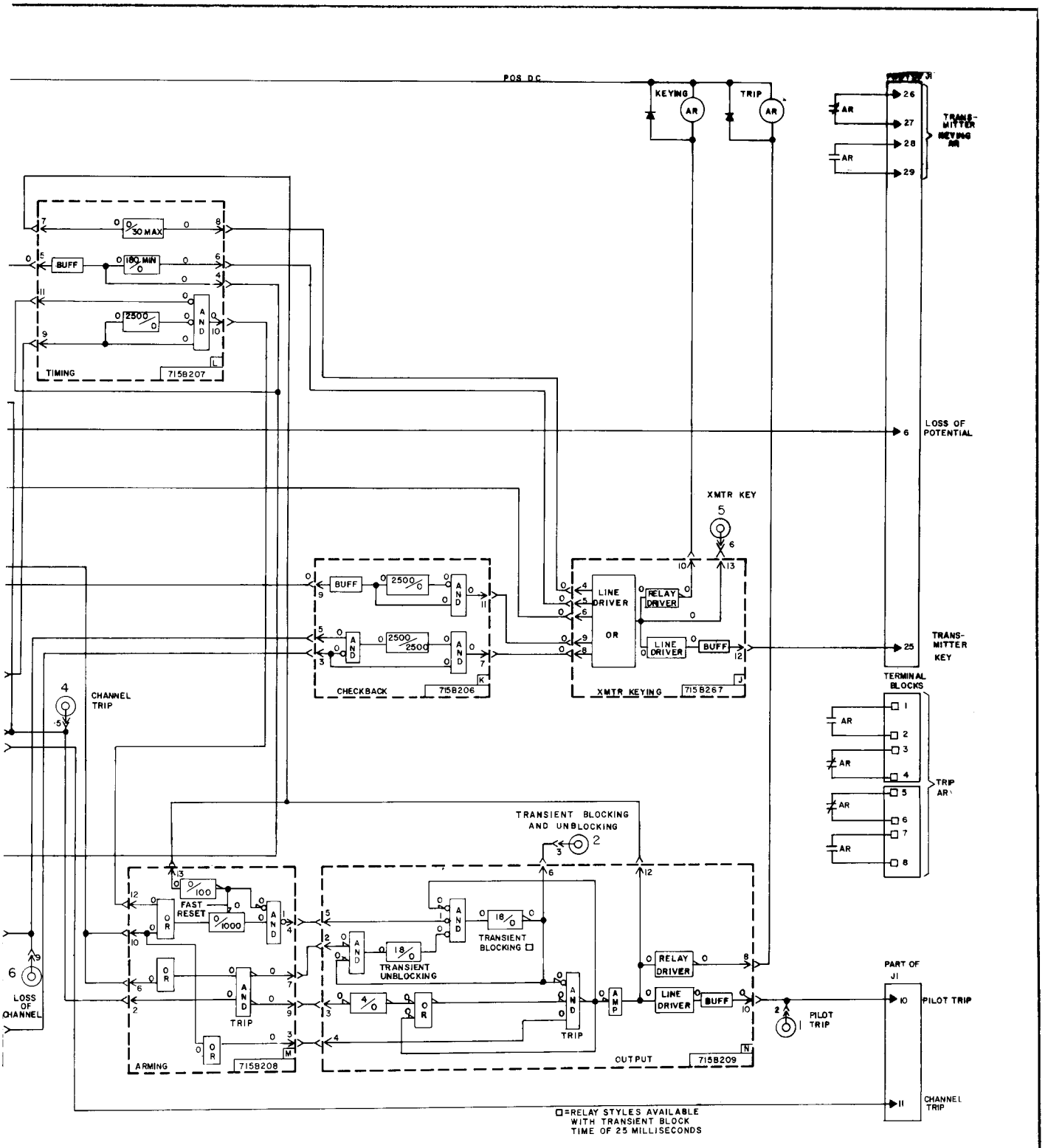
SYMBOL INDICATES POINT ON TEST BOARD (SLOT 0)

SYMBOLS "0" AND "1" REPRESENT THE LOGIC VOLTAGE STATES FOR NORMAL OPERATING STATE OF RELAY

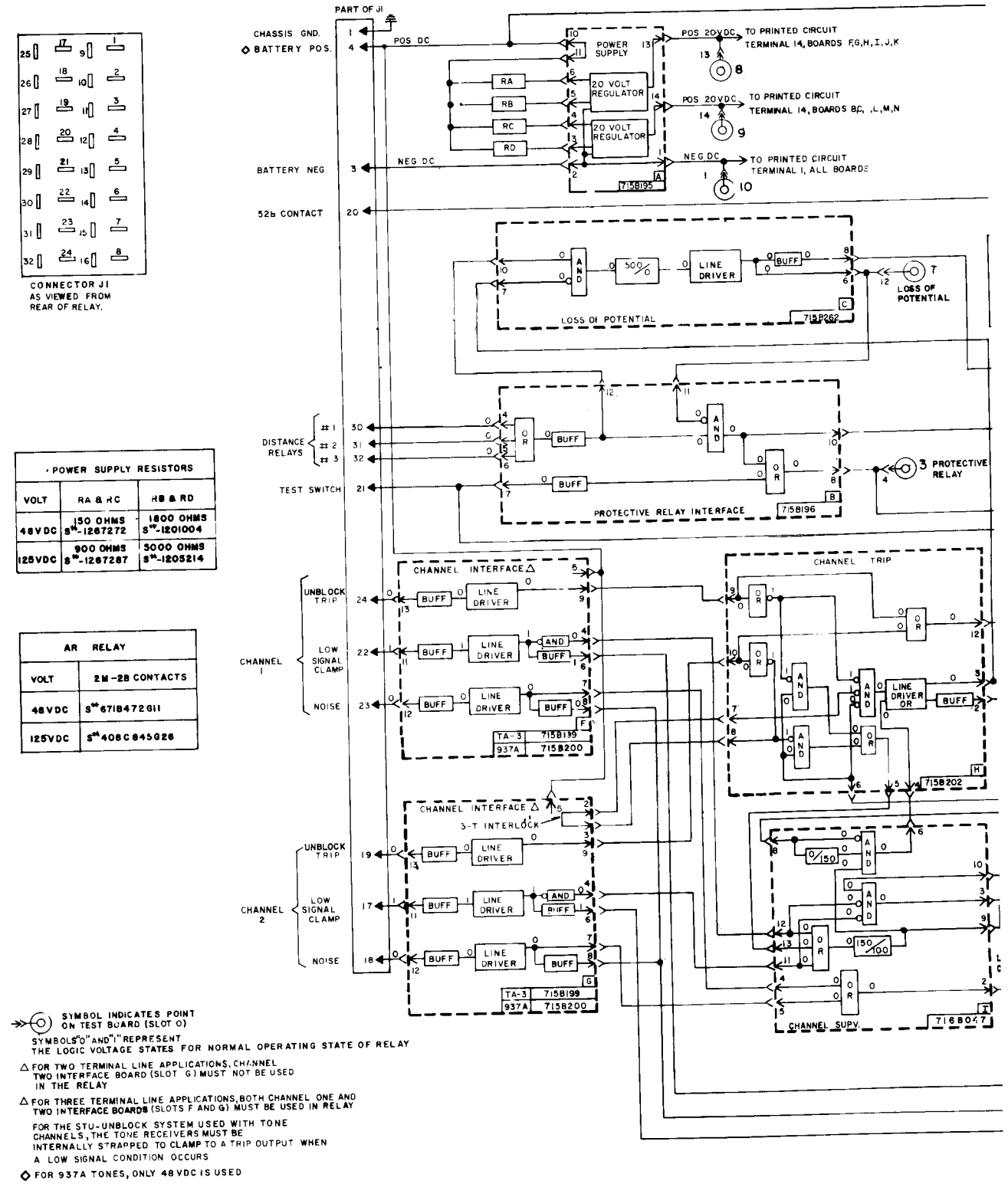
△ FOR TWO TERMINAL LINE APPLICATIONS, CHANNEL TWO INTERFACE BOARD (SLOT G) MUST NOT BE USED IN THE RELAY

△ FOR THREE TERMINAL LINE APPLICATIONS, BOTH CHANNEL ONE AND TWO INTERFACE BOARDS (SLOTS F AND G) MUST BE USED IN RELAY

*Fig. 5 STU logic - for use w*
*carrier channel.*




ith solid state distance relays and a TCF




| POWER SUPPLY RESISTORS | | |
|---|---|---|
| VOLT | RA & RC | RB & RD |
| 48VDC | 150 OHMS S[M]-1267272 | 1800 OHMS S[M]-1201004 |
| 125VDC | 900 OHMS S[M]-1267287 | 5000 OHMS S[M]-1205214 |

| AR RELAY | |
|---|---|
| VOLT | 2M-2B CONTACTS |
| 48VDC | S[M]67184726II |
| 125VDC | S[M]408C845G26 |

SYMBOL INDICATES POINT ON TEST BOARD (SLOT O)

SYMBOLS "0" AND "1" REPRESENT THE LOGIC VOLTAGE STATES FOR NORMAL OPERATING STATE OF RELAY

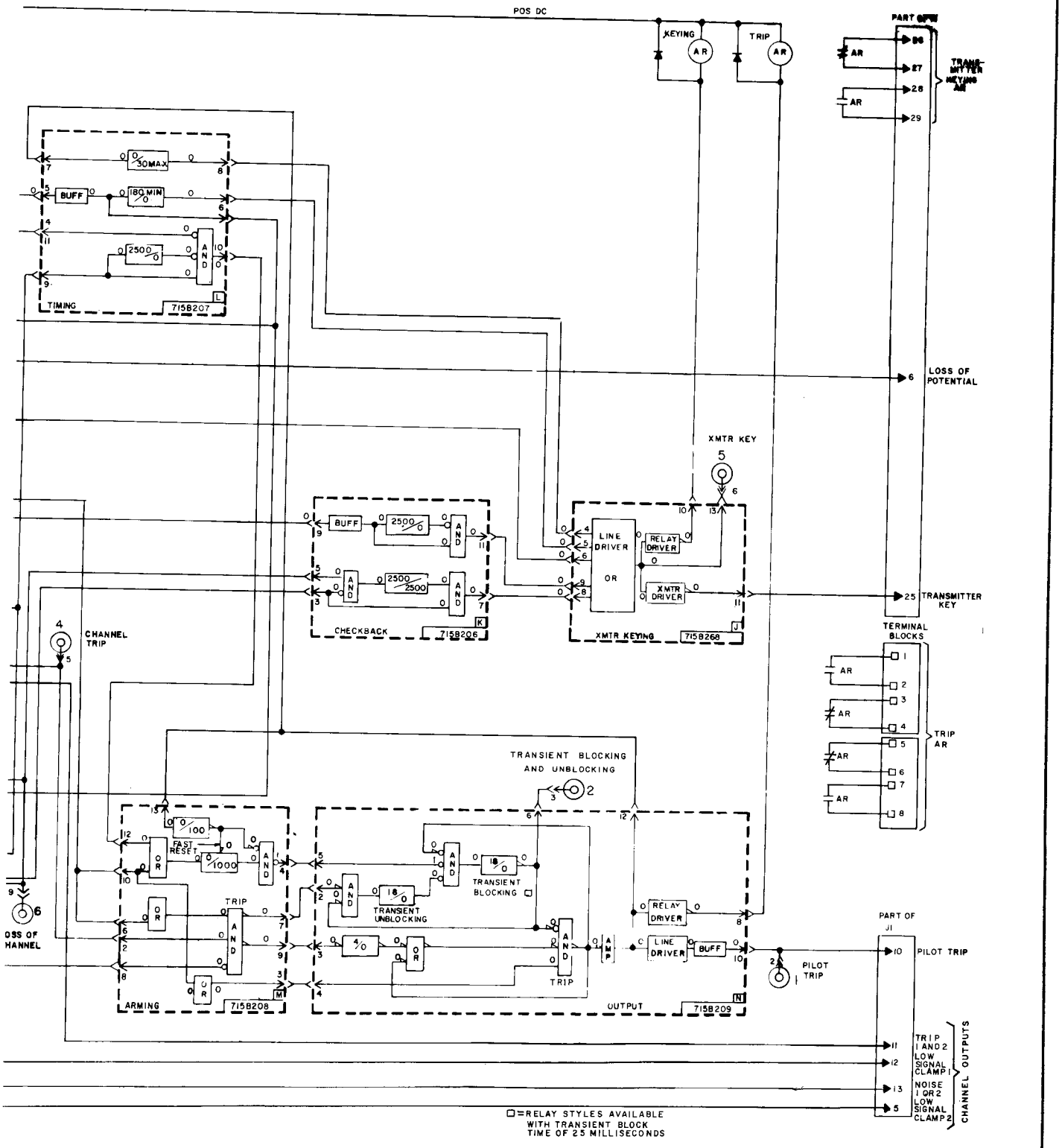
△ FOR TWO TERMINAL LINE APPLICATIONS, CHANNEL TWO INTERFACE BOARD (SLOT G) MUST NOT BE USED IN THE RELAY

△ FOR THREE TERMINAL LINE APPLICATIONS, BOTH CHANNEL ONE AND TWO INTERFACE BOARDS (SLOTS F AND G) MUST BE USED IN RELAY

FOR THE STU-UNBLOCK SYSTEM USED WITH TONE CHANNELS, THE TONE RECEIVERS MUST BE INTERNALLY STRAPPED TO CLAMP TO A TRIP OUTPUT WHEN A LOW SIGNAL CONDITION OCCURS

◇ FOR 937A TONES, ONLY 48 VDC IS USED

*Fig. 7 STU logic - for use with solid*




state distance relays and a tone channel.

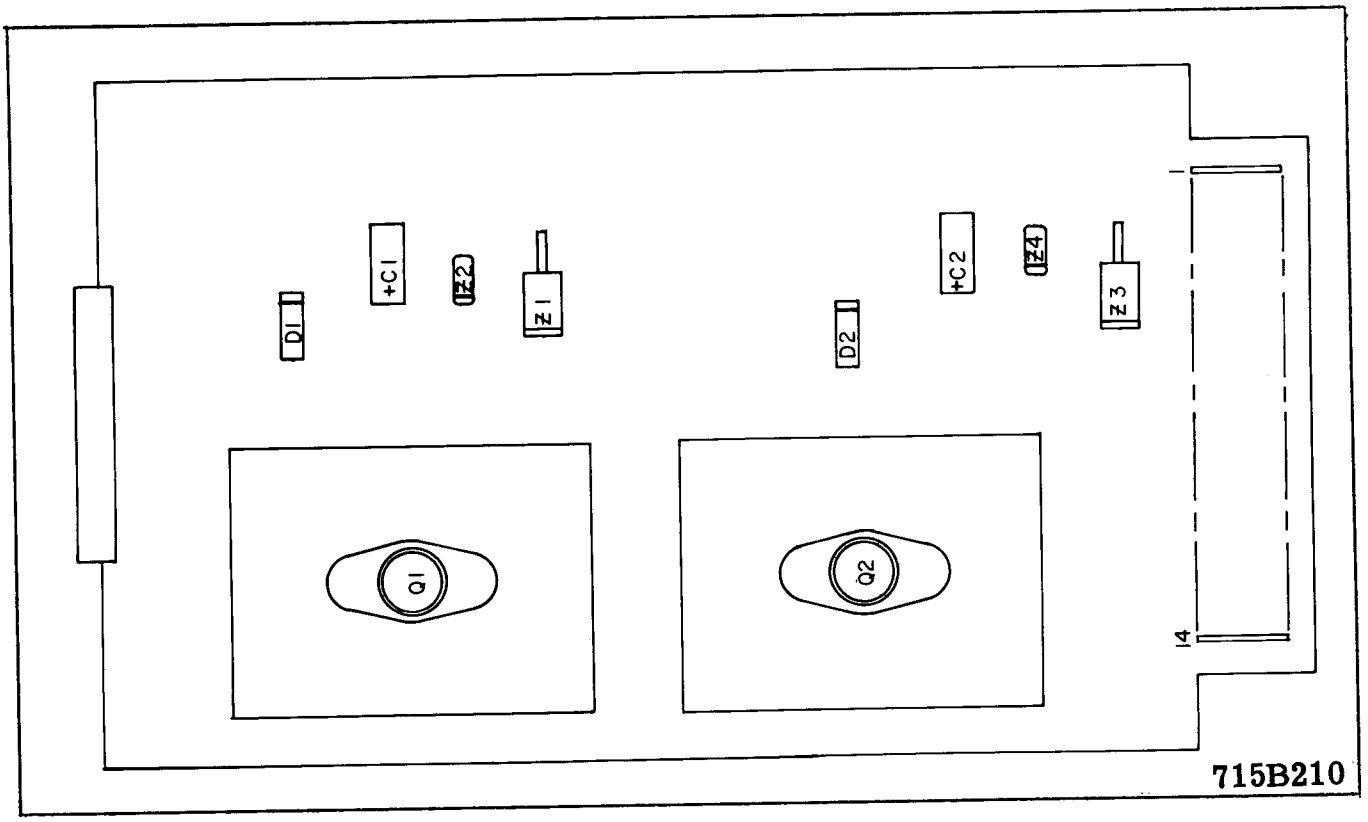



Fig. 8 Component location power supply board.

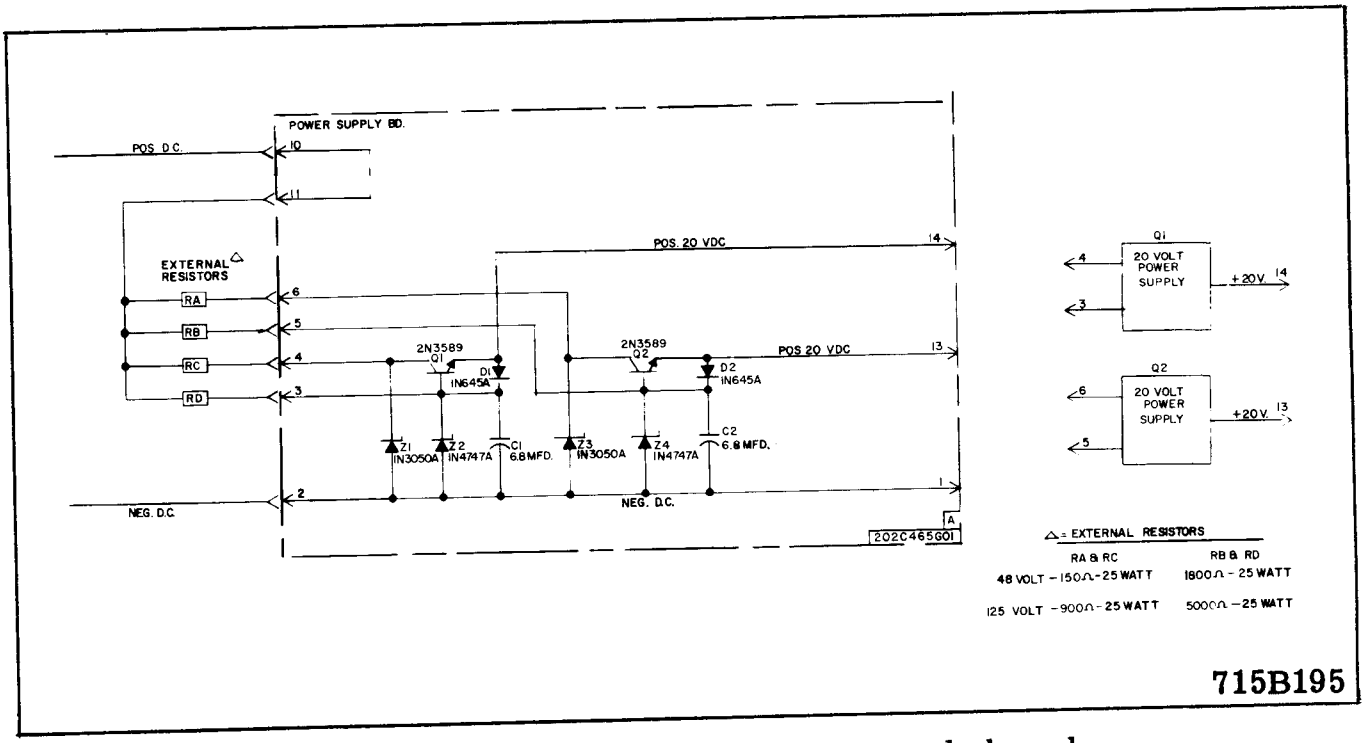



Fig. 9 Internal schematic power supply board

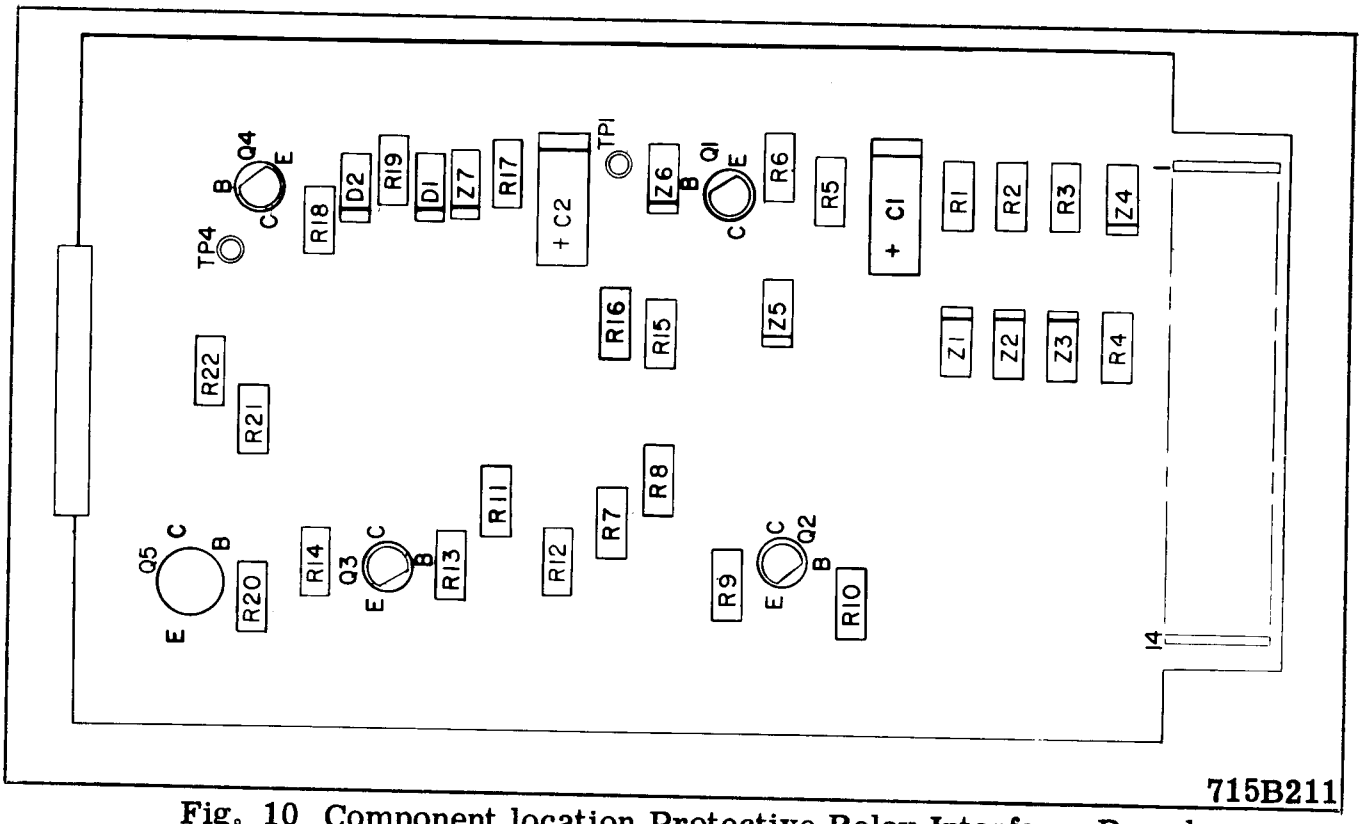



Fig. 10 Component location Protective Relay Interface Board.

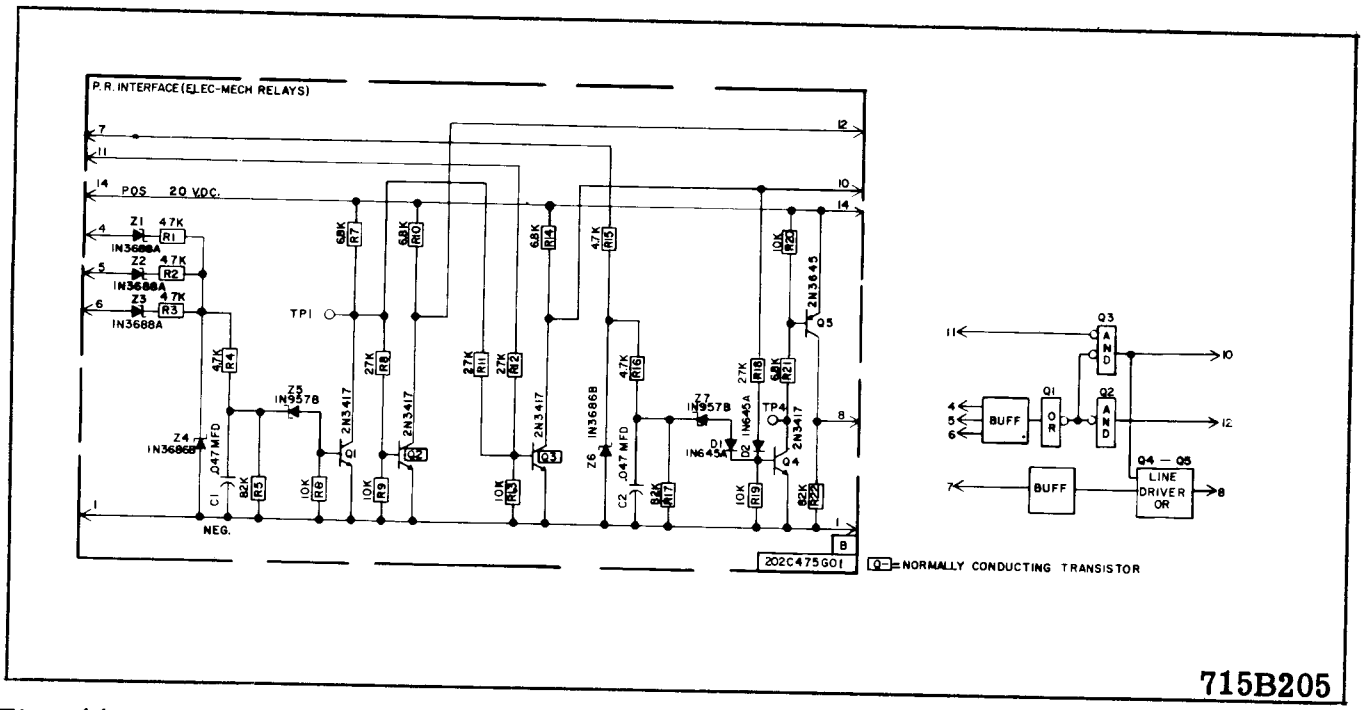



Fig. 11 Internal Schematic Protective Relay Interface Board for Elec-Mech System.

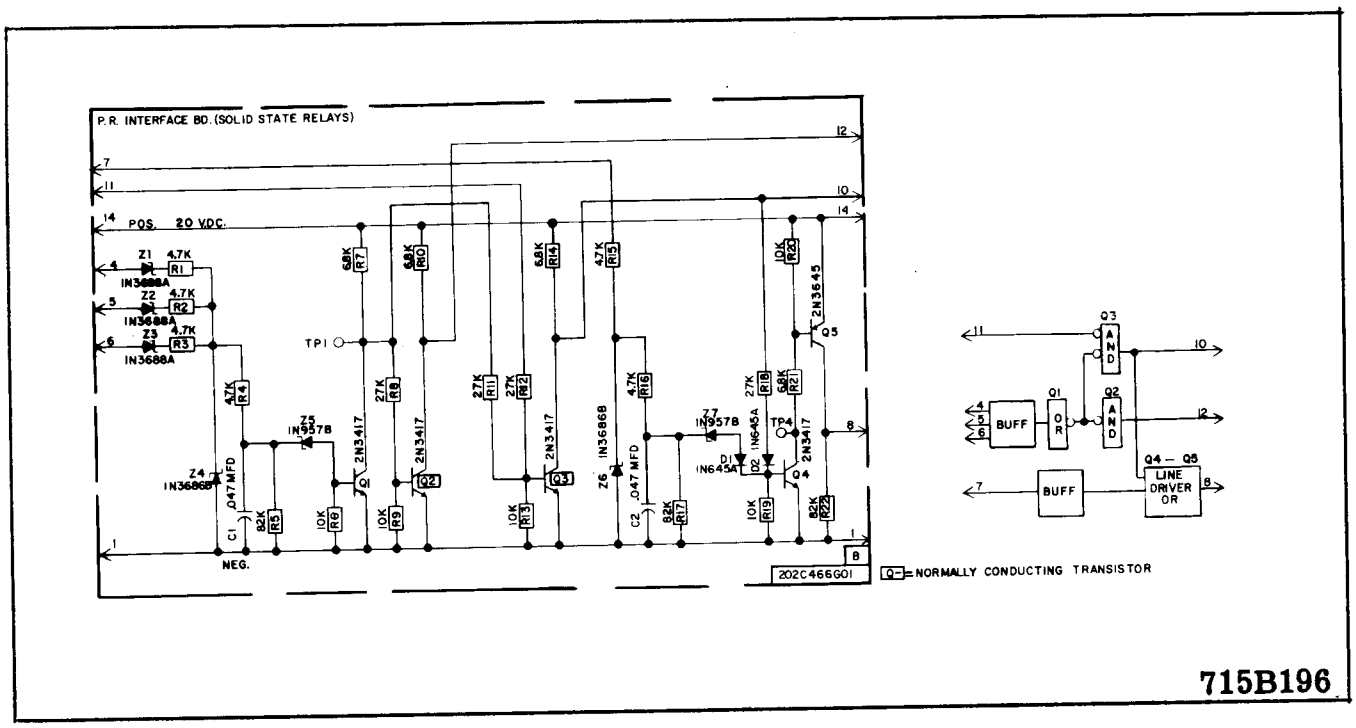



Fig. 12 Internal Schematic Protective Relay Interface Board for solid state System.

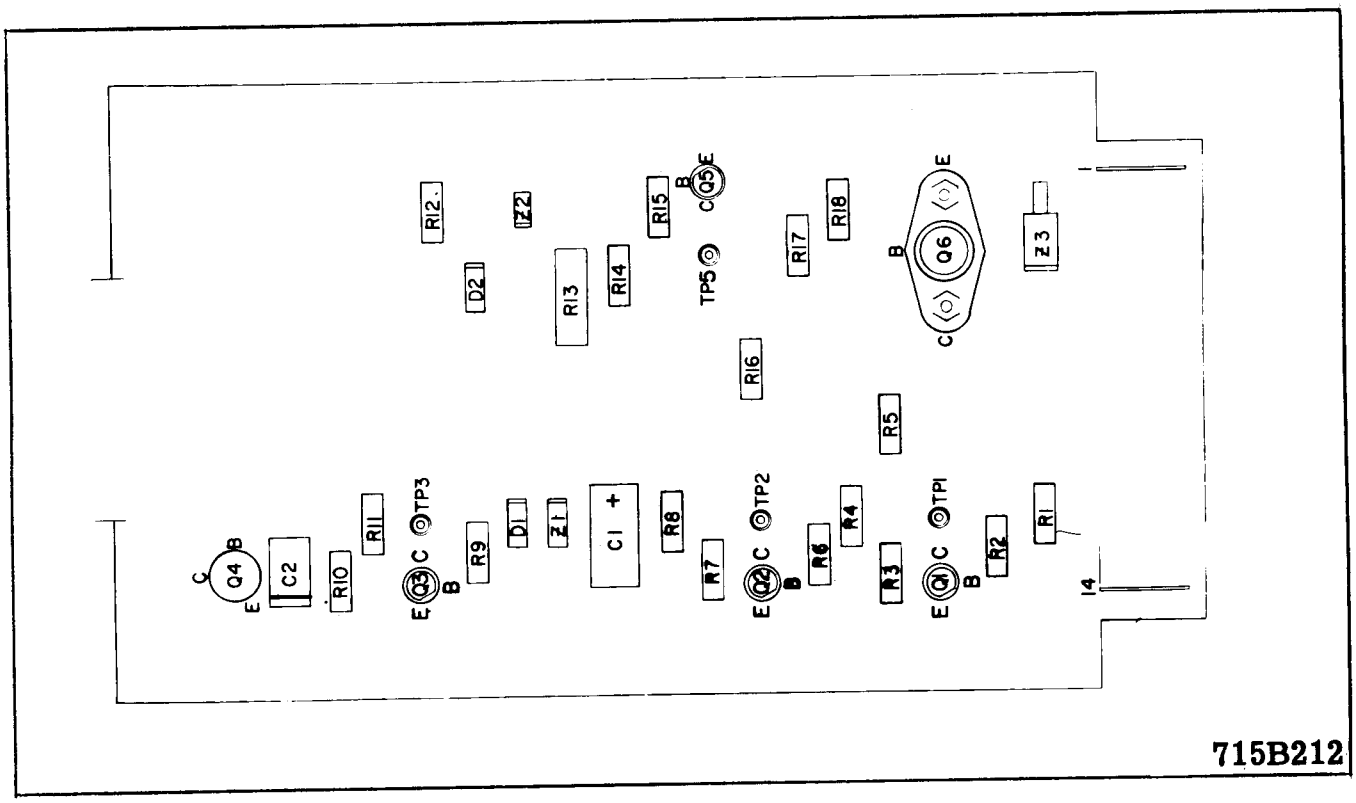



Fig. 13 Component Location Loss of Potential Board.

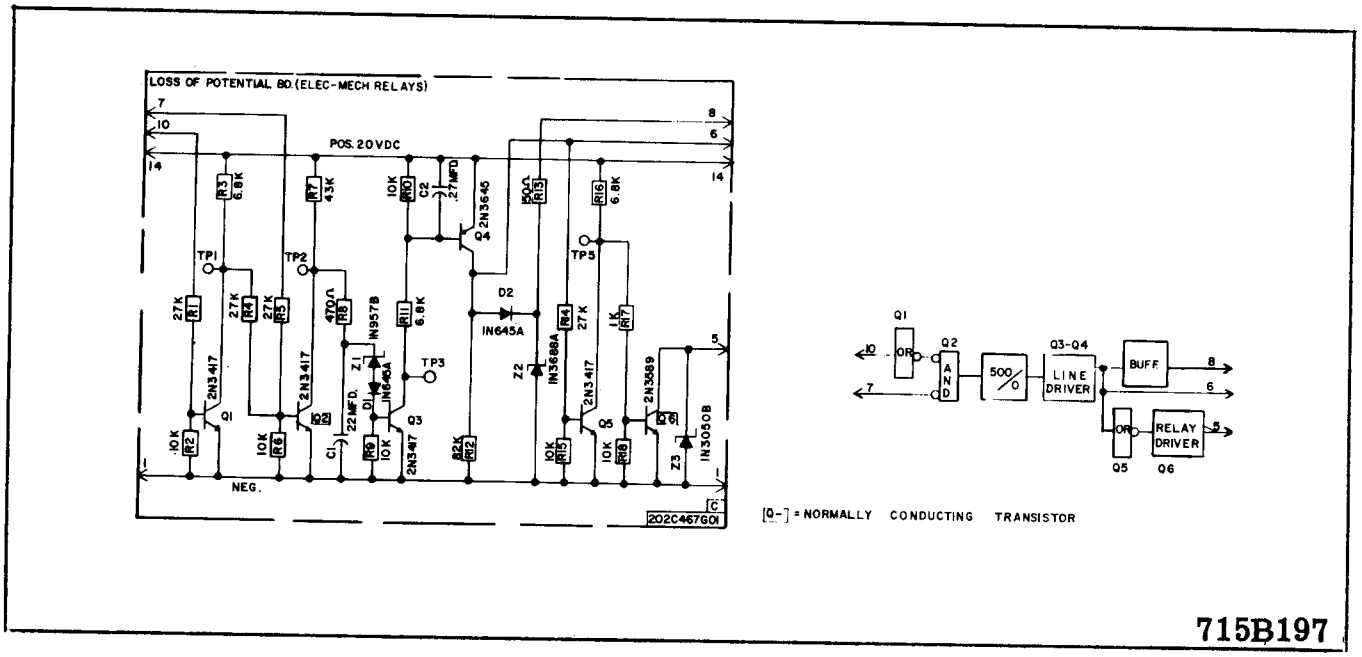



Fig. 14 Internal Schematic Loss of Potential Board for Elec-Mech Systems.

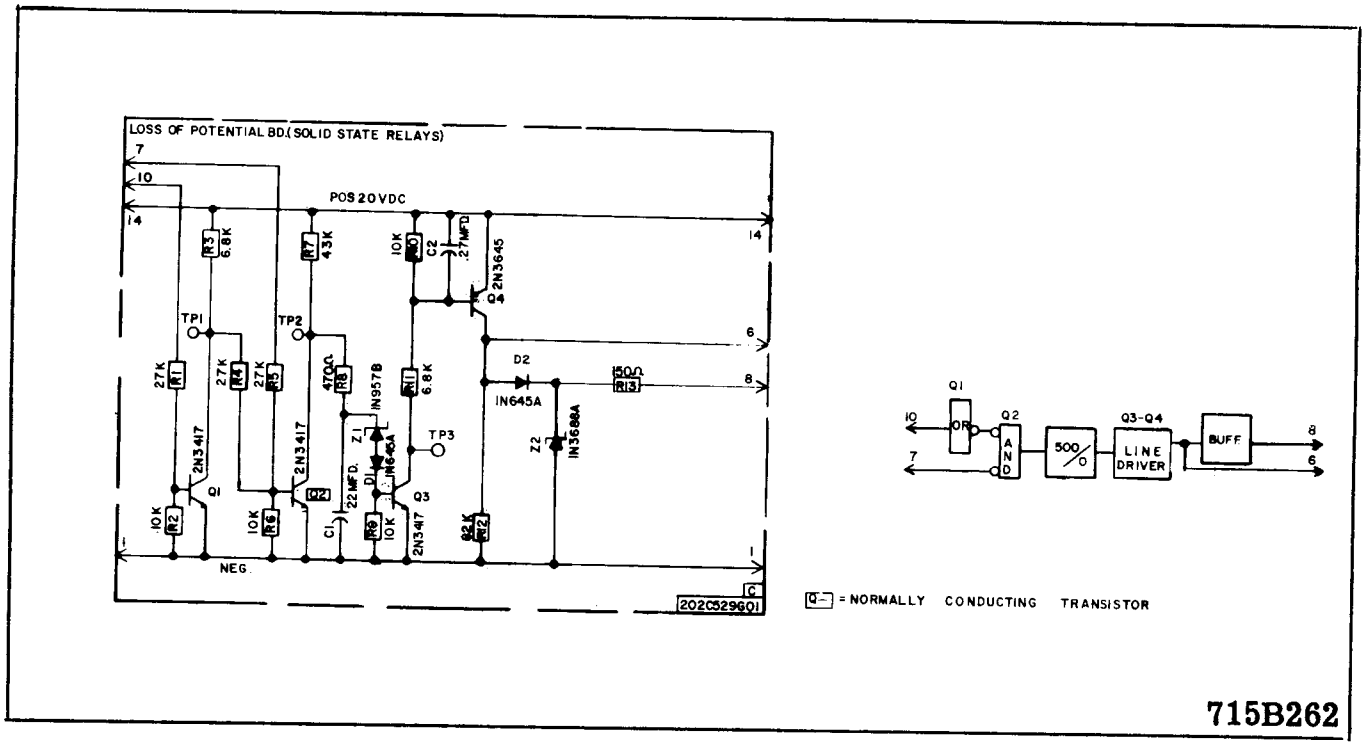



Fig. 15 Internal Schematic Loss of Potential Board for solid state system.

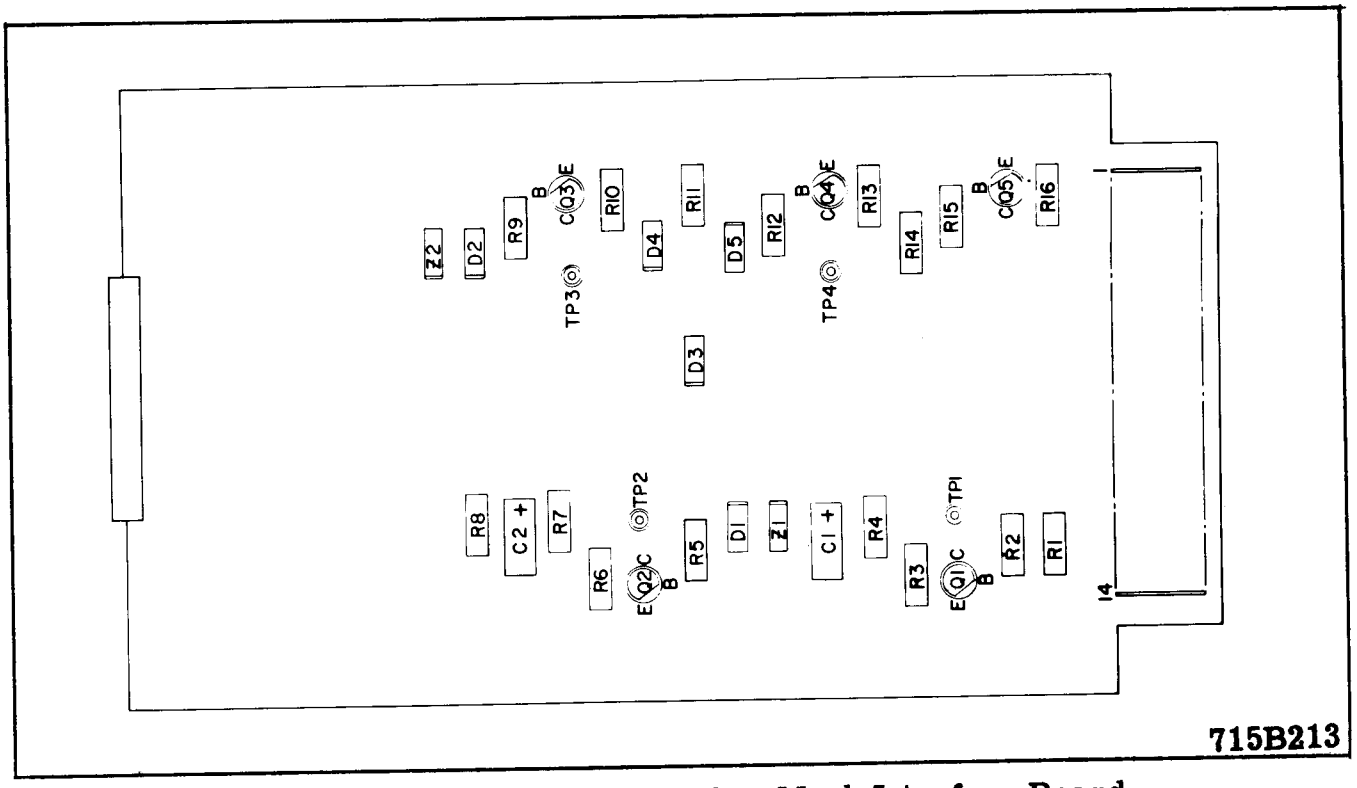



Fig. 16 Component Location Elec-Mech Interface Board.

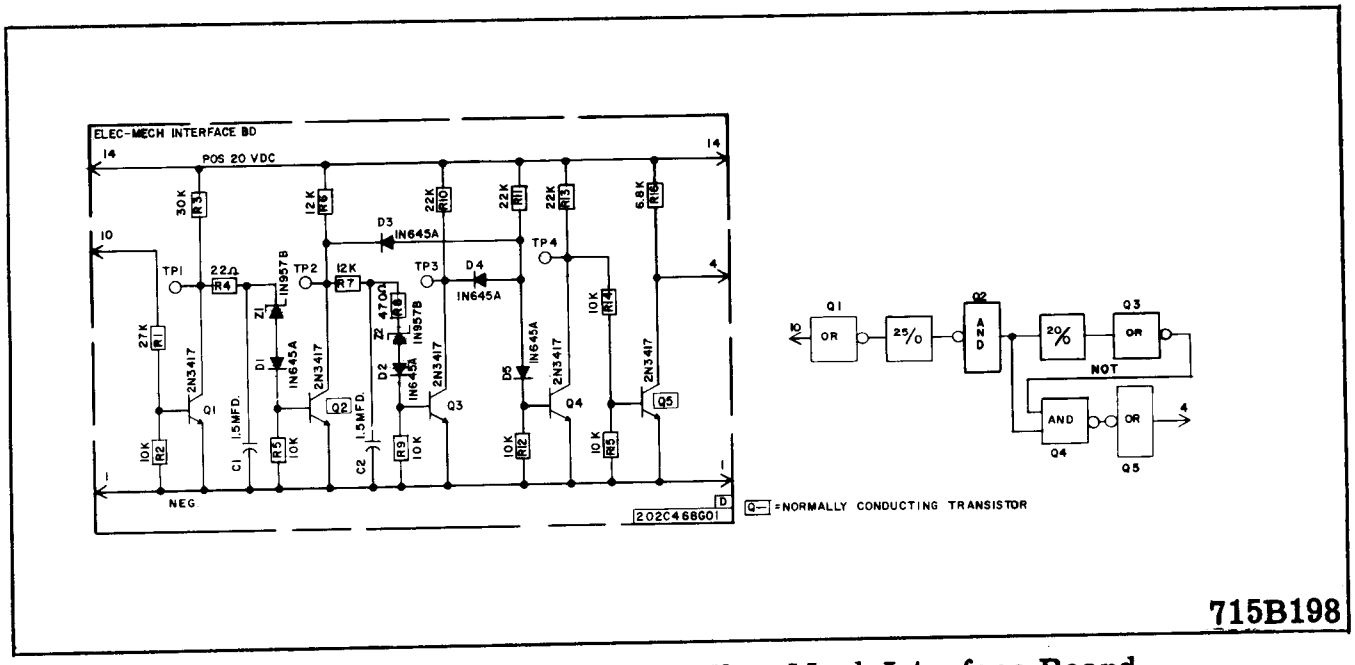



Fig. 17 Internal Schematic Elec-Mech Interface Board.

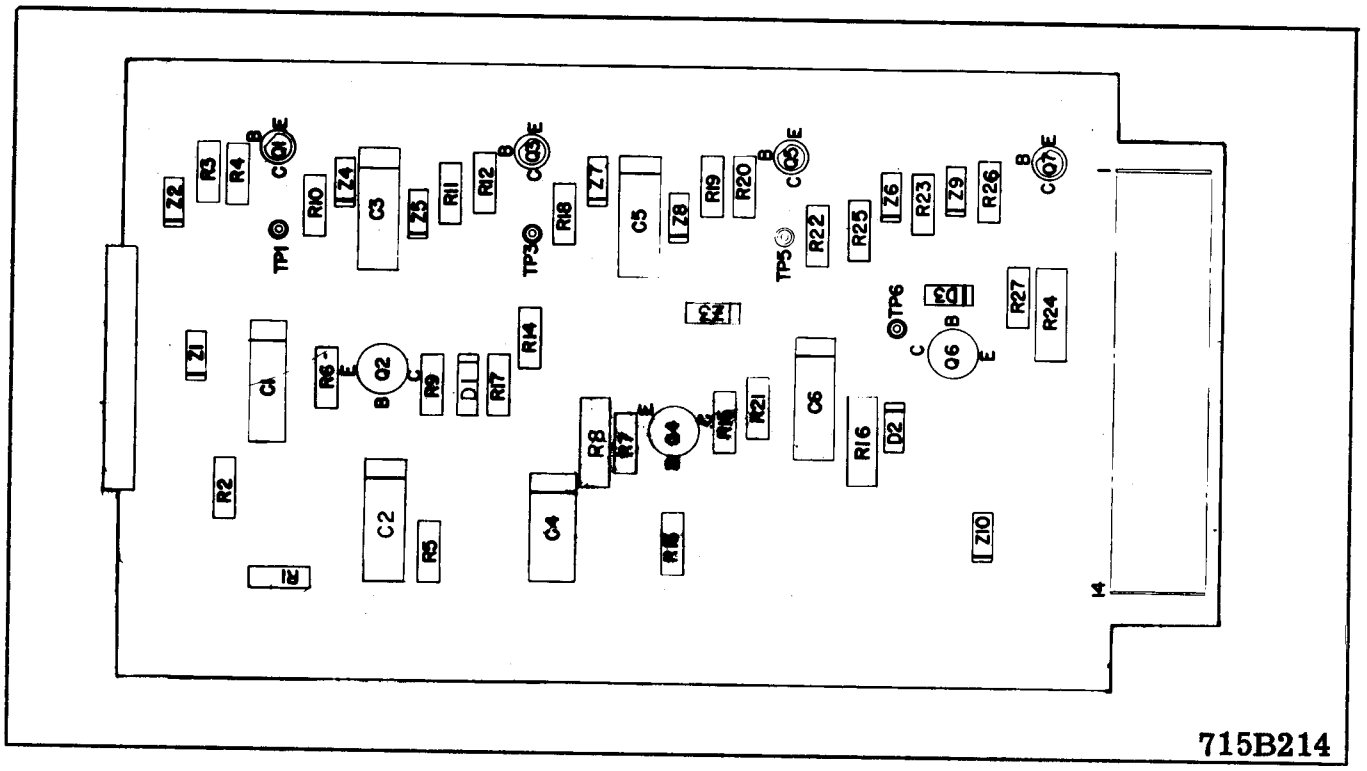



Fig. 18 Component Location Channel Interface Board

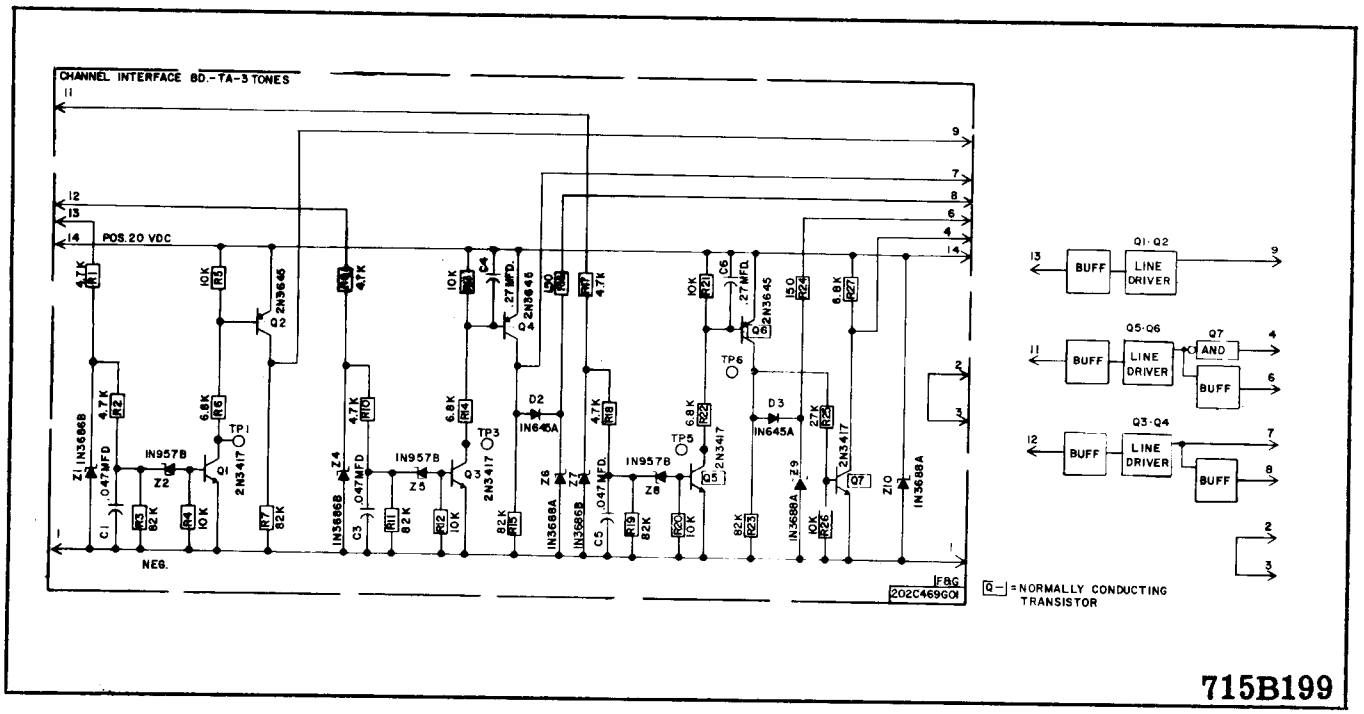



Fig. 19 Internal Schematic Channel Interface Board for TA-3 Tone.

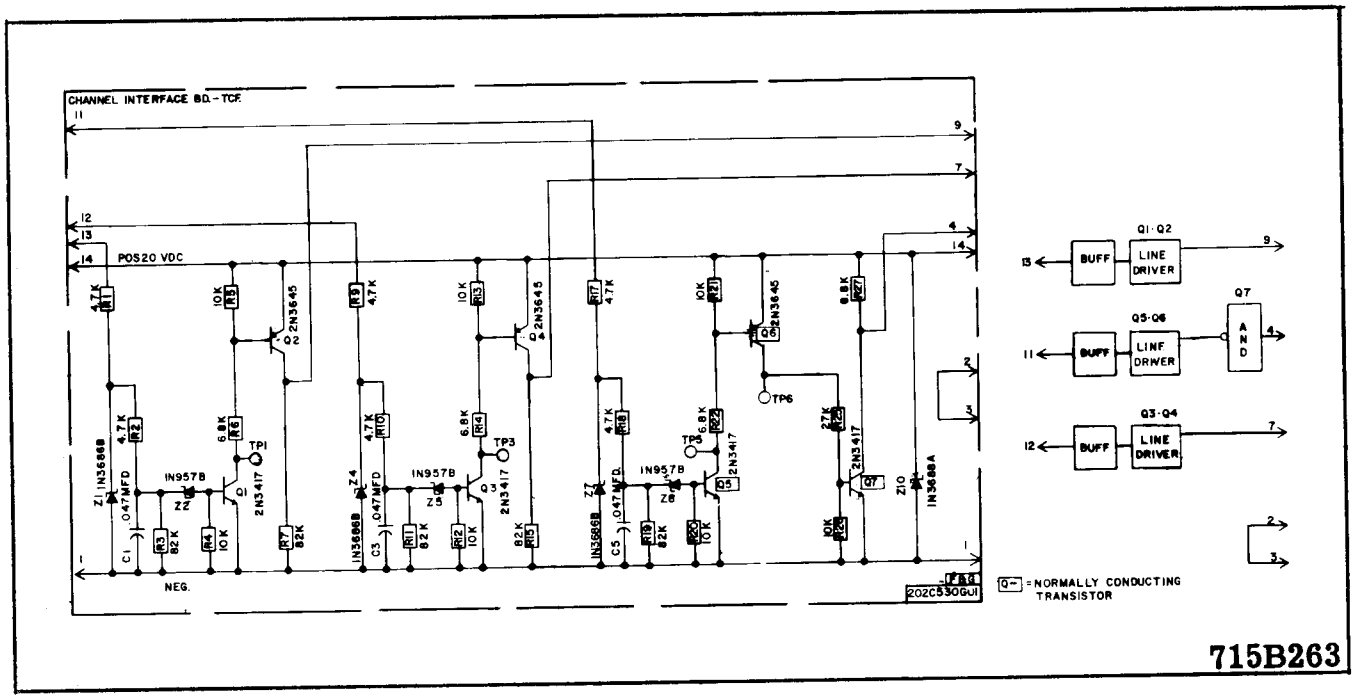



Fig. 20 Internal Schematic Channel Interface Board for TCF Carrier.

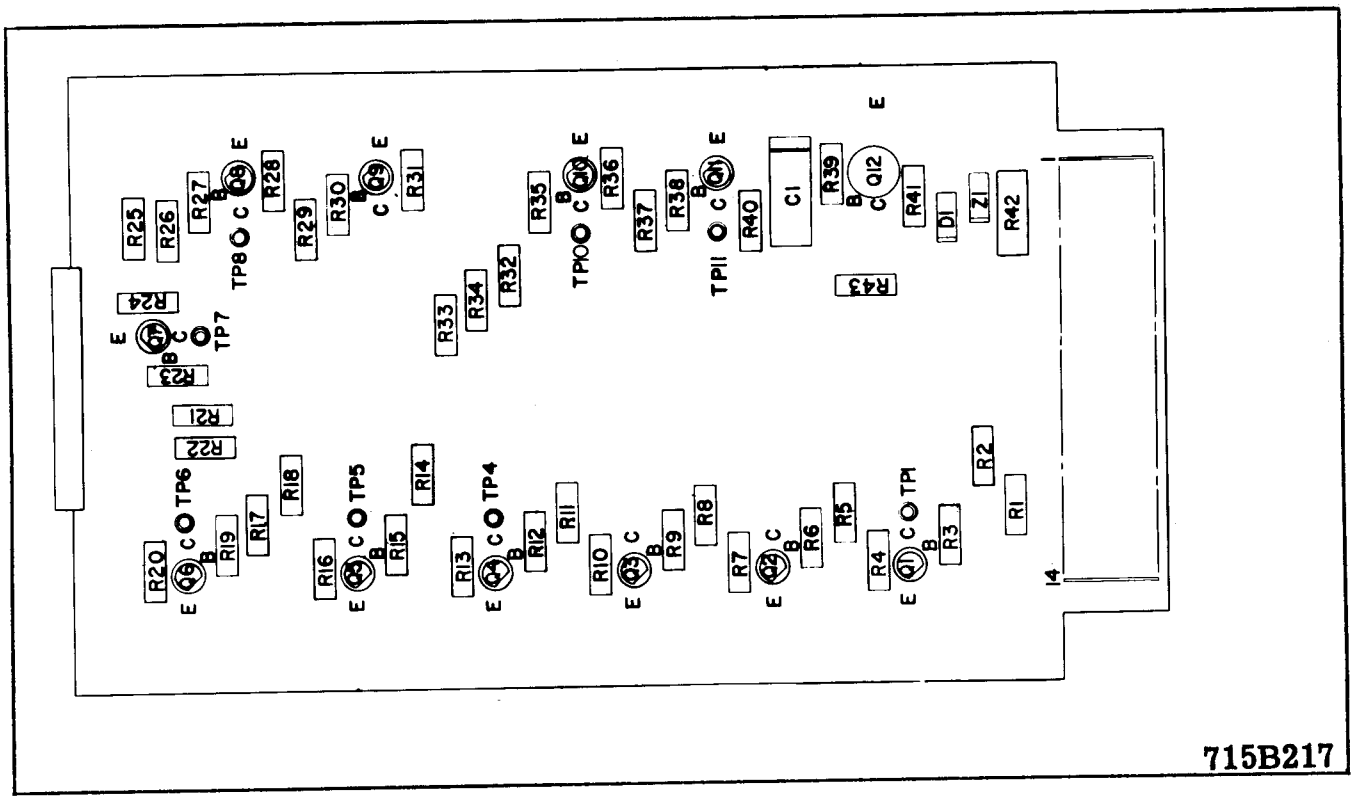



Fig. 21 Component Location Channel Trip Board.

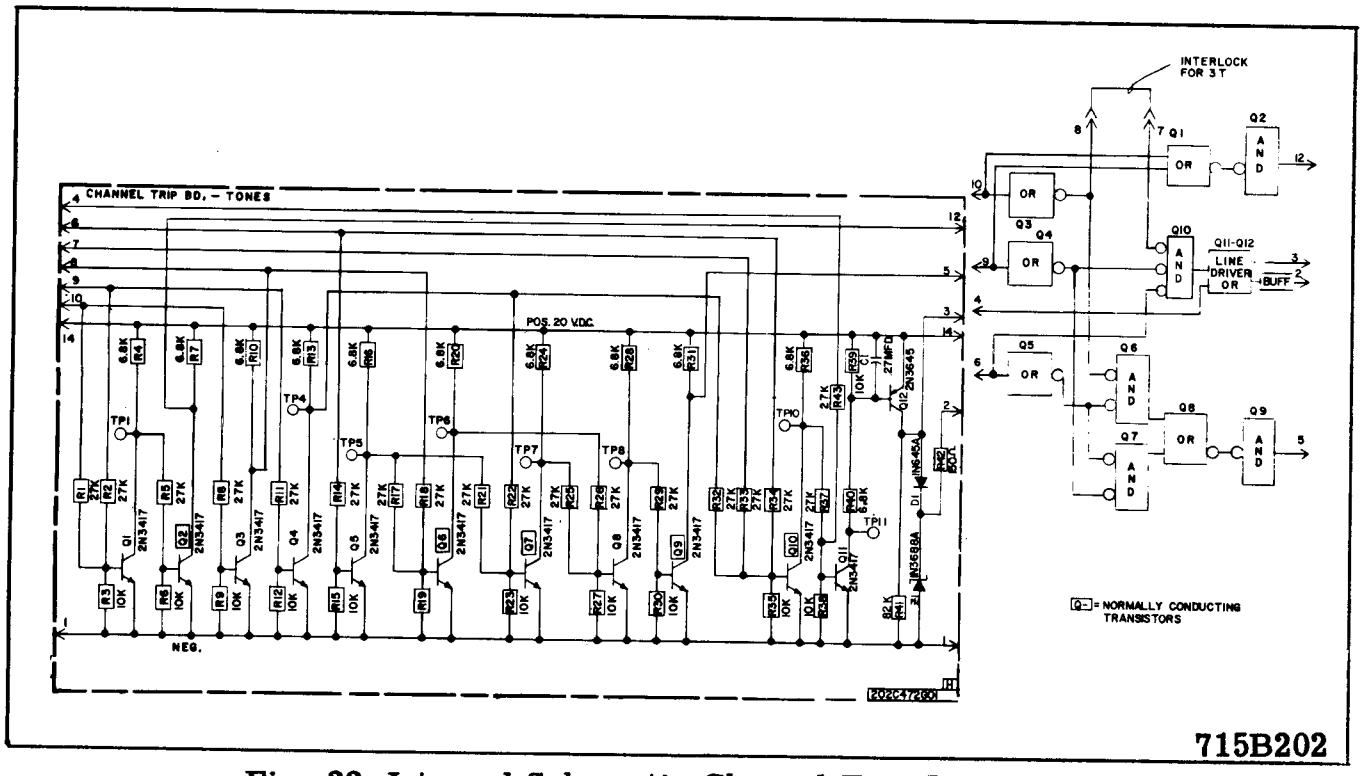



Fig. 22 Internal Schematic Channel Trip Board for Tones.

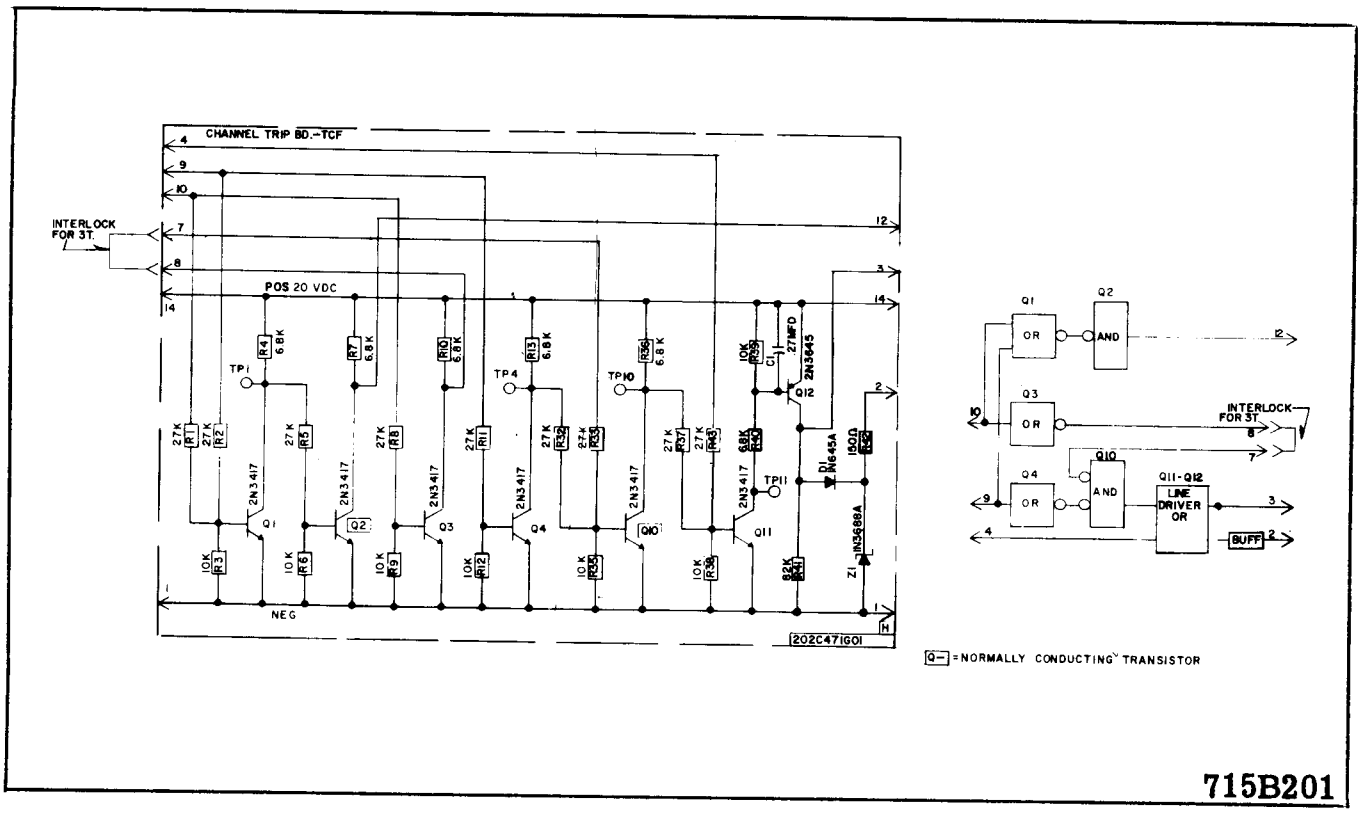



Fig. 23 Internal Schematic Channel Trip Board for TCF.

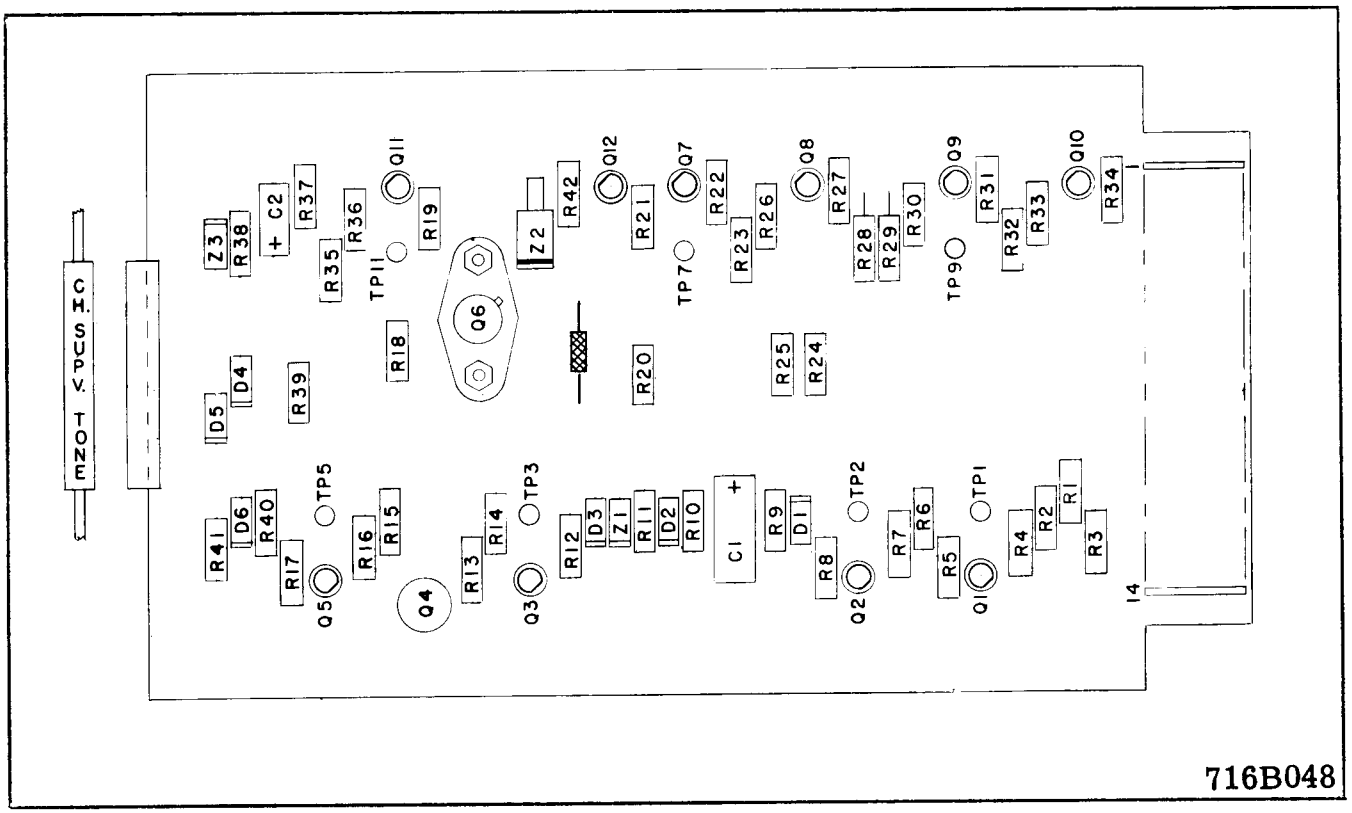



Fig. 24 Component Location Channel Supervision Board tone Channel.

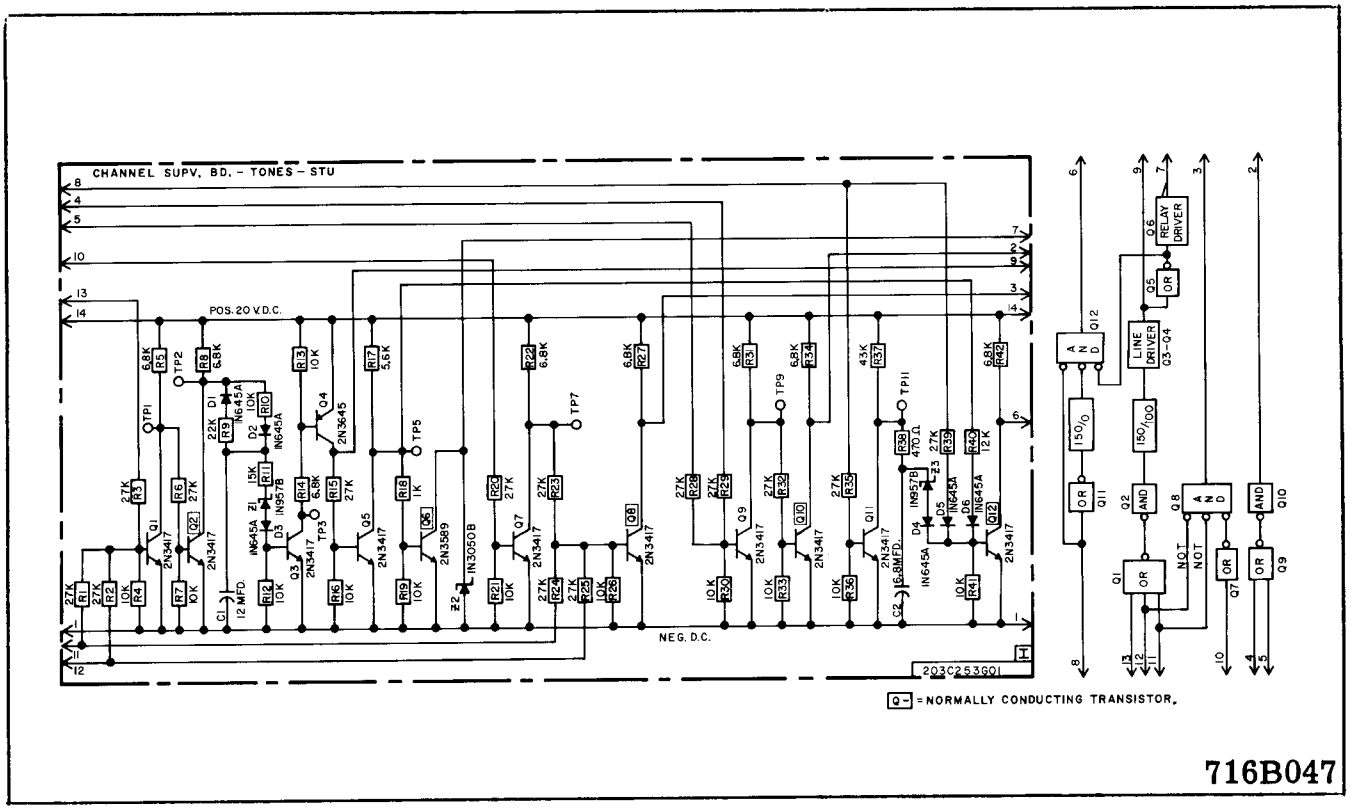



Fig. 25 Internal Schematic Channel Supv. Board for Tone Channel.

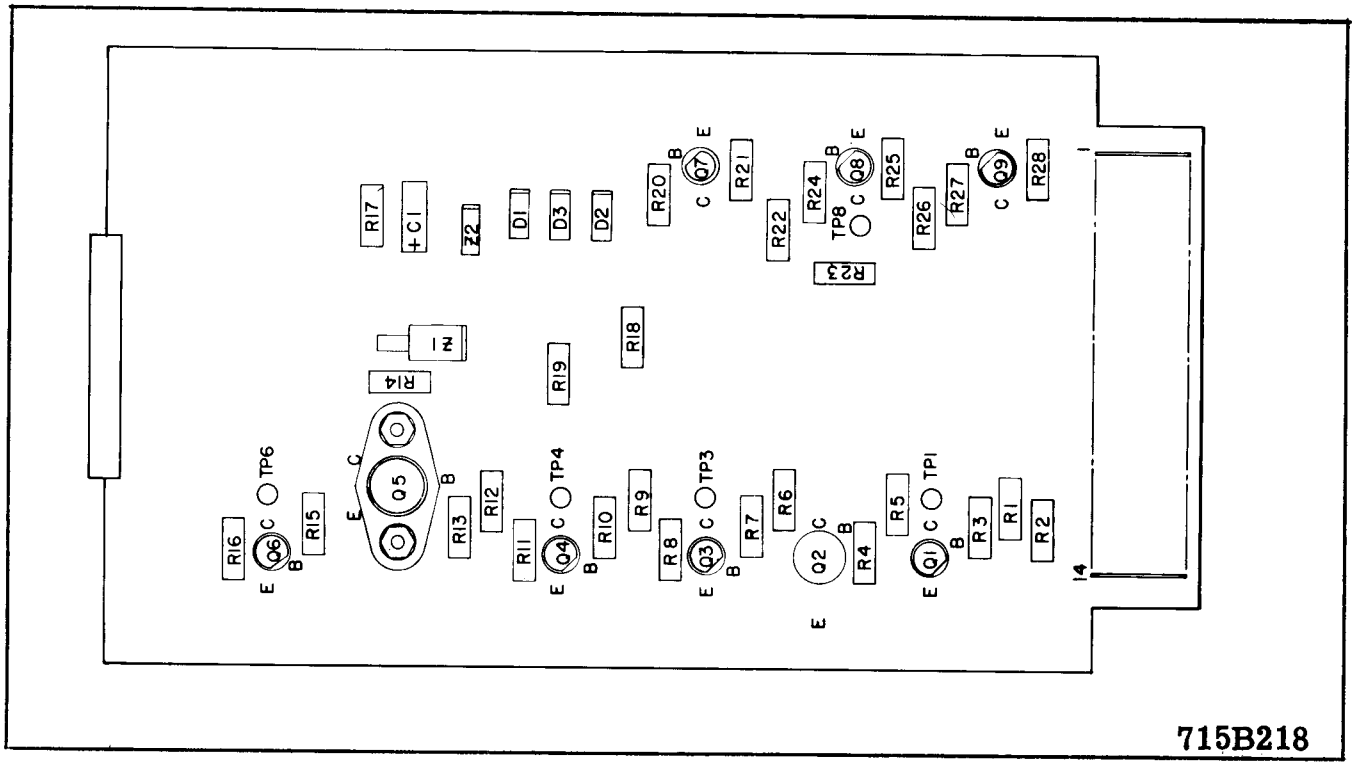



Fig. 26 Component Location Channel Supervision Board - TCF Channel.

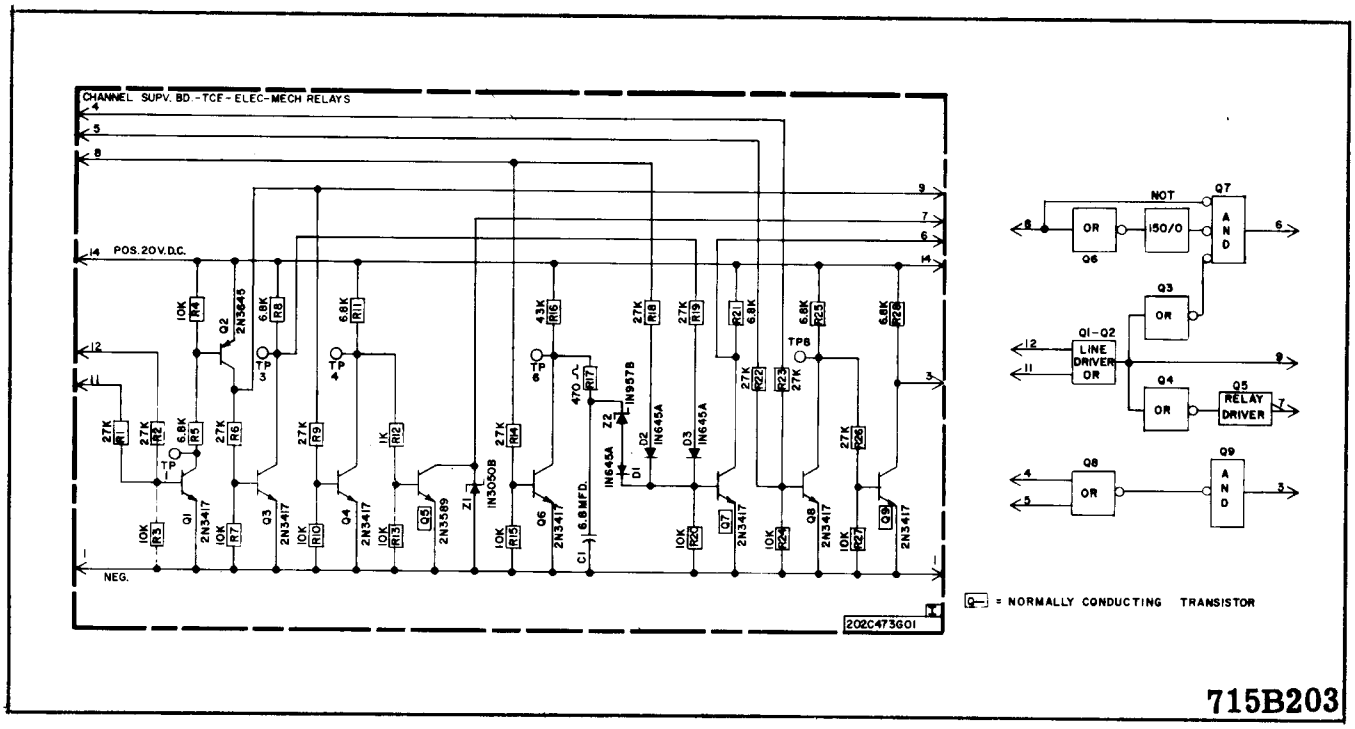



Fig. 27 Internal Schematic Channel Supervision Board for TCF Channel and Elec-Mech System.

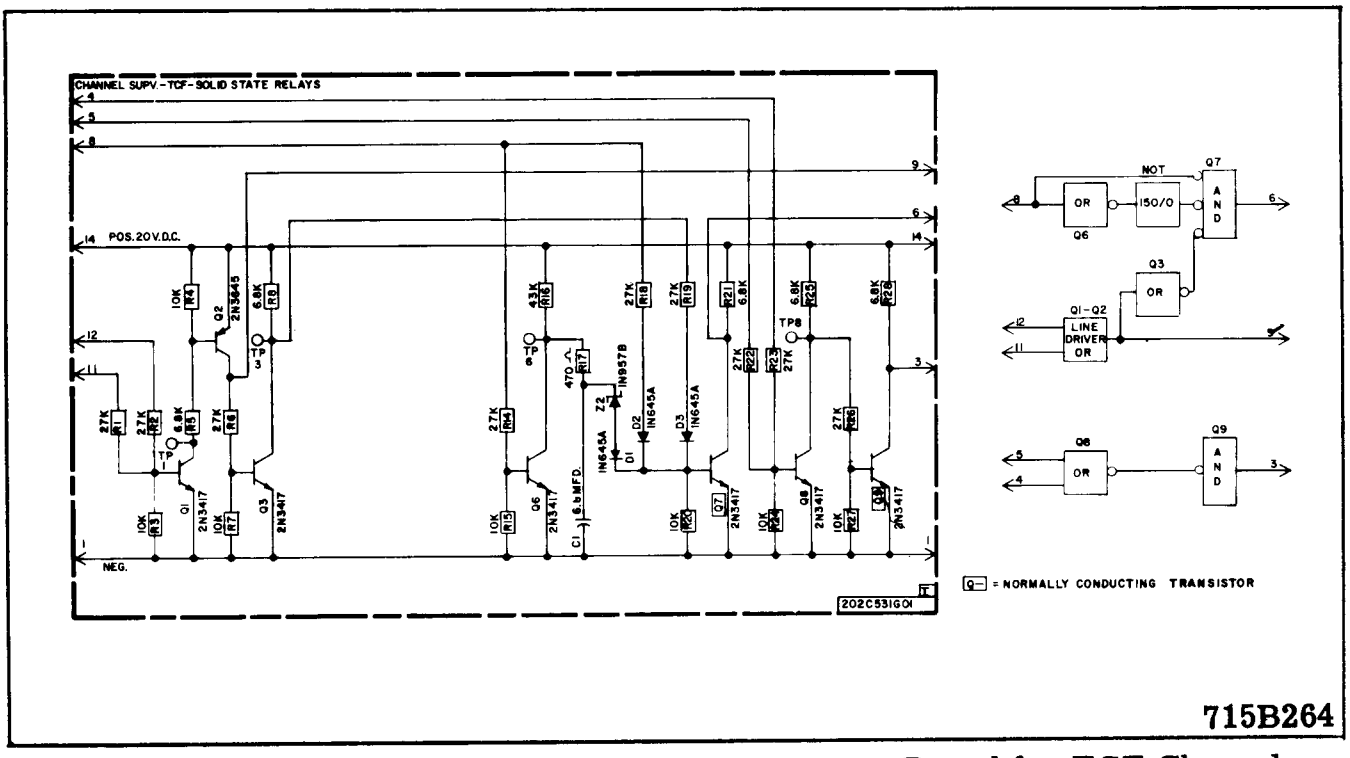



Fig. 28 Internal Schematic Channel Supervision Board for TCF Channel and Solid State System.

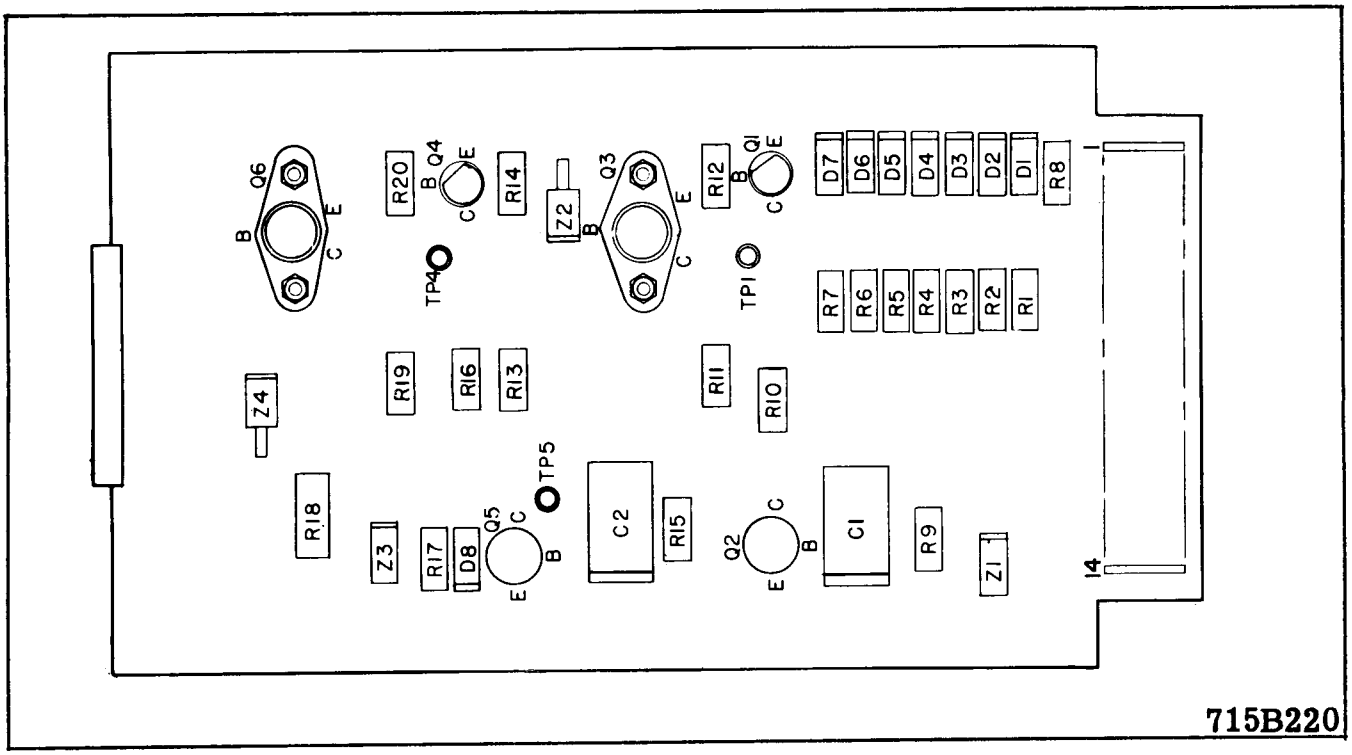



Fig. 29 Component Location Transmitter Key Board.

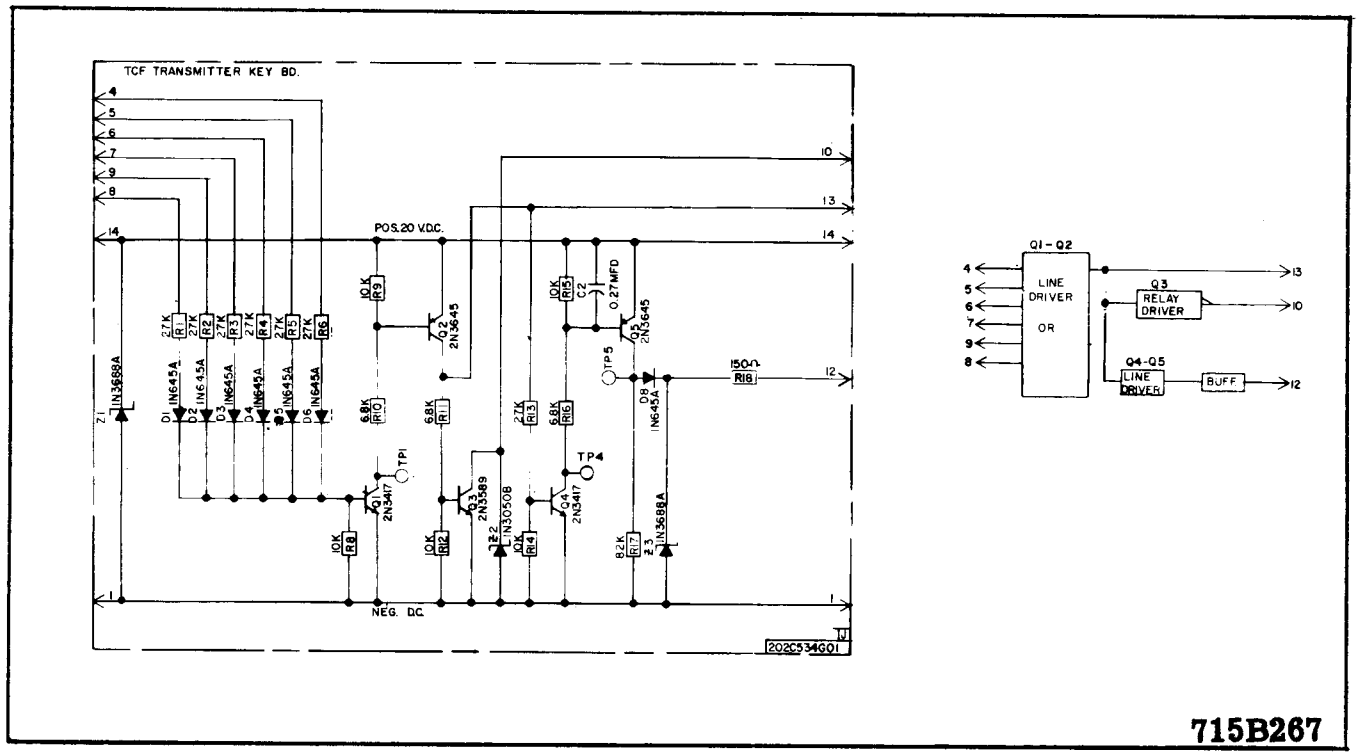



Fig. 30 Internal Schematic Transmitter Key Board for TCF Channel.

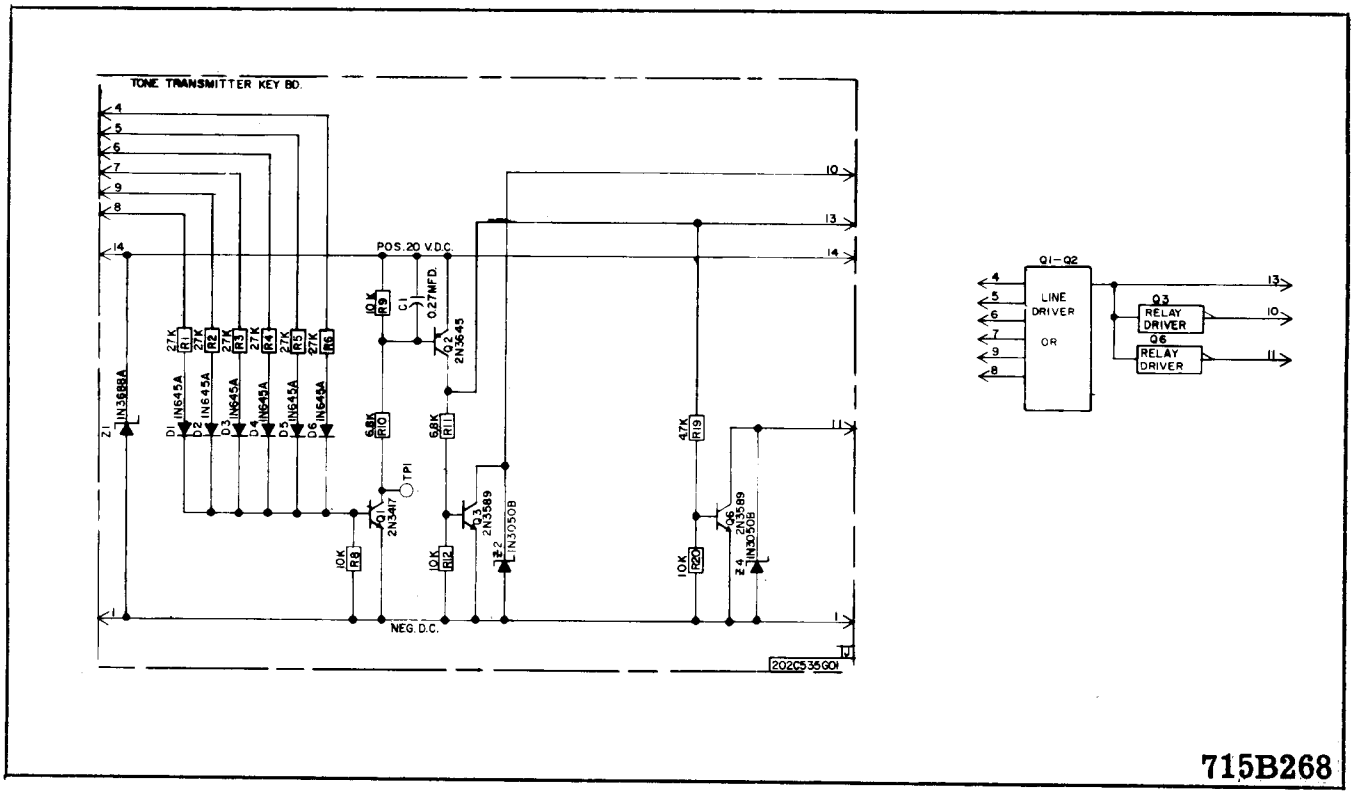



Fig. 31 Internal Schematic Transmitter Key Board for Tone Channel.

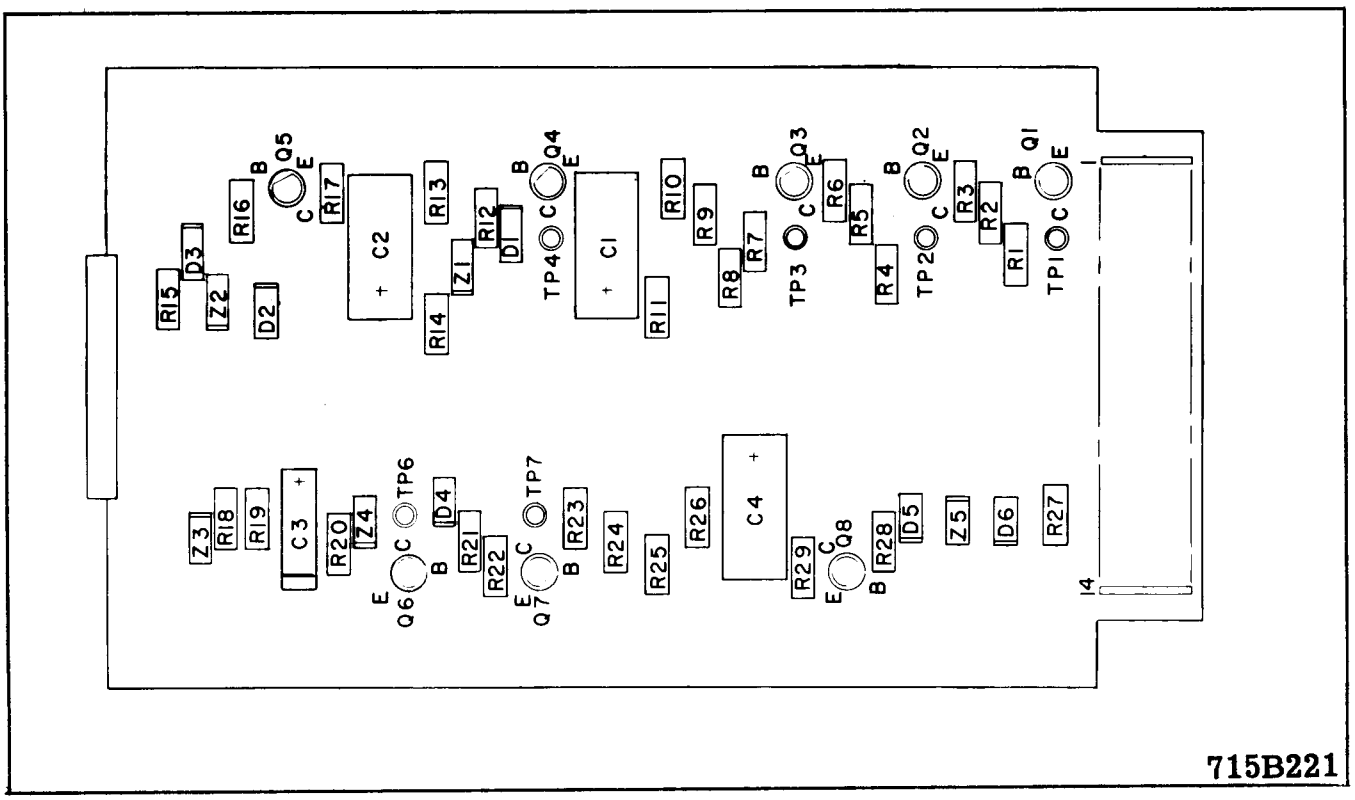



Fig. 32 Component Location Checkback Board.

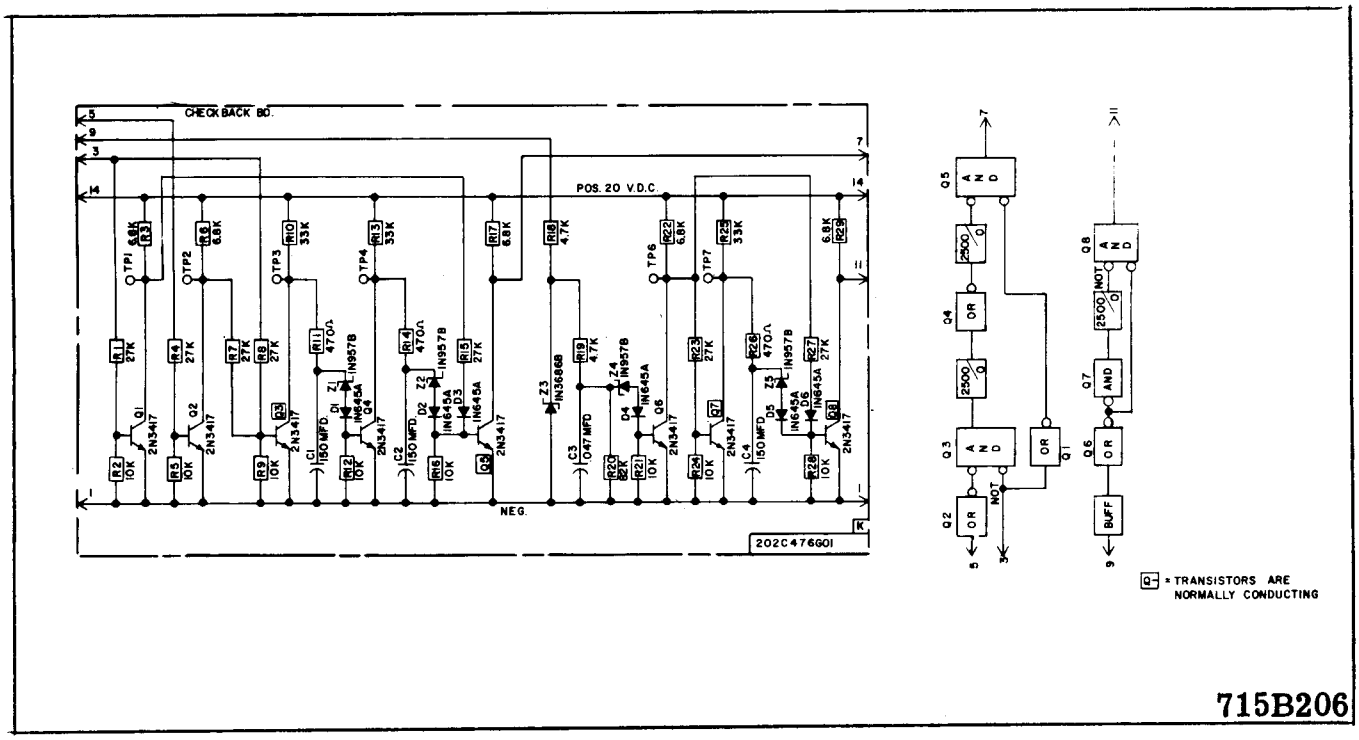



Fig. 33 Internal Schematic Checkback Board.

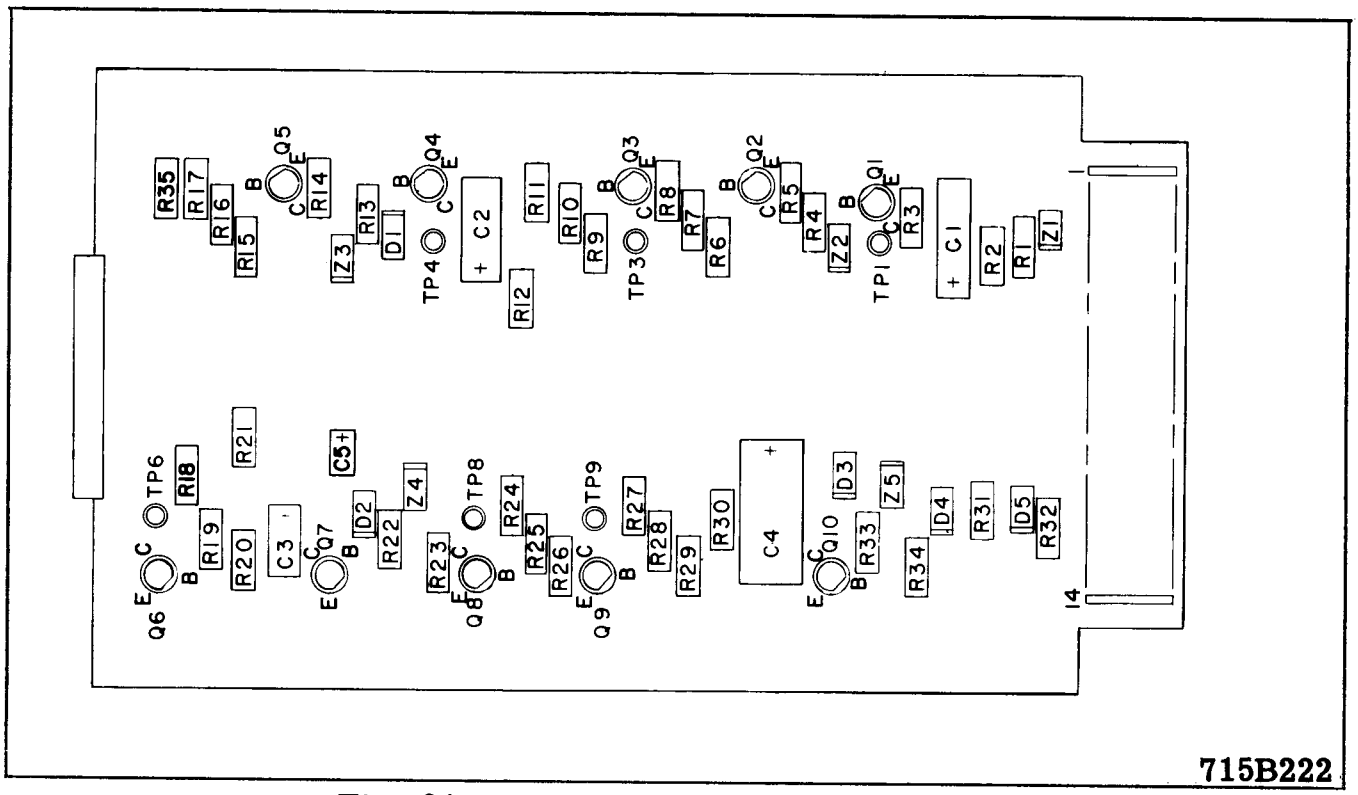



Fig. 34 Component Location Timing Board.

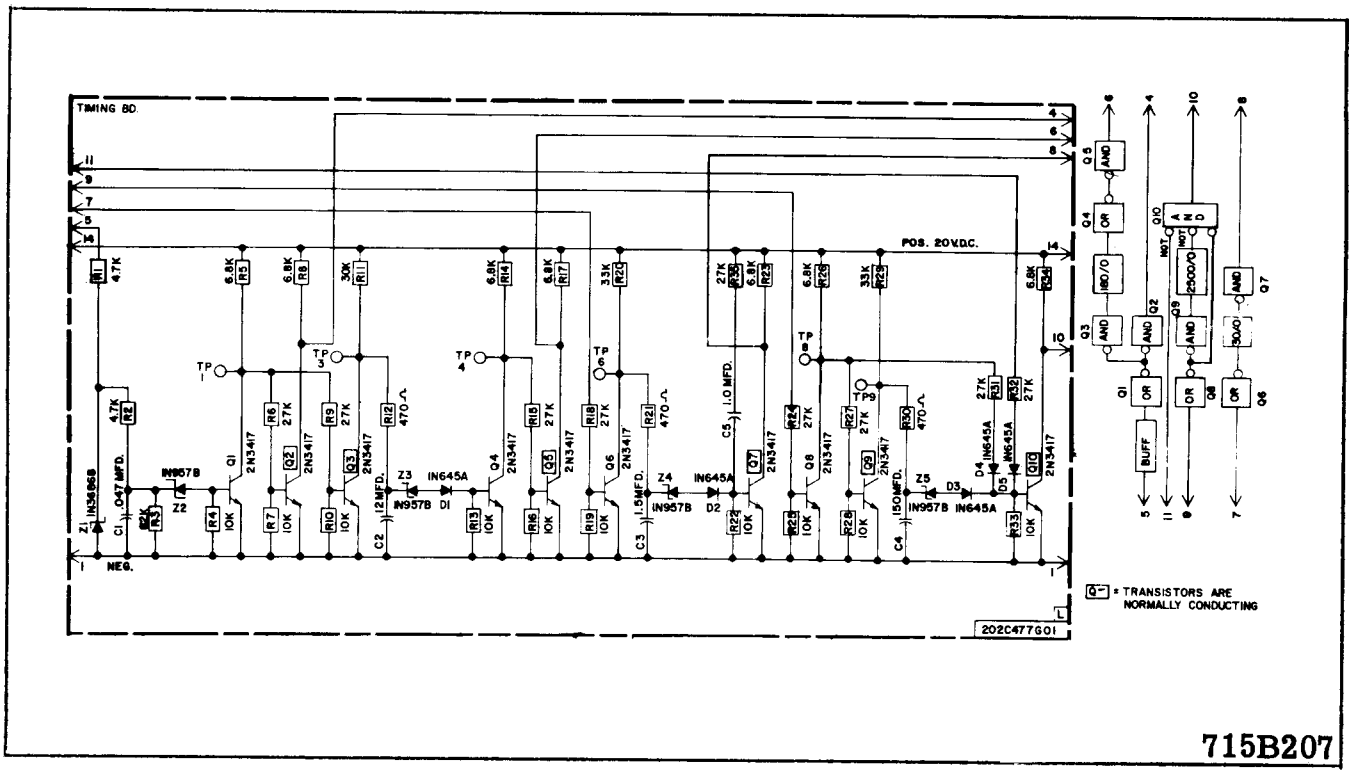



Fig. 35 Internal Schematic Timing Board.

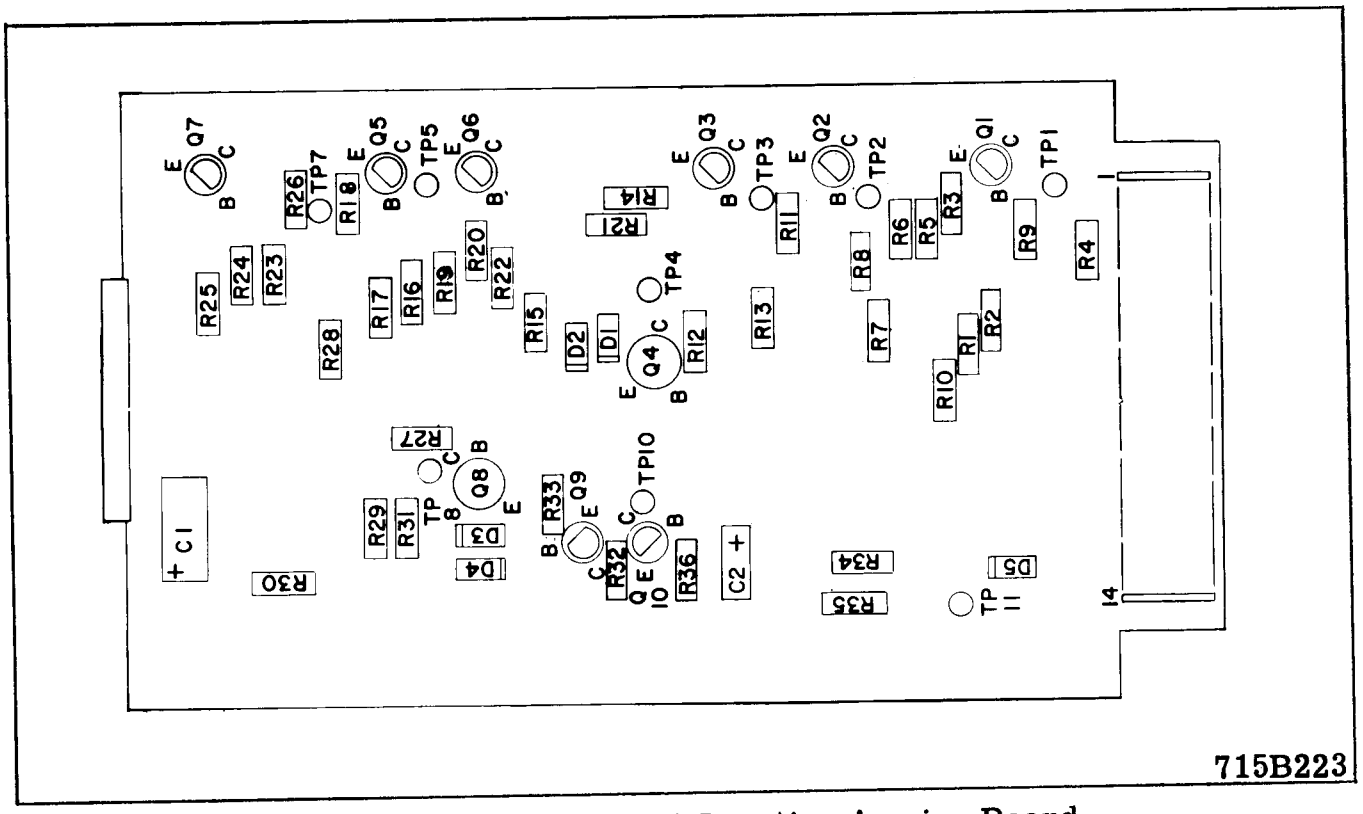



Fig. 36 Component Location Arming Board.

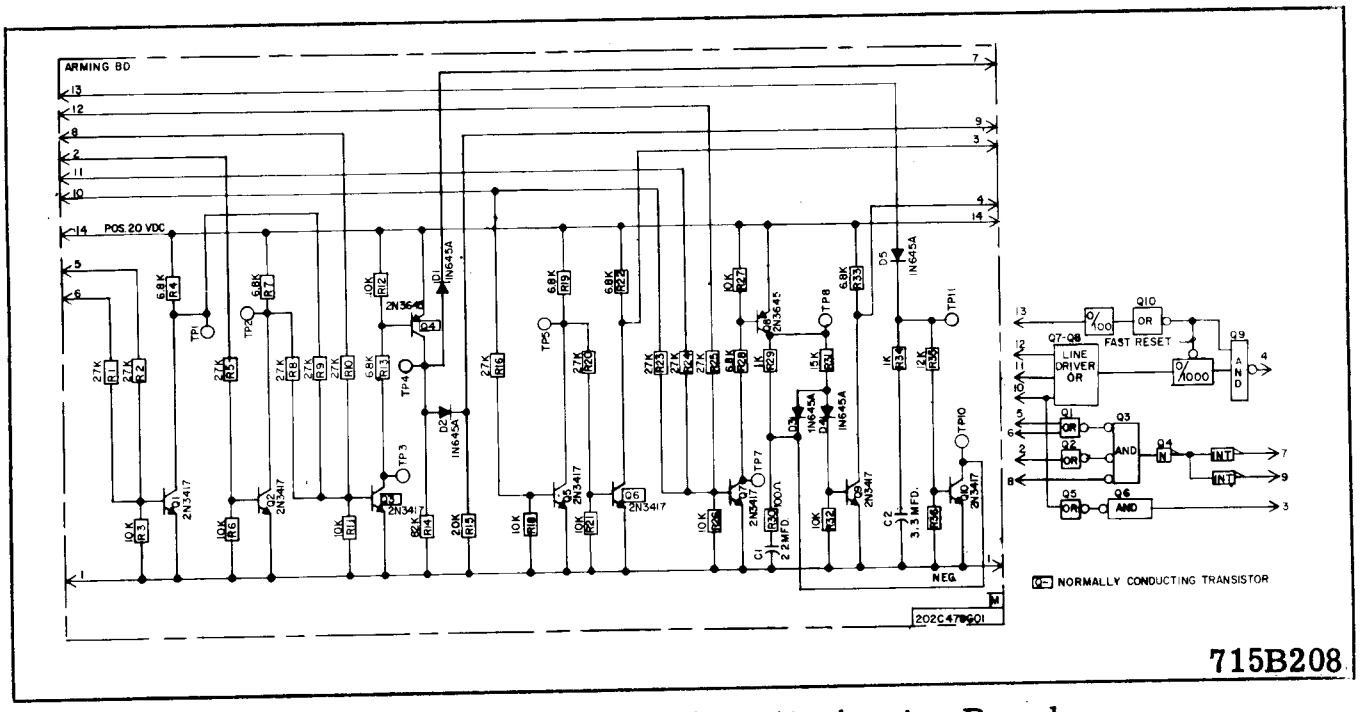



Fig. 37 Internal Schematic Arming Board.

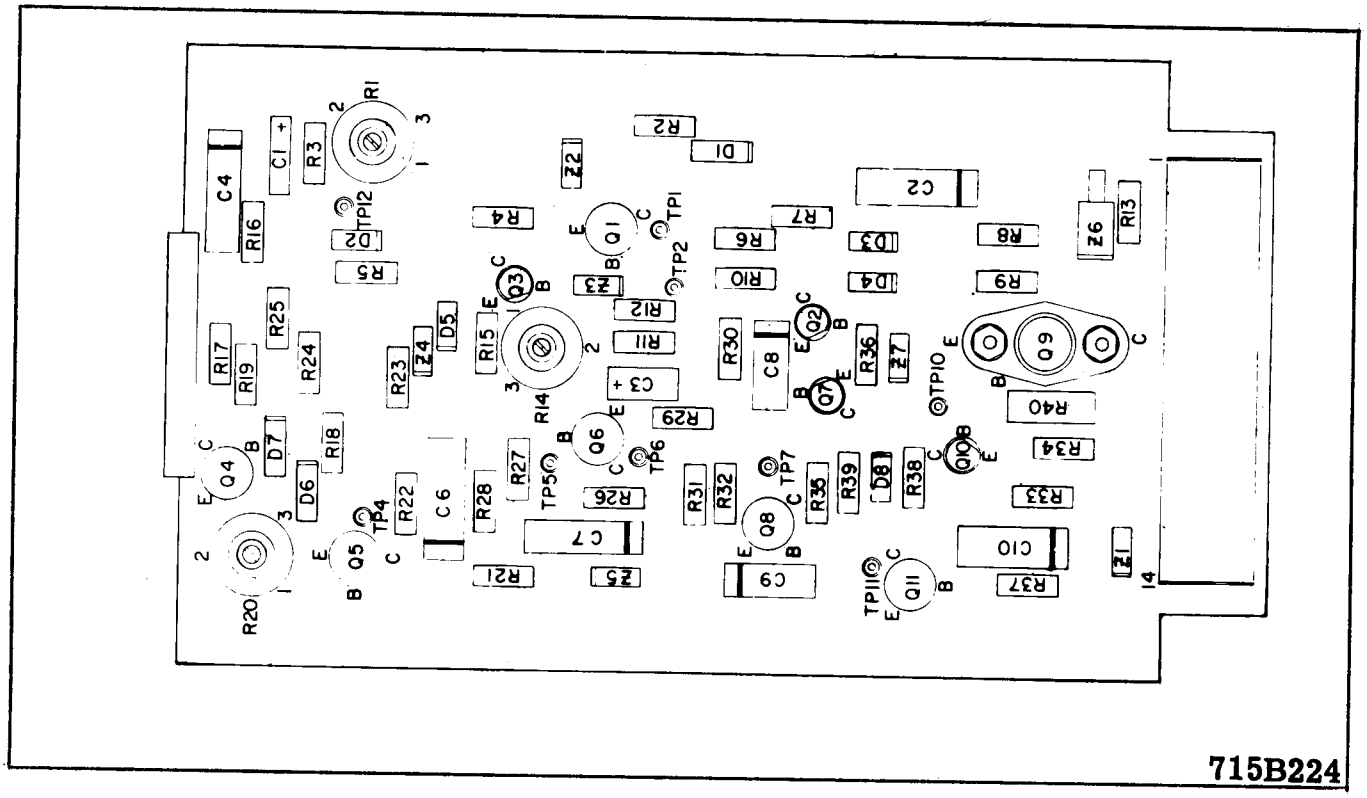



Fig. 38 Component Location Output Board.

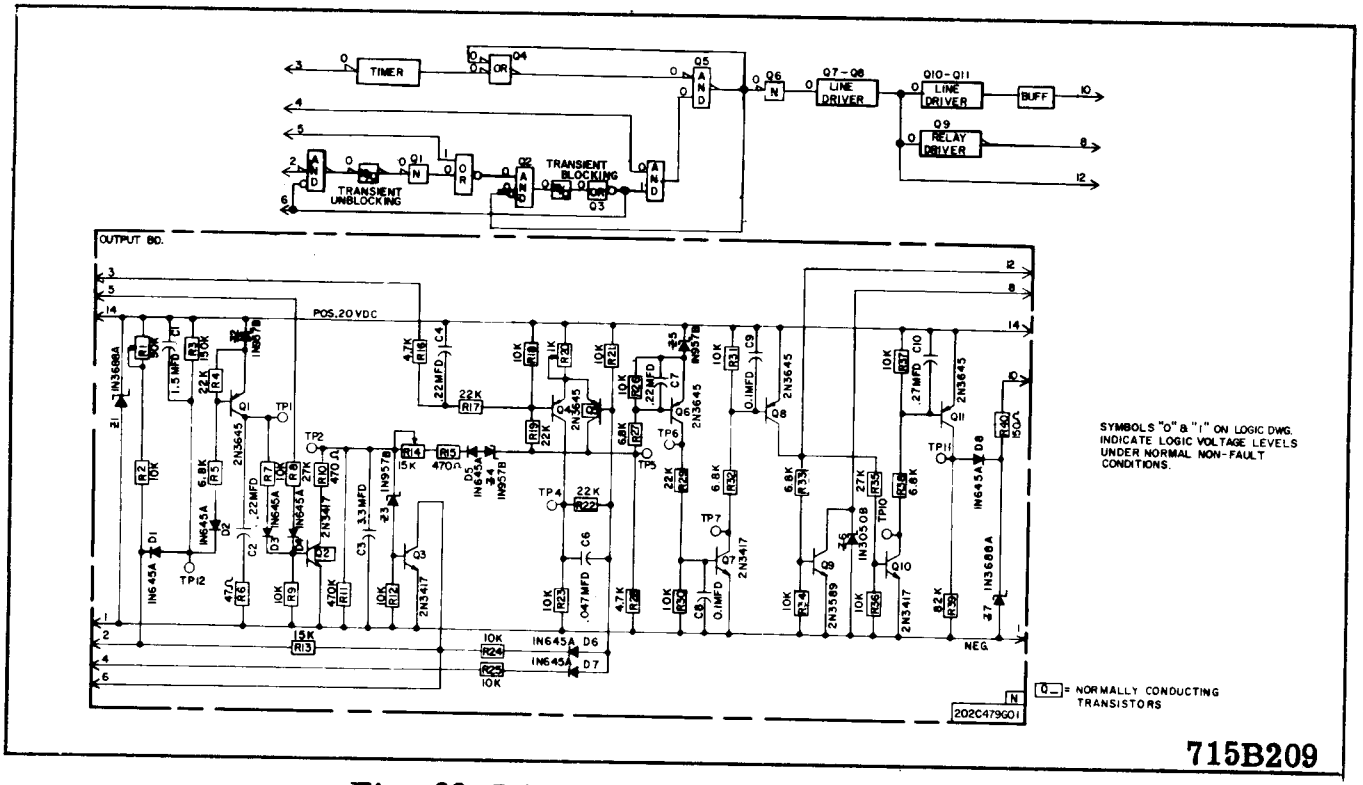



Fig. 39 Internal Schamtic Output Board.

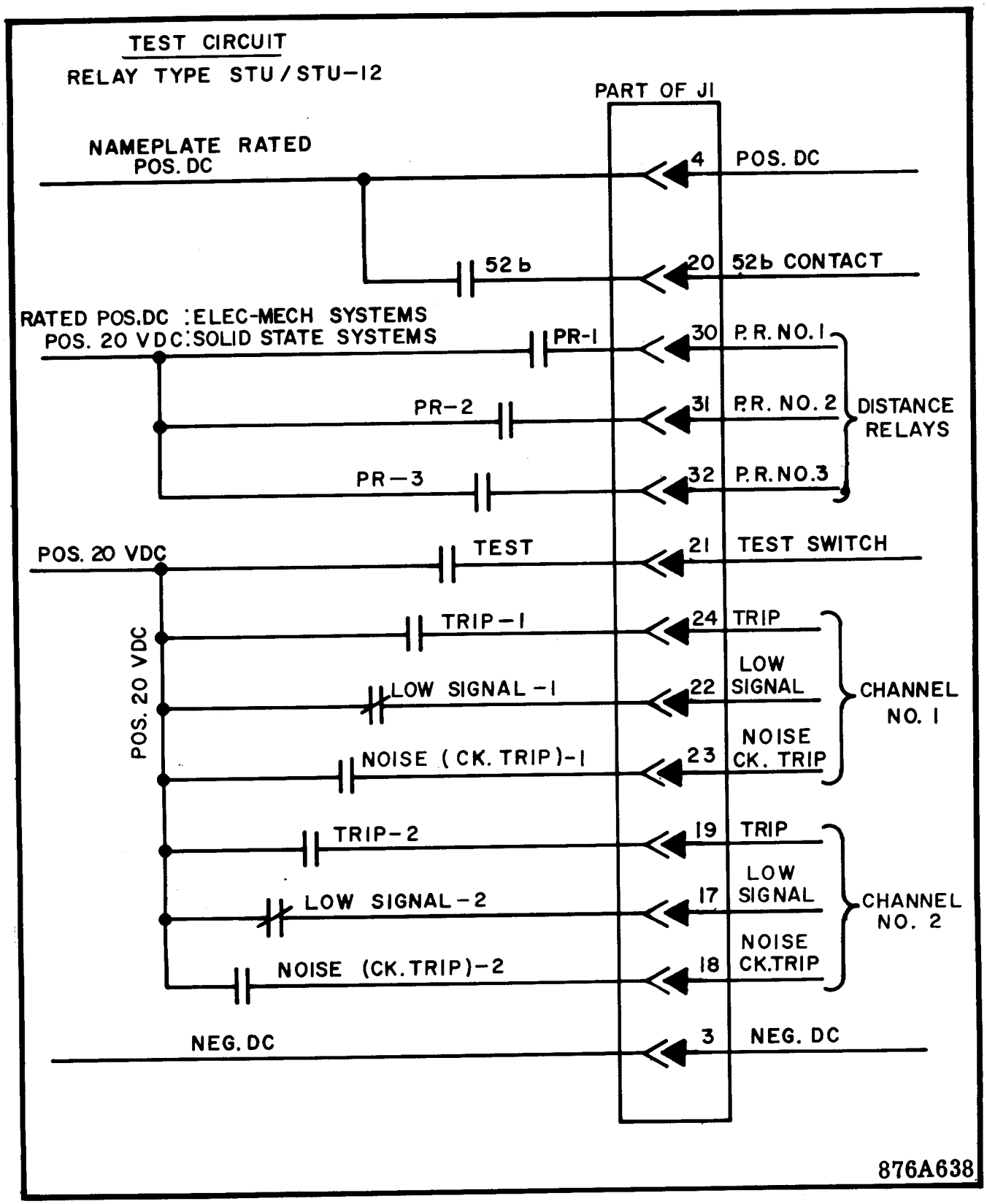



Fig. 40 Test Circuit.

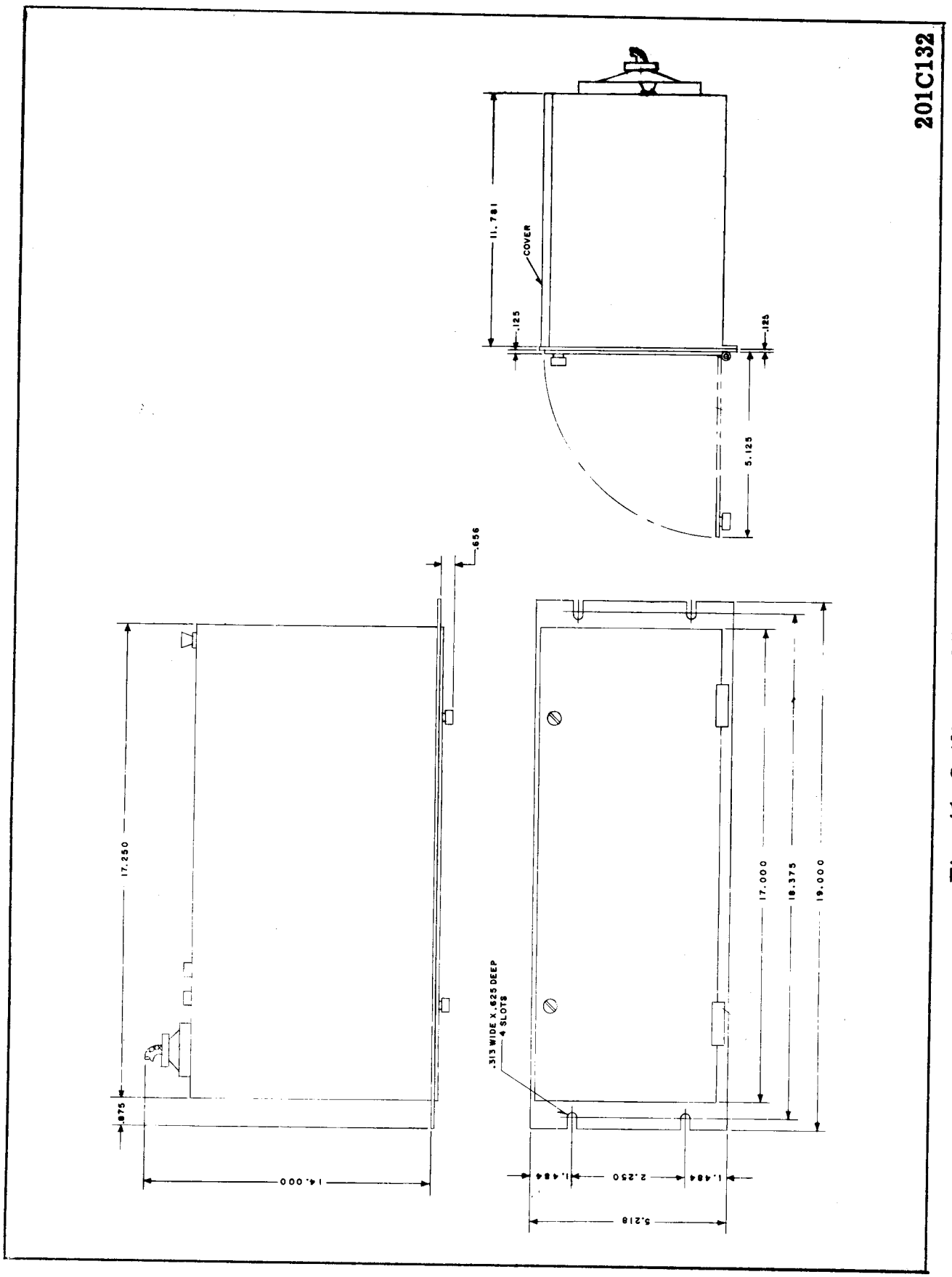
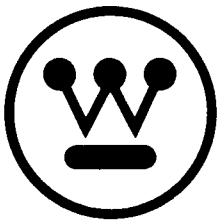



Fig. 41 Outline and Drilling Plan.



**WESTINGHOUSE ELECTRIC CORPORATION**

**RELAY-INSTRUMENT DIVISION** **NEWARK, N. J.**

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