INSTRUCTION MANUAL

DIRECTIONAL OVERCURRENT PROTECTION RELAY

GRD140

TOSHIBA CORPORATION

© TOSHIBA Corporation 2004 All Rights Reserved. **TOSHIBA**

Safety Precautions

Before using this product, please read this chapter carefully.

This chapter describes the safety precautions recommended when using the GRD140. Before installing and using the equipment, this chapter must be thoroughly read and understood.

Explanation of symbols used

Signal words such as DANGER, WARNING, and two kinds of CAUTION, will be followed by important safety information that must be carefully reviewed.

A DANGER Indicates an imminently hazardous situation which will result in death or serious injury if you do not follow the instructions.

AWARNING Indicates a potentially hazardous situation which could result in death or serious injury if you do not follow the instructions.

ACAUTION Indicates a potentially hazardous situation which if not avoided, may result in

minor injury or moderate injury.

CAUTION Indicates a potentially hazardous situation which if not avoided, may result in

property damage.

A DANGER

Current transformer circuit

Never allow the current transformer (CT) secondary circuit connected to this equipment to be opened while the primary system is live. Opening the CT circuit will produce a dangerously high voltage.

AWARNING

Exposed terminals

Do not touch the terminals of this equipment while the power is on, as the high voltage generated is dangerous.

Residual voltage

Hazardous voltage can be present in the DC circuit just after switching off the DC power supply. It takes approximately 30 seconds for the voltage to discharge

Fiber optic

When connecting this equipment via an optical fiber, do not look directly at the optical signal.

ACAUTION

Earth

The earthing terminal of the equipment must be securely earthed.

CAUTION

Operating environment

The equipment must only used within the range of ambient temperature, humidity and dust detailed in the specification and in an environment free of abnormal vibration.

Ratings

Before applying AC voltage and current or the DC power supply to the equipment, check that they conform to the equipment ratings.

Printed circuit board

Do not attach and remove printed circuit boards when the DC power to the equipment is on, as this may cause the equipment to malfunction.

External circuit

When connecting the output contacts of the equipment to an external circuit, carefully check the supply voltage used in order to prevent the connected circuit from overheating.

Connection cable

Carefully handle the connection cable without applying excessive force.

Modification

Do not modify this equipment, as this may cause the equipment to malfunction.

Disposal

When disposing of this equipment, do so in a safe manner according to local regulations.

Contents

	Saf	fety P	recautions	1
	1.	Intr	oduction	8
	2.	App	lication Notes	10
		2.1	Overcurrent and Undercurrent Protection	10
			2.1.1 Non-directional Overcurrent Protection	10
			2.1.2 Directional Overcurrent Protection	17
			2.1.3 Scheme Logic	21
			2.1.4 Phase Undercurrent Protection	44
			2.1.5 Thermal Overload Protection	46
			2.1.6 Broken Conductor Protection	49
			2.1.7 Breaker Failure Protection	52
			2.1.8 Cold Load Protection	55
			2.1.9 CT Requirements	58
		2.2	Overvoltage and Undervoltage Protection	60
			2.2.1 Phase Overvoltage Protection	60
			2.2.2 Phase Undervoltage Protection	63
			2.2.3 Zero Phase Sequence Overvoltage Protection	66
			2.2.4 Negative Phase Sequence Overvoltage Protection	69
		2.3	Frequency Protection	71
		2.4	Trip and Alarm Signal Output	73
		2.5	Autoreclose	75
			2.5.1 Scheme Logic	75
			2.5.2 Sequence Coordination	76
			2.5.3 Setting	77
	3.	Tecl	nnical Description	78
		3.1	Hardware Description	78
			3.1.1 Outline of Hardware Modules	78
		3.2	Input and Output Signals	82
			3.2.1 AC Input Signals	82
			3.2.2 Binary Input, Output Signals	82
	4		3.2.3 Binary Output Signals	86
		3.3	Automatic Supervision	87
			3.3.1 Basic Concept of Supervision	87
		\	3.3.2 Relay Monitoring	87
			3.3.3 CT Failure Supervision	88
			3.3.4 VT Failure Supervision	89
			3.3.5 Trip Circuit Supervision	90
N			3.3.6 Circuit Breaker Monitoring	91
			3.3.7 Failure Alarms	92
N			3.3.8 Trip Blocking	93
7			3.3.9 Setting	94

3.	4 Recording Function	95
	3.4.1 Fault Recording	95
	3.4.2 Event Recording	96
	3.4.3 Disturbance Recording	97
3.	5 Metering Function	99
3.	6 Fault locator	101
	3.6.1 Application	101
	3.6.2 Distance to Fault Calculation	101
	3.6.3 Starting Calculation	102
	3.6.4 Displaying Location	102
	3.6.5 Setting	103
4. U	ser Interface	104
4.	1 Outline of User Interface	104
	4.1.1 Front Panel	104
	4.1.2 Communication Ports	106
4.	2 Operation of the User Interface	107
	4.2.1 LCD and LED Displays	107
	4.2.2 Relay Menu	110
	4.2.3 Displaying Records	113
	4.2.4 Displaying the Status	118
	4.2.5 Viewing the Settings	124
	4.2.6 Changing the Settings	125
	4.2.7 Testing	168
4.	3 Personal Computer Interface	171
4.	4 Relay Setting and Monitoring System	171
4.	5 IEC 60870-5-103 Interface	172
4.	6 Clock Function	172
5. Ir	stallation	173
5.	1 Receipt of Relays	173
5.	2 Relay Mounting	173
5.	3 Electrostatic Discharge	173
5.	4 Handling Precautions	173
5.	5 External Connections	174
6. <i>C</i>	ommissioning and Maintenance	175
6.	1 Outline of Commissioning Tests	175
6.	2 Cautions	176
	6.2.1 Safety Precautions	176
•	6.2.2 Cautions on Tests	176
6.	•	177
6.		178
	6.4.1 User Interfaces	178
	6.4.2 Binary Input Circuit	178
	6.4.3 Binary Output Circuit	179
	6.4.4 AC Input Circuits	180

6.5	Function Test	182
	6.5.1 Measuring Element	182
	6.5.2 Protection Scheme	193
	6.5.3 Metering and Recording	193
6.6	Conjunctive Tests	194
	6.6.1 On Load Test	194
	6.6.2 Tripping and Reclosing Circuit Test	195
6.7	Maintenance	197
	6.7.1 Regular Testing	197
	6.7.2 Failure Tracing and Repair	197
	6.7.3 Replacing Failed Relay Unit	198
	6.7.4 Resumption of Service	199
	6.7.5 Storage	199
Putt	tting Relay into Service	200

Appendix A	Programmable Reset Characteristics and Implementation of Therm	nal	
	Model to IEC60255-8		201
Appendix B	Directional Earth Fault Protection and Power System Earthing		205
Appendix C	Signal List		211
Appendix D	Event Record Items		219
Appendix E	Details of Relay Menu and LCD & Button Operation	•	223
Appendix F	Case Outline		239
Appendix G	Typical External Connection		241
Appendix H	Relay Setting Sheet		247
Appendix I	Commissioning Test Sheet (sample)		261
Appendix J	Return Repair Form		265
Appendix K	Technical Data		269
Appendix L	Symbols Used in Scheme Logic		277
Appendix M	IEC60870-5-103: Interoperability		281
Appendix N	Inverse Time Characteristics		289
Annendix O	Ordering		295

■ The data given in this manual are subject to change without notice. (Ver.0.5)

TOSHIBA 6 F 2 S 0 7 5 8

1. Introduction

GRD140 series relays provide four stage non-directional and directional overcurrent protection for distribution networks, and back-up protection for transmission and distribution networks.

The GRD140 series has three models and provides the following protection schemes in all models.

- Directional overcurrent protection and directional zero phase sequence overcurrent protection for earth fault with definite time or inverse time characteristics
- Instantaneous directional overcurrent protection and instantaneous directional zero phase sequence overcurrent protection for earth fault

Model 110 provides directional earth fault protection and directional sensitive earth fault protection.

Model 400 provides three-phase directional phase fault protection and directional earth fault protection.

Model 420 provides three-phase directional phase fault protection, and directional earth and sensitive earth fault protection.

All models include multiple, high accuracy, overcurrent protection elements (for phase and/or earth fault) with inverse time and definite time delay functions. All phase, earth and sensitive earth fault overcurrent elements can be independently subject to directional control.

In addition, GRD140 provides multi-shot, three phase auto-reclose, with independent sequences for phase fault, and earth fault and sensitive earth fault. Auto-reclosing can also be triggered by external protection devices.

Other protection functions are available according to model type, including thermal protection to IEC60255-8, negative sequence overcurrent protection, under/overvoltage and under/overfrequency protections. See Table 1.1.1 for details of the protection functions available in each model.

All models provide continuous monitoring of internal circuits and of software. External circuits are also monitored, by trip circuit supervision, CT and VT supervision, and CB condition monitoring features.

A user-friendly HMI is provided through a backlit LCD, programmable LEDs, keypad and menu-based operating system. PC access is also provided, either for local connection via a front-mounted RS232 port, or for remote connection via a rear-mounted RS485 or fibre optic port. The communication system allows the user to read and modify the relay settings, and to access data gathered by the relay's metering and recording functions.

Data available either via the relay HMI or communications ports includes the following functions.

The GRD140 series provides the following functions for all models.

- Metering
- Fault recording
- Event recording
- Disturbance recording (available via communications ports)

Table 1.1.1 shows the members of the GRD140 series and identifies the functions to be provided by each member.

Table 1.1.1 Series Members and Functions

Table 1.1.1 Series Members and Funct					
Model Number	GRD14	GRD140 -			
	110	400	420		
Directional Phase Fault O/C OC1 – OC4 (67/50P, 67/51P)		✓	✓		
Directional Earth Fault O/C EF1 – EF4 (67/50N, 67/51N)	✓	✓	✓		
Directional Sensitive Earth Fault SEF1 – SEF4(67/50N, 67/51N)	✓		√ ♦		
Phase Undercurrent UC1, UC2 (37P)		1	✓		
Thermal Overload THM (49)		\ -	V		
Directional Negative Phase Sequence Overcurrent NOC1, NOC2 (67/46)		Y	✓		
Phase Overvoltage OV1, OV2 (59)		V	✓		
Phase Undervoltage UV1, UV2 (27)	5	✓	✓		
Zero Phase Sequence Overvoltage ZOV1, ZOV2 (59N)	V	✓	✓		
Negative Phase Sequence Overvoltage NOV1, NOV2 (47)		✓	✓		
Under/Overfrequency FRQ1 – FRQ4 (81U/81O)		✓	✓		
Broken Conductor BCD		✓	✓		
Circuit Breaker Fail CBF (50BF)		✓	✓		
Cold Load Protection		✓	✓		
Auto-reclose (79)	✓	✓	✓		
Fault Locator		✓	✓		
CT Supervision		✓	✓		
VT Supervision		✓	✓		
Trip circuit supervision	✓	✓	✓		
Self supervision	✓	✓	✓		
CB State Monitoring	✓	✓	✓		
Trip Counter Alarm	✓	✓	✓		
∑l ^y Alarm		✓	✓		
CB Operate Time Alarm	✓	✓	✓		
Four settings groups	✓	✓	✓		
Metering	✓	✓	✓		
Fault records	✓	✓	✓		
Event records	✓	✓	✓		
Disturbance records	✓	✓	✓		
IEC60870-5-103 Communication	✓	✓	✓		
	_	_	_		

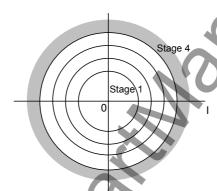
2. Application Notes

2.1 Overcurrent and Undercurrent Protection

2.1.1 Non-directional Overcurrent Protection

GRD140 provides distribution network protection with four-stage phase fault and earth fault overcurrent elements OC1 to OC4, EF1 to EF4, sensitive earth fault elements SEF1 to SEF4, and two-stage negative sequence overcurrent elements NOC1 and NOC2 which can be enabled or disabled by scheme switch setting. The OC1, EF1 and SEF1 elements have selective inverse time and definite time characteristics. The protection of local and downstream terminals is coordinated with the current setting, time setting, or both.

The characteristic of overcurrent elements are as follows:



Note: NOC provides two stage overcurrent elements.

Figure 2.1.1 Characteristic of Overcurrent Elements

2.1.1.1 Inverse Time Overcurrent Protection

In a system for which the fault current is practically determined by the fault location, without being substantially affected by changes in the power source impedance, it is advantageous to use inverse definite minimum time (IDMT) overcurrent protection. This protection provides reasonably fast tripping, even at a terminal close to the power source where the most severe faults can occur.

Where ZS (the impedance between the relay and the power source) is small compared with that of the protected section ZL, there is an appreciable difference between the current for a fault at the far end of the section (ES/(ZS+ZL), ES: source voltage), and the current for a fault at the near end (ES/ZS). When operating time is inversely proportional to the current, the relay operates faster for a fault at the end of the section nearer the power source, and the operating time ratio for a fault at the near end to the far end is ZS/(ZS+ZL).

The resultant time-distance characteristics are shown in Figure 2.1.2 for radial networks with several feeder sections. With the same selective time coordination margin TC as the download section, the operating time can be further reduced by using a more inverse characteristic.

Figure 2.1.2 Time-distance Characteristics of Inverse Time Protection

The inverse time overcurrent protection elements have the IDMT characteristics defined by equation (1):

$$t = TMS \times \left\{ \left\lceil \frac{k}{\left(I/I_{S}\right)^{n} - 1} \right\rceil + c \right\}$$
 (1)

where:

t = operating time for constant current I (seconds),

I = energising current (amps),

Is = overcurrent setting (amps),

TMS = time multiplier setting

k, a, c = constants defining curve

Nine curve types are available as defined in Table 2.1.1. They are illustrated in Figure 2.1.3. Any one curve can be selected for each IDMT element by scheme switch [M***C].

Table 2.1.1 Specification of IDMT Curves

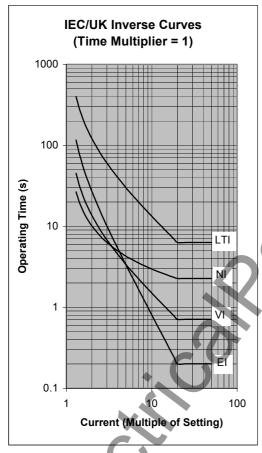
Curve Description	k	а	С	kr	b
IEC Normal Inverse (NI)	0.14	0.02	0	-	-
IEC Very Inverse (VI)	13.5	1	0	-	-
IEC Extremely Inverse (EI)	80	2	0	-	-
UK Long Time Inverse (LTI)	120	1	0	1	-
IEEE Moderately Inverse (MI)	0.0515	0.02	0.114	4.85	2
IEEE Very Inverse (VI)	19.61	2	0.491	21.6	2
IEEE Extremely Inverse (EI)	28.2	2	0.1217	29.1	2
US CO8 Inverse	5.95	2	0.18	5.95	2
US CO2 Short Time Inverse	0.02394	0.02	0.01694	2.261	2

Note: kr, b are used to define the reset characteristic. Refer to equation (2).

In addition to above nine curve types, GRD140 can provide a user configurable IDMT curve. If required, set the scheme switch [M***C] to "CON" and set the curve defining constants k, a, c.

The following table shows the setting ranges of the curve defining constants.

Curve defining constants	Range	Step
k	0.000 - 30.000	0.001
a	0.00 - 5.00	0.01
С	0.000 - 5.000	0.001
kr	0.000 - 30.000	0.001
b	0.00 - 5.00	0.01



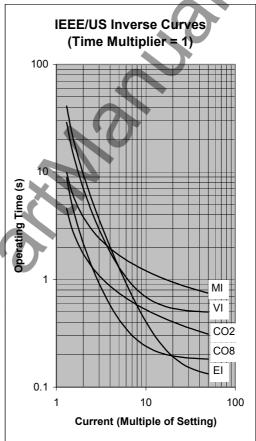


Figure 2.1.3 IDMT Characteristics

Programmable Reset Characteristics

OC1, EF1 and SEF1 have a programmable reset feature: instantaneous, definite time delayed, or dependent time delayed reset. (Refer to Appendix A for a more detailed description.)

Instantaneous resetting is normally applied in multi-shot auto-reclosing schemes, to ensure correct grading between relays at various points in the scheme.

The inverse reset characteristic is particularly useful for providing correct coordination with an supstream induction disc type overcurrent relay.

The definite time delayed reset characteristic may be used to provide faster clearance of intermittent ('pecking' or 'flashing') fault conditions.

Definite time reset

The definite time resetting characteristic is applied to the IEC/IEEE/US operating characteristics.

If definite time resetting is selected, and the delay period is set to instantaneous, then no intentional delay is added. As soon as the energising current falls below the reset threshold, the element returns to its reset condition.

If the delay period is set to some value in seconds, then an intentional delay is added to the reset period. If the energising current exceeds the setting for a transient period without causing tripping, then resetting is delayed for a user-definable period. When the energising current falls below the reset threshold, the integral state (the point towards operation that it has travelled) of the timing function (IDMT) is held for that period.

This does not apply following a trip operation, in which case resetting is always instantaneous.

Dependent time reset

The dependent time resetting characteristic is applied only to the IEEE/US operate characteristics, and is defined by the following equation:

$$t = RTMS \times \left[\frac{kr}{1 - \left(\frac{I}{I_S} \right)^b} \right]$$
 (2)

where:

t = time required for the element to reset fully after complete operation (seconds),

I = energising current (amps),

Is = overcurrent setting (amps),

kr = time required to reset fully after complete operation when the energising current is zero (see Table 2.1.1),

RTMS = reset time multiplier setting.

b = constants defining curve.

Figure 2.1.4 illustrates the dependent time reset characteristics.

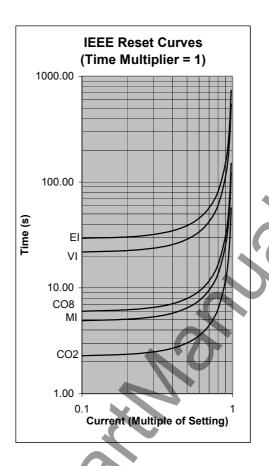


Figure 2.1.4 Dependent Time Reset Characteristics

2.1.1.2 Definite Time Overcurrent Protection

In a system in which the fault current does not vary a great deal in relation to the position of the fault, that is, the impedance between the relay and the power source is large, the advantages of the IDMT characteristics are not fully utilised. In this case, definite time overcurrent protection is applied. The operating time can be constant irrespective of the magnitude of the fault current.

The definite time overcurrent protection consists of instantaneous overcurrent measuring elements and delayed pick-up timers started by the elements, and provides selective protection with graded setting of the delayed pick-up timers. Thus, the constant time coordination with the downstream section can be maintained as shown in Figure 2.1.5. As is clear in the figure, the nearer to the power source a section is, the greater the delay in the tripping time of the section. This is undesirable particularly where there are many sections in the series.

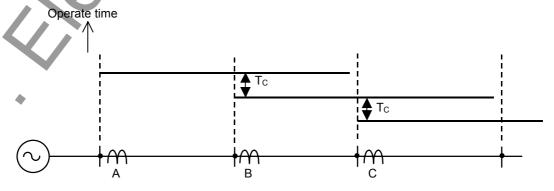


Figure 2.1.5 Definite Time Overcurrent Protection

2.1.1.3 Instantaneous Overcurrent Protection

In conjunction with inverse time overcurrent protection, additional overcurrent elements provide instantaneous or definite time overcurrent protection.

OC1 to OC4 and EF1 to EF4 are phase fault and earth fault protection elements, respectively. Each element is programmable for instantaneous or definite time delayed operation. (In case of instantaneous operation, the delayed pick-up timer is set to 0.00.) The phase fault elements operate on a phase segregated basis, although tripping is for three phase only.

Selective Instantaneous Overcurrent Protection

When they are applied to radial networks with several feeder sections where ZL (impedance of the protected line) is large enough compared with ZS (the impedance between the relay and the power source), and the magnitude of the fault current for a local end fault is much greater (3 times or more, or $(ZL+ZS)/ZS \ge 3$, for example) than that for a remote end fault under the condition that ZS is maximum, the pick-up current can be set sufficiently high so that the operating zone of the elements do not reach the remote end of the feeder, and thus instantaneous and selective protection can be applied.

This high-set overcurrent protection is applicable and effective particularly for feeders near the power source where the setting is feasible, but the longest tripping times would otherwise have to be accepted.

As long as the associated inverse time overcurrent protection is correctly coordinated, the instantaneous protection does not require setting coordination with the downstream section.

Figure 2.1.6 shows operating times for instantaneous overcurrent protection in conjunction with inverse time overcurrent protection. The shaded area shows the reduction in operating time by applying the instantaneous overcurrent protection. The instantaneous protection zone decreases as ZS increases.

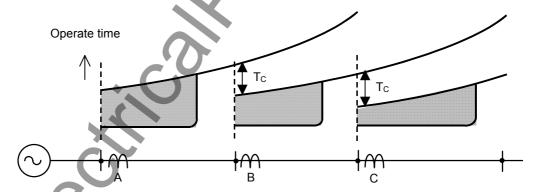


Figure 2.1.6 Conjunction of Inverse and Instantaneous Overcurrent Protection

The current setting is set 1.3 to 1.5 times higher than the probable maximum fault current in the event of a fault at the remote end. The maximum fault current for elements OC1 to OC4 is obtained in case of three-phase faults, while the maximum fault current for elements EF1 to EF4 is obtained in the event of single phase earth faults.

2.1.1.4 Staged Definite Time Overcurrent Protection

When applying inverse time overcurrent protection for a feeder system as shown in Figure 2.1.7, well coordinated protection with the fuses in branch circuit faults and high-speed protection for the feeder faults can be provided by adding staged definite time overcurrent protection with time-graded OC2 and OC3 or EF2 and EF3 elements.

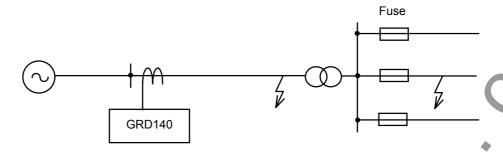


Figure 2.1.7 Feeder Protection Coordinated with Fuses

Configuring the inverse time element OC1 (and EF1) and time graded elements OC2 and OC3 (or EF2 and EF3) as shown in Figure 2.1.8, the characteristic of overcurrent protection can be improved to coordinate with the fuse characteristic.

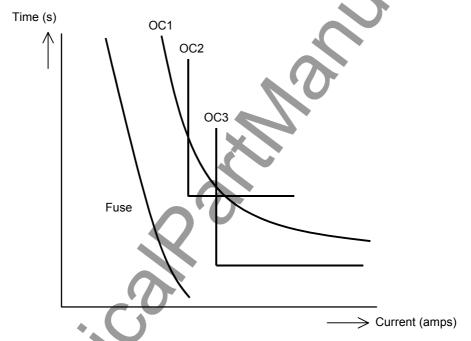


Figure 2.1.8 Staged Definite Time Protection

2.1.2 Directional Overcurrent Protection

In a system including parallel feeder circuits, ring main circuits or sources at both line terminals, the fault current at the relay location can flow in either direction. In such a case, directional control should be added to overcurrent elements.

GRD140 provides directional control for phase fault and earth fault overcurrent elements OC1 to OC4, EF1 to EF4, SEF1 to SEF4, NOC1 and NOC2 which can be enabled or disabled by scheme switch setting. The directional characteristic can be selected to "Forward" or "Reverse" or "Non" by scheme switch setting [***-DIR]. The OC1, EF1 and SEF1 elements have selective inverse time and definite time characteristics.

2.1.2.1 Application of Directional Overcurrent Protection

Parallel Feeder Circuits

If non-directional protection were applied to the circuit shown in Figure 2.1.9, then a fault at F would result in both feeders being tripped at points A and B, and total loss of supply to the load.

Directional relays can be applied to look back into the feeder, thereby ensuring that only the faulty feeder is disconnected. The relays at A and B would normally be set to operate at 50% of the full load current of the circuit, via their inverse time elements OC1 and EF1, with a directional characteristic looking in the direction shown by the arrows.

The various overcurrent elements of GRD140 are independently programmable for directional operation. Therefore, elements OC2 and EF2 could be set for non-directional operation to provide time-delayed back-up protection for the load.

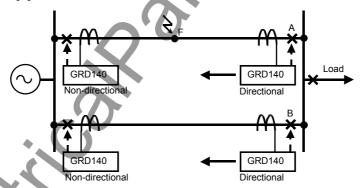


Figure 2.1.9 Application of GRD140 to Parallel Feeders

Ring Main Circuits

A ring main circuit is commonly protected by directional overcurrent relays, since current may flow in either direction past the relaying points. The normal grading procedure is applied separately in both the clockwise and anti-clockwise directions. Conventionally, two directional relays would be required at each load connection point, one for each direction.

A simple system is illustrated in Figure 2.1.10 showing definite time grading, although inverse time can also be applied. Non-directional relays are applied at the in-feeds to the ring. All other protections are directional relays. It can be seen that a fault at F is cleared by tripping at A in 1.0s and at B in 0.4s.

Alternatively, since GRD140 provides multiple, independent bi-directional overcurrent stages, a scheme could be implemented in which a single relay can perform the necessary protection functions in both directions at each load connection point. Each GRD140 overcurrent element can be programmed with different settings for forward and reverse direction, thus allowing correct grading to be achieved in both the clockwise and anti-clockwise directions.

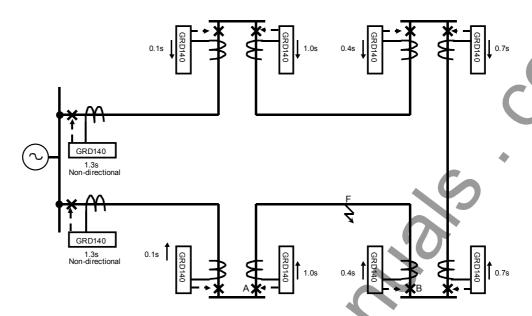


Figure 2.1.10 Protection of a Ring Main Circuit

Power Systems with Sources at both Line Terminals

In power systems with sources at both line terminals as shown in Figure 2.1.11, the fault current flows in from both terminals.

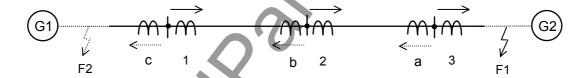


Figure 2.1.11 Protection of a power system with sources at both line terminals

The protection is performed by setting the directional element at points 1, 2 and 3 which operates only when the fault current (F1: solid lines) flows in from source G1 and at points a, b and c which operates only when the fault current (F2: dotted lines) flows in from source G2, with grading provided by time delays.

2.1.2.2 Directional Characteristics

Figure 2.1.12 illustrates the directional characteristic, with the forward operate zone shaded. The reverse zone is simply a mirror image of the forward zone. The forward operate zone or reverse operate zone is selectable by the scheme switch [OC-DIR], [EF-DIR], [SE-DIR] and [NC-DIR]. As shown in Figure 2.1.13, each directional characteristic is composed of forward directional characteristic, reverse directional characteristic and overcurrent thresholds.

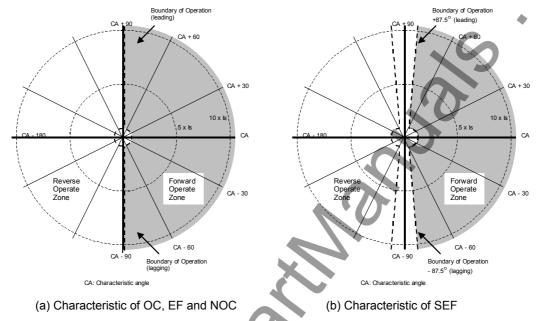


Figure 2.1.12 Directional Operate Characteristic

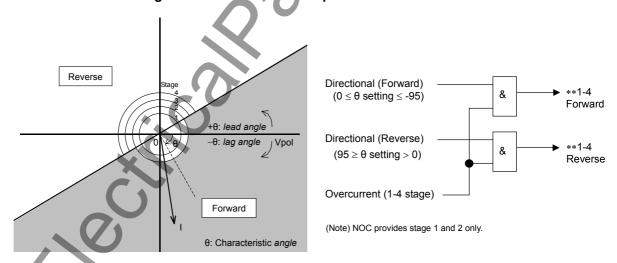


Figure 2.1.13 Directional element

Polarising signals of directional elements are shown in Figure 2.1.14. Polarisation for directional phase overcurrent element OC is achieved by the 90° quadrature method, whereby each current's phase angle is compared with the phase to phase voltage between the other two phases. Since the voltage inputs to the relay will normally be connected phase to neutral, the polarising phase to phase voltages are derived internally. The polarizing negative sequence voltage is also derived internally. The polarizing zero sequence voltage is derived from a residual voltage or internally depending on the model. Direction is determined in each case by measuring the phase angle of the current with respect to a suitable polarising quantity. Table 2.1.2 summarises the current inputs and their respective polarising signals. For details of the relationship between directional earth fault protection and power system earthing, see Appendix B.

TOSHIBA 6 F 2 S 0 7 5 8

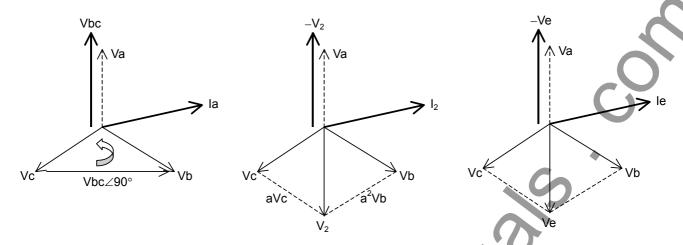


Figure 2.1.14 Relationship between Current Input and Polarising signal

Table 2.1.2 Directional polarising signals

Note (*): The quadrature voltages used for polarization the phase fault elements are automatically phase-shifted by +90°, such that they are in phase with the faulted phase voltage under normal conditions. Therefore the faulted phase current will normally <u>lag</u> its polarizing voltage under fault conditions and should be set with a <u>negative</u> characteristic angle. Refer to section 2.1.3.3 for guidance on choice of settings.

In the event of a close up three phase fault, all three polarising signals will collapse below the minimum threshold. Voltage memory provides a temporary polarising signal in these circumstances. GRD140 maintains the polarising signal for a short period by reconstructing the pre-fault voltages and judges the fault direction. After the voltage memory has disappeared, the direction judgement is effective while the fault current flows as shown in Figure 2.1.15.

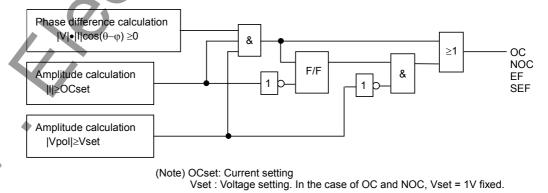


Figure 2.1.15 Direction Judgement after Disappearance of Voltage Memory

To cover applications where a 2:1:1 current distribution^(*) may be experienced, it is possible to

programme the directional phase fault protection such that a trip output will only be given if two or more phases detect fault current in the same operate zone.

Note (*): Only one-phase is in heavy load condition.

2.1.3 Scheme Logic

2.1.3.1 Phase overcurrent protection

Figures 2.1.16 to 2.1.19 show the scheme logic of the non-directional and directional phase overcurrent protection OC1 to OC4.

The directional control characteristic can be selected to "Forward (FWD)" or "Reverse (REV)" or "Non" by scheme switch setting [OC*-DIR] (not shown in Figures 2.1.16 to 2.1.19).

The OC1 protection provides selective definite time or inverse time characteristic as shown in Figure 2.1.16. The definite time protection is selected by setting [MOC1] to "DT" and trip signal OC1 TRIP is given through the delayed pick-up timer TOC1. The inverse time protection is selected by setting [MOC1] to any one of "IEC", "IEEE", "US" or "CON" and then setting [MOC1C] according to the required IDMT characteristic, and trip signal OC1 TRIP is given.

Figure 2.1.17 to Figure 2.1.19 show the scheme logic of the definite time phase overcurrent protection OC2 to OC4. The OC2 to OC4 give trip and alarm signals OC2 TRIP, OC3 TRIP and OC4 ALARM through the delayed pick-up timers TOC2 to TOC4 respectively.

The trip mode of OC1 TRIP to OC4 ALARM can be selected by setting [OCTP] to "3POR" (any one of 3 phases) or "2OUTOF3" (2 out of 3 phases) gate. When the "2OUTOF3" selected, the trip signal is not issued during a single-phase fault. The switch [OCTP] is common for OC1 to OC4 protection.

The signal OC1-INST to OC4-INST are available to trip instantaneously for a fault such as a reclose-on-to-a-fault. (See Section 2.5)

The OC1HS (high speed) element is used for blocked overcurrent protection. See Section 2.1.3.6.

GRD140 incorporates a VT failure supervision function (VTFS). (See Section 3.3.4.) When the VTFS detects a VT failure, it can alarm and block the OC1 to OC4 protection by the scheme switch [VTF OC1-BLK] to [VTF OC4-BLK] respectively.

The OC1 to OC4 protection can be disabled by the scheme switches [OC1EN] to [OC4EN] or the binary input signals OC1 BLOCK to OC4 BLOCK respectively.

Note: For the symbols used in the scheme logic, see Appendix L.

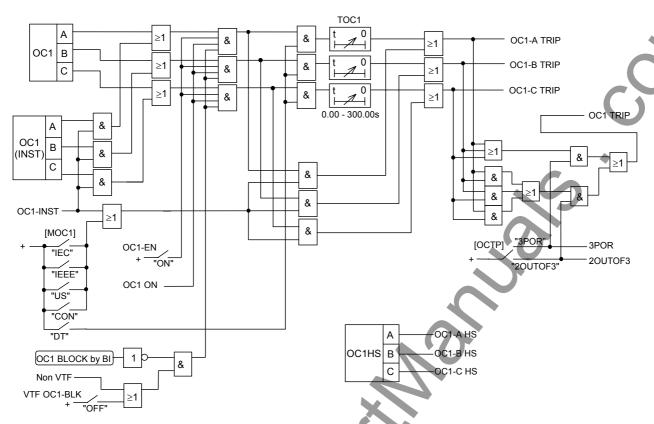


Figure 2.1.16 OC1 Phase Fault Overcurrent Protection

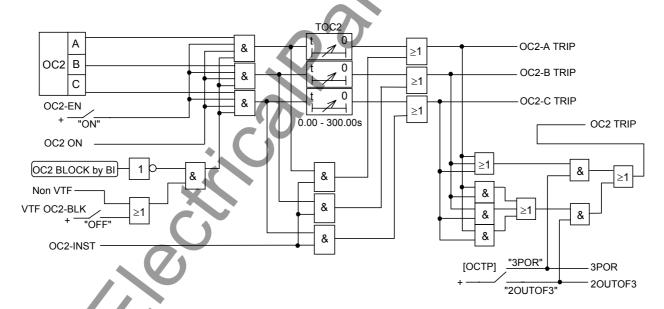


Figure 2.1.17 OC2 Phase Fault Overcurrent Protection

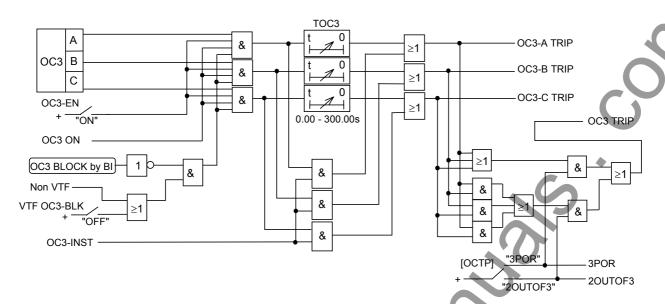


Figure 2.1.18 OC3 Definite Time Phase Overcurrent Protection

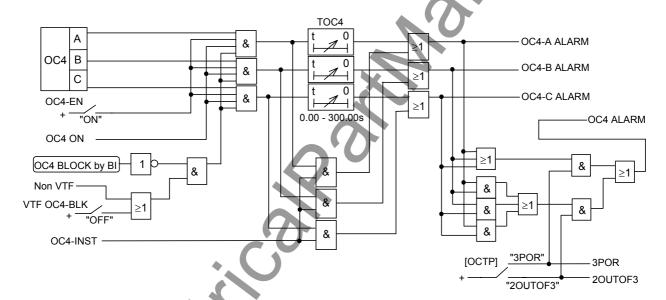


Figure 2.1.19 OC4 Definite Time Phase Overcurrent Protection

2.1.3.2 Earth fault protection

Figure 2.1.20 to Figure 2.1.23 show the scheme logic of the non-directional and directional earth fault protection EF1 to EF4.

The directional control characteristic can be selected to "FWD" or "REV" or "Non" by scheme switch setting [EF*-DIR] (not shown in Figures 2.1.20 to 2.1.23).

The EF1 protection provides selective definite time or inverse time characteristic as shown in Figure 2.1.20. The definite time protection is selected by setting [MEF1] to "DT", and the trip signal EF1 TRIP is given through the delayed pick-up timer TEF1. The inverse time protection is selected by setting [MEF1] to any one of "IEC", "IEEE", "US" or "CON" and then setting [MEF1C] according to the required IDMT characteristic, and the trip signal EF1 TRIP is given.

Figure 2.1.21 to Figure 2.1.23 show the scheme logic of the definite time earth fault protection EF2 to EF4. The EF2 to EF4 give trip and alarm signals EF2 TRIP, EF3 TRIP and EF4 ALARM through the delayed pick-up timers TEF2, TEF3 and TEF4 respectively.

The signal EF1-INST to EF4-INST are available to trip instantaneously for a fault such as a reclose-on-to-a-fault. (See Section 2.5)

EF1HS (high speed) element is used for blocked overcurrent protection. See Section 2.1.3.6,

GRD140 incorporates a VT failure supervision function (VTFS) and a CT failure supervision function (CTFS). When the VTFS or CTFS detects a VT failure or a CT failure, it can alarm and block the EF1 to EF4 protection by the scheme switch [VTF EF1-BLK] to [VTF EF4-BLK] or [CTF EF1-BLK] to [CTF EF4-BLK] respectively.

The EF1 to EF4 protection can be disabled by the scheme switches [EF1EN] to [EF4EN] or the binary input signals EF1 BLOCK to EF4 BLOCK respectively.

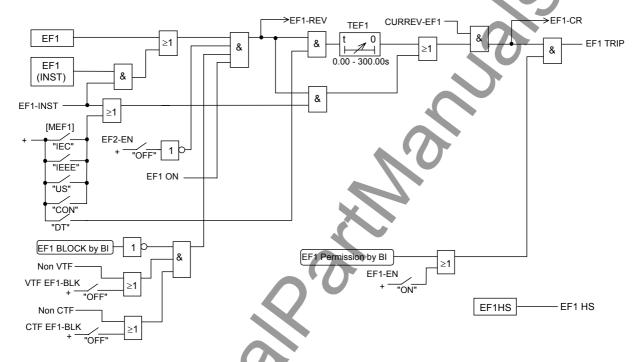


Figure 2.1.20 EF1 Earth Fault Protection

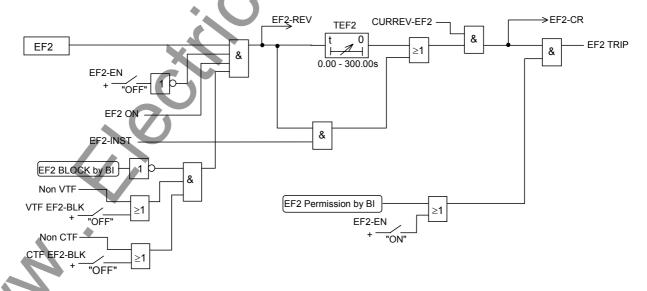


Figure 2.1.21 EF2 Earth Fault Protection

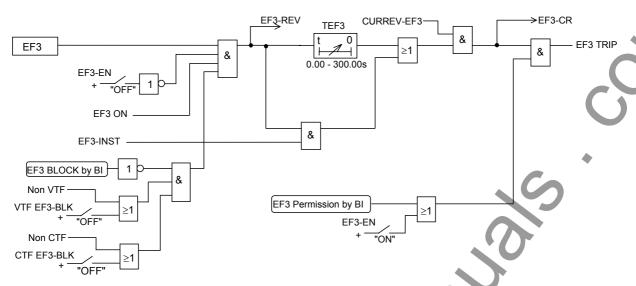


Figure 2.1.22 EF3 Definite Time Earth Fault Protection

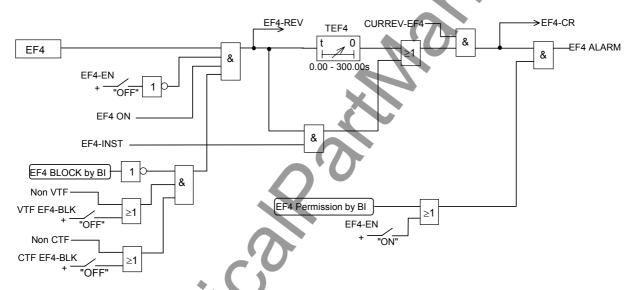


Figure 2.1.23 EF4 Definite Time Earth Fault Protection

Earth fault command protection

GRD140 can provide the command protection. These protections require two stage EF elements, one is for tripping and the other is for blocking or for current reverse detection.

Current reverse detection logic is provided with all stages EF1 to EF4 for command protection as shown in Figure 2.1.24. In response to power system faults on parallel lines, sequential opening of the circuit breaker may cause a fault current reversal on healthy lines. This logic is provided to prevent false operation in the worst case. When EF reverse zone operates and EF*-REV outputs for 20ms or more, then even if the EF forward zone subsequently operates, CURREV-EF* becomes 0 to block tripping of the local terminal relay or transmission of the trip permission signal, for a time set by the TREBK setting.

The stage used for current reverse detection should be selected by the scheme switch [CURREV]. The selected stage should have scheme switch [EF*-DIR] set to "REV".

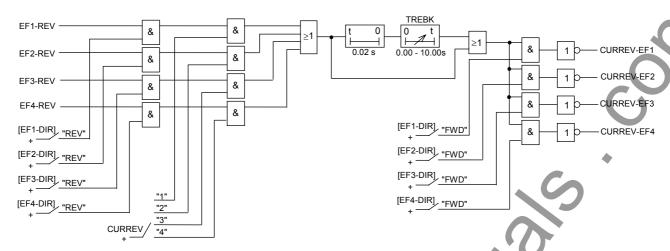


Figure 2.1.24 Current Reverse Detection

2.1.3.3 Setting for OC and EF protection

The table shows the setting elements necessary for the phase overcurrent and earth fault protection and their setting ranges.

Element	Range	Step	Default	Remarks
ОСӨ	−95 − 95°	1°	-45°	OC characteristic angle
OC1	0.1 – 25.0 A (0.02 – 5.00 A)(*)	0.1 A (0.01 A)	5.0 A (1.00 A)	OC1 threshold setting
TOC1	0.00 – 300.00 s	0.01 s	1.00 s	OC1 definite time setting. Required if [MOC1] = DT.
TOC1M	0.010 – 1.500	0.001	1.000	OC1 time multiplier setting. Required if [MOC1] = IEC, IEEE or US.
TOC1R	0.0 – 300.0 s	0.1 s	0.0 s	OC1 definite time delayed reset. Required if [OC1R] = DEF.
TOC1RM	0.010 – 1.500	0.001	1.000	OC1 dependent time delayed reset time multiplier. Required if [OC1R] = DEP.
OC2	0.1 – 25.0 A (0.02 – 5.00 A)(*)	0.1 A (0.01 A)	5.0 A (1.00 A)	OC2 threshold setting
TOC2	0.00 - 300.00 s	0.01 s	1.00 s	OC2 definite time setting.
OC3	0.1 – 250.0 A (0.02 – 50.00 A)(*)	0.1 A (0.01 A)	50.0 A (10.00 A)	OC3 threshold setting
TOC3	0.00 – 300.0 s	0.01 s	1.00 s	OC3 definite time setting
OC4	0.1 – 250.0 A (0.02 – 50.00 A)(*)	0.1 A (0.01 A)	100.0 A (20.00 A)	OC4 threshold setting
TOC4	0.0 - 300.0 s	0.01 s	1.00 s	OC4 definite time setting
EFθ	−95 − 95 °	1°	–45 °	EF characteristic angle
EFV	0.5 – 100.0 V	0.1 V	3.0 V	EF ZPS voltage level
EF1	0.1 – 25.0 A (0.02 – 5.00 A)	0.1 A (0.01 A)	1.5 A (0.30 A)	EF1 threshold setting
TEF1	0.00 – 300.00 s	0.01 s	1.00 s	EF1 definite time setting. Required if [MEF1] = DT.

	Element	Range	Step	Default	Remarks
_	TEF1M	0.010 – 1.500	0.001	1.000	EF1 time multiplier setting. Required if [MEF1] = IEC, IEEE or US.
	TEF1R	0.0 – 300.0 s	0.1 s	0.0 s	EF1 definite time delayed reset. Require [EF1R] = DEF.
	TEF1RM	0.010 – 1.500	0.001	1.000	EF1 dependent time delayed reset time multiplier. Required if [EF1R] = DEP.
	EF2	0.1 – 25.0 A (0.02 – 5.00 A)	0.1 A (0.01 A)	1.5 A (0.30 A)	EF2 threshold setting
	TEF2	0.00 – 300.00 s	0.01 s	1.00 s	EF2 definite time setting.
	EF3	0.1 – 250.0 A (0.02 – 50.00 A)(*)	0.1 A (0.01 A)	25.0 A (5.00 A)	EF3 threshold setting
	TEF3	0.00 - 300.00 s	0.01 s	1.00 s	EF3 definite time setting
	EF4	0.1 – 250.0 A (0.02 – 50.00 A)(*)	0.1 A (0.01 A)	50.0 A (10.00 A)	EF4 threshold setting
	TEF4	0.00 – 300.00 s	0.01 s	1.00 s	EF4 definite time setting
	TREBK	0.00 – 10.00 s	0.01 s	0.10	Current reverse blocking time
	[OC1EN]	Off / On		On	OC1 Enable
	[OC1-DIR]	FWD/REV/NON		FWD	OC1 directional characteristic
	[MOC1]	DT/IEC/IEEE/US/CON		DT	OC1 time characteristic
	[MOC1C] MOC1C-IEC MOC1C-IEEE MOC1C-US	NI/VI/EI/LTI MI/VI/EI CO2/CO8	२	NI MI CO2	OC1 inverse curve type. Required if [MOC1] = IEC. Required if [MOC1] = IEEE. Required if [MOC1] = US.
	[OC1R]	DEF / DEP		DEF	OC1 reset characteristic. Required if [MOC1] = IEEE or US.
	[VTF-OC1BLK]	Off / On		Off	VTF block enable
	[OC2EN]	Off / On		Off	OC2 Enable
	[OC2-DIR]	FWD/REV/NON		FWD	OC2 directional characteristic
	[VTF-OC2BLK]	Off / On		Off	VTF block enable
	[OC3EN]	Off / On		Off	OC3 Enable
	[OC3-DIR]	FWD/REV/NON		FWD	OC3 directional characteristic
	[VTF-OC3BLK]	Off / On		Off	VTF block enable
	[OC4EN]	Off / On		Off	OC4 Enable
	[OC4-DIR]	FWD/REV/NON		FWD	OC4 directional characteristic
	[VTF-OC4BLK]	Off / On		Off	VTF block enable
•	[OCTP]	3POR / 2OUTOF3		3POR	OC trip mode
4	[EF1EN]	Off / On / POP		On	EF1 Enable
7	[EF1-DIR]	FWD/REV/NON		FWD	EF1 directional characteristic
1	[MEF1]	DT/IEC/IEEE/US/CON		DT	EF1 time characteristic
	[MEF1C] MEF1C-IEC	NI / VI / EI / LTI		NI	EF1 inverse curve type. Required if [MEF1] = IEC.

Element	Range	Step	Default	Remarks
MEF1C-IEEE MEF1C-US	MI / VI / EI CO2 / CO8		MI CO2	Required if [MEF1] = IEEE. Required if [MEF1] = US.
[EF1R]	DEF / DEP		DEF	EF1 reset characteristic. Required if [MEF1] = IEEE or US.
[VTF-EF1BLK]	Off / On		Off	VTF block enable
[CTF-EF1BLK]	Off / On		Off	CTF block enable
[EF2EN]	Off / On / POP		Off	EF2 Enable
[EF2-DIR]	FWD/REV/NON		FWD	EF2 directional characteristic
[VTF-EF2BLK]	Off / On		Off	VTF block enable
[CTF-EF2BLK]	Off / On		Off	CTF block enable
[EF3EN]	Off / On / POP		Off	EF3 Enable
[EF3-DIR]	FWD/REV/NON		FWD	EF3 directional characteristic
[VTF-EF3BLK]	Off / On		Off	VTF block enable
[CTF-EF3BLK]	Off / On		Off	CTF block enable
[EF4EN]	Off / On / POP		Off	EF4 Enable
[EF4-DIR]	FWD/REV/NON		FWD	EF4 directional characteristic
[VTF-EF4BLK]	Off / On		Off	VTF block enable
[CTF-EF4BLK]	Off / On		Off	CTF block enable
CURREV	Off / 1 / 2 / 3 / 4		Off	Current reverse detection

^(*) Current values shown in the parenthesis are in the case of a 1 A rating. Other current values are in the case of a 5 A rating.

[Setting Example of Command Protection]

The followings show a setting example of command protection when the EF1 is applied for forward fault detection and the EF2 is applied for reverse fault detection.

(1) POP (Permissive overreach protection)

(a) Setting of EF element

EF1: ** --- depends on power system condition

TEF1: ** --- for time delay trip

EF1EN: POP

EF1-DIR: FWR

EF2: ** --- depends on power system condition

TEF2: <u>0.00s</u>

▶ EF2EN: <u>POP</u>

EF2-DIR: REV

CURREV: 2

(b) Setting of BO (Binary Output)

The signal "EF1-CR (No.285)" is assigned to BOn. --- carrier signal send BO

(c) Setting of BI (Binary Input)

The "EF1 protection permission" is assigned to BIn. --- carrier signal receive BI

BIn SNS: Norm

(2) BOP (Blocking overreach protection)

(a) Setting of EF element

EF1: ** --- depends on power system condition

TEF1: ** --- for time delay trip

EF1EN: <u>POP</u> EF1-DIR: FWR

EF2: ** --- depends on power system condition

TEF2: <u>0.30s (minimum)</u> --- coordination time for blocking carrier signal receiving

EF2EN: POP
EF2-DIR: REV
CURREV: 2

(b) Setting of BO (Binary Output)

The signal "EF2-CR (No.286)" is assigned to BOn. --- carrier signal send BO

(c) Setting of BI (Binary Input)

The "EF1 protection permission" is assigned to BIn. --- carrier signal receive BI

BIn SNS: Inv

[Time Overcurrent Protection Setting]

(1) Settings for Inverse Time Overcurrent Protection

Current setting

In Figure 2.1.25, the current setting at terminal A is set lower than the minimum fault current in the event of a fault at remote end F1. Furthermore, when also considering backup protection for a fault on the next feeder section, it is set lower than the minimum fault current in the event of a fault at remote end F3.

To calculate the minimum fault current, phase-to-phase faults are assumed for the phase overcurrent element, and phase to earth faults for residual overcurrent element, assuming the probable maximum source impedance. When considering the fault at F3, the remote end of the next section is assumed to be open.

The higher the current setting, the more effective the inverse characteristic. On the other hand, the lower the setting, the more dependable the operation. The setting is normally 1 to 1.5 times or less of the minimum fault current.

For grading of the current settings, the terminal furthest from the power source is set to the lowest value and the terminals closer to the power source are set to a higher value.

The minimum setting of the phase overcurrent element is restricted so as not to operate for the maximum load current, and that of the residual overcurrent element is restricted so as to not operate on false zero-sequence current caused by an unbalance in the load current, errors in the current transformer circuits, or zero-sequence mutual coupling of parallel lines.

TOSHIBA 6 F 2 S 0 7 5 8

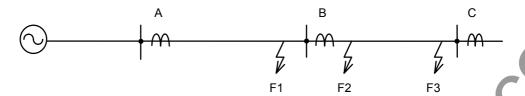


Figure 2.1.25 Current Settings in Radial Feeder

Time setting

Time setting is performed to provide selectivity in relation to the relays on adjacent feeders. Consider the minimum source impedance when the current flowing through the relay reaches a maximum. In Figure 2.1.25, in the event of a fault at F2, the operating time is set so that terminal A may operate by time grading Tc behind terminal B. The current flowing in the relays may sometimes be greater when the remote end of the adjacent line is open. At this time, time coordination must also be kept.

The reason why the operating time is set when the fault current reaches a maximum is that if time coordination is obtained for a large fault current, then time coordination can also be obtained for the small fault current as long as relays with the same operating characteristic are used for each terminal.

The grading margin Tc of terminal A and terminal B is given by the following expression for a fault at point F2 in Figure 2.1.25.

 $T_c = T_1 + T_2 + T_m$

where, T_1 : circuit breaker clearance time at B

T₂: relay reset time at A

T_m: time margin

(2) Settings of Definite Time Overcurrent Protection

Current setting

The current setting is set lower than the minimum fault current in the event of a fault at the remote end of the protected feeder section. Furthermore, when also considering backup protection for a fault in a next feeder section, it is set lower than the minimum fault current, in the event of a fault at the remote end of the next feeder section.

Identical current values can be set for terminals, but graded settings are better than identical settings, in order to provide a margin for current sensitivity. The farther from the power source the terminal is located, the higher the sensitivity (i.e. the lower setting) that is required.

The minimum setting of the phase overcurrent element is restricted so as not to operate for the maximum load current, and that of the residual overcurrent element is restricted so as to not operate on false zero-sequence current caused by an unbalance in the load current, errors in the current transformer circuits, or zero-sequence mutual coupling of parallel lines. Taking the selection of instantaneous operation into consideration, the settings must be high enough not to operate for large motor starting currents or transformer inrush currents.

Time setting

When setting the delayed pick-up timers, the time grading margin Tc is obtained in the same way as explained in "Settings for Inverse Time Overcurrent Protection".

(3) Directional Characteristic Angle Setting

OC Characteristic Angle

The quadrature voltages used for polarization of the phase fault directional elements are automatically phase-shifted in GRD140 by $+90^{\circ}$, such that they are in phase with the corresponding phase voltages under normal conditions. Under fault conditions, the faulted phase current will <u>lag</u> its phase voltage (and hence its polarising voltage) by an angle dependent on the system X/R ratio. Therefore, it is necessary to apply a <u>negative</u> characteristic angle to the phase fault directional elements in order to obtain maximum sensitivity.

The characteristic angle is determined by the $[OC\theta]$ setting. The actual value chosen will depend on the application, but recommended settings for the majority of typical applications are as follows:

- -60°, for protection of plain feeders, or applications with an earthing point behind the relay location.
- -45°, for protection of transformer feeders, or applications with an earthing point in front of the relay location.

EF Characteristic Angle

When determining the characteristic angle for directional earth fault protection, the method of system earthing must be considered. In solidly earthed systems, the earth fault current tends to lag the faulted phase voltage (and hence the inverted residual voltage used for polarising) by a considerable angle, due to the reactance of the source. In resistance earthed systems the angle will be much smaller.

Commonly applied settings are as follows:

- -60°, for protection of solidly earthed transmission systems.
- -45°, for protection of solidly earthed distribution systems.
- 0° or -15°, for protection of resistance earthed systems.

Further guidance on application of directional earth fault protection is given in appendix B.

2.1.3.4 Sensitive Earth Fault Protection

The sensitive earth fault (SEF) protection is applied for distribution systems earthed through high impedance, where very low levels of fault current are expected in earth faults. Furthermore, the SEF elements of GRD140 are also applicable to the "standby earth fault protection" and the "high impedance restricted earth fault protection of transformers".

GRD140 provides directional earth fault protection with more sensitive settings for use in applications where the fault current magnitude may be very low. A 4-stage directional overcurrent function is provided, with the first stage programmable for inverse time or definite time operation. The second, third and fourth stages provide definite time operation.

The sensitive earth fault element includes a digital filter which rejects all harmonics other than the fundamental power system frequency.

The sensitive earth fault quantity is measured directly, using a dedicated core balance earth fault aCT.

This input can also be used in transformer restricted earth fault applications, by the use of external metrosils (varistors) and setting resistors.

The directional sensitive earth fault elements can be configured for directional operation in the same way as the standard earth fault pole, by polarising against the residual voltage. An additional

restraint on operation can be provided by a Residual Power element RP, for use in protection of power systems which utilise resonant (Petersen coil) earthing methods.

The SEF elements provide 20 times more sensitive setting ranges (10 mA to 1 A in 5A rating) than the regular earth fault protection.

Since very low levels of current setting may be applied, there is a danger of unwanted operation due to harmonics of the power system frequency, which can appear as residual current. Therefore the SEF elements operate only on the fundamental component, rejecting all higher harmonics.

The SEF protection is provided in Model 110 and 420 series which have a dedicated earth fault input circuit.

The element SEF1 provides inverse time or definite time selective two-stage overcurrent protection. Stage 2 of the two-stage overcurrent protection is used only for the standby earth fault protection. The SEF2 to SEF4 provide definite time overcurrent protection.

When SEF employs IEEE or USA inverse time characteristics, two reset modes are available: definite time or dependent time resetting. If the IEC inverse time characteristic is employed, definite time resetting is provided. For other characteristics, refer to Section 2.1.1.1.

In applications of SEF protection, it must be ensured that any erroneous zero-phase current is sufficiently low compared to the fault current, so that a highly sensitive setting is available.

The erroneous current may be caused with load current due to unbalanced configuration of the distribution lines, or mutual coupling from adjacent lines. The value of the erroneous current during normal conditions can be acquired on the metering screen of the relay front panel.

The earth fault current for SEF may be fed from a core balance CT, but if it is derived from three phase CTs, the erroneous current may be caused also by the CT error in phase faults. Transient false functioning may be prevented by a relatively long time delay.

Standby earth fault protection

The SEF is energised from a CT connected in the power transformer low voltage neutral, and the standby earth fault protection trips the transformer to backup the low voltage feeder protection, and ensures that the neutral earthing resistor is not loaded beyond its rating. Stage 1 trips the transformer low voltage circuit breaker, then stage 2 trips the high voltage circuit breaker(s) with a time delay after stage 1 operates.

The time graded tripping is valid for transformers connected to a ring bus, banked transformers and feeder transformers.

Restricted earth fault protection

The SEF elements can be applied in a high impedance restricted earth fault scheme (REF), for protection of a star-connected transformer winding whose neutral is earthed directly or through impedance.

As shown in Figure 2.1.26, the differential current between the residual current derived from the three-phase feeder currents and the neutral current in the neutral conductor is introduced into the SEF elements. Two external components, a stabilising resistor and a varistor, are connected as shown in the figure. The former increases the overall impedance of the relay circuit and stabilises the differential voltage, and the latter suppresses any overvoltage in the differential circuit.

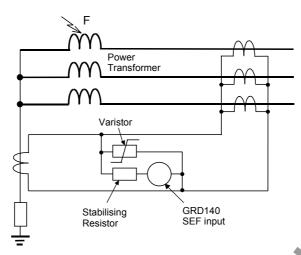


Figure 2.1.26 High Impedance REF

Scheme Logic

Figure 2.1.27 to 2.1.30 show the scheme logic of directional sensitive earth fault protection. The directional control characteristic can be selected to "FWD" or "REV" or "Non" by scheme switch setting [SE*-DIR].

Figure 2.1.27 shows the scheme logic of directional sensitive earth fault protection SEF1 with inverse time or definite time selective two-stage overcurrent protection. The definite time protection is selected by setting [MSE1] to "DT". The element SEF1 is enabled for sensitive earth fault protection and stage 1 trip signal SEF1 TRIP is given through the delayed pick-up timer TSE1. The inverse time protection is selected by setting [MSE1] to either "IEC", "IEEE", "US" or "CON" and then setting [MEF1C] according to the required IDMT characteristic. The element SEF1 is enabled and stage 1 trip signal SEF1 TRIP is given.

Both protections provide stage 2 trip signal SEF1-S2 through a delayed pick-up timer TSE12.

When the standby earth fault protection is applied by introducing earth current from the transformer low voltage neutral circuit, stage 1 trip signals are used to trip the transformer low voltage circuit breaker. If SEF1 continues operating after stage 1 has operated, the stage 2 trip signal can be used to trip the transformer high voltage circuit breaker(s).

SEF1HS (high speed) element is used for blocked overcurrent protection. See Section 2.1.3.6.

Figure 2.1.28 to Figure 2.1.30 show the scheme logic of the definite time sensitive earth fault protection SEF2 to SEF4. SEF2 to SEF4 give trip and alarm signals SEF2 TRIP, SEF3 TRIP and SEF4 ALARM through delayed pick-up timers TSE2, TSE3 and TSE4 respectively.

The signal SE1-INST to SE4-INST are available to trip instantaneously for a fault such as a reclose-on-to-a-fault. (See Section 2.5.)

The SEF1 to SEF4 protections can be disabled by the scheme switches [SE1EN] to [SE4EN] or binary input signals SEF1 BLOCK to SEF4 BLOCK. The SEF1 stage 2 trip of standby earth fault protection can be disabled by the scheme switch [SE1S2].

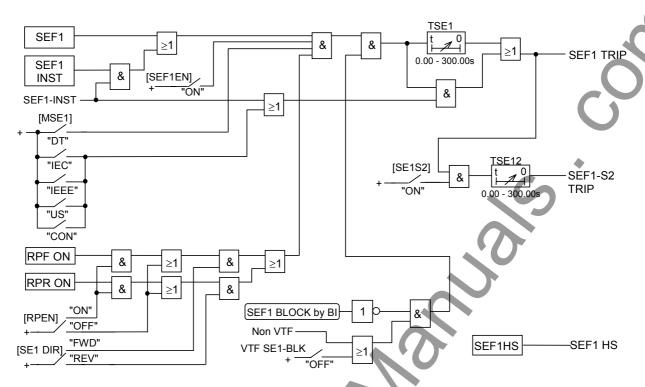


Figure 2.1.27 SEF1 Sensitive Earth Fault Protection Scheme Logic

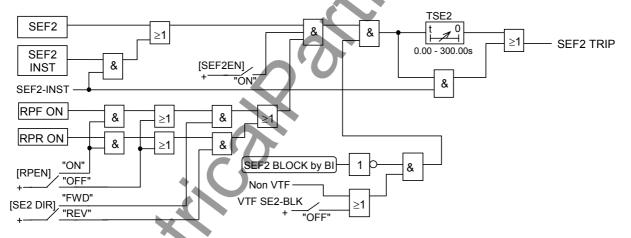


Figure 2.1.28 SEF2 Sensitive Earth Fault Protection Scheme Logic

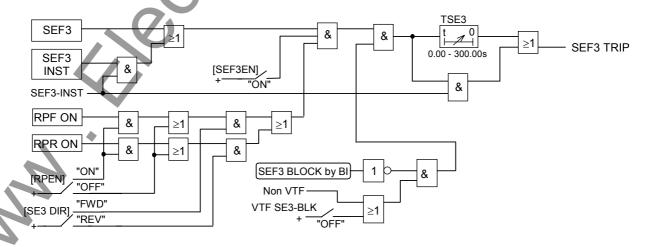


Figure 2.1.29 SEF3 Sensitive Earth Fault Protection Scheme Logic

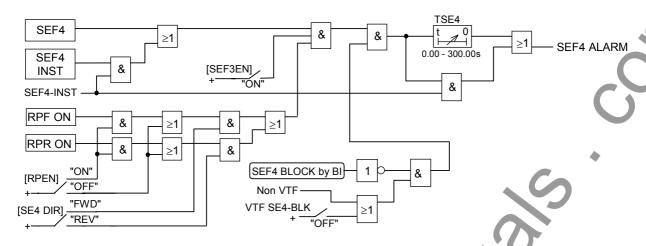


Figure 2.1.30 SEF4 Sensitive Definite Earth Fault Protection Scheme Logic

Setting

The table below shows the setting elements necessary for the sensitive earth fault protection and their setting ranges.

	842.			
Element	Range	Step	Default	Remarks
SEθ	−95° − 95°	1°	0°	SEF characteristic angle
SEV	0.5 – 100.0	0.1 V	3.0V	SEF ZPS voltage level
SE1	0.01 – 1.00 A (0.002 – 0.200 A)(*)	0.01 A (0.001 A)	0.05 A (0.010 A)	SEF1 threshold setting
TSE1M	0.010 – 1.500	0.001	1.000	SEF1 inverse time multiplier setting. Required if [MSE1] = IEC, IEEE or US.
TSE1	0.00 – 300.00 s	0.01 s	1.00 s	SEF1 definite time setting. Required if [MSE1] = DT.
TSE1R	0.0 – 300.0 s	0.1 s	0.0 s	SEF1 definite time delayed reset. Require if [MSE1] = IEC or [SE1R] = DEF.
TSE1RM	0.010 – 1.500	0.001	1.000	SEF1 dependent time delayed reset time multiplier. Required if [SE1R] = DEP.
TSE12	0.00 – 300.00 s	0.01 s	1.00 s	SEF1 stage 2 definite time setting
SE2	0.01 – 1.00 A (0.002 – 0.200 A)(*)	0.01 A (0.001 A)	0.05 A (0.010 A)	SEF2 threshold setting
TSE2	0.00 – 300.00 s	0.01 s	1.00 s	SEF2 definite time setting.
SE3	0.01 – 1.00 A (0.002 – 0.200 A)(*)	0.01 A (0.001 A)	0.05 A (0.010 A)	SEF3 threshold setting
TSE3	0.00 – 300.00 s	0.01 s	1.00 s	SEF3 definite time setting.
SE4	0.01 – 1.00 A (0.002 – 0.200 A)(*)	0.01 A (0.001 A)	0.05 A (0.010 A)	SEF4 threshold setting
TSE4	0.00 – 300.00 s	0.01 s	1.00 s	SEF4 definite time setting.
RP	0.00 - 100.00 W (0.00 - 20.00 W)(*)	0.01 W (0.01 W)	0.00 W (0.00 W)	Residual power sensitivity
[SE1EN]	Off / On		Off	SEF1 Enable
[SE1-DIR]	FWD / REV / NON		FWD	SEF1 directional characteristic

Element	Range	Step	Default	Remarks
[MSE1]	DT/IEC/IEEE/US/CON		DT	SEF1 characteristic
[MSE1C]				SEF1 inverse curve type.
MSE1C-IEC MSE1C-IEEE MSE1C-US	NI / VI / EI / LTI MI / VI / EI CO2 / CO8		NI MI CO2	Required if [MSE1] = IEC. Required if [MSE1] = IEEE. Required if [MSE1] = US.
[SE1R]	DEF / DEP		DEF	SEF1 reset characteristic. Required if [MSE1] = IEEE or US.
[SE1S2]	Off / On		Off	SEF1 stage 2 timer enable
[VTF-SE1BLK]	Off / On		Off	VTF block enable
[SE2EN]	Off / On		Off	SEF2 Enable
[SE2-DIR]	FWD / REV /NON		FWD	SEF2 directional characteristic
[VTF-SE2BLK]	Off / On		Off	VTF block enable
[SE3EN]	Off / On		Off	SEF3 Enable
[SE3-DIR]	FWD / REV / NON		FWD	SEF3 directional characteristic
[VTF-SE3BLK]	Off / On		Off	VTF block enable
[SE4EN]	Off / On		Off	SEF4 Enable
[SE4-DIR]	FWD / REV / NON		FWD	SEF4 directional characteristic
[VTF-SE4BLK]	Off / On	4	Off	VTF block enable
[RPEN]	Off / On		Off	Residual power block enable

^(*) Current values shown in parenthesis are in the case of a 1 A rating. Other current values are in the case of a 5 A rating.

SEF

SEF is set smaller than the available earth fault current and larger than the erroneous zero-phase current. The erroneous zero-phase current exists under normal conditions due to the unbalanced feeder configuration. The zero-phase current is normally fed from a core balance CT on the feeder, but if it is derived from three phase CTs, the erroneous current may be caused also by the CT error in phase faults.

The erroneous steady state zero-phase current can be acquired on the metering screen of the relay front panel.

Directional SEF

Directional SEF protection is commonly applied to unearthed systems, and to systems earthed by an inductance (Peterson Coil). Refer to appendix B for application guidance.

High impedance REF protection

CT saturation under through fault conditions results in voltage appearing across the relay circuit. The voltage setting of the relay circuit must be arranged such that it is greater than the maximum voltage that can occur under through fault conditions. The worst case is considered whereby one CT of the balancing group becomes completely saturated, while the others maintain linear operation. The excitation impedance of the saturated CT is considered to approximate a short-circuit.

Figure 2.1.31 Maximum Voltage under Through Fault Condition

The voltage across the relay circuit under these conditions is given by the equation:

$$V_S = I_F \times (R_{CT} + R_L)$$

where:

 V_S = critical setting voltage (rms)

 I_F = maximum prospective secondary through fault current (rms)

 $R_{CT} = CT$ secondary winding resistance

 R_L = Lead resistance (total resistance of the loop from the saturated CT to the relaying point)

A series stabilising resistor is used to raise the voltage setting of the relay circuit to V_S . No safety margin is needed since the extreme assumption of unbalanced CT saturation does not occur in practice. The series resistor value, R_S , is selected as follows:

$$R_S = V_S / I_S$$

 $I_{\rm S}$ is the current setting (in secondary amps) applied to the GRD140 relay. However, the actual fault setting of the scheme includes the total current flowing in all parallel paths. That is to say that the actual primary current for operation, after being referred to the secondary circuit, is the sum of the relay operating current, the current flowing in the varistor, and the excitation current of all the parallel connected CTs at the setting voltage. In practice, the varistor current is normally small enough that it can be neglected. Hence:

$$I_{S} \leq I_{P}/N - 4I_{mag}$$

where:

 I_S = setting applied to GRD140 relay (secondary amps)

 I_P = minimum primary current for operation (earth fault sensitivity)

N = CT ratio

 $I_{max} = CT$ magnetising (excitation) current at voltage V_S

More sensitive settings for I_S allow for greater coverage of the transformer winding, but they also require larger values of R_S to ensure stability, and the increased impedance of the differential circuit can result in high voltages being developed during internal faults. The peak voltage, V_{pk} , developed may be approximated by the equation:

$$V_{pk} = 2 \times \sqrt{2 \times V_k \times (I_F R_S - V_k)}$$

where:

 $V_k = CT$ knee point voltage

 I_F = maximum prospective secondary current for an internal fault

When a Metrosil is used for the varistor, it should be selected with the following characteristics:

 $V = CI^{\beta}$

where:

V = instantaneous voltage

I = instantaneous current

 β = constant, normally in the range 0.20 - 0.25

C = constant.

The C value defines the characteristics of the metrosil, and should be chosen according to the following requirements:

- 1. The current through the metrosil at the relay voltage setting should be as low as possible, preferably less than 30mA for a 1Amp CT and less than 100mA for a 5Amp CT.
- 2. The voltage at the maximum secondary current should be limited, preferably to 1500Vrms.

Restricted earth fault schemes should be applied with high accuracy CTs whose knee point voltage V_k is chosen according to the equation:

$$V_k \ge 2 \times V_S$$

where V_S is the differential stability voltage setting for the scheme.

2.1.3.5 Negative Sequence Overcurrent Protection

The negative sequence overcurrent protection (NOC) is used to detect asymmetrical faults (phase-to-phase and phase-to-earth faults) with high sensitivity in conjunction with phase overcurrent protection and residual overcurrent protection. It also used to detect load unbalance conditions.

Phase overcurrent protection must be set to lower sensitivity when the load current is large but NOC sensitivity is not affected by magnitude of the load current, except in the case of erroneous negative sequence current due to the unbalanced configuration of the distribution lines.

For some earth faults, only a small zero sequence current is fed while the negative sequence current is comparatively larger. This is probable when the fault occurs at the remote end with a small reverse zero sequence impedance and most of the zero sequence current flows to the remote end

In these cases, NOC backs up the phase overcurrent and residual overcurrent protection. The NOC also protects the rotor of a rotating machine from over heating by detecting a load unbalance. Unbalanced voltage supply to a rotating machine due to a phase loss can lead to increases in the negative sequence current and in machine heating.

GRD140 provides the directional negative sequence overcurrent protection with definite time characteristics.

Two independent elements NOC1 and NOC2 are provided for tripping and alarming. These elements can be directionalised by polarising against the negative sequence voltage.

The NOC protection is enabled when three-phase current is introduced and the scheme switch [APPL-CT] is set to "3P".

Scheme Logic

Figure 2.1.32 and 2.1.33 show the scheme logic of directional negative sequence overcurrent protection NOC1 and NOC2. The directional control characteristic can be selected to "Forward"

or "Reverse" or "Non" by scheme switch setting [NC1-DIR] and [NC2-DIR] (not shown in Figures 2.1.32 and 2.1.33).

In Figures 2.1.32 and 2.1.33, the NOC1 and NOC2 gives a trip signal NOC1 TRIP and an alarm signal NOC2 ALARM through delayed pick-up timers TNC1 and TNC2.

When the VTFS or CTFS detects a VT failure or a CT failure, it can alarm and block the NC1 and NC2 protection by the scheme switch [VTF NC1-BLK] and [VTF NC2-BLK] or [CTF NC1-BLK] and [CTF NC2-BLK] respectively.

The NC1 and NC2 protection can be disabled by the scheme switches [NC1EN], [NC2EN] and [APPL-CT] or the binary input signals NC1 BLOCK and NC2 BLOCK respectively.

The scheme switch [APPL-CT] is available in which three-phase overcurrent protection can be selected. The NOC protection is enabled when three-phase current is introduced and [APPL-CT] is set to "3P".

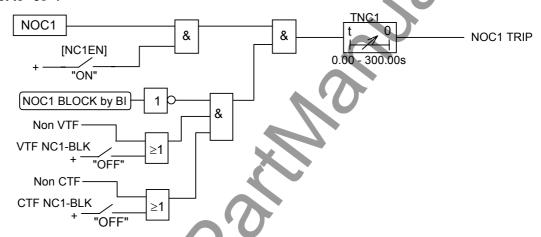


Figure 2.1.32 Negative Sequence Overcurrent Protection NOC1 Scheme Logic

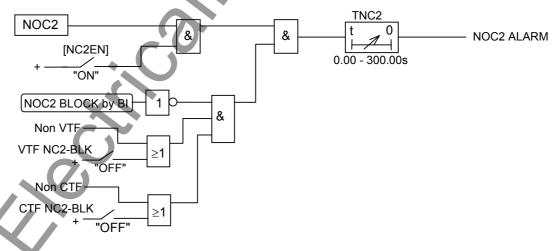


Figure 2.1.33 Negative Sequence Overcurrent Protection NOC2 Scheme Logic

Setting

The table below shows the setting elements necessary for the NOC protection and their setting ranges.

Element	Range	Step	Default	Remarks
NCθ	−95° − 95°	1°	−45°	NOC characteristic angle
NCV	0.5 – 25.0 V	0.1 V	3.0 V	NOC NPS voltage level

NC1	0.5 – 10.0 A (0.10 – 2.00 A)(*)	0.1 A (0.01 A)	2.0 A (0.40 A)	NOC1 threshold setting.
TNC1	0.00 – 300.00 s	0.01 s	1.00 s	NOC1 definite time setting. Required if [MNC1] = DT.
TNC1M	0.010 – 1.500	0.001	1.000	NOC1 time multiplier setting. Required if [MNC1] = IEC, IEEE or US.
TNC1R	0.0 – 300.0 s	0.1 s	0.0 s	NOC1 definite time delayed reset. Required if [NC1R] = DEF.
TNC1RM	0.010 – 1.500	0.001	1.000	NC1 dependent time delayed reset time multiplier. Required if [NC1R] = DEP.
NC2	0.5 - 10.0 A (0.10 – 2.00 A)	0.1 A (0.01 A)	1.0 A (0.20 A)	NOC2 threshold setting.
TNC2	0.00 - 300.00 s	0.01 s	1.00 s	NOC2 definite time setting
[NC1EN]	Off / On		Off	NOC1 Enable
[MNC1C]				NOC1 inverse curve type.
MNC1C-IEC	NI / VI / EI / LTI		NI	Required if [MNC1] = IEC.
MNC1C-IEEE MNC1C-US	MI / VI / EI CO2 / CO8		MI CO2	Required if [MNC1] = IEEE. Required if [MNC1] = US.
[NC1R]	DEF / DEP		DEF	NOC1 reset characteristic. Required if [MNC1] = IEEE or US.
[CTF-NC1BLK]	Off / On	4	Off	CTF block enable for NOC1
[VTF-NC1BLK]	Off / On		Off	VTF block enable for NOC1
[NC2EN]	Off / On	10	Off	NOC2 Enable
[CTF-NC2BLK]	Off / On		Off	CTF block enable for NOC2
[VTF-NC2BLK]	Off / On		Off	VTF block enable for NOC2
[APPL-CT]	3P / 2P / 1P	•	3P	Three-phase current input

^(*) Current values shown in the parenthesis are in the case of a 1 A rating. Other current values are in the case of a 5 A rating.

Sensitive setting of NOC1 and NOC2 thresholds is restricted by the negative phase sequence current normally present on the system. The negative phase sequence current is measured in the relay continuously and displayed on the metering screen of the relay front panel along with the maximum value. It is recommended to check the display at the commissioning stage and to set NOC1 and NOC2 to 130 to 150% of the maximum value displayed.

The delay time setting TNC1 and TNC2 is added to the inherent delay of the measuring elements NOC1 and NOC2. The minimum operating time of the NOC elements is around 200ms.

Under fault conditions, the negative sequence current lags the negative sequence voltage by an angle dependent on the negative sequence source impedance of the system. This should be accounted for by setting the NOC characteristic angle setting [NC θ] when the negative sequence protection is used in directional mode. Typical settings are as follows:

- -60° for transmission systems
- +45° for distribution systems

2.1.3.6 Application of Protection Inhibits

All GRD140 protection elements can be blocked by a binary input signal. This feature is useful in a number of applications.

Blocked Overcurrent Protection

Conventional time-graded definite time overcurrent protection can lead to excessive fault clearance times being experienced for faults closest to the source. The implementation of a blocked overcurrent scheme can eliminate the need for grading margins and thereby greatly reduce fault clearance times. Such schemes are suited to radial feeder circuits, particularly where substations are close together and pilot cables can be economically run between switchboards.

Figure 2.1.34 shows the operation of the scheme.

Instantaneous phase fault and earth fault pick-up signals OC1HS, EF1HS and SEF1HS of OC1, EF1 and SEF1 elements are allocated to any of the binary output relays and used as a blocking signal. OC2, EF2 and SEF2 protections are set with a short delay time. (For pick-up signals, refer to Figure 2.1.16, 2.1.20 and 2.1.27.)

For a fault at F as shown, each relay sends the blocking signal to its upstream neighbor. The signal is input as a binary input signal OC2 BLOCK, EF2 BLOCK and SEF2 BLOCK at the receiving end, and blocks the OC2, EF2 and SEF2 protection. Minimum protection delays of 50ms are recommended for the OC2, EF2 and SEF2 protection, to ensure that the blocking signal has time to arrive before protection operation.

Inverse time graded operation with elements OC1, EF1 and SEF1 are available with the scheme switch [MOC1], [MEF1] and [MSE1] setting, thus providing back-up protection in the event of a failure of the blocked scheme.

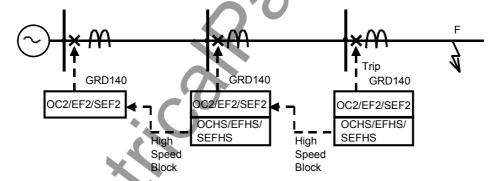


Figure 2.1.34 Blocked Overcurrent Protection

Blocked Busbar Protection

Non-directional overcurrent protection can be applied to provide a busbar zone scheme for a simple radial system where a substation has only one source, as illustrated in Figure 2.1.35.

For a fault on an outgoing feeder F1, the feeder protection sends a hardwired blocking signal to inhibit operation of the incomer, the signal OCHS, EFHS and SEFHS being generated by the instantaneous phase fault, and earth fault pick-up outputs of OC1, EF1 and SEF1 allocated to any of the binary output relays. Meanwhile, the feeder is tripped by the OC1, EF1 and SEF1 elements, programmed with inverse time or definite time delays and set to grade with downstream protections.

The incomer protection is programmed to trip via its instantaneous elements OC2, EF2 and SEF2 set with short definite time delay settings (minimum 50ms), thus providing rapid isolation for faults in the busbar zone F2.

At the incomer, inverse time graded operation with elements OC1, EF1 and SEF1 are available with the scheme switch [MOC1], [MEF1] and [MSE1] setting, thus providing back-up protection in the event of failure of the blocked scheme.

GRD140 integrated circuit breaker failure protection can be used to provide additional back-trips from the feeder protection to the incomer, and from the incomer to the HV side of the power transformer, in the event of the first trip failing to clear the earth fault.

In the case of more complex systems where the substation has two incomers, or where power can flow into the substation from the feeders, then directional protection must be applied.

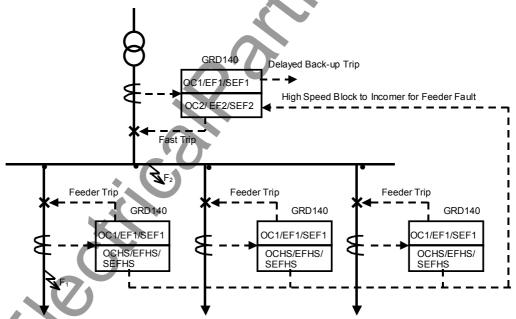


Figure 2.1.35 Blocked Busbar Protection Scheme 1

Figure 2.1.36 shows one half of a two-incomer station. A directional overcurrent relay protects the incomer, with non-directional overcurrent units on the feeders.

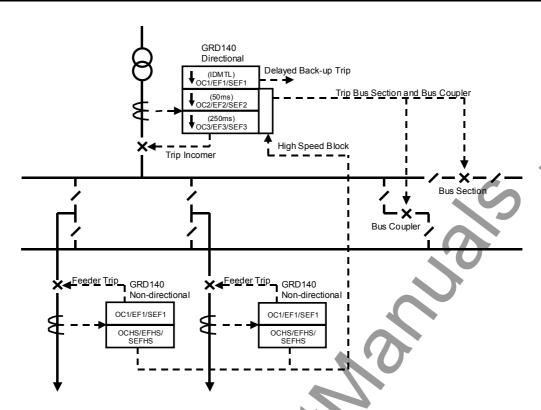


Figure 2.1.36 Blocked Busbar Protection Scheme 2

For a fault on an outgoing feeder, the non-directional feeder protection sends a hardwired blocking signal to inhibit operation of both incomers, the signal OCHS, EFHS and SEFHS being generated by the instantaneous phase fault and earth fault pick-up outputs. Meanwhile, the feeder is tripped by the OC1, EF1 and SEF1 elements, programmed with inverse time delays and set to grade with downstream protections.

The incomer protection is programmed for directional operation such that it will only trip for faults on the busbar side of its CTs. Hence, although a fault on the HV side may be back-fed from the busbars, the relay does not trip.

For a fault in the busbar zone, the GRD140 is programmed to trip the bus section and bus coupler circuit breakers via its instantaneous elements OC2, EF2 and SEF2 set with short definite time delay settings (minimum 50ms). This first stage trip maintains operation of half the substation in the event of a busbar fault or incomer fault in the other half.

If the first stage trip fails to clear the fault, a second stage trip is given to the local incomer circuit breaker via instantaneous elements OC3, EF3 and SEF3 after a longer delay, thus isolating a fault on the local busbar.

GRD140 integrated circuit breaker fail protection can be used to provide additional back-trips from the feeder protection to the incomer, and from the incomer to the HV side of the power transformer, in the event of the main trip failing to clear the fault.

A further development of this scheme might see directional relays being applied directly to the bus section and bus coupler circuit breakers, to speed up operation of the scheme.

This scheme assumes that a busbar fault cannot be fed from the outgoing feeder circuits. In the case of an interconnected system, where a remote power source may provide a back-feed into the substation, directional relays must also be applied to protect the feeders.

2.1.4 Phase Undercurrent Protection

The phase undercurrent protection is used to detect a decrease in current caused by a loss of load, typically motor load. Two stage undercurrent protection UC1 and UC2 are available.

The undercurrent element operates for current falling through the threshold level. But the operation is blocked when the current falls below 4 % of CT secondary rating to discriminate the loss of load from the feeder tripping by other protection. Figure 2.4.37 shows the undercurrent element characteristic.

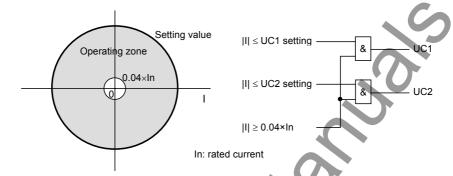


Figure 2.1.37 Undercurrent Element Characteristic

Each phase has two independent undercurrent elements for tripping and alarming. The elements are programmable for instantaneous or definite time delayed operation.

The undercurrent element operates on per phase basis, although tripping and alarming is three-phase only.

Scheme Logic

Figure 2.1.38 shows the scheme logic of the phase undercurrent protection.

The undercurrent elements UC1 and UC2 output UC1 TRIP and UC2 ALARM through delayed pick-up timers TUC1 and TUC2.

This protection can be disabled by the scheme switch [UC1EN] and [UC2EN] or binary input signals UC1 BLOCK and UC2 BLOCK.

Further, this protection can be blocked when CT failure (CTF) is detected.

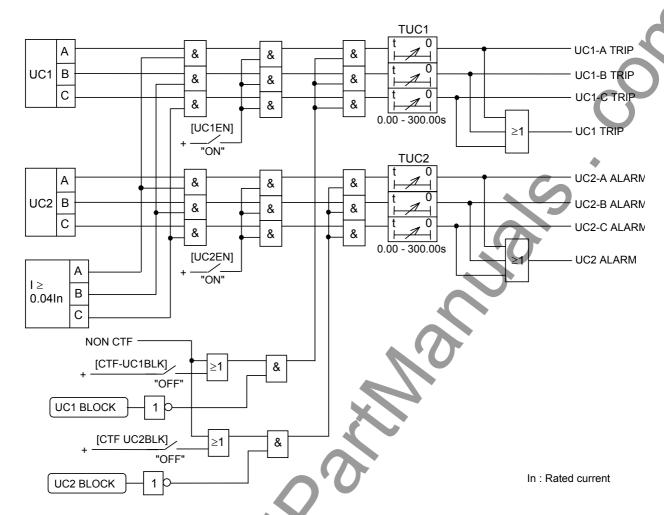


Figure 2.1.38 Undercurrent Protection Scheme Logic

Setting

The table below shows the setting elements necessary for the undercurrent protection and their setting ranges.

Element	Range	Step	Default	Remarks
UC1	0.5 – 10.0 A (0.10 – 2.00 A)(*)	0.1 A (0.01 A)	1.0 A (0.20 A)	UC1 threshold setting
TUC1	0.00 – 300.00 s	0.01 s	1.00 s	UC1 definite time setting
UC2	0.5 – 10.0 A (0.10 – 2.00 A)	0.1 A (0.01 A)	2.0 A (0.40 A)	UC2 threshold setting
TUC2	0.00 - 300.00 s	0.01 s	1.00 s	UC2 definite time setting
[UC1EN]	Off / On		Off	UC1 Enable
[UC2EN]	Off / On		Off	UC2 Enable
[CTF-UC1BLK]	Off / On		Off	UC1 CTF block
[CTF-UC2BLK]	Off / On		Off	UC2 CTF block

^(*) Current values shown in parenthesis are in the case of a 1 A rating. Other current values are in the case of a 5 A rating.

2.1.5 Thermal Overload Protection

The temperature of electrical plant rises according to an I²t function and the thermal overload protection in GRD140 provides a good protection against damage caused by sustained overloading. The protection simulates the changing thermal state in the plant using a thermal model.

The thermal state of the electrical system can be shown by equation (1).

$$\theta = \frac{I^2}{I_{AOL}^2} \left(1 - e^{-t/\tau} \right) \times 100\% \tag{1}$$

where:

 θ = thermal state of the system as a percentage of allowable thermal capacity,

I = applied load current,

 I_{AOL} = allowable overload current of the system,

 τ = thermal time constant of the system.

The thermal state 0% represents the cold state and 100% represents the thermal limit, which is the point at which no further temperature rise can be safely tolerated and the system should be disconnected. The thermal limit for any given system is fixed by the thermal setting I_{AOL} . The relay gives a trip output when $\theta = 100\%$.

The thermal overload protection measures the largest of the three phase currents and operates according to the characteristics defined in IEC60255-8. (Refer to Appendix A for the implementation of the thermal model for IEC60255-8.)

Time to trip depends not only on the level of overload, but also on the level of load current prior to the overload - that is, on whether the overload was applied from 'cold' or from 'hot'.

Independent thresholds for trip and alarm are available.

The characteristic of the thermal overload element is defined by equation (2) and equation (3) for 'cold' and 'hot'. The cold curve is a special case of the hot curve where prior load current Ip is zero, catering to the situation where a cold system is switched on to an immediate overload.

$$t = \tau \cdot Ln \left[\frac{I^2}{I^2 - I_{AOL}^2} \right]$$
 (2)

$$t = \tau \cdot Ln \left[\frac{\mathbf{I}^2 - \mathbf{I}_p^2}{\mathbf{I}^2 - \mathbf{I}_{AOL}^2} \right]$$
 (3)

where

t = time to trip for constant overload current I (seconds)

I = overload current (largest phase current) (amps)

 I_{AOL} = allowable overload current (amps)

 I_P = previous load current (amps)

 τ = thermal time constant (seconds)

Ln = natural logarithm

Figure 2.1.39 illustrates the IEC60255-8 curves for a range of time constant settings. The left-hand chart shows the 'cold' condition where an overload has been switched onto a previously un-loaded system. The right-hand chart shows the 'hot' condition where an overload is switched onto a

system that has previously been loaded to 90% of its capacity.

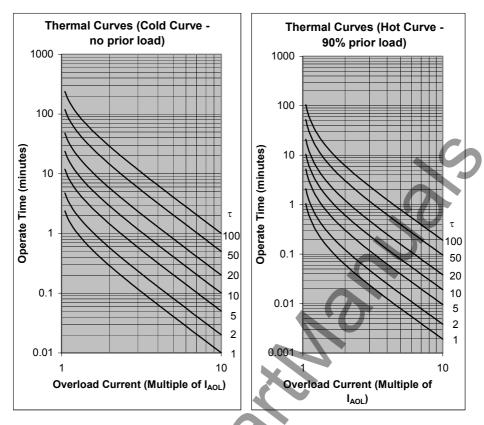


Figure 2.1.39 Thermal Curves

Scheme Logic

Figure 2.1.40 shows the scheme logic of the thermal overload protection.

The thermal overload element THM has independent thresholds for alarm and trip, and outputs alarm signal THM ALARM and trip signal THM TRIP. The alarming threshold level is set as a percentage of the tripping threshold.

The alarming and tripping can be disabled by the scheme switches [THMAEN] and [THMEN] respectively or binary input signals THMA BLOCK and THM BLOCK.

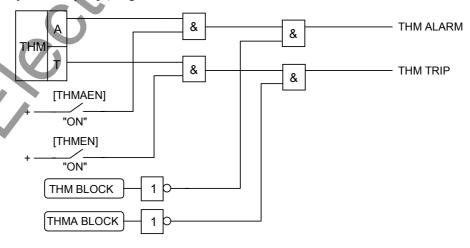


Figure 2.1.40 Thermal Overload Protection Scheme Logic

Setting

The table below shows the setting elements necessary for the thermal overload protection and their setting ranges.

Element	Range	Step	Default	Remarks
THM	2.0 – 10.0 A (0.40 – 2.00 A)(*)	0.1 A (0.01 A)	5.0 A (1.00 A)	Thermal overload setting. (THM = I _{AOL} : allowable overload current)
THMIP	0.0 – 5.0 A (0.00 – 1.00 A)(*)	0.1 A (0.01 A)	0.0 A (0.00 A)	Previous load current
TTHM	0.5 - 100.0 min	0.1 min	10.0 min	Thermal time constant
THMA	50 – 99 %	1 %	80 %	Thermal alarm setting. (Percentage of THM setting.)
[THMEN]	Off / On		Off	Thermal OL enable
[THMAEN]	Off / On		Off	Thermal alarm enable

^(*) Current values shown in the parenthesis are in the case of a 1 A rating. Other current values are in the case of a 5 A rating.

Note: THMIP sets a minimum level of previous load current to be used by the thermal element, and is typically used when testing the element. For the majority of applications, THMIP should be set to its default value of zero, in which case the previous load current, Ip, is calculated internally by the thermal model, providing memory of conditions occurring before an overload.

2.1.6 Broken Conductor Protection

Series faults or open circuit faults which do not accompany any earth faults or phase faults are caused by broken conductors, breaker contact failure, operation of fuses, or false operation of single-phase switchgear.

Figure 2.1.41 shows the sequence network connection diagram in the case of a single-phase series fault assuming that the positive, negative and zero sequence impedance of the left and right side system of the fault location is in the ratio of k_1 to $(1 - k_1)$, k_2 to $(1 - k_2)$ and k_0 to $(1 - k_0)$.

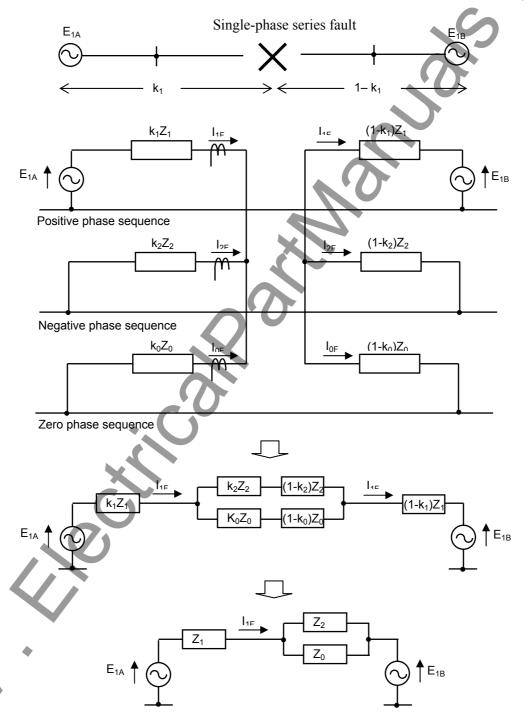


Figure 2.1.41 Equivalent Circuit for a Single-phase Series Fault

Positive phase sequence current I_{1F}, negative phase sequence current I_{2F} and zero phase sequence

current I_{0F} at fault location in an single-phase series fault are given by:

$$I_{1F} + I_{2F} + I_{0F} = 0$$
 (1)

$$Z_{2F}I_{2F} - Z_{0F}I_{0F} = 0 (2)$$

$$E_{1A} - E_{1B} = Z_{1F}I_{1F} - Z_{2F}I_{2F}$$
 (3)

where,

 E_{1A} , E_{1B} : power source voltage

 Z_1 : positive sequence impedance

Z₂: negative sequence impedance

Z₀: zero sequence impedance

From the equations (1), (2) and (3), the following equations are derived.

$$I_{1F} = \frac{Z_2 + Z_0}{Z_1 Z_2 + Z_1 Z_0 + Z_2 Z_0} (E_{1A} - E_{1B})$$

$$I_{2F} = \frac{-Z_0}{Z_1 Z_2 + Z_1 Z_0 + Z_2 Z_0} \left(E_{1A} - E_{1B} \right)$$

$$I_{0F} = \frac{-Z_2}{Z_1 Z_2 + Z_1 Z_0 + Z_2 Z_0} (E_{1A} - E_{1B})$$

The magnitude of the fault current depends on the overall system impedance, difference in phase angle and magnitude between the power source voltages behind both ends.

Broken conductor protection element BCD detects series faults by measuring the ratio of negative to positive phase sequence currents (I_{2F}/I_{1F}). This ratio is given with negative and zero sequence impedance of the system:

$$\frac{I_{2F}}{I_{1F}} = \frac{|I_{2F}|}{|I_{1F}|} = \frac{Z_0}{Z_2 + Z_0}$$

The ratio is higher than 0.5 in a system when the zero sequence impedance is larger than the negative sequence impedance. It will approach 1.0 in a high-impedance earthed or a one-end earthed system.

The characteristic of BCD element is shown in Figure 2.1.42 to obtain the stable operation.

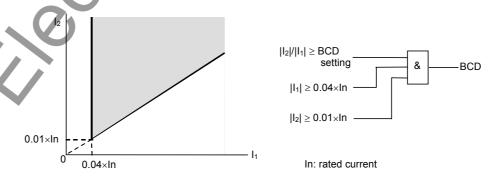


Figure 2.1.42 BCD Element Characteristic

Scheme Logic

Figure 2.1.43 shows the scheme logic of the broken conductor protection. BCD element outputs trip signals BCD TRIP through a delayed pick-up timer TBCD.

The tripping can be disabled by the scheme switch [BCDEN], [APPL] or binary input signal BCD BLOCK. The scheme switch [APPL-CT] is available in Model 400 and 420 in which three-phase or two-phase phase overcurrent protection can be selected. The broken conductor protection is enabled when three-phase current is introduced and [APPL-CT] is set to "3P" in those models.

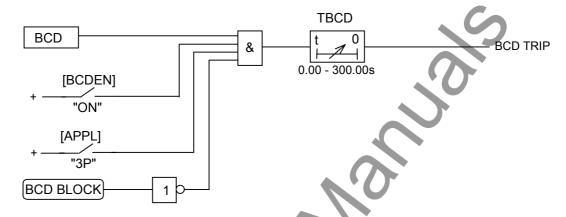


Figure 2.1.43 Broken Conductor Protection Scheme Logic

Settings

The table below shows the setting elements necessary for the broken conductor protection and their setting ranges.

Element	Range	Step	Default	Remarks
BCD	0.10 – 1.00	0.01	0.20	l ₂ / l ₁
TBCD	0.00 - 300.00s	0.01s	0.00 s	BCD definite time setting
[BCDEN]	Off / On		Off	BCD Enable
[APPL-CT]	3P / 2P / 1P		3P	Three-phase current input. Only required in Model 400 and 420.

Minimum setting of the BC threshold is restricted by the negative phase sequence current normally present on the system. The ratio I_2/I_1 of the system is measured in the relay continuously and displayed on the metering screen of the relay front panel, along with the maximum value of the last 15 minutes I_{21} max. It is recommended to check the display at the commissioning stage. The BCD setting should be 130 to 150% of I_2/I_1 displayed.

Note. It must be noted that I_2 / I_1 is displayed only when the positive phase sequence current (or load current) in the secondary circuit is larger than 2 % of the rated secondary circuit current.

TBCD should be set to more than 1 cycle to prevent unwanted operation caused by a transient operation such as CB closing.

2.1.7 Breaker Failure Protection

When fault clearance fails due to a breaker failure, the breaker failure protection (BFP) clears the fault by backtripping adjacent circuit breakers.

If the current continues to flow even after a trip command is output, the BFP judges it as a breaker failure. The existence of the current is detected by an overcurrent element CBF provided for each phase. For high-speed operation of the BFP, a high-speed reset overcurrent element (less than 20ms) is used. The CBF element resets when the current falls below 80% of the operating value as shown in Figure 2.1.44.

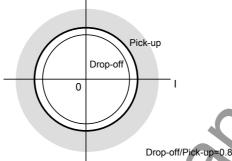


Figure 2.1.44 CBF element Characteristic

In order to prevent the BFP from starting by accident during maintenance work and testing, and thus tripping adjacent breakers, the BFP has the optional function of retripping the original breaker. To make sure that the breaker has actually failed, a trip command is made to the original breaker again before tripping the adjacent breakers to prevent unnecessary tripping of the adjacent breakers following the erroneous start-up of the BFP. It is possible to choose not to use retripping at all, or use retripping with trip command plus delayed pick-up timer, or retripping with trip command plus overcurrent detection plus delayed pick-up timer.

An overcurrent element and delayed pick-up timer are provided for each phase which also operate correctly during the breaker failure routine in the event of an evolving fault.

Scheme logic

The BFP initiation is performed on per-phase basis. Figure 2.1.45 shows the scheme logic for the BFP. The BFP is started by per-phase base trip signals EXT TRIP-APH to EXT TRIP-CPH or three-phase base trip signal EXT TRIP-3PH by binary inputs. These trip signals must continuously exist as long as the fault is present.

The backtripping signal to the adjacent breakers CBF TRIP is output if the overcurrent element CBF operates continuously for the setting time of the delayed pick-up timer TBTC after initiation. Tripping of adjacent breakers can be blocked with the scheme switch [BTC].

There are two kinds of modes of the retrip signal to the original breaker CBF RETRIP, the mode in which retrip is controlled by the overcurrent element CBF, and the direct trip mode in which retrip is not controlled. The retrip mode together with the trip block can be selected with the scheme switch [RTC]. In the scheme switch [RTC], "DIR" is the direct trip mode, and "OC" is the trip mode controlled by the overcurrent element CBF.

Figure 2.1.46 shows a sequence diagram for the BFP when a retrip and backup trip are used. If the circuit breaker trips normally, the CBF is reset before timer TRTC or TBTC is picked up and the BFP is reset. As TRTC and TBTC start at the same time, the setting value of TBTC should include that of TRTC.

If the CBF continues to operate, a retrip command is given to the original breaker after the setting time of TRTC. Unless the breaker fails, the CBF is reset by retrip. TBTC does not time-out and the BFP is reset. This sequence of events may happen if the BFP is initiated by mistake and

unnecessary tripping of the original breaker is unavoidable.

If the original breaker fails, retrip has no effect and the CBF continues operating and the TBTC finally picks up. A trip command CBF TRIP is given to the adjacent breakers and the BFP is completed.

The BFP protection can be disabled by the scheme switches [BTC] and [RTC] or the binary input signal CBF BLOCK.

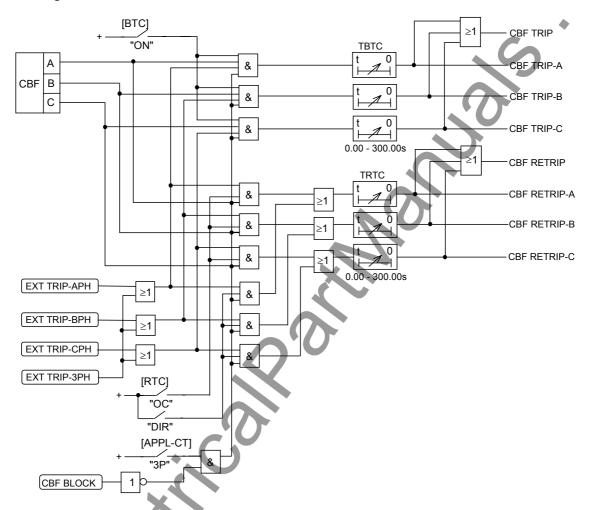


Figure 2.1.45 Breaker Failure Protection Scheme Logic

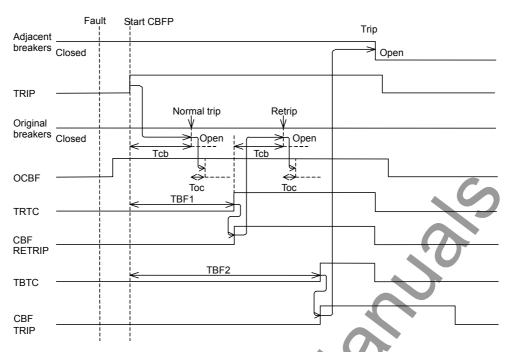


Figure 2.1.46 Sequence Diagram

Setting

The setting elements necessary for the breaker failure protection and their setting ranges are as follows:

Element	Range	Step	Default	Remarks
CBF	0.5 – 10.0 A	0.1 A	2.5 A	Overcurrent setting
	(0.10 - 2.00 A)(*)	(0.01 A)	(0.50 A)	
TRTC	0.00 - 300.00 s	0.01 s	0.40 s	Retrip time setting
TBTC	0.00 – 300.00 s	0.01 s	0.50 s	Back trip time setting
[RTC]	Off / DIR / OC		Off	Retrip control
[BTC]	Off / On		Off	Back trip control

^(*) Current values shown in the parentheses are in the case of 1 A rating. Other current values are in the case of 5 A rating.

The overcurrent element CBF checks that the circuit breaker has opened and that the current has disappeared. Therefore, since it is allowed to respond to load current, it can be set to 10 to 200% of the rated current.

The settings of TRTC and TBTC are determined by the opening time of the original circuit breaker (Teb in Figure 2.1.46) and the reset time of the overcurrent element (Toc in Figure 2.1.46). The timer setting example when using retrip can be obtained as follows.

If retrip is not used, the setting of the TBTC can be the same as the setting of the TRTC.

2.1.8 Cold Load Protection

GRD140 provides cold load protection to prevent incorrect operation from a magnetising inrush current during transformer energisation.

In normal operation, the load current on the distribution line is smaller than the sum of the rated loads connected to the line. But it amounts to several times the maximum load current for a moment when all of the loads are energised at once after a long interruption, and decreases to 1.5 times normal peak load after three or four seconds.

To protect those lines with overcurrent element, it is necessary to use settings to discriminate the inrush current in cold load restoration and the fault current.

This function modifies the overcurrent protection settings for a period after closing on to the type of load that takes a high level of load on energisation. This is achieved by a 'Cold Load Setting', in which the user can program alternative setting. Normally the user will choose higher current settings within this setting.

A state transition diagram and its scheme logic are shown in Figure 2.1.47 and Figure 2.1.48 for the cold load protection. Note that the scheme requires the use of two binary inputs assigned by PLC function, one each for CB OPEN and CB CLOSED.

Under normal conditions, where the circuit breaker has been closed for some time, the scheme is in STATE 0, and the normal default setting is applied to the overcurrent protection.

If the circuit breaker opens then the scheme moves to STATE 1 and runs the Cold Load Enable timer TCLE. If the breaker closes again while the timer is running, then STATE 0 is re-entered. Alternatively, if TCLE expires then the load is considered cold and the scheme moves to STATE 2, and stays there until the breaker closes, upon which it goes to STATE 3.

In STATE 2 and STATE 3, the 'Cold Load Setting' is applied.

In STATE 3 the Cold Load Reset timer TCLR runs. If the circuit breaker re-opens while the timer is running then the scheme returns to STATE 2. Alternatively, if TCLR expires then it goes to STATE 0, the load is considered warm and normal settings can again be applied.

Accelerated reset of the cold load protection is also possible. In STATE 3, the phase currents are monitored by overcurrent element ICLDO and if all phase currents drop below the ICLDO threshold for longer than the cold load drop off time (TCLDO) then the scheme automatically reverts to STATE 0. The accelerated reset function can be enabled with the scheme switch [CLDOEN] setting.

Cold load protection can be disabled by setting [CLEN] to "Off".

To test the cold load protection function, the switch [CLPTST] is provided to set the STATE 0 or STATE 3 condition forcibly.

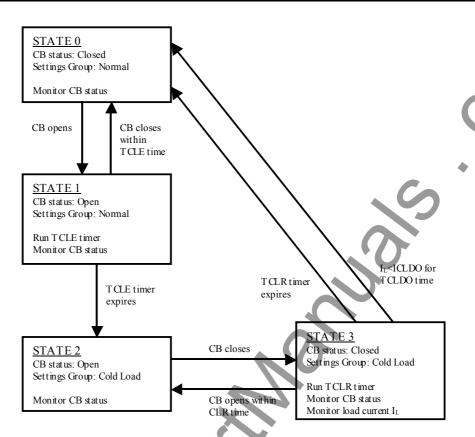


Figure 2.1.47 State Transition Diagram for Cold Load Protection

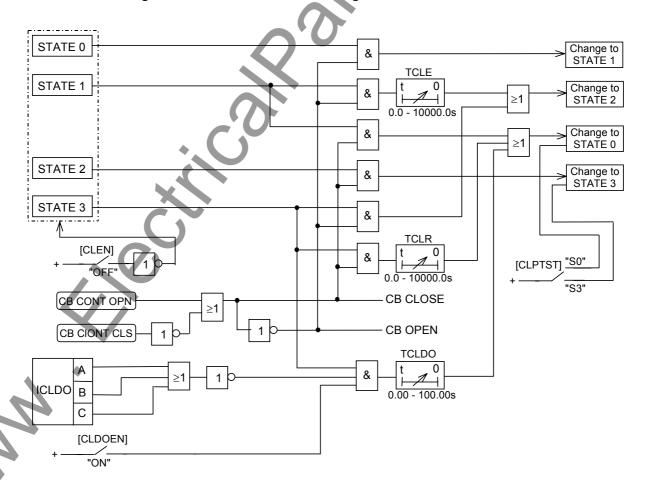


Figure 2.1.48 Scheme Logic for Cold Load Protection

Setting

The setting elements necessary for the cold load protection and their setting ranges are as follows:

Element	Range	Step	Default	Remarks
ICLDO	0.5 – 10.0 A (0.10 - 2.00 A)(*)	0.1 A (0.01 A)	2.5 A (0.50 A)	Cold load drop-off threshold setting
TCLE	0-10000 s	1 s	100 s	Cold load enable timer
TCLR	0-10000 s	1 s	100 s	Cold load reset timer
TCLDO	0.00-100.00 s	0.01 s	0.00 s	Cold load drop-off timer
[CLEN]	Off / On		Off	Cold load protection enable
[CLDOEN]	Off / On		Off	Cold load drop-off enable

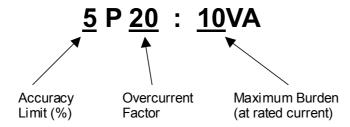
^(*) Current values shown in the parentheses are in the case of a 1 A rating. Other current values are in the case of a 5 A rating.

Further, other element settings (OC1 to OC4, EF1 to EF4, SEF1 to SEF4, NOC1, NOC2 and BCD) are required for the cold load protection.

2.1.9 CT Requirements

2.1.9.1 Phase Fault and Earth Fault Protection

Protection class current transformers are normally specified in the form shown below. The CT transforms primary current within the specified accuracy limit, for primary current up to the overcurrent factor, when connected to a secondary circuit of the given burden.



Accuracy limit: Typically 5 or 10%. In applications where current grading is to be applied and small grading steps are desirable, then a 5% CT can assist in achieving the necessary accuracy. In less onerous applications, a limit of 10% may be acceptable.

Overcurrent factor: The multiple of the CT rating up to which the accuracy limit is claimed, typically 10 or 20 times. A value of 20 should be specified where maximum fault current is high and accurate inverse time grading is required. In applications where fault current is relatively low, or where inverse time grading is not used, then an overcurrent factor of 10 may be adequate.

Maximum burden: The total burden calculated at rated secondary current of all equipment connected to the CT secondary, including relay input burden, lead burden, and taking the CT's own secondary resistance into account. GRD140 has an extremely low AC current burden, typically less than 0.1VA for a 1A phase input, allowing relatively low burden CTs to be applied. Relay burden does not vary with settings.

If a burden lower than the maximum specified is connected, then the practical overcurrent factor may be scaled accordingly. For the example given above, at a rated current of 1A, the maximum value of CT secondary resistance plus secondary circuit resistance (RCT + R2) should be 10Ω . If a lower value of, say, (RCT + R2) = 5Ω is applied, then the practical overcurrent factor may be increased by a factor of two, that is, to 40A.

In summary, the example given of a 5P20 CT of suitable rated burden will meet most applications of high fault current and tight grading margins. Many less severe applications may be served by 5P10 or 10P10 transformers.

2.1.9.2 Minimum Knee Point Voltage

An alternative method of specifying a CT is to calculate the minimum knee point voltage, according to the secondary current which will flow during fault conditions:

$$V_k \ge I_f (R_{CT} + R_2)$$

where:

 V_k = knee point voltage

 $I_f = maximum secondary fault current$

 R_{CT} = resistance of CT secondary winding

 R_2 = secondary circuit resistance, including lead resistance.

When using this method, it should be noted that it is often not necessary to transform the maximum fault current accurately. The knee point should be chosen with consideration of the settings to be applied and the likely effect of any saturation on protection performance. Further,

care should be taken when determining R2, as this is dependent on the method used to connect the CTs (E.g. residual connection, core balanced CT connection, etc).

2.1.9.3 Sensitive Earth Fault Protection

A core balance CT should be applied, with a minimum knee point calculated as described above.

2.1.9.4 Restricted Earth Fault Protection

High accuracy CTs should be selected with a knee point voltage Vk chosen according to the equation:

$$V_k \geq 2 \times \, V_s$$

where Vs is the differential stability voltage setting for the scheme.

2.2 Overvoltage and Undervoltage Protection

2.2.1 Phase Overvoltage Protection

GRD140 provides two independent phase overvoltage elements with programmable dropoff/pickup(DO/PU) ratio. OV1 is programmable for inverse time (IDMT) or definite time (DT) operation. OV2 has definite time characteristic only.

Figure 2.2.1 shows the characteristic of overvoltage elements.

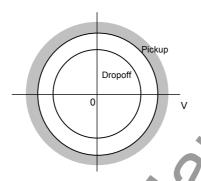


Figure 2.2.1 Characteristic of Overvoltage Elements

The overvoltage protection element OV1 has the IDMT characteristic defined by equation (1):

$$t = TMS \times \left[\frac{1}{\left(\frac{V}{V_S} \right) - 1} \right] \tag{1}$$

where:

t = operating time for constant voltage V (seconds),

V = energising voltage (V)

Vs = overvoltage setting (V)

TMS = time multiplier setting.

The IDMT characteristic is illustrated in Figure 2.2.2.

The OV2 element is used for definite time overvoltage protection.

Definite time reset

The definite time resetting characteristic is applied to the OV1 element when the inverse time delay is used.

If definite time resetting is selected, and the delay period is set to instantaneous, then no intentional delay is added. As soon as the energising voltage falls below the reset threshold, the element returns to its reset condition.

If the delay period is set to some value in seconds, then an intentional delay is added to the reset period. If the energising voltage exceeds the setting for a transient period without causing tripping, then resetting is delayed for a user-definable period. When the energising voltage falls below the reset threshold, the integral state (the point towards operation that it has travelled) of the timing function (IDMT) is held for that period.

This does not apply following a trip operation, in which case resetting is always instantaneous.

Both OV1 and OV2 have a programmable dropoff/pickup(DO/PU) ratio.

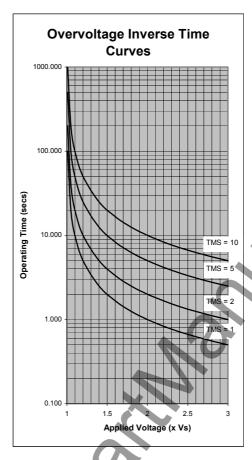


Figure 2.2.2 IDMT Characteristic

Scheme Logic

Figure 2.2.3 shows the scheme logic of the OV1 overvoltage protection with selective definite time or inverse time characteristic.

The definite time protection is enabled by setting [OV1EN] to "DT", and trip signal OV1 TRIP is given through the delayed pick-up timer TOV1. The inverse time protection is enabled by setting [OV1EN] to "IDMT", and trip signal OV1 TRIP is given.

The OV1 protection can be disabled by the scheme switch [OV1EN] or the binary input signal OV1 BLOCK.

Figure 2.2.4 shows the scheme logic of the OV2 protection with definite time characteristic. The OV2 gives the signal OV2-ALARM through delayed pick-up timer TOV2.

The OV2-ALARM signal can be blocked by incorporated scheme switch [OV2EN] and the binary input signal OV2 BLOCK.

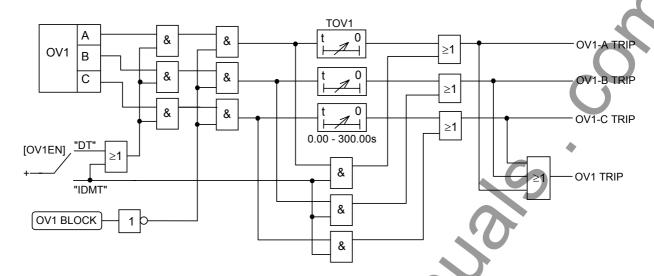


Figure 2.2.3 OV1 Overvoltage Protection

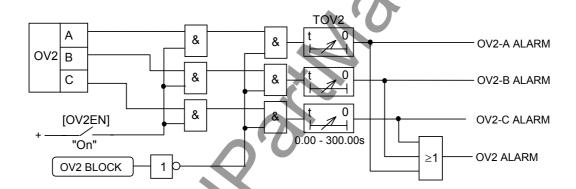


Figure 2.2.4 OV2 Overvoltage Protection

Setting

The table shows the setting elements necessary for the overvoltage protection and their setting ranges.

	Element	Range	Step	Default	Remarks
	OV1	10.0 – 200.0 V	0.1 V	120.0 V	OV1 threshold setting
	TOV1M	0.05 – 100.00	0.01	1.00	OV1 time multiplier setting. Required if [OV1EN] = IDMT.
	TOV1	$0.00 - 300.00 \mathrm{s}$	0.01 s	1.00 s	OV1 definite time setting. Required if [OV1EN] = DT.
	TOV1R	0.0 – 300.0 s	0.1 s	0.0 s	OV1 definite time delayed reset.
	OV1DPR	10 – 98 %	1 %	95 %	OV1 DO/PU ratio setting.
	OV2	10.0 – 200.0 V	0.1 V	140.0 V	OV2 threshold setting.
	TOV2	0.00 - 300.00 s	0.01 s	1.00 s	OV2 definite time setting.
	OV2DPR	10 - 98 %	1 %	95 %	OV2 DO/PU ratio setting.
	[OV1EN]	Off / DT / IDMT		Off	OV1 Enable
N	[OV2EN]	Off / On		Off	OV2 Enable
14					

2.2.2 Phase Undervoltage Protection

GRD140 provides two independent phase undervoltage elements. UV1 programmable for inverse time (IDMT) or definite time (DT) operation. UV2 has definite time characteristic only.

Figure 2.2.5 shows the characteristic of the undervoltage elements.

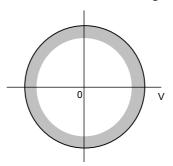


Figure 2.2.5 Characteristic of Undervoltage Elements

The undervoltage protection element UV1 has an IDMT characteristic defined by equation (2):

$$t = TMS \times \left[\frac{1}{1 - \left(\frac{V}{V_S} \right)} \right]$$
 (2)

where:

t = operating time for constant voltage V (seconds),

V = energising voltage (V),

Vs = undervoltage setting (V)

TMS = time multiplier setting

The IDMT characteristic is illustrated in Figure 2.2.6.

The UV2 element is used for definite time undervoltage protection.

Definite time reset

The definite time resetting characteristic is applied to the UV1 element when the inverse time delay is used.

If definite time resetting is selected, and the delay period is set to instantaneous, then no intentional delay is added. As soon as the energising voltage rises above the reset threshold, the element returns to its reset condition.

If the delay period is set to some value in seconds, then an intentional delay is added to the reset period. If the energising voltage is below the undercurrent setting for a transient period without causing tripping, then resetting is delayed for a user-definable period. When the energising voltage rises above the reset threshold, the integral state (the point towards operation that it has travelled) of the timing function (IDMT) is held for that period.

This does not apply following a trip operation, in which case resetting is always instantaneous.

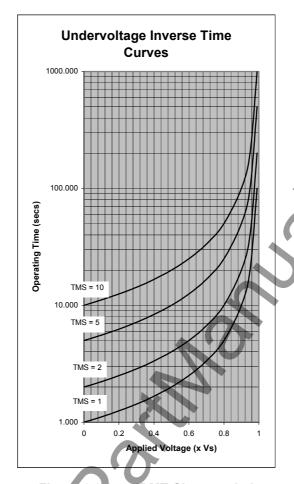


Figure 2.2.6 IDMT Characteristic

Scheme Logic

Figure 2.2.7 shows the scheme logic of the UV1 undervoltage protection with selective definite time or inverse time characteristic.

The definite time protection is selected by setting [UV1EN] to "DT", and trip signal UV1 TRIP is given through the delayed pick-up timer TUV1. The inverse time protection is selected by setting [UV1EN] to "IDMT", and trip signal UV1 TRIP is given.

The UV1 protection can be disabled by the scheme switch [UV1EN] or binary input signal UV1 BLOCK.

Figure 2.2.8 shows the scheme logic of the UV2 protection with definite time characteristic. The UV2 gives the signal UV2-ALARM through delayed pick-up timer TUV2.

The UV2-ALARM can be blocked by incorporated scheme switch [UV2EN] and the binary input signal UV2 BLOCK.

In addition, there is a user programmable voltage threshold VBLK. If all measured phase voltages drop below this setting, then both UV1 and UV2 are prevented from operating. This function can be blocked by the scheme switch [VBLKEN]. The [VBLKEN] should be set to "OFF" (not used) when the UV elements are used as fault detectors, and set to "ON" (used) when used for load shedding.

Note: The VBLK must be set lower than any other UV setting values.

Further, these protection can be blocked when VT failure (VTF) is detected.

TOSHIBA 6 F 2 S 0 7 5 8

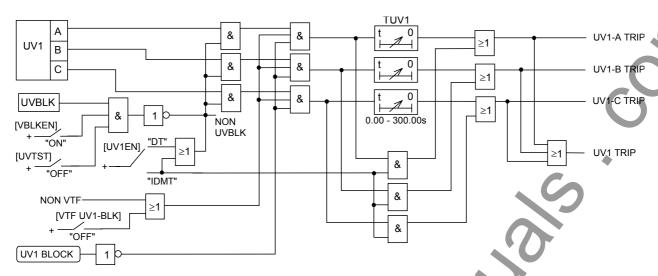


Figure 2.2.7 UV1 Undervoltage Protection

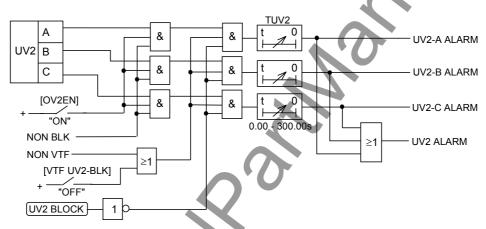


Figure 2.2.8 UV2 Undervoltage Protection

Setting

The table shows the setting elements necessary for the undervoltage protection and their setting ranges.

Element	Range	Step	Default	Remarks
UV1	5.0 – 130.0 V	0.1 V	60.0 V	UV1 threshold setting
TUV1M	0.05-100.00	0.01	1.00	UVI time multiplier setting. Required if [UV1EN] = IDMT.
TUV1	0.00 – 300.00 s	0.01 s	1.00 s	UV1 definite time setting. Required if [UV1EN] = DT.
TUV1R	0.0 - 300.0 s	0.1 s	0.0 s	UV1 definite time delayed reset.
UV2	5.0 – 130.0 V	0.1 V	40.0 V	UV2 threshold setting.
TUV2	0.00 – 300.00 s	0.01 s	1.00 s	UV2 definite time setting.
VBLK •	5.0 - 20.0 V	0.1 V	10.0 V	Undervoltage block threshold setting.
[UV1EN]	Off / DT / IDMT		DT	UV1 Enable
[VTF UV1BLK]	Off / On		Off	UV1 VTF block
[VBLKEN]	Off / On		Off	UV block Enable
[UV2EN]	Off / On		Off	UV2 Enable
[VTF UV2BLK]	Off / On		Off	UV2 VTF block

2.2.3 Zero Phase Sequence Overvoltage Protection

The zero phase sequence overvoltage protection (ZOV) is applied to earth fault detection on unearthed, resistance-earthed system or on ac generators.

The ZOV is available for the following models and their [APPL-VT] settings:

Model	110	400,	420	
[APPL-VT] setting	_	3PN 3PV		
ZOV	√ (*1)	√ (*2)	√ (*1)	

Note: (*1); V_0 is measured directly in the form of the system residual voltage. (*2); V_0 is calculated from the three measured phase voltages.

The low voltage settings which may be applied make the ZOV element susceptible to any 3rd harmonic component which may be superimposed on the input signal. Therefore, a 3rd harmonic filter is provided to suppress such superimposed components.

For the earth fault detection, following two methods are in general use.

- Measuring the zero sequence voltage produced by VT residual connection (broken-delta connection) as shown in Figure 2.2.9.
- Measuring the residual voltage across the earthing transformers as shown in Figure 2.2.10.

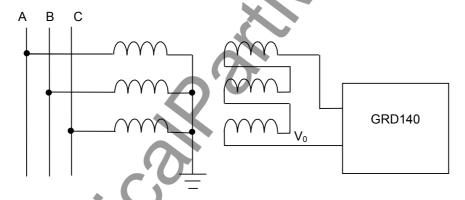


Figure 2.2.9 Earth Fault Detection on Unearthed System

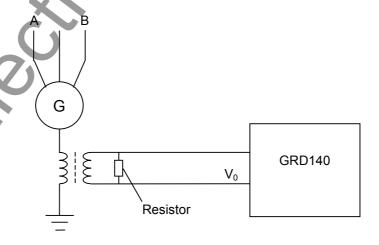


Figure 2.2.10 Earth Fault Detection on Generator

Two independent elements ZOV1 and ZOV2 are provided. The ZOV1 element is programmable for definite time delayed or inverse time delayed (IDMT) operation, and the ZOV2 element for

definite time delayed operation only.

The inverse time characteristic is defined by equation (3).

$$t = TMS \times \left[\frac{1}{\left(V_0 / V_S \right) - 1} \right]$$
 (3)

where:

t =operating time for constant voltage V_0 (seconds),

 $V_0 = Zero$ sequence voltage (V),

Vs = Zero sequence overvoltage setting (V),

TMS = time multiplier setting.

The IDMT characteristic is illustrated in Figure 2.2.11.

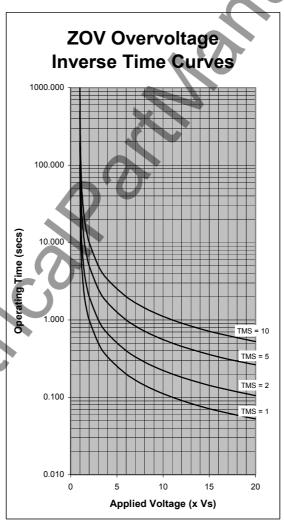


Figure 2.2.11 IDMT Characteristic of ZOV

Definite time reset

A definite time reset characteristic is applied to the ZOV1 element when the inverse time delay is used. Its operation is identical to that for the phase overvoltage protection.

Scheme Logic

Figure 2.2.12 shows the scheme logic of the zero sequence overvoltage protection. Two negative sequence overvoltage elements ZOV1 and ZOV2 with independent thresholds output trip signals ZOV1 TRIP and ZOV2 TRIP through delayed pick-up timers TZOV1 and TZOV2.

The tripping can be disabled by the scheme switches [ZOV1EN] and [ZOV2EN] or binary input signals ZOV1 BLOCK and ZOV2 BLOCK.

Further, this protection can be blocked when VT failure (VTF) is detected.

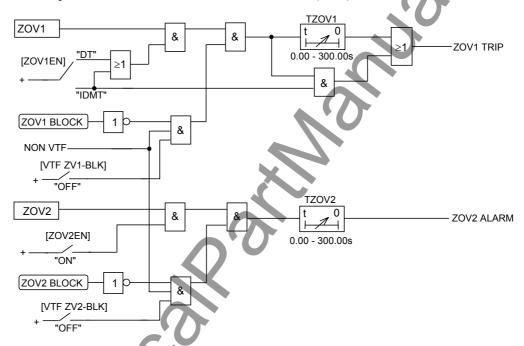


Figure 2.2.12 Zero Sequence Overvoltage Protection

Setting

The table below shows the setting elements necessary for the zero sequence overvoltage protection and their setting ranges.

Element	Range	Step	Default	Remarks
ZOV1	1.0 - 130.0 V	0.1V	20.0 V	ZOV1 threshold setting (V ₀) for tripping.
ZOV2	1.0 - 130.0 V	0.1V	40.0 V	ZOV2 threshold setting $$ (V ₀) for alarming.
TZOV1P	0.05 – 100.00	0.01	1.00	ZOV1 time multiplier setting. Required if [ZOV1EN]=IDMT.
TZOV1D	0.00 – 300.00 s	0.01 s	1.00 s	ZOV1 definite time setting. Required if [ZOV1EN]=DT.
TZOV1R	0.0 - 300.0 s	0.1 s	0.0 s	ZOV1 definite time delayed reset.
TZOV2	0.00 – 300.00 s	0.01 s	1.00 s	ZOV2 definite time setting
[ZOV1EN]	Off / DT/IDMT		DT	ZOV1 Enable
[VTF ZV1BLK]	Off / On		Off	ZOV1 VTF block
[ZOV2EN]	Off / On		Off	ZOV2 Enable
[VTF ZV2BLK]	Off / On		Off	ZOV2 VTF block

2.2.4 Negative Phase Sequence Overvoltage Protection

The negative phase sequence overvoltage protection is used to detect voltage unbalance conditions such as reverse-phase rotation, unbalanced voltage supply etc.

The NOV protection is applied to protect three-phase motors from the damage which may be caused by the voltage unbalance. Unbalanced voltage supply to motors due to a phase loss can lead to increases in the negative sequence voltage.

The NOV protection is also applied to prevent the starting of the motor in the wrong direction, if the phase sequence is reversed.

Two independent elements NOV1 and NOV2 are provided. The NOV1 element is programmable for definite time delayed or inverse time delayed (IDMT) operation, and the NOV2 element for definite time delayed operation only.

The inverse time characteristic is defined by equation (4).

$$t = TMS \times \left[\frac{1}{\left(\frac{V_2}{V_S} \right) - 1} \right] \tag{4}$$

where:

t = operating time for constant voltage V₂ (seconds),

 V_2 = Negative sequence voltage (V),

Vs = Negative sequence overvoltage setting (V),

TMS = time multiplier setting.

The IDMT characteristic is illustrated in Figure 2.2.13.

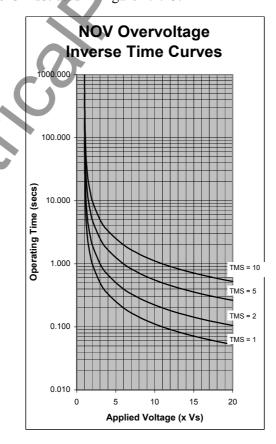


Figure 2.2.13 IDMT Characteristic of NOV

Definite time reset

A definite time reset characteristic is applied to the NOV1 element when the inverse time delay is used. Its operation is identical to that for the phase overvoltage protection.

Scheme Logic

Figure 2.2.14 shows the scheme logic of the negative sequence overvoltage protection. Two negative sequence overvoltage elements NOV1 and NOV2 with independent thresholds output trip signals NOV1 TRIP and NOV2 TRIP through delayed pick-up timers TNOV1 and TNOV2.

The tripping can be disabled by the scheme switches [NOV1EN] and [NOV2EN] or binary input signals NOV1 BLOCK and NOV2 BLOCK.

Further, this protection can be blocked when VT failure (VTF) is detected.

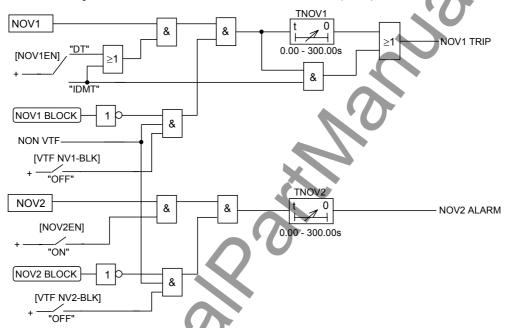


Figure 2.2.14 Negative Sequence Overvoltage Protection

Setting

The table below shows the setting elements necessary for the negative sequence overvoltage protection and their setting ranges.

The delay time setting TNOV1 and TNOV2 is added to the inherent delay of the measuring elements NOV1 and NOV2. The minimum operating time of the NOV elements is around 200ms.

Element	Range	Step	Default	Remarks
NOV1	1.0 - 130.0 V	0.1V	20.0 V	NOV1 threshold setting for tripping.
NOV2	1.0 - 130.0 V	0.1V	40.0 V	NOV2 threshold setting for alarming.
TNOV1P	0.05 – 100.00	0.01	1.00	NOV1 time multiplier setting. Required if [NOV1EN]=IDMT.
TNOV1D	0.00 - 300.00 s	0.01 s	1.00 s	NOV1 definite time setting. Required if [NOV1EN]=DT.
TNOV1R	0.0 - 300.0 s	0.1 s	0.0 s	NOV1 definite time delayed reset.
TNOV2	0.00 - 300.00 s	0.01 s	1.00 s	NOV2 definite time setting
[NOV1EN]	Off / DT/IDMT		Off	NOV1 Enable
[NOV2EN]	Off / On		Off	NOV2 Enable

2.3 Frequency Protection

For a four-stage frequency protection, GRD140 incorporates dedicated frequency measuring elements and scheme logic for each stage. Each stage is programmable for underfrequency or overfrequency protection.

Underfrequency protection is provided to maintain the balance between the power generation capability and the loads. It is also used to maintain the frequency within the normal range by load shedding.

Overfrequency protection is typically applied to protect synchronous machines from possible damage due to overfrequency conditions.

A-phase to B-phase voltage is used to detect frequency.

Frequency element

Underfrequency element UF operates when the power system frequency falls under the setting value

Overfrequency element OF operates when the power system frequency rises over the setting value.

These elements measure the frequency and check for underfrequency or overfrequency every 5 ms. They operate when the underfrequency or overfrequency condition is detected 16 consecutive times.

Both UF and OF elements output is invalidated by undervoltage block element (FVBLK) operation during undervoltage condition.

Figure 2.3.1 shows characteristics of UF and OF elements.

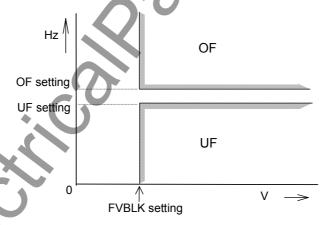


Figure 2.3.1 Underfrequency and Overfrequency Element

Scheme Logic

Figure 2.3.2 shows the scheme logic of frequency protection in stage 1. The frequency element FRQ1 can output a trip command under the condition that the system voltage is higher than the setting of the undervoltage element FVBLK (FVBLK=1). The FRQ1 element is programmable for underfrequency or overfrequency operation by the scheme switch [FRQ1EN].

The tripping can be disabled by the scheme switches [FRQ1EN].

The stage 2 (FRQ2) to stage 4 (FRQ4) are the same logic of FRQ1

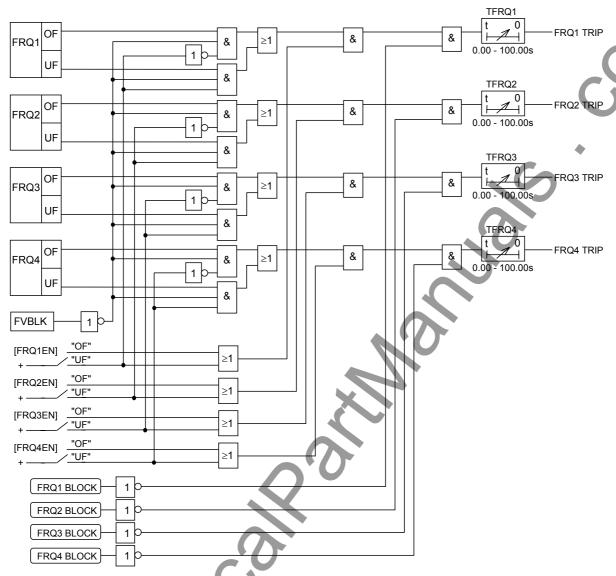


Figure 2.3.2 Scheme Logic of Frequency Protection

Setting

The setting elements necessary for the frequency protection and their setting ranges are shown in the table below.

	Element	Range	Step	Default	Remarks
	FRQ1	-10.00 – +10.00 Hz	0.01 Hz	-1.00 Hz	FRQ1 frequency element setting
	TFRQ1	0.00 – 300.00 s	0.01 s	1.00 s	Timer setting of FRQ1
	FRQ2	-10.00 - +10.00 Hz	0.01 Hz	-1.00 Hz	FRQ2 frequency element setting
	TFRQ2	0.00 – 300.00 s	0.01 s	1.00 s	Timer setting of FRQ2
	FRQ3	-10.00 - +10.00 Hz	0.01 Hz	-1.00 Hz	FRQ3 frequency element setting
	TFRQ3	0.00 - 300.00 s	0.01 s	1.00 s	Timer setting of FRQ3
	FRQ4	-10.00 - +10.00 Hz	0.01 Hz	-1.00 Hz	FRQ4 frequency element setting
	TFRQ4	0.00 - 300.00 s	0.01 s	1.00 s	Timer setting of FRQ4
7	FVBLK	40.0 – 100.0 V	0.1 V	40.0 V	UV block setting
	FRQ1EN	Off / OF / UF		Off	FRQ1 Enable
	FRQ2EN	Off / OF / UF		Off	FRQ2 Enable
	FRQ3EN	Off / OF / UF		Off	FRQ3 Enable
	FRQ4EN	Off / OF / UF		Off	FRQ4 Enable

2.4 Trip and Alarm Signal Output

GRD140 provides various trip and alarm signal outputs such as three-phase and single-phase trip and alarm of each protection. Figures 2.4.1 and 2.4.2 show gathered trip and alarm signals of each protection.

GRD140 provides 8 auxiliary relays for binary outputs as described in Section 3.2.7 of the auxiliary relays can be assigned to any protection outputs.

After the trip signal disappears by clearing the fault, the reset time of the tripping output relay can be programmed. The setting is respective for each output relay.

When the relay is latched, it can be reset with the RESET key on the relay front panel or a binary input. This resetting resets all the output relays collectively.

In the tripping output relay, it must be checked that the tripping circuit is opened with a circuit breaker auxiliary contact prior to the tripping output relay resetting, in order to prevent the tripping output relay from directly interrupting the circuit breaker tripping coil current.

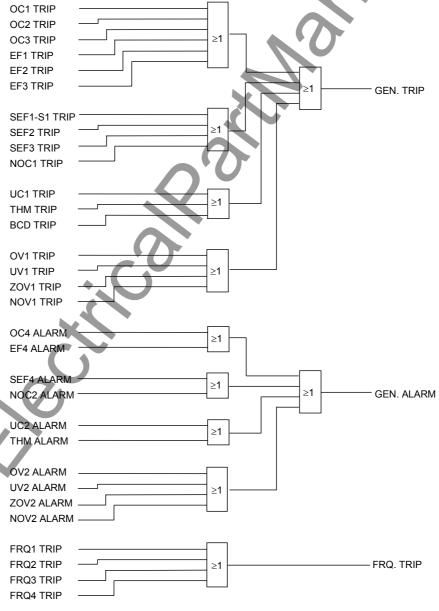


Figure 2.4.1 Three-phase Output

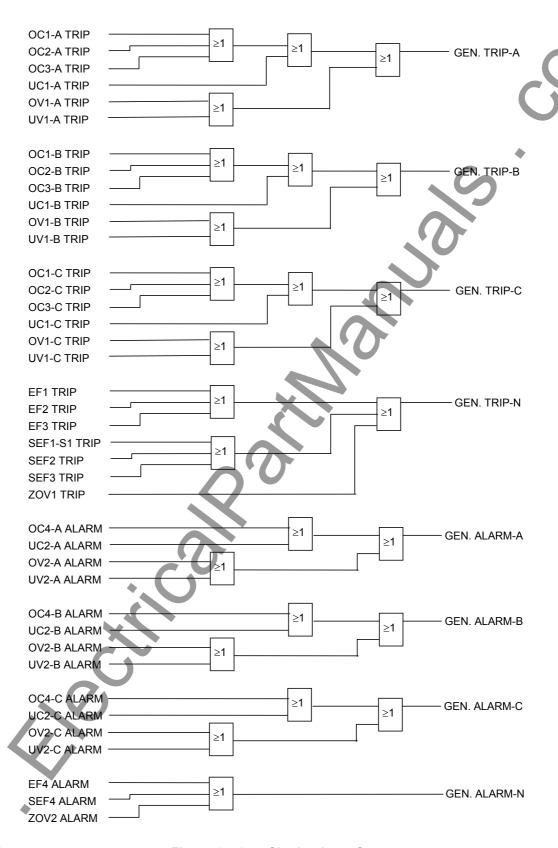


Figure 2.4.2 Single-phase Output

2.5 Autoreclose

The GRD140 provides a multi-shot (five shots) autoreclosing scheme applied for one-circuit breaker:

- Three phase autoreclosing scheme for all shots
- Autoreclosing counter

The autoreclosing (ARC) can be initialized by OC1 to OC4, EF1 to EF4, SEF1-S1 to SEF4 trip signals or external trip signals via binary inputs, as determined by scheme switches [****-INIT]. Trip signals are selected to be used or not used for ARC, by setting [****-INIT] to "On" or "NA" respectively. If a trip signal is used to block ARC, then [****-INIT] is set to "BLK". ARC can also be blocked by binary input signal ARC BLOCK.

Three-phase autoreclosing is provided for all shots, regardless of whether the fault is single-phase or multi-phase. Autoreclosing can be programmed to provide any number of shots, from one to five. In each case, if the first shot fails, then all subsequent shots apply three-phase tripping and reclosing.

To disable autoreclosing, scheme switch [ARCEN] is set to "Off"

2.5.1 Scheme Logic

Figure 2.5.1 shows the simplified scheme logic for the autoreclose. Autoreclose becomes ready when the circuit breaker is closed and ready for autoreclose (CB READY=1), the on-delay timer TRDY is picked up, and the [ARCEN] is set to "ON". TRDY is used to determine the reclaim time.

If the autoreclose is ready, then reclosing is activated by ARC INIT. ARC INIT is programmed from tripping commands of the various protections by scheme switches [****-INIT]. Further, the external tripping command signal EXT TRIP-APH, EXT TRIP-BPH, EXT TRIP-CPH or EXT TRIP-3PH can also activate the autoreclose via binary inputs.

Once autoreclose is activated, it is maintained by a flip-flop circuit until one reclosing cycle is completed.

Multi-shot autoreclose

Regardless of the tripping mode, three-phase reclose is performed. If the [ARCEN] is set to "On", the dead time counter TD1 for three-phase reclosing is started. After the dead time has elapsed, reclosing command ARC-SHOT is initiated.

Multi-shot autoreclose can be executed up to four times after the first-shot autoreclose fails. The multi-shot mode, one to five shots, is set with the scheme switch [ARC*-NUM].

During multi-shot reclosing, the dead time counter TD2 for the second shot is activated if the first shot autoreclose is performed, but tripping occurs again. Second shot autoreclose is performed after the period of time set on TD2 has elapsed. At this time, outputs of the step counter are: SP1 = 1, SP2 = 0, SP3 = 0, SP4 = 0 and SP5 = 0.

Autoreclose is completed at this step if the two shots mode is selected for the multi-shot mode. In this case, tripping following a "reclose-onto-a-fault" becomes the final trip (ARC FT = 1).

If three shot mode is selected for the multi-shot mode, autoreclose is further retried after the above tripping occurs. At this time, the T1S3 is started. The third shot autoreclose is performed after the period of time set on the TD3 has elapsed. At this time, outputs of the step counter are: SP1 = 0, SP2 = 1, SP3 = 0, SP4 = 0 and SP5 = 0.

The three shot mode of autoreclose is then completed, and tripping following a "reclose-onto-a-fault" becomes the final trip (ARC FT = 1).

When four or five shot autoreclose is selected, autoreclose is further retried once again for tripping that occurs after "reclose-onto-a-fault". This functions in the same manner as the three shot autoreclose.

If a fault occurs under the following conditions, the final trip is performed and autoreclose is blocked.

- Reclosing block signal is applied.
- During the reclaim time

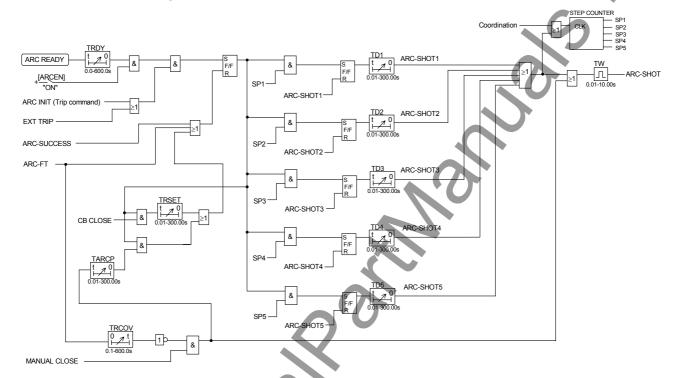


Figure 2.5.1 Autoreclose Scheme Logic

2.5.2 Sequence Coordination

Co-ordination is maintained between the autoreclose sequences of adjacent relays on a feeder. This means that a relay will register the flow of fault current and increment through its autoreclose sequence even if another relay actually carries out the tripping and reclosing operations. This function is initiated by the operation of OC, EF or SEF element, and can be disabled by the scheme switch [COORD-OC], [COORD-EF] or [COORD-SE].

The reclose shot number at the local terminal A is coordinated with that at the adjacent terminal B as shown in Figure 2.5.2.



Figure 2.5.2 Sequence Coordination

2.5.3 Setting

The setting elements necessary for the autoreclose and their setting ranges are shown in the table below.

Element	Range	Step	Default	Remarks
ARC				
TRDY	0.0 - 600.0 s	0.1 s	60.0 s	Reclaim time
TD1	0.01 - 300.00 s	0.01 s	10.00 s	1st shot dead time for Stage 1
TD2	0.01 - 300.00 s	0.01 s	10.00 s	2 nd shot dead time for Stage 1
TD3	0.01 - 300.00 s	0.01 s	10.00 s	3rd shot dead time for Stage 1
TD4	0.01 - 300.00 s	0.01 s	10.00 s	4th shot dead time for Stage 1
TD5	0.01 - 300.00 s	0.01 s	10.00 s	5th shot dead time for Stage 1
TW	0.01 - 10.00 s	0.01 s	2.00 s	Output pulse time
TSUC	0.1 – 600.0 s	0.1 s	3.0 s	Autoreclose succeed judgement time
TRCOV	0.1 – 600.0 s	0.1 s	10.0 s	Autoreclose recovery time after final trip
TARCP	0.1 – 600.0 s	0.1 s	10.0 s	Autoreclose pause time after manually closing
TRSET	0.01 – 300.00 s	0.01 s	3.00 s	Autoreclose reset time
[ARCEN]	Off/On		On	Autoreclose enable
[ARC-NUM]	S1/S2/S3/S4/S5		S1	Autoreclosing shot number
[OC1-INIT]	NA/A1/A2/BLK		A1	Autoreclose initiation by OC1
[OC2-INIT]	NA/A1/A2/BLK		NA	Autoreclose initiation by OC2
[OC3-INIT]	NA/A1/A2/BLK		NA	Autoreclose initiation by OC3
[OC4-INIT]	NA/A1/A2/BLK		NA	Autoreclose initiation by OC4
[EF1-INIT]	NA/A1/A2/BLK		NA	Autoreclose initiation by EF1
[EF2-INIT]	NA/A1/A2/BLK		NA	Autoreclose initiation by EF2
[EF3-INIT]	NA/A1/A2/BLK		NA	Autoreclose initiation by EF3
[EF4-INIT]	NA/A1/A2/BLK		NA	Autoreclose initiation by EF4
[SE1-INIT]	NA/A1/A2/BLK		NA	Autoreclose initiation by SE1
[SE2-INIT]	NA/A1/A2/BLK		NA	Autoreclose initiation by SE2
[SE3-INIT]	NA/A1/A2/BLK		NA	Autoreclose initiation by SE3
[SE4-INIT]	NA/A1/A2/BLK		NA	Autoreclose initiation by SE4
[EXT-INIT]	NA/A1/A2/BLK		NA	Autoreclose initiation by external trip command
[COORD-OC]	Off/On		Off	OC relay for Co-ordination
[COORD-EF]	Off/On		Off	EF relay for Co-ordination
[COORD-SE]	Off/On		Off	SE relay for Co-ordination
OC	0.2 – 250.0 A	0.1 A	5.0 A	OC for co-ordination
	(0.04 – 50.00 A) (*)	(0.01 A)	(1.00 A)	
EF	0.2 - 250.0 A	0.1 A	1.5 A	EF for co-ordination
	(0.04 - 50.00 A)	(0.01 A)	(0.30 A)	
SEF	0.025 - 0.125 A	0.01 A	0.050 A	SEF for co-ordination
	(0.005 - 0.025 A)	(0.01 A)	(0.010 A)	

^(*) Current values shown in the parenthesis are in the case of a 1 A rating. Other current values are in the case of a 5 A rating.

To determine the dead time, it is essential to find an optimal value while taking factors, de-ionization time and power system stability, into consideration which normally contradict each other.

Normally, a longer de-ionization time is required as for a higher line voltage or larger fault current. For three-phase autoreclose, the dead time is generally 15 to 30 cycles.

TOSHIBA

3. Technical Description

3.1 Hardware Description

3.1.1 Outline of Hardware Modules

The case outline of GRD140 is shown in Appendix F.

The hardware structure of GRD140 is shown in Figure 3.1.1.

The GRD140 relay unit consists of the following hardware modules. These modules are fixed in a frame and cannot be taken off individually. The human machine interface module is provided with the front panel.

- Power module (POWD)
- Signal processing module (SPMD)
- Human machine interface module (HMI)

The hardware block diagram of GRD140 is shown in Figure 3.1.2

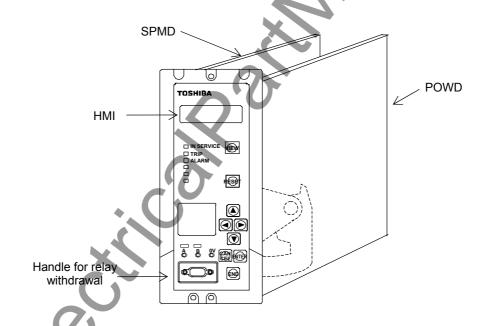


Figure 3.1.1 Hardware Structure without Case

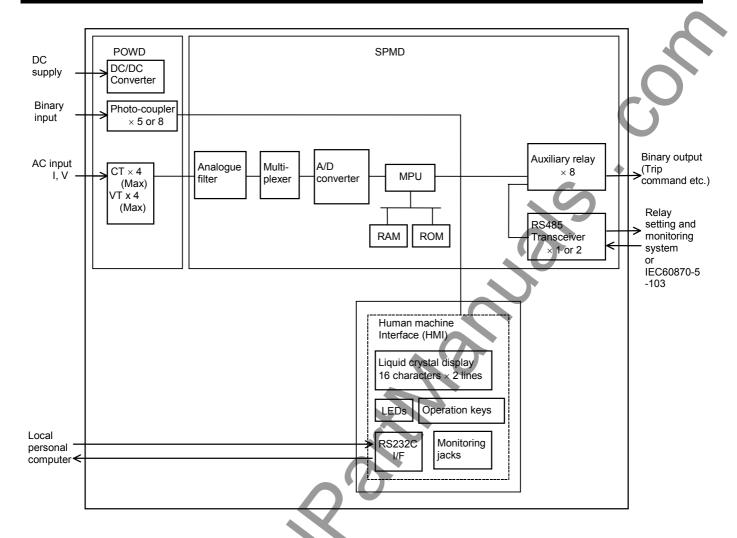


Figure 3.1.2 Hardware Block Diagram

POWD Module

The POWD module insulates between the internal and external circuits through an auxiliary transformer and transforms the magnitude of AC input signals to suit the electronic circuits. The AC input signals may be one to three phase currents and a residual current depending on the relay model.

This module incorporates max. 4 auxiliary CTs and max. 4 VTs, DC/DC converter and 5 or 8 photo-coupler circuits for binary input signals.

The available input voltage ratings of the DC/DC converter are, 48V, 110V/125V or 220/250V. The normal range of input voltage is -20% to +20%.

SPMD Module

The SPMD module consists of analogue filter, multiplexer, analogue to digital (A/D) converter, main processing unit (MPU), random access memory (RAM) and read only memory (ROM) and executes all kinds of processing such as protection, measurement, recording and display.

The analogue filter performs low-pass filtering for the corresponding current signals.

The A/D converter has a resolution of 12 bits and samples input signals at sampling frequencies of 2400 Hz (at 50 Hz) and 2880 Hz (at 60 Hz).

The MPU implements more than 240 MIPS and uses a RISC (Reduced Instruction Set Computer) type 32-bit microprocessors.

The SPMD module also incorporates 8 auxiliary relays (BO1-BO7 and FAIL) for binary output signals and an RS485 transceiver.

BO1 to BO6 are user configurable output signals and have one normally open and one normally closed contact. BO7 is also a user-configurable output signal and has one normally open contact.

The auxiliary relay FAIL has one normally open and one normally closed contacts, and operates when a relay failure or abnormality in the DC circuit is detected.

The RS485 transceiver is used for the link with the relay setting and monitoring (RSM) system or IEC60870-5-103 communication. The external signal is isolated from the relay's internal circuits.

Human Machine Interface (HMI) Module

The operator can access the GRD140 via the human machine interface (HMI) module. As shown in Figure 3.1.3, the HMI panel has a liquid crystal display (LCD), light emitting diodes (LED), view and reset keys, operation keys, monitoring jacks and an RS232C connector on the front panel.

The LCD consists of 16 columns by 2 rows with a back-light and displays recording, status and setting data.

There are a total of 6 LED indicators and their signal labels and LED colors are defined as follows:

Label	Color	Remarks
IN SERVICE	Green	Lit when the relay is in service and flickered when the relay is in "Test" menu.
TRIP	Red	Lit when a trip command is issued.
ALARM	Red	Lit when a failure is detected.
(LED1)	Yellow	
(LED2)	Yellow	
(LED3)	Yellow	

LED1, LED2 and LED3 are user-configurable. Each is driven via a logic gate which can be programmed for OR gate or AND gate operation. Further, each LED has a programmable reset characteristic, settable for instantaneous drop-off, or for latching operation. A configurable LED can be programmed to indicate the OR combination of a maximum of 4 elements, the individual statuses of which can be viewed on the LCD screen as "Virtual LEDs." For the setting, see Section 4.2.6.10. For the operation, see Section 4.2.1.

The TRIP LED and an operated LED if latching operation is selected, must be reset by user, either by pressing the RESET key, by energising a binary input which has been programmed for 'Remote Reset' operation, or by a communications command. Other LEDs operate as long as a signal is present. The RESET key is ineffective for these LEDs.

The VIEW key starts the LCD indication and switches between windows. The RESET key clears the LCD indication and turns off the LCD back-light.

The operation keys are used to display the record, status and setting data on the LCD, input the settings or change the settings.

The monitoring jacks and two pairs of LEDs, A and B, on top of the jacks can be used while the test mode is selected in the LCD window. Signals can be displayed on LED A or LED B by selecting the signal to be observed from the "Signal List" and setting it in the window and the signals can be transmitted to an oscilloscope via the monitoring jacks. (For the "Signal List", see Appendix C.)

The RS232C connector is a 9-way D-type connector for serial RS232C connection. This

connector is used for connection with a local personal computer.

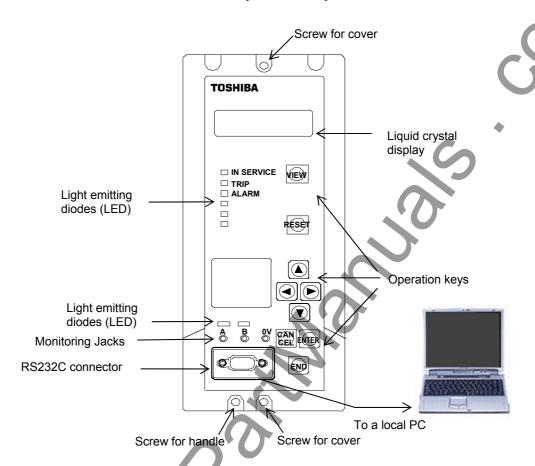


Figure 3.1.3 Front Panel

3.2 Input and Output Signals

3.2.1 AC Input Signals

Table 3.2.1 shows the AC input signals necessary for the GRD140 model and their respective input terminal numbers. Model 400 and 420 depend on their scheme switch [APPL] setting.

Term.	. [APPL-CT] setting		ing	[A	PPL-VT] settir	L-VT] setting		
No.	3P	2P	1P (Model 110)	3PN	3PV	Model 110		
TB1 1-2	A phase current la	A phase current la				Residual voltage Ve		
TB1 3-4	B phase current lb	C phase current lc						
TB1 5-6	C phase current lc	Residual current le	Residual current le	5				
TB1 7-8	Residual current le or Zero sequence current lse(*)	Zero sequence current lse(*)	Zero sequence current lse(*)					
TB2 A1-B2				A phase voltage Va	A phase voltage Va			
TB2 B1-B2				B phase voltage Vb	B phase voltage Vb			
TB2 A2-B2			50	C phase voltage Vc	C phase voltage Vc			
TB2 A3-B3			-		Residual voltage Ve			

Table 3.2.1 AC Input Signals

3.2.2 Binary Input, Output Signals

The GRD140 provides eight programmable binary input circuits. Each binary input circuit is programmable, and provided with the function of Logic level inversion and Function selection.

Logic level inversion

The binary input circuit of the GRD140 is provided with a logic level inversion function and a pick-up and drop-off delay timer function as shown in Figure 3.2.1. Each input circuit has a binary switch BISNS which can be used to select either normal or inverted operation. This allows the inputs to be driven either by normally open or normally closed contacts. Where the driving contact meets the contact conditions then the BISNS can be set to "Norm" (normal). If not, then "Inv" (inverted) should be selected. The pick-up and drop-off delay times can be set 0.0 to 300.00s respectively.

Logic level inversion function, and pick-up and drop-off delay timer settings are as follow:

Element	Contents	Range	Step	Default
BI1SNS - BI8SNS	Binary switch	Norm/ Inv		Norm
BI1PUD - BI8PUD	Delayed pick-up timer	0.00 - 300.00s	0.01s	0.00
BI1DOD - BI8DOD	Delayed drop-off timer	0.00 - 300.00s	0.01s	0.00

^{(*):} Ise required for SEF elements. In the model 420 and [APPL-CT]=3P, the residual current is calculated by Ia , Ib and Ic

The operating voltage of binary input signal is typical 74V DC at 110V/125V DC rating and 138V DC at 220/250V DC. The minimum operating voltage is 70V DC at 110/125V DC rating and 125V DC at 220/250V DC.

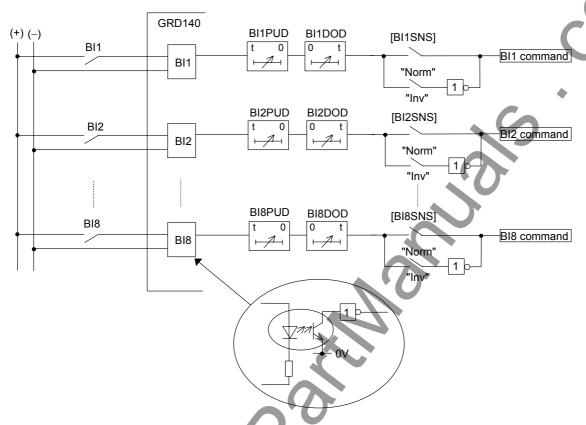


Figure 3.2.1 Logic Level Inversion

Function selection

The input signals BI1 COMMAND to BI5 COMMAND or to BI8 COMMAND are used for the functions listed in Table 3.2.2. Each input signal can be allocated for one or some of those functions by setting. For the setting, refer to Section 4.2.6.8.

The Table also shows the signal name corresponding to each function used in the scheme logic and LCD indication and driving contact condition required for each function.

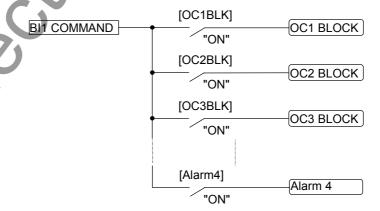


Figure 3.2.2 Function Scheme Logic

The logic of BI2 COMMAND to BI8 COMMAND are the same as that of BI1 COMMAND as shown in Figure 3.2.2.

Table 3.2.2 Function of Binary Input Signals

		Table 3.2.2 Fullction of B	mary input Signais
	Functions	Signal Names (*1)	Driving Contact Condition
-	Change active setting Group 1	SET.GROUP1	Closed to change the setting to Group 1
	Change active setting Group 2	SET.GROUP2	Closed to change the setting to Group 2
	Change active setting Group 3	SET.GROUP3	Closed to change the setting to Group 3
	Change active setting Group 4	SET.GROUP4	Closed to change the setting to Group 4
	OC1 protection block	OC1 BLOCK / OC1BLK	Closed to block OC1
	OC2 protection block	OC2 BLOCK / OC2BLK	Closed to block OC2
	OC3 protection block	OC3 BLOCK / OC3BLK	Closed to block OC3
	OC4 protection block	OC4 BLOCK / OC4BLK	Closed to block OC4
	EF1 protection block	EF1 BLOCK / EF1BLK	Closed to block EF1
	EF2 protection block	EF2 BLOCK / EF2BLK	Closed to block EF2
	EF3 protection block	EF3 BLOCK / EF3BLK	Closed to block EF3
	EF4 protection block	EF4 BLOCK / EF4BLK	Closed to block EF4
	EF1 protection permission	EF1 PERMIT	Closed to permit EF1
	EF2 protection permission	EF2 PERMIT	Closed to permit EF2
	EF3 protection permission	EF3 PERMIT	Closed to permit EF3
	EF4 protection permission	EF4 PERMIT	Closed to permit EF4
	SEF1 protection block	SEF1 BLOCK / SEF1BLK	Closed to block SEF1
	SEF2 protection block	SEF2 BLOCK / SEF2BLK	Closed to block SEF2
	SEF3 protection block	SEF3 BLOCK / SEF3BLK	Closed to block SEF3
	SEF4 protection block	SEF4 BLOCK / SEF4BLK	Closed to block SEF4
	UC1 protection block	UC1 BLOCK / UC1BLK	Closed to block UC1
	UC2 protection block	UC2 BLOCK / UC1BLK	Closed to block UC2
	THM protection block	THM BLOCK / THMBLK	Closed to block THM
	THMA protection block	THMA BLOCK / THMABLK	Closed to block THMA
	NOC1 protection block	NOC1 BLOCK / NC1BLK	Closed to block NOC1
	NOC2 protection block	NOC2 BLOCK / NC1BLK	Closed to block NOC2
	BCD protection block	BCD BLOCK / BCDBLK	Closed to block BCD
	CBF protection block	CBF BLOCK / CBFBLK	Closed to block CBF
	OV1 protection block	OV1 BLOCK / OV1BLK	Closed to block OV1
	OV2 protection block	OV2 BLOCK / OV2BLK	Closed to block OV2
	UV1 protection block	UV1 BLOCK / OV1BLK	Closed to block UV1
	UV2 protection block	UV2 BLOCK / OV2BLK	Closed to block UV2
	ZOV1 protection block	ZOV1 BLOCK / ZOV1BLK	Closed to block ZOV1
	ZOV2 protection block	ZOV2 BLOCK / ZOV2BLK	Closed to block ZOV2
	NOV1 protection block	NOV1 BLOCK / NOV1BLK	Closed to block NOV1
	NOV2 protection block	NOV2 BLOCK / NOV2BLK	Closed to block NOV2
	FRQ1 protection block	FRQ1 BLOCK / FRQ1BLK	Closed to block FRQ1
1	FRQ2 protection block	FRQ2 BLOCK / FRQ1BLK	Closed to block FRQ2
	FRQ3 protection block	FRQ3 BLOCK / FRQ1BLK	Closed to block FRQ3
1	FRQ4 protection block	FRQ4 BLOCK / FRQ1BLK	Closed to block FRQ4
	Autoreclose (ARC) scheme block	ARC BLOCK / ARCBLK	Closed to block ARC

Functions	Signal Names (*1)	Driving Contact Condition
ARC ready	ARC READY / ARCRDY	Closed when CB is closed and gas pressure is sufficient.
ARC initiation	ARC INIT / ARCINI	Closed to initiate ARC
Manual close	MANUAL CLOSE / MNLCLS	Closed to close CB manually.
ARC not applied	ARC N/A / ARCNA	Closed not to apply ARC scheme
CTF function block	CTF BLOCK / CTFBLK	Closed to block CTF function
External CTF	EXT CTF / CTFEXT	Closed to block a protection
VTF function block	VTF BLOCK / VTFBLK	Closed to block VTF function
External VTF	EXT VTF / VTFEXT	Closed to block a protection
Trip circuit supervision	TC FAIL / TCFALM	Trip circuit failure alarm
State transition for cold load protection, trip supervision and CB monitoring	CB CONT OPN / CBOPN	CB normally open contact
CB monitoring	CB CONT CLS / CBCLS	CB normally closed contact.
Breaker failure protection initiate	EXT TRIP-3PH / EXT3PH	External trip - 3 phase.
Breaker failure protection initiate	EXT TRIP-APH / EXTAPH	External trip - A phase.
Breaker failure protection initiate	EXT TRIP-BPH / EXTBPH	External trip - B phase
Breaker failure protection initiate	EXT TRIP-CPH / EXTCPH	External trip - C phase
Indication remote reset	REMOTE RESET / RMTRST	Closed to reset TRIP LED indication and latch of binary output relays
Synchronise clock	SYNC CLOCK / SYNCLK	Synchronise clock
Disturbance record store	STORE RECORD / STORCD	Closed to store the record
Alarm 1	Alarm 1 / Alarm1	Closed to display Alarm 1 text.
Alarm 2	Alarm 2 / Alarm2	Closed to display Alarm 2 text.
Alarm 3	Alarm 3 / Alarm3	Closed to display Alarm 3 text.
Alarm 4	Alarm 4 / Alarm4	Closed to display Alarm 4 text.

(*1): Signal names are those used in the scheme logic / LCD indication.

The binary input signals can be programmed to switch between four settings groups.

Element	Contents	Range	Step	Default
BI1SGS – BI8SGS	Setting group selection	OFF/1/2/3/4		OFF

Four alarm messages can be set. The user can define a text message within 16 characters for each alarm. The messages are valid for any of the input signals BI1 to BI8 by setting. Then when inputs associated with that alarm are raised, the defined text is displayed on the LCD.

3.2.3 Binary Output Signals

The number of binary output signals and their output terminals are as shown in Appendix G. All outputs, except the relay failure signal, can be configured.

The signals shown in the signal list in Appendix B can be assigned to the output relays BO1 to BO7 individually or in arbitrary combinations. Signals can be combined using either an AND circuit or OR circuit with 4 gates each as shown in Figure 3.2.3. The output circuit can be configured according to the setting menu. Appendix H shows the factory default settings.

Further, each BO has a programmable reset characteristic, settable for instantaneous drop-off "Inst", for delayed drop-off "Dl", for dwell operation "Dw" or for latching operation "Latch" by the scheme switch [RESET]. The time of the delayed drop-off "Dl" or dwell operation "Dw" can be set by TBO. When "Dw" selected, the BO outputs for the TBO set time if the input signal does not continue on the TBO set time. If the input signal continues more, the BO output is continuous for the input signal time.

The relay failure contact closes when a relay defect or abnormality in the DC power supply circuit is detected.

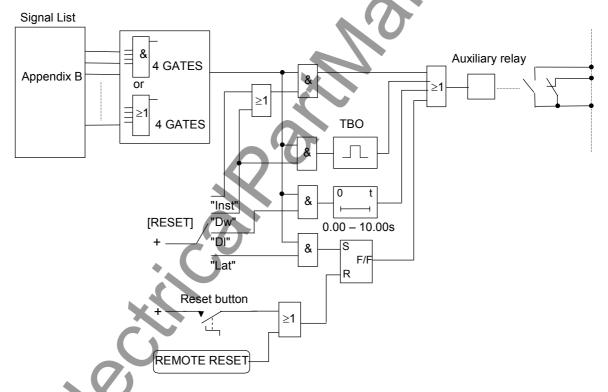


Figure 3.2.3 Configurable Output

Settings

The setting elements necessary for binary output relays and their setting ranges are as follows:

Element	Range	Step	Default	Remarks
[RESET]	Inst / DI / Dw /Latch		See Appendix C	Output relay reset time. Instantaneous, delayed, dwell or latched.
TBO	0.00 - 10.00s	0.01s	See Appendix C	

3.3 Automatic Supervision

3.3.1 Basic Concept of Supervision

Though the protection system is in a non-operating state under normal conditions, it waits for a power system fault to occur at any time, and must operate for the fault without fail. Therefore, the automatic supervision function, which checks the health of the protection system during normal operation, plays an important role. The GRD140 implements an automatic supervision function, based on the following concepts:

- The supervising function should not affect the protection performance
- Perform supervision with no omissions wherever possible.
- When a failure occurs, it is recorded as Alarm record, the user should be able to easily identify
 the location of the failure.

3.3.2 Relay Monitoring

The relay is supervised by the following functions.

AC input imbalance monitoring

The AC current input is monitored to check that the following equation is satisfied and the health of the AC input circuit is verified.

• CT circuit current monitoring for [APPL-CT] = "3P" setting

$$\begin{aligned} & \text{Max}(|I_a|, |I_b|, |I_c|) - 4 \times \text{Min}(|I_a|, |I_b|, |I_c|) \geq k_0 \\ & \text{where,} \end{aligned}$$

 $Max(|I_a|, |I_b|, |I_c|) = Maximum$ amplitude among I_a , I_b and I_c $Min(|I_a|, |I_b|, |I_c|) = Minimum$ amplitude among I_a , I_b and I_c $k_0 = 20\%$ of rated current

• Zero sequence voltage monitoring for [APPL-VT]= "3PN" setting

$$|V_a + V_b + V_c| / 3 \le 6.35 (V)$$

• Negative sequence voltage monitoring for [APPL-VT]= "3PN" and "3PV" setting

$$|V_a + a^2V_b + aV_c| / 3 \le 6.35 \text{ (V)}$$

where, $a = Phase shifter of 120^{\circ}$, $a^2 = Phase shifter of 240^{\circ}$

The CT circuit current monitoring allows high sensitivity detection of failures that have occurred in the AC input circuit. This monitoring can be disabled by the scheme switch [CTSVEN].

The zero sequence monitoring and negative sequence monitoring allow high sensitivity detection of failures that have occurred in the AC input circuits. These monitoring can be disabled by the scheme switches [V0SVEN] and [V2SVEN] respectively.

The negative sequence voltage monitoring allows high sensitivity detection of failures in the voltage input circuit, and it is effective for detection particularly when cables have been connected with the incorrect phase sequence.

A/D accuracy checking

An analog reference voltage is input to a prescribed channel in the analog-to-digital (A/D) converter, and it is checked that the data after A/D conversion is within a prescribed range, and

that the A/D conversion characteristics are correct.

Memory monitoring

Memory is monitored as follows, depending on the type of memory, and checks are done to verify that memory circuits are healthy:

• Random access memory monitoring:

Writes/reads prescribed data and checks the storage function.

Program memory monitoring: Checks the checksum value of the written data.

• Setting value monitoring: Checks discrepancies between the setting values stored in

duplicate.

Watchdog Timer

A hardware timer that is cleared periodically by the software is provided, which checks that the software is running normally.

DC Supply Monitoring

The secondary voltage level of the built-in DC/DC converter is monitored, and is checked to see that the DC voltage is within a prescribed range.

3.3.3 CT Failure Supervision

This function is available for [APPL-CT] = "3P" setting only.

Figure 3.3.1 shows the scheme logic of the CT failure supervision (CTFS). If the residual overcurrent element EFF(EFCF) operates and the residual overvoltage element ZOVF(ZOVCF) does not operate, CT failure (CTF) is detected. When the CTFS detects a CTF, it can alarm and block various protections as EF, NOC and UC protections etc.

The CTF signal is reset 100 ms after the CT failure condition has reset. When the CTF continues for 10s or more, "Err: CTF" is displayed in LCD message.

Further, the CT failure is detected when the binary input signal (external CTF) is received.

This function can be enabled or disabled by the scheme switch [CTFEN] and has a programmable reset characteristic. For latching operation, set to "ON", and for automatic reset after recovery, set to "OPT-ON".

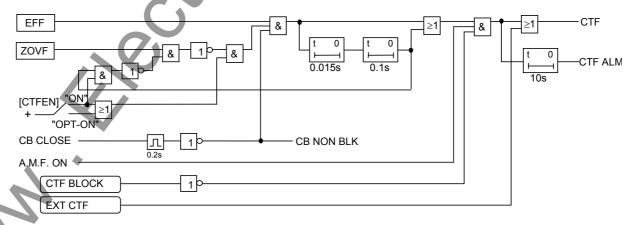


Figure 3.3.1 CT Failure Supervision

3.3.4 VT Failure Supervision

This function is available for [APPL-VT] = "3PN" and "3PV" settings.

When a fault occurs in the secondary circuit of the voltage transformer (VT), the voltage dependent measuring elements may operate incorrectly. GRD140 incorporates a VT failure supervision function (VTFS) as a measure against such incorrect operation. When the VTFS detects a VT failure, it can alarm and block the following voltage dependent protections by a binary input.

- Directional overcurrent protection
- Directional earth fault protection
- Directional sensitive earth fault protection
- Directional negative overcurrent protection
- Undervoltage protection
- Zero phase sequence overvoltage protection
- Negative phase sequence overvoltage protection

A binary input signal (external VTF) to indicate a miniature circuit breaker trip in the VT circuits is also available for the VTFS.

Scheme logic

Figure 3.3.2 shows the scheme logic for the VTFS. VT failure is detected by the following two schemes.

VTF1: The residual overcurrent element EFF(EFVF) does not operate (EFF=0), the residual overvoltage element ZOVF(ZOVVF) operates (ZOVF=1) and the phase current change detection element OCDF(OCDVF) does not operate (OCDF=0).

VTF2: The phase undervoltage element UVF(UVVF) operates (UVF=1) when the three phases of the circuit breaker are closed (CB CLOSE=1) and the phase current change detection element OCDF(OCDVF) does not operate (OCDF=0).

In order to prevent detection of false VT failures due to unequal pole closing of the circuit breaker, the VTFS is blocked for 200 ms after line energization.

The VTF signal is reset 100 ms after the VT failure condition has reset. When the VTF continues for 10s or more, "Err: VTF1" or "Err: VTF2" is displayed in LCD message.

Further, the VT failure is detected when the binary input signal (external VTF) is received.

This function can be enabled or disabled by the scheme switch [VTF1EN] or [VTF2EN] and has a programmable reset characteristic. For latching operation, set to "ON", and for automatic reset after the recover, set to "OPT-ON".

TOSHIBA

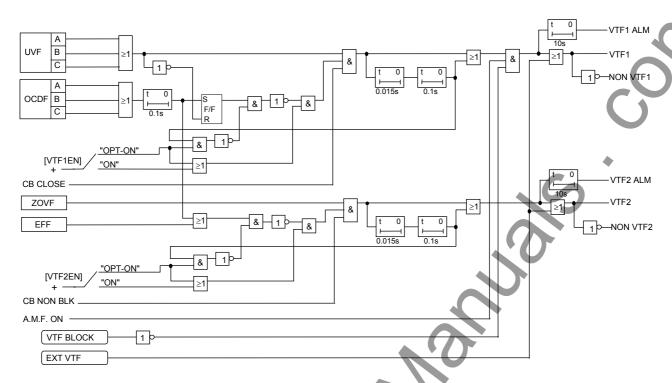


Figure 3.3.2 VT Failure Supervision

3.3.5 Trip Circuit Supervision

The circuit breaker tripping control circuit can be monitored by a binary input. Figure 3.3.3 shows a typical scheme. When the trip circuit is complete, a small current flows through the binary input and the trip circuit. Then logic signal of the binary input circuit BI is "1".

If the trip supply is lost or if a connection becomes an open circuit, then the binary input resets and the BI output is "0". A trip circuit fail alarm TCSV is output when the BI output is "0".

If the trip circuit failure is detected, then "ALARM" LED is lit and "Err: TC" is displayed in LCD message.

The monitoring is enabled by setting the scheme switch [TCSPEN] to "ON" or "OPT-ON". When "OPT-ON" is selected, the monitoring is enabled only while CB is closed.

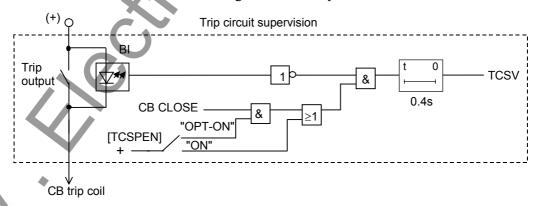


Figure 3.3.3 Trip Circuit Supervision Scheme Logic

3.3.6 Circuit Breaker Monitoring

The relay provides the following circuit breaker monitoring functions.

Circuit Breaker State Monitoring

Circuit breaker state monitoring is provided for checking the health of circuit breaker (CB). If two binary inputs are programmed to the functions 'CB OPEN' and 'CB CLOSED', then the CB state monitoring function becomes active. In normal circumstances these inputs are in opposite states. Figure 3.3.4 shows the scheme logic. If both show the same state during five seconds, then a CB state alarm CBSV operates and "Err:CB" and "CB err" are displayed in LCD message and event record message respectively.

The monitoring can be enabled or disabled by setting the scheme switch [CBSMEN].

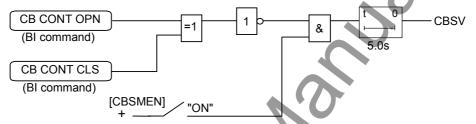


Figure 3.3.4 CB State Monitoring Scheme Logic

Normally open and normally closed contacts of the CB are connected to binary inputs BIm and BIn respectively, and functions of BIm and BIn are set to "CBOPN=ON" and "CBCLS=ON". (Refer to Section 4.2.6.8.)

Circuit Breaker Condition Monitoring

Periodic maintenance of CB is required for checking of the trip circuit, the operation mechanism and the interrupting capability. Generally, maintenance is based on a time interval or a number of fault current interruptions.

The following CB condition monitoring functions are provided to determine the time for maintenance of CB:

- Trip is counted for maintenance of the trip circuit and CB operation mechanism. The trip counter increments the number of tripping operations performed. An alarm is issued and informs user of time for maintenance when the count exceeds a user-defined setting TCALM. The trip count alarm can be enabled or disabled by setting the scheme switch [TCAEN].
- Sum of the broken current quantity ΣI^y is counted for monitoring the interrupting capability of CB. The ΣI^y counter increments the value of current to the power 'y', recorded at the time of issue of the tripping signal, on a phase by phase basis. For oil circuit breakers, the dielectric withstand of the oil generally decreases as a function of ΣI²t, and maintenance such as oil changes, etc., may be required. 'I' is the fault current broken by CB. 't' is the arcing time within the interrupter tank and it cannot be determined accurately. Therefore, 'y' is normally set to 2 to monitor the broken current squared. For other circuit breaker types, especially those for HV systems, 'y' may be set lower, typically 1.0. An alarm is issued when the count for any phase exceeds a user-defined setting ΣI^yALM. This feature is not available in GRD140-110. The ΣI^y count alarm can be enabled or disabled by setting the scheme switch [ΣI^yAEN].
- Operating time monitoring is provided for CB mechanism maintenance. It checks CB operating time and the need for mechanism maintenance is informed if the CB operation is slow. The operating time monitor records the time between issuing the tripping signal and the phase currents falling to zero. An alarm is issued when the operating time for any phase

exceeds a user-defined setting OPTALM. The operating time is set in relation to the specified interrupting time of the CB. The operating time alarm can be enabled or disabled by setting the scheme switch [OPTAEN].

The maintenance program should comply with the switchgear manufacturer's instructions.

The CB condition monitoring functions are triggered each time a trip is issued, and they can also be triggered by an external device via binary input EXT TRIP3PH (EXT3PH) or EXT TRIP*PH (EXT*PH) as shown in Figure 3.3.5. (Refer to Section 4.2.6.8.)

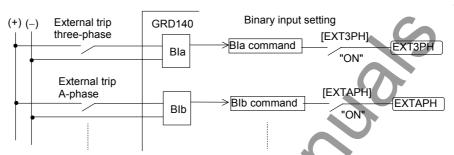


Figure 3.3.5 Binary Input Setting for CB Condition Monitoring

3.3.7 Failure Alarms

When a failure is detected by the automatic supervision, it is followed with an LCD message, LED indication, external alarm and event recording. Table 3.3.1 summarizes the supervision items and alarms.

The LCD messages are shown on the "Auto-supervision" screen, which is displayed automatically when a failure is detected or displayed by pressing the VIEW key. The event record messages are shown on the "Event record" screen by opening the "Record" sub-menu.

The alarms are retained until the failure is recovered.

The alarms can be disabled collectively by setting the scheme switch [AMF] to "OFF". The AC input imbalance monitoring alarms can be disabled collectively by setting the scheme switches [CTSVEN], [V0SVEN] and [V2SVEN] to "OFF". The setting is used to block unnecessary alarms during commissioning, test or maintenance.

When the Watchdog Timer detects that the software is not running normally, LCD display and event recording of the failure may not function normally.

Supervision Item	LCD Message	LED "IN Service"	LED "ALARM"	External alarm	Alarm record Message	
AC input imbalance monitoring	Err:CT, Err:V0, Err:V2 (1)	On/Off (2)	On	(4)	CT err, V0 err, V2 err, Relay fail or Relay fail-A (2)	
A/D accuracy check	Err:A/D	Off	On	(4)	Relay fail	
Memory monitoring	Err:SUM, Err:RAM, Err:BRAM, Err:EEP	Off	On	(4)	Relay fail	
Watchdog Timer		Off	On	(4)	<u> </u>	
DC supply monitoring	Err:DC	Off	(3)	Off	Relay fail-A	
Trip circuit supervision	Err:TC	On	On	Off	TC err, Relay fail-A	
CB state monitoring	Err:CB	On	On	Off	CB err, Relay fail-A	
CB condition monitoring						
Trip count alarm	ALM:TP COUNT	On	On	Off	TP COUNT ALM, Relay fail-A	
Operating time alarm	ALM: OP time	On	On	Off	OP time ALM, Relay fail-A	
∑l ^y count alarm	ALM:∑IY	On	On	Off	Σ IY-A ALM, Σ IY-B ALM or Σ IY-C ALM, Relay fail-A	
CT failure supervision	Err:CTF	On	On	Off	CTF err, Relay fail-A	
VT failure supervision	Err:VTF1, Err:VTF2	On	On	Off	VTF1 err, VTF2 err, Relay fail-A	

Table 3.3.1 Supervision Items and Alarms

- (1): Diverse messages are provided as expressed with "Err:---" in the table in Section 6.7.2.
- (2): The LED is on when the scheme switch [CTSVEN], [V0SVEN] or [V2SVEN] is set to "ALM" and off when set to "ALM & BLK" (refer to Section 3.3.6). The message "Relay fail-A" is recorded when the scheme switch [SVCNT] is set to "ALM".
- (3): Whether the LED is lit or not depends on the degree of the voltage drop.
- (4): The binary output relay "FAIL" operates.

The relationship between the LCD message and the location of the failure is shown in Table 6.7.1 in Section 6.7.2.

3.3.8 Trip Blocking

When a failure is detected by the following supervision items, the trip function is blocked as long as the failure exists, and is restored when the failure is removed.

- A/D accuracy check
- Memory monitoring
- Watchdog Timer

When a fault is detected by the AC input imbalance monitoring, the scheme switches [CTSVEN], [V0SVEN] and [V2SVEN] setting can be used to determine if both tripping is blocked and an alarm is output, or if only an alarm is output.

3.3.9 Setting

The setting element necessary for the automatic supervision and its setting range are shown in the table below.

Element	Range	Step	Default	Remarks
CTF supervision				
EFF	0.1 - 25.0 A	0.1 A	1.0 A	Residual overcurrent threshold setting
	(0.02 - 5.00 A	0.01 A	0.20 A) (*)	*
ZOVF	5.0 – 130.0 V	0.1 V	20.0 V	Residual overvoltage threshold setting
VTF supervision				
UVF	5.0 – 130.0 V	0.1 V	51.0 V	Undervoltage threshold setting
OCDF	0.5 A (Fixed)			Phase current change detection
	(0.1 A (Fixed))			
[CTFEN]	Off/On/OPT-On		Off	CTF supervision
[VTF1EN]	Off/On/OPT-On		Off	VTF1 supervision
[VTF2EN]	Off/On/OPT-On		Off	VTF2 supervision
[CTSVEN]	Off/ALM&BLK/ALM		ALM	AC input imbalance monitoring (current)
[V0SVEN]	Off/ALM&BLK/ALM		ALM	AC input imbalance monitoring (Vo)
[V2SVEN]	Off/ALM&BLK/ALM		ALM	AC input imbalance monitoring (V2)
[TCSPEN]	Off/On/OPT-On		Off	Trip circuit supervision
[CBSMEN]	Off/On		Off	CB condition supervision
[TCAEN]	OFF/ON		OFF	Trip count alarm
[∑lyAEN]	OFF/ON		OFF	\sum l ^y count alarm
[OPTAEN]	OFF/ON	<'O	OFF	Operate time alarm
TCALM	1 - 10000	1	10000	Trip count alarm threshold setting
Σ ly ALM	10 – 10000 E6	E6	10000	\sum l ^y alarm threshold setting
YVALUE	1.0 – 2.0	0.1	2.0	y value setting
OPTALM	100 – 5000 ms	10 ms	1000 ms	Operate time alarm threshold setting

^(*) Current values shown in the parentheses are in the case of 1 A rating. Other current values are in the case of 5 A rating.

When setting the ZOVF and EFF, the maximum detection sensitivity of each element should be set with a margin of 15 to 20% taking account of variations in the system voltage, the asymmetry of the primary system and CT and VT error.

3.4 Recording Function

The GRD140 is provided with the following recording functions:

Fault recording

Event recording

Disturbance recording

Counters

These records are displayed on the LCD of the relay front panel or on the local or remote PC.

3.4.1 Fault Recording

Fault recording is started by a tripping command of the GRD140 and the following items are recorded for one fault:

Date and time

Trip mode

Operating phase

Fault location

Relevant events

Power system quantities

Up to the 8 most-recent faults are stored as fault records. If a new fault occurs when 8 faults have been stored, the record of the oldest fault is deleted and the record of the latest fault is then stored.

Date and time occurrence

This is the time at which a tripping command has been initiated.

The time resolution is 1 ms using the relay internal clock.

Trip mode

This shows the protection scheme such as OC1, EF1, UV1 etc. that output the tripping command.

Operating phase

This is the phase to which a tripping command is output.

Fault location

The distance to the fault point calculated by the fault locator is recorded.

The distance is expressed in km and as a percentage (%) of the line length.

Relevant events

Such events as autoreclose, re-tripping following the reclose-on-to-a fault or autoreclose are recorded with time-tags.

Power system quantities

The following power system quantities in pre-faults and post-faults are recorded.

- Magnitude and phase angle of phase voltage (Va, Vb, Vc)
- Magnitude and phase angle of phase-to-phase voltage (Vab, Vbc, Vca)
- Magnitude and phase angle of symmetrical component voltage (V₁, V₂, V₀)

- Magnitude and phase angle of zero sequence voltage which is measured directly in the form of the system residual voltage (V_e)
- Magnitude and phase angle of phase current (I_a, I_b, I_c)
- Magnitude and phase angle of symmetrical component current (I₁, I₂, I₀)
- Magnitude and phase angle of zero sequence current from residual circuit (Ie)
- Magnitude and phase angle of zero sequence current from core balance CT (I_{se}) for model 110 and 420 series
- Percentage of thermal capacity (THM%) only recorded at post-fault
- Frequency (f)

The displayed power system quantities depend on [APPL-CT] and [APPL-VT] setting for models 400 and 420 as shown in Table 3.4.1.

[APPL-VT] [APPL-CT] Power system quantities 3P 2P 3PN 3PV Phase voltage Va, Vb, Vc V_a , V_b , V_c Phase-to-phase voltage Residual voltage Symmetrical component voltage V_1, V_2, V_0 Phase current Zero sequence current from I_e (*) or I_e (*) or residual circuit $I_{e}, I_{se}(**)$ $I_{e}, I_{se}(**)$ Symmetrical component current Percentage of thermal capacity THM

Table 3.4.1 Displayed Power System Quantities

Note: (*) marked for Model 400. (**) marked for Model 420.

3.4.2 Event Recording

The events shown in Appendix D are recorded with the 1 ms resolution time-tag when the status changes. For BI1 to BI8 command, the user can select the recording items and their status change mode to initiate recording as below.

One of the following four modes is selectable.

	Modes	Setting
Not to record the ev	vent.	N
To record the even	t when the status changes to "operate".	0
To record the even	t when the status changes to "reset".	R
To record the even	t when the status changes both to "operate" and "reset".	В

For the setting, see the Section 4.2.6.5. The default setting is "B"

Up to 480 records can be stored. If an additional event occurs when 480 records have been stored, the oldest event record is deleted and the latest event record is then stored.

3.4.3 Disturbance Recording

Disturbance recording is started when the overcurrent, overvoltage or undervoltage starter element operates or a tripping command is initiated. The records include maximum 8 analogue signals as shown in Table 3.4.2, 32 binary signals and the dates and times at which recording started. Any binary signal shown in Appendix C can be assigned by the binary signal setting of disturbance record.

Model Model 420 Model 110 Model 400 **APPL** setting APPL CT = 1P I_0 $I_e(I_0)$, $I_{se}(I_0)$ CT APPL CT = 2P $I_{e}(I_{0}), I_{se}(I_{0})$ a, Ic, Ie(I₀), Ise(I₀) $I_a, I_c, I_e(I_0)$ APPL CT = 3P $I_a, I_b, I_c, I_e(I_0)$ $I_a, I_b, I_c, I_{se}(I_0)$ V_a , V_b , V_c APPL VT = 3PN V_a, V_b, V_c VT $V_e(V_0)$ APPL VT = 3PV V_a , V_b , V_c , $V_e(V_0)$

Table 3.4.2 Analog Signals for Disturbance Recording

The LCD display only shows the dates and times of disturbance records stored. Details can be displayed on a PC. For how to obtain disturbance records on the PC, see the PC software instruction manual.

The pre-fault recording time is fixed at 0.3s and post-fault recording time can be set between 0.1 and 3.0s

The number of records stored depends on the post-fault recording time. The approximate relationship between the post-fault recording time and the number of records stored is shown in Table 3.4.2.

Note: If the recording time setting is changed, the records stored so far are deleted.

Table 3.4.2 Post Fault Recording Time and Number of Disturbance Records Stored

Recording time	0.1s	0.5s	1.0s	1.5s	2.0s	2.5s	3.0s
50Hz	40	23	14	10	8	6	5
60Hz	38	19	11	8	6	5	4

Settings

The elements necessary for initiating a disturbance recording and their setting ranges are shown in the table below.

Element	Range	Step	Default	Remarks
OC	0.1-250.0 A	0.1 A	10.0 A	Overcurrent detection
	(0.02-50.00 A	0.01 A	2.00 A) (*)	
EF	0.1-125.0 A	0.1 A	3.0 A	Earth fault detection
	(0.02-25.00 A	0.01 A	0.60A)	
SEF	0.01-1.00 A	0.01 A	1.00 A	Sensitive earth fault detection
	(0.002-0.200 A	0.001 A	0.200 A)	
NC	0.5-10.0 A	0.1 A	2.0 A	Negative sequence overcurrent detection
	(0.10-2.00 A	0.01 A	0.40 A)	

Element	Range	Step	Default	Remarks
OV	10.0-200.0 V	0.1 V	120.0 V	Overvoltage detection
UV	1.0-130.0 V	0.1 V	60.0 V	Undervoltage detection
ZOV	1.0-130.0 V	0.1 V	20.0 V	Zero sequence overvoltage detection
NOV	1.0-130.0 V	0.1 V	20.0 V	Negative sequence overvoltage detection

^(*) Current values shown in the parentheses are for the case of a 1A rating. Other current values are for the case of a 5A rating.

Starting the disturbance recording by a tripping command or the starter element listed above is enabled or disabled by setting the following scheme switches.

Element	Range	Step	Default	Remarks
[Trip]	OFF/ON		ON	Start by tripping command
[BI]	OFF/ON		ON	Start by Binary Input signal
[OC]	OFF/ON		ON	Start by OC operation
[EF]	OFF/ON		ON	Start by EF operation
[SEF]	OFF/ON		ON	Start by SEF operation
[NC]	OFF/ON		ON	Start by NC operation
[OV]	OFF/ON		ON	Start by OV operation
[UV]	OFF/ON		ON	Start by UV operation
[ZOV]	OFF/ON		ON	Start by ZOV operation
[NOV]	OFF/ON		ON	Start by NOV operation

3.5 Metering Function

The GRD140 measures current and demand values of phase currents, phase and phase-to-phase voltages, residual current, residual voltage, symmetrical component currents and voltages, frequency, power factor, active and reactive power, and apparent power. The measurement data shown below is displayed on the LCD of the relay front panel or on the local or remote PC.

Current

The following quantities are measured and updated every second.

- Magnitude and phase angle of phase current (I_a, I_b, I_c)
- Magnitude and phase angle of zero sequence current from residual circuit (Ie)
- Magnitude and phase angle of zero sequence current from core balance CT (I_{se}) for model 110 and 420 series
- Magnitude of positive and negative sequence currents (I₁, I₂)
- The ratio of negative to positive sequence current (I₂/I₁)
- Magnitude and phase angle of phase voltage (Va, Vb, Vc)
- Magnitude and phase angle of phase-to-phase voltage (Vab, Vbc, Vca)
- Magnitude and phase angle of zero sequence voltage which is measured directly in the form of the system residual voltage (V_e)
- Magnitude and phase angle of symmetrical component voltage (V₁, V₂, V₀)
- Active power (P)
- Reactive power (Q)
- Apparent power (S)
- Power factor (PF)
- Frequency (f)
- Percentage of thermal capacity (THM%)
- Direction of each current (I_a, I_b, I_c, I_e, I_{se}, I₂)

Demand

- Maximum and minimum of phase voltage (V_a, V_b, V_c: max, min)
- Maximum and minimum of zero sequence voltage (V₀: max, min)
- Maximum and minimum of zero sequence voltage which is measured directly in the form of the system residual voltage (Ve: max, min)
- Maximum of phase current (I_a, I_b, I_c: max.)
- Maximum of zero sequence current from residual circuit (I_e: max)
- Maximum of zero sequence current from core balance CT (Ise: max) for model 110 and 420 series
- Maximum of negative sequence current (I2: max.)
- Maximum of the ratio of negative to positive sequence current (I₂/I₁(I₂1): max)
- Maximum of active power (P: max.)
- Maximum of reactive power (Q: max.)
- Maximum of apparent power (S: max.)
- Maximum and minimum of frequency (f: max, min)

The above system quantities are displayed in values on the primary side or on the secondary side as determined by a setting. To display accurate values, it is necessary to set the CT ratio as well.

For the setting method, see "Setting the metering" in 4.2.6.6 and "Setting the parameter" in 4.2.6.7. In the case of the maximum and minimum values display above, the measured quantity is averaged over a rolling 15 minute time window, and the maximum and minimum recorded average values are shown on the display screen.

The displayed quantities depend on [APPL-CT] and [APPL-VT] setting as shown in Table 3.5.1. Input current and voltage greater than 0.01×In(rated current) and 0.06V at the secondary side are required for the measurement.

The zero sequence current I_e in "3P" setting of the model 420 is calculated from the three phase input currents and the calculated I_e (I_0) is displayed. The I_e displayed in other settings and models is the current fed from CT.

Phase angles above are expressed taking the positive sequence voltage as a reference phase angle, where leading phase angles are expressed as positive, (+).

The signing of active and reactive power flow direction can be set positive for either power sending or power receiving. The signing of reactive power can be also set positive for either lagging phase or leading phase.

Table 3.5.1 Displayed Quantity Depends on APPL setting

Model	110		400	,		420		400,	420
APPL setting		A	APPL-C	T	7	APPL-C	T	APP	L-VT
Quantity		1P	2P	3P	1P	2P	3P	3PN	3PV
la			✓ •	√		✓	✓		
lb				~			✓		
Ic			1	V		✓	✓		
le (lo)			✓	✓	✓	✓	✓		
lse	•				✓	✓	✓		
l1			•	✓			✓		
12				✓			✓		
12/11				✓			✓		
Va								✓	✓
Vb								✓	✓
Vc								✓	✓
Vab								✓	✓
Vbc								✓	✓
Vca								✓	✓
Ve									✓
V1								✓	✓
V2								✓	✓
V0								✓	✓
P			✓	✓		✓	✓	✓	✓
Q			✓	✓		✓	✓	✓	✓
S			✓	✓		✓	✓	✓	✓
PF			✓	✓		✓	✓	✓	✓
f								✓	✓
THM			✓	✓					

3.6 Fault locator

3.6.1 Application

The fault locator incorporated in the GRD140 measures the distance to fault on the protected line using local voltages and currents. The measurement result is expressed as a percentage (%) of the line length and the distance (km) and is displayed on the LCD on the relay front panel. It is also output to a local PC or RSM (relay setting and monitoring) system.

To measure the distance to fault, the fault locator requires minimum 3 cycles as fault duration time.

In distance to fault calculations, the change in the current before and after the fault has occurred is used as a reference current, alleviating influences of the load current and arc voltage. As a result, the location error is a maximum of ± 2.5 km for faults at a distance of up to 100 km, and a maximum of $\pm 2.5\%$ for faults at a distance between 100 km and 250 km.

The fault locator is available for [APPL-CT]= "3P" and [APPL-VT]= "3PN" or "3PV" setting.

The fault locator cannot correctly measure the distance to fault during a power swing.

3.6.2 Distance to Fault Calculation

The distance to fault x_1 is calculated from equation (1) and (2) using the voltage and current of the fault phase and a current change before and after the fault occurrence. The current change before and after the fault occurrence represented by $I\beta$ " and $I\alpha$ " is used as the reference current. The impedance imbalance compensation factor is used to maintain high measuring accuracy even when the impedance of each phase has great variations.

Distance calculation for phase fault (in the case of BC-phase fault)

$$x_1 = \frac{I_{\mathbf{m}}(\mathbf{V}_{\mathbf{bc}} \cdot \mathbf{I}\boldsymbol{\beta}^{"}) \times \mathbf{L}}{\{I_{\mathbf{m}}(\mathbf{R}_1 \cdot \mathbf{I}_{\mathbf{bc}} \times \mathbf{I}\boldsymbol{\beta}^{"}) + \mathbf{R}_{\mathbf{c}}(\mathbf{X}_1 \cdot \mathbf{I}_{\mathbf{bc}} \cdot \mathbf{I}\boldsymbol{\beta}^{"})\} \times \mathbf{K}_{\mathbf{bc}}}$$
(1)

where.

 V_{bc} = fault voltage between faulted phases = $V_b - V_c$

 I_{bc} = fault current between faulted phases = $I_b - I_c$

 $I\beta'' = \text{change of fault current before and after fault occurrence} = (I_b - I_c) - (I_L - I_L - I_C)$

 $I_{I,b}$, $I_{I,c} = load$ current

R₁ = resistance component of line positive sequence impedance

 X_1 = reactance component of line positive sequence impedance

 K_{bc} = impedance imbalance compensation factor

 $I_{m}()$ = imaginary part in parentheses

 $R_e()$ = real part in parentheses

L = line length (km)

Distance calculation for earth fault (in the case of A-phase earth fault)

$$x_{1} = \frac{I_{m}(V_{a} \cdot I_{\alpha}") \times L}{\{I_{m}(R_{1} \cdot I_{\alpha} \cdot I_{\alpha}" + R_{0} \cdot I_{0S} \cdot I_{\alpha}") + R_{e}(X_{1} \cdot I_{\alpha} \cdot I_{\alpha}" + X_{0} \cdot I_{0S} \cdot I_{\alpha}")\} \times K_{a}}$$
(2)

where,

 V_a = fault voltage

 I_{α} = fault current = $(2I_a - I_b - I_c)/3$

 I_{α} " = change of fault current before and after fault occurrence

$$= \frac{2I_{a} - I_{b} - I_{c}}{3} - \frac{2I_{La} - I_{Lb} - I_{Lc}}{3}$$

 I_a , I_b , I_c = fault current

 I_{La} , I_{Lb} , I_{Lc} = load current

 I_{0s} = zero sequence current

 R_1 = resistance component of line positive sequence impedance

 X_1 = reactance component of line positive sequence impedance

 R_0 = resistance component of line zero sequence impedance

 X_0 = reactance component of line zero sequence impedance

 K_a = impedance imbalance compensation factor

 $I_{m}()$ = imaginary part in parentheses

 $R_e()$ = real part in parentheses

L = line length (km)

Equations (1) and (2) are general expressions when lines are treated as having lumped constants and these expressions are sufficient for lines within 100 km. For lines exceeding 100 km, influences of the distributed capacitance must be considered. For this fault locator, the following equation is used irrespective of line length to find the compensated distance x_2 with respect to distance x_1 which was obtained in equation (1) or (2).

$$x_2 = x_1 - k^2 \cdot \frac{x_1^3}{3}$$
 (3)

where

 $k \neq \text{propagation constant of the protected line} = 0.001 \text{km}^{-1} \text{ (fixed)}$

3.6.3 Starting Calculation

Calculation of the fault location is initiated by tripping signals.

3.6.4 Displaying Location

The measurement result is stored in the "Fault record" and displayed on the LCD of the relay front panel or on the local or remote PC. For displaying on the LCD, see Section 4.2.3.1.

3.6.5 Setting

The setting items necessary for the fault location and their setting ranges are shown in the table below. The reactance and resistance values are input in expressions on the secondary side.

When there are great variations in the impedance of each phase, equation (4) is used to find the positive sequence impedance, zero sequence impedance and zero sequence mutual impedance, while equation (5) is used to find imbalance compensation factors K_{ab} to K_a .

When variations in impedance of each phase can be ignored, the imbalance compensation factor is set to 100%.

$$Z_{1} = \{(Z_{aa} + Z_{bb} + Z_{cc}) - (Z_{ab} + Z_{bc} + Z_{ca})\}/3$$

$$Z_{0} = \{(Z_{aa} + Z_{bb} + Z_{cc}) + 2(Z_{ab} + Z_{bc} + Z_{ca})\}/3$$

$$K_{ab} = \{(Z_{aa} + Z_{bb})/2 - Z_{ab}\}/Z_{1}$$

$$K_{bc} = \{(Z_{bb} + Z_{cc})/2 - Z_{bc}\}/Z_{1}$$

$$K_{ca} = \{(Z_{cc} + Z_{aa})/2 - Z_{ca}\}/Z_{1}$$

$$K_{a} = \{(Z_{aa} - (Z_{ab} + Z_{ca})/2\}/Z_{1}$$

$$K_{b} = \{(Z_{bb} - (Z_{bc} + Z_{ab})/2\}/Z_{1}$$

$$K_{c} = \{(Z_{cc} - (Z_{ca} + Z_{ab})/2\}/Z_{1}$$

Item	Range	Step	Default	Remarks
R ₁	0.0 - 199.99 Ω	0.01 Ω	0.20Ω	
	(0.0 - 999.9 Ω	0.1 Ω	1.0Ω) (*)	
X ₁	0.0 - 199.99 Ω	0.01 Ω	2.00Ω	
	(0.0 - 999.9 Ω	0.1 Ω	$10.0\Omega)$	
R ₀	0.0 - 999.99 Ω	0.01Ω	0.70Ω	
	$(0.0$ - 999.9 Ω	0.1 Ω	3.5Ω)	
Х0	0.0 - 199.99 Ω	0.01 Ω	6.80Ω	
. ($(0.0$ - 999.9 Ω	0.1 Ω	$34.0\Omega)$	
K _{ab}	80 - 120%	1%	100%	
K _{bc}	80 - 120%	1%	100%	
K _{ca}	80 - 120%	1%	100%	
Ka	80 - 120%	1%	100%	
Kb	80 - 120%	1%	100%	
K _C	80 - 120%	1%	100%	
Line	0 - 399.9 km	0.1 km	50.0km	

^(*) Ohmic values shown in the parentheses are in the case of 1 A rating. Other ohmic values are in the case of 5A rating.

TOSHIBA 6 F 2 S 0 7 5 8

4. User Interface

4.1 Outline of User Interface

The user can access the relay from the front or rear panel.

Local communication with the relay is also possible using a personal computer (PC) via an RS232C port. Furthermore, remote communication is also possible using RSM (Relay Setting and Monitoring) or IEC60870-5-103 communication via RS485 port.

This section describes the front panel configuration and the basic configuration of the menu tree of the local human machine communication ports and HMI (Human Machine Interface).

4.1.1 Front Panel

As shown in Figure 3.1.3, the front panel is provided with a liquid crystal display (LCD), light emitting diodes (LED), operation keys, and RS-232C connector.

LCD

The LCD screen, provided with a 2-line, 16-character display and back-light, provides the user with information such as records, statuses and settings. The LCD screen is normally unlit, but pressing the VIEW key will display the digest screen and pressing any key other than VIEW and RESET will display the menu screen.

These screens are turned off by pressing the RESET key or END key. If any display is left for 5 minutes or longer without operation, the back-light will go off.

LED

There are 6 LED displays. The signal labels and LED colors are defined as follows:

Label	Color 🄷	Remarks
IN SERVICE	Green	Lit when the relay is in service and flickered when the relay is in "Test" menu.
TRIP	Red	Lit when a trip command is issued.
ALARM	Red	Lit when a failure is detected.
(LED1)	Yellow	
(LED2)	Yellow	
(LED3)	Yellow	

LED1, LED2 and LED3 are configurable. For the setting, see Section 4.2.6.10.

The TRIP LED lights up once the relay is operating and remains lit even after the trip command goes off. The TRIP LED can be turned off by pressing the RESET key. Other LEDs are lit as long as a signal is present and the RESET key is invalid while the signal is being maintained.

Operation keys

The operation keys are used to display records, status, and set values on the LCD, as well as to input or change set values. The function of each operation key is as follows:

① ▼, ▲, ◀, ▶: Used to move between lines displayed on a screen and to enter numerical values and text strings.

② (CANCEL): Used to cancel entries and return to the upper screen.

③ END: Used to end the entering operation, return to the upper screen or turn off the display.

(4) ENTER: Used to store or establish entries.

VIEW and RESET keys

Pressing VIEW key displays digest screens such as "Metering", "Latest fault", "Auto-supervision", "Alarm display" and "Indication".

Pressing RESET key turns off the display.

Monitoring jacks

The two monitoring jacks A and B and their respective LEDs can be used when the test mode is selected on the LCD screen. By selecting the signal to be observed from the "Signal List" and setting it on the screen, the signal can be displayed on LED A or LED B, or transmitted to an oscilloscope via a monitoring jack.

RS232C connector

The RS232C connector is a 9-way D-type connector for serial RS232C connection with a local personal computer.

4.1.2 Communication Ports

The following two interfaces are mounted as communication ports:

- RS232C port
- RS485 port

RS232C port

This connector is a standard 9-way D-type connector for serial port RS232C transmission and is mounted on the front panel. By connecting a personal computer to this connector, setting operation and display functions can be performed.

RS485 port

The RS485 port is used for the RSM (Remote Setting and Monitoring system) via the protocol converter G1PR2 and IEC60870-5-103 communication via BCU/RTU (Bay Control Unit / Remote Terminal Unit) to connect between relays and to construct a network communication system. (See Figure 4.4.1 in Section 4.4.)

One or two RS485 ports (COM1 and COM2) is provided on the rear of the relay as shown in Figure 4.1.1. In the relay provided with two RS485 ports, COM1 is used for the RSM or IEC60870-5-103 communication, and COM2 used for IEC60870-5-103 communication. When the COM1 is used for IEC60870-5-103 communication, the COM2 cannot be used for IEC60870-5-103 communication.

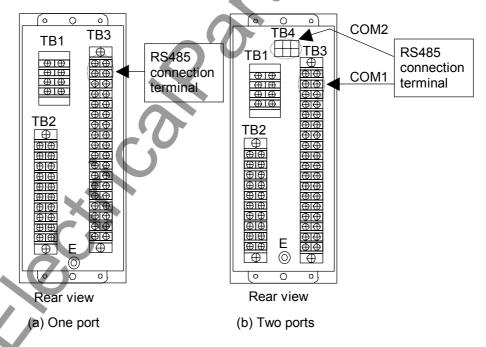


Figure 4.1.1 Location of RS485 Port

4.2 Operation of the User Interface

The user can access such functions as recording, measurement, relay setting and testing with the LCD display and operation keys.

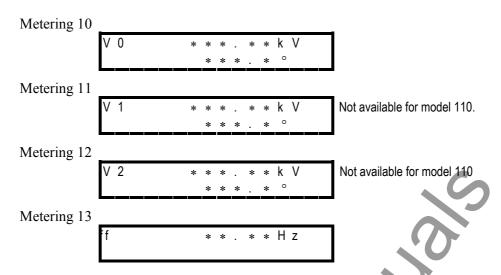
4.2.1 LCD and LED Displays

Displays during normal operation

When the GRD140 is operating normally, the green "IN SERVICE" LED is lit and the LCD is off.

Press the (VIEW) key when the LCD is off to display the digest screens which are "Indication", "Metering1", "Metering2", "Metering3", "Metering4", "Metering5", "Latest fault", "Auto-supervision" and "Alarm Display" screens in turn. "Latest fault", "Auto-supervision" and "Alarm Display" screens are displayed only when there is some data. The following are the digest screens and can be displayed without entering the menu screens.

Indication		
marcation	IND1[0000 0000]	
	IND2 0001 0000	J O .
Metering 1		
-	la **.** k A	Not available for model 110 and APPL=1P
		setting in models 400 and 420.
Metering 2		_
	l b * * . * * k A	Not available for model 110, and APPL=1P and 2P settings in models 400 and 420.
		Settings in models 400 and 420.
Metering 3	I C ** * * K A	Not evailable for model 440 and ADDL -4D
	I c * * * * * K A	Not available for model 110 and APPL=1P setting in models 400 and 420.
Metering 4		
Metering 4	l e * * * * * k A	7
Metering 5		
	l s e * * * * * * K A	Not available for model 400.
Metering 6		
1/6	V a n * * * . * * k V	Available for APPL=3PN and 3PV settings in models 400 and 420.
	* * * . * °	models 400 and 420.
Metering 7	h	-
	V b n * * * . * * k V	Available for APPL=3PN and 3PV settings in models 400 and 420.
*		modele 100 dita 120.
Metering 8	V o n	Available for ADDI = 2DN and 2DV settings in
	V c n * * * . * * k V * * * . * °	Available for APPL=3PN and 3PV settings in models 400 and 420.
Matarina 0		·
Metering 9	V e * * * * * K V	⊣
	* * * . * °	

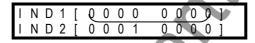


To clear the latched indications (LEDs, LCD screen of Latest fault), press (RESET) key for 3 seconds or more.

For any display, the back-light is automatically turned off after five minutes.

Indication

This screen shows the status of elements assigned as a virtual LED.



Status of element

Elements depend on user setting. 1: Operate, 0: Not operate (Reset)

Displays in tripping

Latest fault



If a fault occurs and a tripping command is output when the LCD is off, the red "TRIP" LED and other configurable LED if signals assigned to trigger by tripping

Press the VIEW key to scroll the LCD screen to read the rest of messages.

Press the RESET key to turn off the LEDs and LCD display.

Notes:

- When configurable LEDs (LED1 through LED3) are assigned to latch signals by trigger of tripping, press the RESET key more than 3s until the LCD screens relight. Confirm turning off the configurable LEDs. Refer to Table 4.2.1 Step 1.
- Then, press the (RESET) key again on the "Latest fault" screen in short period, confirm turning off the "TRIP" LED. Refer to Table 4.2.1 Step 2.
- 3) When only the "TRIP" LED is go off by pressing the RESET key in short period, press the RESET key again to reset remained LEDs in the manner 1) on the "Latest fault" screen or other digest screens. LED1 through LED3 will remain lit in case the assigned signals are still active state.

		LED ligh	ting status
	Operation	"TRIP" LED	Configurable LED (LED1 – LED3)
Step 1	Press the RESET key more than 3s on the "Latest fault" screen	*	*
		continue to lit	turn off
Step 2	Then, press the RESET key in short period on the "Latest fault" screen		10
		turn off	

Table 4.2.1 Turning off latch LED operation

When any of the menu screens is displayed, the VIEW and RESET keys do not function.

To return from menu screen to the digest "Latest fault" screen, do the following:

- Return to the top screen of the menu by repeatedly pressing the END key.
- Press the END key to turn off the LCD.
- Press the VIEW key to display the digest "Latest fault" screen.

Auto-supervision

If the automatic supervision function detects a failure while the LCD is off, the "Auto-supervision" screen is displayed automatically, showing the location of the failure, and the "ALARM" LED lights.

Press the VIEW key to display other digest screens in turn including the "Metering" and "Latest fault" screens.

Press the RESET key to turn off the LEDs and LCD display. However, if the failure continues, the "ALARM" LED remains lit.

After recovery from a failure, the "ALARM" LED and "Auto-supervision" display turn off automatically.

If a failure is detected while any of the screens is displayed, the current screen remains displayed and the "ALARM" LED lights.

Notes:

- 1) When configurable LEDs (LED1 through LED3) are assigned to latch signals by issuing an alarm, press the (RESET) key more than 3s until all LEDs reset except "IN SERVICE" LED.
- 2) When configurable LED is still lit by pressing (RESET) key in short period, press (RESET) key again to reset remained LED in the above manner.
- 3) LED1 through LED3 will remain lit in case the assigned signals are still active state.

While any of the menu screens is displayed, the VIEW and RESET keys do not function. To

return to the digest "Auto-supervision" screen, do the following:

- Return to the top screen of the menu by repeatedly pressing the END key.
- Press the END key to turn off the LCD.
- Press the VIEW key to display the digest screen.

Alarm Display

Alarm Display (ALM1 to ALM4)



The four alarm screens can be provided, and their text messages are defined by user. (For setting, see Section 4.2.6.8) These alarms are raised by associated binary inputs.

Press the <u>VIEW</u> key to display other digest screens in turn including the "Metering" and "Latest fault" screens.

To clear the Alarm Display, press RESET key. The clearing is available after displaying up to ALM4.

4.2.2 Relay Menu

Figure 4.2.1 shows the menu hierarchy in the GRD140. The menu has five sub-menus, "Record", "Status", "Set. (view)", "Set. (change)", and "Test". For details of the menu hierarchy, see Appendix E.

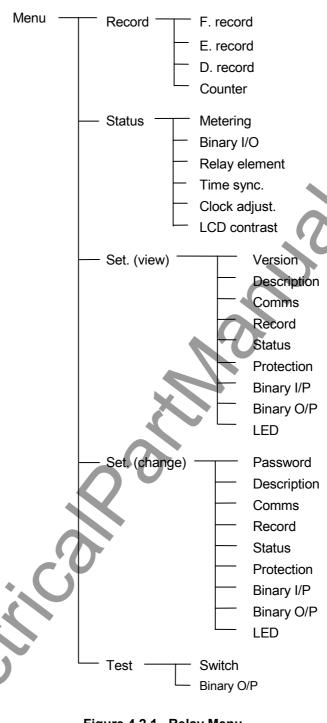


Figure 4.2.1 Relay Menu

Record

In the "Record" menu, the fault records event records, disturbance records and counts such as trip count.

Status

The "Status" menu displays the power system quantities, binary input and output status, relay measuring element status, signal source for time synchronisation (BI, RSM or IEC60870-5-103), clock adjustment and LCD contrast.

Set. (view)

The "Set. (view)" menu displays the relay version, description, relay address and baud rate in RSM or IEC60870-5-103 communication, the current settings of record, status, protection, binary inputs, configurable binary outputs and configurable LEDs.

Set. (change)

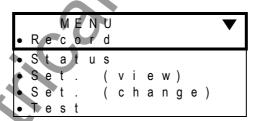
The "Set. (change)" menu is used to change the settings of password, description, relay address and baud rate in RSM or IEC60870-5-103 communication, record, status, protection, binary inputs, configurable binary outputs and configurable LEDs.

Since this is an important menu and is used to change settings related to relay tripping, it has password security protection.

Test

The "Test" menu is used to set testing switches and to forcibly operate binary output relays.

When the LCD is off, press any key other than the <u>(VIEW)</u> and <u>(RESET)</u> keys to display the top "MENU" screen and then proceed to the relay menus.

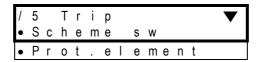


To display the "MENU" screen when the digest screen is displayed, press the (RESET) key to turn off the LCD, then press any key other than the (VIEW) and (RESET) keys.

Press the END key when the top screen is displayed to turn off the LCD.

An example of the sub-menu screen is shown below. The top line shows the hierarchical layer. The last item is not displayed for all the screens. "\(\neg \)" or "\(\textit{\Lambda}\)" displayed on the far right shows that lower or upper lines exist.

To move the cursor downward or upward for setting or for viewing other lines not displayed on the window, use the ∇ and \triangle keys.



To return to the higher screen or move from the right side screen to the left side screen in Appendix

E, press the END key.

The CANCEL key can also be used to return to the higher screen but it must be used carefully because it may cancel entries made so far.

To move between screens of the same hierarchical depth, first return to the higher screen and then move to the lower screen.

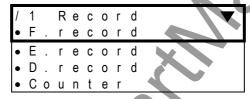
4.2.3 Displaying Records

The sub-menu of "Record" is used to display fault records, event records, disturbance records and counts such as trip count, Σ Iy count and reclose count.

4.2.3.1 Displaying Fault Records

To display fault records, do the following:

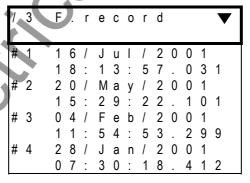
- Open the top "MENU" screen by pressing any keys other than the VIEW and RESET keys.
- Select "Record" to display the "Record" sub-menu.



• Select "F. record" to display the "F. record" screen.



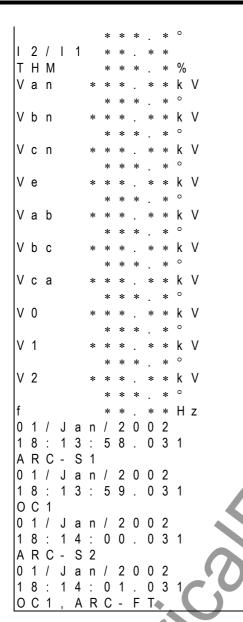
• Select "Display" to display the dates and times of fault records stored in the relay from the top in new-to-old sequence.



• Move the cursor to the fault record line to be displayed using the ▲ and ▼ keys and press the ENTER key to display the details of the fault record.

Ī	/ 0	4	1		a								#	1	▼]
	0	8 C	: 1	1	3		5	7				1				Trip element
	*	h * r	a * e		e * a		m	B (t		* V	* a	% I	,	е	s	Not available for model 110. Not available for model 110.
		a	J	•	u	ŭ	*	*	*	*	*	k °	A	Ū	Ü	Not available for model 110 and APPL=1P setting in models 400 and 420.
		b					*	*	*	*	*	0	A			Not available for model 110 and APPL=1P and 2P settings in models 400 and 420.
		c e					* *	* *	*	* .	* *	0	A A			Not available for model 110 and APPL=1P setting in models 400 and 420.
	I	s	е			*	*	*	*	*	* *	。 k 。	Α			Not available for model 400.
	I	1					*	*	. *	*	*		Α			Not available for model 110 and APPL=1P and 2P settings in models 400 and 420.
		2	,		4		*	*	*	*	*	k °	Α			Not available for model 110 and APPL=1P and 2P settings in models 400 and 420.
,	•	a	n	I	1	*	* *	* *	. *	*	* *	k °	V			Not available for model 110 and APPL=1P and 2P settings in models 400 and 420. Not available for model 110 and APPL=3P and 2P settings in models 400 and 420.
		b				*	*	*	*	*	*	0	٧			Not available for model 110 and APPL=3P and 2P settings in models 400 and 420.
	V V	c e	n			*	* *	* *	*	* *	* *	0	V			Not available for model 110 and APPL=3P and 2P settings in models 400 and 420.
,	V	а	b			*	*	*	*	*	*	° k	٧	4	<	Not available for model 110.
,	V	b	С			*	* *	* *	* .	*	* *	∘ k ∘	٧		7)	Not available for model 110.
		С	а			*	*	*	*	*	*	k °	٧			Not available for model 110.
	V V					*	* *	* *	*	*	* *	κ ∘ k	V			Not available for model 110. Not available for model 110.
,	V	2				*	*	*	*	*	*	o k	٧			Not available for model 110.
	f F	а	u	À	t		* * V	* *). 	* U	* * e	° H s	z			Not available for model 110.
	I	а		<			*	*	*	*	*	k ∘	A			Not available for model 110 and APPL=1P setting in models 400 and 420.
		b c					* *	* *	*	* *	* *	0	A A			Not available for model 110 and APPL=1P and 2P settings in models 400 and 420. Not available for model 110 and APPL=1P setting in models 400 and 420.
		е	~				*	*	*		*	° k	Α			
>	l	s	е			*	* *	. *	* *	*	* *	∘ k ∘	Α			Not available for model 400.
	I	1					*	*	*	*	*	0	Α			Not available for model 110 and APPL=1P and 2P settings in models 400 and 420.
	I	2					*	*	٠	*	*	k	A			Not available for model 110 and APPL=1P and 2P settings in models 400 and 420.

TOSHIBA 6 F 2 S 0 7 5 8



Not available for model 110 and APPL=1P and 2P settings in models 400 and 420. Not available for model 110.

Not available for model 110 and APPL=3P and 2P settings in models 400 and 420

Not available for model 110 and APPL=3P and 2P settings in models 400 and 420.

Not available for model 110 and APPL=3P and 2P settings in models 400 and 420.

Not available for model 110.

The lines which are not displayed in the window can be displayed by pressing the \triangle and ∇ keys.

To clear all the fault records, do the following:

- Open the "Record" sub-menu.
- Select "F. record" to display the "F. record" screen.
- Select "Clear" to display the following confirmation screen.

Clear records? END=Y CANCEL=N

• Press the END (= Y) key to clear all the fault records stored in non-volatile memory.

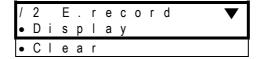
If all fault records have been cleared, the "Latest fault" screen of the digest screens is not displayed.

Note: When changing the units (kA/A) of primary side current with RSM100, press the "Units" button which is indicated in the primary side screen.

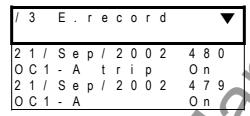
4.2.3.2 Displaying Event Records

To display event records, do the following:

- Open the top "MENU" screen by pressing any keys other than the (VIEW) and (RESET) keys
- Select "Record" to display the "Record" sub-menu.
- Select "E. record" to display the "E. record" screen.



• Select "Display" to display the events with date from the top in new-to-old sequence.



The time is displayed by pressing the key.

/	3		Ε		r	е	С	0	r	d			
1	3	:	2	2	:	4	5		2	Ì	1	V)
0	С	1	-	Α		t	r		р	٩,		0	n
1	3	:	2	2	:	4	5		1	0	9		
0	С	1	-	Α				•		厂		0	n

Press the ◀ key to return the screen with date.

The lines which are not displayed in the window can be displayed by pressing the \triangle and ∇ keys.

To clear all the event records, do the following:

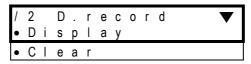
- Open the "Record" sub-menu.
- Select "E. record" to display the "E. record" screen.
- Select "Clear" to display the following confirmation screen.

• Press the END (= Y) key to clear all the event records stored in non-volatile memory.

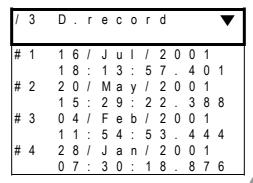
4.2.3.3 Displaying Disturbance Records

Details of disturbance records can be displayed on the PC screen only (*); the LCD displays only the recorded date and time for all disturbances stored in the relay. They are displayed in the following sequence.

- (*) For the display on the PC screen, refer to RSM100 manual.
- Open the top "MENU" screen by pressing any keys other than the VIEW and RESET keys.
- Select "Record" to display the "Record" sub-menu.
- Select "D. record" to display the "D. record" screen.



• Select "Display" to display the date and time of the disturbance records from the top in new-to-old sequence.



The lines which are not displayed in the window can be displayed by pressing the \triangle and ∇ keys.

To clear all the disturbance records, do the following:

- Open the "Record" sub-menu.
- Select "D. record" to display the "D. record" screen.
- Select "Clear" to display the following confirmation screen.

• Press the END (= Y) key to clear all the disturbance records stored in non-volatile memory.

4.2.3.4 Displaying Counter

- Open the top "MENU" screen by pressing any keys other than the VIEW and RESET keys.
- Select "Record" to display the "Record" sub-menu.
- Select "Counter" to display the "Counter" screen.

_	2 D						е	r			•	7
• • • • • • •	C C		e e e e e e	a a a a a a	r r r r r	T T T Σ Σ	r r l l	i i ^ ^	р р у у	s s A B C	A B C	(*) (*) (*)

- (*) Note: These settings are only available when single phase External Trip BI functions are used. In this case, the main "Clear Trips" option is not available.
- Select "Display" to display the counts stored in the relay.



(*) Note: These settings are only available when single phase External Trip BI functions are used. In this case, the main "Trips" option is not available.

The lines which are not displayed in the window can be displayed by pressing the **\(\Lambda \)** and **\(\V** keys.

To clear each count, do the following:

- Open the "Record" sub-menu.
- Select "Counter" to display the "Counter" screen.
- Select "Clear Trips" to display the following confirmation screen.

• Select "Clear Trips A" to display the following confirmation screen.

• Select "Clear Trips B" to display the following confirmation screen.

• Select "Clear Trips C" to display the following confirmation screen.

• Select "Clear Σ I^yA" to display the following confirmation screen.

C | e a r
$$\Sigma$$
 | ^ y A ?
E N D = Y C A N C E L = N

• Select "Clear $\Sigma l^{\Lambda}yB$ " to display the following confirmation screen.

• Select "Clear ∑ l^yC" to display the following confirmation screen.

• Select "Clear ARCs" to display the following confirmation screen.

• Press the END (= Y) key to clear the count stored in non-volatile memory.

4.2.4 Displaying the Status

From the sub-menu of "Status", the following status condition can be displayed on the LCD:

Metering data of the protected line, apparatus, etc.

Status of binary inputs and outputs

Status of measuring elements output

Status of time synchronisation source

Status of clock adjustment

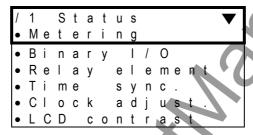
Status of LCD contrast

The data are updated every second.

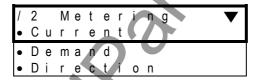
4.2.4.1 Displaying Metering Data

To display metering data on the LCD, do the following:

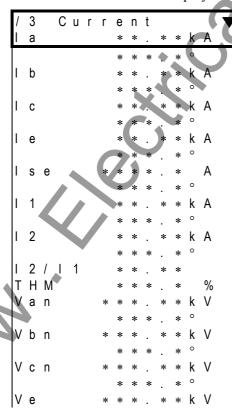
• Select "Status" on the top "MENU" screen to display the "Status" screen.



• Select "Metering" to display the "Metering" screen.



• Select "Current" to display the current power system quantities on the "Metering" screen.



Not available for model 110 and APPL=1P setting in models 400 and 420.

Not available for model 110 and APPL=1P and 2P settings in models 400 and 420.

Not available for model 110 and APPL=1P setting in models 400 and 420.

Not available for model 400.

Not available for model 110 and APPL=1P and 2P settings in models 400 and 420.

Not available for model 110 and APPL=1P and 2P settings in models 400 and 420.

Not available for model 110 and APPL=1P and 2P settings in models 400 and 420. Not available for model 110 and APPL=1P setting in models 400 and 420. Not available for model 110 and APPL=3P and 2P settings in models 400 and 420.

Not available for model 110 and APPL=3P and 2P settings in models 400 and 420.

Not available for model 110 and APPL=3P and 2P settings in models 400 and 420.

						*	*	*		*	0			
V	а	b			*	*	*		*	*	k	٧		Not available for model 110.
						*	*	*		*	0			
V	b	С			*	*	*		*	*	k	٧		Not available for model 110.
						*	*	*		*	0			
V	С	а			*	*	*		*	*	k	٧		Not available for model 110.
						*	*	*		*	0			
V	0				*	*	*		*	*	k	٧		Not available for model 110.
						*	*	*		*	0			
V	1				*	*	*		*	*	k	٧		Not available for model 110.
						*	*	*		*	0			
٧	2				*	*	*		*	*	k	٧		Not available for model 110.
						*	*	*		*	0			
f						*	*		*	*	Н	Z		Not available for model 110.
Р	F			-	*		*	*	*					Not available for model 110. Total 3 phase power factor.
Р			-	*	*	*	*	*	*	k	W	'		Not available for model 110. Total 3 phase active power.
Q			-	*	*	*	*	*	*	k	٧	а	r	Not available for model 110. Total 3 phase reactive power.
S			-	*	*	*	*	*	*	k	٧	Α		Not available for model 110. Total 3 phase apparent power.

If the primary side unit (A) is required, select 2(=Pri-A) on the "Metering" screen. See Section 4.2.6.6.

Note: When changing the units (kA/A) of primary side current with RSM100, press the "Units" button which is indicated in the primary side screen.

• Select "Demand" to display the current demand on the "Metering" screen.

/	3		D	е	m	а	n	d						V	
I	а	m	а	Х			*	*		*	*		k	Α	Not available for model 110.
I	b	m	а	Χ			*	*		*	*		k	Α	Not available for model 110.
I	С	m	а	Χ			*	*		*	*		k	A	Not available for model 110.
П	е	m	а	Χ			*	*		*	*		k	A	
П	S	е	m	а	X		*	*		*	*	*	k	A	Not available for model 400.
П	2	m	а	Χ			*	*		*	*		k	A	Not available for model 110.
	2	1	m	а	X		*	*		*	*				Not available for model 110.
P	m	а	Χ		-	*	*	*	*	*	*	K	W	1	Not available for model 110.
Q	m	-	Χ		-	*	*	*	*	*	*	K	V	a	Not available for model 110.
S	m	а	X		-	*	*	*	*	*	*	K	V	A	Not available for model 110.
V	а	n	m	a	X		*	*	*		*	*	k	V	Not available for model 110.
V	a	n	m	1	n		*	*	*	•	*	*	k	V	Not available for model 110.
\V	b	n	m	а	Х		*	*	*	•	*	*	k	V	Not available for model 110.
\V	b	n	m	1	n		*	*	*		*	*	k	V	Not available for model 110.
\V	С	n	m	а	X		*	*	*		*	*	k L	V	Not available for model 110.
V	С	n	m		n	V	*	*	*		*	*	K	V	Not available for model 110.
V	е		m	a	X	٦	*	*	*		*	*	k	V	Not available for model 110.
V	e	≤	m		n		*	*	*		*	*	k	V	Not available for model 110.
V	0	m	a	X			*	*	*	•	*	*	k	V	
V	0	m	1	n			*	*	*		*	*	K	V _	N. (11.1. (1.1.4.2
f	m	a :	X					*	*		*	*	Н	Z -	Not available for model 110.
<u>f</u>	m	L	n					*	*		*	*	Н	Z	Not available for model 110.

To clear all max data, do the following:

• Press the RESET key on any max demand screen (primary or secondary) to display the following confirmation screen.



- Press the (END) (= Y) key to clear all max data stored in non-volatile memory.
- Select "Direction" to display the direction of a current on the "Metering" screen.

The direction of each current is displayed when the directional characteristic is selected as follows:

Ia, Ib, Ic: [OC*-DIR]= "FWD" or "REV" setting

Ie: [EF*-DIR]= "FWD" or "REV" setting

Ise: [SE*-DIR]= "FWD" or "REV" setting

I2: [NC*-DIR]= "FWD" or "REV" setting

/	3		D	i	r	е	С	t	i	0	n			\blacksquare	
I	а						F	0	r	W	а	r	d		Not available for model 110.
I	b						R	е	٧	е	r	s	е		Not available for model 110.
I	С						F	0	r	W	а	r	d		Not available for model 110.
I	е						F	0	r	W	а	r	d		
1	s	е					F	0	r	W	а	r	d		Not available for model 400.
	2						_	_	_	_	_	_	_		Not available for model 110.

4.2.4.2 Displaying the Status of Binary Inputs and Outputs

To display the binary input and output status, do the following:

- Select "Status" on the top "MENU" screen to display the "Status" screen.
- Select "Binary I/O" to display the binary input and output status.

/ 2	Binary	I / 0 ▼
ΙP	0000]	0001
0 P	0 0 0 0 0	0000]

The display format is shown below.

							■]
Input (IP)	B1 B12 B01 B02	BI3	BI4	BI5	BI6	BI7	BI8
Output (OP)	BO1 BO2	BO3	BO4	BO5	BO6	BO7	FAIL

Line 1 shows the binary input status. BI1 to BI8 correspond to each binary input signal. The models 400 and 420 are available for BI1 to BI5. For the binary input signal, see Appendix H. The status is expressed with logical level "1" or "0" at the photo-coupler output circuit.

Line 2 shows the binary output status. All binary outputs BO1 to BO7 are configurable. The status of these outputs is expressed with logical level "1" or "0" at the input circuit of the output relay driver. That is, the output relay is energised when the status is "1".

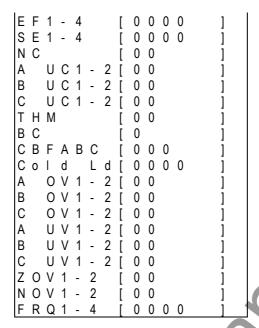
To display all the lines, press the \triangle and ∇ keys.

4.2.4.3 Displaying the Status of Measuring Elements

To display the status of measuring elements on the LCD, do the following:

- Select "Status" on the top "MENU" screen to display the "Status" screen.
- Select 3 "Ry element" to display the status of the relay elements.

/	2		R	у		е	I	е	m	е	n	t	_
Α		0	С	1	-	4	[0	0	0	0]
B C		0	С	1	-	4	[0	0	0	0]
С		0	С	1	-	4	[0	0	0	0		j



The displayed elements depend on relay model. (See Table 1.1.1 in Section 1.)

The operation status of phase and residual overcurrent elements are shown as below.

	[=			-]	
A OC1-4	OC1	OC2	OC3	OC4		A phase OC elements
B OC1-4	OC1	OC2	OC3	OC4		B phase OC elements
C OC1-4	OC1	OC2	OC3	OC4		C phase OC elements
EF1-4	EF1	EF2	EF3	EF4		
SE1-4	SE1	SE2	SE3	SE4		
NC	NC1	NC2	-	-		
A UC1-2	UC1	UC2)-	-		A phase UC elements
B UC1-2	UC1	UC2	-	-		B phase UC elements
C UC1-2	UC1	UC2	-	-		C phase UC elements
THM	Alarm	Trip	-	-		
BC	BC	-	-	-		
CBFABC	A	В	С	-		
Cold Ld	0	1	2	3		Cold Load state
A OV1-2	OV1	OV2	-	-		A phase OV elements
B OV1-2	OV1	OV2	-	-		B phase OV elements
C OV1-2	OV1	OV2	-	-		C phase OV elements
A UV1-2	UV1	UV2	-	-		A phase UV elements
B UV1-2	UV1	UV2	-	-		B phase UV elements
C UV1-2	UV1	UV2	-	-		C phase UV elements
ZOV1-2	ZOV1	ZOV2	-	-		
NOV1-2	NOV1	NOV2	-	-		
FRQ1-4	FRQ1	FRQ2	FRQ3	FRQ4		

The status of each element is expressed with logical level "1" or "0". Status "1" means the element is in operation.

4.2.4.4 Displaying the Status of the Time Synchronisation Source

The internal clock of the GRD140 can be synchronised with external clocks such as the binary input signal clock, RSM (relay setting and monitoring system) clock or IEC60870-5-103. To display on the LCD whether these clocks are active (=Act.) or inactive (=Inact.) and which clock the relay is synchronised with, do the following:

- Select "Status" on the top "MENU" screen to display the "Status" screen.
- Select "Time sync." to display the status of time synchronisation sources.

					m	е		s	у	n	С	▼
*	В		:				Α	С	t			
	R	S	М	:			I	n	а	С	t	
	I	Ε	С	:			1	n	а	С	t	

The asterisk on the far left shows that the internal clock is synchronised with the marked source clock. If the marked source clock is inactive, the internal clock runs locally.

Note: If the Binary input signal has not been detected for one hour or more after the last detection, the status becomes "inactive".

For details of the setting time synchronisation, see Section 4.2.6.6.

4.2.4.5 Clock Adjustment

To adjust the clock when the internal clock is running locally, do the following:

- Select "Status" on the top "MENU" screen to display the "Status" screen.
- Select "Clock adjust." to display the setting screen.

	/	2		1 2	2	<	N 0) v 3 :	,	<i>T</i> 1	2	0	0	1	•	,
ı	М	j	n	u	t	е					Ť					
	Н	0	u	r	5	6		-								
4	D	а	у		1	2										
	M	0	n	t	h											
	>	е	•	r	1	1										
1	,	U	а 2	0	0	1										

Line 1 and 2 show the current date and time. The time can be adjusted only when the clock is running locally. When [BI], [RSM] or [IEC] is active, the adjustment is invalid.

- Enter a numerical value for each item and press the ENTER key. For details to enter a numerical value, see 4.2.6.1.
- Press the END key to adjust the internal clock to the set hours without fractions and return to the previous screen.

If a date which does not exist in the calendar is set and END is pressed, "**** Error ****" is displayed on the top line and the adjustment is discarded. Return to the normal screen by pressing the CANCEL key and adjust again.

4.2.4.6 LCD Contrast

To adjust the contrast of LCD screen, do the following:

- Select "Status" on the top "MENU" screen to display the "Status" screen.
- Select "LCD contrast" to display the setting screen.



• Press the ◀ or ▶ key to adjust the contrast. The characters on the screen become thin by pressing the ◀ key and deep by pressing the ▶ key.

4.2.5 Viewing the Settings

The sub-menu "Set. (view)" is used to view the settings made using the sub-menu "Set. (change)". The following items are displayed:

Relay version

Description

Relay address and baud rate in the RSM (relay setting and monitoring system) or IEC60870-5-103 communication

Record setting

Status setting

Protection setting

Binary input setting

Binary output setting

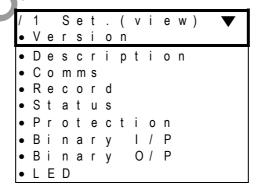
LED setting

Enter an item on the LCD to display each item as described in the previous sections.

4.2.5.1 Relay Version

To view the relay version, do the following.

• Press the "Set.(view)" on the main menu.



• Press the "Version" on the "Set.(view)" menu.



• Software

• Select "Relay type" to display the relay type form and model number.

GRD140-110A-11 -11

- Select "Serial number" to display the relay manufacturing number.
- Select "Software" to display the relay software type form and version.

GS1DP1-04-*

4.2.5.2 **Settings**

The "Description", "Comms", "Record", "Status", "Protection", "Binary I/P", "Binary O/P" and "LED" screens display the current settings input using the "Set. (change)" sub-menu.

4.2.6 Changing the Settings

The "Set. (change)" sub-menu is used to make or change settings for the following items:

Password

Description

Relay address and baud rate in the RSM or IEC60870-5-103 communication

Recording setting

Status setting

Protection setting

Binary input setting

Binary output setting

LED setting

All of the above settings except the password can be seen using the "Set. (view)" sub-menu.

CAUTION

Modification of settings: Care should be taken when modifying settings for "active group", "scheme switch" and "protection element" in the "Protection" menu. Dependencies exist between the settings in the various menus, with settings in one menu becoming active (or inactive) depending on the selection made in another menu. Therefore, it is recommended that all necessary settings changes be made while the circuit breaker tripping circuit is disconnected.

Alternatively, if it is necessary to make settings changes with the tripping circuit active, then it is recommended to enter the new settings into a different settings group, and then change the "active group" setting, thus ensuring that all new settings become valid simultaneously.

4.2.6.1 Setting Method

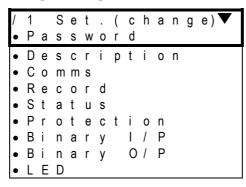
There are three setting methods as follows:

- To enter a selected item
- To enter a text string
- To enter numerical values

To enter a selected item

If a screen as shown below is displayed, perform setting as follows.

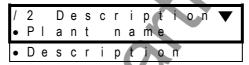
The cursor can be moved to upper or lower lines within the screen by pressing the \triangle and ∇ keys. If setting (change) is not required, skip the line with the \triangle and ∇ keys.



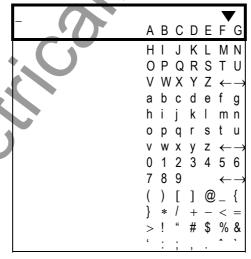
- Move the cursor to a setting item.
- Press the ENTER key.

To enter a text string

Texts strings are entered under "Plant name" or "Description" screen.



To select a character, use keys ∇ , \triangle , \triangleleft and \triangleright to move blinking cursor down, up, left and right. " \rightarrow " and " \leftarrow " on each of lines 4, 8 and 10 indicate a space and backspace, respectively. A maximum of 22 characters can be entered.



- Set the cursor position in the bracket by selecting "→" or "←" and pressing the (ENTER) key.
- Move the blinking cursor to a selecting character.
- Press the ENTER key to enter the blinking character at the cursor position in the brackets.
- Press the END key to confirm the entry and return to the upper screen.

To correct the entered character, do either of the following:

- Discard the character by selecting "←" and pressing the (ENTER) key and enter the new character.
- Discard the whole entry by pressing the CANCEL key and restart the entry from the first

To enter numerical values

When the screen shown below is displayed, perform setting as follows:

The number to the left of the cursor shows the current setting or default setting set at shipment. The cursor can be moved to upper or lower lines within the screen by pressing the \triangle and ∇ keys. If setting (change) is not required, skip the line with the \triangle and ∇ keys.

/	4		T	i	m	е	1	s	t	а	r	t	е	r	•
Τ	i	m										S			
0	С	2		0		-						Α			
				0	0										
Ε	F	0		6	٥							A			
S	Ε	F										Α	3		
N	_	0		2	0	0				4	E	Α			
		0		4	0							7			
0	V 1	2	٥		0				4			V		,	
U		2	U	•	U				7			٧			
7	0	6	0		0				(1	7	V			
		2	0		0							٧			
N	0	٧	4					,				٧			
		2	0	0	0		_								

- Move the cursor to a setting line.
- Press the

 or

 key to set a desired value. The value is up or down by pressing the

 or

 key.
- Press the ENTER key to enter the value.
- After completing the setting on the screen, press the END key to return to the upper screen.

To correct the entered numerical value, do the following.

- If it is before pressing the ENTER key, press the CANCEL key and enter the new numerical value.
- If it is after pressing the ENTER key, move the cursor to the correcting line by pressing the
 ▲ and ▼ keys and enter the new numerical value.

Note: If the CANCEL key is pressed after any entry is confirmed by pressing the ENTER key, all the entries made so far on the screen concerned are canceled and screen returns to the upper one.

To complete the setting

Enter after making entries on each setting screen by pressing the (ENTER) key, the new settings are not yet used for operation, though stored in the memory. To validate the new settings, take the

following steps.

 Press the END key to return to the upper screen. Repeat this until the confirmation screen shown below is displayed. The confirmation screen is displayed just before returning to the "Set. (change)" sub-menu.

• When the screen is displayed, press the ENTER key to start operation using the new settings, or press the CANCEL key to correct or cancel entries. In the latter case, the screen turns back to the setting screen to enable re-entries. Press the CANCEL key to cancel entries made so far and to turn to the "Set. (change)" sub-menu.

4.2.6.2 Password

For the sake of security of setting changes, password protection can be set as follows:

- Select "Set. (change)" on the main "MENU" screen to display the "Setting change" screen.
- Select "Password" to display the "Password" screen.
- Enter a 4-digit number within the brackets after "Input" and press the (ENTER) key.

• For confirmation, enter the same 4-digit number in the brackets after "Retype".

• Press the END key to display the confirmation screen. If the retyped number is different from that first entered, the following message is displayed on the bottom of the "Password" screen before returning to the upper screen.

"Unmatch passwd!"

Re-entry is then requested.

Password trap

After the password has been set, the password must be entered in order to enter the setting change screens.

If "Set. (change)" is entered on the top "MENU" screen, the password trap screen "Password" is displayed. If the password is not entered correctly, it is not possible to move to the "Setting (change)" sub-menu screens.

Canceling or changing the password

To cancel the password protection, enter "0000" in the two brackets on the "Password" screen. The "Set. (change)" screen is then displayed without having to enter a password.

The password can be changed by entering a new 4-digit number on the "Password" screen in the same way as the first password setting.

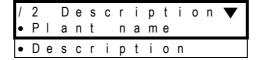
If you forget the password

Press CANCEL and RESET keys together for one second on the top "MENU" screen. The screen goes off, and the password protection of the GRD140 is canceled. Set the password again.

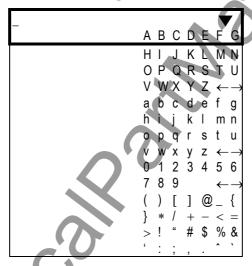
4.2.6.3 Plant Name

To enter the plant name and other data, do the following. These data are attached to records.

- Select "Set. (change)" on the main "MENU" screen to display the "Set. (change)" screen.
- Select "Description" to display the "Description" screen.



- To enter the plant name, select "Plant name" on the "Description" screen.
- To enter special items, select "Description" on the "Description" screen.

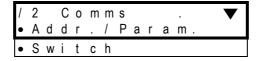


• Enter the text string

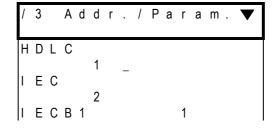
4.2.6.4 Communication

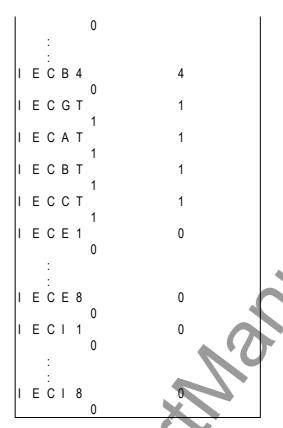
If the relay is linked with RSM (relay setting and monitoring system) or IEC60870-5-103 communication, the relay address must be set. Do this as follows:

- Select "Set (change)" on the main "MENU" screen to display the "Set. (change)" screen.
- Select "Comms" to display the "Comms" screen.



• Select "Addr./Param." on the "Comms" screen to enter the relay address number.





• Enter the relay address number on "HDLC" line for RSM or "IEC" line for IEC60870-5-103 and press the ENTER key.

CAUTION Do not overlap the relay address number.

Settings for IEC60870-5-103 communication

The lines "IECB1" to "IECB4" are used for auxiliary inputs of IEC103 events INF27 to INF30 in Appendix M. Assign signals to the columns "IECB1" to "IECB4" by entering the number corresponding to each signal referring to Appendix C.

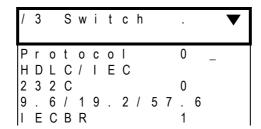
The lines "IECGT" to "IECCT" are used for fault indications of IEC103 events INF68 to INF71 in Appendix M. Assign signals to the columns "IECGT" to "IECCT" by entering the BO numbers (1 to 7) corresponding to the binary output settings.

The lines "IECE1" to "IECE8" are used to assign the signals for user customization. Assign signals to the columns "IECE1" to "IECE8" by entering the number corresponding to each signal referring to Appendix C.

Note: Assign "0" to the column when this function is not used.

The lines "IECI1" to "IECI8" are used to assign the above signals of "IECE1" to "IECE8" to each INF number. Enter the INF number to the columns "IECI1" to "IECI8".

• Select "Switch" on the "Comms" screen to select the protocol and transmission speed (baud rate), etc., of the RSM and IEC60870-5-103.



```
6 / 1 9 .
 ECBLK
    mal/Blocked
 ECNFI
                0
  2 / 2 .
 ECNFV
                0
  2 / 2 .
 ECNFP
  2 / 2
 ECNFf
 . 2 / 2 . 4
IECFL
                n
Prim/Second
IECGI1
No/Yes
IECGI8
                0
No/Yes
```

Select the number and press the ENTER key.

<Protocol>

This setting is for changing the protocol (HDLC or IEC) of the channel 1 (COM1 port). In the model with two channels (COM1 and COM2 ports), this setting for COM1 should be "HDLC".

• When the remote RSM system applied, select 0(=HDLC). When the IEC60870-5-103 applied, select 1(=IEC103).

CAUTION When changing the setting to the HDLC during the IEC103 operation, the IEC103 command INF18 in Appendix M is canceled.

The output of IEC103 command INF18 can be observed by assigning their signal numbers to LEDs or binary output relays (see Sections 4.2.6.9 and 4.2.6.10).

<232C>

This line is to select the RS-232C baud rate when the RSM system applied.

Note: The default setting of the 232C is 9.6kbps. The 57.6kbps setting, if possible, is recommended to serve user for comfortable operation. The setting of RSM100 is also set to the same baud rate.

<IECBR>

This line is to select the baud rate when the IEC60870-5-103 system applied.

<IECBLK>

Enter 1(=Blocked) to block the monitor direction in the IEC60870-5-103 communication.

<IECNFI, IECNFV, IECNFP, IECNFf>

These lines are to select the normalized factor (1.2 or 2.4) of the current measurand.

IECNFI: Current

IECNFV: Voltage

IECNFP: Active power, Reactive power

IECNFf: Frequency

<IECFL >

This line is to select the measurement result of the fault locator which is expressed as the primary side value or the secondary side value of power system impedance, or the distance (km).

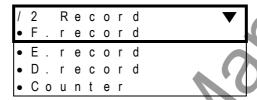
<IECGI1 - 8 >

These lines are to use the GI (General Interrogation) or not for user customized signals. If use the GI, enter 1(=Yes).

4.2.6.5 Setting the Recording

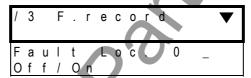
To set the recording function as described in Section 4.2.3, do the following:

- Select "Set. (change)" on the main "MENU" screen to display the "Set. (change)" screen.
- Select "Record" to display the "Record" screen.



Setting the fault recording

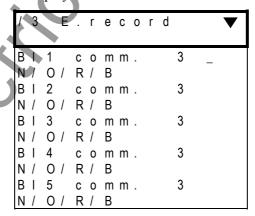
• Select "F. record" to display the "F. record" screen.



• Enter 1 to enable the fault locator. If to disable the fault locator, enter 0.

Setting the event recording

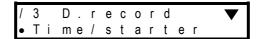
• Select "E. record" to display the "E. record" screen.



• Enter 0(=None) or 1(=Operate) or 2(=Reset) or 3(=Both) for BI command trigger setting and press the (ENTER) key.

Setting the disturbance recording

• Select "D. record" to display the "D. record" screen.



•	S	С	h	е	m	е	S	W		
•	В	i	n	а	r	у	S	i	g	

• Select "Time/starter" to display the "Time/starter" screen.

/	4		Τ	i	m	е	/	s	t	а	r	ter▼
Τ	j	m		_								S
0	С	2	•	0		-						Α
		2		0	0							
Ε	F	0		6	Λ							Α
S	Ε		•	U	U							Α
	^	0		2	0	0						
N	С	0		4	0							Α
0				•	·							V
U		2	0		0							V
U		6	0		0							\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
Z	0	٧			_							V
N	0	2 V	0		0					4	R	V
		2	0		0					N		

• Enter the recording time and starter element settings.

To set each starter to use or not to use, do the following:

• Select "Scheme sw" on the "D. record" screen to display the "Scheme sw" screen.

/	4		S	C	h e m e	S	W	•
Τ	r	į	p	7			1	_
0 B 0 0 0	f I f	f	1	0	n n		1	
ŏ	C		_	U	"		1	
0 E	f F	f	1	0	n		1	
0			1	0	n			
S O	E f	F f	1	0	n		1	
N	C						1	
0	f V	f	<i> </i>	0	n		1	
0	f	f	1	0	n		'	
U	٧						1	
U 0 Z 0	0	f V	1	0	П		1	
0	f	f	1	0	n			
N O	O f	V f	/	0	n		1	

• Enter 1 to use as a starter. If not to be used as a starter, enter 0.

To set each signal number to record binary signals, do the following:

• Select "Binary sig." on the "D. record" screen to display the "Binary sig." screen.

/	4		В	i	n	а	r	у	S	i	g	•
S	I	G	1									
			1	0	1		_					
S		G	2									
			1	0	2							
S	1	G	3	2								****
			1		3							

• Enter the signal number to record binary signals in Appendix C.

Setting the counter

• Select "Counter" to display the "Counter" screen.

ľ	/	3		С	0	u	n	t	е	r	▼
						m					
Ī	•	Α	I	а	r	m		s	е	t	

To set each counter to use or not to use, do the following:

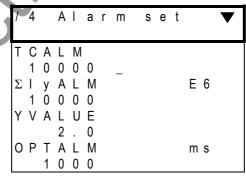
• Select "Scheme sw" on the "Counter" screen to display the "Scheme sw" screen.

/	4		S	С	h	е	m	е	5	W		7	
Τ	С	S	Р	Ε	Ν					0	_		
0	f	f	1	0	n	1	0	р	t -	0	n	•	
С	В	S	M	Ε	Ν					0			
0	f	f	1	0	n								
Т	С	Α	Ε	Ν				•		0			
0	f	f	1	0	n								
Σ		у	A	Ε	N	\checkmark				0			
0	f	f	1	0	n.								
0	Ρ	Τ	A	E	N		, ·			0			
0	f	f		0	n								

• Enter 1 to use as a counter. If not to be used as a counter, enter 0.

To set threshold setting, do the following:

• Select "Alarm set" on the "Counter" screen to display the "Alarm set" screen.



• Enter the threshold settings.

4.2.6.6 Status

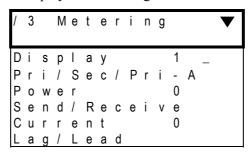
To set the status display described in Section 4.2.4, do the following:

Select "Status" on the "Set. (change)" sub-menu to display the "Status" screen.

/	2		S	t	а	t	u	S			V
•	2 M	е	t	е	r	i	n	g			
	Τ								С		

Setting the metering

• Select "Metering" to display the "Metering" screen.



• Enter 0 or 1 or 2 for Display.

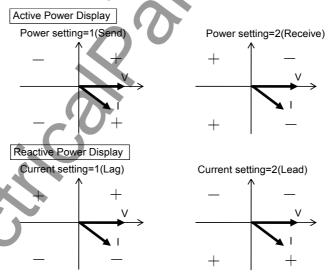
Enter 0(=Pri) to display the primary side current in kilo-amperes(kA).

Enter 1(=Sec) to display the secondary side current.

Enter 2(=Pri-A) to display the primary side current in amperes(A).

• Enter 0(=Send) or 1(=Receive) for Power, and 0(=Lag) or 1(=Lead) for Current, and press the ENTER key.

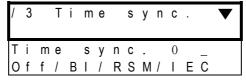
Note: Power and Current setting



Setting the time synchronisation

The calendar clock can run locally or be synchronised with the binary input signal, RSM clock, or by an IEC60870-5-103. This is selected by setting as follows.

• Select "Time sync." to display the "Time sync" screen.



• Enter 0, 1, 2 or 3 and press the ENTER key.

Enter 0(=off) not to be synchronised with any external signals.

Enter 1(=BI) to be synchronised with the binary input signal.

Enter 2(=RSM) to be synchronised with the RSM clock.

Enter 3(=IEC) to be synchronised with IEC60870-5-103.

Note: When selecting BI, RSM or IEC, check that they are active on the "Status" screen in "Status" sub-menu.

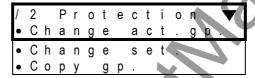
If BI is selected, the BI command trigger setting should be "None" because event records will become full soon. (See Section 4.2.6.5.)

If it is set to an inactive BI, RSM or IEC, the calendar clock runs locally.

4.2.6.7 Protection

The GRD140 can have 4 setting groups for protection in order to accommodate changes in the operation of the power system, one setting group is assigned active. To set the protection, do the following:

• Select "Protection" on the "Set. (change)" screen to display the "Protection" screen.



Changing the active group

• Select "Change act. gp." to display the "Change act. gp." screen.

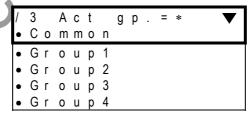
/	3		C g	h a p .	n g	e	а	С	t		•
Α	С	t	i	v e	g	р		1		_	

• Enter the group number and press the [ENTER] key.

Changing the settings

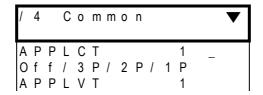
Almost all the setting items have default values that are set when the product is shipped. For the default values, see Appendix H. To change the settings, do the following:

• Select "Change set." to display the "Act gp.= *" screen.



Changing the Common settings

• Select "Common" to set the current and voltage input state and input imbalance monitoring for GRD140-400 and -420 and press the ENTER key.



```
Off/3PN/3PV
Optime 0
Normal/Fast
CTFEN 0
Off/On/OPT-On
VTF1EN 0
Off/On/OPT-On
VTF2EN 0
Off/On/OPT-On
CTSVEN 2
Off/ALM&BLK/ALM
V0SVEN 2
Off/ALM&BLK/ALM
V2SVEN 2
```

<APPLCT>

• Enter 0(=Off: not used), 1(=3P: 3 phase), 2(=2P: 2 phase) or 3(=1P: 1 pole) to set the current input state and press the (ENTER) key.

<APPLVT>

• Enter 0(=Off: not used), 1(=3PN: three phase-to-neutral voltage input) or 2(=3PV: three phase-to-neutral voltage and zero sequence voltage input) and press the ENTER key.

<Optime>

• Enter 0(=Normal : Transient free operation), 1(=Fast : High speed operation) to set the operating time and press the ENTER key.

Note: If "Fast" selected, all OC and EF elements operate at high-speed (approximately 20ms).

<CTFEN, VTF1EN, VTF2EN>

To set CT failure function and VT failure function enable, do the following.

• Enter 0(=Off) or 1(=On) or 2(=OPT-On) by pressing the ◀ or ▶ key and press the (ENTER) key.

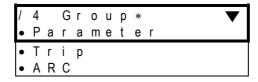
< CTSVEN, V0SVEN, V2SVEN>

To set AC input imbalance supervision enable, do the following.

• Enter 0 = 0 or 1 = ALM&BLK) or 2 = ALM by pressing the \triangleleft or \triangleright key and press the ENTER key.

Changing the Group settings

• Select the "Group*" on the "Act gp.= *" screen to change the settings and press the ENTER key.



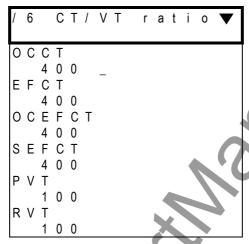
Setting the parameter

Enter the line name, the CT/VT ratio and the fault locator as follows:

• Select "Parameter" on the "Group *" screen to display the "Parameter" screen.

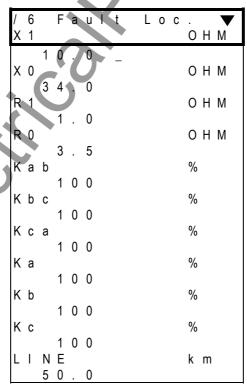
	/	5		Р	а	r	а	m a	е	t	е	r		▼
ı	•	L	i	n	е		n	а	m	е				
Ī	•	С	Τ	/	٧	Τ		r o	а	t	i	0		
	•	F	а	u		t	L	0	С	а	t	0	r	

- Select "Line name" to display the "Line name" screen.
- Enter the line name as a text string and press the END key.
- Select "CT/VT ratio" to display the "CT/VT ratio" screen.



Note: The "CT/VT ratio" screen depends on the APPLCT and APPLVT setting.

- Enter the CT/VT ratio and press the ENTER key.
- Select "Fault Locator" to display the "Fault Locator" screen.

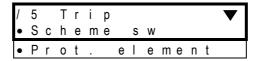


• Enter the setting value and press the ENTER key.

Setting the trip function

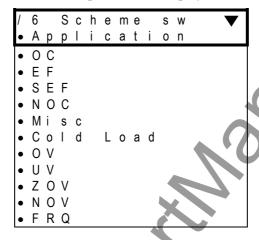
To set the scheme switches and protection elements, do the following.

• Select "Trip" on the "Group *" screen to display the "Trip" screen.



Setting the scheme switch

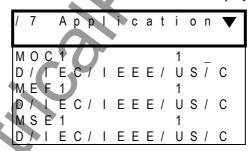
• Select "Scheme sw" on the "Trip" screen to display the "Scheme sw" screen.



Setting the application

To set the application setting, do the following.

• Select "Application" on the "Scheme sw" screen to display the "Application" screen.



<MOC1>, <MEF1>, <MSE1>

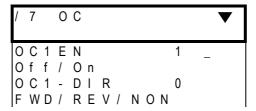
To set the OC1, EF1 and SEF1 time delay characteristic type, do the following.

• Enter 0(=D: DT) or 1(=IEC) or 2(=IEEE) or 3(=US) or 4(=C: CON) and press the (ENTER) key.

Setting the OC protection

The settings for the OC protection are as follows:

• Select "OC" on the "Scheme sw" screen to display the "OC" screen.



M N M	0 I 0	C / C /	1 V 1 V	C I C	- / -	I E I	E I E	C / E	L E	T	0 I 0	
M M C	0 0	/ C 2	v 1 /	I C C	/ - 0	E U 8	I S				0	
0	С	1	R								0	
D V	E	F	<i>-</i>	D 0	С	P 1	В	L	K		0	
0 0	f C	f 2 f	/ E /	0 N	n						0	
0 0 F	f C W	2 D	<i>-</i> /	O D R	n -	R V	1	N	0	N	0	
V 0	T f	F f	<i>-</i> /	0 0	E C n	2		L	K	IN	0	
0	C	3 f	/ E /	N O							0	
0	C	3	<i>-</i> /	D R	n I E	R V	1	N	0	N	0	
F V O	T f	F f	- /	0		3		L	K	IN	0	
0 0	C f	4 f	/ E /	N O							0	4
0	C	4 D	<i>-</i> /	D R	n I E	R V	,	N	0	N	0	X
F V O	T f	F	<i>-</i> /		С	4	/ B	L	K	IN	0	
0	C P	f T O	P R	1	n 2	0	U	T	0	F	0 3)

This setting is displayed if [MOC1] is 1(=IEC).

This setting is displayed if [MOC1] is 2(=IEEE)

This setting is displayed if [MOC1] is 3(=US)

<OC*EN>

• Enter 1(=On) to enable the OC* and press the [ENTER] key. If disabling the OC*, enter 0(=Off) and press the [ENTER] key.

<OC*-DIR>

To set the OC* directional characteristic, do the following.

• Enter 0(=FWD) or 1(=REV) or 2(=NON) and press the ENTER key.

<MOC1C>

To set the OC1 Inverse Curve Type, do the following.

- If [MOC1] is 1(=IEC), enter 0(=NI) or 1(=VI) or 2(=EI) or 3(=LTI) and press the [ENTER]
- If [MOC1] is 2(=IEEE), enter 0(=MI) or 1(=VI) or 2(=EI) and press the [ENTER] key.
- If [MOC1] is 3(=US), enter 0(=CO2) or 1(=CO8) and press the [ENTER] key.

<0C1R>

To set the Reset Characteristic, do the following.

• If [MOC1] is 2(=IEEE) or 3(=US), enter 0(=DEF) or 1(=DEP) and press the [ENTER] key.

<VTF-OC*BLK>

To set the VTF block enable of OC*, do the following.

• Enter 1(=On) to enable "Trip block" by the VTF function and press the ENTER key. If disabling it, enter 0(=Off) and press the ENTER key.

<OCTP>

To set the trip mode, do the following.

- Enter 0(=3POR) or 1(=2OUTOF3) and press the ENTER key. If the "2OUTOF3" selected, the trip signal is not issued when only one phase element operates.
- After setting, press the (END) key to display the following confirmation screen.

• Press the ENTER (=Y) key to change settings and return to the "Scheme sw" screen.

Setting the EF protection

The settings for the EF protection are as follows:

Off/

• Select the "EF" on the "Scheme sw" screen to display the "EF" screen.



This setting is displayed if [MEF1] is 1(=IEC).

This setting is displayed if [MEF1] is 2(=IEEE).

This setting is displayed if [MEF1] is 3(=US).

```
V T F - E F 3 B L K 0
O f f / O n
E F 4 E N 0
O f f / O n
E F 4 - D I R 0
F W D / R E V / N O N
C T F - E F 4 B L K 0
O f f / O n
V T F - E F 4 B L K 0
O f f / O n
C U R R E V 0
O f f / 1 / 2 / 3 / 4
```

<EF*EN>

• Enter 1(=On) to use an earth fault protection or enter 2(=POP) to use the directional earth fault command protection (POP scheme), and press the ENTER key. If disabling the EF*, enter 0(=Off) and press the ENTER key.

<EF*-DIR>

To set the EF* directional characteristic, do the following.

• Enter 0(=FWD) or 1(=REV) or 2(=NON) and press the ENTER key.

<MEF1C>

To set the EF1 Inverse Curve Type, do the following.

- If [MEF1] is 1(=IEC), enter 0(=NI) or 1(=VI) or 2(=EI) or 3(=LTI) and press the ENTER key.
- If [MEF1] is 2(=IEEE), enter 0(=MI) or 1(=VI) or 2(=EI) and press the ENTER key.
- If [MEF1] is 3(=US), enter 0(=CO2) or 1(=CO8) and press the ENTER key.

<EF1R>

To set the Reset Characteristic, do the following.

• If [MEF1] is 2(=IEEE) or 3(=US), enter 0(=DEF) or 1(=DEP) and press the ENTER key.

<CTF-EF*BLK>. <VTF-EF*BLK>

To set the CTF block and VTF block enable of EF*, do the following.

• Enter 1(=On) to enable "Trip block" by the CTF function and VTF function, and press the ENTER key. If disabling them, enter 0(=Off) and press the ENTER key.

<CURREV>

To set which stage is used for current reverse detection in the command protection, do the following.

- Enter 1(=EF1), 2(=EF2), 3(EF3) or 4(=EF4) and press the (ENTER) key. If disabling them, enter 0(=Off) and press the (ENTER) key.
- After setting, press the (END) key to display the following confirmation screen.

Change settings? ENTER=Y CANCEL=N

Press the (ENTER) (=Y) key to change settings and return to the "Scheme sw" screen.

Setting the SEF protection

The settings for the SEF protection are as follows:

• Select "SEF" on the "Scheme sw" screen to display the "SEF" screen.



This setting is displayed if [MSE1] is 1(=IEC).

This setting is displayed if [MSE1] is 2(=IEEE).

This setting is displayed if [MSE1] is 3(=US).

<SE*EN>

• Enter 1(=On) to enable the SEF* and press the ENTER key. If disabling the SEF*, enter 0(=Off) and press the ENTER key.

<MSE1C>

To set the SEF1 Inverse Curve Type, do the following.

- If [MSE1] is 1(=IEC), enter 0(=NI) or 1(=VI) or 2(=EI) or 3(=LTI) and press the ENTER key.
- If [MSE1] is 2(=IEEE), enter 0(=MI) or 1(=VI) or 2(=EI) and press the (ENTER) key.
- If [MSE1] is 3(=US), enter 0(=CO2) or 1(=CO8) and press the ENTER key.

<SE1R>

To set the Reset Characteristic, do the following.

• If [MSE1] is 2(=IEEE) or 3(=US), enter 0(=DEF) or 1(=DEP) and press the [ENTER] key.

<SE1S2>

To set the Stage 2 Timer Enable, do the following.

• Enter 1(=On) to enable the SE1S2 and press the ENTER key. If disabling the SE1S2, enter 0(=Off) and press the ENTER key.

<VTF-SE*BLK>

To set the VTF block enable of SE*, do the following.

• Enter 1(=On) to enable "Trip block" by the VTF function and press the (ENTER) key. If disabling it, enter 0(=Off) and press the (ENTER) key.

<RPEN>

To set the residual power block enable of SE*, do the following.

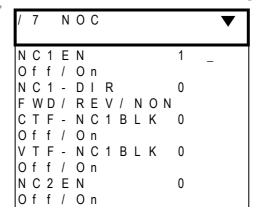
- Enter 1(=On) to enable "Trip block" by the residual power block function and press the ENTER key. If disabling it, enter 0(=Off) and press the ENTER key.
- After setting, press the END key to display the following confirmation screen.

• Press the (ENTER) (=Y) key to change settings and return to the "Scheme sw" screen.

Setting the NOC protection

The settings for the NOC protection are as follows:

• Select the "NOC" on the "Scheme sw" screen to display the "NOC" screen.



```
N C 2 - D I R 0
F W D / R E V / N O N
C T F - N C 2 B L K 0
O f f / O n
V T F - N C 2 B L K 0
O f f / O n
```

<NC*EN>

• Enter 1(=On) to enable the NC* and press the ENTER key. If disabling the NC*, enter 0(=Off) and press the ENTER key.

<NC*-DIR>

To set the NC* directional characteristic, do the following.

• Enter 0(=FWD) or 1(=REV) or 2(=NON) and press the ENTER key.

<CTF-NC*BLK>, <VTF-NC*BLK>

To set the CTF block and VTF block enable of NC*, do the following.

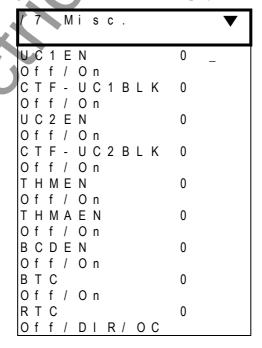
- Enter 1(=On) to enable "Trip block" by the CTF function and VTF function, and press the ENTER key. If disabling them, enter 0(=Off) and press the ENTER key.
- After setting, press the (END) key to display the following confirmation screen.

• Press the (ENTER) (=Y) key to change settings and return to the "Scheme sw" screen.

Setting the Misc. protection

The settings for the miscellaneous protection are as follows:

• Select "Misc." on the "Scheme sw" screen to display the "Misc." screen.



<UC*EN>

• Enter 1(=On) to enable the UC* and press the ENTER key. If disabling the UC*, enter 0(=Off) and press the ENTER key.

<CTF-UC*BLK>

To set the CTF block enable of UC*, do the following.

• Enter 1(=On) to enable "Trip block" by the CTF function, and press the ENTER key. If disabling it, enter 0(=Off) and press the ENTER key.

<THMEN>

• Enter 1(=On) to enable the Thermal OL and press the ENTER key. If disabling the Thermal OL, enter 0(=Off) and press the ENTER key.

<THMAEN>

• Enter 1(=On) to enable the Thermal Alarm and press the ENTER key. If disabling the Thermal Alarm, enter 0(=Off) and press the ENTER key.

<BCDEN>

• Enter 1(=On) to enable the Broken Conductor and press the ENTER key. If disabling the Broken Conductor, enter 0(=Off) and press the ENTER key.

<BTC>

• Enter 1(=On) to set the Back-trip control and press the ENTER key. If not setting the Back-trip control, enter 0(=Off) and press the ENTER key.

<RTC>

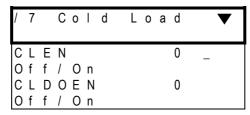
To set the Re-trip control, do the following.

• Enter 0(=Off) or 1(=Direct) or 2(=OC controlled) and press the ENTER key.

Setting the Cold Load protection

The settings for the Cold Load protection are as follows:

• Select "Misc." on the "Scheme sw" screen to display the "Misc." screen.



<CLEN>

To set the Cold load function enable, do the following.

• Enter 1(=On) to enable the Cold Load function and press the (ENTER) key. If disabling the Cold Load, enter 0(=Off) and press the (ENTER) key.

<CLDOEN>

• Enter 1(=On) to enable the Cold Load drop-off and press the ENTER key. If disabling the Cold Load drop-off, enter 0(=Off) and press the ENTER key.

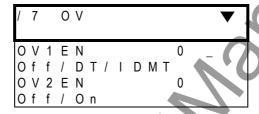
• After setting, press the END key to display the following confirmation screen.

• Press the (ENTER) (=Y) key to change settings and return to the "Scheme sw" screen.

Setting the OV protection

The settings for the OV protection are as follows:

• Select "OV" on the "Scheme sw" screen to display the "OV" screen.



<OV1EN>

To set the OV1 delay type, do the following.

• Enter 1 (=DT) or 2 (=IDMT) and press the ENTER key. If disabling the OV1, enter 0 (=Off) and press the ENTER key.

<OV2EN>

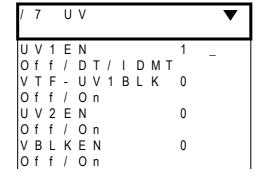
- Enter 1 (=On) to enable the OV2 and press the ENTER key. If disabling the OV2, enter 0 (=Off) and press the ENTER key.
- After setting, press the END key to display the following confirmation screen.

• Press the ENTER (= Y) key to change settings and return to the "Scheme sw" screen.

Setting the UV protection

The settings for the UV protection are as follows:

• Select "UV" on the "Scheme sw" screen to display the "UV" screen.



<UV1EN>

To set the UV1 delay type, do the following.

• Enter 1 (=DT) or 2 (=IDMT) and press the (ENTER) key. If disabling the UV1, enter 0 (=Off) and press the (ENTER) key.

<UV2EN>

• Enter 1 (=On) to enable the UV2 and press the ENTER key. If disabling the UV2, enter 0 (=Off) and press the ENTER key.

<VBLKEN>

• Enter 1 (=On) to enable the UV blocking and press the ENTER key. If disabling the UV blocking, enter 0 (=Off) and press the ENTER key.

<VTF-UV*BLK>

To set the VTF block enable of UV*, do the following.

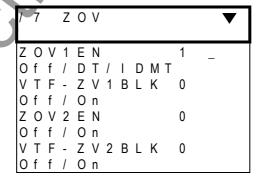
- Enter 1(=On) to enable "Trip block" by the VTF function and press the ENTER key. If disabling it, enter 0(=Off) and press the ENTER key.
- After setting, press the END key to display the following confirmation screen.

• Press the ENTER (= Y) key to change settings and return to the "Scheme sw" screen.

Setting the ZOV protection

The settings for the ZOV protection are as follows:

• Select "ZOV" on the "Scheme sw" screen to display the "ZOV" screen.



<ZOV1EN>

To set the ZOV1 delay type, do the following.

• Enter 1(=DT) or 2(=IDMT) and press the ENTER key. If disabling the ZOV1, enter 0(=Off) and press the ENTER key.

<ZOV2EN>

• Enter 1(=On) to enable the ZOV2 and press the ENTER key. If disabling the ZOV2, enter 0(=Off) and press the ENTER key.

<VTF-ZV*BLK>

To set the VTF block enable of ZOV*, do the following.

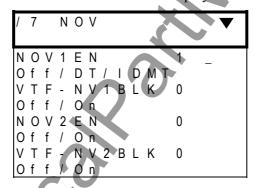
- Enter 1(=On) to enable "Trip block" by the VTF function and press the ENTER key. If disabling it, enter 0(=Off) and press the ENTER key.
- After setting, press the END key to display the following confirmation screen.

• Press the ENTER (= Y) key to change settings and return to the "Scheme sw" screen.

Setting the NOV protection

The settings for the NOV protection are as follows:

• Select "NOV" on the "Scheme sw" screen to display the "NOV" screen.



<NOV1EN>

To set the NOV1 delay type, do the following.

• Enter 1(=DT) or 2(=IDMT) and press the ENTER key. If disabling the NOV1, enter 0(=Off) and press the ENTER key.

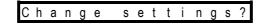
< NOV2EN :

• Enter 1(=On) to enable the NOV2 and press the ENTER key. If disabling the NOV2, enter 0(=Off) and press the ENTER key.

<VTF-NV*BLK>

To set the VTF block enable of NOV*, do the following.

- Enter 1(=On) to enable "Trip block" by the VTF function and press the ENTER key. If disabling it, enter 0(=Off) and press the ENTER key.
- After setting, press the (END) key to display the following confirmation screen.



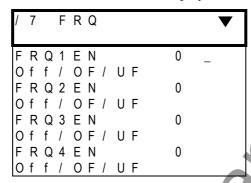
ENTER=Y CANCEL=N

• Press the ENTER (= Y) key to change settings and return to the "Scheme sw" screen.

Setting the FRQ protection

The settings for the FRQ (over/under frequency) protection are as follows:

• Select "FRQ" on the "Scheme sw" screen to display the "FRQ" screen.



<FRQ*EN>

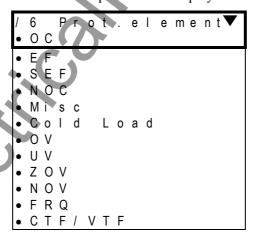
To set the FRQ* scheme enable, do the following.

• Enter 1(=OF, overfrequency) or 2(=UF, underfrequency) and press the ENTER key. If disabling the FRQ*, enter 0(=Off) and press the ENTER key.

Setting the protection elements

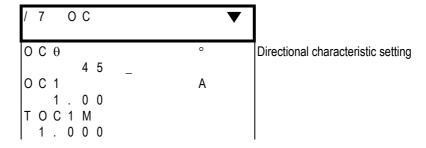
To set the protection elements, do the following.

• Select "Prot. element" on the "Trip" screen to display the "Prot. element" screen.



Setting the OC elements

• Select "OC" on the "Prot. element" screen to display the "OC" screen.



T O C 1	S	
1.00	•	
TOC1R		
	S	
0.0		
TOC1RM		
1.000		
O C 2	Α	
5.00		
T O C 2	•	
	S	♦
0.00		
O C 3	Α	. (0
10.00		
T O C 3	S	
0.00		
O C 4	Α	. • / / /
20.00	, ,	
T O C 4	_	
	S	
0.00		
O C 1 - k		OC1 User configurable IDMT curve setting
0.000		
O C 1 - α		ditto
0.00		. 0
0 C 1 - C		ditto
		ditto
0.000		172
0 C 1 - k r		ditto
0.000		
O C 1 - β		ditto
0.00		

- Enter the numerical value and press the ENTER key.
- After setting, press the END key to display the following confirmation screen.



• Press the ENTER (=Y) key to change settings and return to the "Prot. element" screen.

Setting the EF elements

• Select "EF" on the "Prot. element" screen to display the "EF" screen.

			-1	1					
	1	7		E	F			▼	
	E	F	θ			_		0	Directional characteristic setting
				_	4	5	_		
,	Ε	F	٧					V	V0 threshold setting for directional characteristic
				3		0			
	Ε	F	1					Α	
			0		3	0	_		
	Τ	Ε	F	1	M				
		1		0	0	0			
	Τ	Ε	F	1				S	
			1		0	0			
	Τ	Ε	F	1	R			S	
				0		0			
	Τ	Ε	F	1	R	M			
		1		0	0	0			
	lΕ	F	2					Α	

•				
3 .	0	0		
T E F 2	-	-	C	
	_	_	S	
1 .	0	0		
E F 3			Α	
	Λ	Λ	,,	
	0	U		
T E F 3			S	
0 .	0	0		
	٠	Ū	Λ	
E F 4			Α	
1 0 .	0	0		
T E F 4			S	
	^	^	3	
	0	0		
TREB	K		S	Delay time of current reverse detection
0.	1	0		
_	-	U		FEATH
E F 1 -	K			EF1 User configurable IDMT curve setting
0.0	0	0		AY ()
E F 1 -	α			ditto
		^		uitto
0 .	0	0		
E F 1 -	С			ditto
	0	0		
E F 1 -	K	r		ditto
0.0	0	0		
1		-		ditto
	β	_		dillo
0 .	0	0		

- Enter the numerical value and press the ENTER key.
- After setting, press the END key to display the following confirmation screen.



• Press the ENTER (=Y) key to change settings and return to the "Prot. element" screen.

Setting the SEF elements

• Select "SEF" on the "Prot. element" screen to display the "SEF" screen.

_			-
,	/ 7 SEF	•	
	S E 0 + 9 0	0	Directional characteristic setting
	S E V	V	V0 threshold setting for directional characteristic
4	S E 1 0 . 0 1 0	Α	
	TSE1M		
	1 . 0 0 0 T S E 1	s	
	1 . 0 0 T S E 1 R	S	
	0 . 0 T S E 1 R M		
	1 . 0 0 0 T S 1 S 2	S	
	0 . 0 0 S E 2	А	
	0 . 0 1 0 T S E 2	S	
	1.00	Ü	

S E 3 0 . 0 1 0	Α	
T S E 3	s	
S E 4 0 . 0 10	Α	
T S E 4	s	
S E 1 - k 0 . 0 0 0		SE1 User configurable IDMT curve setting
S E 1 - α 0 . 0 0		ditto
S E 1 - C		ditto
0 . 0 0 0 S E 1 - k r		ditto
0.000 SE1-β		ditto
0.00		

- Enter the numerical value and press the ENTER key.
- After setting, press the END key to display the following confirmation screen.



• Press the (ENTER) (=Y) key to change settings and return to the "Prot. element" screen.

Setting the NOC elements

• Select "EF" on the "Prot. element" screen to display the "EF" screen.

	/ 7	N	0	С		▼	
	N C	θ_	4	5	0	0	Directional characteristic setting
	N C	V 3				V	V0 threshold setting for directional characteristic
	N C	1	2	0		Α	
	T N	C 1	0			S	
	ŢΝ	C 1 0	R	0		S	
4	ΤN	-					
•	. 1		0	0			
	N C		4	0		Α	
	ΤN	0 . C 2	4	U		S	
		0 .	0	0			

- Enter the numerical value and press the ENTER key.
- After setting, press the END key to display the following confirmation screen.

Change settings? ENTER=Y CANCEL=N

• Press the ENTER (=Y) key to change settings and return to the "Prot. element" screen.

Setting the Misc. protection elements

• Select "Misc." on the "Prot. element" screen to display the "Misc." screen.

/	7		M	i	S	С		▼
U	С							Α
				4	0		_	
	U		1	^	^			S
	С	2		U	U			Α
	Ü	0		2	0			Λ
Т	U	С	2					S
		-		0	0			
Τ	Η			٥	٥			Α
Т	Н	1 M		0 P	U			Α
	•			0	0			71
Т	Т	Н	М					min 🐗
		1						~
I	Н	M		8				%
В	С	D			U			
	Ū	0		2	0			
Τ	В		D					S
	В			0	0			
	В			5	٥			Α
Т	В		Ċ	J	J		(s
		0		5	0			·U
Т	R	Ţ			Š			S
		1	. 4	0	0	4		

- Enter the numerical value and press the ENTER key.
- After setting, press the END key to display the following confirmation screen.

• Press the ENTER (=Y) key to change settings and return to the "Prot. element" screen.

Setting the Cold Load protection elements

• Select "Cold Load" on the "Prot. element" screen to display the "Cold Load" screen.

/	7		М	İ	S	С		•
0	С							Α
	^	2	•	0	0		_	٨
0		_		0	Λ			Α
0			•	U	U			Α
	2	0		0	0			
0					_			Α
Е	4	0		0	0			٨
	Γ	2		0	0			А
Ε	F		•	J	J			Α
	1	0		0	0			

Ε	F	3				Α
	2	0		0	0	
Ε	F	4		_		Α
	4	0		0	0	
S	Е 0	1	0	2	Λ	A
S	E	2	U	_	U	Α
	0		0	2	0	
S	0 E	3				Α
	0	4	0	2	0	
S	E		_	_	•	Α
N	0 C	1	0	2	0	A
IN	C	0		8	Λ	A
N	С		•	Ü	U	Α
	_	0		4	0	
В	С	D				
		0		4	0	
Т	С	L	Ε	^		S
Т	С	1 L	0 R	0		90
	U	1	0	0		S
I	С	Ĺ	D	Ö		A
		0		5	0	
Т	С	L	D	0		S
		0		0	0	

- Enter the numerical value and press the ENTER key.
- After setting, press the END key to display the following confirmation screen.

• Press the (ENTER) (=Y) key to change settings and return to the "Prot. element" screen.

Setting the OV elements

• Select "OV" on the "Prot. element" screen to display the "OV" screen.

			<u> </u>					
	1	7		0	٧		_	,
	0	V	1				V	OV1 Threshold setting.
	K	1	2	0		0 _		
5	Ţ	0	٧	1	M			
			1		0	0		
•	Τ	0	٧	1			s	
			0		0	0		
	Τ	0	٧	1	R		S	OV1 Definite time reset delay.
				0		0		
	0	٧	1	D	Ρ	R	%	OV1 DO/PU ratio
					9	5		
	0	٧	2				V	OV2 Threshold setting.
		1	4	0		0		
	Т	0	٧	2			S	OV2 Definite time setting.
			0		0	0		
	0	٧	2	D	Ρ	R	%	OV2 DO/PU ratio
					9	5		

- Enter the numerical value and press the ENTER key.
- After setting, press the END key to display the following confirmation screen.

Change settings? ENTER=Y CANCEL=N

• Press the ENTER (= Y) key to change settings and return to the "Prot. element" screen.

Setting the UV elements

• Select "UV" on the "Prot. element" screen to display the "UV" screen.

/	7	U	٧		•	
U	٧	1			V	UV1 Threshold setting.
		6 0		0	_	
Τ	U '	V 1	M			
		1 .	0	0		
Τ	U '	V 1			S	
		0.	0	0		
Τ	U '	V 1	R		S	UV1 Definite time reset delay.
		0		0		
U	V :	2			V	UV2 Threshold setting.
		4 0		0		
Т	U '	V 2			S	UV2 Definite time setting.
		0.	0	0		
٧	В	L K			V	UV Blocking threshold
		1 0		0		

- Enter the numerical value and press the ENTER key.
- After setting, press the END key to display the following confirmation screen.

• Press the ENTER (= Y) key to change settings and return to the "Prot. element" screen.

Setting the ZOV elements

• Select "ZOV" on the "Prot. element" screen to display the "ZOV" screen.

						-	
1	7		Z	0	٧	▼	
Z	0	٧	1			V	ZOV1 Threshold setting.
		2	0		0	_	ŭ
Т	Ζ	0	٧	1	M		
		1		0	0		
Т	Ζ	0	٧	1		S	
		0		0	0		
Т	Ζ	0	٧	1	R	S	ZOV1 Definite time reset delay.
			0		0		•
Z	0	٧	2			V	ZOV2 Threshold setting.
		4	0		0		_
T	Ζ	0	٧	2		S	ZOV2 Definite time setting.
		0		0	0		•

• Enter the numerical value and press the ENTER key.

• After setting, press the END key to display the following confirmation screen.

• Press the ENTER (= Y) key to change settings and return to the "Prot. element" screen.

Setting the NOV protection elements

• Select "NOV" on the "Prot. element" screen to display the "NOV" screen.

/	7	N O	V	•	
N	O V 2	1 0 .	0	V	NOV1 Threshold setting.
Т		V 1	М	_	
Т	N O 0	V 1	0	s	
Т	N O	V 1 0 .	R 0	S	NOV1 Definite time reset delay.
N	O V 4	-	0	V	NOV2 Threshold setting.
Т	N O 0	V 2 . 0	0	S	NOV2 Definite time setting.

- Enter the numerical value and press the ENTER key.
- After setting, press the END key to display the following confirmation screen.

• Press the ENTER (= Y) key to change settings and return to the "Prot. element" screen.

Setting the FRQ elements

• Select "FRQ" on the "Prot. element" screen to display the "FRQ" screen.

/	7		F	R	Q				•
F	Ŕ	Q		^	^			Н	Z
T	F	R	O	0	U	-			
Ö)			0	0				
F	R							Н	Z
_	_	1			0				
I	F	1			0				
F	R			Ü	Ü			Н	Z
	_				0				
T	F				^				
F	R		1	U	0			Н	7
	_	1		0	0				_
T	F		Q	4		_			
_	. ,	1			0			. ,	
۲	٧	В 4	L 0		0			٧	
		+	U	•	U				

UV Blocking threshold

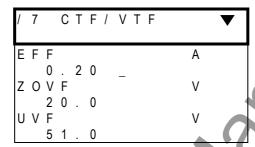
- Enter the numerical value and press the ENTER key.
- After setting, press the END key to display the following confirmation screen.

Change settings? ENTER=Y CANCEL=N

• Press the ENTER (= Y) key to change settings and return to the "Prot. element" screen.

Setting the CTF/VTF elements

• Select "CTF/VTF" on the "Prot. element" screen to display the "CTF/VTF" screen.



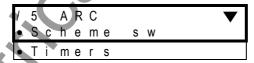
- Enter the numerical value and press the ENTER key.
- After setting, press the END key to display the following confirmation screen.

• Press the ENTER (=Y) key to change settings and return to the "Prot. element" screen.

Setting the autoreclose function

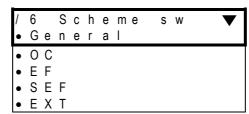
To set the autoreclose function, do the following.

• Select "ARC" on the "Group *" screen to display the "ARC" screen.



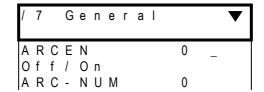
Setting the scheme switch

• Select "Scheme sw" on the "ARC" screen to display the "Scheme sw" screen.



<General>

• Select "General" on the "Scheme sw" screen to set the autoreclose mode.

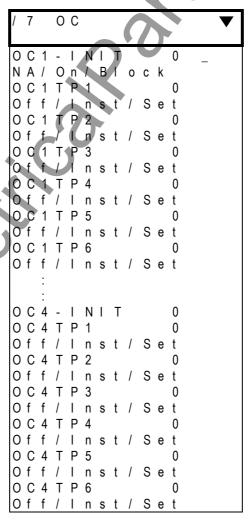


S	1	/	S	2	1	S	3	/	S	4	/	S	5	
S C	0	0	R	D	-	0	С				0			
0														
С	0	0	R	D	-	Ε	F				0			
0														
С	0	0	R	D	-	S	Ε				0			
0	f	f	1	0	n									

- Enter 1(=On) or 0(=Off) to enable or to disable the autoreclose.
- Enter 0 or 1 or 2 or 3 or 4 to set the number of shot.
 - Enter 0 = S1 to perform single-shot autoreclosing.
 - Enter 1 (= S2) to perform two-shot autoreclosing..
 - Enter 2 (= S3) to perform three-shot autoreclosing.
 - Enter 3 (= S4) to perform four-shot autoreclosing.
 - Enter 4 (= S5) to perform five-shot autoreclosing.
- Enter 1(=On) or 0(=Off) to enable or to disable the co-ordination for "COOD-OC", "COOD-EF" and "COOD-SE" and press the ENTER key.

<0C>, <EF>, <SEF>

• Select "OC" on the "Scheme sw" screen to set the autoreclose initiation and trip mode of OC protection.



- Enter 1(=INIT) or 2(=Block) to initiate or to block the autoreclose by the OC1 trip in "OC1-INIT". To neither initiate nor block it, enter 0(=NA).
- Enter 1(=Inst) or 2(=Set) to set the OC1 first trip to "Instantaneous trip" or "Set time delay trip' in the "OC1-TP1". To not use the OC1 trip, enter 0(=Off).

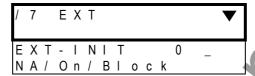
Note: OC1-TP2 to OC1-TP6 show the OC1 second trip to OC1 sixth trip.

For OC2 to OC4, the settings are same as OC1. After changing settings, press the (ENTER) key.

The setting method for EF and SEF is same as that of OC above.

<EXT>

• Select "EXT" on the "Scheme sw" screen to set the external initiation of the autoreclose.



• Enter 1(=INIT) or 2(=Block) to initiate or to block the autoreclose by the external trip. To neither initiate nor block it, enter 0(=NA).

Setting the timers

• Select "Timers" on the "Group *" screen to set timer setting and the threshold setting of OC, EF and SEF for co-ordination.

	/	6		Τ	i	mers	•
	T	R	D 6	Υ	4	S	
	Т	D	1	0		s	
	Т	1 D	0 2	1	0	0 s	
		1	0	ľ	0	0	
4	Τ.	D 1	3	_	0	s 0	
	1	D	4	•		S	
	T	1 D	0 5		0	0 s	
	T	1 W	0		0	0 s	
			2		0	0	
	Τ	S	U 3	C	0	s 0	
	Т	R 1	С	0	V 0	s 0	
	Т	Α	0 R	C	Р	S	
	Т	1 R	0 S	Е	0 T	0 s	
			3		0	0	
	0	С	1		0	A 0	
	Ε	F	0		3	Α	
	S	Ε	U		J	0	

0.010

- Enter the numerical value and press the ENTER key.
- After setting, press the (END) key to display the following confirmation screen.

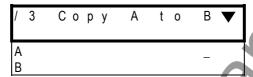
Change settings? ENTER=Y CANCEL=N

• Press the ENTER (=Y) key to change settings and return to the "ARC" screen.

Setting group copy

To copy the settings of one group and overwrite them to another group, do the following:

• Select "Copy gp." on the "Protection" screen to display the "Copy A to B" screen.



- Enter the group number to be copied in line A and press the ENTER key.
- Enter the group number to be overwritten by the copy in line B and press the (ENTER) key.

4.2.6.8 Binary Input

The logic level of binary input signals can be inverted by setting before entering the scheme logic. Inversion is used when the input contact cannot meet the requirements described in Table 3.2.2.

• Select "Binary I/P" on the "Set. (change)" sub-menu to display the "Binary I/P" screen.

						$\overline{}$	_								
	<i>!</i>	2 B		B ¹	-	n	а	5	y		l	1	Р	•	
		В	I	2	7		•								
		В	4	3	L	J									
		В		4	•										
4		В	1	5											
	7	В	1	6											
		В	T	7											
		В	1	8											
Ó		Α	1	а	r	m	1		Τ	е	Χ	t			
	١.	Α	1	а	r	m	2		Τ	е	Χ	t			
		Α	1	а	r	m	3		Τ	е	Χ	t			
		Α	I	а	r	m	4		T	е	Χ	t			

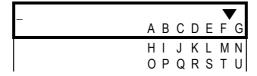
Selection of Binary Input

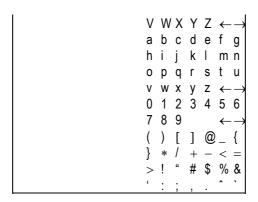
• Select the input number (BI number) on the "Binary I/P" screen.

Setting Alarm * Text

If the BI selected is used for an alarm, alarm message can be set.

• Select the Alarm* text and press the ENTER key to display the text input screen.





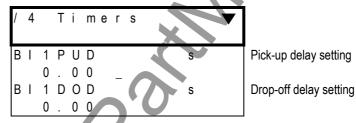
• Enter the characters (up to 22 characters) according to the text setting method.

After setting, press the ENTER key to display the "BI*" screen.



Setting timers

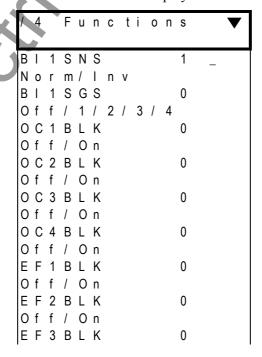
• Select "Timers" on the "BI" screen to display the "Timers" screen.



- Enter the numerical value and press the ENTER key.
- After setting, press the END key to return to the "BI*" screen.

Setting Functions

• Select "Functions" on the "BI" screen to display the "Functions" screen.



Off/On	
FRQ3BL	K 0
Off/On	
FRQ4BL	K 0
Off/On	0
ARCBLK Off/On	0
ARCRDY	0
Off / On	Ů
ARCINI	0
Off/On	
MNLCLS	0
Off/On ARCNA	0
ARCNA Off/On	U
CTFBLK	0
Off/On	
VTFBLK	0
Off/On	
CTFEXT	0
Off/On VTFEXT	
V T F E X T O f f / O n	
EXTAPH	0
Off / On	
ЕХТВРН	0
Off/On	~' <i>U</i>
EXTCPH	0
Off/On	0
EXT3PH Off/On	0
TCFALM	0
0 f f / 0 n	·
CBOPN	0
0 f f / 0 n	
CBCLS	0
Off/On RMTRST	0
RMTRST Off/On	0
SYNCLK	0
Off/On	
STORCD	0
Off/On	
Alarm1	0
Off/On	_
Alarm2 Off/On	0
Alarm3	0
Off / On	Ţ
Alarm4	0
Off/On	

<BI1SNS>

To set the Binary Input 1 Sense, do the following.

• Enter 0(=Normal) or 1(=Inverted) and press the ENTER key.

<BI1SGS>

To set the Binary Input 1 Settings Group Select, do the following.

• Enter 0(=Off) or 1(=1) or 2(=2) or 3(=3) or 4(=4) and press the ENTER key.

<Others>

- Enter 1(=On) to set the function and press the ENTER key. If not setting the function, enter 0(=Off) and press the ENTER key.
- After setting, press the END key to return to the "BI*" screen.

4.2.6.9 Binary Output

All the binary outputs of the GRD140 except the relay failure signal are user-configurable. It is possible to assign one signal or up to four ANDing or ORing signals to one output relay. Available signals are listed in Appendix C.

It is also possible to attach Instantaneous or delayed or latched reset timing to these signals.

Appendix H shows the factory default settings.

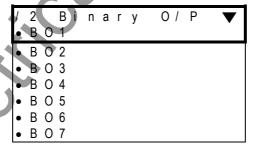
CAUTION

When having changed the binary output settings, release the latch state on a digest screen by pressing the RESET key for more than 3 seconds.

To configure the binary output signals, do the following:

Selection of output relay

• Select "Binary O/P" on the "Set. (change)" screen to display the "Binary O/P" screen.



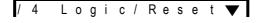
Note: The setting is required for all the binary outputs. If any of the binary outputs are not used, enter 0 to logic gates #1 to #4 in assigning signals.

• Select the output relay number (BO number) and press the ENTER key to display the "BO*" screen.



Setting the logic gate type and timer

• Select "Logic/Reset" to display the "Logic/Reset" screen.



L	0	g	i	С						0		_	
L O	R	Ĭ	Α	Ν	D								
R										0			
I	n	s	1	D		1	D	w /	L	а	t		

- Enter 0(=OR) or 1(=AND) to use an OR gate or AND gate and press the (ENTER) key.
- Enter 0(=Instantaneous) or 1(=Delayed) or 2(=Dwell) or 3(=Latched) to select the reset timing and press the (ENTER) key.
- Press the END key to return to the "BO*" screen.

Note: To release the latch state, push the [RESET] key for more than 3 seconds.

Assigning signals

• Select "Functions" on the "BO*" screen to display the "Functions" screen.

/	4		F	u	n	С	t	i	0	n	S	V
I	n		#	1 2	1							11
I	n		#	2			-			4	B	
ı	n		#	1	1							
				2	4							
I	n		#	4	^							
Т	В	O 0		2	0)	•		•		S

Assign signals to gates (In #1 to #4) by entering the number corresponding to each signal referring to Appendix C. Do not assign the signal numbers 471 to 477 (signal names: "BO1 OP" to "BO7 OP"). And set the delay time of timer TBO.

Note: If signals are not assigned to all the gates #1 to #4, enter 0 for the unassigned gate(s).

Repeat this process for the outputs to be configured.

4.2.6.10 LEDs

Three LEDs of the GRD140 are user-configurable. A configurable LED can be programmed to indicate the OR combination of a maximum of 4 elements, the individual statuses of which can be viewed on the LED screen as "Virtual LEDs." The signals listed in Appendix C can be assigned to each LED as follows.

CAUTION

When having changed the LED settings, must release the latch state on a digest screen by pressing the (RESET) key for more than 3 seconds.

Selection of LEDs

• Select "LED" on the "Set. (change)" screen to display the "LED" screen.



Selection of real LEDs

• Select "LED" on the "/2 LED" screen to display the "/3 LED" screen.

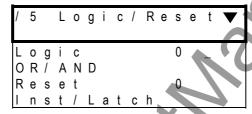
/	3			Ε	D	V
•	L	Ε	D	1		
•	L	Ε	D	2		
•	L	Ε	D	3		

• Select the LED number and press the ENTER key to display the "LED*" screen.



Setting the logic gate type and reset tipe

• Select "Logic/Reset" to display the "Logic/Reset" screen.

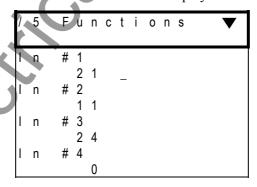


- Enter 0(=OR) or 1(=AND) to use an OR gate or AND gate and press the ENTER key.
- Enter 0(=Instantaneous) or 1(=Latched) to select the reset timing and press the ENTER key.
- Press the END key to return to the "LED*" screen.

Note: To release the latch state, refer to Section 4.2.1.

Assigning signals

• Select "Functions" on the "LED*" screen to display the "Functions" screen.



- Assign signals to gates (In #1 to #4) by entering the number corresponding to each signal referring to Appendix C.
 - ◆Note: If signals are not assigned to all the gates #1 to #4, enter 0 for the unassigned gate(s).
- Press the END key to return to the "LED*" screen.

Repeat this process for the outputs to be configured.

Selection of virtual LEDs

• Select "Virtual LED" on the "/2 LED" screen to display the "Virtual LED" screen.

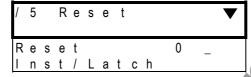
/	3		٧	i	r	t	u	а		L E D 🔻
•	I	N	D	1						
•	I	N	D	2						

• Select the IND number and press the ENTER key to display the "IND*" screen.



Setting the reset timing

• Select "Reset" to display the "Reset" screen.

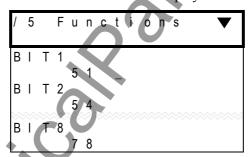


- Enter 0(=Instantaneous) or 1(=Latched) to select the reset timing and press the (ENTER) key.
- Press the END key to return to the "IND*" screen.

Note: To release the latch state, push the [RESET] key for more than 3 seconds.

Assigning signals

• Select "Functions" on the "IND*" screen to display the "Functions" screen.



 Assign signals to bits (1 to 8) by entering the number corresponding to each signal referring to Appendix C.

Note: If signals are not assigned to all the bits 1 to 8, enter 0 for the unassigned bit(s).

• Press the END key to return to the "IND*" screen.

Repeat this process for the outputs to be configured.

4.2.7 Testing

The sub-menu "Test" provides such functions as disabling the automatic monitoring function and forced operation of binary outputs.

Note: When operating the "Test" menu, the "IN SERVICE" LED is flickering. But if an alarm occurs during the test, the flickering stops. The "IN SERVICE" LED flickers only in a lighting state.

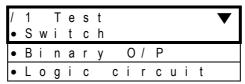
4.2.7.1 Scheme Switch

The automatic monitor function (A.M.F.) can be disabled by setting the switch [A.M.F] to "OFF". Disabling the A.M.F. inhibits trip blocking even in the event of a failure in the items being

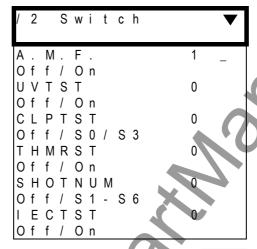
monitored by this function. It also prevents failures from being displayed on the "ALARM" LED and LCD described in Section 4.2.1. No events related to A.M.F. are recorded, either.

Disabling A.M.F. is useful for blocking the output of unnecessary alarms during testing.

• Select "Test" on the top "MENU" screen to display the "Test" screen.



• Select "Switch" to display the "Switch" screen.

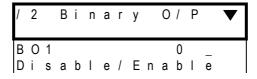


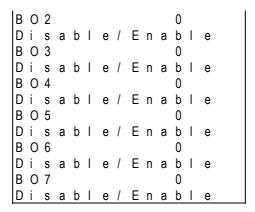
- Enter 0(=Off) to disable the A.M.F. and press the ENTER key.
- Enter 1(=On) to disable the UV block when testing UV elements and press the (ENTER) key.
- Enter 0(=Off) or 1(=State0) or 2(=State3) to set forcibly the test condition of the Cold Load Protection (CLPTST) and press the ENTER key.
- Enter 1(=On) to reset forcibly the thermal overload element for testing (THMRST) and press the (ENTER) key.
- Enter 0(=Off) or 1(=S1) or 2(=S2) or 3(=S3) or 4(=S4) or 5(=S5) to set shot number for autoreclose test and press the (=S1) key.
- Enter 1(=On) for IECTST to transmit 'test mode' to the control system by IEC60870-5-103 communication when testing the local relay, and press the ENTER key.
- Press the END key to return to the "Test" screen.

4.2.7.2 Binary Output Relay

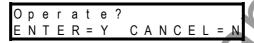
It is possible to forcibly operate all binary output relays for checking connections with the external devices. Forced operation can be performed on one or more binary outputs at a time.

• Select "Binary O/P" on the "Test" screen to display the "Binary O/P" screen. Then the LCD displays the name of the output relay.





- Enter 1(=Enable) and press the ENTER key to operate the output relays forcibly.
- After completing the entries, press the END key. Then the LCD displays the screen shown below.

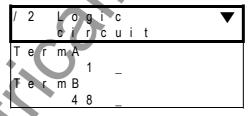


- Keep pressing the ENTER key to operate the assigned output relays.
- Release pressing the ENTER key to reset the operation.
- Press the CANCEL key to return to the upper "Binary O/P" screen.

4.2.7.3 Logic Circuit

It is possible to observe the binary signal level on the signals listed in Appendix C with monitoring jacks A and B.

• Select "Logic circuit" on the "Test" screen to display the "Logic circuit" screen.



- Enter a signal number to be observed at monitoring jack A and press the ENTER key.
- Enter the other signal number to be observed at monitoring jack B and press the (ENTER) key.

After completing the setting, the signals can be observed by the binary logic level at monitoring jacks A and B or by the LEDs above the jacks.

On screens other than the above screen, observation with the monitoring jacks is disabled.

4.3 Personal Computer Interface

The relay can be operated from a personal computer using an RS232C port on the front panel. On the personal computer, the following analysis and display of the fault currents are available in addition to the items available on the LCD screen.

Display of current and voltage waveforms: Oscillograph display
 Symmetrical component analysis: On arbitrary time span
 Harmonic analysis: On arbitrary time span
 Frequency analysis: On arbitrary time span

For the details, see the separate instruction manual "PC INTERFACE RSM100".

4.4 Relay Setting and Monitoring System

The Relay Setting and Monitoring (RSM) system is a system that retrieves and analyses the data on power system quantities, fault and event records and views or changes settings in individual relays via a telecommunication network using a remote PC.

Figure 4.4.1 shows the typical configuration of the RSM system via a protocol converter G1PR2. The relays are connected through twisted pair cables, and the maximum 256 relays can be connected since the G1PR2 can provide up to 8 ports. The total length of twisted pair wires should not exceed 1200 m. Relays are mutually connected using an RS485 port on the relay rear panel and connected to a PC RS232C port via G1PR2. Terminal resistor (150 ohms) is connected the last relay. The transmission rate used is 64 kbits/s.

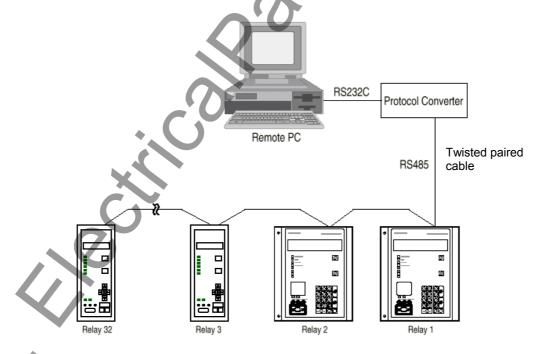


Figure 4.4.1 Relay Setting and Monitoring System

4.5 IEC 60870-5-103 Interface

The GRD140 supports the IEC60870-5-103 communication protocol. This protocol is mainly used when the relay communicates with a control system and is used to transfer the following measurand and status data from the relay to the control system. (For details, see Appendix M.)

- Measurand data: current, voltage, active power, reactive power, frequency
- Status data: events, fault indications, etc.

The protocol can be used through the RS485 port on the relay rear panel.

The relay supports two baud-rates 9.6kbps and 19.2kbps, and supports two normalizing factors 1.2 and 2.4 for measurand. These are selected by setting. See Section 4.2.6.4.

The data transfer from the relay can be blocked by the setting.

For the settings, see the Section 4.2.6.

4.6 Clock Function

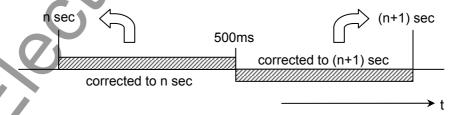
The clock function (Calendar clock) is used for time-tagging for the following purposes:

- Event records
- Disturbance records
- Fault records

The calendar clock can run locally or be synchronised with the external clock such as the binary time standard input signal, RSM clock or IEC60870-5-103. This can be selected by setting.

The "clock synchronise" function synchronises the relay internal clock to the binary input signal by the following method. Since the BI signal is an "ON" or "OFF" signal which cannot express year-month-day and hour-minute-second etc, synchronising is achieved by setting the number of milliseconds to zero. This method will give accurate timing if the synchronising BI signal is input every second.

Synchronisation is triggered by an "OFF" to "ON" (rising edge) transition of the BI signal. When the trigger is detected, the millisecond value of the internal clock is checked, and if the value is between 0~500ms then it is rounded down. If it is between 500~999ms then it is rounded up (ie the number of seconds is incremented).



When the relays are connected with the RSM system as shown in Figure 4.4.1 and selected "RSM" in the time synchronisation setting, the calendar clock of each relay is synchronised with the RSM clock. If the RSM clock is synchronised with the external time standard, then all the relay clocks are synchronised with the external time standard.

TOSHIBA

5. Installation

5.1 Receipt of Relays

When relays are received, carry out the acceptance inspection immediately. In particular, check for damage during transportation, and if any is found, contact the vendor.

Always store the relays in a clean, dry environment.

5.2 Relay Mounting

A flush mounting relay is included. Appendix F shows the case outline.

For details of relay withdrawal and insertion, see Section 6.7.3.

5.3 Electrostatic Discharge

ACAUTION

Do not take out the relay unit outside the relay case since electronic components on the modules are very sensitive to electrostatic discharge. If it is absolutely essential to take the modules out of the case, do not touch the electronic components and terminals with your bare hands. Additionally, always put the module in a conductive anti-static bag when storing it.

5.4 Handling Precautions

A person's normal movements can easily generate electrostatic potentials of several thousand volts. Discharge of these voltages into semiconductor devices when handling electronic circuits can cause serious damage. This damage often may not be immediately apparent, but the reliability of the circuit will have been reduced.

The electronic circuits are completely safe from electrostatic discharge when housed in the case. Do not expose them to risk of damage by withdrawing the relay unit unnecessarily.

The relay unit incorporates the highest practical protection for its semiconductor devices. However, if it becomes necessary to withdraw the relay unit, precautions should be taken to preserve the high reliability and long life for which the equipment has been designed and manufactured.

ACAUTION

- Before removing the relay unit, ensure that you are at the same electrostatic potential as the equipment by touching the case.
- Use the handle to draw out the relay unit. Avoid touching the electronic components, printed circuit board or connectors.
- Do not pass the relay unit to another person without first ensuring you are both at the same electrostatic potential. Shaking hands achieves equipotential.
- Place the relay unit on an anti-static surface, or on a conducting surface which is at the same potential as yourself.
- Do not place the relay unit in polystyrene trays.

It is strongly recommended that detailed investigations on electronic circuitry should be carried out in a Special Handling Area such as described in the aforementioned IEC 60747.

5.5 External Connections

External connections for each relay model are shown in Appendix G.

6. Commissioning and Maintenance

6.1 Outline of Commissioning Tests

The GRD140 is fully numerical and the hardware is continuously monitored.

Commissioning tests can be kept to a minimum and need only include hardware tests and the conjunctive tests. The function tests are at the user's discretion.

In these tests, user interfaces on the front panel of the relay or local PC can be fully applied.

Test personnel must be familiar with general relay testing practices and safety precautions to avoid personal injuries or equipment damage.

Hardware tests

These tests are performed for the following hardware to ensure that there is no hardware defect. Defects of hardware circuits other than the following can be detected by monitoring which circuits function when the DC power is supplied.

User interfaces
Binary input circuits and output circuits
AC input circuits

Function tests

These tests are performed for the following functions that are fully software-based.

Measuring elements Metering and recording

Conjunctive tests

The tests are performed after the relay is connected with the primary equipment and other external equipment.

The following tests are included:

On load test: phase sequence check and polarity check Tripping circuit test Reclosing circuit test

6.2 Cautions

6.2.1 Safety Precautions

ACAUTION

- The relay rack is provided with an earthing terminal.

 Before starting the work, always make sure the relay rack is earthed.
- When connecting the cable to the back of the relay, firmly fix it to the terminal block and attach the cover provided on top of it.
- Before checking the interior of the relay, be sure to turn off the power.

Failure to observe any of the precautions above may cause electric shock or malfunction.

6.2.2 Cautions on Tests

ACAUTION

- While the power is on, do not drawout/insert the relay unit.
- Before turning on the power, check the following:
 - Make sure the polarity and voltage of the power supply are correct.
 - Make sure the CT circuit is not open.
 - Make sure the VT circuit is not short-circuited.
- Be careful that the relay is not damaged due to an overcurrent or overvoltage.
- If settings are changed for testing, remember to reset them to the original settings.

Failure to observe any of the precautions above may cause damage or malfunction of the relay.



6.3 Preparations

Test equipment

The following test equipment is required for the commissioning tests.

- 1 Single-phase current source
- 1 Three-phase current source
- 1 Single-phase voltage source
- 1 Three-phase voltage source
- 1 DC power supply
- 3 Phase angle meter
- 3 AC ammeter
- 3 AC voltmeter
- 1 Time counter, precision timer
- 1 PC (not essential)

Relay settings

Before starting the tests, it must be specified whether the tests will use the user's settings or the default settings.

For the default settings, see the Appendix H Relay Setting Sheet.

Visual inspection

After unpacking the product, check for any damage to the relay case. If there is any damage, the internal module might also have been affected. Contact the vendor.

Relay ratings

Check that the items described on the nameplate on the front of the relay conform to the user's specification. The items are: relay type and model, AC current and frequency ratings, and auxiliary DC supply voltage rating.

Local PC

When using a local PC, connect it with the relay via the RS232C port on the front of the relay. RSM100 software is required to run the PC.

For the details, see the separate volume "PC INTERFACE RSM100".

6.4 Hardware Tests

The tests can be performed without external wiring, but a DC power supply and AC current and voltage sources are required.

6.4.1 User Interfaces

This test ensures that the LCD, LEDs and keys function correctly.

LCD display

• Apply the rated DC voltage and check that the LCD is off.

Note: If there is a failure, the LCD will display the "Err: " screen when the DC voltage is applied.

• Press the RESET key for one second or more and check that black dots appear on the whole screen.

LED display

- Apply the rated DC voltage and check that the "IN SERVICE" LED is lit in green.
- Press the (RESET) key for one second or more and check that remaining five LEDs are lit in red or yellow. (Programmable LEDs are yellow.)

VIEW and RESET keys

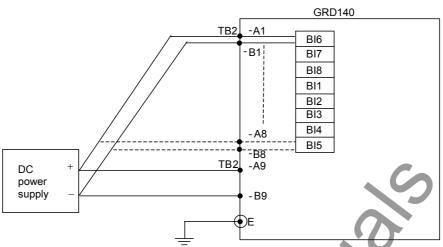
- Press the VIEW key when the LCD is off and check that the "Virtual LED" and "Metering" screens are sequentially displayed on the LCD.
- Press the RESET key and check that the LCD turns off.

Other operation keys

- Press any key when the LCD is off and check that the LCD displays the "MENU" screen. Press the END key to turn off the LCD.
- Repeat this for all keys.

6.4.2 Binary Input Circuit

The testing circuit is shown in Figure 6.4.1.



Note: Models 400 and 420 are not provided with BI6 to BI8.

Figure 6.4.1 Testing Binary Input Circuit

• Display the "Binary I/O" screen from the "Status" sub-menu.

/ 2	В	i	n	а	r	у		I	/	0
ΙP	[0	0	0	0		0	0	0	0]
ОР	[0	0	0	0		0	0	0	0]

• Apply the rated DC voltage to terminal A1-B1, A2-B2, ..., A8-B8 of terminal block TB2. Check that the status display corresponding to the input signal (IP) changes from 0 to 1. (For details of the binary input status display, see Section 4.2.4.2.)

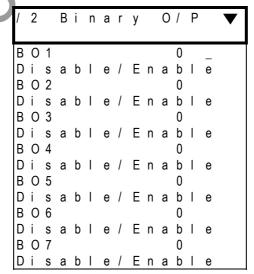
Note: Models 400 and 420 are not provided with BI6 to BI8.

The user will be able to perform this test for one terminal to another or for all the terminals at once.

6.4.3 Binary Output Circuit

This test can be performed by using the "Test" sub-menu and forcibly operating the relay drivers and output relays. Operation of the output contacts is monitored at the output terminal. The output contact and corresponding terminal number are shown in Appendix G.

• Select "Binary O/P" on the "Test" screen to display the "Binary O/P" screen. The LCD displays the name of the output relay.



- Enter 1 and press the ENTER key.
- After completing the entries, press the END key. The LCD will display the screen shown below. If 1 is entered for all the output relays, the following forcible operation can be performed collectively.

Operate? ENTER=Y CANCEL=N

- Keep pressing the ENTER key to operate the output relays forcibly.
- Check that the output contacts operate at the terminal.
- Stop pressing the ENTER key to reset the operation

6.4.4 AC Input Circuits

This test can be performed by applying known values of voltage and current to the AC input circuits and verifying that the values applied coincide with the values displayed on the LCD screen.

The testing circuits are shown in Figures 6.4.2 and 6.4.3. A three-phase voltage source and a single-phase current source are required.

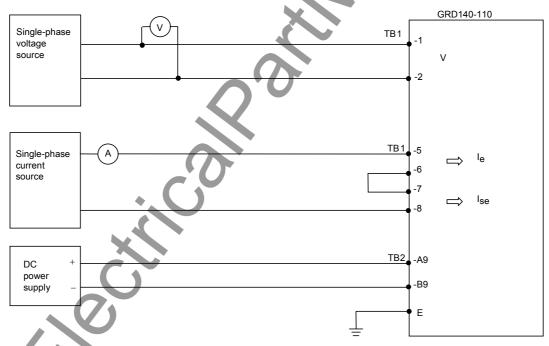


Figure 6.4.2 Testing AC Input Circuit for Model 110

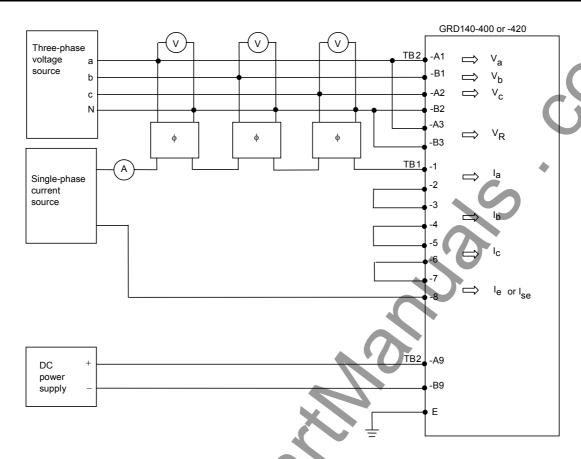


Figure 6.4.3 Testing AC Input Circuit for Models 400 and 420

• Check that the metering data is set to be expressed as secondary values on the "Metering switch" screen.

"Settings" sub-menu → "Status" screen → "Metering switch" screen

If the setting is "Display Value = Primary", change the setting in the "Metering switch". Remember to reset it to the initial setting after the test is finished.

• Open the "Metering" screen in the "Status" sub-menu.

"Status" sub-menu → "Metering" screen

• Apply AC rated voltages and currents and check that the displayed values are within \pm 5% of the input values.

6.5 Function Test

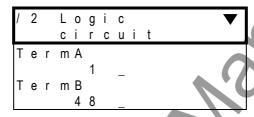
CAUTION

The function test may cause the output relays to operate including the tripping output relays. Therefore, the test must be performed with tripping circuits disconnected.

6.5.1 Measuring Element

Measuring element characteristics are realized by software, so it is possible to verify the overall characteristics by checking representative points.

Operation of the element under test is observed by the binary output signal at monitoring jacks A or B or by the LED indications above the jacks. In any case, the signal number corresponding to each element output must be set on the "Logic circuit" screen of the "Test" sub-menu.



When a signal number is entered for the Term A line, the signal is observed at monitoring jack A and when entered for the Term B line, it is observed at monitoring jack B.

Note: The voltage level at the monitoring jacks is +5V for logic level "1" and less than 0.1V for logic level "0".

CAUTION

- Use test equipment with more than 1 $k\Omega$ of internal impedance when observing the output signal at the monitoring jacks.
- Do not apply an external voltage to the monitoring jacks.
- Do not leave the A or B terminal shorted to 0V terminal for a long time.

In case of a three-phase element, it is sufficient to test for a representative phase. The A-phase element is selected hereafter. Further, the [APPL-CT] and [APPL-VT] settings are selected "3P" and "3PV".

Note: Operating time test of measuring relay elements at monitoring jack A or B is not including the operation of binary output. Whole the operating time test, if required, should be measured at a binary output relay.

6.5.1.1 Overcurrent and undercurrent element OC1 to OC4, UC1, UC2 and CBF and Earth fault element EF1 to EF4 and SEF1 to SEF4

The overcurrent element is checked on the operating current value and operating time for IDMT curve.

Operating current check

Figure 6.5.1 shows a testing circuit. The operating current value is checked by increasing or decreasing the magnitude of the current applied.

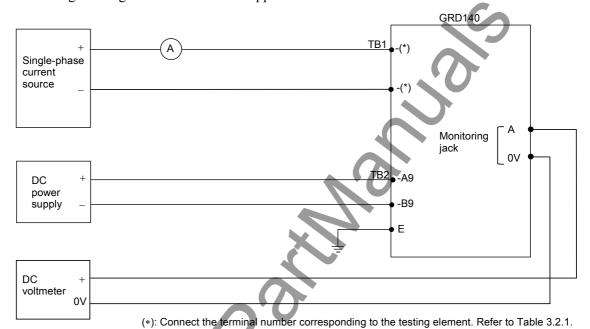


Figure 6.5.1 Operating Current Value Test

The output signal of testing element is assigned to the monitoring jack A.

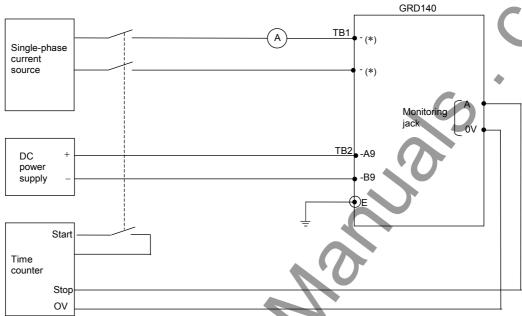
The output signal numbers of the elements are as follows:

Element	Signal No.	Element	Signal No.	Element	Signal No.	Element	Signal No.
OC1-A	101	EF1	131	SEF1	141	UC1-A	161
OC2-A	107	EF2	133	SEF2	143	UC2-A	164
OC3-A	113	EF3	135	SEF3	145	CBF-A	173
OC4-A	116	EF4	136	SEF4	146		

- Enter the signal number to observe the operation at the LED as shown in Section 6.5.1 and press the ENTER key.
- Set the scheme switches [***-DIR] to "NON".
- Apply a test current and change the magnitude of the current applied and measure the value at which the element operates.
 - Check that the measured value is within 5% of the setting value.

Operating time check for IDMT curve

The testing circuit is shown in Figure 6.5.2.



(*): Connect the terminal number corresponding to the testing element. Refer to Table 3.2.1.

Figure 6.5.2 Testing IDMT

One of the inverse time characteristics can be set, and the output signal numbers of the IDMT elements are as follows:

Element	Signal No.
OC1-A	101
EF1	131
SEF1	141

Fix the time characteristic to test by setting the scheme switch MOC1, MEF1 or MSE1 on the "OC", "EF" or "SEF" screen.

Example: "Settings" sub-menu \rightarrow "Protection" screen \rightarrow "Group*" screen \rightarrow "OC" screen

The test procedure is as follows:

- Enter the signal number to observe the operating time at the monitoring jack A as shown in Section 6.5.1.
- Apply a test current and measure the operating time. The magnitude of the test current should be between $1.2 \times I_S$ to $20 \times I_S$, where I_S is the current setting.
- Calculate the theoretical operating time using the characteristic equations shown in Section 2.1.1. Check that the measured operating time is within IEC 60255-3 class 5.

6.5.1.2 Directional characteristic test

The directional characteristic is checked as follows:

OC element for Models 400 and 420

The test circuit is shown in Figure 6.5.3.

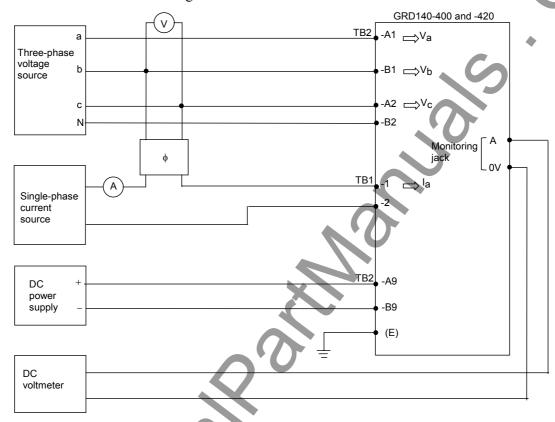


Figure 6.5.3 Testing OC Element

OC elements and their output signal number are shown in Section 6.5.1.1.

The following shows the case when testing OC1.

- Select "Logic circuit" on the Test screen to display the "Logic circuit" screen.
- Enter the signal number to be observed at monitoring jack as shown in Section 6.5.1.
- Set the scheme switch [OC1-DIR] to "FWD".
- Apply three-phase rated voltage and single-phase test current IT (= I_a).
 Set IT to lag V_{bc} by OC characteristic angle OC θ. (The default setting of OC θ is -45°.)
- Changing the magnitude of IT while retaining the phase angle with the voltages, and measure
 the current at which the element operates. Check that the measured current magnitude is within
 ± 5% of the current setting.

EF element

The test circuit is shown in Figure 6.5.4.

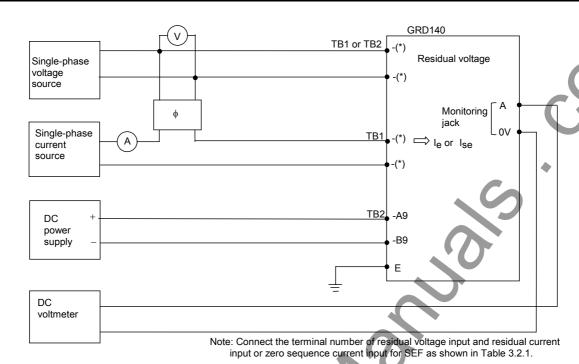


Figure 6.5.4 Testing EF and SEF Elements

EF elements and their output signal number are shown in Section 6.5.1.1.

The following shows the case when testing EF1.

- Select "Logic circuit" on the "Test menu" screen to display the "Logic circuit" screen.
- Enter the signal number to be observed at monitoring jack A as shown in Section 6.5.1.
- Set the scheme switch [EF1-DIR] to "FWD".
- Apply the rated voltage VT (= V_0) and single-phase test current IT. Set IT to lag V_0 by EF characteristic angle EF θ . (The default setting of EF θ is -45°.)
- Changing the magnitude of IT while retaining the phase angle with the voltages, and measure
 the current at which the element operates. Check that the measured current magnitude is within
 ± 5% of the current setting.

SEF element

The test circuit is shown in Figure 6.5.4.

SEF elements and their output signal number are shown in Section 6.5.1.1.

The following shows the case when testing SEF1.

- Select "Logic circuit" on the "Test menu" screen to display the "Logic circuit" screen.
- Enter the signal number to be observed at monitoring jack A as shown in Section 6.5.1.
- Set the scheme switch [SE1-DIR] to "FWD".
- Apply the rated voltage VT (= V₀) and single-phase test current IT (= I_{Se}).
 Set IT to lag V₀ by SEF characteristic angle SE θ. (The default setting of SE θ is 0°.)
- Changing the magnitude of IT while retaining the phase angle with the voltages, and measure the current at which the element operates. Check that the measured current magnitude is within ± 5% of the current setting.

6.5.1.3 Thermal overload element THM-A and THM-T

The testing circuit is same as the circuit shown in Figure 6.5.2.

The output signal of testing element is assigned to the monitoring jack A.

The output signal numbers of the elements are as follows:

Element	Signal No.
THM-A	167
THM-T	168

To test easily the thermal overload element, the scheme switch [THMRST] in the "Switch" screen on the "Test" menu is used.

- Set the scheme switch [THMRST] to "ON".
- Enter the signal number to observe the operation at the monitoring jack A as shown in Section 6.5.1.
- Apply a test current and measure the operating time. The magnitude of the test current should be between $1.2 \times I_S$ to $10 \times I_S$, where I_S is the current setting.

CAUTION

After the setting of a test current, apply the test current after checking that the THM% has become 0 on the "Metering" screen.

• Calculate the theoretical operating time using the characteristic equations shown in Section 2.1.5. Check that the measured operating time is within 5%.

6.5.1.4 Negative sequence overcurrent element NOC1 and NOC2

The testing circuit is shown in Figure 6.5.5.

The output signal of testing element is assigned to the monitoring jack A.

The output signal numbers of the elements are as follows:

Element	Signal No.
NOC1	169
NOC2	171

- Enter the signal number to observe the operation at the monitoring jack A as shown in Section 6.5.1.
- Apply the three-phase balance current and the operating current value is checked by increasing the magnitude of the current applied.

Check that the measured value is within 5% of the setting value.

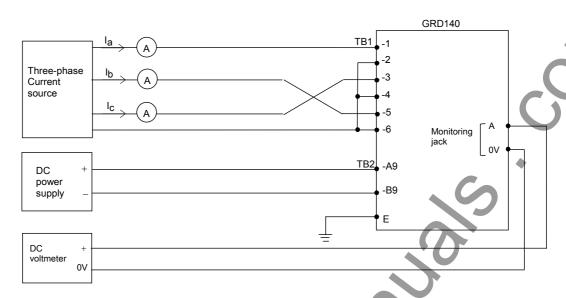


Figure 6.5.5 Testing NOC elements

Directional characteristic test of NOC element

The test circuit is shown in Figure 6.5.6.

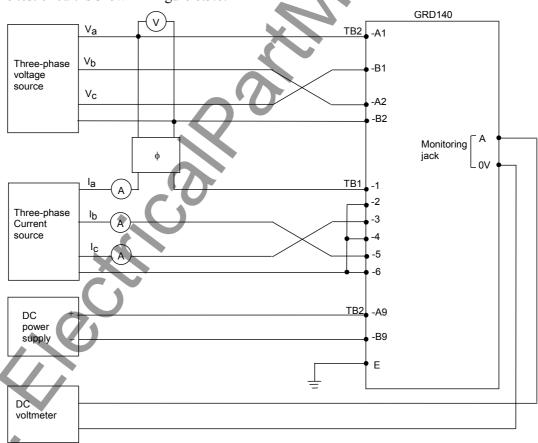


Figure 6.5.6 Testing Directional Characteristic of NOC Element

The following shows the case when testing NOC1.

- Select "Logic circuit" on the Test screen to display the "Logic circuit" screen.
- Enter the signal number to be observed at monitoring jack as shown in Section 6.5.1.

- Set the scheme switch [NC1-DIR] to "FWD".
- Apply three-phase balance voltage (=30V) and three-phase balance current. Set I_a to lag V_a by NOC characteristic angle NC θ . (The default setting of NC θ is -45°.)
- Changing the magnitude of three-phase balance current while retaining the phase angle with
 the voltages, and measure the current I_a at which the element operates. Check that the
 measured current magnitude is within ± 5% of the current setting.

6.5.1.5 Broken conductor detection element BCD

The testing circuit is shown in Figure 6.5.7.

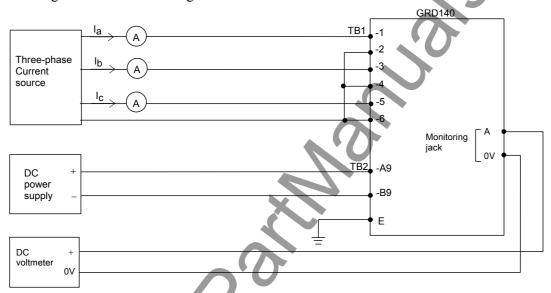


Figure 6.5.7 Testing BCD element

The output signal of testing element is assigned to the monitoring jack A.

The output signal numbers of the elements are as follows:

Element	Signal No.
BCD	172

- Enter the signal number to observe the operation at the monitoring jack A as shown in Section 6.5.1.
- Apply the three-phase balance current at 10% of the rated current and interrupt a phase current.

Then, check the BCD element operates.

6.5.1.6 Cold load protection

The testing circuit is same as the circuit shown in Figure 6.5.1.

To check the cold load protection function, the scheme switch [CLPTST] in the "Switch" screen on the "Test" menu is used. Test the item of OC1 shown in Section 6.5.1.1.

- Set the scheme switch [CLPTST] to "S0".
 Check that the OC1 operates at the setting value of normal setting group.
- Next, set the scheme switch [CLPTST] to "S3".

Check that the OC1 operates at the setting value of cold load setting group [CLSG].

6.5.1.7 Overvoltage and undervoltage elements

The testing circuit is shown in Figure 6.5.8.

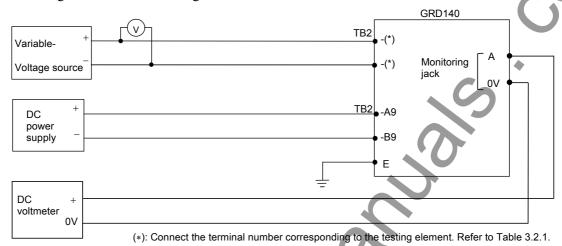


Figure 6.5.8 Operating Value Test Circuit

The output signal of testing element is assigned to the monitoring jack A.

Overvoltage and undervoltage elements and their output signal number are listed below.

Element	Signal No.
OV1-A	191
OV2-A	197
UV1-A	201
UV2-A	207
ZOV1	211
ZOV2	213

• Enter the signal number to observe the operation at the monitoring jack A as shown in Section 6.5.1.

Operating value test of OV1, OV2, ZOV1, ZOV2

- Apply a rated voltage as shown in Figure 6.5.8.
- Increase the voltage and measure the value at which the element operates. Check that the measured value is within \pm 5% of the setting.

Operating value test of UV1, UV2

- Apply a rated voltage and frequency as shown Figure 6.5.8.
- Decrease the voltage and measure the value at which the element operates. Check that the measured value is within \pm 5% of the setting.

Operating time check of OV1, UV1, ZOV1 IDMT curves

- Change the voltage from the rated voltage to the test voltage quickly and measure the operating time.
- Calculate the theoretical operating time using the characteristic equations shown in Section 2.2.1 and 2.2.2. Check the measured operating time.

6.5.1.8 Negative sequence overvoltage element NOV1 and NOV2

The testing circuit is shown in Figure 6.5.9.

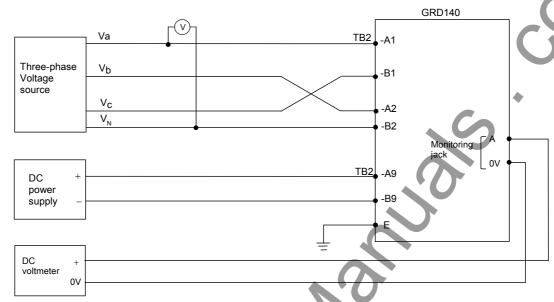


Figure 6.5.9 Testing NOV elements

The output signal of testing element is assigned to the monitoring jack A.

The output signal numbers of the elements are as follows:

Element	Signal No.
NOV1	214
NOV2	216

- Enter the signal number to observe the operation at the monitoring jack A as shown in Section 6.5.1.
- Apply the three-phase balance voltage and the operating voltage value is checked by increasing the magnitude of the voltage applied.

Check that the measured value is within 5% of the setting value.

Operating time check of NOV1 IDMT curve

- Change the voltage from the rated voltage to the test voltage quickly and measure the operating time.
- Calculate the theoretical operating time using the characteristic equations shown in Section 2.2.4. Check the measured operating time.

6.5.1.9 Frequency Elements

The testing circuit is shown in Figure 6.5.10.

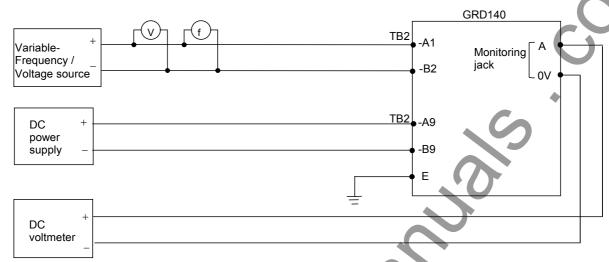


Figure 6.5.10 Operating Value Test Circuit

The output signal of testing element is assigned to the monitoring jack A.

Frequency elements and their output signal number are listed below.

Element	Signal No.
FRQ1	218
FRQ2	219
FRQ3	220
FRQ4	221
FRQBLK	222

Overfrequency or underfrequency elements FRQ1 to FRQ4

- Enter the signal number to observe the operation at the monitoring jack A as shown in Section 6.5.1.
- Apply a rated voltage and frequency as shown in Figure 6.5.10.

In case of overfrequency characteristic,

• Increase the frequency and measure the value at which the element operates. Check that the measured value is within ± 0.005 Hz of the setting.

In case of underfrequency characteristics,

• Decrease the frequency and measure the value at which the element operates. Check that the measured value is within ± 0.005 Hz of the setting.

Undervoltage block test, FRQBLK

- Apply a rated voltage and change the magnitude of frequency to operate an element.
- Keep the frequency that the element is operating, and change the magnitude of the voltage applied from the rated voltage to less than FRQBLK setting voltage. And then, check that the element resets.

6.5.2 Protection Scheme

In the protection scheme tests, a dynamic test set is required to simulate power system pre-fault, fault and post-fault conditions.

Tripping is observed with the tripping command output relays after a simulated fault occurs.

Circuit Breaker failure tripping

- Set the scheme switch [BTC] to "ON" and [RTC] to "DIR" or "OC".
- Apply a fault, retain it and input an external trip signal. Check that the retrip output relays
 operate after the time setting of the TRTC and the adjacent breaker tripping output relay
 operates after the time setting of the TBTC.

6.5.3 Metering and Recording

The metering function can be checked while testing the AC input circuit. See Section 6.4.4.

Fault recording can be checked while testing the protection schemes. Open the "Fault record" screen and check that the descriptions are correct for the fault concerned.

Recording events are listed in Appendix D. There are internal events and external events by binary input commands. Event recording on the external event can be checked by changing the status of binary input command signals. Change the status in the same way as the binary input circuit test (see Section 6.4.2) and check that the description displayed on the "Event record" screen is correct. Some of the internal events can be checked in the protection scheme tests.

Disturbance recording can be checked while testing the protection schemes. The LCD display only shows the date and time when a disturbance is recorded. Open the "Disturbance record" screen and check that the descriptions are correct.

Details can be displayed on the PC. Check that the descriptions on the PC are correct. For details on how to obtain disturbance records on the PC, see the RSM100 Manual.

6.6 Conjunctive Tests

6.6.1 On Load Test

To check the polarity of the current and voltage transformers, check the load current, system voltage and their phase angle with the metering displays on the LCD screen.

- Open the "Auto-supervision" screen check that no message appears.
- Open the following "Metering" screen from the "Status" sub-menu to check the above.

/		3		С	u	r	r	e	n	t					▼
ľ		а		Ŭ	u	•	•	*	*		*	*	k	Α	Not available for model 110 and APPL=1P setting in models 400 and 420.
ľ								*	*	*		*	0		Total and to thouse the direction of the second of the sec
I		b						*	*		*	*	k °	Α	Not available for model 110 and APPL=1P and 2P settings in models 400 and 420
I		С						*	*	*	*	*	k	Α	Not available for model 110 and APPL=1P setting in models 400 and 420.
		е						*	*	*		*	° k	Α	
ľ		C						*	*	*		*	0	$^{\wedge}$	
I		s	е				*	*	*	*		*		Α	Not available for model 400.
								*	*	*		*	0		
I		1						*	*		*	*	k	Α	Not available for model 110 and APPL=1P and 2P settings in models 400 and 420
ı.		_						*	*	*		*	•		
I		2						*	*		*	*	k °	Α	Not available for model 110 and APPL=1P and 2P settings in models 400 and 420
l,		2	1	ı	1			*	*	т		*			Not available for model 110 and APPL=1P and 2P settings in models 400 and 420
ľ			M	•	•			*	*	*	•••	*		%	Not available for model 110 and APPL=1P and 2P setting in models 400 and 420.
		a								•			k	V	Not available for model 110 and APPL=1P setting in models 400 and 420.
'	′	а	11				~	*	*	*	*	*	0	V	Not available for filoder 110 and AFFL-5F and 2F settings in filoders 400 and 420
١	/	b	n				*	*	*		*	*	k	V	Not available for model 110 and APPL=3P and 2P settings in models 400 and 420
		-						*	*	*		*	0		2 3 2 2 3 2 3 3 3 3 3 3 3 3 3 3 3 3 3 3
١	/	С	n				*	*	*		*	*	k	٧	Not available for model 110 and APPL=3P and 2P settings in models 400 and 420
								*	*	*		*	0		
١	/	е					*	*	*		*	*	k	V	, C
,	,	_	L					*	*	*	•	*	8	v	
١,	/	а	b				*	*	*		*	*	K	V	Not available for model 110.
\	/	b	С				*	*	*	* ·	*	*	k	V	Not available for model 110.
Ι,	,	J	Ü				•	*	*	*		*	°	٧	Not available for frioder 110.
١	/	С	а				*	*	*		*	*	k	V	Not available for model 110.
								*	*	*		*	0		
١	/	0					*	*	*		*	*	k	V	Not available for model 110.
	,							*	*	*	٠	*	•	.,	
١,	/	1					*	*	*		*	*	k	V	Not available for model 110.
\	/	2		V	7			*	*	ж		*	k	V	Not available for model 110.
`	'	_					~	*	*	*	~	*	0	V	Not available for model 110.
f								*	*		*	*	Н	z	Not available for model 110.
F		F	4	•		-	*		*	*	*				Not available for model 110. Total 3 phase power factor.
N.)				-	*	*	*	*	*	*	k	W	1	Not available for model 110. Total 3 phase active power.
(2				-	*	*	*	*	*	*	k	٧	a i	
9	3				_	*	*	*	*	*	*	k		Α	Not available for model 110. Total 3 phase apparent power.

Note: The magnitude of current can be set in values on the primary side or on the secondary side by the setting. (The default setting is the secondary side.)

Directional check of Directional phase overcurrent element

The rightness of the polarity of directional phase overcurrent element is verified if current and voltage values and their phase angle are all right in above metering check. Further, it can be also checked as follows:

• Select "Direction" on the "Metering" screen to display "Direction" screen, and then the direction of current is displayed. (See Section 4.2.4.1.) Check the direction of current is correct.

Note: Not available for models 110 and APPL=1P and 2P settings in models 400 and 420.

Directional check of Directional earth fault element

The rightness of the polarity of directional earth fault element is verified if current and voltage values and their phase angle are all right in above metering check. Further, if required, it can be also checked as follows:

• Check the operation of this element by simulating the unbalanced condition of three phase voltages and currents.

Note: Not available for APPL=1P and 2P settings in models 400 and 420.

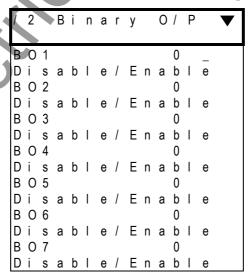
CAUTION: Must block the tripping circuit while checking by simulating the unbalanced condition. After checking, must return the connections to their original state.

6.6.2 Tripping and Reclosing Circuit Test

The tripping circuit including the circuit breaker is checked by forcibly operating the output relay and monitoring the circuit breaker to confirm that it is tripped. Forcible operation of the output relay is performed on the "Binary O/P" screen of the "Test" sub-menu as described in Section 6.4.3.

Tripping circuit

- Set the breaker to be closed.
- Select "Binary O/P" on the "Test" sub-menu screen to display the "Binary O/P" screen.



BO1 to BO7 are output relays with one normally open contact.

• Enter 1 for BO1 and press the ENTER key.

• Press the (END) key. Then the LCD displays the screen shown below.

Operate? ENTER=Y CANCEL=N

- Keep pressing the ENTER key to operate the output relay BO1 and check that the A-phase breaker is tripped.
- Stop pressing the ENTER key to reset the operation.
- Repeat the above for BO2 to BO7.

Reclosing circuit

- Ensure that the circuit breaker is open.
- Select "Binary O/P" on the "Test" sub-menu screen to display the "Binary O/P" screen.
- Select the BO number which is an autoreclose command output relay with one normally open contact.

Note: The autoreclose command is assigned to any of the output relays by the user setting

• Operate the BO by the same manner as above.

6.7 Maintenance

6.7.1 Regular Testing

The relay is almost completely self-supervised. The circuits that can not be supervised are binary input and output circuits and human interfaces.

Therefore, regular testing is minimised to checking the unsupervised circuits. The test procedures are the same as described in Sections 6.4.1, 6.4.2 and 6.4.3.

6.7.2 Failure Tracing and Repair

Failures will be detected by automatic supervision or regular testing.

When a failure is detected by supervision, a remote alarm is issued with the binary output relay of FAIL and the failure is indicated on the front panel with LED indicators or LCD display. It is also recorded in the event record.

Failures detected by supervision are traced by checking the "Err: " screen on the LCD. Table 6.7.1 shows LCD messages and failure locations.

The locations marked with (1) have a higher probability than locations marked with (2).

Message **Failure location** Relay Unit AC cable CB or cable Err: SUM ×(Flash memory) Err: RAM \times (SRAM) Err: BRAM ×(Backup RAM) Err: EEP ×(EEPROM) Err: A/D ×(A/D converter) Err: DC \times (DC power supply circuit) Err: TC Tripping circuit)(1) \times (2) Err: CT, Err: V0, Er × (AC input circuit)(1) \times (2) Err: CB × (Circuit breaker)(1) \times (2) Err: CTF × (AC input circuit)(2) \times (1) Err: VTF1, Err: VTF2 × (AC input circuit)(2) \times (1)

Table 6.7.1 LCD Message and Failure Location

Probable failure location in the relay unit including its peripheral circuits.

If no message is shown on the LCD, this means that the failure location is either in the DC power supply circuit or in the microprocessors. If the "ALARM" LED is off, the failure is in the DC power supply circuit. If the LED is lit, the failure is in the microprocessors. Replace the relay unit in both cases after checking if the correct DC voltage is applied to the relay.

If a failure is detected by automatic supervision or regular testing, replace the failed relay unit.

Note: When a failure or an abnormality is detected during the regular test, confirm the following first:

- Test circuit connections are correct.
- Modules are securely inserted in position.
- Correct DC power voltage is applied.

- Correct AC inputs are applied.
- Test procedures comply with those stated in the manual.

6.7.3 Replacing Failed Relay Unit

If the failure is identified to be in the relay unit and the user has a spare relay unit, the user can recover the protection by replacing the failed relay unit.

Repair at the site should be limited to relay unit replacement. Maintenance at the component level is not recommended.

Check that the replacement relay unit has an identical Model Number and relay version (software type form) as the removed relay.

The Model Number is indicated on the front of the relay. For the relay version, see Section 4.2.5.1.

Replacing the relay unit

CAUTION After replacing the relay unit, check the settings.

The procedure of relay withdrawal and insertion is as follows:

• Switch off the DC power supply.

Hazardous voltage may remain in the DC circuit just after switching off the DC power supply. It takes about 30 seconds for the voltage to discharge.

- Disconnect the trip outputs.
- Short-circuit all AC current inputs. Open all AC voltage inputs.
- Unscrew the relay front cover.
- Unscrew the binding screw on the handle.
- To remove the relay unit from its case, pull up the handle and pull the handle towards you. (See Figure 6.7.1.)
- Insert the (spare) relay unit in the reverse procedure.

CAUTION To avoid risk of damage:

- Keep the handle up when inserting the relay unit into the case.
- Do not catch the handle when carrying the relay unit.
- Check that the relay unit and its case have the identical Model Number when inserting the relay unit.

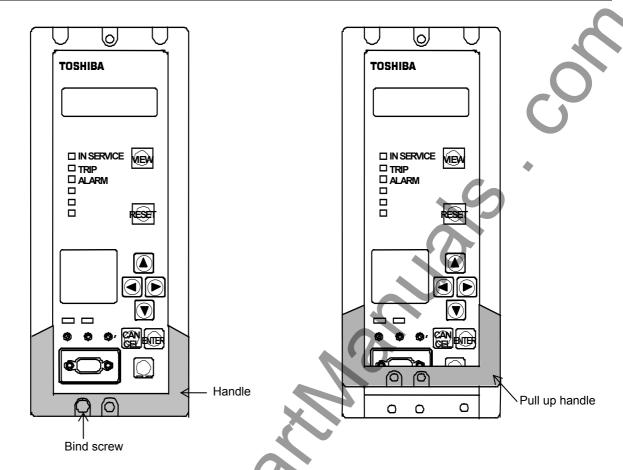


Figure 6.7.1 Handle of Relay Unit

6.7.4 Resumption of Service

After replacing the failed relay unit or repairing failed external circuits, take the following procedures to restore the relay to the service.

- Switch on the DC power supply and confirm that the "IN SERVICE" green LED is lit and the "ALARM" red LED is not lit.
- Supply the AC inputs and reconnect the trip outputs.

6.7.5 Storage

The spare relay should be stored in a dry and clean room. Based on IEC Standard 60255-6 the storage temperature should be -25° C to $+70^{\circ}$ C, but the temperature of 0° C to $+40^{\circ}$ C is recommended for long-term storage.

7. Putting Relay into Service

The following procedure must be adhered to when putting the relay into service after finishing the commissioning tests or maintenance tests.

- Check that all the external connections are correct.
- Check the settings of all measuring elements, timers, scheme switches, recordings and clock are correct.

In particular, when settings are changed temporarily for testing, be sure to restore them.

- Clear any unnecessary records on faults, alarms, events, disturbances and counters which are recorded during the tests.
- Press the VIEW key and check that no failure message is displayed on the "Alarm view" screen.
- Check that the green "IN SERVICE" LED is lit and no other LEDs are lit on the front panel.

Appendix A

Programmable Reset Characteristics and Implementation of Thermal Model to IEC60255-8

Programmable Reset Characteristics

The overcurrent stages for phase and earth faults, OC1 and EF1, each have a programmable reset feature. Resetting may be instantaneous, definite time delayed, or, in the case of IEEE/US curves, inverse time delayed.

Instantaneous resetting is normally applied in multi-shot auto-reclosing schemes, to ensure correct grading between relays at various points in the scheme. On the other hand, the inverse reset characteristic is particularly useful to provide correct co-ordination with an upstream induction disc type overcurrent relay.

The definite time delayed reset characteristic may be used to provide faster clearance of intermittent ('pecking' or 'flashing') fault conditions. An example of where such phenomena may be experienced is in plastic insulated cables, where the fault energy melts the cable insulation and temporarily extinguishes the fault, after which the insulation again breaks down and the process repeats.

An inverse time overcurrent protection with instantaneous resetting cannot detect this condition until the fault becomes permanent, thereby allowing a succession of such breakdowns to occur, with associated damage to plant and danger to personnel. If a definite time reset delay of, for example, 60 seconds is applied, on the other hand, the inverse time element does not reset immediately after each successive fault occurrence. Instead, with each new fault inception, it continues to integrate from the point reached during the previous breakdown, and therefore operates before the condition becomes permanent. Figure A-1 illustrates this theory.

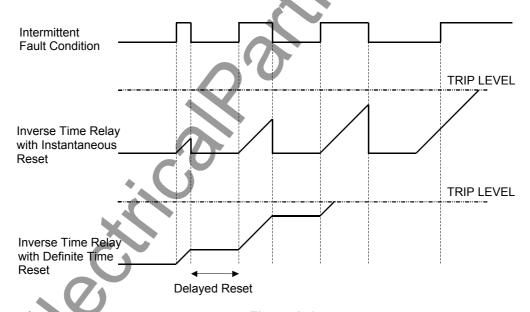


Figure A-1

TOSHIBA

Implementation of Thermal Model to IEC60255-8

Heating by overload current and cooling by dissipation of an electrical system follow exponential time constants. The thermal characteristics of the electrical system can be shown by equation (1).

$$\theta = \frac{I^2}{I_{AOL}^2} \left(1 - e^{-t/\tau} \right) \times 100\% \tag{1}$$

where:

 θ = thermal state of the system as a percentage of allowable thermal capacity

I = applied load current,

 I_{AOL} = allowable overload current of the system,

 τ = thermal time constant of the system.

The thermal state θ is expressed as a percentage of the thermal capacity of the protected system, where 0% represents the cold state and 100% represents the thermal limit, that is the point at which no further temperature rise can be safely tolerated and the system should be disconnected. The thermal limit for any given electrical plant is fixed by the thermal setting I_{AOL} . The relay gives a trip output when $\theta = 100\%$.

If current I is applied to a cold system, then θ will rise exponentially from 0% to ($I^2/I_{AOL}^2 \times 100\%$), with time constant τ , as in Figure A-2. If $\theta = 100\%$, then the allowable thermal capacity of the system has been reached.

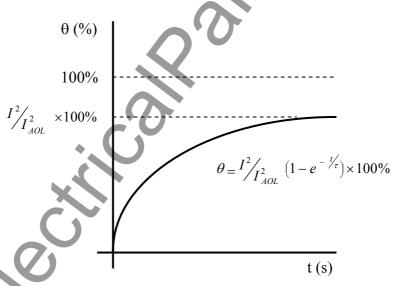


Figure A-2

A thermal overload protection relay can be designed to model this function, giving tripping times according to the IEC60255-8 'Hot' and 'Cold' curves.

$$t = \tau \cdot Ln \left[\frac{I^2}{I^2 - I_{AOL}^2} \right]$$
 (1) ····· Cold curve

$$t = \tau \cdot Ln \left[\frac{I^2 - I_p^2}{I^2 - I_{AOI}^2} \right]$$
 (2) ····· Hot curve

where:

 I_P = prior load current.

In fact, the cold curve is simply a special case of the hot curve where prior load current $I_P = 0$, catering for the situation where a cold system is switched on to an immediate overload.

Figure A-3 shows a typical thermal profile for a system which initially carries normal load current, and is then subjected to an overload condition until a trip results, before finally cooling to ambient temperature.

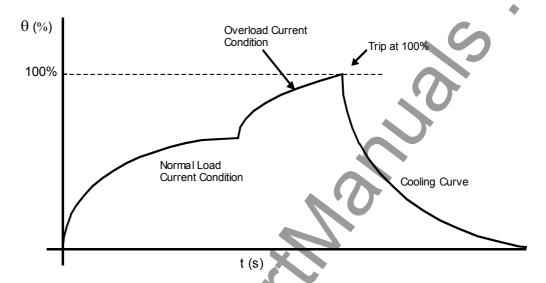


Figure A-3

Appendix B

Directional Earth Fault Protection and Power System Earthing

Directional Earth Fault Protection and Power System Earthing

Power systems may be solidly earthed, impedance earthed or unearthed (insulated). Depending on the method used, faults to earth have widely differing characteristics, and so methods of earth fault protection differ greatly between the various types of system.

1. Solidly earthed systems

In a solidly earthed system the neutral points of the power transformers are connected directly to earth, for the purposes of reducing overvoltages and facilitating fault detection. The disadvantage of solid earthing is that fault currents can be very high, and must be disconnected quickly.

Since the impedance of the source is normally very low, fault current varies greatly in magnitude depending on the location of the fault. Selective isolation of a faulty section is therefore possible via time/current graded earth fault overcurrent protection. Fault current is detected by measuring the system residual current.

On an interconnected system, where fault current can flow in either direction, then directional earth fault relays are applied. The fault causes a residual voltage to be generated, and this can be used for directional polarization. Residual current and voltage can be measured as shown in Figure B-1.

Residual current I_R is equal in magnitude and direction to the fault current. It typically lags the faulted phase voltage by a considerable angle due to the reactance of the source. Directional control is achieved by polarising against the system residual voltage, which may be found either by summating the phase voltages, or it may be extracted from the open delta connected secondary (or tertiary) winding of a five limb VT, as shown in the diagram.

A directional earth fault relay protecting a solidly earthed system is normally connected to measure V_R inverted. If GRD140 is applied to derive residual voltage from the phase voltages then the inversion of V_R is performed internally.

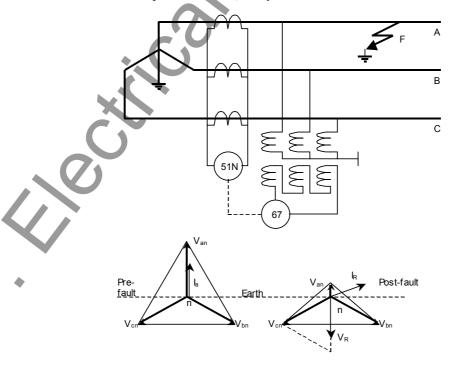


Figure B-1 Directional Earth Fault Protection for Solidly Earthed Systems

The relay characteristic angle setting is applied to compensate for lag of the fault current. Generally accepted angle settings are -45° for solidly earthed distribution systems and -60° for transmission systems.

Due to system imbalances and measuring tolerances, small levels of residual voltage can be present during normal operating conditions. Therefore, GRD140 provides a voltage threshold which must be exceeded before the directional protection will operate. Although this threshold is user programmable, most applications will be satisfied by the default setting of 3V.

2. Unearthed (insulated) systems

An insulated system has no intentional connection to earth, although all systems are in fact earthed by natural capacitive coupling. Fault current is very low, being made up of capacitive charging currents, thus limiting damage to plant. However, high steady-state and transient overvoltages are produced, and selective isolation of faults is difficult.

An earth fault on an ungrounded system causes a voltage shift between the neutral point and earth, and the fault can be detected by measuring this shift. So called neutral voltage displacement protection is commonly applied but, unfortunately, the shift in voltage is essentially the same throughout the system and so this method cannot selectively isolate a faulted section.

The method of directional earth fault protection described previously for solidly earthed systems cannot be used in the case of insulated systems because of the absence of real fault current. However, an alternative method can be applied, using GRD140 directional sensitive earth fault protection. The relay must be connected using a core balance CT, to measure the flow of capacitive charging currents, which become unbalanced in the event of a fault.

A phase to earth fault effectively short circuits that phase's capacitance to earth for the whole system, thus creating an unbalance in the charging currents for all feeders connected to the system. The resulting fault current is made up of the sum of the combined residual charging currents for both the faulty and healthy feeders.

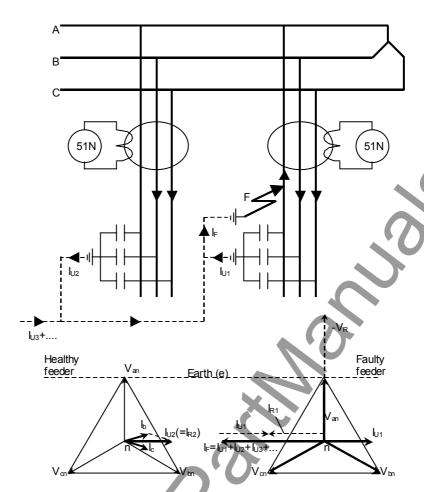


Figure B-2 Residual Current Flow in an Unearthed System

It can be shown that the residual current measured in the faulty feeder is 180° out of phase with that in the healthy feeder, as illustrated in Figure B-2 This fact can be used to apply a GRD140 directional sensitive earth fault relay. The polarising voltage used for directional earth fault relays is normally $-V_R$ (the residual voltage inverted), and it can be seen that the residual current (I_{R1}) for the faulty feeder leads this voltage by 90° . For the healthy feeders the residual current lags the voltage by 90° . Therefore, the GRD140 sensitive earth fault protection should be applied with a characteristic angle of $+90^{\circ}$ so as to provide discriminatory protection.

The residual current in the faulted phase is equal to three times the per phase charging current, and the sensitive earth fault element should be set well below this value to ensure operation (30% of this value is typical).

3. Impedance earthing

In between the two extremes of solidly earthed and unearthed systems there are a variety of compromise solutions, which normally involve connecting the system neutrals to earth via a resistance or reactance.

3a. Resistance earthing

In the case of resistance earthed systems, GRD140 directional earth fault relays can normally be applied in a similar manner to that for solidly earthed systems, with the exceptions that current settings will be lower and the characteristic angle setting will probably be different. In the event of a fault, it is the resistance in the neutral which predominates in the source impedance, and so the residual current lags its polarising voltage by a much smaller angle. Characteristic angle

settings of -15° or 0° are common.

3b. Reactance earthing

Reactance earthed systems are also common in many countries. A special case of this method is known as Petersen coil, or resonant, earthing. The inductance in the neutral is chosen to cancel the total capacitance of the system so that no current flows into an earth fault.

Directional sensitive earth fault protection can again be applied by detecting the unbalance in charging currents. It can be shown that the residual current distribution for healthy and faulty feeders is as illustrated in Figure B-3.

In the case of the healthy feeder, the residual current lags the polarising voltage (\sqrt{VR}) by more than 90°, while for the faulty feeder, the angle is less than 90°. GRD140 directional sensitive earth fault protection can be applied, with a 0° characteristic angle. Note that the SEF boundary of directional operation should be set to ± 90 °. The residual current for the healthy feeder then falls in the restraint zone, while for the faulty feeder it lies in the operate zone, thus providing selective isolation of the fault.

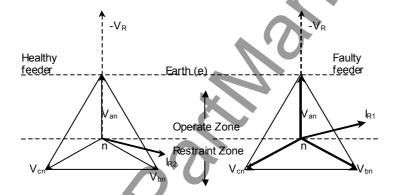


Figure B-3 Residual Current Flow in a Resonant Earthed System

3c. Reactance Earthing and Residual Power Control

GRD140 can provide an additional restraint on operation by the (optional) residual power control feature. The active component of residual power can be calculated as follows:

$$\Re(P_R) = I_R \times V_R \times \cos\phi$$

where ϕ is the phase angle between the residual current (I_R) and the polarising voltage (-V_R).

It is clear from Figure B-3 that this value will be positive when measured at the faulty feeder and negative anywhere else. GRD140 directional sensitive earth fault protection can be applied with a power threshold such that operation is permitted when residual power exceeds the setting and is in the operate direction.

Appendix C
Signal List

No.	Signal Name	Contents
0		Not in use
1	BI1 COMMAND	Binary input signal of BI1
2	BI2 COMMAND	Binary input signal of BI2
3	BI3 COMMAND	Binary input signal of BI3
4	BI4 COMMAND	Binary input signal of BI4
5	BI5 COMMAND	7
		Binary input signal of BI5
6	BI6 COMMAND	Binary input signal of BI6
7	BI7 COMMAND	Binary input signal of BI7
8	BI8 COMMAND	Binary input signal of BI8
9		
10		
11		
12		
13		
14		
15	1	
_		
16		
17		
18		
19		
20		
21	SET.GROUP1	BI command of change active setting group1
22	SET.GROUP2	BI command of change active setting group2
23	SET.GROUP3	BI command of change active setting group3
24	SET.GROUP4	BI command of change active setting group4
25	OC1 BLOCK	BI command of OC1 protection scheme block
		PLearmand of OC2 protection scheme black
26	OC2 BLOCK	BI command of OC2 protection scheme block
27	OC3 BLOCK	BI command of OC3 protection scheme block
28	OC4 BLOCK	BI command of OC4 protection scheme block
29	EF1 BLOCK	BI command of EF1 protection scheme block
30	EF2 BLOCK	BI command of EF2 protection scheme block
31	EF3 BLOCK	BI command of EF3 protection scheme block
32	EF4 BLOCK	BI command of EF4 protection scheme block
33	EF1 PERMIT	BI command of EF1 protection scheme permission
34	EF2 PERMIT	BI command of EF2 protection scheme permission
35	EF3 PERMIT	BI command of EF3 protection scheme permission
36	EF4 PERMIT	BI command of EF4 protection scheme permission
37	SEF1 BLOCK	BI command of SEF1 protection scheme block
38	SEF2 BLOCK	BI command of SEF2 protection scheme block
39	SEF3 BLOCK	BI command of SEF3 protection scheme block
40	SEF4 BLOCK	BI command of SEF4 protection scheme block
41	UC1 BLOCK	BI command of UC1 protection scheme block
42	UC2 BLOCK	BI command of UC2 protection scheme block
43	THM BLOCK	BI command of Thermal overload protection scheme block
44	THMA BLOCK	Bl command of Thermal overload processor scheme block
	NOC1 BLOCK	
45		BI command of NOC1 protection scheme block
46	NOC2 BLOCK	Bl command of NOC2 protection scheme block
47	BCD BLOCK	BI command of Broken Conductor protection scheme block
48	CBF BLOCK	BI command of CBF protection scheme block
49	OV1 BLOCK	BI command of OV1 protection scheme block
50	OV2 BLOCK	BI command of OV2 protection scheme block
51	UV1 BLOCK	BI command of UV1 protection scheme block
52	UV2 BLOCK	BI command of UV2 protection scheme block
53	ZOV1 BLOCK	BI command of ZOV1 protection scheme block
54	ZOVI BLOCK	BI command of ZOV1 protection scheme block
55	NOV1 BLOCK	BI command of NOV1 protection scheme block
56	NOV2 BLOCK	BI command of NOV2 protection scheme block
57	FRQ1 BLOCK	BI command of FRQ1 protection scheme block
58_	FRQ2 BLOCK	BI command of FRQ2 protection scheme block
59	FRQ3 BLOCK	BI command of FRQ3 protection scheme block
60	FRQ4 BLOCK	BI command of FRQ4 protection scheme block
61	ARC BLOCK	BI command of ARC scheme block
62	ARC READY	BI command of ARC ready
63	ARC INIT	BI command of ARC initiation
64	MANUAL CLOSE	BI command of Manual close
65	ARC N/A	BI command of ARC not applied
66	CTF BLOCK	BI command of CTF blocking
67	EXT CTF	BI command of External CTF
68	VTF BLOCK	BI command of VTF blocking
69	EXT VTF	BI command of External VTF
70	TC FAIL	BI command of Trip circuit Fail Alarm
71	CB CONT OPN	BI command of CB N/O contact
72	CB CONT CLS	BI command of CB N/C contact
		Di command of Evternal tria (2.25)
73	EXT TRIP-3PH	BI command of External trip (3 Phase)
74	EXT TRIP-APH	BI command of External trip (A Phase)
	EXT TRIP-BPH	BI command of External trip (B Phase)
75	EVE TOUR ARL	BI command of External trip (C Phase)
75 76	EXT TRIP-CPH	Di command di Externa tip (o i maco)
	REMOTE RESET	Bl command of Remote reset
76 77	REMOTE RESET	BI command of Remote reset
76		

No.	Signal Name	Contents
81	ALARM2	BI command of Alarm2
82	ALARM3	BI command of Alarm3
83	ALARM4	BI command of Alarm4
84	7 127 11 1177	ST COMMISSION OF THE STATE OF T
85	1	
86		
87		
88		
89		
90	1	
91	1	
92		
93		
94		
95		
96	1	
97	+	
98		
99		
100		
101	OC1-A	OC1-A relay element output
102	OC1-B	OC1-B relay element output
103	OC1-C	OC1-C relay element output
104	OC1-A INST	OC1-A relay element start
105	OC1-B INST	OC1-B relay element start
106	OC1-C INST	OC1-C relay element start
107	OC2-A	OC2-A relay element output
108	OC2-R	
		OC2-B relay element output
109	OC2-C	OC2-C relay element output
110		
111		
112		
113	OC3-A	OC3-A relay element output
114	OC3-B	OC3-B relay element output
115	OC3-C	OC3-C relay element output
116	OC4-A	OC4-A relay element output
117	OC4-B	OC4-B relay element output
118	OC4-C	OC4-C relay element output
119	OC1-A HS	High speed output of OC1-A relay
120	OC1-B HS	High speed output of OC1-B relay
121	OC1-C HS	High speed output of OC1-C relay
122	OC1 INST	OC1 relay element start (OR Logic of No. 104, 105 and 106)
123		
124		
125	1	
126		
127		
128		
128	. (
128 129 130	EF1	EF1 relay element output
128 129 130 131	EF1 FF1 INST	EF1 relay element output EF1 relay element start
128 129 130 131 132	EF1 INST	EF1 relay element start
128 129 130 131 132 133		
128 129 130 131 132 133 134	EF1 INST EF2	EF1 relay element start EF2 relay element output
128 129 130 131 132 133 134 135	EF1 INST EF2 EF3	EF1 relay element start EF2 relay element output EF3 relay element output
128 129 130 131 132 133 134	EF1 INST EF2 EF3 EF4	EF1 relay element start EF2 relay element output
128 129 130 131 132 133 134 135	EF1 INST EF2 EF3	EF1 relay element start EF2 relay element output EF3 relay element output
128 129 130 131 132 133 134 135 136	EF1 INST EF2 EF3 EF4 CUR-REV DET.	EF1 relay element start EF2 relay element output EF3 relay element output EF4 relay element output Current reversal detection.
128 129 130 131 132 133 134 135 136 137	EF1 INST EF2 EF3 EF4	EF1 relay element start EF2 relay element output EF3 relay element output EF4 relay element output
128 129 130 131 132 133 134 135 136 137 138	EF1 INST EF2 EF3 EF4 CUR-REV DET.	EF1 relay element start EF2 relay element output EF3 relay element output EF4 relay element output Current reversal detection.
128 129 130 131 132 133 134 135 136 137 138 139	EF1 INST EF2 EF3 EF4 CUR-REV DET. EF1 HS	EF1 relay element start EF2 relay element output EF3 relay element output EF4 relay element output Current reversal detection. High speed output of EF1 relay
128 129 130 131 132 133 134 135 136 137 138 139 140	EF1 INST EF2 EF3 EF4 CUR-REV DET. EF1 HS SEF1	EF1 relay element start EF2 relay element output EF3 relay element output EF4 relay element output Current reversal detection. High speed output of EF1 relay SEF1 relay element output
128 129 130 131 132 133 134 135 136 137 138 139 140	EF1 INST EF2 EF3 EF4 CUR-REV DET. EF1 HS SEF1 SEF1 INST	EF1 relay element start EF2 relay element output EF3 relay element output EF4 relay element output Current reversal detection. High speed output of EF1 relay SEF1 relay element output SEF1 relay element start
128 129 130 131 132 133 134 135 136 137 138 139 140 141 142	EF1 INST EF2 EF3 EF4 CUR-REV DET. EF1 HS SEF1	EF1 relay element start EF2 relay element output EF3 relay element output EF4 relay element output Current reversal detection. High speed output of EF1 relay SEF1 relay element output
128 129 130 131 132 133 134 135 136 137 138 139 140	EF1 INST EF2 EF3 EF4 CUR-REV DET. EF1 HS SEF1 SEF1 INST	EF1 relay element start EF2 relay element output EF3 relay element output EF4 relay element output Current reversal detection. High speed output of EF1 relay SEF1 relay element output SEF1 relay element start
128 129 130 131 132 133 134 135 136 137 138 139 140 141 142	EF1 INST EF2 EF3 EF4 CUR-REV DET. EF1 HS SEF1 SEF1 INST	EF1 relay element start EF2 relay element output EF3 relay element output EF4 relay element output Current reversal detection. High speed output of EF1 relay SEF1 relay element output SEF1 relay element start
128 129 130 131 132 133 134 135 136 137 138 139 140 141 142 143 144	EF1 INST EF2 EF3 EF4 CUR-REV DET. EF1 HS SEF1 SEF1 INST SEF2 SEF3	EF1 relay element start EF2 relay element output EF3 relay element output EF4 relay element output Current reversal detection. High speed output of EF1 relay SEF1 relay element output SEF1 relay element start SEF2 relay element output SEF3 relay element output
128 129 130 131 132 133 134 135 136 137 138 139 140 141 142 143 144 145	EF1 INST EF2 EF3 EF4 CUR-REV DET. EF1 HS SEF1 SEF1 INST SEF2 SEF3 SEF4	EF1 relay element start EF2 relay element output EF3 relay element output EF4 relay element output Current reversal detection. High speed output of EF1 relay SEF1 relay element output SEF1 relay element start SEF2 relay element output SEF3 relay element output SEF4 relay element output
128 129 130 131 132 133 134 135 136 137 138 140 141 142 143 144 145 146	EF1 INST EF2 EF3 EF4 CUR-REV DET. EF1 HS SEF1 SEF1 INST SEF2 SEF3 SEF4 SEF1 HS	EF1 relay element start EF2 relay element output EF3 relay element output EF4 relay element output Current reversal detection. High speed output of EF1 relay SEF1 relay element output SEF1 relay element start SEF2 relay element output SEF3 relay element output SEF4 relay element output SEF4 relay element output SEF5 relay element output SEF6 relay element output
128 129 130 131 132 133 134 135 136 137 138 139 140 141 142 143 144 145 146 147	EF1 INST EF2 EF3 EF4 CUR-REV DET. EF1 HS SEF1 SEF1 INST SEF2 SEF3 SEF4 SEF1 HS RPF	EF1 relay element start EF2 relay element output EF3 relay element output EF4 relay element output Current reversal detection. High speed output of EF1 relay SEF1 relay element output SEF1 relay element start SEF2 relay element output SEF3 relay element output SEF4 relay element output SEF4 relay element output SEF5 relay element output SEF6 relay element output SEF6 relay element output SEF7 relay element output SEF6 relay element output SEF6 relay element output SEF7 relay element output SEF6 relay element output SEF7 relay element output SEF7 relay element output SEF8 relay element output SEF9 relay element output SEF9 relay element output
128 129 130 131 132 133 134 135 136 137 138 140 141 142 143 144 145 146	EF1 INST EF2 EF3 EF4 CUR-REV DET. EF1 HS SEF1 SEF1 INST SEF2 SEF3 SEF4 SEF1 HS	EF1 relay element start EF2 relay element output EF3 relay element output EF4 relay element output Current reversal detection. High speed output of EF1 relay SEF1 relay element output SEF1 relay element start SEF2 relay element output SEF3 relay element output SEF4 relay element output SEF4 relay element output SEF5 relay element output SEF6 relay element output
128 129 130 131 132 133 134 135 136 137 138 139 140 141 142 143 144 145 146 147	EF1 INST EF2 EF3 EF4 CUR-REV DET. EF1 HS SEF1 SEF1 INST SEF2 SEF3 SEF4 SEF1 HS RPF	EF1 relay element start EF2 relay element output EF3 relay element output EF4 relay element output Current reversal detection. High speed output of EF1 relay SEF1 relay element output SEF1 relay element start SEF2 relay element output SEF3 relay element output SEF4 relay element output SEF4 relay element output SEF5 relay element output SEF6 relay element output SEF6 relay element output SEF7 relay element output SEF6 relay element output SEF6 relay element output SEF7 relay element output SEF6 relay element output SEF7 relay element output SEF7 relay element output SEF8 relay element output SEF9 relay element output SEF9 relay element output
128 129 130 131 132 133 134 135 136 137 138 139 140 141 142 143 144 145 146 147 148 149 150	EF1 INST EF2 EF3 EF4 CUR-REV DET. EF1 HS SEF1 SEF1 INST SEF2 SEF3 SEF4 SEF1 HS RPF	EF1 relay element start EF2 relay element output EF3 relay element output EF4 relay element output Current reversal detection. High speed output of EF1 relay SEF1 relay element output SEF1 relay element start SEF2 relay element output SEF3 relay element output SEF4 relay element output SEF4 relay element output SEF5 relay element output SEF6 relay element output SEF6 relay element output SEF7 relay element output SEF6 relay element output SEF6 relay element output SEF7 relay element output SEF6 relay element output SEF7 relay element output SEF7 relay element output SEF8 relay element output SEF9 relay element output SEF9 relay element output
128 129 130 131 132 133 134 135 136 137 138 139 140 141 142 143 144 145 146 147 148 149 150	EF1 INST EF2 EF3 EF4 CUR-REV DET. EF1 HS SEF1 SEF1 INST SEF2 SEF3 SEF4 SEF1 HS RPF	EF1 relay element start EF2 relay element output EF3 relay element output EF4 relay element output Current reversal detection. High speed output of EF1 relay SEF1 relay element output SEF1 relay element start SEF2 relay element output SEF3 relay element output SEF4 relay element output SEF4 relay element output SEF5 relay element output SEF6 relay element output SEF6 relay element output SEF7 relay element output SEF6 relay element output SEF6 relay element output SEF7 relay element output SEF6 relay element output SEF7 relay element output SEF7 relay element output SEF8 relay element output SEF9 relay element output SEF9 relay element output
128 129 130 131 132 133 134 135 136 137 138 139 140 141 142 143 144 145 146 147 148 149 150 151	EF1 INST EF2 EF3 EF4 CUR-REV DET. EF1 HS SEF1 SEF1 INST SEF2 SEF3 SEF4 SEF1 HS RPF	EF1 relay element start EF2 relay element output EF3 relay element output EF4 relay element output Current reversal detection. High speed output of EF1 relay SEF1 relay element output SEF1 relay element start SEF2 relay element output SEF3 relay element output SEF4 relay element output SEF4 relay element output SEF5 relay element output SEF6 relay element output SEF6 relay element output SEF7 relay element output SEF6 relay element output SEF6 relay element output SEF7 relay element output SEF6 relay element output SEF7 relay element output SEF7 relay element output SEF8 relay element output SEF9 relay element output SEF9 relay element output
128 129 130 131 132 133 134 135 136 137 138 140 141 142 143 144 145 146 147 148 149 150 151 152 153	EF1 INST EF2 EF3 EF4 CUR-REV DET. EF1 HS SEF1 SEF1 INST SEF2 SEF3 SEF4 SEF1 HS RPF	EF1 relay element start EF2 relay element output EF3 relay element output EF4 relay element output Current reversal detection. High speed output of EF1 relay SEF1 relay element output SEF1 relay element start SEF2 relay element output SEF3 relay element output SEF4 relay element output SEF4 relay element output SEF5 relay element output SEF6 relay element output SEF6 relay element output SEF7 relay element output SEF6 relay element output SEF6 relay element output SEF7 relay element output SEF6 relay element output SEF7 relay element output SEF7 relay element output SEF8 relay element output SEF9 relay element output SEF9 relay element output
128 129 130 131 132 133 134 135 136 137 138 139 140 141 142 143 144 145 146 147 148 149 150 151	EF1 INST EF2 EF3 EF4 CUR-REV DET. EF1 HS SEF1 SEF1 INST SEF2 SEF3 SEF4 SEF1 HS RPF	EF1 relay element start EF2 relay element output EF3 relay element output EF4 relay element output Current reversal detection. High speed output of EF1 relay SEF1 relay element output SEF1 relay element start SEF2 relay element output SEF3 relay element output SEF4 relay element output SEF4 relay element output SEF5 relay element output SEF6 relay element output SEF6 relay element output SEF7 relay element output SEF6 relay element output SEF6 relay element output SEF7 relay element output SEF6 relay element output SEF7 relay element output SEF7 relay element output SEF8 relay element output SEF9 relay element output SEF9 relay element output
128 129 130 131 132 133 134 135 136 137 138 140 141 142 143 144 145 146 147 148 149 150 151 152 153	EF1 INST EF2 EF3 EF4 CUR-REV DET. EF1 HS SEF1 SEF1 INST SEF2 SEF3 SEF4 SEF1 HS RPF	EF1 relay element start EF2 relay element output EF3 relay element output EF4 relay element output Current reversal detection. High speed output of EF1 relay SEF1 relay element output SEF1 relay element start SEF2 relay element output SEF3 relay element output SEF4 relay element output SEF4 relay element output SEF5 relay element output SEF6 relay element output SEF6 relay element output SEF7 relay element output SEF6 relay element output SEF6 relay element output SEF7 relay element output SEF6 relay element output SEF7 relay element output SEF7 relay element output SEF8 relay element output SEF9 relay element output SEF9 relay element output
128 129 130 131 132 133 134 135 136 137 138 139 140 141 142 143 144 145 146 147 148 149 150 151 152 153 154 155	EF1 INST EF2 EF3 EF4 CUR-REV DET. EF1 HS SEF1 SEF1 INST SEF2 SEF3 SEF4 SEF1 HS RPF	EF1 relay element start EF2 relay element output EF3 relay element output EF4 relay element output Current reversal detection. High speed output of EF1 relay SEF1 relay element output SEF1 relay element start SEF2 relay element output SEF3 relay element output SEF4 relay element output SEF4 relay element output SEF5 relay element output SEF6 relay element output SEF6 relay element output SEF7 relay element output SEF6 relay element output SEF6 relay element output SEF7 relay element output SEF6 relay element output SEF7 relay element output SEF7 relay element output SEF8 relay element output SEF9 relay element output SEF9 relay element output
128 129 130 131 132 133 134 135 136 137 138 139 140 141 142 143 144 145 146 147 149 150 151 151 152 154 155 156	EF1 INST EF2 EF3 EF4 CUR-REV DET. EF1 HS SEF1 SEF1 INST SEF2 SEF3 SEF4 SEF1 HS RPF	EF1 relay element start EF2 relay element output EF3 relay element output EF4 relay element output Current reversal detection. High speed output of EF1 relay SEF1 relay element output SEF1 relay element start SEF2 relay element output SEF3 relay element output SEF4 relay element output SEF4 relay element output SEF5 relay element output SEF6 relay element output SEF6 relay element output SEF7 relay element output SEF6 relay element output SEF6 relay element output SEF7 relay element output SEF6 relay element output SEF7 relay element output SEF7 relay element output SEF8 relay element output SEF9 relay element output SEF9 relay element output
128 129 130 131 132 133 134 135 136 137 138 139 140 141 142 143 144 145 146 147 148 149 150 151 152 153 155 156 157	EF1 INST EF2 EF3 EF4 CUR-REV DET. EF1 HS SEF1 SEF1 INST SEF2 SEF3 SEF4 SEF1 HS RPF	EF1 relay element start EF2 relay element output EF3 relay element output EF4 relay element output Current reversal detection. High speed output of EF1 relay SEF1 relay element output SEF1 relay element start SEF2 relay element output SEF3 relay element output SEF4 relay element output SEF4 relay element output SEF5 relay element output SEF6 relay element output SEF6 relay element output SEF7 relay element output SEF6 relay element output SEF6 relay element output SEF7 relay element output SEF6 relay element output SEF7 relay element output SEF7 relay element output SEF8 relay element output SEF9 relay element output SEF9 relay element output
128 129 130 131 132 133 134 135 136 137 138 139 140 141 142 143 144 145 146 147 148 149 150 151 152 153 154 156 157 158	EF1 INST EF2 EF3 EF4 CUR-REV DET. EF1 HS SEF1 SEF1 INST SEF2 SEF3 SEF4 SEF1 HS RPF	EF1 relay element start EF2 relay element output EF3 relay element output EF4 relay element output Current reversal detection. High speed output of EF1 relay SEF1 relay element output SEF1 relay element start SEF2 relay element output SEF3 relay element output SEF4 relay element output SEF4 relay element output SEF5 relay element output SEF6 relay element output SEF6 relay element output SEF7 relay element output SEF6 relay element output SEF6 relay element output SEF7 relay element output SEF6 relay element output SEF7 relay element output SEF7 relay element output SEF8 relay element output SEF9 relay element output SEF9 relay element output
128 129 130 131 132 133 134 135 136 137 138 140 141 142 143 144 145 146 147 148 149 150 151 152 153 154 155 156 157 158	EF1 INST EF2 EF3 EF4 CUR-REV DET. EF1 HS SEF1 SEF1 INST SEF2 SEF3 SEF4 SEF1 HS RPF	EF1 relay element start EF2 relay element output EF3 relay element output EF4 relay element output Current reversal detection. High speed output of EF1 relay SEF1 relay element output SEF1 relay element start SEF2 relay element output SEF3 relay element output SEF4 relay element output SEF4 relay element output SEF5 relay element output SEF6 relay element output SEF6 relay element output SEF7 relay element output SEF6 relay element output SEF6 relay element output SEF7 relay element output SEF6 relay element output SEF7 relay element output SEF7 relay element output SEF8 relay element output SEF9 relay element output SEF9 relay element output
128 129 130 131 132 133 134 135 136 137 138 139 140 141 142 143 144 145 146 147 148 149 150 151 152 153 154 156 157 158	EF1 INST EF2 EF3 EF4 CUR-REV DET. EF1 HS SEF1 SEF1 INST SEF2 SEF3 SEF4 SEF1 HS RPF	EF1 relay element start EF2 relay element output EF3 relay element output EF4 relay element output Current reversal detection. High speed output of EF1 relay SEF1 relay element output SEF1 relay element start SEF2 relay element output SEF3 relay element output SEF4 relay element output SEF4 relay element output SEF5 relay element output SEF6 relay element output SEF6 relay element output SEF7 relay element output SEF6 relay element output SEF6 relay element output SEF7 relay element output SEF6 relay element output SEF7 relay element output SEF7 relay element output SEF8 relay element output SEF9 relay element output SEF9 relay element output

No.	Cignal Nama	Contents
161	Signal Name	
161	UC1-A	UC1-A relay element output
162	UC1-B	UC1-B relay element output
163	UC1-C	UC1-C relay element output
164	UC2-A	UC2-A relay element output
165	UC2-B	UC2-B relay element output
166	UC2-C	UC2-C relay element output
167	THM-A	THERMAL Alarm relay element output
168	THM-T	THERMAL Trip relay element output
169	NOC1	NOC1 relay element output
170		1100 110ta) cionioni dalpai
171	NOC2	NOC2 relay element output
172	BCD	
		BCD relay element output
173	CBF-A	CBF-A relay element output
174	CBF-B	CBF-B relay element output
175	CBF-C	CBF-C relay element output
176	ICLDO-A	ICLDO-A relay (OC relay) element output used in "CLP scheme"
177	ICLDO-B	ICLDO-B relay (OC relay) element output used in "CLP scheme"
178	ICLDO-C	ICLDO-C relay (OC relay) element output used in "CLP scheme"
179	OC-A DIST	OC-A relay for disturbance record
180	OC-B DIST	OC-B relay for disturbance record
181		
_	OC-C DIST	OC-C relay for disturbance record
182	EF DIST	EF relay for disturbance record
183	SEF DIST	SEF relayfor disturbance record
184	NOC DIST	NOC relay for disturbance record
185		4
186		
187	1	
188	<u> </u>	
		<u> </u>
189	ļ	
190	0)/4 4	0/4/10/10/10/10/10/10
191	OV1-A	OV1-1 relay element output
192	OV1-B	OV1-2 relay element output
193	OV1-C	OV1-3 relay element output
194	OV1-A INST	OV1-1 relay element start
195	OV1-B INST	OV1-2 relay element start
196	OV1-C INST	OV1-3 relay element start
197	OV2-A	·
		OV2-1 relay element output
198	OV2-B	OV2-2 relay element output
199	OV2-C	OV2-3 relay element output
200		
201	UV1-A	UV1-1 relay element output
202	UV1-B	UV1-2 relay element output
203	UV1-C	UV1-3 relay element output
204	UV1-A INST	UV1-1 relay element start
205	UV1-B INST	UV1-2 relay element start
206	UV1-C INST	
		UV1-3 relay element start
207	UV2-A	UV2-1 relay element output
208	UV2-B	UV2-2 relay element output
209	UV2-C	UV2-3 relay element output
210	• .	
211	ZOV1	ZOV1 relay element ouput
212	ZOV1 INST	ZOV1 relay element start
213	70\/2	7OV2 relay element quout
213	ZOV2	ZOV2 relay element ouput
214	NOV1	NOV1 relay element ouput
214 215	NOV1 NOV1 INST	NOV1 relay element ouput NOV1 relay element start
214 215 216	NOV1 NOV1 INST NOV2	NOV1 relay element ouput NOV1 relay element start NOV2 relay element ouput
214 215 216 217	NOV1 NOV1-INST NOV2 UVBLK	NOV1 relay element ouput NOV1 relay element start NOV2 relay element ouput UV blocked element operating
214 215 216 217	NOV1 NOV1 INST NOV2	NOV1 relay element ouput NOV1 relay element start NOV2 relay element ouput
214 215 216 217 218	NOV1 NOV1-INST NOV2 UVBLK	NOV1 relay element ouput NOV1 relay element start NOV2 relay element ouput UV blocked element operating
214 215 216 217 218 219	NOV1 NOV1 INST NOV2 UVBLK FRQ1	NOV1 relay element ouput NOV1 relay element start NOV2 relay element ouput UV blocked element operating FRQ1 relay element ouput FRQ2 relay element ouput
214 215 216 217 218 219 220	NOV1 NOV1 INST NOV2 UVBLK FRQ1 FRQ2 FRQ3	NOV1 relay element ouput NOV1 relay element start NOV2 relay element ouput UV blocked element operating FRQ1 relay element ouput FRQ2 relay element ouput FRQ3 relay element ouput
214 215 216 217 218 219 220 221	NOV1 NOV1-INST NOV2 UVBLK FRQ1 FRQ2 FRQ3 FRQ4	NOV1 relay element ouput NOV1 relay element start NOV2 relay element ouput UV blocked element operating FRQ1 relay element ouput FRQ2 relay element ouput FRQ3 relay element ouput FRQ3 relay element ouput FRQ4 relay element ouput
214 215 216 217 218 219 220 221 222	NOV1 NOV1 INST NOV2 UVBLK FRQ1 FRQ2 FRQ3	NOV1 relay element ouput NOV1 relay element start NOV2 relay element ouput UV blocked element operating FRQ1 relay element ouput FRQ2 relay element ouput FRQ3 relay element ouput
214 215 216 217 218 219 220 221 222 223	NOV1 NOV1-INST NOV2 UVBLK FRQ1 FRQ2 FRQ3 FRQ4	NOV1 relay element ouput NOV1 relay element start NOV2 relay element ouput UV blocked element operating FRQ1 relay element ouput FRQ2 relay element ouput FRQ3 relay element ouput FRQ3 relay element ouput FRQ4 relay element ouput
214 215 216 217 218 219 220 221 222 223 224	NOV1 NOV1-INST NOV2 UVBLK FRQ1 FRQ2 FRQ3 FRQ4	NOV1 relay element ouput NOV1 relay element start NOV2 relay element ouput UV blocked element operating FRQ1 relay element ouput FRQ2 relay element ouput FRQ3 relay element ouput FRQ3 relay element ouput FRQ4 relay element ouput
214 215 216 217 218 219 220 221 222 223	NOV1 NOV1-INST NOV2 UVBLK FRQ1 FRQ2 FRQ3 FRQ4	NOV1 relay element ouput NOV1 relay element start NOV2 relay element ouput UV blocked element operating FRQ1 relay element ouput FRQ2 relay element ouput FRQ3 relay element ouput FRQ3 relay element ouput FRQ4 relay element ouput
214 215 216 217 218 219 220 221 222 223 224	NOV1 NOV1-INST NOV2 UVBLK FRQ1 FRQ2 FRQ3 FRQ4	NOV1 relay element ouput NOV1 relay element start NOV2 relay element ouput UV blocked element operating FRQ1 relay element ouput FRQ2 relay element ouput FRQ3 relay element ouput FRQ3 relay element ouput FRQ4 relay element ouput
214 215 216 217 218 219 220 221 222 223 224 225	NOV1 NOV1-INST NOV2 UVBLK FRQ1 FRQ2 FRQ3 FRQ4	NOV1 relay element ouput NOV1 relay element start NOV2 relay element ouput UV blocked element operating FRQ1 relay element ouput FRQ2 relay element ouput FRQ3 relay element ouput FRQ3 relay element ouput FRQ4 relay element ouput
214 215 216 217 218 219 220 221 222 223 224 225 226 227	NOV1 NOV1-INST NOV2 UVBLK FRQ1 FRQ2 FRQ3 FRQ4	NOV1 relay element ouput NOV1 relay element start NOV2 relay element ouput UV blocked element operating FRQ1 relay element ouput FRQ2 relay element ouput FRQ3 relay element ouput FRQ3 relay element ouput FRQ4 relay element ouput
214 215 216 217 218 219 220 221 222 223 224 225 226 227 228	NOV1 NOV1-INST NOV2 UVBLK FRQ1 FRQ2 FRQ3 FRQ4	NOV1 relay element ouput NOV1 relay element start NOV2 relay element ouput UV blocked element operating FRQ1 relay element ouput FRQ2 relay element ouput FRQ3 relay element ouput FRQ3 relay element ouput FRQ4 relay element ouput
214 215 216 217 218 219 220 221 222 223 224 225 226 227 228 229	NOV1 NOV1-INST NOV2 UVBLK FRQ1 FRQ2 FRQ3 FRQ4	NOV1 relay element ouput NOV1 relay element start NOV2 relay element ouput UV blocked element operating FRQ1 relay element ouput FRQ2 relay element ouput FRQ3 relay element ouput FRQ3 relay element ouput FRQ4 relay element ouput
214 215 216 217 218 219 220 221 222 223 224 225 226 227 228 229 230	NOV1 NOV1-INST NOV2 UVBLK FRQ1 FRQ2 FRQ3 FRQ4 FRQBLK	NOV1 relay element ouput NOV1 relay element start NOV2 relay element ouput UV blocked element operating FRQ1 relay element ouput FRQ2 relay element ouput FRQ3 relay element ouput FRQ4 relay element ouput FRQ4 relay element ouput FRQ4 relay element ouput
214 215 216 217 218 219 220 221 222 223 224 225 226 227 228 229 230 231	NOV1 NOV1 INST NOV2 UVBLK FRQ1 FRQ2 FRQ3 FRQ4 FRQBLK	NOV1 relay element ouput NOV1 relay element start NOV2 relay element ouput UV blocked element operating FRQ1 relay element ouput FRQ2 relay element ouput FRQ3 relay element ouput FRQ4 relay element ouput FRQ4 relay element ouput FRQ blocked element operating
214 215 216 217 218 219 220 221 222 223 224 225 226 227 228 229 230	NOV1 NOV1-INST NOV2 UVBLK FRQ1 FRQ2 FRQ3 FRQ4 FRQBLK	NOV1 relay element ouput NOV1 relay element start NOV2 relay element ouput UV blocked element operating FRQ1 relay element ouput FRQ2 relay element ouput FRQ3 relay element ouput FRQ4 relay element ouput FRQ4 relay element ouput FRQ4 relay element ouput
214 215 216 217 218 219 220 221 222 223 224 225 226 227 228 229 230 231	NOV1 NOV1 INST NOV2 UVBLK FRQ1 FRQ2 FRQ3 FRQ4 FRQBLK	NOV1 relay element ouput NOV1 relay element start NOV2 relay element ouput UV blocked element operating FRQ1 relay element ouput FRQ2 relay element ouput FRQ3 relay element ouput FRQ4 relay element ouput FRQ4 relay element ouput FRQ blocked element operating
214 215 216 217 218 219 220 221 222 223 224 225 226 227 228 229 230 231 232	NOV1 NOV1 INST NOV2 UVBLK FRQ1 FRQ2 FRQ3 FRQ4 FRQBLK	NOV1 relay element ouput NOV1 relay element start NOV2 relay element ouput UV blocked element ouput FRQ1 relay element ouput FRQ3 relay element ouput FRQ4 relay element ouput FRQ4 relay element ouput FRQ blocked element ouput FRQ blocked element operating EF element for CTF detection ZOV element for CTF detection UV-A element for VTF detection
214 215 216 217 218 220 221 222 223 224 225 226 227 228 229 230 231 232 233 234	NOV1 NOV1-INST NOV2 UVBLK FRQ1 FRQ2 FRQ3 FRQ4 FRQBLK FRQBLK FRQBLK UVVF-A	NOV1 relay element ouput NOV1 relay element start NOV2 relay element ouput UV blocked element ouput FRQ1 relay element ouput FRQ2 relay element ouput FRQ3 relay element ouput FRQ4 relay element ouput FRQ4 relay element ouput FRQ blocked element operating EF element for CTF detection ZOV element for VTF detection UV-A element for VTF detection UV-B element for VTF detection
214 215 216 217 218 220 221 222 223 224 225 226 227 228 229 230 231 232 233 234 235	NOV1 NOV1-INST NOV2 UVBLK FRQ1 FRQ2 FRQ3 FRQ4 FRQBLK FRQBLK FRQBLK UVVF-A UVVF-A UVVF-B	NOV1 relay element ouput NOV1 relay element start NOV2 relay element ouput UV blocked element operating FRQ1 relay element ouput FRQ3 relay element ouput FRQ4 relay element ouput FRQ6 blocked element ouput FRQ6 blocked element operating EF element for CTF detection UV-A element for VTF detection UV-B element for VTF detection UV-C element for VTF detection UV-C element for VTF detection
214 215 216 217 218 220 221 222 223 224 225 226 227 228 229 230 231 232 233 234 235 236	NOV1 NOV1-INST NOV2 UVBLK FRQ1 FRQ2 FRQ3 FRQ4 FRQBLK FRQBLK EFCF ZOVCF UVVF-A UVVF-B UVVF-C UVVF-OR	NOV1 relay element ouput NOV1 relay element start NOV2 relay element ouput UV blocked element operating FRQ1 relay element ouput FRQ2 relay element ouput FRQ3 relay element ouput FRQ4 relay element ouput FRQ blocked element ouput FRQ blocked element operating EF element for CTF detection ZOV element for VTF detection UV-A element for VTF detection UV-C element for VTF detection UV-OR element for VTF detection
214 215 216 217 218 220 221 222 223 224 225 226 227 228 229 230 231 232 233 234 235 235 236 237	NOV1 NOV1 INST NOV2 UVBLK FRQ1 FRQ2 FRQ3 FRQ4 FRQBLK EFCF ZOVCF UVVF-A UVVF-B UVVF-C UVVF-C UVVF-OR OCDVF-A	NOV1 relay element ouput NOV1 relay element start NOV2 relay element ouput UV blocked element operating FRQ1 relay element ouput FRQ2 relay element ouput FRQ3 relay element ouput FRQ4 relay element ouput FRQ4 relay element ouput FRQ blocked element operating EF element for CTF detection ZOV element for CTF detection UV-A element for VTF detection UV-C element for VTF detection UV-C element for VTF detection UV-OR element for VTF detection UV-OR element for VTF detection OCD-A element for VTF detection
214 215 216 217 218 220 221 222 223 224 225 226 227 228 229 230 231 232 233 234 235 236 237 238	NOV1 NOV1 INST NOV2 UVBLK FRQ1 FRQ2 FRQ3 FRQ4 FRQBLK EFCF ZOVCF UVVF-A UVVF-B UVVF-C UVVF-OR OCDVF-A OCDVF-B	NOV1 relay element ouput NOV1 relay element start NOV2 relay element ouput UV blocked element ouput FRQ1 relay element ouput FRQ2 relay element ouput FRQ3 relay element ouput FRQ4 relay element ouput FRQ6 relay element ouput FRQ6 relay element ouput FRQ7 relay element ouput FRQ7 relay element ouput FRQ9 relay element for CTF detection UV-A element for VTF detection UV-OR element for VTF detection OCD-A element for VTF detection OCD-B element for VTF detection
214 215 216 217 218 220 221 222 223 224 225 226 227 228 229 230 231 232 233 234 235 237 238 239	NOV1 NOV1 INST NOV2 UVBLK FRQ1 FRQ2 FRQ3 FRQ4 FRQBLK EFCF ZOVCF UVVF-A UVVF-B UVVF-C UVVF-OR OCDVF-A OCDVF-B OCDVF-B	NOV1 relay element ouput NOV1 relay element start NOV2 relay element ouput UV blocked element operating FRQ1 relay element ouput FRQ2 relay element ouput FRQ3 relay element ouput FRQ4 relay element ouput FRQ6 relay element ouput FRQ6 relay element ouput FRQ7 relay element ouput FRQ7 relay element ouput FRQ9 relay element for CTF detection UV-A element for VTF detection UV-C element for VTF detection UV-OR element for VTF detection OCD-A element for VTF detection OCD-B element for VTF detection OCD-C element for VTF detection
214 215 216 217 218 220 221 222 223 224 225 226 227 228 229 230 231 232 233 234 235 236 237 238	NOV1 NOV1 INST NOV2 UVBLK FRQ1 FRQ2 FRQ3 FRQ4 FRQBLK EFCF ZOVCF UVVF-A UVVF-B UVVF-C UVVF-OR OCDVF-A OCDVF-B	NOV1 relay element ouput NOV1 relay element start NOV2 relay element ouput UV blocked element operating FRQ1 relay element ouput FRQ2 relay element ouput FRQ3 relay element ouput FRQ4 relay element ouput FRQ6 blocked element operating EF element for CTF detection UV-A element for VTF detection UV-B element for VTF detection UV-C element for VTF detection UV-OR element for VTF detection UV-OR element for VTF detection OCD-A element for VTF detection OCD-B element for VTF detection

241	Signal Name	Contents
	ZOVVF	ZOV element for VTF detection
242	EFVF	EF element for VTF detection
243	OC COORD-A	OC-A coordination element
244	OC COORD-B	OC-B coordination element
	OC COORD-C	OC-C coordination element
246	EF COORD	EF coordination element
	SEF COORD	SEF coordination element
	ZOV DIST	ZOV relay for disturbance record
249	NOV DIST	NOV relay for disturbance record
	OV-A DIST	OV-A relay for disturbance record
	OV-B DIST	OV-B relay for disturbance record
	OV-C DIST	OV-C relay for disturbance record
	UV-A DIST	UV-A relay for disturbance record
	UV-B DIST	UV-B relay for disturbance record
	UV-C DIST	UV-C relay for disturbance record
256	0 0 0 0 10 1	(NOT USED, reserved for disturbance record)
257		(ITO T GGEB; TGGGTTGG TGT GIGGTBGTTGGTG)
258		
259		
260		
	OC4 TRIR	OC1 trip command
	OC1 TRIP OC1-A TRIP	OC1 trip command OC1 trip command (A Phase)
	OC1-A TRIP	OC1 trip command (A Phase) OC1 trip command (B Phase)
	OC1-B TRIP	
		OC1 trip command (C Phase)
	OC2 TRIP	OC2 trip command (A Phase)
	OC2-A TRIP	OC2 trip command (A Phase)
	OC2-B TRIP	OC2 trip command (B Phase)
	OC2-C TRIP	OC2 trip command (C Phase)
	OC3 TRIP	OC3 trip command
	OC3-A TRIP	OC3 trip command (A Phase)
	OC3-B TRIP	OC3 trip command (B Phase)
	OC3-C TRIP	OC3 trip command (C Phase)
	OC4 ALARM	OC4 alarm command
	OC4-A ALARM	OC4 alarm command (A Phase)
	OC4-B ALARM	OC4 alarm command (B Phase)
	OC4-C ALARM	OC4 alarm command (C Phase)
277		
278		
279		
280		
281	EF1 TRIP	EF1 trip command
	EF2 TRIP	EF2 trip command
	EF3 TRIP	EF3 trip command
284	EF4 ALARM	EF4 alarm command
285	EF1 CARRIER	EF1 carrier command
286	EF2 CARRIER	EF2 carrier command
287	EF3 CARRIER	EF3 carrier command
288	EF4 CARRIER	EF4 carrier command
289		
290		
291	SEF1-S1 TRIP	SEF1 Stage1 trip command
	SEF1-S2 TRIP	SEF1 Stage2 trip command
000	SEF2 TRIP	SEF2 trip command
293		
	SEF3 TRIP	SEF3 trip command
294	SEF3 TRIP SEF4 ALARM	
294		SEF3 trip command
294 295		SEF3 trip command
294 295 296		SEF3 trip command
294 295 296 297		SEF3 trip command
294 295 296 297 298 299	SEF4 ALARM	SEF3 trip command
294 295 296 297 298 299 300		SEF3 trip command
294 295 296 297 298 299 300 301	SEF4 ALARM	SEF3 trip command SEF4 alarm command UC1 trip command
294 295 296 297 298 299 300 301 302	SEF4 ALARM UC1 TRIP	SEF3 trip command SEF4 alarm command
294 295 296 297 298 299 300 301 302 303	UC1 TRIP UC1-A TRIP UC1-B TRIP	SEF3 trip command SEF4 alarm command UC1 trip command UC1 trip command (A Phase) UC1 trip command (B Phase)
294 295 296 297 298 299 300 301 302 303 304	UC1 TRIP UC1-A TRIP UC1-B TRIP UC1-C TRIP	SEF3 trip command SEF4 alarm command UC1 trip command UC1 trip command (A Phase) UC1 trip command (B Phase) UC1 trip command (C Phase)
294 295 296 297 298 299 300 301 302 303 304 305	UC1 TRIP UC1-A TRIP UC1-B TRIP UC1-C TRIP UC2 ALARM	SEF3 trip command SEF4 alarm command UC1 trip command UC1 trip command (A Phase) UC1 trip command (B Phase) UC1 trip command (C Phase) UC2 alarm command
294 295 296 297 298 299 300 301 302 303 304 305 306	UC1 TRIP UC1-A TRIP UC1-B TRIP UC1-C TRIP UC2 ALARM UC2-A ALARM	SEF3 trip command SEF4 alarm command UC1 trip command UC1 trip command (A Phase) UC1 trip command (B Phase) UC1 trip command (C Phase) UC2 alarm command UC2 alarm command UC2 alarm command
294 295 296 297 298 299 300 301 302 303 304 305 306 307	UC1 TRIP UC1-A TRIP UC1-B TRIP UC1-C TRIP UC2 ALARM UC2-A ALARM UC2-B ALARM	SEF3 trip command SEF4 alarm command UC1 trip command UC1 trip command (A Phase) UC1 trip command (B Phase) UC1 trip command (C Phase) UC2 alarm command UC2 alarm command UC2 alarm command (A Phase) UC2 alarm command (B Phase)
294 295 296 297 298 299 300 301 302 303 304 305 306 307 308	UC1 TRIP UC1-A TRIP UC1-B TRIP UC1-C TRIP UC2 ALARM UC2-A ALARM UC2-B ALARM UC2-B ALARM UC2-C ALARM	SEF3 trip command SEF4 alarm command UC1 trip command UC1 trip command (A Phase) UC1 trip command (B Phase) UC1 trip command (C Phase) UC2 alarm command UC2 alarm command UC2 alarm command (A Phase) UC2 alarm command (A Phase) UC2 alarm command (C Phase) UC2 alarm command (C Phase)
294 295 296 297 298 299 300 301 302 303 304 305 306 307 308 309	UC1 TRIP UC1-A TRIP UC1-B TRIP UC1-C TRIP UC2 ALARM UC2-A ALARM UC2-B ALARM UC2-C ALARM THM ALARM	SEF3 trip command SEF4 alarm command UC1 trip command UC1 trip command (A Phase) UC1 trip command (B Phase) UC1 trip command (C Phase) UC2 alarm command UC2 alarm command UC2 alarm command (A Phase) UC2 alarm command (B Phase) UC2 alarm command (C Phase) Thermal alarm command
294 295 296 297 298 299 300 301 302 303 304 305 306 307 308 309 310	UC1 TRIP UC1-A TRIP UC1-B TRIP UC1-C TRIP UC2-A ALARM UC2-B ALARM UC2-B ALARM UC2-C ALARM THM ALARM THM TRIP	SEF3 trip command SEF4 alarm command UC1 trip command UC1 trip command UC1 trip command (A Phase) UC1 trip command (B Phase) UC1 trip command (C Phase) UC2 alarm command UC2 alarm command (A Phase) UC2 alarm command (B Phase) UC2 alarm command (B Phase) UC2 alarm command (B Phase) UC2 alarm command (C Phase) Thermal alarm command Thermal trip command
294 295 296 297 298 299 300 301 302 303 304 305 306 307 308 309 310 311	UC1 TRIP UC1-A TRIP UC1-B TRIP UC1-C TRIP UC2 ALARM UC2-A ALARM UC2-B ALARM UC2-C ALARM THM ALARM THM TRIP NOC1 TRIP	SEF3 trip command SEF4 alarm command UC1 trip command UC1 trip command (A Phase) UC1 trip command (B Phase) UC1 trip command (C Phase) UC2 alarm command (C Phase) UC2 alarm command (C Phase) UC2 alarm command (B Phase) UC2 alarm command (B Phase) UC2 alarm command (B Phase) UC2 alarm command (C Phase) Thermal alarm command Thermal trip command NOC1 trip command
294 295 296 297 298 300 301 302 303 304 306 307 308 309 311 311 312	SEF4 ALARM UC1 TRIP UC1-A TRIP UC1-B TRIP UC2-C TRIP UC2-A ALARM UC2-B ALARM UC2-B ALARM THM ALARM THM ALARM THM TRIP NOC1 TRIP NOC2 ALARM	SEF3 trip command SEF4 alarm command UC1 trip command UC1 trip command (A Phase) UC1 trip command (B Phase) UC1 trip command (C Phase) UC2 alarm command UC2 alarm command (A Phase) UC2 alarm command (B Phase) UC2 alarm command (C Phase) UC2 alarm command (C Phase) UC3 alarm command (C Phase) UC4 alarm command (C Phase) UC5 alarm command (C Phase) UC6 alarm command (C Phase) Thermal alarm command NOC1 trip command NOC2 alarm command
294 295 296 297 298 300 301 302 303 304 305 306 307 308 309 311 312 313	UC1 TRIP UC1-A TRIP UC1-B TRIP UC2-A LARM UC2-A ALARM UC2-B ALARM UC2-B ALARM THM ALARM THM TRIP NOC1 TRIP NOC1 TRIP NOC2 ALARM BCD TRIP	SEF3 trip command SEF4 alarm command UC1 trip command UC1 trip command (A Phase) UC1 trip command (B Phase) UC1 trip command (C Phase) UC2 alarm command UC2 alarm command (A Phase) UC2 alarm command (C Phase) UC2 alarm command (C Phase) UC2 alarm command (C Phase) UC3 alarm command (C Phase) UC4 alarm command (C Phase) UC5 alarm command (C Phase) UC6 alarm command UC7 trip command UC7 trip command UC7 trip command
294 295 296 297 298 300 301 302 303 304 305 306 307 308 309 310 311 312 313	SEF4 ALARM UC1 TRIP UC1-A TRIP UC1-B TRIP UC1-C TRIP UC2 ALARM UC2-A ALARM UC2-B ALARM UC2-B ALARM THM ALARM THM TRIP NOC1 TRIP NOC2 ALARM BCD TRIP CBF RETRIP	SEF3 trip command SEF4 alarm command UC1 trip command UC1 trip command (A Phase) UC1 trip command (B Phase) UC1 trip command (C Phase) UC2 alarm command UC2 alarm command UC2 alarm command (C Phase) UC2 alarm command (C Phase) UC3 trip command (C Phase) UC4 alarm command UC5 alarm command (C Phase) UC6 alarm command (C Phase) UC7 alarm command (C Phase) UC8 alarm command UC9 trip command
294 295 296 297 298 299 300 301 302 303 304 305 306 307 309 310 311 312 313 314 315	SEF4 ALARM UC1 TRIP UC1-A TRIP UC1-B TRIP UC1-C TRIP UC2 ALARM UC2-A ALARM UC2-B ALARM UC2-C ALARM THM TRIP NOC1 TRIP NOC1 TRIP NOC2 ALARM BCD TRIP CBF RETRIP CBF RETRIP-A	SEF3 trip command SEF4 alarm command UC1 trip command UC1 trip command UC1 trip command (A Phase) UC1 trip command (B Phase) UC1 trip command (C Phase) UC2 alarm command UC2 alarm command (A Phase) UC2 alarm command (B Phase) UC2 alarm command (B Phase) UC2 alarm command (C Phase) UC3 alarm command (C Phase) Thermal alarm command Thermal trip command NOC1 trip command NOC1 trip command NOC2 alarm command SCD trip command CBF retrip command
294 295 296 297 298 299 300 301 302 303 304 305 306 307 308 309 310 311 312 313 314 315 316	SEF4 ALARM UC1 TRIP UC1-A TRIP UC1-B TRIP UC1-C TRIP UC2 ALARM UC2-A ALARM UC2-B ALARM THM ALARM THM TRIP NOC1 TRIP NOC2 ALARM BCD TRIP CBF RETRIP CBF RETRIP-A CBF RETRIP-B	SEF3 trip command SEF4 alarm command UC1 trip command UC1 trip command UC1 trip command (A Phase) UC1 trip command (B Phase) UC1 trip command (C Phase) UC2 alarm command (A Phase) UC2 alarm command (A Phase) UC2 alarm command (A Phase) UC2 alarm command (B Phase) UC2 alarm command (C Phase) UC2 alarm command (C Phase) UC2 alarm command (C Phase) UC2 alarm command UC2 alarm command UC2 trip command UC3 trip command UC4 trip command UC5 trip command UC5 trip command UC6 trip command UC7 trip command UC7 trip command UC8 trip command UC8 trip command UC9 trip command
294 295 296 297 298 300 301 302 303 304 305 306 307 308 309 310 311 312 313 314 315 316 317	UC1 TRIP UC1-A TRIP UC1-B TRIP UC1-C TRIP UC2-A ALARM UC2-A ALARM UC2-B ALARM UC2-B ALARM THM ALARM THM TRIP NOC1 TRIP NOC2 ALARM BCD TRIP CBF RETRIP CBF RETRIP-A CBF RETRIP-B CBF RETRIP-C	SEF3 trip command SEF4 alarm command UC1 trip command UC1 trip command (A Phase) UC1 trip command (B Phase) UC1 trip command (C Phase) UC2 alarm command (C Phase) UC2 alarm command (B Phase) UC2 alarm command Thermal trip command NOC1 trip command NOC1 trip command NOC2 trip command CBF retrip command CBF retrip command(CBF retrip comma
294 295 296 297 298 300 301 302 303 304 305 306 307 308 309 311 312 313 314 315 316 317 318	SEF4 ALARM UC1 TRIP UC1-A TRIP UC1-B TRIP UC1-C TRIP UC2 ALARM UC2-A ALARM UC2-B ALARM THM ALARM THM TRIP NOC1 TRIP NOC2 ALARM BCD TRIP CBF RETRIP CBF RETRIP-A CBF RETRIP-B	SEF3 trip command SEF4 alarm command UC1 trip command UC1 trip command UC1 trip command (A Phase) UC1 trip command (B Phase) UC1 trip command (C Phase) UC2 alarm command (A Phase) UC2 alarm command (A Phase) UC2 alarm command (A Phase) UC2 alarm command (B Phase) UC2 alarm command (C Phase) UC2 alarm command (C Phase) UC2 alarm command (C Phase) UC2 alarm command UC2 alarm command UC2 trip command UC3 trip command UC4 trip command UC5 trip command UC5 trip command UC6 trip command UC7 trip command UC7 trip command UC8 trip command UC8 trip command UC9 trip command

No.	Signal Name	Contents
321	CBF TRIP-C	CBF back trip command(C Phase)
322		
323		
324		
325		
326		
327		
328		
329		
330		
331	OV1 TRIP	OV1 trip command
	OV1-IKII OV1-A TRIP	
332		OV1 trip command(A Phase)
333	OV1-B TRIP	OV1 trip command(B Phase)
334	OV1-C TRIP	OV1 trip command(C Phase)
335	OV2 ALARM	OV2 alarm command
336	OV2-A ALARM	OV2 alarm command(A Phase)
337	OV2-B ALARM	OV2 alarm command(B Phase)
338	OV2-C ALARM	OV2 alarm command(C Phase)
	OVZ-O ALAKWI	OVZ diarifi cominand(O i nase)
339		
340		
341	UV1 TRIP	UV1 trip command
342	UV1-A TRIP	UV1 trip command(A Phase)
343	UV1-B TRIP	UV1 trip command(B Phase)
344	UV1-C TRIP	UV1 trip command(C Phase)
345	UV2 ALARM	UV2 alarm command
346	UV2-A ALARM	UV2 alarm command(A Phase)
347	UV2-B ALARM	UV2 alarm command(B Phase)
348	UV2-C ALARM	UV2 alarm command(C Phase)
349		
350		
351	ZOV1 TRIP	ZOV1 trip command
352	ZOV2 ALARM	ZOV2 alarm command
353	NOV1 TRIP	NOV1 trip command
354	NOV2 ALARM	NOV2 alarm command
355	FRQ TRIP	FRQ trip command
356	FRQ1 TRIP	FRQ1 trip command
357	FRQ2 TRIP	FRQ2 trip command
358	FRQ3 TRIP	FRQ3 trip command
359	FRQ4 TRIP	FRQ4 trip command
360		
361		
361 362		
361 362 363		
361 362		
361 362 363		
361 362 363 364 365		
361 362 363 364 365 366		
361 362 363 364 365 366 367		
361 362 363 364 365 366 367 368		
361 362 363 364 365 366 367 368 369		
361 362 363 364 365 366 367 368 369 370		
361 362 363 364 365 366 367 368 369 370 371	GEN.TRIP	General trip command
361 362 363 364 365 366 367 368 369 370	GEN.TRIP GEN.TRIP-A	General trip command General trip command (A Phase)
361 362 363 364 365 366 367 368 369 370 371		
361 362 363 364 365 366 367 368 369 370 371	GEN.TRIP-A GEN.TRIP-B	General trip command (A Phase) General trip command (B Phase)
361 362 363 364 365 366 367 368 369 370 371 372 373	GEN.TRIP-A GEN.TRIP-B GEN.TRIP-C	General trip command (A Phase) General trip command (B Phase) General trip command (C Phase)
361 362 363 364 365 366 367 368 369 370 371 372 373 374	GEN.TRIP-A GEN.TRIP-B GEN.TRIP-C GEN.TRIP-N	General trip command (A Phase) General trip command (B Phase) General trip command (C Phase) General trip command (N Phase)
361 362 363 364 365 366 367 368 369 371 372 373 374 375 376	GEN.TRIP-A GEN.TRIP-B GEN.TRIP-C GEN.TRIP-N CLP STATE0	General trip command (A Phase) General trip command (B Phase) General trip command (C Phase) General trip command (N Phase) Cold Load Protection State
361 362 363 364 365 366 367 368 370 371 372 373 374 375 376	GEN.TRIP-A GEN.TRIP-B GEN.TRIP-C GEN.TRIP-N CLP STATE0 CLP STATE1	General trip command (A Phase) General trip command (B Phase) General trip command (C Phase) General trip command (N Phase) Cold Load Protection State Cold Load Protection State
361 362 363 364 365 366 367 368 370 371 372 373 374 375 376 377	GEN.TRIP-A GEN.TRIP-B GEN.TRIP-C GEN.TRIP-N CLP STATE0 CLP STATE1 CLP STATE2	General trip command (A Phase) General trip command (B Phase) General trip command (C Phase) General trip command (N Phase) General trip command (N Phase) Cold Load Protection State Cold Load Protection State Cold Load Protection State
361 362 363 364 365 366 367 368 369 370 371 372 373 374 375 376 377	GEN.TRIP-A GEN.TRIP-B GEN.TRIP-C GEN.TRIP-N CLP STATE0 CLP STATE1 CLP STATE2 CLP STATE2	General trip command (A Phase) General trip command (B Phase) General trip command (C Phase) General trip command (N Phase) Cold Load Protection State
361 362 363 364 365 366 367 368 370 371 372 373 374 375 376 377	GEN.TRIP-A GEN.TRIP-B GEN.TRIP-C GEN.TRIP-N CLP STATE0 CLP STATE1 CLP STATE2	General trip command (A Phase) General trip command (B Phase) General trip command (C Phase) General trip command (N Phase) General trip command (N Phase) Cold Load Protection State Cold Load Protection State Cold Load Protection State
361 362 363 364 365 366 367 368 369 370 371 372 373 374 375 376 377	GEN.TRIP-A GEN.TRIP-B GEN.TRIP-C GEN.TRIP-N CLP STATE0 CLP STATE1 CLP STATE2 CLP STATE2	General trip command (A Phase) General trip command (B Phase) General trip command (C Phase) General trip command (N Phase) Cold Load Protection State
361 362 363 364 365 366 367 368 369 370 371 372 373 374 375 376 377 378 379 380	GEN.TRIP-A GEN.TRIP-B GEN.TRIP-C GEN.TRIP-N CLP STATE0 CLP STATE1 CLP STATE2 CLP STATE3 GEN.ALARM GEN.ALARM-A	General trip command (A Phase) General trip command (B Phase) General trip command (C Phase) General trip command (N Phase) General trip command (N Phase) Cold Load Protection State Cold Load Protection State Cold Load Protection State Cold Load Protection State General alarm command General alarm command
361 362 363 364 365 366 367 368 369 370 371 372 373 374 375 376 377 378 379 380 381	GEN.TRIP-A GEN.TRIP-B GEN.TRIP-C GEN.TRIP-N CLP STATE0 CLP STATE1 CLP STATE2 CLP STATE3 GEN.ALARM GEN.ALARM-A GEN.ALARM-B	General trip command (A Phase) General trip command (B Phase) General trip command (C Phase) General trip command (N Phase) General trip command (N Phase) Cold Load Protection State Cold Load Protection State Cold Load Protection State Cold Load Protection State General alarm command General alarm command General alarm command (B Phase) General alarm command (B Phase)
361 362 363 364 365 366 367 368 369 371 372 373 374 375 376 377 378 379 381 382 383	GEN.TRIP-A GEN.TRIP-B GEN.TRIP-C GEN.TRIP-N CLP STATE0 CLP STATE1 CLP STATE2 CLP STATE3 GEN.ALARM-A GEN.ALARM-B GEN.ALARM-B GEN.ALARM-C	General trip command (A Phase) General trip command (B Phase) General trip command (C Phase) General trip command (N Phase) General trip command (N Phase) Cold Load Protection State General alarm command General alarm command (A Phase) General alarm command (B Phase) General alarm command (C Phase)
361 362 363 364 365 366 367 368 369 370 371 372 373 374 375 376 377 378 379 380 381 382 383	GEN.TRIP-A GEN.TRIP-B GEN.TRIP-C GEN.TRIP-N CLP STATE0 CLP STATE1 CLP STATE2 CLP STATE3 GEN.ALARM GEN.ALARM-B GEN.ALARM-B GEN.ALARM-C GEN.ALARM-N	General trip command (A Phase) General trip command (B Phase) General trip command (C Phase) General trip command (N Phase) General trip command (N Phase) Cold Load Protection State Cold Load Protection State Cold Load Protection State Cold Load Protection State General alarm command General alarm command (A Phase) General alarm command (B Phase) General alarm command (C Phase) General alarm command (N Phase)
361 362 363 364 365 366 367 368 369 370 371 372 373 374 375 376 377 378 379 380 381 382 383 384	GEN.TRIP-A GEN.TRIP-B GEN.TRIP-C GEN.TRIP-N CLP STATE0 CLP STATE1 CLP STATE2 CLP STATE3 GEN.ALARM GEN.ALARM-A GEN.ALARM-B GEN.ALARM-C GEN.ALARM-N CTF	General trip command (A Phase) General trip command (B Phase) General trip command (C Phase) General trip command (N Phase) General trip command (N Phase) Cold Load Protection State Cold Load Protection State Cold Load Protection State Cold Load Protection State General alarm command General alarm command (A Phase) General alarm command (B Phase) General alarm command (C Phase) General alarm command (N Phase) General alarm command (N Phase) General alarm command (N Phase)
361 362 363 364 365 366 367 368 369 370 371 372 373 374 375 376 377 378 379 380 381 382 383 384 365 386	GEN.TRIP-A GEN.TRIP-B GEN.TRIP-C GEN.TRIP-N CLP STATE0 CLP STATE1 CLP STATE2 CLP STATE3 GEN.ALARM GEN.ALARM-A GEN.ALARM-A GEN.ALARM-C GEN.ALARM-C GEN.ALARM-N CTF	General trip command (A Phase) General trip command (B Phase) General trip command (C Phase) General trip command (N Phase) General trip command (N Phase) Cold Load Protection State Cold Load Protection State Cold Load Protection State Cold Load Protection State General alarm command General alarm command (A Phase) General alarm command (B Phase) General alarm command (C Phase) General alarm command (N Phase) CT failure detection
361 362 363 364 365 366 367 368 369 370 371 372 373 374 375 376 377 378 379 380 381 382 383 384	GEN.TRIP-A GEN.TRIP-B GEN.TRIP-N CLP STATE0 CLP STATE1 CLP STATE2 CLP STATE3 GEN.ALARM GEN.ALARM-A GEN.ALARM-B GEN.ALARM-C GEN.ALARM-N CTF VTF	General trip command (A Phase) General trip command (B Phase) General trip command (C Phase) General trip command (N Phase) General trip command (N Phase) Cold Load Protection State Cold Load Protection State Cold Load Protection State Cold Load Protection State General alarm command General alarm command (A Phase) General alarm command (B Phase) General alarm command (C Phase) General alarm command (N Phase) CT failure detection VT failure detection VT failure detection
361 362 363 364 365 366 367 368 369 370 371 372 373 374 375 376 377 378 379 380 381 382 383 384 365 386	GEN.TRIP-A GEN.TRIP-B GEN.TRIP-C GEN.TRIP-N CLP STATE0 CLP STATE1 CLP STATE2 CLP STATE3 GEN.ALARM GEN.ALARM-A GEN.ALARM-A GEN.ALARM-C GEN.ALARM-C GEN.ALARM-N CTF	General trip command (A Phase) General trip command (B Phase) General trip command (C Phase) General trip command (N Phase) General trip command (N Phase) Cold Load Protection State Cold Load Protection State Cold Load Protection State Cold Load Protection State General alarm command General alarm command (A Phase) General alarm command (B Phase) General alarm command (C Phase) General alarm command (N Phase) CT failure detection
361 362 363 364 365 366 367 368 369 370 371 372 373 374 375 376 377 378 380 381 382 383 384 385 386	GEN.TRIP-A GEN.TRIP-B GEN.TRIP-N CLP STATE0 CLP STATE1 CLP STATE2 CLP STATE3 GEN.ALARM GEN.ALARM-A GEN.ALARM-B GEN.ALARM-C GEN.ALARM-N CTF VTF	General trip command (A Phase) General trip command (B Phase) General trip command (C Phase) General trip command (N Phase) General trip command (N Phase) Cold Load Protection State Cold Load Protection State Cold Load Protection State Cold Load Protection State General alarm command General alarm command (A Phase) General alarm command (B Phase) General alarm command (C Phase) General alarm command (N Phase) CT failure detection VT failure detection VT failure detection
361 362 363 364 365 366 367 368 370 371 372 373 374 375 376 377 378 379 381 382 383 384 385 386 387	GEN.TRIP-A GEN.TRIP-B GEN.TRIP-N CLP STATE0 CLP STATE1 CLP STATE2 CLP STATE3 GEN.ALARM GEN.ALARM-A GEN.ALARM-B GEN.ALARM-C GEN.ALARM-N CTF VTF	General trip command (A Phase) General trip command (B Phase) General trip command (C Phase) General trip command (N Phase) General trip command (N Phase) Cold Load Protection State Cold Load Protection State Cold Load Protection State Cold Load Protection State General alarm command General alarm command (A Phase) General alarm command (B Phase) General alarm command (C Phase) General alarm command (N Phase) CT failure detection VT failure detection VT failure detection
361 362 363 364 365 366 367 368 369 370 371 372 373 374 375 376 377 378 379 380 381 382 383 384 385 386 387 388 389	GEN.TRIP-A GEN.TRIP-B GEN.TRIP-N CLP STATE0 CLP STATE1 CLP STATE2 CLP STATE3 GEN.ALARM GEN.ALARM-A GEN.ALARM-B GEN.ALARM-C GEN.ALARM-N CTF VTF	General trip command (A Phase) General trip command (B Phase) General trip command (C Phase) General trip command (N Phase) General trip command (N Phase) Cold Load Protection State Cold Load Protection State Cold Load Protection State Cold Load Protection State General alarm command General alarm command (A Phase) General alarm command (B Phase) General alarm command (C Phase) General alarm command (N Phase) CT failure detection VT failure detection VT failure detection
361 362 363 364 365 366 367 368 369 370 371 372 373 374 375 376 377 378 379 380 381 382 383 384 385 386 387 389 390 391	GEN.TRIP-A GEN.TRIP-B GEN.TRIP-N CLP STATE0 CLP STATE1 CLP STATE2 CLP STATE3 GEN.ALARM GEN.ALARM-A GEN.ALARM-B GEN.ALARM-C GEN.ALARM-N CTF VTF	General trip command (A Phase) General trip command (B Phase) General trip command (C Phase) General trip command (N Phase) General trip command (N Phase) Cold Load Protection State Cold Load Protection State Cold Load Protection State Cold Load Protection State General alarm command General alarm command (A Phase) General alarm command (B Phase) General alarm command (C Phase) General alarm command (N Phase) CT failure detection VT failure detection VT failure detection
361 362 363 364 365 366 367 368 369 370 371 372 373 374 375 376 377 378 380 381 382 383 384 385 386 387 388 389 390 391	GEN.TRIP-A GEN.TRIP-B GEN.TRIP-N CLP STATE0 CLP STATE1 CLP STATE2 CLP STATE3 GEN.ALARM GEN.ALARM-A GEN.ALARM-B GEN.ALARM-C GEN.ALARM-N CTF VTF	General trip command (A Phase) General trip command (B Phase) General trip command (C Phase) General trip command (N Phase) General trip command (N Phase) Cold Load Protection State Cold Load Protection State Cold Load Protection State Cold Load Protection State General alarm command General alarm command (A Phase) General alarm command (B Phase) General alarm command (C Phase) General alarm command (N Phase) CT failure detection VT failure detection VT failure detection
361 362 363 364 365 366 367 368 369 370 371 372 373 374 375 376 377 378 379 380 381 382 383 384 385 386 387 388 389 390 391 392 393	GEN.TRIP-A GEN.TRIP-B GEN.TRIP-N CLP STATE0 CLP STATE1 CLP STATE2 CLP STATE3 GEN.ALARM GEN.ALARM-A GEN.ALARM-B GEN.ALARM-C GEN.ALARM-N CTF VTF	General trip command (A Phase) General trip command (B Phase) General trip command (C Phase) General trip command (N Phase) General trip command (N Phase) Cold Load Protection State Cold Load Protection State Cold Load Protection State Cold Load Protection State General alarm command General alarm command (A Phase) General alarm command (B Phase) General alarm command (C Phase) General alarm command (N Phase) CT failure detection VT failure detection VT failure detection
361 362 363 364 365 366 367 368 369 370 371 372 373 374 375 376 377 378 380 381 382 383 384 385 386 387 388 389 390 391	GEN.TRIP-A GEN.TRIP-B GEN.TRIP-N CLP STATE0 CLP STATE1 CLP STATE2 CLP STATE3 GEN.ALARM GEN.ALARM-A GEN.ALARM-B GEN.ALARM-C GEN.ALARM-N CTF VTF	General trip command (A Phase) General trip command (B Phase) General trip command (C Phase) General trip command (N Phase) General trip command (N Phase) Cold Load Protection State Cold Load Protection State Cold Load Protection State Cold Load Protection State General alarm command General alarm command (A Phase) General alarm command (B Phase) General alarm command (C Phase) General alarm command (N Phase) CT failure detection VT failure detection VT failure detection
361 362 363 364 365 366 367 368 369 370 371 372 373 374 375 376 377 378 380 381 382 383 384 385 386 387 388 389 390 391 392	GEN.TRIP-A GEN.TRIP-B GEN.TRIP-N CLP STATE0 CLP STATE1 CLP STATE2 CLP STATE3 GEN.ALARM GEN.ALARM-A GEN.ALARM-B GEN.ALARM-C GEN.ALARM-N CTF VTF	General trip command (A Phase) General trip command (B Phase) General trip command (C Phase) General trip command (N Phase) General trip command (N Phase) Cold Load Protection State Cold Load Protection State Cold Load Protection State Cold Load Protection State General alarm command General alarm command (A Phase) General alarm command (B Phase) General alarm command (C Phase) General alarm command (N Phase) CT failure detection VT failure detection VT failure detection
361 362 363 364 365 366 367 368 369 370 371 372 373 374 375 376 377 378 379 380 381 382 383 384 385 386 387 389 390 391 393 394 395	GEN.TRIP-A GEN.TRIP-B GEN.TRIP-N CLP STATE0 CLP STATE1 CLP STATE2 CLP STATE3 GEN.ALARM GEN.ALARM-A GEN.ALARM-B GEN.ALARM-C GEN.ALARM-N CTF VTF	General trip command (A Phase) General trip command (B Phase) General trip command (C Phase) General trip command (N Phase) General trip command (N Phase) Cold Load Protection State Cold Load Protection State Cold Load Protection State Cold Load Protection State General alarm command General alarm command (A Phase) General alarm command (B Phase) General alarm command (C Phase) General alarm command (N Phase) CT failure detection VT failure detection VT failure detection
361 362 363 364 365 366 367 368 369 370 371 372 373 374 375 376 377 378 379 380 381 382 383 384 385 387 389 390 391 392 393 394 395 396	GEN.TRIP-A GEN.TRIP-B GEN.TRIP-N CLP STATE0 CLP STATE1 CLP STATE2 CLP STATE3 GEN.ALARM GEN.ALARM-A GEN.ALARM-B GEN.ALARM-C GEN.ALARM-N CTF VTF	General trip command (A Phase) General trip command (B Phase) General trip command (C Phase) General trip command (N Phase) General trip command (N Phase) Cold Load Protection State Cold Load Protection State Cold Load Protection State Cold Load Protection State General alarm command General alarm command (A Phase) General alarm command (B Phase) General alarm command (C Phase) General alarm command (N Phase) CT failure detection VT failure detection VT failure detection
361 362 363 364 365 366 367 368 369 370 371 372 373 374 375 376 377 378 380 381 382 383 384 385 386 387 389 390 391 392 393	GEN.TRIP-A GEN.TRIP-B GEN.TRIP-N CLP STATE0 CLP STATE1 CLP STATE2 CLP STATE3 GEN.ALARM GEN.ALARM-A GEN.ALARM-B GEN.ALARM-C GEN.ALARM-N CTF VTF	General trip command (A Phase) General trip command (B Phase) General trip command (C Phase) General trip command (N Phase) General trip command (N Phase) Cold Load Protection State Cold Load Protection State Cold Load Protection State Cold Load Protection State General alarm command General alarm command (A Phase) General alarm command (B Phase) General alarm command (C Phase) General alarm command (N Phase) CT failure detection VT failure detection VT failure detection
361 362 363 364 365 366 367 368 369 370 371 372 373 374 375 376 377 378 379 380 381 382 383 384 385 386 387 388 389 390 391 392 393 394 396 397 398	GEN.TRIP-A GEN.TRIP-B GEN.TRIP-N CLP STATE0 CLP STATE1 CLP STATE2 CLP STATE3 GEN.ALARM GEN.ALARM-A GEN.ALARM-B GEN.ALARM-C GEN.ALARM-N CTF VTF	General trip command (A Phase) General trip command (B Phase) General trip command (C Phase) General trip command (N Phase) General trip command (N Phase) Cold Load Protection State Cold Load Protection State Cold Load Protection State Cold Load Protection State General alarm command General alarm command (A Phase) General alarm command (B Phase) General alarm command (C Phase) General alarm command (N Phase) CT failure detection VT failure detection VT failure detection
361 362 363 364 365 366 367 368 369 370 371 372 373 374 375 376 377 378 379 380 381 382 383 384 385 386 387 389 390 391 392 393 394 395 396 397	GEN.TRIP-A GEN.TRIP-B GEN.TRIP-N CLP STATE0 CLP STATE1 CLP STATE2 CLP STATE3 GEN.ALARM GEN.ALARM-A GEN.ALARM-B GEN.ALARM-C GEN.ALARM-N CTF VTF	General trip command (A Phase) General trip command (B Phase) General trip command (C Phase) General trip command (N Phase) General trip command (N Phase) Cold Load Protection State Cold Load Protection State Cold Load Protection State Cold Load Protection State General alarm command General alarm command (A Phase) General alarm command (B Phase) General alarm command (C Phase) General alarm command (N Phase) CT failure detection VT failure detection VT failure detection

No.	Signal Name	Contents
401	ARC READY T	Auto-Reclosing ready condition
401	ARC READY I	Auto-Reclosing ready condition Auto-Reclosing in-progress condition
402	ARC SHOT	
403	ARC SHOT1	Auto-Reclosing shot Auto-Reclosing shot of number1
		v
405	ARC SHOT2	Auto-Reclosing shot of number2
406	ARC SHOT3	Auto-Reclosing shot of number3
407	ARC SHOT4	Auto-Reclosing shot of number4
408	ARC SHOT5	Auto-Reclosing shot of number5
409	ARC FT	Auto-Reclosing failed (Final trip)
410	ARC SUCCESS	Auto-Reclosing succeed
411	ARC COORD	Auto-Reclosing coordination
412		•
413		
414		
415		
416		
417		
418		
419		
420		
421	A.M.F.OFF	Automatic monitoring function off
422	RELAY FAIL	Relay failure & trip blocked alarm
423	RELAY FAIL-A	Relay failure alarm (Trip not blocked)
424	TCSV	Trip circuit supervision failure
425	CBSV	Circuit breaker status monitoring failure
426	TC ALARM	Trip counter alarm
427	SGM I'y ALM	ΣIY alarm
428	OT ALARM	Operate time alarm
429	CT ERR	CT circuit supervison
430	V0 ERR	
		VT circuit supervison(V0)
431	V2 ERR	VT circuit supervison(V2)
432	CTF ALARM	CT failure detection
433	VTF1 ALARM	VT failure detection 1
434	VTF2 ALARM	VT failure detection 2
435		
436		
437		
438		
439		
440		
441		/10
442		
443		
444		
445		
446		
447		1 / F
448		
449		
450	•	
451	F.RECORD CLR	Fault record cleared
452	E.RECORD CLR	Event record cleared
453	D.RECORD CLR	Disturbance record cleared
454	TP COUNT CLR	Trip counter cleared
455	I'v COUNT CLR	SGM_I^y counter cleared
456	AR COUNT CLR	ARC Counter CLR
457	DEMAND CLR	Demand cleared
458	IND.RESET	Indication reset
459		Data lost
	DATA LOST	
460	SYS.CHANGE	System setting changed
461	RLY.CHANGE	Relay setting changed
462	GRP.CHANGE	Group setting changed
463	Y	
464		
465	<u> </u>	
466		
467		
468		
469		
470		
471	BO1 OP	Binary output 1
472	BO2 OP	Binary output 1
473	BO3 OP	Binary output 3
	BO4 OP	Binary output 4
474		Binary output 5
475	BO5 OP	
475 476	BO6 OP	Binary output 6
475 476 477		
475 476	BO6 OP	Binary output 6
475 476 477 478 479	BO6 OP	Binary output 6
475 476 477 478	BO6 OP	Binary output 6

No.	Signal Name	Contents	
481			
482			
483			
484			
485			
486			
487			
488			
489			
490			
491	LCD IND.	LCD indication(Virtual LED) command	
492	LCD IND1.	LCD indication1(Virtual LED) command	
493	LCD IND2.	LCD indication2(Virtual LED) command	
494	TESTING	Test LED ON	_
495	ARC.COM.ON	Auto-recloser command ON	
496			
497	PROT.COM.ON	Protection command ON	
498	IECTST	IEC60870-5-103 test mode	
499	IECBLK	IEC60870-5-103 monitor direction blocked	
500			
	•		

Appendix D

Event Record Items

\vdash	ıΔr	٦ŧ	Da	200	rd	Iten	ne
\Box	/UI	ш	Πt	CU	ıu	пеп	uъ

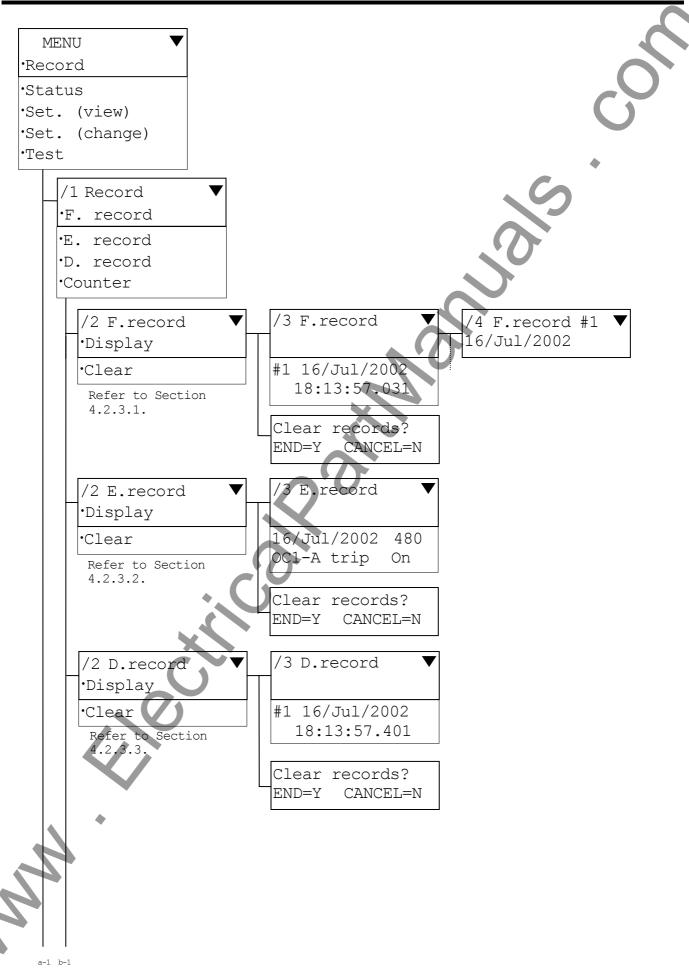
Even	t Record Items		
No.	LCD indication		Contents
1	GEN.trip	Off/On	General trip command
2	GEN.alarm	Off/On	General trip command
3	OC1 trip	Off/On	OC1 trip command
4	OC2 trip	Off/On	OC2 trip command
5	OC3 trip	Off/On	OC3 trip command
6	OC4 alarm	Off/On	OC4 alarm command
7	EF1 trip	Off/On	EF1 trip command
8	EF2 trip	Off/On	EF2 trip command
9	EF3 trip	Off/On	EF3 trip command
10	EF4 alarm	Off/On	EF4 alarm command
11	SEF1-S1 trip	Off/On	SEF1 Stage1 trip command
12	SEF1-S2 trip	Off/On	SEF1 Stage2 trip command
13	SEF2 trip	Off/On	SEF2 trip command
14	SEF3 trip	Off/On	SEF3 trip command
15	SEF4 alarm	Off/On	SEF4 alarm command
16	NOC1 trip	Off/On	NOC1 trip command
17	NOC2 alarm	Off/On	NOC2 alarm command
18	UC1 trip	Off/On	UC1 trip
19	UC2 alarm	Off/On	UC2 alarm
20	THM alarm	Off/On	Thermal alarm command
21	THM trip	Off/On	Thermal trip command
22	BCD trip	Off/On	BCD trip command
23	CBF retrip	Off/On	CBF retrip command
24	CBF trip	Off/On	CBF back trip command
25	OV1 trip	Off/On	OV1 trip command
26	OV2 alarm	Off/On	OV3 alarm command
27	UV1 trip	Off/On	UV1 trip command
28	UV2 alarm	Off/On	UV3 alarm command
29	ZOV1 trip	Off/On	ZOV1 trip command
30	ZOV2 alarm	Off/On	ZOV2 alarm command
31	NOV1 trip	Off/On	NOV1 trip command
32	NOV2 alarm	Off/On	NOV2 alarm command
33	FRQ1 trip	Off/On	FRQ1 trip command
34	FRQ2 trip	Off/On	FRQ2 trip command
35	FRQ3 trip	Off/On	FRQ3 trip command
36	FRQ4 trip	Off/On	FRQ4 trip command
37	ARC READY T	Off/On	Auto-Reclosing ready
38	ARC SHOT	Off/On	Auto-Reclosing shot of number
39	ARC IN-PROG	Off/On	Auto-Reclosing in progress
40	OC1-A	Off/On	OC1-A relay element operating
41	OC1-B	Off/On	OC1-B relay element operating
42	OC1-C	Off/On	OC1-C relay element operating
43	OC2-A	Off/On	OC2-A relay element operating
44	OC2-B	Off/On	OC2-B relay element operating
45	OC2-C	Off/On	OC2-C relay element operating
46	OC3-A	Off/On	OC3-A relay element operating
47	OC3-B	Off/On	OC3-B relay element operating
48	OC3-C	Off/On	OC3-C relay element operating
49	OC4-A	Off/On	OC4-A relay element operating
50	OC4-B	Off/On	OC4-B relay element operating
51	OC4-C	Off/On	OC4-C relay element operating
52	EF1	Off/On	EF1 relay element operating
53	EF2	Off/On	EF2 relay element operating
54	EF3	Off/On	EF3 relay element operating
55	EF4	Off/On	EF4 relay element operating
56	SEF1	Off/On	SEF1 relay element operating
57	SEF2	Off/On	SEF2 relay element operating
58	SEF3	Off/On	SEF3 relay element operating
59	SEF4	Off/On	SEF4 relay element operating
60	NOC1	Off/On	NOC1 relay element operating
61	NOC2	Off/On	NOC2 relay element operating
62	UC1-A	Off/On	UC1-A relay element operating
6 3	UC1-B	Off/On	UC1-B relay element operating
64	UC1-C	Off/On	UC1-C relay element operating
65	UC2-A	Off/On	UC2-A relay element operating
66	UC2-B	Off/On	UC2-B relay element operating
67	UC2-C	Off/On	UC2-C relay element operating
68	THM-A	Off/On	Thermal-Alarm operating
69	THM	Off/On	Thermal operating
70	BCD	Off/On	BCD relay element operating
	-		· · · · · ·

No	 LCD indication 		Contents
71		Off/On	Cold Load Protection State
72		Off/On	ditto
73		Off/On	ditto
74		Off/On	ditto
75	RPF	Off/On	Residual power forward
76		Off/On	Residual Power reverse
77	OV1-A	Off/On	OV1-1 relay element operating
78	OV1-B	Off/On	OV1-2 relay element operating
79		Off/On	OV1-3 relay element operating
80	OV2-A	Off/On	OV2-1 relay element operating
81	OV2-B	Off/On	OV2-2 relay element operating
82		Off/On	OV2-3 relay element operating
83		Off/On	UV1-1 relay element operating
84		Off/On	UV1-2 relay element operating
85		Off/On	UV1-3 relay element operating
86		Off/On	UV2-1 relay element operating
87		Off/On	UV2-2 relay element operating
88		Off/On	UV2-3 relay element operating
89		Off/On	UV blocking element operationg
90		Off/On	ZOV1 relay element operating
91		Off/On	ZOV2 relay element operating
92		Off/On	NOC1 relay element operating
93		Off/On	NOC2 relay element operating
94		Off/On	FRQ1 relay element operating
95	FRQ2	Off/On	FRQ2 relay element operating
96		Off/On	FRQ3 relay element operating
97		Off/On	FRQ4 relay element operating
98		Off/On	FRQ blockig element operating
99		Off/On	Binary input signal of BI1
100		Off/On	Binary input signal of BI2
10		Off/On	Binary input signal of Bl3
102		Off/On	Binary input signal of BI4
103		Off/On	Binary input signal of BI5
104		Off/On	Binary input signal of BI6
10		Off/On	Binary input signal of BI7
106		Off/On	Binary input signal of BI8
107		Off/On	BI command of change active setting group1
108		Off/On	BI command of change active setting group2
109	<u> </u>	Off/On	BI command of change active setting group3
110		Off/On	BI command of change active setting group4
11		Off/On	BI command of OC1 protection scheme block
112		Off/On	BI command of OC2 protection scheme block
113		Off/On	BI command of OC3 protection scheme block
114		Off/On	BI command of OC4 protection scheme block
11		Off/On	BI command of EF1 protection scheme block
116		Off/On	BI command of EF2 protection scheme block
117		Off/On	BI command of EF3 protection scheme block
118		Off/On	BI command of EF4 protection scheme block
119		Off/On	BI command of EF1 protection scheme permission
120		Off/On	BI command of EF2 protection scheme permission
12		Off/On	BI command of EF3 protection scheme permission
122		Off/On	BI command of EF4 protection scheme permission
123		Off/On	BI command of SEF1 protection scheme block
124		Off/On	BI command of SEF2 protection scheme block
12		Off/On	BI command of SEF3 protection scheme block
120		Off/On	BI command of SEF4 protection scheme block
12	7 10100411	Off/On	BI command of NOC1 protection scheme block
128	NOC2 block	Off/On	BI command of NOC2 protection scheme block
128 129	NOC2 block UC1 block	Off/On Off/On	BI command of NOC2 protection scheme block BI command of UC1 protection scheme block
128 129 130	NOC2 block UC1 block UC2 block	Off/On Off/On Off/On	BI command of NOC2 protection scheme block BI command of UC1 protection scheme block BI command of UC2 protection scheme block
128 130 131	NOC2 block UC1 block UC2 block THM block	Off/On Off/On Off/On Off/On	BI command of NOC2 protection scheme block BI command of UC1 protection scheme block BI command of UC2 protection scheme block BI command of Thermal overload protection scheme block
128 129 130 131	NOC2 block UC1 block UC2 block THM block THMA block	Off/On Off/On Off/On Off/On	BI command of NOC2 protection scheme block BI command of UC1 protection scheme block BI command of UC2 protection scheme block BI command of Thermal overload protection scheme block BI command of Thermal overload alarm scheme block
128 129 130 131 132 133	3 NOC2 block 9 UC1 block 1 UC2 block 1 THM block 2 THMA block 3 CBF block	Off/On Off/On Off/On Off/On	BI command of NOC2 protection scheme block BI command of UC1 protection scheme block BI command of UC2 protection scheme block BI command of Thermal overload protection scheme block
128 130 131 132 133 134	3 NOC2 block 9 UC1 block 1 UC2 block 1 THM block 2 THMA block 3 CBF block 4 BCD block	Off/On Off/On Off/On Off/On Off/On Off/On Off/On Off/On	BI command of NOC2 protection scheme block BI command of UC1 protection scheme block BI command of UC2 protection scheme block BI command of Thermal overload protection scheme block BI command of Thermal overload alarm scheme block BI command of CBF protection scheme block BI command of Broken Conductor protection scheme block
128 129 130 131 132 133	3 NOC2 block D UC1 block D UC2 block THM block THMA block CBF block BCD block	Off/On Off/On Off/On Off/On Off/On Off/On Off/On Off/On	BI command of NOC2 protection scheme block BI command of UC1 protection scheme block BI command of UC2 protection scheme block BI command of Thermal overload protection scheme block BI command of Thermal overload alarm scheme block BI command of CBF protection scheme block BI command of Broken Conductor protection scheme block BI command of OV1 protection scheme block BI command of OV1 protection scheme block
128 130 131 132 133 134 136 136	3 NOC2 block D UC1 block D UC2 block THM block THMA block CBF block BCD block OV1 block OV2 block	Off/On Off/On Off/On Off/On Off/On Off/On Off/On Off/On Off/On	BI command of NOC2 protection scheme block BI command of UC1 protection scheme block BI command of UC2 protection scheme block BI command of Thermal overload protection scheme block BI command of Thermal overload alarm scheme block BI command of CBF protection scheme block BI command of Broken Conductor protection scheme block BI command of OV1 protection scheme block BI command of OV2 protection scheme block BI command of OV2 protection scheme block
128 130 131 132 133 134 134	3 NOC2 block 9 UC1 block 1 UC2 block 1 THM block 2 THMA block 3 CBF block 4 BCD block 5 OV1 block 6 OV2 block 7 UV1 block	Off/On	BI command of NOC2 protection scheme block BI command of UC1 protection scheme block BI command of UC2 protection scheme block BI command of Thermal overload protection scheme block BI command of Thermal overload alarm scheme block BI command of CBF protection scheme block BI command of Broken Conductor protection scheme block BI command of OV1 protection scheme block BI command of OV2 protection scheme block BI command of UV1 protection scheme block BI command of UV1 protection scheme block BI command of UV1 protection scheme block
128 139 130 133 134 136 136 137 138	3 NOC2 block D UC1 block D UC2 block THM block C THMA block C UC1 block C UV1 block C UV2 block	Off/On	BI command of NOC2 protection scheme block BI command of UC1 protection scheme block BI command of UC2 protection scheme block BI command of Thermal overload protection scheme block BI command of Thermal overload alarm scheme block BI command of CBF protection scheme block BI command of Broken Conductor protection scheme block BI command of OV1 protection scheme block BI command of OV2 protection scheme block BI command of UV2 protection scheme block BI command of UV1 protection scheme block BI command of UV2 protection scheme block BI command of UV2 protection scheme block
128 129 130 131 132 133 134 136 136	3 NOC2 block D UC1 block D UC2 block THM block C THMA block C UV1 block	Off/On	BI command of NOC2 protection scheme block BI command of UC1 protection scheme block BI command of UC2 protection scheme block BI command of Thermal overload protection scheme block BI command of Thermal overload alarm scheme block BI command of CBF protection scheme block BI command of Broken Conductor protection scheme block BI command of OV1 protection scheme block BI command of OV2 protection scheme block BI command of UV1 protection scheme block BI command of UV1 protection scheme block BI command of UV1 protection scheme block

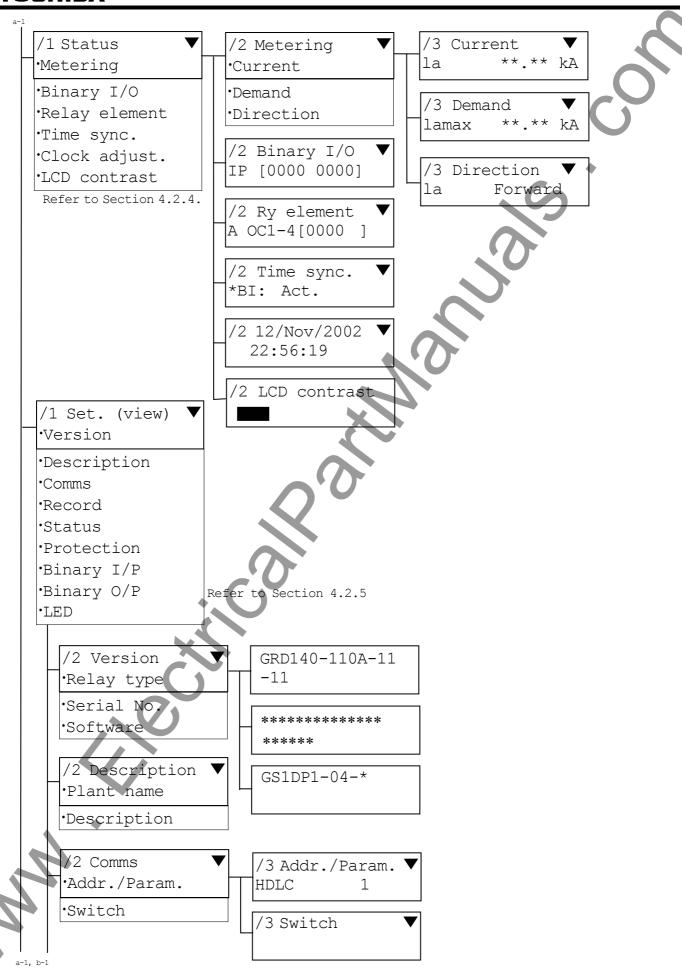
	100: " "		2 1 1
No.	LCD indication	0.00	Contents
141	NOV1 block	Off/On	BI command of NOV1 protection scheme block
142	NOV2 block	Off/On	BI command of NOV2 protection scheme block
143	FRQ1 block	Off/On	BI command of FRQ1 protection scheme block
144	FRQ2 block	Off/On	BI command of FRQ2 protection scheme block
145	FRQ3 block	Off/On	BI command of FRQ3 protection scheme block
146	FRQ4 block	Off/On	BI command of FRQ4 protection scheme block
147	ARC block	Off/On	BI command of ARC block
148	ARC ready	Off/On	BI command of ARC ready
149	ARC INIT	Off/On	BI command of ARC initiation
150	ARC N/A	Off/On	BI command of ARC no action
151	Manual CLS	Off/On	BI command of ARC initiation
152	EXT trip-3PH	Off/On	BI command of External trip (3 Phase)
153	EXT trip-APH	Off/On	BI command of External trip (A Phase)
154	EXT trip-BPH	Off/On	BI command of External trip (8 Phase)
155	EXT trip-CPH	Off/On	BI command of External trip (B Phase)
	EXT CTF		
156		Off/On	BI command of External CTF
157	CTF block	Off/On	BI command of CTF scheme block
158	EXT VTF	Off/On	BI command of External VTF
159	VTF block	Off/On	BI command of VTF scheme block
	TC fail	Off/On	BI command of Trip circuit Fail Alarm
161	CB CONT OPN	Off/On	BI command of CB N/O contact
162	CB CONT CLS	Off/On	BI command of CB N/C contact
163	Remote reset	Off/On	BI command of Remote reset
164	Store record	Off/On	BI command of Store Disturbance Record
165	Alarm1	Off/On	BI command of Alarm1
166	Alarm2	Off/On	BI command of Alarm2
167	Alarm3	Off/On	BI command of Alarm3
168	Alarm4	Off/On	BI command of Alarm4
169	CTF	Off/On	CTF detection
	VTF1	Off/On	VTF1 detection
	VTF2	Off/On	VTF2 detection
	Relay fail	Off/On	Relay failure & trip blocked alarm
		Off/On	
173	Relay fail-A		Relay failure alarm (Trip not blocked)
174	TC err	Off/On	Trip circiut supervision failure
175	CB err	Off/On	Circuit breaker status monitoring failure
176	CT err	Off/On	CT circuit supervision failure
177	TP COUNT ALM	Off/On	Trip counter alarm
178	V0 err	Off/On	VT surpervision V0 error
179	V2 err	Off/On	VT supervision V2 error
180	ΣI^yA ALM	Off/On	ΣIY A-phase alarm
181	ΣI^yA ALM	Off/On	ΣIY B-phase alarm
182	ΣI^yA ALM	Off/On	ΣIY C-phase alarm
183	OP time ALM	Off/On	Operate time alarm
184	ARC SHOT1	On	Auto-Reclosing shot of number1
185	ARC SHOT2	On	Auto-Reclosing shot of number2
186	ARC SHOT3	. On	Auto-Reclosing shot of number3
			Auto-Reclosing shot of number4
	ARC SHOT5	On	Auto-Reclosing shot of number5
189	ARC 5HO15	On	Auto-Reclosing failed (Final trip)
	ARC SUCCESS	On	
			Auto-Reclosing succeed
191	ARC RESET	On On	Auto-Reclosing reset
192	ARC CRD RST	On	Auto-Reclosing coordination reset
193	ARC COORD	On	Auto-Reclosing coordination
194	F.record CLR	On	Clear Fault records
195	E.record CLR	On	Clear Event records
	D.record CLR	On	Clear Disturbance records
197	TP COUNT CLR	On	Clear Trip counter
198	ΣI^y CLR	On	Clear ΣIY counter
	AR COUNT CLR	On	Clear Autoreclose counter
199		On	Clear demand
	Demand CLR		
200	Demand CLR IND.reset	On	Reset the indication of Trip mode, Alarm etc
200	IND.reset		
200 201 202	IND.reset Data lost	On On	Record and time date lost bye DC power supply off for a long time
200 201 202 203	IND.reset Data lost Sys.change	On On On	Record and time date lost bye DC power supply off for a long time Setting change command
200 201 202	IND.reset Data lost	On On	Record and time date lost bye DC power supply off for a long time

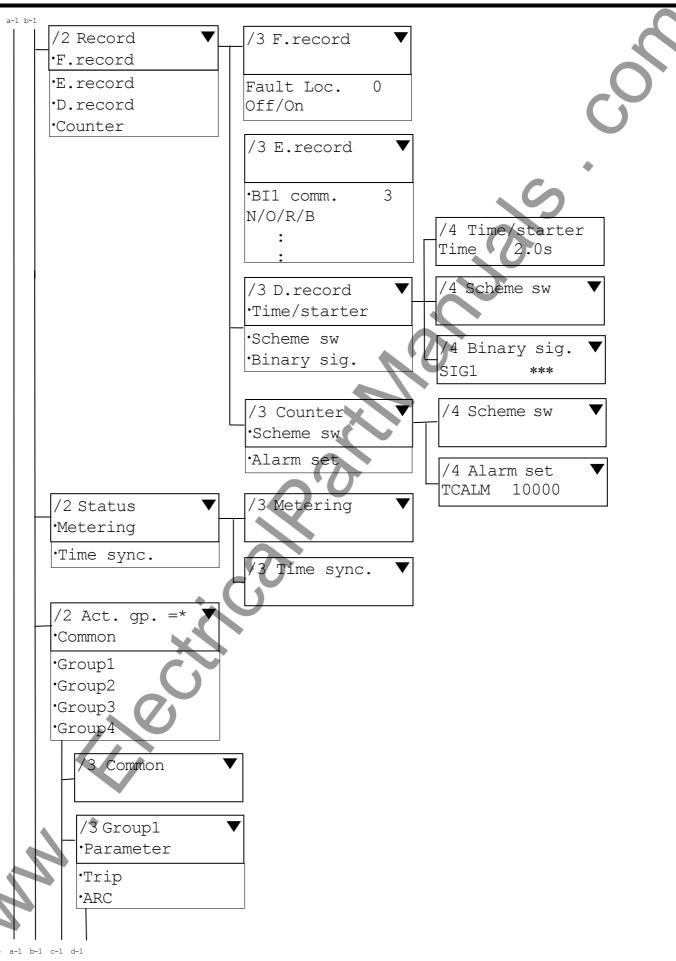
Appendix E

Details of Relay Menu and LCD & Button Operation

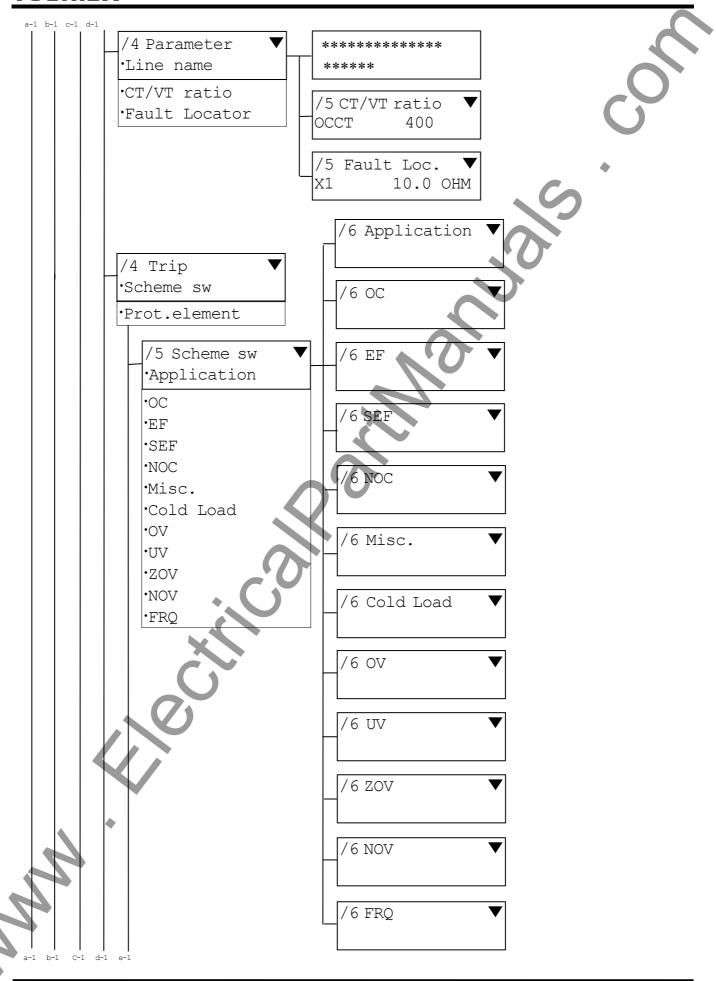


/2 Counter /3 Counter Trips ***** Display ·Clear Trips TripsA **** ·Clear Trips A TripsB **** ·Clear Trips B TripsC ***** ·Clear Trips C Σ | ^VA *****E6 ·Clear Σ In YA Σ | Λ_{VB} *****E6 ·Clear ΣI^{Λ} yB Σ | Λ_VC *****E6 •Clear ΣI^{\bullet} yC ARCs ***** ·Clear ARCs Clear Trips? Refer to Section 4.2.3.4. END=Y CANCEL=N Clear Trips A2 END=Y CANCEL=N Clear Trips B? CANCEL=N END=Y Clear Trips C? END=Y CANCEL=N Clear ΣI^{Λ} yA? END=Y CANCEL=N Clear ΣI^{Λ} yB? CANCEL=N END=Y Clear ΣI^{Λ} yC? END=Y CANCEL=N Clear ARCs? END=Y CANCEL=N

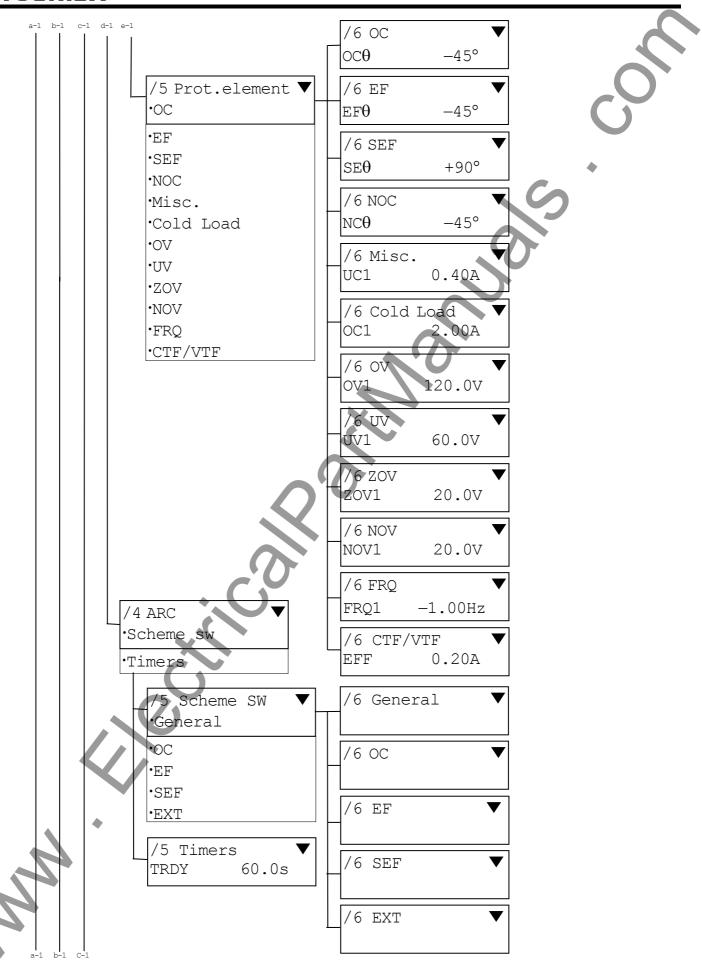


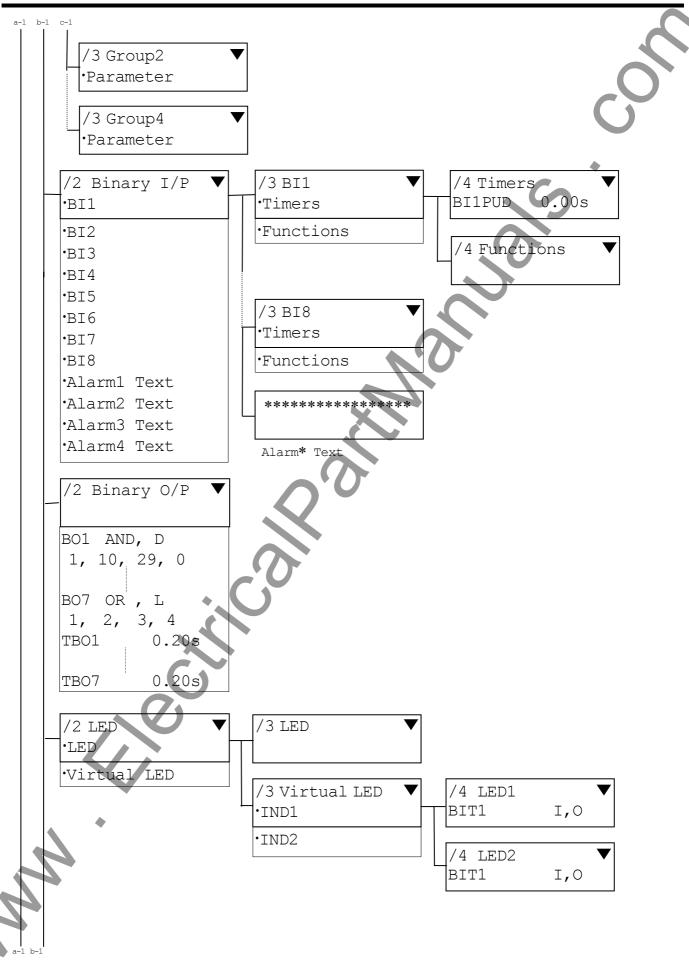


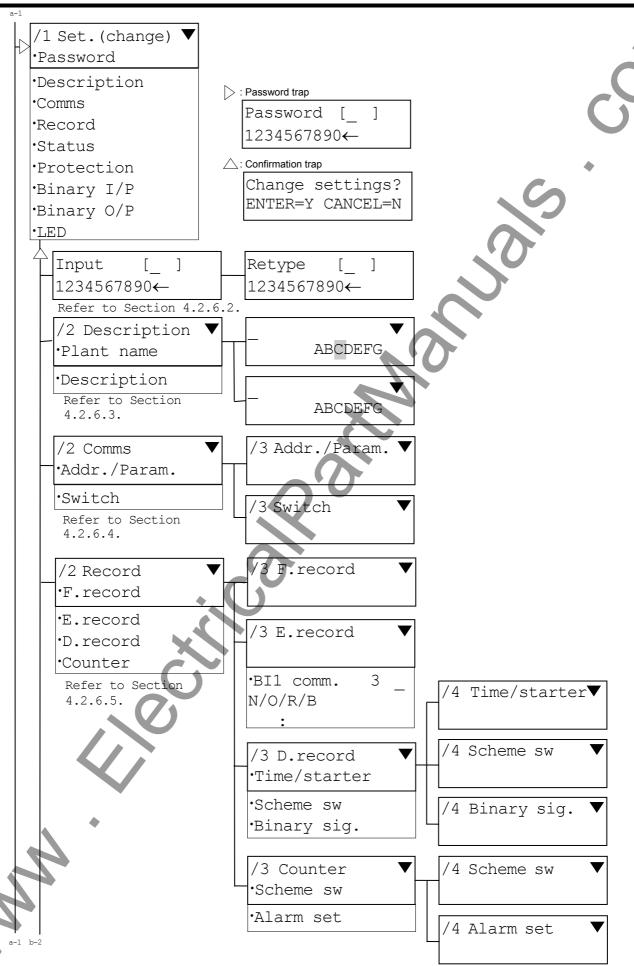
TOSHIBA

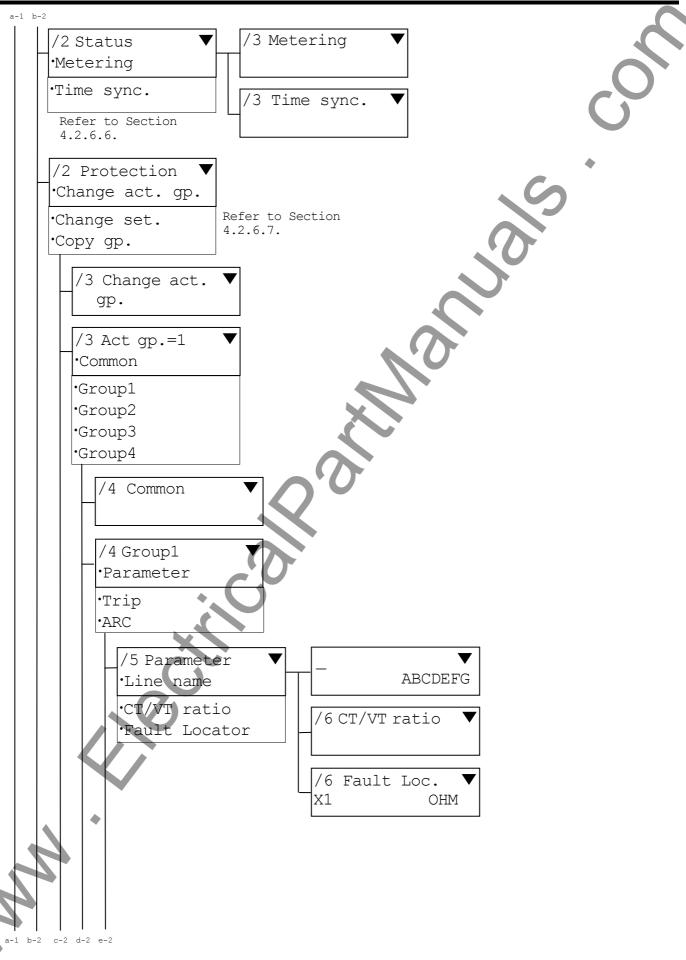


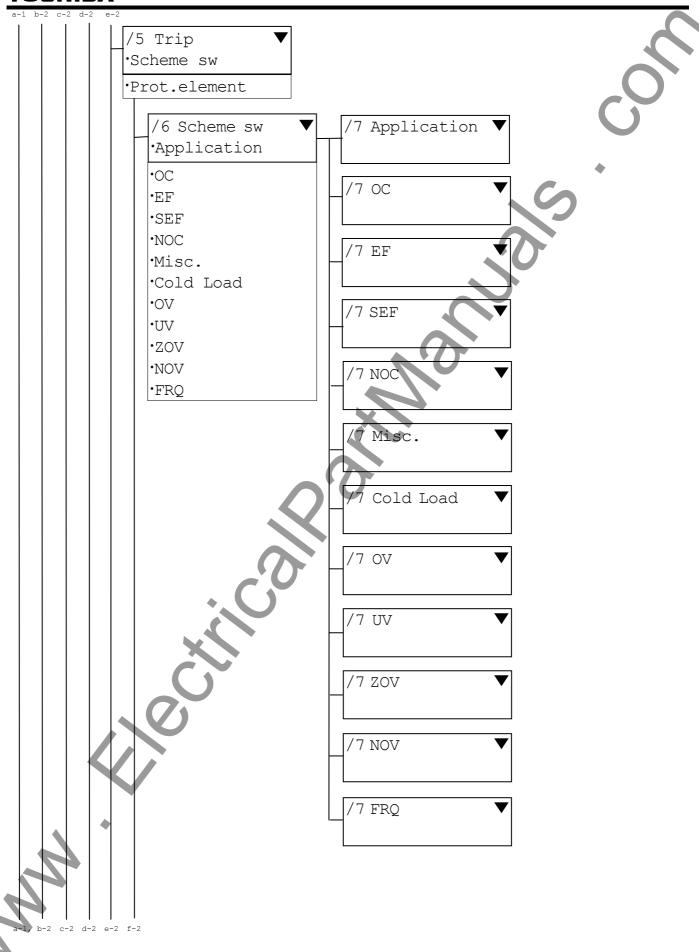
TOSHIBA

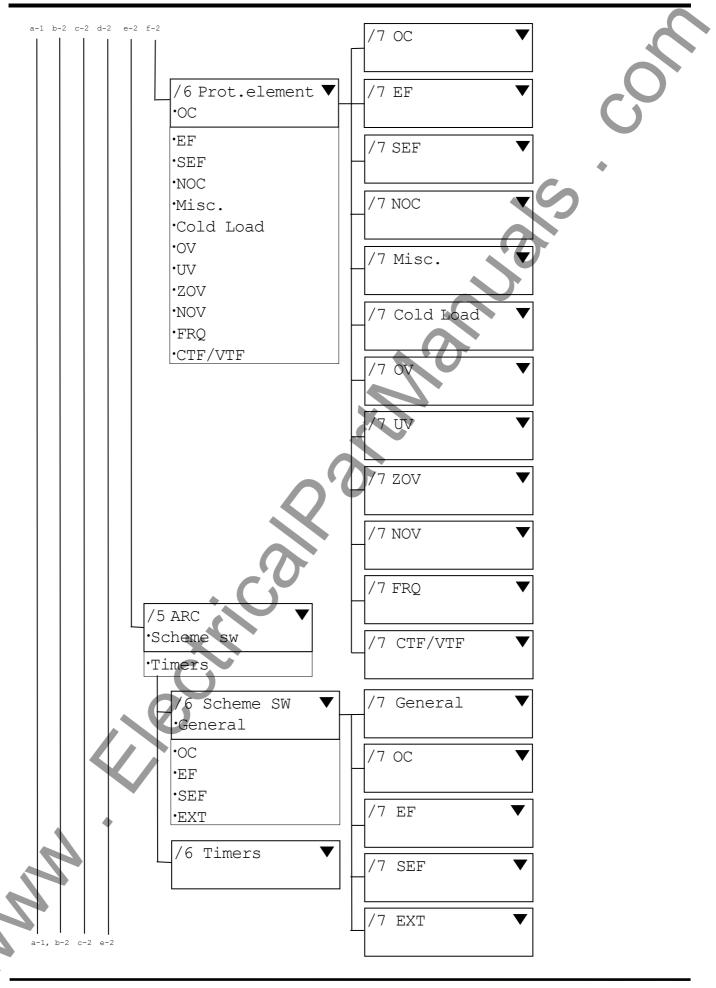


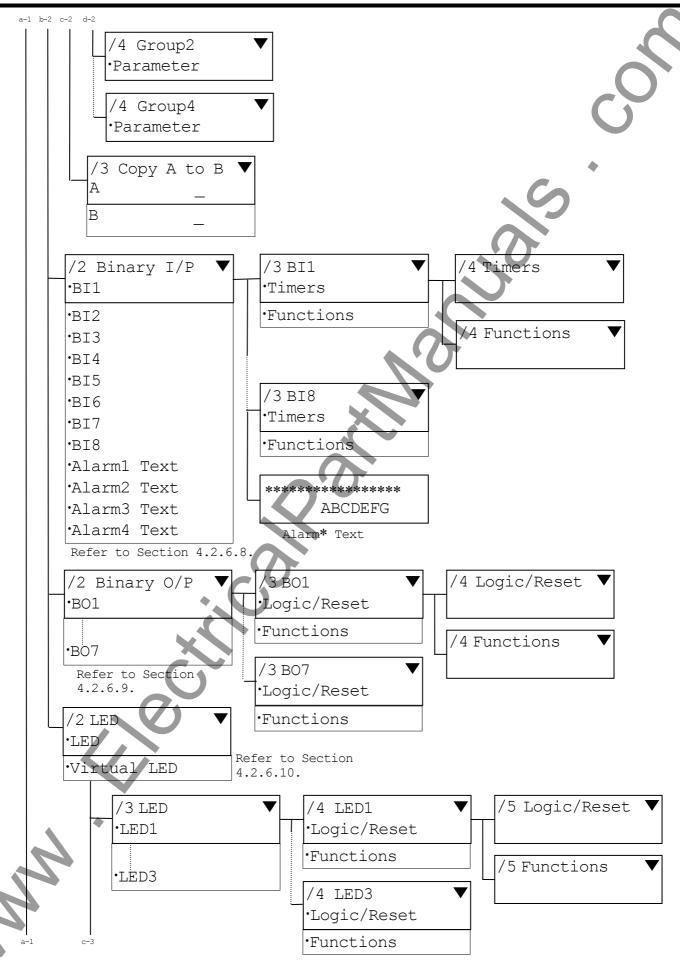


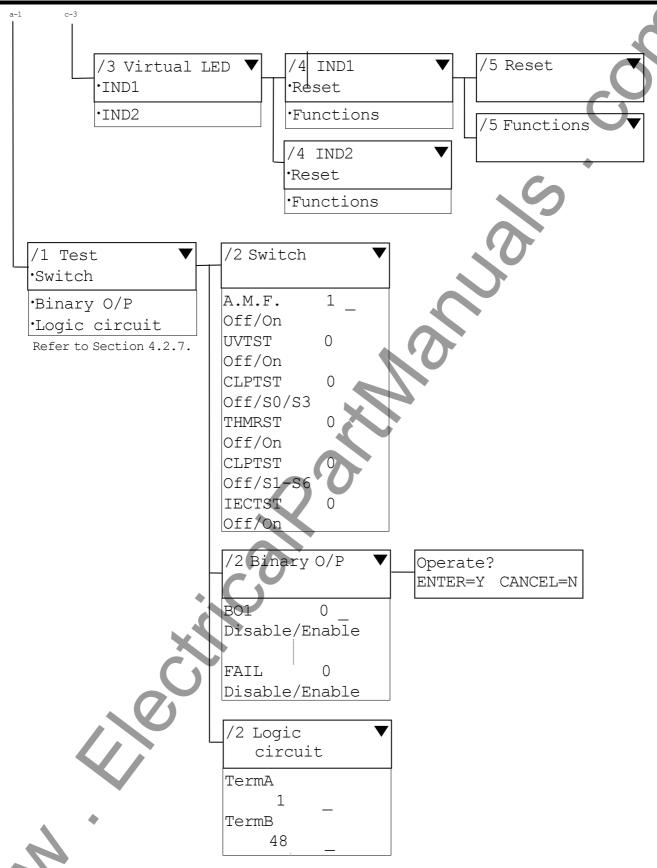




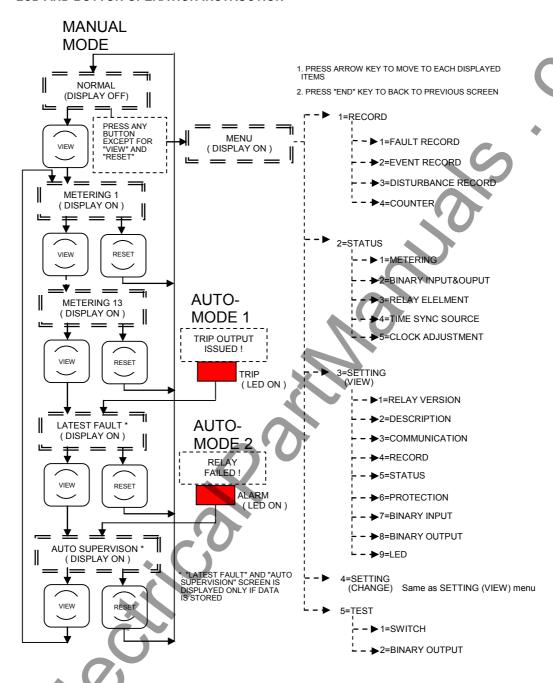






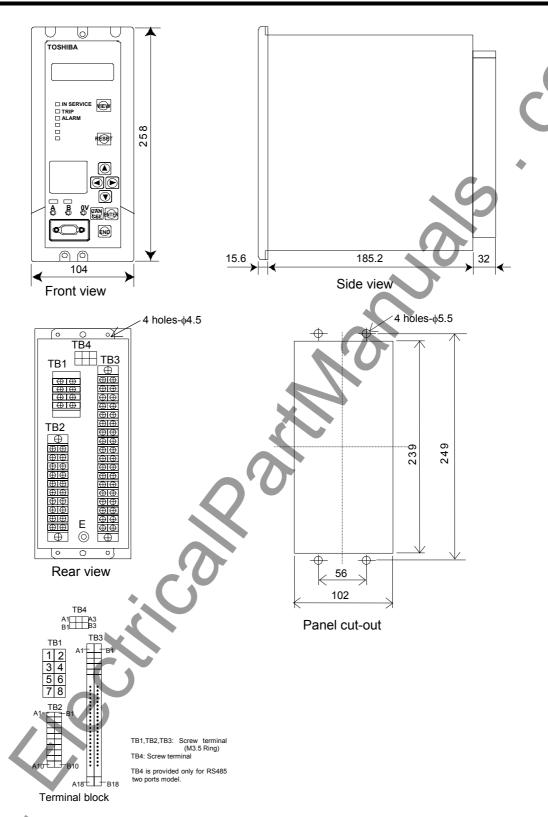


LCD AND BUTTON OPERATION INSTRUCTION



Appendix F

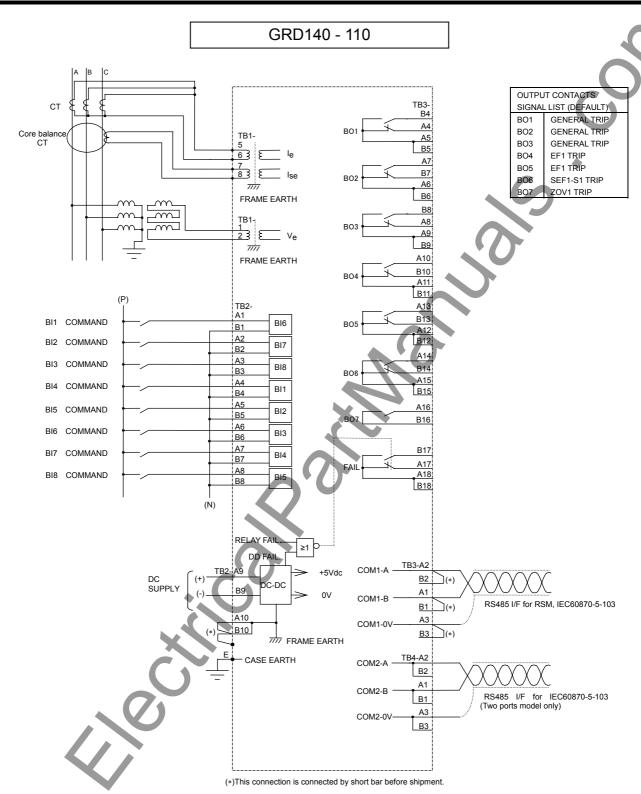
Case Outline



Case Outline

Appendix G

Typical External Connection



Typical External Connection

В6

В8

A8 A9

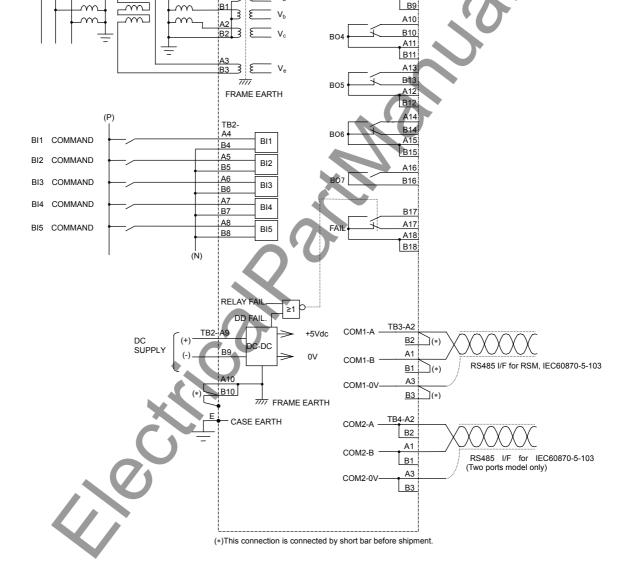
GRD140 - 400

TB2-

FRAME EARTH

OUTPUT CONTACTS
SIGNAL LIST (DEFAULT)
BO1 GENERAL TRIP
BO2 GENERAL TRIP
BO3 GENERAL TRIP
BO4 OC1 TRIP
BO5 EF1TRIP
BO6 UV1 TRIP

ZOV1 TRIP



APPL-CT = 3P, APPL-VT = 3PV Setting

Typical External Connection

GRD140 - 420 OUTPUT CONTACTS TB1-TB3-SIGNAL LIST (DEFAULT) 23 8 GENERAL TRIP BO1 A4 3 4 3 8 B01 GENERAL TRIP BO2 A5 воз OC1 TRIP B5 BO4 EFT TRIP Α7 SEF1-S1 TRIP BO5 Core balance CT В7 83 8 **UV1 TRIP BO6** A6 7/// ZOV1 TRIP В6 FRAME EARTH В8 TB2-A8 A1 3 | E Α9 B1 E В9 A2 B2 3 ξ A10 B10 B11 B3 3 E FRAME EARTH TB2-A4 BI1 COMMAND BI1 A15 B4 B15 A5 BI2 COMMAND BI2 B5 A16 A6 BI3 COMMAND B16 BI3 B6 Α7 BI4 COMMAND BI4 В7 B17 Α8 A17 BI5 COMMAND BI5 A18 B18 (N) ≥1 □ DD FAIL. TB3-A2 COM1-A -+5Vdc B2 0V COM1-B RS485 I/F for RSM, IEC60870-5-103 B1 <u></u>(*) A10 АЗ COM1-0V B10 B3 卅 FRAME EARTH CASE EARTH TB4-A2 COM2-A -B2

APPL-CT = 3P, APPL-VT = 3PV Setting

Α1

B1 A3

В3

RS485 I/F for IEC60870-5-103 (Two ports model only)

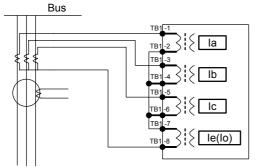
COM2-B

COM2-0V

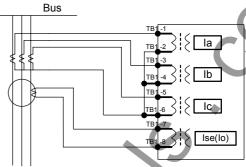
Typical External Connection

TOSHIBA

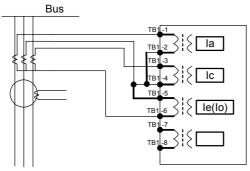
CT connection



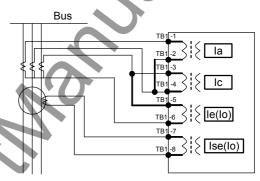
[APPL-CT] = 3P Setting for Model 400



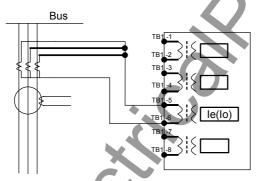
[APPL-CT] = 3P Setting for Model 420



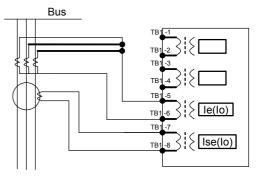
[APPL-CT] = 2P Setting for Model 400



[APPL-CT] = 2P Setting for Model 420

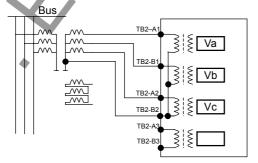


[APPL-CT] = 1P Setting for Model 400

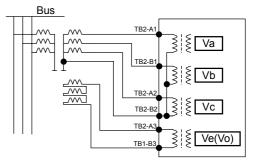


[APPL-CT] = 1P Setting for Model 420

VT connection



[APPL-VT] = 3PN Setting for Model 400 or 420



[APPL-VT] = 3PV Setting for Model 400 or 420

Appendix H

Relay Setting Sheet

- 1. Relay Identification
- 2. Line parameter
- 3. Binary output setting
- 4. Relay setting
- 5. Disturbance record signal setting
- 6. LED setting

1.	Re	av	Ide	ntifi	cati	on

Date:

Relay type	Serial Number	
Frequency	AC current	4

AC voltage DC supply voltage Password

2. Line parameter

 CT ratio
 OC:
 EF:
 SEF:

 VT ratio
 PVT:
 RVT:

3. Binary output setting

Active setting group

Model	l 110												
		Setting range			Default Setting				Setting				
ВО	Logic	Reset	Func	tions				110				Set	urig
					Logic	BOTD		Fun	ctions	Logic	BOTD	•	Functions
BO1	OR/AND	Ins/DI/Dw/Lat	ln #1	0-500	OR	Del	ln #1	371	GEN.TRIP			ln #1	
			ln #2	0-500			In #2	0		T T		ln #2	
			In #3	0-500			In #3	0				ln #3	
			In #4	0-500			In #4	0				ln #4	
	Timer	0.00 -).20					-
BO2	OR / AND	Ins/DI/Dw/Lat	ln #1	0-500	OR	Del	ln #1	371	GEN.TRIP			ln #1	
			ln #2	0-500			ln #2	0				ln #2	
			In #3	0-500			In #3	0				ln #3	
			ln #4	0-500			In #4	0				In #4	
	Timer	0.00 -						0.20					
BO3	OR / AND	Ins/DI/Dw/Lat		0-500	OR	Del	In #1	371	GEN.TRIP			ln #1	
			In #2	0-500			In #2	0				ln #2	
			In #3	0-500			In #3	0				In #3	
			In #4	0-500			In #4	6				In #4	
	Timer	0.00 -).20					
BO4	OR / AND	Ins/DI/Dw/Lat	In #1	0-500	OR	Del	In #1	281	EF1 TRIP			ln #1	
			In #2	0-500			ln #2	0				In #2	
			In #3	0-500			In #3	0				In #3	
			In #4	0-500			∃n #4	0				In #4	
	Timer	0.00 -).20					
BO5	OR / AND	Ins/DI/Dw/Lat	ln #1	0-500	OR	Del	ln #1	281	EF1 TRIP			ln #1	
			In #2	0-500	_		In #2	0				In #2	
			In #3	0-500			In #3	0				In #3	
	_	0.00	In #4	0-500			In #4	0				In #4	
200	Timer	0.00 -		0.500).20	OFFI OF TOIL				
BO6	OR / AND	Ins/DI/Dw/Lat		0-500	OR	Del	In #1	291	SEF1-S1 TRIP			In #1	
			In #2	0-500			In #2	0				In #2	
			In #3	0-500			In #3	0				In #3	
	-	2.00	In #4	0-500			In #4	0				In #4	
DO7	Timer	0.00 -	_	0.500	OR	Del	In #1).20	ZOV1 TRIP			In #4	-
BO7	OR / AND	Ins/DI/Dw/Lat	In #1	0-500 0-500	UK	Del		351	ZOVTIRIP			In #1	
			In #2	0-500			In #2 In #3	0				In #2	
			In #3	0-500			In #3	0				In #3	
	Timor	0.00 -		0-500				0.20				ii1 #4	
	Timer	0.00 -	10.00				·	J.ZU					

	1 400													
1		Setting range					Defau	lt Settin	g			So	tting	
ВО	Logic	Reset	Func	tions			4	100				36	ung	
					Logic	BOTD			ections	Logic	BOTD		Func	ctions
BO1	OR / AND	Ins/DI/Dw/Lat	In #1	0-500	OR	Del	In #1	371	GEN.TRIP			In #1		
			In #2	0-500			In #2	0				In #2		
			In #3	0-500 0-500			In #3	0				In #3 In #4		
	Timer	0.00 -		0-300				0.20				III #4		ļ
BO2	OR / AND	Ins/DI/Dw/Lat	In #1	0-500	OR	Del	ln #1	371	GEN.TRIP			ln #1	1	
502	OI (7 / II II)	#10/D#DW/Eat	In #2	0-500	Ort	Doi	In #2	0	OLI V. IT VIII			In #2		
			In #3	0-500			In #3	0				In #3		
			In #4	0-500			In #4	0				In #4		
	Timer	0.00 -	10.00				(0.20						
BO3	OR / AND	Ins/DI/Dw/Lat	ln #1	0-500	OR	Del	ln #1	371	GEN.TRIP			ln #1		
			ln #2	0-500			ln #2	0				ln #2		
			In #3	0-500			ln #3	0				In #3		
			In #4	0-500			ln #4	0				In #4		
	Timer	0.00 -).20					<u> </u>	
BO4	OR / AND	Ins/DI/Dw/Lat	In #1	0-500	OR	Del	In #1	261	OC1 TRIP			In #1		
			In #2	0-500			ln #2	0				In #2		
			In #3	0-500			In #3	0			_	In #3		
	Timor	0.00 -	In #4	0-500			In #4	0				In #4	, ·	j
BO5	Timer OR / AND	Ins/DI/Dw/Lat	In #1	0-500	OR	Del	In #1).20 281	EF1 TRIP	.		In #1		1
500	JIV/ AIND	"13/D/DW/Lat	In #2	0-500	- Oil	Dei	In #2	0	LI IINE			in #2		
			In #3	0-500	-		In #3	0				In #3		
			In #4	0-500			In #4	0				In #4		
	Timer	0.00 -				1		0.20			F		·	
BO6	OR / AND	Ins/DI/Dw/Lat	ln #1	0-500	OR	Del	ln #1	341	UV1 TRIP			ln #1		ļ
			ln #2	0-500			ln #2	0				ln #2		
			ln #3	0-500			ln #3	0				ln #3		
			ln #4	0-500			ln #4	0				ln #4		
	Timer	0.00 -	10.00				(0.20	7					
BO7	OR/AND	Ins/DI/Dw /Lat	ln #1	0-500	OR	Del	ln #1	351	ZOV1 TRIP			ln #1		i
			ln #2	0-500			ln #2	0				ln #2		
			In #3	0-500			In #3	0				ln #3		
			ln #4	0-500			In #4	0				ln #4		
	Timer	0.00 -	10.00					0.20						
Mode	1 420													
		Setting range					Dofou	t Setting						l.
ВО	Logic						Delau	ii oeiiiii	q					
		Reset	Func	tions	. 4			120	g			Set	tting	
1 1		Reset	Fund	tions	Logic	BOTD		120	ctions	Logic	BOTD	Set		etions
BO1	OR/AND	Reset Ins/Dl/Dw/Lat	In #1	0-500	Logic OR	BOTD Del	In #1	20 Fun 371		Logic	BOTD	Set		ctions
BO1	_		In #1 In #2	0-500 0-500			In #1 In #2	Fun 371 0	ctions	Logic	BOTD	In #1 In #2		ctions
BO1	_		In #1 In #2 In #3	0-500 0-500 0-500			In #1 In #2 In #3	Fun 371 0	ctions	Logic	BOTD	In #1 In #2 In #3		etions
BO1	OR/AND	Ins/Dl/Dw/Lat	In #1 In #2 In #3 In #4	0-500 0-500			In #1 In #2 In #3 In #4	Fun 371 0 0	ctions	Logic	BOTD	In #1 In #2		ctions
	OR / AND	Ins/Dl/Dw/Lat	In #1 In #2 In #3 In #4	0-500 0-500 0-500 0-500	OR	Del	In #1 In #2 In #3 In #4	Fun 371 0 0 0	ctions GEN.TRIP	Logic	BOTD	In #1 In #2 In #3 In #4		etions
BO1	OR/AND	Ins/Dl/Dw/Lat	In #1 In #2 In #3 In #4 10.00 In #1	0-500 0-500 0-500 0-500			In #1 In #2 In #3 In #4	Fun 371 0 0 0 0.20	ctions	Logic	BOTD	in #1 in #2 in #3 in #4		etions
	OR / AND	Ins/Dl/Dw/Lat	In #1 In #2 In #3 In #4 10.00 In #1 In #2	0-500 0-500 0-500 0-500 0-500 0-500	OR	Del	In #1 In #2 In #3 In #4 (In #1 In #2	Fun 371 0 0 0 0.20 371	ctions GEN.TRIP	Logic	BOTD	In #1 In #2 In #3 In #4 In #1 In #2		tions
	OR / AND	Ins/Dl/Dw/Lat	In #1 In #2 In #3 In #4 10.00 In #1 In #2 In #3	0-500 0-500 0-500 0-500 0-500 0-500 0-500	OR	Del	In #1 In #2 In #3 In #4 (In #1 In #2 In #3	Fun 371 0 0 0 0.20 371 0	ctions GEN.TRIP	Logic	BOTD	In #1 In #2 In #3 In #4 In #1 In #2 In #3		ctions
	OR / AND Timer OR / AND	Ins/DI/Dw /Lat 0.00 - Ins/DI/Dw /Lat	In #1 In #2 In #3 In #4 10.00 In #1 In #2 In #3 In #4	0-500 0-500 0-500 0-500 0-500 0-500	OR	Del	In #1 In #2 In #3 In #4 In #2 In #3 In #4 In #2 In #3 In #4	Fun 371 0 0 0 0 0 220 371 0 0	ctions GEN.TRIP	Logic	BOTD	In #1 In #2 In #3 In #4 In #1 In #2		ctions
	OR / AND	Ins/Dl/Dw/Lat	In #1 In #2 In #3 In #4 10.00 In #1 In #2 In #3 In #4 10.00	0-500 0-500 0-500 0-500 0-500 0-500 0-500	OR	Del	In #1 In #2 In #3 In #4 In #2 In #3 In #4 In #2 In #3 In #4	Fun 371 0 0 0 0.20 371 0	ctions GEN.TRIP	Logic	BOTD	In #1 In #2 In #3 In #4 In #1 In #2 In #3		ctions
BO2	OR / AND Timer OR / AND	0.00 - 0.	In #1 In #2 In #3 In #4 10.00 In #1 In #2 In #3 In #4 10.00	0-500 0-500 0-500 0-500 0-500 0-500 0-500	OR OR	Del	In #1 In #2 In #3 In #4 In #2 In #3 In #4 In #2 In #3 In #4	Fun 371 0 0 0 0 0.20 371 0 0 0	GEN.TRIP	Logic	BOTD	In #1 In #2 In #3 In #4 In #1 In #2 In #3 In #4		ctions
BO2	OR / AND Timer OR / AND	0.00 - 0.	In #1 In #2 In #3 In #4 10.00 In #1 In #2 In #3 In #4 10.00 In #1	0-500 0-500 0-500 0-500 0-500 0-500 0-500 0-500	OR OR	Del	In #1 In #2 In #3 In #4 In #2 In #3 In #4 In #2 In #3 In #4 In #4	Fun 371 0 0 0 0 0 0 0 0 0 0 0 0 0	GEN.TRIP	Logic	BOTD	In #1 In #2 In #3 In #4 In #1 In #2 In #3 In #4		ctions
BO2	OR / AND Timer OR / AND	Ins/DI/Dw/Lat 0.00 - Ins/DI/Dw/Lat 0.00 - Ins/DI/Dw/Lat	In #1 In #2 In #3 In #4 10.00 In #1 In #2 In #3 In #4 10.00 In #1 In #2 In #3 In #4	0-500 0-500 0-500 0-500 0-500 0-500 0-500 0-500 0-500	OR OR	Del	In #1 In #2 In #3 In #4 In #2 In #3 In #4 In #2 In #3 In #4 In #1 In #2	Fun 371 0 0 0 0 0 220 371 0 0 0 0 220 261 0	GEN.TRIP	Logic	BOTD	In #1 In #2 In #3 In #4 In #2 In #3 In #4 In #1 In #2 In #3 In #4		ctions
BO2	OR / AND Timer OR / AND Timer OR / AND	0.00 - Ins/DI/Dw /Lat	In #1 In #2 In #3 In #4 10.00 In #1 In #2 In #3 In #4 10.00 In #1 In #2 In #3 In #4 10.00 In #1 In #2 In #3 In #4	0-500 0-500 0-500 0-500 0-500 0-500 0-500 0-500 0-500 0-500	OR OR	Del Del	In #1 In #2 In #3 In #4	Fun 371 0 0 0.20 371 0 0 0 0.20 261 0 0 0 0.20 0 0 0 0 0 0 0 0 0 0 0 0 0 0	GEN.TRIP GEN.TRIP OC1 TRIP	Logic	BOTD	In #1 In #2 In #3 In #4 In #1 In #2 In #3 In #4 In #1 In #2 In #3 In #4		ctions
BO2	OR / AND Timer OR / AND Timer OR / AND	Ins/DI/Dw/Lat 0.00 - Ins/DI/Dw/Lat 0.00 - Ins/DI/Dw/Lat	In #1 In #2 In #3 In #4 10.00 In #1 In #2 In #3 In #4 10.00 In #1 In #2 In #3 In #4 10.00 In #1 In #2 In #3 In #4	0-500 0-500 0-500 0-500 0-500 0-500 0-500 0-500 0-500 0-500 0-500	OR OR	Del	In #1 In #2 In #3 In #4 In #2 In #3 In #4 In #3 In #4 In #2 In #3 In #4 In #2 In #3 In #4	Fun 371 0 0 0 0 0 220 371 0 0 0 0 220 261 0 0 0 220 281	GEN.TRIP	Logic	BOTD	In #1 In #2 In #3 In #4 In #3 In #4 In #3 In #4 In #1 In #2 In #3 In #4 In #1		ctions
BO2	OR / AND Timer OR / AND Timer OR / AND	0.00 - Ins/DI/Dw /Lat	In #1 In #2 In #3 In #4 10.00 In #1 In #2 In #3 In #4 10.00 In #1 In #2 In #3 In #4 10.00 In #1 In #2	0-500 0-500 0-500 0-500 0-500 0-500 0-500 0-500 0-500 0-500 0-500 0-500	OR OR	Del Del	In #1 In #2 In #3 In #4 In #2 In #3 In #4 In #3 In #4 In #3 In #4 In #3 In #4 In #1 In #2	Fun 371 0 0 0 0.20 371 0 0 0 0.20 261 0 0 0 0.20 281 0	GEN.TRIP GEN.TRIP OC1 TRIP	Logic	BOTD	In #1 In #2 In #3 In #4 In #3 In #4 In #1 In #2 In #3 In #4 In #1 In #2 In #3 In #4		ctions
BO2	OR / AND Timer OR / AND Timer OR / AND	0.00 - Ins/DI/Dw /Lat	In #1 In #2 In #3 In #4 10.00 In #1 In #2 In #3 In #4 10.00 In #1 In #2 In #3 In #4 10.00 In #1 In #2 In #3	0-500 0-500 0-500 0-500 0-500 0-500 0-500 0-500 0-500 0-500 0-500 0-500 0-500	OR OR	Del Del	In #1 In #2 In #3 In #4 In #2 In #3 In #4 In #1 In #2 In #3 In #4 In #1 In #2 In #3 In #4 In #3 In #4	Fun 371 0 0 0 20 371 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	GEN.TRIP GEN.TRIP OC1 TRIP	Logic	BOTD	In #1 In #2 In #3 In #4 In #3 In #4 In #1 In #2 In #3 In #4 In #1 In #2 In #3 In #4		ctions
BO2	OR/AND Timer OR/AND Timer OR/AND Timer OR/AND	Ins/DI/Dw/Lat 0.00 - Ins/DI/Dw/Lat 0.00 - Ins/DI/Dw/Lat 0.00 - Ins/DI/Dw/Lat	In #1 In #2 In #3 In #4 10.00 In #1 In #2 In #3 In #4 10.00 In #1 In #2 In #3 In #4 10.00 In #1 In #2 In #3 In #4	0-500 0-500 0-500 0-500 0-500 0-500 0-500 0-500 0-500 0-500 0-500 0-500	OR OR	Del Del	n #1	Fun 371 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	GEN.TRIP GEN.TRIP OC1 TRIP	Logic	BOTD	In #1 In #2 In #3 In #4 In #3 In #4 In #1 In #2 In #3 In #4 In #1 In #2 In #3 In #4		ctions
BO2 BO3	OR/AND Timer OR/AND Timer OR/AND Timer OR/AND	Ins/DI/Dw/Lat 0.00 - Ins/DI/Dw/Lat 0.00 - Ins/DI/Dw/Lat 0.00 - Ins/DI/Dw/Lat	In #1 In #2 In #3 In #4 10.00 In #1 In #2 In #3 In #4 10.00 In #1 In #2 In #3 In #4 In #1	0-500 0-500 0-500 0-500 0-500 0-500 0-500 0-500 0-500 0-500 0-500 0-500 0-500 0-500 0-500	OR OR OR	Del Del Del	n #1	Fun 371 0 0 0 .20 371 0 0 0 .220 281 0 0 0 0 .20 .20 .20 .20 .20 .20 .20 .20	GEN.TRIP GEN.TRIP OC1 TRIP EF1 TRIP	Logic	BOTD	h #1		ctions
BO2	OR/AND Timer OR/AND Timer OR/AND Timer OR/AND	Ins/DI/Dw/Lat 0.00 - Ins/DI/Dw/Lat 0.00 - Ins/DI/Dw/Lat 0.00 - Ins/DI/Dw/Lat	In #1 In #2 In #3 In #4 In #0 In #1 In #2 In #3 In #4 In #0 In #1 In #2 In #3 In #4 In #0 In #1 In #2 In #3 In #4 In #0 In #1 In #2 In #3 In #4 In #0 In #1 In #2 In #3 In #4 In #0 In #1 In #2 In #3 In #4 In #0 In #1	0-500 0-500 0-500 0-500 0-500 0-500 0-500 0-500 0-500 0-500 0-500 0-500 0-500	OR OR	Del Del	In #1	Fun 371 0 0 0 220 371 0 0 0 0 220 281 0 0 0 0 220 291	GEN.TRIP GEN.TRIP OC1 TRIP	Logic	BOTD	h #1 h #2 ln #3 ln #4 h #1 h #1 h #2 h #3 h #4 h #1 h #4 h #4 h #4 h #4 h #4		ctions
BO2 BO3	OR/AND Timer OR/AND Timer OR/AND Timer OR/AND	Ins/DI/Dw/Lat 0.00 - Ins/DI/Dw/Lat 0.00 - Ins/DI/Dw/Lat 0.00 - Ins/DI/Dw/Lat	In #1 In #2 In #3 In #4 In #0 In #1 In #2 In #3 In #4 In #0 In #1 In #2 In #3 In #4 In #0 In #1 In #2 In #3 In #4	0-500 0-500	OR OR OR	Del Del Del	n #1	Fun 371 0 0 0 20 371 0 0 0 0 20 261 0 0 0 0 220 281 0 0 0 0 220 291 0 0 0 0 20 0 0 0 0 0 0 0 0 0 0 0 0 0 0	GEN.TRIP GEN.TRIP OC1 TRIP EF1 TRIP	Logic	BOTD	h #1 h #2 h #4		ctions
BO2 BO3	OR/AND Timer OR/AND Timer OR/AND Timer OR/AND	Ins/DI/Dw/Lat 0.00 - Ins/DI/Dw/Lat 0.00 - Ins/DI/Dw/Lat 0.00 - Ins/DI/Dw/Lat	In #1 In #2 In #3 In #4 10.00 In #1 In #2 In #3 In #4 10.00 In #1 In #2 In #3 In #4	0-500 0-	OR OR OR	Del Del Del	N #1	Fun 371 0 0 0 0 220 3711 0 0 0 0 0 220 261 0 0 0 0 0 220 281 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	GEN.TRIP GEN.TRIP OC1 TRIP EF1 TRIP	Logic	BOTD	h #1 h #2 h #3 h #4 h #1 h #4 h #1 h #4		ctions
BO2 BO3	OR/AND Timer OR/AND Timer OR/AND Timer OR/AND Timer OR/AND	Ins/DI/Dw/Lat 0.00 - Ins/DI/Dw/Lat 0.00 - Ins/DI/Dw/Lat 0.00 - Ins/DI/Dw/Lat	In #1 In #2 In #3 In #3 In #4 10.00 In #1 In #2 In #3 In #4 10.00 In #1 In #2 In #3 In #4 In #1 In #2 In #3 In #4 In #3 In #4 In #3 In #4 In #3 In #4	0-500 0-500	OR OR OR	Del Del Del	N #1	Fun 371 0 0 0 220 371 0 0 0 0 220 281 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	GEN.TRIP GEN.TRIP OC1 TRIP EF1 TRIP	Logic	BOTD	h #1 h #2 h #4		tions
BO2 BO3 BO4	OR/AND Timer OR/AND Timer OR/AND Timer OR/AND Timer OR/AND	Ins/DI/Dw/Lat 0.00 - Ins/DI/Dw/Lat 0.00 - Ins/DI/Dw/Lat 0.00 - Ins/DI/Dw/Lat 0.00 - Ins/DI/Dw/Lat	In #1 In #2 In #3 In #4 10.00 In #1 In #2 In #3 In #4 10.00 In #1 In #2 In #3 In #4 10.00 In #1 In #2 In #3 In #4 10.00 In #1 In #2 In #3 In #4 10.00	0-500 0-	OR OR OR	Del Del Del	N #1	Fun 371 0 0 0 220 371 0 0 0 0 220 261 0 0 0 0 220 291 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	GEN.TRIP GEN.TRIP OC1 TRIP EF1 TRIP SEF1-S1 TRIP	Logic	BOTD	h #1 h #2 h #3 h #4 h #1 h #4		tions
BO2 BO3	OR/AND Timer OR/AND Timer OR/AND Timer OR/AND Timer OR/AND	Ins/DI/Dw/Lat 0.00 - Ins/DI/Dw/Lat 0.00 - Ins/DI/Dw/Lat 0.00 - Ins/DI/Dw/Lat	In #1 In #2 In #3 In #4 10.00 In #1 In #2 In #3 In #4 10.00 In #1 In #2 In #3 In #4 10.00 In #1 In #2 In #3 In #4 10.00 In #1 In #2 In #3 In #4	0-500 0-	OR OR OR	Del Del Del	N #1	Fun 371 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	GEN.TRIP GEN.TRIP OC1 TRIP EF1 TRIP	Logic	BOTD	h #1		tions
BO2 BO3 BO4	OR/AND Timer OR/AND Timer OR/AND Timer OR/AND Timer OR/AND	Ins/DI/Dw/Lat 0.00 - Ins/DI/Dw/Lat 0.00 - Ins/DI/Dw/Lat 0.00 - Ins/DI/Dw/Lat 0.00 - Ins/DI/Dw/Lat	In #1 In #2 In #3 In #4 In #0 In #1 In #2 In #3 In #4 In #0 In #1 In #2 In #3 In #4 In #0 In #1 In #2 In #3 In #4 In #0 In #1 In #2 In #3 In #4 In #0 In #1 In #2 In #3 In #4 In #0 In #1 In #2 In #3 In #4 In #4 In #4 In #4 In #6 In #7	0-500 0-	OR OR OR	Del Del Del	n #1	Fun 371 0 0 0 220 371 0 0 0 0 220 261 0 0 0 0 220 291 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	GEN.TRIP GEN.TRIP OC1 TRIP EF1 TRIP SEF1-S1 TRIP	Logic	BOTD	h #1 h #2 h #3 h #4 h #1 h #4		tions
BO2 BO3 BO4	OR/AND Timer OR/AND Timer OR/AND Timer OR/AND Timer OR/AND	Ins/DI/Dw/Lat 0.00 - Ins/DI/Dw/Lat 0.00 - Ins/DI/Dw/Lat 0.00 - Ins/DI/Dw/Lat 0.00 - Ins/DI/Dw/Lat	In #1 In #2 In #3 In #4 10.00 In #1 In #2 In #3 In #4 10.00 In #1 In #2 In #3 In #4 10.00 In #1 In #2 In #3 In #4 10.00 In #1 In #2 In #3 In #4	0-500 0-	OR OR OR	Del Del Del	N #1	Fun 371 0 0 0 0 0 0 0 0 0	GEN.TRIP GEN.TRIP OC1 TRIP EF1 TRIP SEF1-S1 TRIP	Logic	BOTD	h #1 h #2 h #3 h #4 h #1 h #2 h #3 h #4 h #1 h #4		tions
BO2 BO3 BO4	OR/AND Timer OR/AND Timer OR/AND Timer OR/AND Timer OR/AND	Ins/DI/Dw/Lat 0.00 - Ins/DI/Dw/Lat 0.00 - Ins/DI/Dw/Lat 0.00 - Ins/DI/Dw/Lat 0.00 - Ins/DI/Dw/Lat	In #1 In #2 In #3 In #4 I0.00 In #1 In #2 In #3 In #4 I0.00 In #1 In #2 In #3 In #4 I0.00 In #1 In #2 In #3 In #4 I0.00 In #1 In #2 In #3 In #4 I0.00 In #1 In #2 In #3 In #4 I0.00 In #1 In #2 In #3 In #4 I0.00 In #1 In #2 In #3 In #4 I0.00 In #1 In #2 In #3 In #4	0-500 0-	OR OR OR	Del Del Del	N #1	Section Sect	GEN.TRIP GEN.TRIP OC1 TRIP EF1 TRIP SEF1-S1 TRIP	Logic	BOTD	h #1 h #2 h #3 h #4 h #1 h #4 h #1 h #4 h #4 h #4 h #4		tions
BO2 BO3 BO4	Timer OR / AND Timer OR / AND Timer OR / AND Timer OR / AND	Ins/DI/Dw/Lat 0.00 - Ins/DI/Dw/Lat 0.00 - Ins/DI/Dw/Lat 0.00 - Ins/DI/Dw/Lat 0.00 - Ins/DI/Dw/Lat	In #1 In #2 In #3 In #4 10.00 In #1 In #2 In #3 In #4 10.00 In #1 In #2 In #3 In #4 10.00 In #1 In #2 In #3 In #4 10.00 In #1 In #2 In #3 In #4 10.00 In #1 In #2 In #3 In #4 10.00 In #1 In #2 In #3 In #4 10.00 In #1 In #2	0-500 0-	OR OR OR	Del Del Del	N #1	Fun 371 0 0 0 220 3711 0 0 0 0 220 281 0 0 0 0 220 291 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	GEN.TRIP GEN.TRIP OC1 TRIP EF1 TRIP SEF1-S1 TRIP	Logic	BOTD	h #1 h #2 h #3 h #4 h #1 h #4 h #1 h #4 h #4 h #4 h #4		tions
BO2 BO3 BO4 BO6	OR/AND Timer OR/AND Timer OR/AND Timer OR/AND Timer OR/AND Timer OR/AND	Ins/DI/Dw/Lat 0.00 - Ins/DI/Dw/Lat	In #1 In #2 In #3 In #4 10.00 In #1 In #2 In #3 In #4 10.00 In #1 In #2 In #3 In #4 10.00 In #1 In #2 In #3 In #4 10.00 In #1 In #2 In #3 In #4 10.00 In #1 In #2 In #3 In #4 10.00 In #1 In #2 In #3 In #4 10.00 In #1 In #2	0-500 0-	OR OR OR OR	Del Del Del Del	N #1	Fun 371 0 0 0 220 371 0 0 0 0 220 281 0 0 0 0 220 291 0 0 0 0 220 341 0 0 0 0 220 291 20 0 0 0 0 220 291 20 0 0 0 0 220 291 20 0 0 0 0 220 291 0 0 0 0 0 220 291 0 0 0 0 0 220 291 0 0 0 0 0 220 291 0 0 0 0 0 220 291 0 0 0 0 0 220 291 0 0 0 0 0 220 291 0 0 0 0 0 220 291 0 0 0 0 0 220 291 0 0 0 0 0 220 291 0 0 0 0 0 220 291 0 0 0 0 0 220 291 0 0 0 0 0 0 220 291 0 0 0 0 0 0 0 220 0 0 0 0 0 0 0 0 0 0	GEN.TRIP GEN.TRIP OC1 TRIP EF1 TRIP SEF1-S1 TRIP UV1 TRIP	Logic	BOTD	h #1 h #2 h #3 h #4 h #1 h #4 h #1 h #4		tions
BO2 BO3 BO4 BO6	OR/AND Timer OR/AND Timer OR/AND Timer OR/AND Timer OR/AND Timer OR/AND	Ins/DI/Dw/Lat 0.00 - Ins/DI/Dw/Lat	In #1 In #2 In #3 In #4 10.00 In #1 In #2 In #3 In #4 10.00 In #1 In #2 In #3 In #4 10.00 In #1 In #2 In #3 In #4 10.00 In #1 In #2 In #3 In #4 10.00 In #1 In #2 In #3 In #4 10.00 In #1 In #2 In #3 In #4 10.00 In #1 In #2 In #3 In #4	0-500 0-	OR OR OR OR	Del Del Del Del	N #1	Fun 371 0 0 0 220 371 0 0 0 0 220 281 0 0 0 0 220 291 0 0 0 0 220 341 0 0 0 0 220 351	GEN.TRIP GEN.TRIP OC1 TRIP EF1 TRIP SEF1-S1 TRIP UV1 TRIP	Logic	BOTD	h #1 h #2 h #3 h #4 h #1 h #2 h #3 h #4 h #1 h #2 h #3 h #4 h #1 h #2 h #3 h #4		tions
BO2 BO3 BO4 BO6	OR/AND Timer OR/AND Timer OR/AND Timer OR/AND Timer OR/AND Timer OR/AND	Ins/DI/Dw/Lat 0.00 - Ins/DI/Dw/Lat	In #1 In #2 In #3 In #4 10.00 In #1 In #2 In #3 In #4 10.00 In #1 In #2 In #3 In #4 10.00 In #1 In #2 In #3 In #4 10.00 In #1 In #2 In #3 In #4 10.00 In #1 In #2 In #3 In #4 10.00 In #1 In #2 In #3 In #4 10.00 In #1 In #2 In #3 In #4 10.00 In #1 In #2 In #3 In #4	0-500 0-	OR OR OR OR	Del Del Del Del	N #1	Fun 371 0 0 0 220 371 0 0 0 0 220 281 0 0 0 0 220 341 0 0 0 0 0 220 341 0 0 0 0 0 220 351 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	GEN.TRIP GEN.TRIP OC1 TRIP EF1 TRIP SEF1-S1 TRIP UV1 TRIP	Logic	BOTD	h #1 h #1 h #2 h #3 h #4 h #1 h #4 h #1 h #2 h #3 h #4		tions

4. Relay setting

Setting 1

	Setting	I								
			D-				Default Se	etting (5A rating /	1A rating)	
No.		Name	Rai	nge	Units	Contents	Model	Model	Model	User
			5A rating	1A rating			110	400	420	Setting
-			ű	Ü						Setting
1		APPL-CT		/2P/1P		Application setting of CT		3		
2		APPL-VT	Off/3P	N/3PV		Application setting of VT		3F	? V	
3	S	CTFEN	Off/On/	OPT-On		CTF Enable		C	ff	
4		VTF1EN	Off/On/	OPT-On		VTF1 Enable		C	off	
		VTF2EN		OPT-On		VTF2 Enable				
								Off ALM		
6		CTSVEN		Off/ALM&BLK/ALM Off/ALM&BLK/ALM		AC input imbalance Super Visor Eable				
7	1	VOSVEN	Off / ALM8	BLK/ALM		ditto		AL	М	
8	8	V2SVEN	Off / ALM8	BLK/ALM		ditto		AL	M	
9		MOC1	DT / IEC / IEE	E/US/CON		OC1 Delay Type (if OC1EN=On)	-	P	Ť.	
10		MEF1	DT/IEC/IEE	E/US/CON		EF1 Delay Type (if EF1EN=On)		DT		
11		MSE1	DT/IEC/IEE				DT	31	DT	
						SEF1 Delay Type (if SE1EN=On)				
12		OC1EN	Off/			OC1 Enable		C		
13	3	OC1-DIR	FWD/RI	EV/NON		OC1 Directional Characteristic (if OC1EN=On)		FV	VD O	
14	l.	MOC1C-IEC	NI/M/	E/LTI		OC1 IEC Inverse Curve Type (if MOC1=IEC)		N	II	
15		MOC1C-IEEE	MI/\	/I/El		OC1 IEEE Inverse Curve Type (if MOC1=IEEE)		N.	11	
16		MOC1C-US	CO2/					_		
						OC1 US Inverse Curve Type (if MOC1=US)		V		
17		OC1R	DEF /			OC1 Reset Characteristic (if MOCI=IEEE,orUS)	-	DE		
18		VTF-OC1BLK	Off /	/On		VTF block enable		С	Mf	
19		OC2EN	Off /	On		OC2 Enable	į	С	ff	
20		OC2-DIR	FWD/RI	EV/NON		OC2 Directional Characteristic (if OC2EN=On)	- Tan	FV	VD O	
21		VTF-OC2BLK	Off /					C		
******						VTF block enable				
22		OC3EN	Off /			OC3 Enable		С		
23	8	OC3-DIR	FWD/RI	EV/NON		OC3 Directional Characteristic (if OC3EN=On)		FV	MD	
24		VTF-OC3BLK	Off /	On On	-	VTF block enable		С	ff	
25		OC4EN	Off /	/On		OC4 Enable		С	off .	
26		OC4-DIR	FWD/RI			OC4 Directional Characteristic (if OC4EN=On).		FV		
27		VTF-OC4BLK	Off /			VTF block enable		С		
28	8	OCTP	3POR/2	OUTOF3		OC trip mode (if OC1 or 2 or 3 or 3EN=On)	-	3P	OR	
29	EF .	EF1EN	Off / Or	n/POP	-	EF1 Enable		On		
30		EF1-DIR	FWD/RI	EV/NON		EF1 Directional Characteristic (if EF1EN=On)		FWD		
31		MEF1C-IEC	NI/VI/			EF1 IEC Inverse Curve Type (if MEF1=IEC)		NI		
32		MEF1C-IEEE	MI/\					MI		
						EF1 IEEE Inverse Curve Type (if MEF1=IEEE)				
33		MEF1C-US	CO2/	CO8		EF1 US Inverse Curve Type (if MEF1=US)		CO2		
34	ŀ	EF1R	DEF /	DEP		EF1 Reset Characteristic. (if MEFI=IEEE,orUS)		DEF		
35	5	CTF-EF1BLK	Off /	On On	4	CTF block enable		C	ff	
36		VTF-EF1BLK	Off /	/On		VTF block enable		С	eff	
37		EF2EN	Off / Or	_	,			Off		
					_	EF2 Enable				
38		EF2-DIR	FWD/RI			EF2 Directional Characteristic (if EF2EN=On)		FWD		
39		CTF-EF2BLK	Off /	/On	-	CTF block enable		C	iff	
40)	VTF-EF2BLK	Off /	On		VTF block enable	-	C	ff	
41		EF3EN	Off / Or	1/POP	(EF3 Enable		Off		
42		EF3-DIR	FWD/RI	_				FWD		
						EF3 Directional Characteristic (if EF3EN=On)			uff	
43		CTF-EF3BLK	Off /	$\overline{}$		CTF block enable		С		
44		VTF-EF3BLK	Off /	On .		VTF block enable		С	ff	
45		EF4EN	Off / Or	1/POP	-	EF4 Enable		Off		
46	i	EF4-DIR	FWD/RI	EV/NON		EF4 Directional Characteristic (if EF4EN=On)		FWD		
47		CTF-EF4BLK		'On	-				Mf	
48						CTF block enable		0		
		VTF-EF4BLK		On		VTF block enable			711	
49		CURREV		2/3/4	-	Current reverse detection		Off		
50	SEF	SE1EN	Off/	On	-	SEF1 Enable	On		On	
51		SE1-DIR	FWD/RI	EV/NON		SEF1 Directional Characteristic (if SE1EN=On)	FWD		FWD	
52		MSE1C-IEC	NI/M/			SEF1 IEC Inverse Curve Type (if MSE1=IEC)	NI		NI	
53		MSE1C-IEEE	MI/\				MI		MI	
						SEF1 IEEE Inverse Curve Type (if MSE1=IEEE)				
54		MSE1C-US		CO8		SEF1 US Inverse Curve Type (if MSE1=US)	CO2		CO2	
55		SE1R	DEF /	DEP		SEF1 Reset Characteristic. (if MSEI=IEEE,orUS)	DEF		DEF	
56		SE1S2	Off /	On		SEF1 Stage 2 Timer Enable (if SE1EN=0m)	Off		Off	
57		VTF-SE1BLK		On On		VTF block enable	-	-	Off	
58		SE2EN		On On		SEF2 Enable	Off		Off	
59										
		SE2-DIR	FWD/RI			SEF2 Directional Characteristic (if SE2EN=On)	FWD		FWD	
60		VTF-SE2BLK	Off /	On		VTF block enable	-	-	Off	
61	A	SE3EN	Off /	On On		SEF3 Enable	Off		Off	
62		SE3-DIR	FWD/RI	EV/NON		SEF3 Directional Characteristic (if SE3EN=On)	FWD		FWD	
63		VTF-SE3BLK	Off /						Off	
-						VTF block enable	-			
64		SE4EN	Off /			SEF4 Enable	Off		Off	
65		SE4-DIR	FWD/RI	EV/NON		SEF4 Directional Characteristic (if SE4EN=On)	FWD		FWD	
66		VTF-SE4BLK	Off /	On On		VTF block enable	-	-	Off	
67		RPEN	Off /	On On		Residual Power block Enable.	Off		Off	
_							_		_	

			1			5 () 0		
l l			Range				tting (5A rating / 1A rating)	
No.		Name	· ·	Units	Contents	Model	Model Model	User
			5A rating 1A rating			110	400 420	Setting
68	NOC	NC1EN	Off/On		NOC1 Enable		Off	
69		NC1-DIR	FWD/REV/NON		NOC1 Directional Characteristic (if NC1EN=On)		FWD	
70		CTF-NC1BLK	Off / On		CTF block enable		Off	
71		VTF-NC1BLK	Off/On		VTF block enable		Off	
72		NC2EN	Off/On		NOC2 Enable		Off	
73		NC2-DIR	FWD/REV/NON				FWD	
					NOC2 Directional Characteristic (if NC2EN=On)			
74		CTF-NC2BLK	Off/On		CTF block enable		Off	
75		VTF-NC2BLK	Off/On		VTF block enable		Off	
76	UC	UC1EN	Off/On		UC1 Enable		Off	
77		CTF-UC1BLK	Off / On		CTF block enable		Off	
78		UC2EN	Off/On	-	UC2 Enable		Off	
79		CTF-UC2BLK	Off / On		CTF block enable		Off	
80	Thermal	THMEN	Off/On	-	Thermal OL Enable		Off	
81		THMAEN	Off / On		Thermal Alarm Enable		Off	
82	BCD	BCDEN	Off/On	-			Off	
83	CBF	BTC	Off/On		Broken Conductor Enable	/	Off	-
	CDF				Back-trip control			
84		RTC	Off/DIR/OC		Re-trip control		Off	
85	Cold Load	CLEN	Off/On		Cold Load Protection Enable		Off	
86	Load	CLDOEN	Off/On		Cold Load drop-off Enable		Off	
87	OV	OV1EN	Off / DT / IDMT		OV1 Enable		Off	
88		OV2EN	Off/On		OV2 Enable		Off	
89	UV	UV1EN	Off/DT/IDMT		UV1 Enable		DT	
90		VTF-UV1BLK	Off/On		VTF block enable		Off	
91		UV2EN	Off/On		UV2 Enable	-	Off	
92		VTF-UV2BLK	Off/On				Off	
93		VBLKEN	Off/On		VTF block enable		Off	
-	701				UV Block Enable			
94	ZOV	ZOV1EN	Off / DT / IDMT		ZOV1 Enable		DT	
95		VTF-ZOV1BLK	Off/On		VTF block enable		Off	
96		ZOV2EN	Off/On		ZOV2 Enable		Off	
97		VTF-ZOV2BLK	Off/On		VTF block enable		Off	
98	NOV	NOV1EN	Off / DT / IDMT	-	NOV1 Enable		Off	
99		VTF-NV1BLK	Off / On	-	VTF block enable		Off	
100		NV2EN	Off/On		NOV2 Enable		Off	
101		VTF-NV2BLK	Off/On		VTF block enable		Off	
102	FRQ	FRQ1EN	Off/OF/UF		FRQ1 Enable		Off	
103	11102	FRQZEN	Off/OF/UF				Off	
					FRQ2 Enable			
104		FRQ3EN	Off/OF/UF		FRQ3 Enable		Off	
105		FRQ4EN	Off/OF/UF		FRQ4 Enable		Off	
106	ARC	ARCEN	Off/On		Autoreclosing Enable.		On	
107		ARC-NUM	S1/S2/S3/S4/S5		Reclosing shot max number		S1	
108		COORD-OC	Off/On		OC relay for Co-ordination Enable		Off	
106		COORD-EF	Off / On		EF relay for Co-ordination Enable		Off	
105		COORD-SE	Off/On	-	SEF relay for Co-ordination Enable	Off	Off	
106		OC1-INIT	NA/On/Block	_	Autoreclosing initiation by OC1 enable		NA NA	
107		OC1-TP1	Off / Inst / Set	- 7			SET	
108		OC1-TP2	Off / Inst / Set		QC1 trip mode of 1st trip (if QC1EN=Qn)		SET	
					OC1 trip mode of 2nd trip (if OC1EN=On)			
109		OC1-TP3	Off/Inst/Set		OC1 trip mode of 3rd trip (if OC1EN=On)		SET	
110		OC1-TP4	Off / Inst / Set	-	OC1 trip mode of 4th trip (if OC1EN=On)		SET	
111		OC1-TP5	Off / Inst / Set	~	OC1 trip mode of 5th trip (if OC1EN=On)		SET	
112		OC1-TP6	Off / Inst / Set		OC1 trip mode of 6th trip (if OC1EN=On)		SET	
113		OC2-INIT	NA/On/Block		Autoreclosing initiation by OC2 enable		NA	
114		OC2-TP1	Off / Inst / Set		OC2 trip mode of 1st trip (if OC2EN=On)		SET	
115		OC2-TP2	Off / Inst / Set		OC2 trip mode of 2nd trip (if OC2EN=On)		SET	
116		OC2-TP3	Off / Inst / Set		OC2 trip mode of 3rd trip (if OC2EN=On)		SET	
117		OC2-TP4	Off / Inst / Set				SET	
118					OC2 trip mode of 4th trip (if OC2EN=On)			
		OC2-TP5	Off / Inst / Set		OC2 trip mode of 5th trip (if OC2EN=On)		SET	
119		OC2-TP6	Off / Inst / Set		OC2 trip mode of 6th trip (if OC2EN=On)		SET	
120		OC3-INIT	NA/On/Block		Autoreclosing initiation by OC3 enable		NA	
121		OC3-TP1	Off / Inst / Set		OC3 trip mode of 1st trip (if OC3EN=On)		SET	
122		OC3-TP2	Off / Inst / Set		OC3 trip mode of 2nd trip (if OC3EN=On)		SET	
123		OC3-TP3	Off / Inst / Set		OC3 trip mode of 3rd trip (if OC3EN=On)		SET	
124		OC3-TP4	Off / Inst / Set		OC3 trip mode of 4th trip (if OC3EN=On)		SET	
125		OC3-TP5	Off / Inst / Set		OC3 trip mode of 5th trip (if OC3EN=On)		SET	
126		OC3-TP6	Off / Inst / Set		OC3 trip mode of 6th trip (if OC3EN=On)		SET	
127		OC4-INIT	NA/On/Block				NA NA	
					Autoreclosing initiation by OC4 enable			
128	_	OC4-TP1	Off / Inst / Set		OC4 trip mode of 1st trip (if OC4EN=On)		SET	
129		OC4-TP2	Off / Inst / Set		OC4 trip mode of 2nd trip (if OC4EN=On)		SET	
130		OC4-TP3	Off / Inst / Set		OC4 trip mode of 3rd trip (if OC4EN=On)		SET	
131	7	OC4-TP4	Off / Inst / Set		OC4 trip mode of 4th trip (if OC4EN=On)		SET	
132		OC4-TP5	Off / Inst / Set		OC4 trip mode of 5th trip (if OC4EN=On)		SET	
133		OC4-TP6	Off / Inst / Set		OC4 trip mode of 6th trip (if OC4EN=On)		SET	
134		EF1-INIT	NA/On/Block		Autoreclosing initiation by EF1 enable		NA	
135		EF1-TP1	Off / Inst / Set				SET	
100		L 2000	Oil / II Bit / Get		EF1 trip mode of 1st trip (if EF1EN=On)			

							Default Se	etting (5A rating /	1A rating)	
No.		Name	Rai	nge	Units	Contents	Model	Model	Model	User
			5A rating	1A rating			110	400	420	Setting
136		EF1-TP2		st / Set		EF1 trip mode of 2nd trip (if EF1EN=On)		SET		3200
137		EF1-TP3		st / Set		EF1 trip mode of 3rd trip (if EF1EN=On)		SET		
138		EF1-TP4	Off / In	st / Set		EF1 trip mode of 4th trip (if EF1EN=On)		SET		
139		EF1-TP5	Off / In	st / Set		EF1 trip mode of 5th trip (if EF1EN=On)		SET		
140		EF1-TP6		st / Set		EF1 trip mode of 6th trip (if EF1EN=On)		SET		
141		EF2-INIT		n/Block		Autoreclosing initiation by EF2 enable		NA		
142		EF2-TP1		st / Set		EF2 trip mode of 1st trip (if EF2EN=On)		SET		
143		EF2-TP2		st / Set		EF2 trip mode of 2nd trip (if EF2EN=On)		SET		
144		EF2-TP3		st / Set				SET		
145		EF2-TP4		st / Set		EF2 trip mode of 3rd trip (if EF2EN=On) EF2 trip mode of 4th trip (if EF2EN=On)		SET		•
146		EF2-TP5		st / Set		EF2 trip mode of 4th trip (if EF2EN=Cri) EF2 trip mode of 5th trip (if EF2EN=Cri)		SET		
147		EF2-TP6		st/Set				SET		
148		EF3-INIT		n/Block		EF2 trip mode of 6th trip (if EF2EN=On)		NA NA		
149		EF3-TP1		st / Set		Autoreclosing initiation by EF3 enable		SET		
150		EF3-TP2		st / Set		EF3 trip mode of 1st trip (if EF3EN=On)		SET		
151		EF3-TP3		st/Set		EF3 trip mode of 2nd trip (if EF3EN=On)		SET		
152						EF3 trip mode of 3rd trip (if EF3EN=On)		SET		
153		EF3-TP4		st / Set		EF3 trip mode of 4th trip (if EF3EN=On)		SET		
		EF3-TP5		st / Set		EF3 trip mode of 5th trip (if EF3EN=On)	<u> </u>			
154		EF3-TP6		st / Set		EF3 trip mode of 6th trip (if EF1EN=On)		SET		
155		EF4-INIT		n/Block		Autoreclosing initiation by EF4 enable		NA CET		
156		EF4-TP1		st / Set		EF4 trip mode of 1st trip (if EF4EN=On)		SET		
157		EF4-TP2		st / Set		EF4 trip mode of 2nd trip (if EF4EN=On)		SET		
158		EF4-TP3		st / Set		EF4 trip mode of 3rd trip (if EF4EN=On)		SET		
159		EF4-TP4		st / Set		EF4 trip mode of 4th trip (if EF4EN=On)	_	SET		
160		EF4-TP5		st / Set		EF4 trip mode of 5th trip (if EF4EN=On)		SET		
161		EF4-TP6		st / Set		EF4 trip mode of 6th trip (if EF1EN=On)	,	SET		
162		SE1-INIT		n/Block		Autoreclosing initiation by SEF1 enable	NA		NA	
163		SE1-TP1		st / Set		SEF1 trip mode of 1st trip (if SE1EN≠On)	SET		SET	
164		SE1-TP2		st / Set		SEF1 trip mode of 2nd trip (if SE1EN=On)	SET		SET	
165		SE1-TP3		st / Set		SEF1 trip mode of 3rd trip (if SE1EN=On)	SET		SET	
166		SE1-TP4		st / Set		SEF1 trip mode of 4th trip (if SE1EN=On)	SET		SET	
167		SE1-TP5	Off / In	st / Set		SEF1 trip mode of 5th trip (if SE1EN=On)	SET		SET	
168		SE1-TP6	Off / In	st / Set		SEF1 trip mode of 6th trip (if SE1EN=On)	SET		SET	
169		SE2-INIT	NA/Or	n/Block		Autoreclosing initiation by SEF2 enable	NA		NA	
170		SE2-TP1	Off / In	st / Set		SEF2 trip mode of 1st trip (if SE2EN=On)	SET		SET	
171		SE2-TP2	Off / In	st / Set		SEF2 trip mode of 2nd trip (if SE2EN=On)	SET		SET	
172		SE2-TP3	Off / In	st / Set		SEF2 trip mode of 3rd trip (if SE2EN=On)	SET		SET	
173		SE2-TP4	Off / In	st / Set		SEF2 trip mode of 4th trip (if SE2EN=On)	SET		SET	
174		SE2-TP5	Off / In	st / Set	4	SEF2 trip mode of 5th trip (if SE2EN=On)	SET		SET	
175		SE2-TP6	Off / In	st / Set		SEF2 trip mode of 6th trip (if SE2EN=On)	SET		SET	
176		SE3-INIT	NA/Or	n/Block		Autoreclosing initiation by SEF3 enable	NA		NA	
177		SE3-TP1	Off / In	st/Set		SEF3 trip mode of 1st trip (if SE3EN=On)	SET		SET	
178		SE3-TP2	Off / In	st / Set		SEF3 trip mode of 2nd trip (if SE3EN=On)	SET		SET	
179		SE3-TP3	Off / In	st / Set		SEF3 trip mode of 3rd trip (if SE3EN=On)	SET		SET	
180		SE3-TP4	Off / In	st / Set	(SEF3 trip mode of 4th trip (if SE3EN=On)	SET		SET	
181		SE3-TP5	Off / In	st / Set	-)	SEF3 trip mode of 5th trip (if SE3EN=On)	SET		SET	
182		SE3-TP6	Off / In	st / Set		SEF3 trip mode of 6th trip (if SE3EN=On)	SET		SET	
183		SE4-INIT	NA/Or	n/Block		Autoreclosing initiation by SEF4 enable	NA		NA	
184		SE4-TP1	Off / In	st / Set		SEF4 trip mode of 1st trip (if SE4EN=Cn)	SET		SET	
185		SE4-TP2		st / Set		SEF4 trip mode of 2nd trip (if SE4EN=On)	SET		SET	
186		SE4-TP3		st / Set		SEF4 trip mode of 3rd trip (if SE4EN=On)	SET		SET	
187		SE4-TP4		st / Set		SEF4 trip mode of 4th trip (if SE4EN=On)	SET		SET	
188		SE4-TP5		st / Set		SEF4 trip mode of 5th trip (if SE4EN=On)	SET		SET	
189		SE4-TP6		st / Set		SEF4 trip mode of 6th trip (if SE4EN=On)	SET		SET	
190		EXT-INIT		n/Block		Autoreclosing initiation by External Trip Command enable		NA		
191		UVF		130.0	V	UV(Ph-G) Threshold setting for VTF scheme.		51	1.0	
192	VTF	ZOVF	5.0-		V	ZOV Threshold setting for CTF/VTF scheme.			0.0	
193	CTF	OCDF	0.5(Fixed)	0.1(Fixed)	A	OCD Threshold setting for CTF/VTF scheme.			-	
194		EFF	0.1 - 25.0	0.02 - 5.00	A	EF Threshold setting for CTF/VTF scheme.		1.0/	0.20	
195	OC	ОСӨ		- 95	Degree	OC Characteristic Angle (if OC1 or 2 or 3 or 4EN=On)			45	
196	-	001	0.1 - 25.0	0.02 - 5.00	Α	OC1 Threshold setting (if OC1EN=On)			1.00	
197		TOC1		300.00	s	OC1 Definite time setting (if MOC1=DT)			00	
198		TOC1M		- 1.500		OC1 Time multiplier setting (if MOC1=IEC,IEEE,US)			000	
199		TOC1R		300.0	s	OC1 Definite time reset delay (if OC1R =DEF)			.0	
200		TOC1RM		- 1.500		OC1 Dependent time reset time multiplier (if OC1R=DEP)			000	
201		OC2	0.1 - 25.0	0.02 - 5.00	A	OC2 Threshold setting (if OC2EN=On)			/ 5.00	
202		TOC2		300.00	s	OC2 Definite time setting (if MOC2=DT)			00	
203		OC3	0.1 - 250.0	0.02 - 50.00	A				10.00	
204		TOC3		300.00		OC3 Threshold setting (if OC3EN=On)			00	
205	-	003			S	OC3 Definite time setting (if OC3EN=On)				
206		TOC4	0.1 - 250.0	0.02 - 50.00 300.00	A	OC4 Threshold setting (if OC4EN=On)			/ 20.00 00	
207					S	OC4 Definite time setting (if OC4EN=On)				
		OC1-k		30.000		Configurable IDMT Curve settig of CC1.			000	
208		OC1-α	0.00	- 5.00		ditto		0.1	00	

	ı — —		Ι				D (110	W. /FA I. /	44	ı	7
No.		Nome	Ra	nge	Units	Contents		etting (5A rating /		Lloor	1
INO.		Name	5A+:	44	UIIIS	Colletis	Model	Model	Model	User	-
~~~		004.0	5A rating	1A rating			110	400	420	Setting	4
209		OC1-C		- 5.000		ditto			000		4
210		OC1-kr		30.000		ditto			000		-
211		OC1-β		- 5.00		ditto	-		.00		d
212	EF	EFθ		- 95	Degree	EF Characteristic Angle (if EF1 or 2 or 3 or 4EN=On)		-45			4
213		EFV		100.0	V	EF ZPS voltage level (if EF1 or 2 or 3 or 4EN=On)		3.0			_
214		EF1	0.1 - 25.0	0.02 - 5.00	Α	EF1 Threshold setting (if EF1EN=On)		1.5 / 0.30			_
215		TEF1		300.00	S	EF1 EFinite time setting. (if MEF1=DT)		1.00			
216		TEF1M		- 1.500		EF1 Time multiplier setting (if MEF1=IEC,IEEE,US)		1.000			
217		TEF1R		300.0	s	EF1 EFinite time reset delay. (if EF1R =DEF)		0.0			
218		TEF1RM	0.010	- 1.500		EF1 Dependent time reset time multiplier. (if EF1R=DEP)		1.000		~	
219		EF2	0.1 - 25.0	0.02 - 5.00	Α	EF2 Threshold setting (if EF2EN=On)		15.0 / 3.00			
220		TEF2	0.00 -	300.00	S	EF2 EFinite time setting. (if MEF2=DT)		1.00			
221		EF3	0.1 - 250.0	0.02 - 50.00	Α	EF3 Threshold setting (if EF3EN=On)		25.0 / 5.00			
222		TEF3	0.00 -	300.00	s	EF3 EFinite time setting. (if EF3EN=On)		1.00			
223		EF4	0.1 - 250.0	0.02 - 50.00	A	EF4 Threshold setting (if EF4EN=On)		50.0 / 10.00			
224		TEF4	0.00-	300.00	s	EF4 EFinite time setting. (if EF4EN=On)		1.00	*		
225		TREBK	0.00 -	10.00	S	Current reverse blocking time		0.10			-
226		EF1-k		30.000		Configurable IDMT Curve settig of EF1.		0.000			-
227		EF1-α		- 5.00		ditto		0.00			1
228		EF1-C		- 5.000		ditto		0.000			-
229		EF1-kr		30.000				0.000			-
230						ditto					-
	OFF	EF1-β		- 5.00	 D	ditto		0.00			4
231	SEF	SEO		- 95	Degree	SEF Characteristic Angle (if DEF1 or 2 or 3 or 4EN=On)	0		0		-
232		SEV		100.0	V	SEF ZPS voltage level (if DEF1 or 2 or 3 or 4EN=On)	3.0		3.0		_
233		SE1	0.01 - 1.00	0.002 - 0.200	Α	SEF1 Threshold setting (if SE1EN=On)	0.05 / 0.010		0.05 / 0.010		_
234		TSE1		300.00	S	SEF1 Definite time setting. (if MSE1=DT)	1.00		1.00		J
235		TSE1M	0.010	- 1.500		SEF1 Time multiplier setting (if MSE1=IEC, IEEE, US)	1.000		1.000		
236		TSE1R	0.0 -	300.0	S	SEF1 Definite time reset delay. (if SE1R =DEF)	0.0		0.0		1
237		TSE1RM	0.010	- 1.500		SEF1 Dependent time reset time multiplier. (if SE1R=DEP)	1.000		1.000		
238		TS1S2	0.00 -	300.00	S	SEF1 Stage 2 definite timer settings. (if SE1EN=0n and SE1S2=On)	1.00		1.00		
239		SE2	0.01 - 1.00	0.002 - 0.200	Α	SEF2 Threshold setting (if SE2EN=On)	0.05 / 0.010		0.05 / 0.010		-
240		TSE2		300.00	s	SEF2 Definite time setting. (if MSE2=DT)	1.00		1.00		-
241		SE3	0.01 - 1.00	0.002 - 0.200	A	SEF3 Threshold setting (if SE3EN=On)	0.05 / 0.010		0.05 / 0.010		-
242		TSE3		300.00	s		1.00		1.00		-
243		SE4	0.00 -	0.002 - 0.200	A	SEF3 Definite time setting. (if SE3EN=On)	0.05/0.010		0.05/0.010		-
243						SEF4 Threshold setting (if SE4EN=On)					-
		TSE4		300.00	S	SEF4 Definite time setting. (if SE4EN=On)	1.00		1.00		
245		RP	0.00 - 100.00	0.00 - 20.00	W	Residual Power Threshold.	0.00 / 0.00		0.00 / 0.00		
246		SE1-k		30.000		Configurable IDMT Curve settig of SEF1.	0.000		0.000		_
247		SE1-α	0.00	- 5.00		ditto	0.00		0.00		
248		SE1-C	0.000	- 5.000		ditto	0.000		0.000		
249		SE1-kr	0.000 -	30.000		ditto	0.000		0.000		
250		SE1-β	0.00	- 5.00		ditto	0.00		0.00		-
251	NOC	NCθ	-95	- 95	Degree	NOC Characteristic Angle (if NC1 or 2 or 3 or 4EN=On)			45		1
252		NCV	0.5 -	25.0	V	NOC NPS voltage level (if NC1 or 2 or 3 or 4EN=On)		3	3.0		
253		NC1	0.5 - 10.0	0.10 - 2.00	A	NOC1 Threshold setting (if NC1EN=On)		2.0	0.40		-
254		TNC1	0.00-	300,00	s	NOC1 Definite time setting. (if MNC1=DT)		1.	.00		
255		NC2	0.5 - 10.0	0.10 - 2.00	A	NOC2 Threshold setting (if NC2EN=On)			0.20		-
256		TNC2		300.00	S	NOC2 Definite time setting. (if NC2EN=On)			.00		ł
257	UC	UC1	0.5- 10.0	0.10 - 2.00	A				0.20	l 	1
258	- 50	TUC1	_	300.00					.00		-
259			0.5- 10.0		S	UC1 Definite time setting. (if UC1EN=On)					-
		UC2		0.10 - 2.00	A	UC2 Threshold setting (if UC2EN=On)	-		0.40		-
260	Thomas	TUC2		300.00	S	UC2 Definite time setting. (if UC2EN=On)			.00		4
261	Thermal	THM	2.0 - 10.0	0.40 - 2.00	A	Thermal overload setting (if OLTEN=On)			1.00		-
262		THMIP	0.0 - 5.0	0.00 - 1.00	A	Pre Current value (if OLTEN=On)			0.00		_
263		TTHM	0.5-		min	Thermal Time Constant. (if OLTEN=On)			0.0		_
264		THMA		- 99	%	Thermal alarm setting. (if OLTEN =On & ALTEN=On)			30		
265	BCD	BCD	0.10	- 1.00		Broken Conductor Threshold setting. (if BCDEN=On)	-	0.	20		
266		TBCD	,	300.00	S	Broken Conductor Definite time setting. (if BCDEN=On)		1.	.00		
267	CBF	CBF	0.5 - 10.0	0.10 - 2.00	Α	CBF Threshold setting. (if CBFEN=On)		2.5	0.50		1
268	1	IBIC	0.00-	300.00	S	Back trip Definite time setting		0.	.50		-
269		TRTC	0.00-	300.00	s	Re-trip Definite time setting		0.	.40		Ī
270	Cold	OC1	0.1 - 25.0	0.02 - 5.00	Α	OC1 Threshold setting in CLP mode.			/200		1
271	Load	OC2	0.1 - 25.0	0.02 - 5.00	A	OC2 Threshold setting in CLP mode.			/ 5.00		1
272		OC3	0.1 - 250.0	0.02 - 50.00	A	OC3 Threshold setting in CLP mode.			/ 20.00		1
273		OC4	0.1 - 250.0	0.02 - 50.00	A				/ 40.00		1
274		EF1	0.1 - 25.0	0.02 - 5.00	A	OC4 Threshold setting in CLP mode.			/40.00		
						EF1 Threshold setting in CLP mode.					
275		EF2	0.1 - 25.0	0.02 - 5.00	A	EF2 Threshold setting in CLP mode.			/5.00		
276		EF3	0.1 - 250.0	0.02 - 50.00	Α	EF3 Threshold setting in CLP mode.			/ 20.00		_
277	3	EF4	0.1 - 250.0	0.02 - 50.00	Α	EF4 Threshold setting in CLP mode.		200.0	/ 40.00		
278	7	SE1	0.01 - 1.00	0.002 - 0.200	Α	SEF1 Threshold setting in CLP mode.		-	0.10 / 0.020		J
279		SE2	0.01 - 1.00	0.002 - 0.200	Α	SEF2 Threshold setting in CLP mode.		-	0.10 / 0.020		J
280		SE3	0.01 - 1.00	0.002 - 0.200	Α	SEF3 Threshold setting in CLP mode.		-	0.10 / 0.020		J
281		SE4	0.01 - 1.00	0.002 - 0.200	Α	SEF4 Threshold setting in CLP mode.	-	-	0.10 / 0.020		1

		I	1		1	I	D ( 110	/54 /	44 (* )	
No.		Nama	Ra	nge	Units	Contents		etting (5A rating /		User
INU.		Name	5A antion	44	Units	Colletis	Model	Model	Model	
2000		NO	5A rating 0.5 - 10.0	1A rating			110	400	420	Setting
282		NC1		0.10 - 2.00	A	NOC1 Threshold setting in CLP mode.			0.80	
283		NC2	0.5 - 10.0	0.10 - 2.00	Α	NOC2 Threshold setting in CLP mode.			0.40	
284		BCD		- 1.00		Broken Conductor Threshold setting in CLP mode.			40	
285		TCLE		0000	S	Cold load enable timer. (if CLEN=On)		10		
286		TCLR		0000	s	Cold load reset timer. (if CLEN=On)		10		
287		ICLDO	0.5 - 10.0	0.10 - 2.00	Α	Cold load drop-out threshold setting. (if CLDOEN=On)		2.5/	0.50	
288		TCLDO	0.00 -	100.00	s	Cold load drop-out timer. (if CLDOEN=1)		0.	00	
289	OV	OV1	10.0 -	200.0	V	OV1 Threshold setting.		12	0.0	
290		TOV1	0.00 -	300.00	s	OV1 Definite time setting. Display if [OV1EN] = 1.		1.	00	
291		TOV1M	0.05-	100.00		OV1 Time multiplier setting. Display if [OV1EN] = 2.		1.	00	
292		TOV1R	0.0-	300.0	s	OV1 Definite time reset delay.		0	.07	
293		OV1DPR		- 98	%	OV1 DO/PU ratio		9		
294		OV2		200.0	V			14		
295		TOV2		300.00	s	OV2 Threshold setting.			00	
296					%	OV2 Definite time setting.				
		OV2DPR		- 98		OV2 DO/PU ratio			5	
297	UV	UV1		130.0	V	UV1 Threshold setting.			0.0	
298		TUV1		300.00	S	UV1 Definite time setting. Display if [UV1EN] = 1.			00	
299		TUV1M	0.05-	100.00		UV1 Time multiplier setting. Display if [UV1EN] = 2.		1.	00	
300		TUV1R	0.0-	300.0	s	UV1 Definite time reset delay.	A	0	.0	
301		UV2	5.0-	130.0	V	UV2 Threshold setting.	-	40	0.0	
302		TUV2	0.00-	300.00	s	UV2 Definite time setting.	7.7	1.	00	
303		VBLK		20.0	V	UV Blocking threshold	-		0.0	
304	ZOV	ZOV1		130.0	V	ZOV1 Threshold setting.	7	20.0		
305	200	TZOV1		300.00	s			1.00		
						ZOV1 Definite time setting. Display if [ZOV1EN] = 1.				
306		TZOV1M		100.00		ZOV1 Time multiplier setting. Display if [ZOV1EN] = 2.		1.00		
307		TZOV1R		300.0	S	ZOV1 Definite time reset delay.		0.0		
308		ZOV2		130.0	V	ZOV2 Threshold setting.		40.0		
309		TZOV2	0.00 -	300.00	s	ZOV2 Definite time setting.		1.00		
310	NOV	NOV1	1.0-	130.0	V	NOV1 Threshold setting.		20	0.0	
311		TNOV1	0.00-	300.00	s	NOV1 Definite time setting. Display if [MNOV1] = 0.		1.	00	
312		TNOV1M	0.05-	100.00		NOV1 Time multiplier setting. Display if [MNOV1] = 1.		1.	00	
313		TNOV1R	00-	300.0	s	NOV1 Definite time reset delay.		0	0	
314		NOV2		130.0	V	NOV2 Threshold setting.			0.0	
315		TNOV2		300.00						
					S	NOV2 Definite time setting.			00	
316	FRQ	FRQ1		- +10.00	Hz	FRQ1 Threshold setting.		-1.		
317		TFRQ1	0.00 -	300.00	S	FRQ1 Definite time setting.		1.	00	
318		FRQ2	-10.00 -	+10.00	Hz	FRQ2 Threshold setting.		-1.	00	
319		TFRQ2	0.00 -	300.00	s	FRQ2 Definite time setting.		1.	00	
320		FRQ3	-10.00 -	- +10.00	Hz	FRQ3 Threshold setting.		-1.	00	
321		TFRQ3	0.00-	300.00	s	FRQ3 Definite time setting.		1.	00	
322		FRQ4	-10.00-	- +10.00	Hz	FRQ4 Threshold setting.		-1.	m	
323		TFRQ4		300.00	S	FRQ4 Definite time setting.			00	
324		FVBLK		100.0	V				0.0	
	ADO			600.0	_	UV Blocking threshold			2.0	
325	ARC	TRDY			S	Reclaim timer		60.0		
326		TD1		300.00	Ś	1st shot Dead timer of Stage1		10.00		
327		TD2		300.00	S	2nd shot Dead timer of Stage1		10.00		
328		TD3	0.01 -	300.00	S	3rd shot Dead timer of Stage1		10.00		
329		TD4	0.01 -	300.00	S	4th shot Dead timer of Stage1		10.00		
330		TD5	0.01 -	300.00	S	5th shot Dead timer of Stage1		10.00		
331		TW	0.01 -	10.00	s	Out put pulse timer		2.00		
332		TSUC	0.0-	600.0	s	Autoreclosing Pause Time after manualy close		3.0		
333		TRCOV		600.0	S	Autoreclosing Recovery time after Final Trip		10.0		
334		TARCP		600.0	s	Autoreclosing Pause Time after manually close		10.0		
335		TRSET		300.00	s	ARC reset time in CB closing mode.		3.00		
336		OC	0.1 - 250.0	0.02 - 50.00	A				1.00	
337		EĘ (	0.1 - 250.0	0.02 - 50.00	A	For Co-ordination		1.5/0.30	1.00	
		SE				ditto	0.05 / 0.040		0.05 / 0.040	
338	_	_	0.01 - 1.00	0.002 - 0.200	A	ditto	0.05 / 0.010		0.05 / 0.010	
339	FL	X1	0.00 - 199.99	0.0 - 999.9	OHM	ditto		2.00		
340		X0	0.00 - 199.99	0.0 - 999.9	OHM	ditto			34.0	
341	4	R1	0.00 - 199.99	0.0 - 999.9	OHM	ditto			/ 1.0	
342		R0	0.00 - 199.99	0.0 - 999.9	OHM	ditto		0.70	/ 3.5	
343		Kab	80-	120	%	ditto		10	00	
344		Kbc	80-	120	%	ditto		10	00	
345		Kca		120	%	ditto			00	
346		Ka		120	%	ditto			00	
347		Kb		120	%				00	
						ditto				
348		Kc		120	%	ditto		10		
349		LINE		399.9	km	ditto			0.0	
350	Parameters	OCCT		0000		Phase CT ratio		40	00	
351		EFCT	1-20	0000		Residual CT ratio		400		
352		SEFCT	1-20	0000		SEF CT ratio	400		400	
353		PVT	1-20	0000		Phase VT ratio		10	00	
354		RVT		20000		Residual VT ratio		100		
355	System	Line name		d by user		Line name		Specified by user		
356		Active gp.		- 4				1		
300	, wo continue	, ιου νο gp.	1			Active group				

## Setting 2

No.	Name	Ra	nge	Units	Contents	Model	ting (5A rating Model	Model	User
<b>4</b> 0.	Name	5A rating	1A rating	Orinto	Contonio	110	400	420	Settin
1 Passwd	Setting Password	Grading	- Wilding	_	Password for Setting menu	110	0000	120	Octui
2 Notes	Plant name		-	_	Plant name		no-name		
3	Description		-		Description		no-data		
4 Records	TCAEN	Off	/ On	_	Trip CounterAlarm Enable		Off		
5	TCSPEN	Off / On	/ Opt-On	-	Trip Circuit Supervision Enable		Off		7
6	CBSMEN		/ On	-	CB conditon super visor enable		Off		
7	ΣΙγΑΕΝ	Off	/ On		ΣΙ'y Alarm Enable		Off		_
8	OPTAEN	Off	/ On	_	Operate Time Alarm Enable		Off		-
9	TCALM		0000	_	Trip Count Alarm Threshold		10000		
10	ΣlyALM		10000	E6	ΣΙ'γ Alarm		10000		
11	YVALUE		- 2.0		Y value		2.0		
12	OPTALM		5000	ms	Operate Time Alarm Threshold		1000		
13	Fault locator		/ On	-	Fault Locator Enable		Off		
14	Time		- 3.0	s	Record time		2.0	7	
15	OC	0.1 - 250.0	0.02 - 50.00	A	oc	- 🛦		/ 2.00	
16	EF	0.1 - 250.0	0.02 - 50.00	A	EF	-	3.0 / 0.60	2.00	
17	SEF	0.1 - 250.0	0.02 - 0.200	A	SEF	1.00 / 0.200	3.070.00	1.00 / 0.200	
						1.007 0.200		1.00 / 0.200	
18 10	NC OV	0.5 - 10.0	0.10 - 2.00	A V	NOC OV	-		0.40	
19	OV		200.0					0.0	
20	UV		130.0	V	UV	- '		0.0	
21	ZOV		130.0	V	ZOV		20.0		
22	NOV		130.0	V	NOV	-		0.0	
23	Trip		/ On		Disturbance trigger Trip		On		
24	BI		/ On	-	Disturbance trigger BI		On		
25	OC		/ On		Disturbance trigger OC			)n	
26	EF	Off	/ On	-	Disturbance trigger EF		On		
27	SEF	Off	/ On	-	Disturbance trigger SEF	On		On	
28	NC	Off	/ On	-	Disturbance trigger NC	-	С	)n	
29	OV	Off	/ On	-	Disturbance trigger OV	-	С	)n	
30	UV	Off	/ On	-	Disturbance trigger UV		С	)n	
31	ZOV	Off	/ On	_	Disturbance trigger ZOV		On		
32	NOV	Off	/ On	_	Disturbance trigger NOV	_	С	)n	
33	SIG1		500		Disturbance record binary signal #1	(Refer to	the "Disturband		
34	SIG2		500		Disturbance record binary signal #2	(	ditto	,	
35	SIG3		500	_	Disturbance record binary signal #3		ditto		
36	SIG4		500		Disturbance record binary signal #4		ditto		
37	SIG5		500	_	Disturbance record binary signal #5		ditto		
38	SIG6		500	_	Disturbance record binary signal #6		ditto		
39	SIG7		500	/	Disturbance record binary signal #7		ditto		
40	SIG8		500		Disturbance record binary signal #8		ditto		
41	SIG9		500	_	Disturbance record binary signal #9		ditto		
42	SIG10				Disturbance record binary signal #10				
			500	_	1 -		ditto		
43	SIG11		500	-	Disturbance record binary signal #11		ditto		
44	SIG12		500	1	Disturbance record binary signal #12		ditto		
45	SIG13		500	-	Disturbance record binary signal #13		ditto		
46	SIG14		500	-	Disturbance record binary signal #14		ditto		
47	SIG15		500	-	Disturbance record binary signal #15		ditto		
48	SIG16		500	-	Disturbance record binary signal #16		ditto		
49	SIG17		500	-	Disturbance record binary signal #17		ditto		
50	SIG18		500	_	Disturbance record binary signal #18		ditto		
51	SIG19		500	-	Disturbance record binary signal #19		ditto		
52	SIG20	_	500	-	Disturbance record binary signal #20		ditto		
53	SIG21	0-	500	-	Disturbance record binary signal #21		ditto		
54	SIG22	0-	500	1	Disturbance record binary signal #22		ditto		
55	SIG23	0-	500	-	Disturbance record binary signal #23		ditto		
56	SIG24	0-	500	-	Disturbance record binary signal #24		ditto		
57	SIG25	0-	500	-	Disturbance record binary signal #25		ditto		
58	SIG26	0 -	500	_	Disturbance record binary signal #26		ditto		
59	SIG27		500	_	Disturbance record binary signal #27		ditto		
60	SIG28		500	_	Disturbance record binary signal #28		ditto		
61	SIG29		500	_	Disturbance record binary signal #29		ditto		
62	SIG30		500	_	Disturbance record binary signal #30		ditto		
63	SIG31		500		Disturbance record binary signal #30		ditto		
63 64	SIG32		500	_	Disturbance record binary signal #31 Disturbance record binary signal #32		ditto		
				<del>-</del>			1		
65	HDLC		32		Address for RSM100		2		
66	IEC		254		Address for IEC103				
67	IECB1		500	ļ	IEC user specified signal 1		1		ļ
	· IEODO		500		IEC user specified signal 2	i	2		•
68	IECB2				·				
	IECB2 IECB3 IECB4	0 -	500 500		IEC user specified signal 3 IEC user specified signal 4		3		

				I		Default Set	tting (5A rating	/ 1A rating)	I
No.		Name	Range	Units	Contents	Model	Model	Model Model	User
	l	ranc	5A rating 1A rating			110	400	420	Setting
71		IECGT	0-7		IEC Trip A phase		1		County
72	, ,	IECAT	0-7		IEC Trip B phase		1		
73		IECBT	0-7		IEC Trip C phase		1		-
74	, ,	IECCT	0-7		IEC General Trip		1		
75	, ,	IECE1	0 - 500		IEC usr event 1		0		
76	, ,	IECE2	0 - 500		IEC usr event 2		0		
77	, ,	IECE3	0 - 500		IEC usr event 3		0		
78	, ,	IECE4	0 - 500		IEC usr event 4		0		
79	, ,	IECE5	0 - 500		IEC usr event 5		0		
80	, 1	IECE6	0 - 500		IEC usr event 6		0		
81	, 1	IECE7	0 - 500		IEC usr event 7		0		
82	, ,	IECE8	0 - 500		IEC usr event 8		0		
83	, 1	IECI1	0 - 255		IEC usr INF 1		0		
84	, ,	IECI2	0 - 255		IEC usr INF 2		0		
85	,	IECI3	0 - 255		IEC usr INF 3		0	_	
86	, ,	IECI4	0 - 255		IEC usr INF 4		0	7	
87	, }	IECI5	0 - 255		IEC usr INF 5		0		
88	.	IECI6	0 - 255		IEC usr INF 6		0		
89	, )	IECI7	0 - 255		IEC usr INF 7		0		
90	, ,	IECI7	0 - 255		IEC usr INF 8		0		<del> </del>
91	$\overline{}$	Protocol	HDLC/IEC		0.01.6		HDLC(0)		
92	,	232C	9.6/19.2/57.6		Switch for communications ditto	7			<b> </b>
	,						9.6(0)		
93	,	IECBLK	9.6/19.2		ditto	_	19.2(1)		
94	, ,	IECBLK IECNFI	Normal/Blocked		ditto		Normal(0)		<b> </b>
95			1.2/2.4		ditto		2.4(1)		
96		IECNFV	1.2/2.4		ditto		1.2(0)		
97	ı	IECNFP	1.2/2.4		ditto		2.4(1)		
98		IECNFf	1.2/2.4		ditto		1.2(0)		
99		IECFL	Prim/Second/km		ditto		Prim(0)		
100		IECGI1	No/Yes		IEC event type setting 1		No(0)		
101	ı	IECGI2	No/Yes		IEC event type setting 2		No(0)		
102		IECGI3	No/Yes		IEC event type setting 3		No(0)		
103	ı	IECGI4	No/Yes		IEC event type setting 4		No(0)		
104	ı	IECGI5	No/Yes		IEC event type setting 5		No(0)		
105	ı	IECGI6	No/Yes		IEC event type setting 6		No(0)		
106	ı	IECGI7	No/Yes		IEC event type setting 7		No(0)		
107		IECGI8	No/Yes		IEC evnet type setting 8		No(0)		
108		BI1 comm.	None/Operate/Reset/Both		BI 1 command trigger setting		Both(3)		
109	ı	Bl2 comm.	None/Operate/Reset/Both		BI 2 command trigger setting		Both(3)		
110		BI3 comm.	None/Operate/Reset/Both		BI 3 command trigger setting		Both(3)		
111	ı	Bl4 comm.	None/Operate/Reset/Both		BI 4 command trigger setting		Both(3)		
112	ı	BI5 comm.	None/Operate/Reset/Both		BI 5 command trigger setting		Both(3)		
113	ı	BI6 comm.	None/Operate/Reset/Both		BI 6 command trigger setting	Both(3)	-	-	
114	ı	BI7 comm.	None/Operate/Reset/Both		BI 7 command trigger setting	Both(3)	-	-	
115		BI8 comm.	None/Operate/Reset/Both		BI 8 command trigger setting	Both(3)		-	
116		Alarm1 Text	Specified by user		Alarm1 Text		ALARM 1		
117	, [	Alarm2 Text	Specified by user		Alarm2 Text		ALARM 2		
118	, [	Alarm3 Text	Specified by user		Alarm3 Text		ALARM 3		
119	_i [	Alarm4 Text	Specified by user		Alarm4 Text		ALARM 4		
120	, [	BI1PUD	0.00 - 300.00	S	Binary Input 1 Pick-up delay		0.00		
121	, [	BI1DOD	0.00 - 300.00	S	Binary Input 1 Drop-off delay		0.00		
122	, ,	BI2PUD	0.00 - 300.00	S	Binary Input 2 Pick-up delay		0.00		
123	, [	BI2DOD	0.00 - 300.00	S	Binary Input 2 Drop-off delay		0.00		
124		BI3PUD	0.00 - 300.00	s	Binary Input 3 Pick-up delay		0.00		
125	, /	BI3DOD	0.00 - 300.00	s	Binary Input 3 Drop-off delay		0.00		
126	, 1	BI4PUD	0.00 - 300.00	S	Binary Input 4 Pick-up delay		0.00		
127	, 1	BI4DOD	0.00 - 300.00	s	Binary Input 4 Drop-off delay		0.00		
128	,	BI5PUD	0.00 - 300.00	s	Binary Input 5 Pick-up delay		0.00		
129	, ,	BI5DOD	0.00 - 300.00	s	Binary Input 5 Drop-off delay		0.00		
130	, ,	BI6PUD	0.00 - 300.00	s	Binary Input 6 Pick-up delay	0.00	1	-	
131		BI6DOD	0.00 - 300.00	S	Binary Input 6 Drop-off delay	0.00		_	
132	, )	BIZPUD	0.00 - 300.00	S	Binary Input 7 Pick-up delay	0.00		_	
133		BI7DOD	0.00 - 300.00	s	Binary Input 7 Drop-off delay	0.00		_	1
134		BI8PUD	0.00 - 300.00	s	Binary Input 8 Pick-up delay	0.00		-	
135		BI8DOD	0.00 - 300.00	s	Binary Input 8 Drop-off delay	0.00		<b></b>	
	Repeat I	,	from Binary Input 2 to Binary	<u> </u>					
136	7	BI1SNS	Norm/Inv	,	Binary Input 1 Sense	1	Normal		
137	-	BI1SGS	Off/1/2/3/4		Binary Input 1 Settings Group Select		Off		1
138	,	OC1BLK	Off/On		OC1 Block			Off	
139	, )	OC2BLK	Off/On		OC2 Block			Off	
140	, ,	OC3BLK	Off/On		OC3 Block	_		Off	
140		COUDLIN	On/On		O O O DIOUN			Z11	ı

No.		Name	Range	Units	Contents	Default Set Model	tting (5A rating Model	/ 1A rating) Model	User
140.		Name	5A rating 1A rating	Orinto	Contonio	110	400	420	Setting
141		OC4BLK	Off/On		OC4 Block	-	C		County
142		EF1BLK	Off/On		EF1 Block		Off		
143		EF2BLK	Off/On		EF2 Block		Off		
144		EF3BLK	Off/On		EF3 Block		Off		
145		EF4BLK	Off/On		EF4 Block		Off		
146		EF1PER	Off/On		EF1 Permission		Off		
147		EF2PER	Off/On		EF2 Permission		Off		
148		EF3PER	Off/On		EF3 Permission		Off		
149	-	EF4PER	Off/On		EF4 Permission	0"	Off	0"	•
150 151	-	SE1BLK SE2BLK	Off/On Off/On		SEF1 Block SEF2 Block	Off Off	-	Off	
152	-	SE3BLK	Off/On		SEF3 Block	Off		Off	
153	<b>H</b>	SE4BLK	Off/On		SEF4 Block	Off		Off	
154	Ī	NC1BLK	Off/On		NC1 Block	-	0	_	
155	l l	NC2BLK	Off/On		NC2 Block	-		ff	
156		UC1BLK	Off/On		Undercurrent 1 Block	-	C	ff	
157		UC2BLK	Off/On		Undercurrent 2 Block	-	0	ff	
158		CBFBLK	Off/On		CBF Block	Į.	0	ff	
159		THMBLK	Off/On		Thermal Protection Block	ł	0	ff	
160		THMABLK	Off/On		Thermal Alarm Block		0	ff	
161		BCDBLK	Off/On		Broken Conductor Protection Block	-	0	ff	
162		OV1BLK	Off/On		OV1 Block	1	0		
163		OV2BLK	Off/On		OV2 Block	-	О		
164		UV1BLK	Off/On		UV1 Block	-	0		
165	-	UV2BLK	Off/On		UV2 Block	-	0	ff	
166	-	ZOV1BLK	Off/On		ZOV1 Block		Off		
167 168	-	ZOV2BLK	Off/On		ZOV2 Block NOV1 Block	_	Off	ш	
169	-	NOV1BLK NOV2BLK	Off/On Off/On		NOV2 Block	-	0		
170	-	FRQ1BLK	Off/On		FRQ1 Block		0		
171	F	FRQ2BLK	Off/On		FRQ2 Block	_	0		
172	1	FRQ3BLK	Off/On		FRQ3 Block		O		
173		FRQ4BLK	Off/On		FRQ4 Block	_	0		
174	İ	ARCBLK	Off/On		Autoreclose Block		Off		
175	Ī	ARCRDY	Off/On		Autoreclose Ready		Off		
176	Ī	ARCINI	Off/On		Autoreclose Initiation		Off		
177		MNLCLS	Off/On		Manual Close		Off		
178		ARCNA	Off/On		Autoreclose Not Applicated		Off		
179		CTFBLK	Off/On		CTF-Block	-	0	ff	
180		VTFBLK	Off/On		VTF Block	-	0	ff	
181		CTFEXT	Off/On		External CTF	-	0		
182		VTFEXT	Off/On		External VTF	-	0	ff	
183	-	EXTAPH	Off/On		External Trip - Aphase		Off		
184	-	EXTBPH	Off/On		External Trip - Bphase		Off		
185	-	EXTCPH EXT3PH	Off/On Off/On		External Trip - Cphase  External Trip - 3phase		Off Off		
186 187	-	TCFALM	Off/On		Trip Circuit Fail Alarm		Off		
188	-	CBOPN	Off/On		Circuit Breaker Open		Off		
189	l t	CBCLS	Off/On	<b>&gt;</b>	Circuit Breaker Close		Off		
190		RMTRST	Off/On		Remote Reset		Off		
191		SYNCLK	Off/On		Synchronize clock		Off		
192	Ī	STORCD	Off/On		Store Disturbance Record		Off		
193		Alarm1	Off/On		Alarm screen 1.		Off		
194		Alarm2	Off/On		Alarm screen 2.		Off		
195		Alarm3	Off/On		Alarm screen 3.		Off		
196		Alarm4	Off/On		Alarm screen 4.		Off		
			ing Switches from LED 2 to L	ED3.					
197		Logic	OR/AND		LED1 Logic Gate Type		OR		
198		Reset	Inst/Latch		LED1 Reset operation		Inst		
199		In #1	0 - 500		LED Functions		0		
200		In #2	0 - 500		ditto		0		
201		In #3	0 - 500		ditto		0		
202		In #4 Repeat Follow	0 - 500 wing Switches for IND2.		ditto		0		
202		Repeat Folio	Inst/Latch	-	IND1 Reset operation		Inst		
203 204		BIT1	0 - 500		Virtual LED		0		
205		BIT2	0 - 500		ditto		0		
205 206		BIT3	0 - 500		ditto		0		
207		BIT4	0 - 500		ditto		0		
208		BIT5	0 - 500		ditto		0		
209	İ	BIT6	0 - 500		ditto		0		
210		BIT7	0 - 500		ditto		0		
210			0 - 500		ditto		0		

			De				Default Se	etting (5A rating /	1A rating)	4
No.		Name	r\c	ange	Units	Contents	Model	Model	Model	User
			5A rating	1A rating			110	400	420	Setting
212		TermA	0-	500		Logic circuit Functions		0		
213		TermB	0-	500		ditto		0		
214	Status	Display	Pri/Se	c/Pri-A		metering		Primary		
215		Time sync.	Off/BI/F	RSM / IEC		time sync source		Local		
216		Power	Send/	Receive				Send		
217		Current	Lag	/Lead				Lead		
218	Serial	Serial No.		-		Serial No.		no-No		
219		Main ROM No.		-		Main ROM Information		no-name		
220		Relaytype all		-		Relay type all		no-name		
		Repeat Followi	ng Switches for	BO2-BO7						
221	Binary	Logic	OR	/AND		BO logic	S	ee BO setting sh	eet	
222	Output	Reset	INS/DL	/DW/LAT		BO time delay		ditto		
223		ln#1	0-	500		BO signal.		ditto		
224		ln#2	0-	500		ditto		ditto		
225		ln#3	0-	500		ditto		ditto		
226		In#4	0-	500		ditto		ditto		
227		TBO	0.00	- 10.00		BO delaytimer		ditto		

#### 5. Disturbance record setting

				Default setting								
Name	Range	Unit		110		400		420	Setting			
INCITIC	range	Offic	NO.	Signal name	NO.	Signal name	NO.	Signal name				
SIG1	0 - 500	_	131	EF1	101	OC1-A	101	OC1-A				
SIG2	0 - 500	_	281	EF1 TRIP	102	OC1-B	102	OC1-B				
SIG3	0 - 500	_	141	SEF1	103	OC1-C	103	OC1-C				
SIG4	0 - 500	_	291	SEF1-S1 TRIP	261	OC1 TRIP	261	OC1 TRIP	<b>A</b>			
SIG5	0 - 500	_	211	ZOV1	131	EF1	131	EF1				
SIG6	0 - 500	_	351	ZOV1 TRIP	281	EF1 TRIP	281	EF1 TRIP				
SIG7	0 - 500	_	0		201	UV1-A	141	SEF1				
SIG8	0 - 500	_	0		202	UV1-B	291	SEF1-S1 TRIP				
SIG9	0 - 500	_	0		203	UV1-C	201	UV1-A				
SIG10	0 - 500	_	0		341	UV1 TRIP	202	UV1-B				
SIG11	0 - 500	_	0		211	ZOV1	203	UV1-C				
SIG12	0 - 500	_	0		351	ZOV1 TRIP	341	UV1 TRIP				
SIG13	0 - 500	_	0		0		211	ZOV1				
SIG14	0 - 500	_	0		0		351	ZOV1 TRIP				
SIG15	0 - 500	_	0		0		0 4					
SIG16	0 - 500	_	371	GEN.TRIP	371	GEN.TRIP	371	GEN.TRIP				
SIG17	0 - 500	_	401	ARC READY T	401	ARC READY T		ARC READY T				
SIG18	0 - 500	_	61	ARC BLOCK	61	ARC BLOCK		ARC BLOCK				
SIG19	0 - 500	_	403	ARC SHOT	403	ARC SHOT	403	ARC SHOT				
SIG20	0 - 500	_	0		0		0					
SIG21	0 - 500	_	0		0		0					
SIG22	0 - 500	_	0		0	X 1	0					
SIG23	0 - 500	_	0		0		0					
SIG24	0 - 500	_	0		0		0					
SIG25	0 - 500	_	0		0		0					
SIG26	0 - 500	_	0		0		0					
SIG27	0 - 500		0		0	YU	0					
SIG28	0 - 500	_	0		0		0					
SIG29	0 - 500	_	0		0		0					
SIG30	0 - 500		0		0		0					
SIG31	0 - 500		0		0		0					

#### 6. LED setting

LED1	.ED1 - LED3 setting													
	5	Setting range	A				Default	Setting				Set	tting	•
LED	Logic	Reset	Func	tions	Logic	Reset		Func	tions	Logic	Reset		Fund	ctions
LED1	OR/AND	Inst/Latch	ln #1	0-500	OR	Inst	ln #1	0				In #1		
			In #2	0-500			ln #2	0				ln #2		
			In #3	0-500			In #3	0				In #3		
			In #4	0-500			ln #4	0				ln #4		
LED2	OR / AND	Inst/Latch	ln #1	0-500	OR	Inst	ln #1	0				In #1		
			ln #2	0-500			ln #2	0				ln #2		
			In #3	0-500			In #3	0				In #3		
			In #4	0-500			In #4	0				In #4		
LED3	OR/AND	Inst/Latch	ln #1	0-500	OR	Inst	ln #1	0				In #1		
			ln #2	0-500			ln #2	0				ln #2		
			ln #3	0-500			In #3	0				In #3		
			ln #4	0-500			In #4	0				ln #4		

User s	etting of V	irtual LED	1									
	Setting ran	ge	Defa	ult setting	setting Setting							
LED	Reset	Functions	Reset	Functions	B <b>I</b> I 1	B <b>I</b> T 2	B <b>I</b> I 3	B <b>I</b> I 4	B <b>I</b> I 5	B <b>I</b> I 6	B <b>I</b> T 7	B <b>I</b> I 8
IND1	Inst / Latch	0 - 500	Inst	BIT1 - BIT8 : 0								
IND2	IND2 Inst/Latch 0-500 Inst		BIT1 - BIT8 : 0									

## **Appendix I**

# **Commissioning Test Sheet (sample)**

- 1. Relay identification
- 2. Preliminary check
- 3. Hardware check
- 4. Function test
- 5. Protection scheme test
- 6. Metering and recording check
- 7. Conjunctive test

1. Relay identification	
Type	Serial number
Model	System frequency
Station	Date
Circuit	Engineer
Protection scheme	Witness
Active settings group number	5
2. Preliminary check	
Ratings	
CT shorting contacts	
DC power supply	
Power up	~ (7)~
Wiring	
Relay inoperative alarm contact	
Calendar and clock	
3. Hardware check	<b>5</b>
3.1 User interface check	
3.2 Binary input/binary output circuit check	
Binary input circuit	
Binary output circuit	
3.3 AC input circuit	

#### 4. Function test

#### 4.1 Overcurrent elements test

(1) Operating value test

Element	Current setting	Measured current	Element	Current setting	Measured current
OC1-A			UC1-A		
OC2-A			UC2-A		•
ОС3-А			THM-A		Co
OC4-A			THM-T		
EF1			NOC1		
EF2			NOC2	~0	
EF3			CBF-A		
EF4					
SEF1					
SEF2			1	5	
SEF3		4			
SEF4					

(2) Operating time test (IDMT)

Element	Curve setting	Multiplier setting	Changed current	Measured time
OC1-A			× Current setting × Current setting × Current setting	
EF1		0	× Current setting × Current setting × Current setting	
SEF1			× Current setting × Current setting × Current setting	

(3) Directional operate characteristic test

Element	Current setting	Measured current	Element	Current setting	Measured current
OC1-A			SEF1		
OC2-A			SEF2		
OC3-A			SEF3		
OC4-A			SEF4		
EF1			NOC1		
EF2			NOC2		
EF3					
EF4					

#### 4.2 Overvoltage and undervoltage elements test

(1) Operating value test

Element	Voltage setting	Measured voltage	Element	Voltage setting	Measured voltage
OV1			ZOV1		
OV2			ZOV2		
UV1			NOV1		
UV2			NOV2		

(2) Operating time test (IDMT)

Element	Voltage setting	Multiplier setting	Changed voltage Measured time
OV1			<ul><li>× Voltage setting</li><li>× Voltage setting</li><li>× Voltage setting</li></ul>
UV1			Voltage setting     Voltage setting     Voltage setting
ZOV1			<ul><li>Voltage setting</li><li>Voltage setting</li><li>Voltage setting</li></ul>
NOV1		200	× Voltage setting × Voltage setting × Voltage setting

- 4.3 BCD element check
- 4.4 Cold load function check
- 4.5 Frequency elements test

Element	Frequency setting	Measured frequency
FRQ1		
FRQ2		
FRQ3		
FRQ4		

5. Protection scheme test	5.	Protection	scheme test	
---------------------------	----	------------	-------------	--

- 6. Metering and recording check
- 7. Conjunctive test

Scheme	Results
On load check	
Tripping circuit	
Reclosing circuit	

Appendix J
Return Repair Form

**TOSHIBA** 

#### **RETURN / REPAIR FORM**

Please fill in this form and return it to Toshiba Corporation with the GRD140 to be repaired.

Гуј	pe:	GRD140	)	Model:					
(Ex	amp	le: Type:	(	GRD140	Model:_	400A	_)		•
								. Co	
Pro	duct	:No.:							
	ial N								
								70	
Da	te:								
1.	Rea	ason for re	eturni	ng the relay					
		mal-fun	ction						
		does not	oper	ate					
		increase	d erro	or		27			
		investiga	ation						
		others							
					- 0				
					7				
					X				

2. Fault records, event records or disturbance records stored in the relay and relay settings are very helpful information to investigate the incident.

Please provide relevant information regarding the incident on floppy disk, or fill in the attached fault record sheet and relay setting sheet.

**TOSHIBA** 

#### **Fault Record**

(Example: 04/ Jul./ 2002 15:09:58.442)

#### Faulty phase:

#### Prefault values

Ia:	A
I _b :	A
I _c :	Α
Ie:	Α
I _{se} :	Α
I ₁ :	Α
I ₂ :	A
$I_2^2 / I_1$ :	

V _{an} : V _{bn} :	V
V _{bn} :	V
$V_{cn}$ :	V
V _e :	V
V _e : V _{ab} : V _{bc} :	V
V _{bc} :	V
V _{ca} :	V
V _{ca} : V ₀ :	V
-	

Hz

Hz

#### Fault values

Τ.	Α
I _a :	А
I _b :	Α
I _c :	Α
I _e :	Α
I _{se} :	A
I ₁ :	Α
I ₂ :	A
$\bar{I_2} / I_1$ :	
THM.	0/0

V _{an} :	V
V _{bn} :	V
$V_{cn}$ :	V
V _e :	V
V _{ab} :	V
V _{bc} :	V
V _{ca} :	V
V ₀ :	V
$V_1$ .	V

	3. What was the message on the LCD display at the time of the incident?
	4. Describe the details of the incident:
	5. Date incident occurred
	Day/Month/Year: / /
	(Example: 10/July/2002)
	6. Give any comments about the GRD140, including the documents:
	*.
	. 71
	Customer
	Name:
	Company Name:
	Address:
N	Telephone No.:
10	Facsimile No.:
10	Signature:

**Appendix K Technical Data** 

**— 269 —** 

**TOSHIBA** 6 F 2 S 0 7 5 8

## **TECHNICAL DATA**

Ratings			
AC current In:	1A or 5A		
AC current in: AC voltage Vn:	100V to 120 V		
Frequency:			
	50Hz or 60Hz		
DC auxiliary supply:	110/125Vdc (Operative range: 88 - 150Vdc) 220/250Vdc (Operative range: 176 - 300Vdc)		
	48/54/60Vdc (Operative range: 38.4 - 72Vdc)		
Superimposed AC ripple on DC supply:	maximum 12%		
DC supply interruption:	maximum 50ms at 110V		
Binary input circuit DC voltage:	110/125Vdc (Operative range: 88 - 150Vdc)		
	220/250Vdc (Operative range: 176 - 300Vdc)		
	48/54/60Vdc (Operative range: 38.4 - 72Vdc)		
Overload Ratings			
AC current inputs:	3 times rated current continuous		
	100 times rated current for 1 second		
AC voltage inputs:	2 times rated voltage continuous		
Burden	N.O		
AC phase current inputs:	≤ 0.1VA (1A rating)		
	≤ 0.2VA (5A rating)		
AC earth current inputs:	≤ 0.3VA (1A rating)		
	≤ 0.4VA (5A rating)		
AC sensitive earth inputs:	≤ 0.3VA (1A rating)		
	≤ 0.4VA (5A rating)		
AC voltage inputs:	≤ 0.1VA (at rated voltage)		
DC power supply:	≤ 10W (quiescent)		
Dinary input circuits	≤ 15W (maximum) ≤ 0.5W per input at 110Vdc		
Binary input circuit:	Solow ber input at 110vdc		
Current Transformer Requirements			
Phase Inputs	Typically 5P20 with rated burden according to load.		
Standard Earth Inputs:	Core balance CT or residual connection of phase CTs.		
Sensitive Earth Inputs:	Core balance CT.		
Directional Phase Overcurrent Protection			
P/F 1 st Overcurrent threshold:	OFF, 0.02 – 5.00A in 0.01A steps (1A rating) OFF, 0.1 – 25.0A in 0.1A steps (5A rating)		
Delay type:	DTL, IEC NI, IEC VI, IEC EI, UK LTI, IEEE MI,		
Delay type:	IEEE VI, IEEE EI, US CO8 I, US CO2 STI		
IDMTL Time Multiplier Setting TMS:	0.010 – 1.500 in 0.001 steps		
DTL delay:	0.00 – 300.00s in 0.01s steps		
Reset Type:	Definite Time or Dependent Time		
Reset Definite Delay:	0.0 – 300.0s in 0.1s steps		
Reset Time Multiplier Setting RTMS:	0.010 – 1.500 in 0.001 steps		
P/F 2 nd Overcurrent threshold:	OFF, 0.02 – 5.00A in 0.01A steps (1A rating)		
177 2 Overedment unconoid.	OFF, 0.02 – 5.00A in 0.01A steps (1A rating) OFF, 0.1 – 25.0A in 0.1A steps (5A rating)		
P/F 3 rd , 4 th Overcurrent thresholds:	OFF, 0.02 – 50.00A in 0.01A steps (1A rating)		
, , , , , , , , , , , , , , , , ,	OFF, 0.1 – 250.0A in 0.1A steps (5A rating)		
DTL delay:	0.00 – 300.00s in 0.01s steps		
P/F Characteristic Angle:	_95° to +95° in 1° steps		
· ·	1		

Directional Earth Fault Protection			
E/F 1 st Overcurrent threshold:	OFF 0.00 F 00A in 0.01A ptone (1A retire)		
E/F 1 Overcurrent threshold:	OFF, 0.02 – 5.00A in 0.01A steps (1A rating) OFF, 0.1 – 25.0A in 0.1A steps (5A rating)		
Delay type:	DTL, IEC NI, IEC VI, IEC EI, UK LTI, IEEE MI, IEEE VI, IEEE EI, US CO8 I, US CO2 STI		
IDMTL Time Multiplier Setting TMS:	0.010 – 1.500 in 0.001 steps		
DTL delay:	0.00 – 300.00s in 0.01s steps		
Reset Type:	Definite Time or Dependent Time		
Reset Definite Delay:	0.0 – 300.0s in 0.1s steps		
Reset Time Multiplier Setting RTMS:	0.010 – 1.500 in 0.001 steps		
E/F 2 nd threshold:	OFF, 0.02 – 5.00A in 0.01A steps (1A rating)		
En 2 anoshola.	OFF, 0.1 – 25.0A in 0.1A steps (5A rating)		
E/F 3 rd , 4 th thresholds:	OFF, 0.02 – 50.00A in 0.01A steps (1A rating) OFF, 0.1 – 250.0A in 0.1A steps (5A rating)		
DTL delay:	0.00 – 300.00s in 0.01s steps		
E/F Characteristic angle:	_95° to +95° in 1° steps		
E/F directional voltage threshold:	0.5 – 100.0V in 0.1V steps		
Directional Sensitive Earth Fault Protection	N.O.		
SEF 1 st Overcurrent threshold:	OFF, 0.002 – 0.200A in 0.001A steps (1A rating)		
	OFF, 0.01 + 1.00A in 0.01A steps (5A rating)		
Delay Type:	DTL, IEC NI, IEC VI, IEC EI, UK LTI, IEEE MI,		
	IEEE VI, IEEE EI, US CO8 I, US CO2 STI		
IDMTL Time Multiplier Setting TMS:	0.010 - 1.500 in 0.001 steps		
DTL delay:	0.00 – 300.00s in 0.01s steps		
Reset Type:	Definite Time or Dependent Time		
Reset Definite Delay:	0.0 – 300.0s in 0.1s steps		
Reset Time Multiplier Setting RTMS:	0.010 – 1.500 in 0.001 steps		
DTL delay (back-up timer):	0.00 – 300.00s in 0.01s steps		
SEF 2 nd , 3 rd , 4 th threshold:	OFF, 0.002 – 0.200A in 0.001A steps (1A rating) OFF, 0.01 – 1.00A in 0.01A steps (5A rating)		
DTL delay:	0.00 – 300.00s in 0.01s steps		
SEF Characteristic angle:	-95° to +95° in 1° steps		
SEF Boundary of operation:	•		
SEF directional voltage threshold:	±87.5°, ±90° 0.5 – 100.0V in 0.1V steps		
Residual power threshold:	OFF, 0.00 – 20.00W in 0.1W steps (1A primary)		
itesiduai powei tiliesiloid.	OFF, 0.00 – 20.00W in 0.01W steps (1A primary) OFF, 0.0 – 100.0W in 0.1W steps (5A primary)		
Phase Undercurrent Protection			
Undercurrent 1 st , 2 nd threshold:	OFF, 0.10 – 2.00A in 0.01A steps (1A rating)		
	OFF, 0.5 – 10.0A in 0.1A steps (5A rating)		
DTL Delay:	0.00 – 300.00s in 0.01s steps		
Thermal Overload Protection			
$I_{\theta}$ = k. $I_{FLC}$ (Thermal setting):	OFF, 0.40 – 2.00A in 0.01A steps (1A rating)		
*	OFF, 2.0 – 10.0A in 0.1A steps (5A rating)		
Previous load current (I _P )	0.00 – 1.00A in 0.01A steps (1A rating)		
	0.0 – 5.0A in 0.1A steps (5A rating)		
Time constant (τ):	0.5 – 500.0mins in 0.1min steps		
Thermal alarm:	OFF, 50% to 99% in 1% steps		

Directional Negative Phase Sequence Overcurrent Protection (NOC)			
NOC 1 st , 2 nd threshold:	OFF, 0.10 – 2.00A in 0.01A steps (1A rating)		
Tree 1 , 2 all conoid.	OFF, 0.5 – 10.0A in 0.1A steps (5A rating)		
DTL delay:	0.00 – 300.00s in 0.01s steps		
NOC Characteristic angle:	-95° to +95° in 1° steps		
NOC Directional voltage threshold	0.5 – 25.0V in 0.1V steps		
Overvoltage Protection	•		
1 st , 2 nd Overvoltage thresholds:	OFF, 10.0 – 200.0V in 0.1V steps		
Delay type (1 st threshold only):	DTL, IDMTL		
IDMTL Time Multiplier Setting TMS:	0.05 – 100.00 in 0.01 steps		
DTL delay:	0.00 – 300.00s in 0.01s steps		
DO/PU ratio	10 – 98% in 1% steps		
Reset Delay (1 st threshold only):	0.0 – 300.0s in 0.1s steps		
Undervoltage Protection			
1 st , 2 nd Undervoltage thresholds:	OFF, 5.0 – 130.0V in 0.1V steps		
Delay type (1 st threshold only):	DTL, IDMTL		
IDMTL Time Multiplier Setting TMS:	0.05 – 100.00 in 0.01 steps		
DTL delay:	0.00 – 300.00s in 0.01s steps		
Reset Delay (1 st threshold only):	0.0 – 300.0s in 0.1s steps		
Undervoltage Block	5.0 – 20.0Vin 0.1V steps		
Zero Phase Sequence Overvoltage Protection	(ZOV)		
1 st , 2 nd ZOV Overvoltage thresholds:	OFF, 1.0 – 130.0V in 0.1V steps		
Delay type (1 st threshold only):	DTL, IDMTL		
IDMTL Time Multiplier Setting TMS:	0.05 – 100.00 in 0.01 steps		
L delay: 0.00 – 300.00s in 0.01s steps			
Reset Delay (1 st threshold only): 0.0 – 300.0s in 0.1s steps			
Negative Phase Sequence Overvoltage Protection	ction (NOV)		
1 st , 2 nd NOV Overvoltage thresholds:	OFF, 1.0 – 130.0V in 0.1V steps		
Delay type (1 st threshold only):	DTL, IDMTL		
IDMTL Time Multiplier Setting TMS:	0.05 – 100.00 in 0.01 steps		
DTL delay:	0.00 – 300.00s in 0.01s steps		
Reset Delay (1 st threshold only):	0.0 – 300.0s in 0.1s steps		
Under/Over Frequency Protection			
1 st - 4 th under/overfrequency threshold	$(F_{nom} - 10.00Hz) - (F_{nom} + 10.00Hz)$ in 0.01Hz steps		
. (7)	F _{nom} : nominal frequency		
DTL delay:	0.00 – 300.00s in 0.01s steps		
Frequency UV Block	40.0 – 100.0V in 0.1V steps		
Broken Conductor Protection			
Broken conductor threshold (I ₂ /I ₁ ):	OFF, 0.10 – 1.00 in 0.01 steps		
DTL delay:	0.00 – 300.00s in 0.01s steps		
CBF Protection			
CBF threshold:	OFF, 0.10 – 2.00A in 0.01A steps (1A rating)		
	OFF, 0.5 – 10.0A in 0.1A steps (5A rating)		
CBF stage 1 (Backup trip) DTL: 0.00 – 300.00s in 0.01s steps			
CBF stage 2 (Re-trip) DTL:	0.00 – 300.00s in 0.01s steps		

Autoreclose			
ARC Reclaim Time	0.0– 600.0s in 0.1s steps		
Close Pulse Width	0.01 – 10.00s in 0.01s steps		
Lock-out Recovery Time	OFF, 0.1 – 600.0s in 0.1s steps		
Sequences	1 – 5 Shots to Lock-out, each trip programmable for inst or		
	Delayed operation		
Dead Times(programmable for each shot)	0.01 - 300.00s in 0.01s steps		
Accuracy	. (2)		
Overcurrent Pick-ups:	100% of setting ± 5%		
Overcurrent PU/DO ratio:	≥100%		
Undercurrent Pick-up:	100% of setting ± 5%		
Undercurrent PU/DO ratio:	≤100%		
Overvoltage Pick-ups:	100% of setting ± 5%		
Undervoltage Pick-ups:	100% of setting ± 5%		
Inverse Time Delays:	$\pm$ 5% or 30ms (1.5 to 30 times setting)		
Definite Time Delays:	± 1% or 10ms		
Transient Overreach for instantaneous elements:	<-5% for X/R = 100.		
Front Communication port - local PC (RS232)			
Connection:	Point to point		
Cable type:	Multi-core (straight)		
Cable length:	15m (max.)		
Connector:	RS232C 9-way D-type female		
Rear Communication port - remote PC (RS485)			
Connection:	Multidrop (max. 32 relays)		
Cable type:	Twisted pair		
Cable length:	1200m (max.)		
Connector:	Screw terminals		
Isolation:	1kVac for 1 min.		
Transmission rate:	64kpbs for RSM system		
Trailer Hade:	9.6, 19.2kbps for IEC60870-5-103		
Rear Communication port - remote PC (Fibre O			
Cable type:	50/125 or 62.5/125μm fibre		
Cable length:	1000m (max.)		
Connector:	ST		
Transmission rate:	9.6, 19.2kbps for IEC60870-5-103		
Binary Inputs	0.0, 10.200010 12.000010 0 100		
Operating voltage	Typical 74Vdc(min. 70Vdc) for 110V/125Vdc rating		
Operating voltage	Typical 138Vdc(min. 125Vdc) for 220V/250Vdc rating		
	Typical 31Vdc(min. 28Vdc) for 48V/54V/60Vdc rating		
Binary Outputs			
Number	8		
Ratings:	Make and carry: 4A continuously		
	Make and carry: 20A, 290Vdc for 0.5s (L/R≥5ms)		
	Break: 0.1A, 290Vdc (L/R=40ms)		
Durability:	Loaded contact: 10000 operations		
	Unloaded contact: 100000 operations		

Mechanical design		
Weight	4.5kg	
Case colour	Munsell No. 10YR8/0.5	
Installation	Flush mounting	

### **ENVIRONMENTAL PERFORMANCE**

Test	Standards	Details
Atmospheric Environn	nent	
Temperature	IEC60068-2-1/2	Operating range: -10°C to +55°C. Storage / Transit: -25°C to +70°C.
Humidity	IEC60068-2-3	56 days at 40°C and 93% relative humidity.
Enclosure Protection	IEC60529	IP51
Mechanical Environme	ent	
Vibration	IEC60255-21-1	Response - Class 1 Endurance - Class 1
Shock and Bump	IEC60255-21-2	Shock Response Class 1 Shock Withstand Class 1 Bump Class 1
Seismic	IEC60255-21-3	Class 1
Electrical Environment	t	
Dielectric Withstand	IEC60255-5	2kVrms for 1 minute between all terminals and earth. 2kVrms for 1 minute between independent circuits. 1kVrms for 1 minute across normally open contacts.
High Voltage Impulse	IEC60255-5	Three positive and three negative impulses of 5kV(peak), 1.2/50µs, 0.5J between all terminals and between all terminals and earth.
Electromagnetic Envir	onment	
High Frequency Disturbance / Damped Oscillatory Wave	IEC60255-22-1 Class 3, IEC61000-4-12 / EN61000-4-12	1MHz 2.5kV applied to all ports in common mode. 1MHz 1.0kV applied to all ports in differential mode.
Electrostatic Discharge	IEC60255-22-2 Class 3, IEC61000-4-2 / EN61000-4-2	6kV contact discharge, 8kV air discharge.
Radiated RF Electromagnetic Disturbance	IEC60255-22-3 Class 3, IEC61000-4-3 / EN61000-4-3	Field strength 10V/m for frequency sweeps of 80MHz to 1GHz and 1.7GHz to 2.2GHz. Additional spot tests at 80, 160, 450, 900 and 1890MHz.
Fast Transient Disturbance	IEC60255-22-4, IEC61000-4-4 / EN61000-4-4	4kV, 2.5kHz, 5/50ns applied to all inputs.
Surge Immunity	IEC60255-22-5, IEC61000-4-5 / EN61000-4-5	1.2/50µs surge in common/differential modes: HV ports: 4kV/2kV (peak) PSU and I/O ports: 2kV/1kV (peak) RS485 port: 1kV/0.5kV (peak)
Conducted RF Electromagnetic Disturbance	IEC60255-22-6 Class 3, IEC61000-4-6 / EN61000-4-6	10Vrms applied over frequency range 150kHz to 100MHz. Additional spot tests at 27 and 68MHz.
Power Frequency Disturbance	IEC60255-22-7, IEC61000-4-16 / EN61000-4-16	300V 50Hz for 10s applied to ports in common mode. 150V 50Hz for 10s applied to ports in differential mode. Not applicable to AC inputs.
Conducted and Radiated Emissions	IEC60255-25, EN55022 Class A, IEC61000-6-4 / EN61000-6-4	Conducted emissions: 0.15 to 0.50MHz: <79dB (peak) or <66dB (mean) 0.50 to 30MHz: <73dB (peak) or <60dB (mean) Radiated emissions (at 30m): 30 to 230MHz: <30dB 230 to 1000MHz: <37dB

European Commission Directives			
89/336/EEC	Compliance with the European Commission Electromagnetic Compatibility Directive is demonstrated according to EN 61000-6-2 and EN 61000-6-4.		
73/23/EEC	Compliance with the European Commission Low Voltage Directive is demonstrated according to EN 50178 and EN 60255-5.		

Appendix L
Symbols Used in Scheme Logic

Symbols used in the scheme logic and their meanings are as follows:

#### Signal names

Marked with _____ : Measuring element output signal

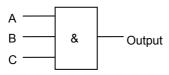
Marked with : Binary signal input from or output to the external equipment

Marked with [ ] : Scheme switch

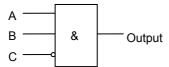
Marked with " : Scheme switch position

Unmarked : Internal scheme logic signal

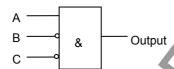
#### **AND** gates



Α	ВС	Output
1	1	1
Ot	her cases	0



АВ	С	Output
1 1	0	1
Other case	es	0

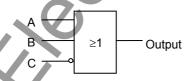


Α	В	С	Output
1	0	0	1
Other cases			0

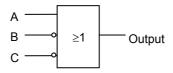
#### **OR** gates



Α	В	С	Output
0	0	0	0
Other cases			1

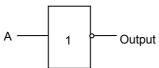


Α	В	С	Output
0	0	1	0
Ot	her cas	es	1



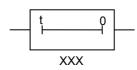
Α	В	С	Output
0	1	1	0
Ot	her cas	es	1

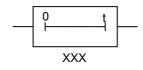
#### Signal inversion

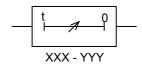


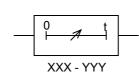
Α	Output
0	1
1	0

#### Timer









Delayed pick-up timer with fixed setting

XXX: Set time

Delayed drop-off timer with fixed setting

XXX: Set time

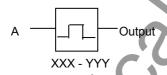
Delayed pick-up timer with variable setting

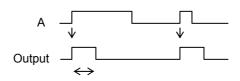
XXX - YYY: Setting range

Delayed drop-off timer with variable setting

XXX - YYY: Setting range

#### One-shot timer



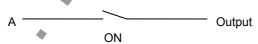


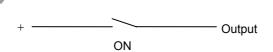
XXX - YYY: Setting range

Flip-flop



Cala	
Scheme	SWITCH
COLICIAL	OF ICOII





S	R	Output
0	0	No change
1	0	1
0	1	0
1	1	0

Α	Switch	Output
1	ON	1
Oth	er cases	0

Switch	Output
ON	1
OFF	0

## **Appendix M**

IEC60870-5-103: Interoperability

#### IEC60870-5-103: Interoperability

#### 1. Physical Layer

1.1 Electrical interface: EIA RS-485

Number of loads, 32 for one protection equipment

1.2 Optical interface

Glass fibre (option)

ST type connector (option)

1.3 Transmission speed

User setting: 9600 or 19200 bit/s

#### 2. Application Layer

COMMON ADDRESS of ASDU

One COMMON ADDRESS OF ASDU (identical with station address)

#### 3. IEC60870-5-103 Interface

#### 3.1 Spontaneous events

The events created by the relay will be sent using Function type (FUN) / Information numbers (INF) to the IEC60870-5-103 master station. 8 wide-use events are provided.

#### 3.2 General interrogation

The GI request can be used to read the status of the relay, the Function types and Information numbers that will be returned during the GI cycle are shown in the table below.

#### 3.3 Cyclic measurements

The relay will produce measured values using Type ID=3 and 9 on a cyclical basis, this can be read from the relay using a Class 2 poll. The rate at which the relay produces new measured values is 2 seconds.

It should be noted that the measurands transmitted by the relay are sent as a proportion of either 1.2 or 2.4 times the rated value of the analog value. Either 1.2 or 2.4 can be selected by the "IECNF*" setting.

#### 3.4 Commands

A list of the supported commands is contained in the table below. The relay will respond to other commands with an ASDU 1, with a cause of transmission (COT) of negative acknowledgement of a command.

#### 3.5 Test mode

In test mode, both spontaneous messages and polled measured values, intended for processing in the control system, are designated by means of the CAUSE OF TRANSMISSION 'test mode'. This means that CAUSE OF TRANSMISSION = 7 'test mode' is used for messages normally transmitted with COT=1 (spontaneous) or COT=2 (cyclic).

For details, refer to the standard IEC60870-5-103.

#### 3.6 Blocking of monitor direction

If the blocking of the monitor direction is activated in the protection equipment, all indications and measurands are no longer transmitted.

For details, refer to the standard IEC60870-5-103.

#### 4. List of Information

#### **List of Information**

				Type		_
INF	Description	Contents	GI	Type ID	COT	FUN
Standa	ard Information numbers in m	onitor direction				
System	Function					
0	End of General Interrogation	Transmission completion of GI items.		8	10	255
0	Time Synchronization	Time Synchronization ACK.		6	8	255
2	Reset FCB	Reset FCB(toggle bit) ACK		5	3	219
3	Reset CU	Reset CU ACK		5	4	219
4	Start/Restart	Relay start/restart		5	5	219
5	Pow er On	Relay pow er on.		Not	supported	
Status I	ndications					
16	Auto-recloser active	If it is possible to use auto-recloser, this item is set active, if impossible, inactive.	Gl	1	1, 7, 9, 11, 12, 20, 21	219
17	Teleprotection active	If protection using telecommunication is available, this item is set to active. If not, set to inactive.	1	Not	supported	
18	Protection active	If the protection is available, this item is set to active. If not, set to inactive.	GI	1	1, 7, 9, 12, 20, 21	219
19	LED reset	Reset of latched LEDs		1	1, 7, 11, 12, 20, 21	219
20	Monitor direction blocked	Block the 103 transmission from a relay to control system. IECBLK: "Blocked" setting.	GI	1	9, 11	219
21	Test mode	Transmission of testmode situation from a relay to control system. IECTST: "ON" setting.	GI	1	9, 11	219
22	Local parameter Setting	When a setting change has done at the local, the event is sent to control system.		Not	supported	
23	Characteristic1	Setting group 1 active	GI	1	1, 7, 9, 11, 12, 20, 21	219
24	Characteristic2	Setting group 2 active	GI	1	1, 7, 9, 11, 12, 20, 21	219
25	Characteristic3	Setting group 3 active	GI	1	1, 7, 9, 11, 12, 20, 21	219
26	Characteristic4	Setting group 4 active	Gl	1	1, 7, 9, 11, 12, 20, 21	219
27	Auxiliary input1	User specified signal 1 (Signal specified by IECB1: ON) (*1)	GI	1	1, 7, 9	219
28	Auxiliary input2	User specified signal 2 (Signal specified by IECB2: ON) (*1)	GI	1	1, 7, 9	219
29	Auxiliary input3	User specified signal 3 (Signal specified by IECB3: ON) (*1)	GI	1	1, 7, 9	219
30	Auxiliary input4	User specified signal 4 (Signal specified by IECB4: ON) (*1)	Gl	1	1, 7, 9	219
Supervi	sion Indications					
32	Measurand supervision I	Zero sequence current supervision	GI	1	1, 7, 9	219
33	Measurand supervision V	Zero sequence voltage supervision	GI	1	1, 7, 9	219
35	Phase sequence supervision	Negative sequence voltage supevision	Gl	1	1, 7, 9	219
36	Trip circuit supervision	Output circuit supervision	GI	1	1, 7, 9	219
37	l>>backup operation			Not	supported	
38	VT fuse failure	VT failure	Gl	1	1, 7, 9	219
39	Teleprotection disturbed	CF(Communication system Fail) supervision		Not	supported	
46	Group warning	Only alarming	Gl	1	1, 7, 9	219
47	Group alarm	Trip blocking and alarming	Gl	1	1, 7, 9	219
	ault Indications					
	Earth Fault L1	A phase earth fault (*2)	Gl	1	1, 7, 9	219
49	Earth Fault L2	B phase earth fault (*2)	Gl	1	1, 7, 9	219
50	Earth Fault L3	C phase earth fault (*2)	Gl	1	1, 7, 9	219
51	Earth Fault Fw d	Earth fault forw ard (*2) (*3)	Gl	1	1, 7, 9	219
52	Earth Fault Rev	Earth fault reverse (*2) (*3)	GI	1	1, 7, 9	219

INF	Description	Contents	GI	Type ID	COT	FUN
Fault Inc	dications					
64	Start/pick-up L1	A phase, A-B phase or C-A phase element pick-up	Gl	2	1, 7, 9	219
65	Start/pick-up L2	B phase, A-B phase or B-C phase element pick-up	Gl	2	1, 7, 9	219
66	Start/pick-up L3	C phase, B-C phase or C-A phase element pick-up	Gl	2	1, 7, 9	219
67	Start/pick-up N	Earth fault element pick-up	Gl	2	1, 7, 9	219
68	General trip	BO status specified by IECGT: ON (*1)		2	1, 7	219
69	Trip L1	BO status specified by IECAT: ON (*1)		2	1, 7	219
70	Trip L2	BO status specified by IECBT: ON (*1)		2	1, 7	219
71	Trip L3	BO status specified by IECCT: ON (*1)	7/8	2	1, 7	219
72	Trip I>>(back-up)	Back up trip		Not	supported	
73	Fault location X In ohms	Fault location (prim. [ohm] / second. [ohm] / km selectable by IECFL)	1	4	1, 7	219
74	Fault forw ard/line	Forw ard fault (*2) (for OC, EF, SEF)		2	1, 7	219
75	Fault reverse/Busbar	Reverse fault (*2) (for OC, EF, SEF)	-	2	1, 7	219
76	Teleprotection Signal transmitted	Carrier signal sending	Not supported			
77	Teleprotection Signal received	Carrier signal receiving		Not	supported	
78	Zone1	Zone 1 trip	Not supported			
79	Zone2	Zone 2 trip	Not supported			
80	Zone3	Zone 3 trip	Not supported			
81	Zone4	Zone 4 trip		Not	supported	
82	Zone5	Zone 5 trip		Not	supported	
83	Zone6	Zone 6 trip		Not	supported	
84	General Start/Pick-up	Any elements pick-up	GI	2	1, 7, 9	219
85	Breaker Failure	CBF trip or CBF retrip	-	2	1, 7	219
86	Trip measuring system L1			Not	supported	
87	Trip measuring system L2			Not	supported	
88	Trip measuring system L3			Not	supported	
89	Trip measuring system E			Not	supported	
90	Trip ⊳	Inverse time OC trip (OC1 trip)		2	1, 7	219
91	Trip >>	Definite time OC trip (OR logic of OC1 to OC3 trip)	-	2	1, 7	219
92	Trip IN>	Inverse time earth fault OC trip (OR logic of EF1 and SEF1 trip)		2	1, 7	219
93	Trip IN>>	Definite time earth fault OC trip (OR logic of EF1 to EF3 and SEF1 to SEF3 trip)	1	2	1, 7	219
Autored	close indications					
128	CB 'ON' by Autoreclose	CB close command output		1	1, 7	219
129	CB 'ON' by long-time Autoreclose			1	1, 7	219
130	Autoreclose Blocked	Autoreclose block	GI	1	1, 7, 9	219

Note (*1): Not available if the setting is "0".

(*2): Not available when neither EF nor SEF element is used.

(*3): Not available when directional operate characteristic is not used.

INF	Description	Contents	GI	Type ID	СОТ	FUN
IECI1	User specified 1	Signal specified by IECE1: ON (*1)	IECG1 (yes/no)	2	1, 7	219
IECI2	User specified 2	Signal specified by IECE2: ON (*1)	IECG2 (yes/no)	2	1, 7	219
IECI3	User specified 3	Signal specified by IECE3: ON (*1)	IECG3 (yes/no)	2	1, 7	219
IECI4	User specified 4	Signal specified by IECE4: ON (*1)	IECG4 (yes/no)	2	1, 7	219
IECI5	User specified 5	Signal specified by IECE5: ON (*1)	IECG5 (yes/no)	2	1, 7	219
IECI6	User specified 6	Signal specified by IECE6: ON (*1)	IECG6 (yes/no)	2	1, 7	219
IECI7	User specified 7	Signal specified by IECE7: ON (*1)	(yes/no)	2	1, 7	219
IECI8	User specified 8	Signal specified by IECE8: ON (*1)	(yes/no)	2	1, 7	219
Measur	ands(*4)					
144	Measurand I	lb meaurand		3.1	2, 7	219
145	Measurand I,V	lb, Vab measurand		3.2	2, 7	219
146	Measurand I,V,P,Q	lb, Vab, P, Q measurand		3.3	2, 7	219
147	Measurand IN,VEN	le, Ve measurand		3.4	2, 7	219
148	Measurand IL1,2,3, VL1,2,3, P,Q,f	la, lb, lc, Va, Vb, Vc, P, Q, f measurand		9	2, 7	219
Generio	Function					
240	Read Headings			Not su	oported	
241	Read attributes of all entries of a group			Not su	oported	
243	Read directory of entry			Not su	oported	
244	Real attribute of entry	0'0'		Not sup	oported	
245	End of GGI	7)	Not supported			
249	Write entry w ith confirm		Not supported			
250	Write entry with execute			Not su	oported	
251	Write entry aborted			Not su	oported	

### Note (*4): depends on relay model as follows:

	Type ID=3.1	Type ID=3	.2	Type ID=3	.3			Type ID=3.4	
Model	(INF=144)	(INF=145)		(INF=146)				(INF=147)	
	IL2	IL2	VL1-VL2	IL2	VL1-VL2	3-phase P	3-phase Q	IN	VEN
Model 110	0	0	0	0	0	0	0	le	Ve
Model 400	lb	lb	Vab	lb	Vab	Р	Q	le	Ve
Model 420	lb	lb	Vab	lb	Vab	Р	Q	le	Ve
	Type ID=9								
Model	(INF=148)								
	IL1	IL2	IL3	VL1	VL2	VL3	3-phase P	3-phase Q	f
Model 110	0	0	0	0	0	0	0	0	0
Model 400	la	lb	lc	Van	Vbn	Vcn	Р	Q	f
Model 420	la	lb	lc	Van	Vbn	Vcn	Р	Q	f

Above values are normalized by IECNF*.

INF	Description	Contents	COM	Type ID	СОТ	FUN
Select	ion of standard information nu	mbers in control direction				
System	functions					
0	Initiation of general interrogation			7	9	255
0	Time synchronization			6	8	255
Genera	l commands				•	
16	Auto-recloser on/off		ONOFF	20	20	219
17	Teleprotection on/off		OWOFF	20	20	219
18	Protection on/off	(*5)	ON/OFF	20	20	219
19	LED reset	Reset indication of latched LEDs.	ON	20	20	219
23	Activate characteristic 1	Setting Group 1	ON	20	20	219
24	Activate characteristic 2	Setting Group 2	ON	20	20	219
25	Activate characteristic 3	Setting Group 3	ON	20	20	219
26	Activate characteristic 4	Setting Group 4	ON	20	20	219
Generio	functions					
240	Read headings of all defined groups	. 05		Not su	pported	
241	Read values or attributes of all entries of one group			Not su	pported	
243	Read directory of a single entry			Not su	pported	
244	Read values or attributes of a single entry		Not supported			
245	General Interrogation of generic data		Not supported			
248	Write entry		Not supported			
249	Write entry with confirmation	7.0	Not supported			
250	Write entry with execution			Not sup	pported	
251	Write entry abort			Not su	pported	

Note (*5): While the relay receives the "Protection off" command, " IN SERVICE LED" is off.

	Description	Contents	GRD140 supported	Comment
Basic a	application functions			
	Test mode		Yes	
	Blocking of monitor direction		Yes	
	Disturbance data		No	
	Generic services		No	
	Private data		Yes	
Miscel	laneous	•	•	
	Measurand		Max. MVAL = rated value times	
	Current L1	la	1,2 or 2,4	IECNFI setting
	Current L2	lb	1,2 or 2,4	IECNFI setting
<b>+</b>	Current L3	Ic	1,2 or 2,4	IECNFI setting
	Voltage L1-E	Va	1,2 or 2,4	IECNFV setting
	Voltage L2-E	Vb	1,2 or 2,4	IECNFV setting
	Voltage L3-E	Vc	1,2 or 2,4	IECNFV setting
	Active power P	Р	1,2 or 2,4	IECNFP setting
	Reactive power Q	Q	1,2 or 2,4	IECNFP setting
	Frequency f	f	1,2 or 2,4	IECNFf setting
	Voltage L1 - L2	Vab	1,2 or 2,4	IECNFV setting

**TOSHIBA** 6 F 2 S 0 7 5 8

#### [Legend]

#### GI: General Interrogation

Type ID: Type Identification (refer to IEC60870-5-103 section 7.2.1)

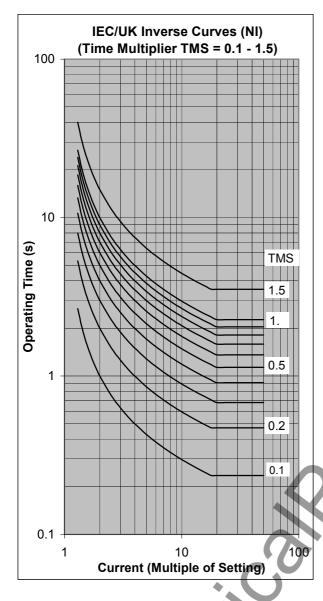
- 1: time-tagged message
- 2: time-tagged message with relative time
- 3: measurands I
- 4: time-tagged measurands with relative time
- 5: identification
- 6: time synchronization
- 8 : general interrogation termination
- 9: measurands II
- 10: generic data
- 11: generic identification
- 20: general command
- 23: list of recorded disturbances
- 26: ready for transmission for disturbance data
- 27: ready for transmission of a channel
- 28: ready for transmission of tags
- 29: transmission of tags
- 30: transmission of disturbance values
- 31: end of transmission

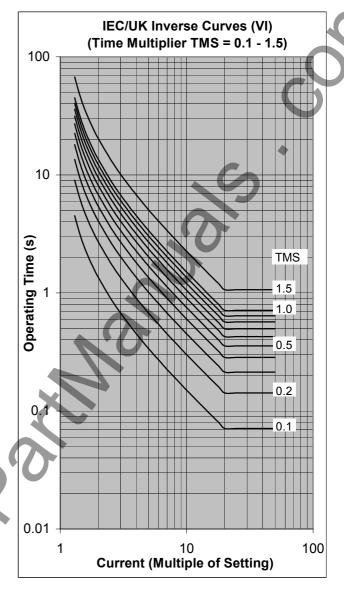
#### COT: Cause of Transmission (refer to IEC60870-5-103 section 7.2.3)

- 1: spontaneous
- 2: cyclic
- 3: reset frame count bit (FCB)
- 4: reset communication unit (CU)
- 5: start / restart
- 6: power on
- 7: test mode
- 8: time synchronization
- 9: general interrogation
- 10: termination of general interrogation
- 11: local operation
- 12: remote operation
- 20: positive acknowledgement of command
- 21 negative acknowledgement of command
- 31: transmission of disturbance data
- 40: positive acknowledgement of generic write command
- 41: negative acknowledgement of generic write command
- 42: valid data response to generic read command
- 43: invalid data response to generic read command
- 44: generic write confirmation

## **Appendix N**

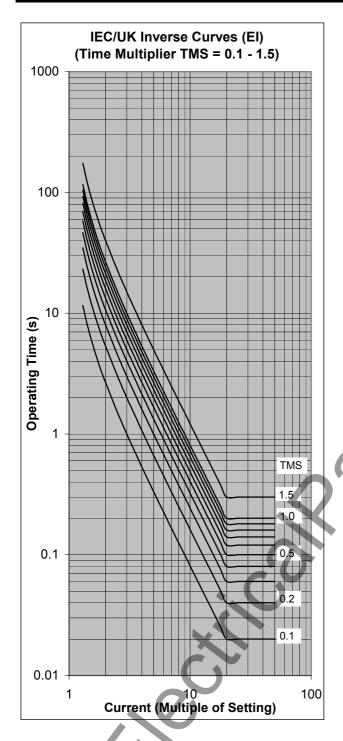
**Inverse Time Characteristics** 

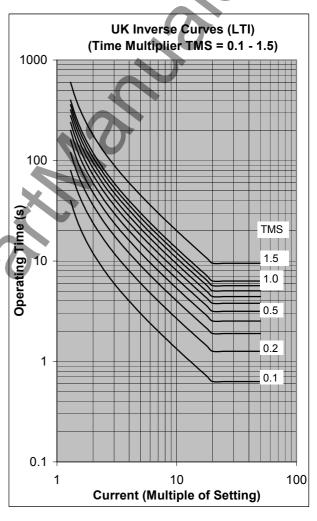




Normal Inverse

**Very Inverse** 

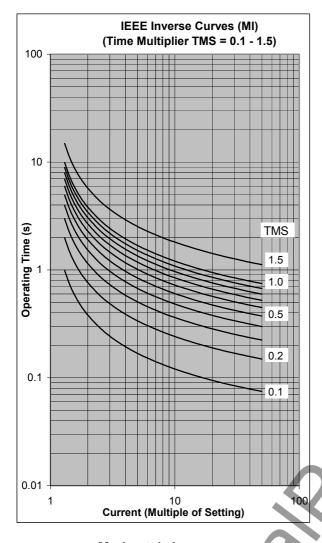


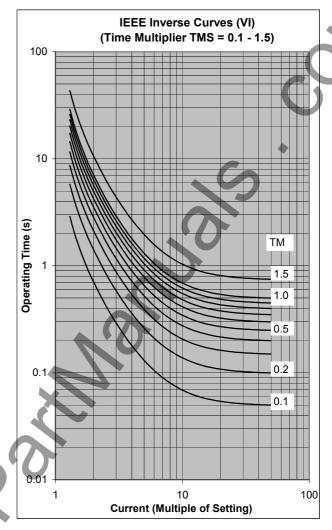


**Extremely Inverse** 

**Long Time Inverse** 

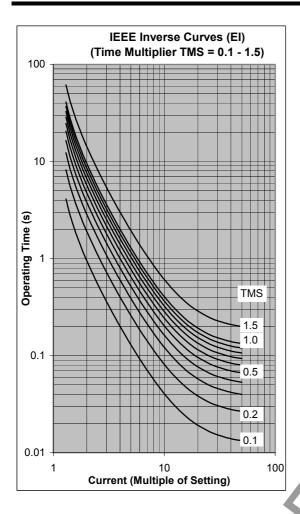
**TOSHIBA** 



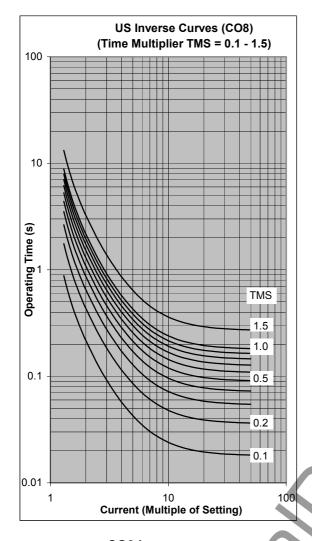


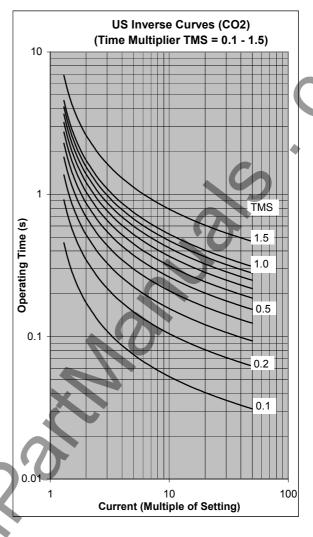
Moderately Inverse

**Very Inverse** 



**Extremely Inverse** 





**CO8 Inverse** 

**CO2 Short Time Inverse** 

Appendix O
Ordering

## **Ordering**

Fibre optic Dual RS485 LED label

Standard

Option: User configurable LED label

Directional	Overcurrent Relay
-------------	-------------------

Directional Overcurrent Relay	GRD140 - A
Type:	
Directional Overcurrent Relay	GRD140
Model:	
-Model 110: Directional earth fault and directional sensitive earth fault	110
-Model 400: Directional 3 phase + earth fault	400
-Model 420: Directional 3 phase + earth + sensitive earth	420
CT Rating:	
1A	1
5A	2
Frequency:	
50Hz	1
60Hz	2
DC auxiliary supply rating:	
110V/125V	
220V/250V	2
48V	3
Rear communication port:	
RS485	

None

## Version-up Records

Version No.	Date	Revised Section	Contents
0.0	Mar. 25, 2004		First issue
0.1	Apr. 23, 2004	2.1.2	Modified the description of sections 2.1.2.1 and 2.1.2.2.
		2.1.3	Modified the description of sections 2.1.3.1 to 2.1.3.6, and Figure 2.1.16.
		2.1.8	Modified the description.
		2.3	Modified the description.
		2.5, 2.5.1	Modified the description.
		3.3	Modified the descriptions of sections 3.3.3 and 3.3.4.
		4.2.6.7	Modified the description.
		6.4.2	Modified the Figure 6.4.1.
		Appendices	Modified the Appendix C (No. 122 added.), Appendix G (GRD140-110 and CT connection modified.) and Appendix H (Setting sheet modified.).
0.2	Aug. 19, 2004	3.2.2	Modified the description.
		Appendices	Modified the Appendix K and M.
0.3	Sep. 01, 2005	2.1.1.1	Modified the configurable curve setting range. (k and kr corrected.)
	,	2.1.3.4	Modified the description of setting table.
		2.1.6	Modified the description.
		2.1.7	Modified the description.
		3.3.6	Modified the description.
		3.3.7	Modified Table 3.3.1.
		4.2.6.8	Modified the description.
		Appendices	Modified Appendix M.
0.4	Apr. 17, 2007	2.1.6	Added Figure 2,1.42.
		2.3	Modified the description.
		4.1.1	Modified the description.
		4.2.1	Modified the description and added Table 4.2.1.
		4.2.3.1, 4.2.4.1	Added 'Note'.
		4.2.6.6, 4.2.6.10	Modified the description.
		4.4	Modified the description.
		Appendices	Modified Appendix E, H and O.
0.5	Jul. 24, 2007	2.2.3	Modified the description.
		3.3.9	Modified the description of setting table.
		6.6.1	Added the description of 'Directional check'.
		Appendices	Modified Appendix H.
			L Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Company of the Comp

PORATION TOSHIBA CORPORATION