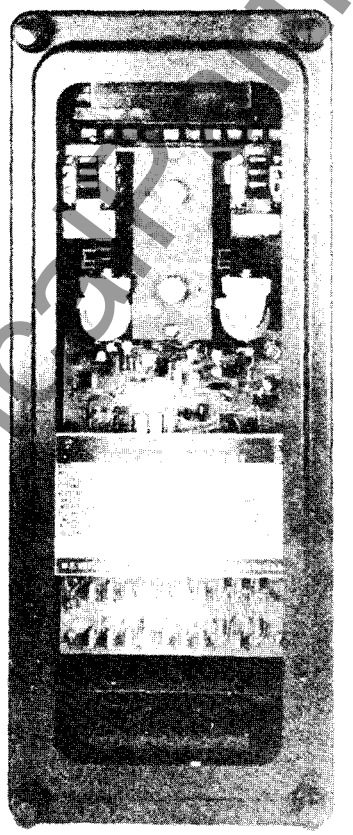
INSTRUCTIONS GEK-49923C

STATIC FREQUENCY RELAY

TYPE SFF31A,C
SFF32A,C



GENERAL ELECTRIC

* The SFF31 relays provide a single set point for underfrequency tripping. The SFF32 relays provide two set points and they are easily convertible by plug connection from MODE I, (a relay with two set points for underfrequency tripping) to MODE II (a relay with one set point for underfrequency tripping and one set point for load restoration).

The two set points of the SFF32 relay are set independently of each other over the entire range of 44 to 61 hertz. This is true whether MODE I, underfrequency tripping operation only, or MODE II, underfrequency tripping and overfrequency restoration operation, is chosen. There are two separate plug switch registers provided at the bottom of the printed circuit card on the front of the relay. The upper one is for frequency 1 (F1) and the lower one is for frequency 2 (F2) (SFF32 models only). The settings of F1 and F2 control the operation of output relays TR1 and TR2 respectively.

These relays may be set for any frequency over the range of 44 to 61 hertz, and that setting can be obtained within 0.03 hertz. This setting is repeatable within ± 0.005 hertz over the complete range of rated temperature and voltage variations. The relay is rated for 120 volts AC input and either 50 or 60 hertz system frequency.

The figures that show each relay's internal connections and outline and panel drilling are indicated in Table I. External-connection diagrams are shown in Figures 11, 12, 13 and 14.

All the relays are provided with an adjustable AC undervoltage cutoff feature. This feature operates to cut off the outputs of the relay whenever the AC input voltage is less than the preset undervoltage setting.

* The relays that are designed to operate from a DC control voltage utilize an external resistor, which is furnished with the relay and is mounted on the back of the relay case. See the external-connection diagram for the DC control voltage connections.

An indicating lamp (LED) is provided to indicate that the relay power supply is energized. This LED is mounted on the main printed circuit card and is visible just over the center of the nameplate.

APPLICATION

* The Type SFF31 and SFF32 series of static underfrequency relays are applied wherever an extremely stable device is required to provide accurate detection of underfrequency conditions. The relay may be set for any frequency over the range of 44 to 61 hertz, and that setting can be obtained within 0.03 hertz. This setting is repeatable within ± 0.005 hertz over the complete range of rated temperature and voltage variations.

While it is physically possible to make settings on the relay below 44 hertz, they are not recommended. At frequencies below 44 hertz there are errors in measurement introduced, which make the relay operation unpredictable.

The relay's minimum operating time for an underfrequency trip condition is approximately 70 milliseconds. This corresponds to one complete underfrequency cycle plus 55 milliseconds. This time is measured from the beginning of the first complete cycle of frequency below the relay set point until the relay contacts change state. In addition, an adjustable timer is provided for each underfrequency trip set point to delay the output up to a maximum of 1.3 seconds total time. The relay's minimum operating time for a 'restore' condition, where the system frequency is increasing from low to high, is approximately 30 milliseconds until the 'restore' output contacts change state. This operating time is non-adjustable. However, a complete restoration scheme will usually be designed to operate on a relatively long time basis and an external timer is recommended. Also, other auxiliary devices may be needed to implement the 'restore' function.

The AC undervoltage cutoff feature of the relay operates to cut off the relay outputs whenever the AC input voltage is less than the preset undervoltage cutoff. Its function is to prevent operation of the TR output relays. This operation takes place whether the relay is being used in a MODE I or MODE II type of

*Revised since last issue

operation, and both output relays will be de-energized. When the undervoltage cutoff feature operates, the output relays will be de-energized in less than 30 milliseconds.

As the voltage again increases above the cutoff level, reset of the cutoff will be achieved in less than 5 milliseconds. However, from this point the normal timing for a relay operating condition begins again. The adjustment range for the relay models using AC control power is 50% to 90% of rated AC voltage. The 50% lower limit is the minimum level needed to supply a reliable internal DC voltage to the relay logic. For the relay models using a DC control voltage, the AC undervoltage cutoff feature is supplied with an adjustment range of 20% to 90% of rating.

Underfrequency Tripping - General

The underfrequency trip functions of the SFF relays were specifically designed to be applied in underfrequency load-conservation schemes where the accuracy and repeatability of the measurements are important. If a system disturbance results in some loss of generating capacity, such that the load exceeds the generation, the system is in danger of collapse. The first indication of impending difficulties is a slowing down of the generators, which results in a proportionately lower frequency. Underfrequency relays distributed around the system will detect this condition and operate to disconnect system load in a programmed manner in order to compensate for the loss of generation. Such action must be taken promptly, and must be of sufficient magnitude, to enable the system to recover and so conserve the major part of the total system load. By preventing a complete system shutdown, restoration of the entire system to normal operation is greatly facilitated and expedited.

An overall load-conservation scheme can be arranged to trip off non-essential or interruptible load in several different ways:

a. Trip off blocks of load in several steps, with several relays set at successively lower frequency values;

b. Trip off blocks of load in several steps on a time basis at one level of frequency, so that as each time step is reached additional load is dropped;

c. Any combination of the two schemes described above,

When applying these relays in a system load-conservation program, it must be recognized that a low-frequency condition does not begin to be corrected until a circuit breaker operation occurs that disconnects some load. The family of curves shown in Figure 15 is constructed to show the system frequency versus the time required to disconnect load after the disturbance begins. This is shown for a wide band of rates of change of frequency, and for several different relay underfrequency trip settings. The curve calculations include an allowance of six cycles (0.1 second) for total circuit-breaker-clearing time and an allowance of 4.2 cycles (0.070 second) for the minimum relay operating time for an underfrequency trip operation. These curves allow the user to predict the clearing time and the decrease of system frequency that will occur during various parts of a load-shedding program.

The underfrequency operating characteristics of the relay are such that an underfrequency condition must persist continuously for a minimum of approximately 4.2 cycles (0.070 second) to a maximum of about 1.3 seconds, depending on the setting, before a tripping output is produced. The relay bases its measurement of frequency on the time between successive positive-going zero crossings of the voltage wave. If this voltage wave is distorted in a manner so as to affect the zero crossings, and if this distortion persists for the time-delay setting on the relay, it is possible for the relay to make an incorrect measurement of fundamental system frequency. Longer time-delay settings make this less likely to occur. If the system frequency goes above the underfrequency set point of the relay for one cycle or more during the period the relay is timing out, the relay will reset. If the underfrequency condition then recurs, the entire timing sequence must begin again.

In the application of underfrequency relays the location of the potential source from which the relay makes its frequency measurement is an important consideration. In general it is not good practice to supply a relay from a potential source that is connected to one bus section and use that relay to shed load on another bus section. Experience has indicated that the voltage and frequency of circuits to which

motor load is connected do not go to zero immediately when the circuits are de-energized. Rather, both the voltage and the frequency often decay at different rates on different circuits, depending on the characteristics of the circuit and the load. An underfrequency relay supplied from a potential source that is connected in a motor circuit could operate when the motor circuit is de-energized and the frequency decays to a value below the trip setting. Thus, if an underfrequency relay is supplied with potential from a source on a motor circuit and is connected to trip a second circuit, loss of the motor circuit could cause the relay to operate as the frequency decays, and this would result in the loss of the second circuit also. In summary, this faulty operation is caused by frequency decay if the voltage remains above the undervoltage cutoff level until the relay time-delay setting (if any) expires.

A substation that has a large amount of motor load may present a problem of time coordination in load shedding applications. If the transmission sources to such a substation were tripped out for some reason, the motor loads would tend to maintain the voltage while the frequency decreased as the motors were slowing down. This slow decay of voltage combined with a fast operation of an underfrequency relay may cause motor breakers to trip and lock out unnecessarily. In an unattended station, restoration of the motor load would not then be accomplished by simply re-energizing the transmission sources. One solution to this problem that has been applied is to select appropriate and coordinated settings of: (1) time delay of the underfrequency trip, and 2) a suitable level of undervoltage cutoff, to ride over these conditions.

While the SFF relays will be applied principally on electric utility power systems, they are also well suited for use on industrial systems. One such application is a case where an industrial installation is tapped off a power company through-transmission circuit that utilizes high-speed automatic reclosing. For faults on the through-transmission line, the power company will trip both ends of their circuit, and then they generally initiate high speed reclosing of the line. Since this reclosing is automatic, it is important for the industrial load to disconnect prior to reclosure, in order to prevent damage to motors and/or generators that may have slowed down during the interruption. An SFF relay at the industrial plant could detect the drop in frequency that may sometimes occur during the time that the power company supply is open. The relay could then trip the incoming breaker to the industrial plant and separate the plant from the power company system before reclosing takes place. Each application should be analyzed to determine the amount of frequency decay that will occur during the open-circuit period.

Underfrequency Tripping - Two-Set-Point Relays

The Type SFF32 relays are designed to provide two modes of operation:

MODE I - two set points for underfrequency tripping; or

MODE II - one set point for underfrequency tripping and one set point for overfrequency load restoration.

The desired mode of operation is set by a plug switch setting (SW21) in the upper left corner of the printed-circuit board on the front of the relay. With the plug in the TRIP 2 (plug horizontal) position, MODE I operation is chosen. With the plug in the RESTORE (plug vertical) position, MODE II operation is chosen.

In addition to placing the plug switch in the TRIP 2 position for MODE I operation, the restore supervision (RS) contact should be shorted on the restore supervision printed-circuit card mounted on the back of the relay.

* There is one movable plug provided on this card, and there are two positions available for its location. One position, immediately adjacent to the RS reed relay, is the RS contact shorting position for MODE I operation. The other position is the DC control voltage selection position for the RS relay coil. The DC control voltage selection position is used only for MODE II operation. Refer to the following section on LOAD RESTORATION for a description of the use of the RS auxiliary function.

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Load Restoration

If a load-shedding program has been successfully implemented, the system frequency will stabilize and then recover to normal frequency. This recovery is assisted by governor action on available spinning reserve generation, or by the addition of other generation to the system. The recovery of system frequency to normal is likely to be quite slow and may extend over a period of several minutes. When normal-frequency operation has been restored to an island, then interconnecting tie lines with other systems or portions of systems can be synchronized and closed in.

As the system frequency approaches normal a frequency relay can be used to begin automatically restoring the load that has been shed. The amount of load that can be restored is determined by the ability of the system to serve it. The criterion is that the available generation must always exceed the amount of load being restored, so that the system frequency will continue to recover toward normal frequency. Any serious decrease in system frequency at this point could lead to undesirable load-shedding repetition, which could start a system oscillation between shedding and restoration. The availability of generation, either locally or through system interconnections, determines whether or not the shed load can be successfully restored. Therefore, a load restoration program usually incorporates time delay, which is related to the amount of time required to add generation or to close tie-lines during emergency conditions. Also, both the time-delay and the restoration-frequency set points should be staggered so that all of the load is not reconnected at the same time. Reconnecting loads on a distributed basis also minimizes power swings across the system and thereby minimizes the possibility of initiating a new disturbance.

The 'restore' function of the SFF32 relay is intended to operate in conjunction with underfrequency trip functions in an overall load-conservation program. In general the load restoration part of this program will use substantial time delay, in the order of several minutes, which must be provided by a timer external to the SFF relay. It appears desirable to time-step the restoration so that the total shed load is restored in small blocks, with significant time between each step. In this way, as each small block of load is restored, the system has a chance to absorb this load and stabilize at its new frequency. If this frequency does not fall below the restoration frequency, then the next load block is switched on after a time delay. If the restoration of a load block causes a drop in frequency below the restoration point, this signifies that the system is loaded beyond its full capacity and the 'restore' contacts on the relay will open to prevent any further restoration until action is taken to increase the system capability.

It is obvious that a load-conservation scheme including automatic restoration will require auxiliary functions in addition to the SFF relays. The functions will depend on the exact scheme to be employed, which in turn would to some degree depend on such factors as the presence of automatic reclosing relays, the presence of supervisory control, the desire for voltage magnitude supervision, and possibly power pool agreements. However, regardless of the exact scheme, a long time delay will be required for the restoration function. The characteristic of this timer could be an important factor in the overall performance of the restoration scheme.

Since the restoration timers will be set for long time delays, it is essential that they not reset as a result of transient system frequency oscillations that may momentarily reset the 'restore' output of the associated SFF relays. The 'restore' function of the relay is provided with an adjustable time-delay reset before the contacts change state, whenever that function is subjected to a frequency change from above the 'restore' set point to below the set point (high- to low-frequency change). This delay is a maximum of 1.3 seconds. The delay setting should be very brief, only long enough to ride over a temporary underfrequency condition. If the underfrequency persists, it would likely indicate another disturbance and any load restoration program in progress should be terminated at once.

The 'restore' frequency setting of the relay will most likely be at or very close to rated frequency. If the continuous variations in normal frequency are such that the 'restore' function output relay TR2 will pick up and drop out continually, the life of this relay may be shortened. To prevent this type of operation, a reed relay (designated RS) is provided, with its contact connected in series with the 'restore' output relay coil. The RS relay is to be energized by an external device whenever an underfrequency condition has been detected and load has been shed. It should be kept energized until all the load that was shed has been restored, at which time the RS relay should be made to drop out.

In this way, the restore-output relay, TR2, will only be operable after an underfrequency condition has been detected and until the load that was shed has been restored. During normal system operating conditions, RS will be dropped out and the 'restore' feature will not operate due to minor changes in system frequency. Refer to the preceding section on UNDER FREQUENCY TRIPPING - TWO SET POINT RELAYS for additional information on the use of the RS auxiliary function.

CAUTION: Timer TD2 is intended for use in Mode I underfrequency tripping operation only. When using the SFF32 relays in Mode II for trip and restore applications, set timer TD2 to the minimum setting. Use an external time delay of at least 0.5 seconds in the restoration scheme. This will prevent an undesired initiation of the restoration scheme if the SFF relay is de-energized and then re-energized at a frequency below the restore set point.

Since there is no generally accepted scheme for the application of load conservation with automatic restoration, no complete external-connection diagram is included. However, Figures 13 and 14 illustrate the inputs to the relay and the trip- and restore-contact outputs.

SPECIFICATIONS

NOMINAL AC INPUT VOLTAGE	120 Vrms, 44 to 61 Hertz
Minimum Operating AC Input Voltage	SFF31A and SFF32A, 24Vrms SFF31C and SFF32C, 6OVrms
Maximum AC Input Voltage	135Vrms
FREQUENCY SETPOINT RANGE	
F1 and F2	44.00 to 60.98 Hertz
MINIMUM SETPOINT INCREMENTS	0.016 Hz at 44.00 Hertz 0.030 Hz at 60.98 Hertz
FREQUENCY SETPOINT ACCURACY	±0.005 Hertz
Over Temperature Range of	-20°C to 65°C
ADJUSTABLE TIME DELAY	One period of underfrequency plus 0.055 seconds to 1.3 seconds
TD1 and TD2 Repeatability	±0.010 seconds or ± 5%, whichever is greater
AC UNDERVOLTAGE CUTOFF	
Maximum	108V rms (90%)
Minimum	SFF31A & SFF32A 24Vrms (20%) SFF31C & SFF32C 60Vrms (50%)
Undervoltage Operate Time	Less than 28 milliseconds
Undervoltage Reset Time	Less than 5 milliseconds

*NOMINAL DC CONTROL VOLTAGE	Wired by user for desired voltage rating
	External resistor required for 48, 110/125VDC and 220/250 VDC operation on SFF31A and SFF32A
Minimum DC Input Voltage	80% of nominal
Maximum DC Input Voltage	112% of nominal
*NOMINAL RESTORE SUPERVISION CONTROL VOLTAGE	Selected by user for desired voltage rating
(Stud 1 must be positive voltage)	
Minimum Voltage	80% of nominal
Maximum Voltage	112% of nominal

SPECIAL FEATURES

Dual Trip Frequency Settings	SFF32A and SFF32C	
Dual Independent Time Delay	" "	
Trip 2 or Restore Mode Selection	" "	
Trip 2 or Restore Supervision by external contact	" "	
Contact Arrangement	SFF31A	1C
	SFF31C	1A,1C
	SFF32A	2A,2C
	SFF32C	2A,2C
Target Seal-in Units	SFF31A,C	1
	SFF32A,C	2
Power-on Indicator	All models	
Surge Withstand Capability	Passes ANSI/C37.90-1978	
Fast Transient	Passes Standard General Electric Tests	
RFI	Passes Standard General Electric Tests	

RATINGS

BURDENS

		Nominal
DC at Nominal Input Voltage	SFF31A	250 milliamps
	SFF32A	300 milliamps
	SFF31C	0 milliamps
	SFF32C	0 milliamps
Restore Supervision Input Voltage	SFF32A	15 milliamps
	SFF32C	15 milliamps

AC at Nominal Input Voltage (60 HZ)		VA	WATTS	VARS	MA
	SFF31A	1.32	1.3	0.2	15
	SFF32A	1.32	1.3	0.2	15
	SFF31C	11.67	10	69	5
	SFF32C	11.67	10	69	5

RELAY AMBIENT TEMPERATURE

Operating	-20°C to +55°C will not malfunction nor be damaged in ambients up to 65° C

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TELEPHONE RELAY CONTACTS

The telephone relay contacts will make and carry three (3) amperes continuously or 30 amperes for two seconds (2) at 250 VDC or 230 VAC.

Telephone relay dropout time is approximately 200 milliseconds.

TELEPHONE RELAY CONTACT INTERRUPTING RATINGS

INTERRUPTING AMPS

INTERRUPTING AMPS		
VOLTS	INDUCTIVE††	NON-INDUCTIVE
48 DC	1.0	3.0
125 DC	0.5	1.5
250 DC	0.25	0.25
115-60 Hz	0.75	2.0
250-60 Hz	0.5	1.0

†† Inductance of average trip coil

TARGET SEAL-IN COIL AND CONTACTS

TARGET AND SEAL-IN UNIT

TAP	0.2	2
DC RESISTANCE ± 10% (OHMS)	8.3	0.24
MIN. OPERATING (AMPERES)	0.2	2.0
CARRY CONT. (AMPERES)	0.37	2.3
CARRY 30 AMPS FOR (SEC.)	0.05	4
CARRY 10 AMPS FOR (SEC.)	0.45	20
60 HZ IMPEDANCE (OHMS)	50	0.65
50 HZ IMPEDANCE (OHMS)	42	0.54
MINIMUM DROPOUT (AMPERES)	0.05	0.5

If the trip current exceeds 30 amperes, it is recommended that an auxiliary tripping relay be used.

CALCULATION OF SETTINGS

The frequency setpoint is determined by the ten plug switches, SW1 through SW1O for F1 (upper register) and SW11 through SW2O for F2 (lower register in SFF32 models). Note that each plug switch has a "0"(lower) or "1" (upper) position, and it also has a number above it that corresponds to the number of microseconds represented by the switch when it is in the "1" position. The relay has a basic reference setpoint period of 16,400 microseconds when all the setpoint switches are in the "0" position. The basic reference frequency is determined by dividing 106 microseconds by 16,400 microseconds, which is 60.98, nominally 61 hertz. The value in microseconds of time for each of the plug switches is shown in the table below:

PLUG SWITCH	10	9	8	7	6	5	4	3	2	1
TIME in microseconds	4096	2048	1024	512	256	128	64	32	16	8

The total time period in microseconds for a given set of plug switch settings will be 16,400 plus the time value of each plug switch that has been placed in the "1" position.

When the desired trip frequency (TF) has been determined, refer to Tables VI and VII (at the end of the text, before the figures) to determine the required position, "1" or "0", for each of the plug switches in a register. If the plug switch settings have been made according to the table, the set trip frequency can be checked by calculation, using the following equation:

$$TF\ (Hz) = \frac{10^6}{16{,}400 + \text{sum of plug switches}}$$

where "sum of plug switches" refers to all switches that have been placed in the "1" position. The above equation can be transformed so as to be able to determine the necessary plug switch setting for any frequency, as follows:.

$$\text{Period (microseconds)} = \frac{10^6}{TF}$$

For example a TF of 58.56 would have a period of

$$\text{Period (microseconds)} = \frac{10^6}{58.56} = 17076.5, \text{ rounded to } 17077$$

The necessary plug switch settings are determined as follows:

1. 17,077 minus 16,400 = 677
2. Set plug switch 7 (highest time value less than 677) in position "1"; 677 minus 512 = 165
3. Add plug switch 5; 165 minus 128 = 37
4. Add plug switch 3; 37 minus 32 = 5
5. * Actual period = 16,400 plus 512 plus 128 plus 32 = 17072 microseconds
6. Actual frequency = TF = $10^6/17072 = 58.5754$ Hz
7. Error

$$\frac{58.5754-58.56}{58.56} \times 100 \quad \frac{0.0154}{58.56} = +0.0264\ \%$$

8. * Put in plug switch "1" to add eight (8) microseconds; actual period becomes 17080 microseconds, actual frequency becomes 58.548 Hz
9. Error

$$\frac{58.548 - 58.56}{58.56} \times 100 \quad \frac{-0.012}{58.56} = -0.0204\ \%$$

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CHARACTERISTICS

OPERATING PRINCIPLES (Refer to Figure 16)

The basic SFF31 relay monitors an AC voltage and closes a telephone relay contact (TR1) when the frequency of the input voltage remains less than a frequency setpoint value (F1) for a preset time period (TIME DELAY 1). F1 is determined by ten plug switches (SW1-SW1O) mounted on the large printed circuit card on the front of the relay. TIME DELAY 1 is set by the locking potentiometer (R4) mounted above the main printed-circuit card. The relay, (TR1) is de-energized when the magnitude of the AC input voltage is less than a preset value determined by the undervoltage-adjust locking potentiometer (R20) located in the upper right-hand corner of the main printed-circuit card. A manually resettable target and seal-in contact (TSI1) is energized by external DC trip current after the relay contact TR1 closes.

A second model (SFF32) relay contains all the features of the SFF31 relay, and in addition, has a second independent frequency setpoint value (F2), an independent preset time period (TIME DELAY 2) and a second set of telephone relay contacts (TR2). F2 is determined by ten plug switches (SW11-SW2O) mounted on the bottom of the main printed circuit card. TIME DELAY 2 is set by the lower locking potentiometer (R5) mounted above the main printed- circuit card. The AC undervoltage adjust inhibits both TR1 and TR2.

* A separate, manually resettable target and seal-in contact (TSI2) is energized by external DC trip current after the relay contact, TR2, closes. The telephone relay coil of TR2 is supervised by a separate contact converter circuit. The contact converter input DC voltage can be chosen by properly selecting a jumper switch located on the small RESTORE SUPERVISION card mounted at the rear of the relay. If the RESTORE SUPERVISION feature is not desired, the jumper must be in the RS position. The second set point can be used in a TRIP 2 or a RESTORE mode.

Switch SW21 is the plug on the upper-left corner of the printed-circuit card of SFF32 models. It is used to select the operating mode of the relay. When SW21 is in the TRIP 2 position, the TR2 relay is energized if the input frequency remains below the F2 set point for the TIME DELAY 2 setting. When SW21 is in the RESTORE position, the TR2 relay is energized when the frequency is above the F2 set point. The TIME DELAY, TD2, starts when the frequency passes through the F2 set point while going toward a lower frequency.

* A POWER ON indicator located on the main printed circuit card assures the operator that the power supply is energized. Control power for the SFF31A and 32A models is provided by an external DC voltage source. Selection of the proper voltage is made by proper connection to the external power resistor. Internal regulation is provided by two zener diodes. Control power for the SFF31C and 32C models is obtained from the AC input, through a built-in power supply and integrated circuit regulator (IC1).

The basic measurement technique is based on measuring the period of successive cycles of the input voltage. The time between positive-going zero crossing points of the AC input voltage is measured, and a precise comparison made with a known timing period. The known timing period is generated by a stable crystal oscillator and a sixteen stage binary counter. The counter is reset to the all-zero state by the zero-crossing pulse. Sixteen microseconds after the zero crossing, the counter is allowed to count up. The state of counter stages 5 through 14 are monitored by an eleven-input AND gate. Switches SW1 through SW1O select the normal or inverted counter output for input to the AND gate. The eleventh input to the AND gate is permanently connected and disables the gate for 16,384 microseconds after the zero crossing. If switches SW1 through SW1O are kept in the "0" position, the known timing period is equal to 16,400 micro-seconds, which corresponds to a frequency of 60.98 hertz. At the end of the timing period, all inputs to the AND gate will rise and produce an output to the pulse stretching circuit. The AND gate output is only eight microseconds (8 ms) long, but it is stretched to about 30 milliseconds. If a gate output pulse is continuously received every cycle, the TIME DELAY 1 is enabled, and after it completes its elapsed time period, it turns on an output transistor switch, which in turn energizes a telephone relay. However, if the time between successive zero crossings is shorter than the relay set point period, TIME DELAY 1 is reset in less than 30 milliseconds.

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A set point lower than 60.98 hertz is obtained by moving the appropriate plug switches, SW1 through SW1O, to the "1" position. Each switch in the "1" position adds its indicated delay (8 through 4096) to the basic time delay of 16,400 expressed in microseconds. For example, if SW8 (32), SW5 (256) and SW4 (512) are in the "1 "position, the known timing period is:

16,400 + 512 + 256 + 32 = 17,200 microseconds,
which corresponds to 58.140 hertz.

The dual trip (SFF32) models use the same sixteen stage counter as a time reference for the second trip function, but they use a different AND gate. A separate pulse stretcher, TIME DELAY 2, output transistor Q10 and telephone relay TR2 are used for the second trip function. An optional contact converter input supervises the output of the second trip function, and it can be shorted out with a built-in plug switch if desired.

If the second frequency set point (F2) is used as a RESTORE function by setting SW21 to RESTORE, an inverter stage gate is introduced between the TIME DELAY 2 output and the input to transistor Q10.

An adjustable AC undervoltage cutoff circuit disables the telephone relays when the input voltage drops below the preset set point for at least 28 milliseconds.

The fully rectified input signal is attenuated by the UNDERVOLT ADJUST potentiometer, R20. The attenuated signal is then compared to a voltage-reference diode ZD18, and if the instantaneous input voltage is greater than the voltage-reference diode, transistor Q4 is switched on momentarily. When Q4 turns on, it discharges a timing capacitor, C10. As long as capacitor C10 is discharged every half cycle, the input voltage at IC9C is less than five (5V) volts. If the AC system voltage drops below the preset level determined by R20, the transistor, Q4, remains off and the capacitor, C10, charges to above five (5V) volts in approximately 28 milliseconds, which imposes a steady-state clear signal on the sixteen-stage counter and simultaneously holds the main time-delay capacitors (C14 and C20) in a discharge mode. The output of the RESTORE inverter, IC10D, is also forced to an off state, so that the TR2 relay is de-energized for an undervoltage condition.

DETAILED PRINCIPLES OF OPERATION - SEE FIGURES. 6, 7, 8, 9 and 10 thru 10C

Main Underfrequency Printed-Circuit Board (not shown)

The AC input signal from transformer TA is filtered by R13 and C7 before being squared by transistor Q3. Q3 is turned on when the input sine wave is positive and turned of when the sine wave is negative. When the collector of Q3 is switched down to reference, the output of IC9A also is switched down to reference. IC9 and IC10 integrated circuits are high speed, stable comparators with an NPN transistor collector as an output terminal. Four independent comparators are contained in each package. All comparator reference inputs are connected to the five volt (5V) bus. If the unknown input is connected to the plus (+) comparator input, the NPN output transistor will be turned on when the unknown input is less than five volts (<5V). If the unknown input signal is connected to the minus (-) input, the NPN output transistor will be turned on when the input is greater than five volts (>5V).

After the output of IC9A is switched to reference, C9, (which initially has no charge), causes the input of IC9B to switch to reference level. The output of IC9B is turned on and produces the start of the 'clear' pulse for the binary counter.

The output of IC9A will be at reference level for one-half cycle or about eight milliseconds (8ms). However, C9 will charge up toward ten (10V) volts through R17, and when the C9 voltage exceeds five (5V) volts, it will switch IC9B output off. The width of the 'clear' pulse is 16 microseconds. After the 'clear' pulse ends, the binary counter is allowed to begin counting.

The binary counter (see Figure 16) contains sixteen stages with two flip-flops in each integrated circuit package (IC1 through IC8). Each pair of flip-flops are controlled by a common CLOCK PULSE input (CP) and a common CLEAR DIRECT input (CD). Each flip-flop contains a "J" input, a "K" input, a normal output (Q) and a complementary output (Q'). The two flip-flops in each package are identified by a suffix, (a) or (b). The (b) flip-flop always operates at twice the frequency of the (a) flip-flop in the SFF relay. The operation of IC1 is representative of IC2 through IC8 except for operating frequency. The (b) flip-flop of IC1 has its JK inputs tied to plus five (5V) volts and this causes the (b) output to change state when the clock input (CP) goes negative. The (a) flip-flop of IC1 has its JK inputs tied to the normal output of the (b) flip-flop. The JK truth table is shown in Table II.

TABLE II - FLIP-FLOP TRUTH TABLE

t_n		$t_n + 1$
J	K	Q
0	0	Qn
1	0	1
0	1	0
1	1	$\overline{Q}$'n

The (a) flip-flop will only change state when the clock goes negative and the normal output of the (b) flip-flop is in a "1" state. The frequency output of (a) will then be one-half the frequency of (b). The period of each flip-flop is shown in Table III.

TABLE III - BINARY COUNTER PERIODS

SW Nos.	IC No.	Output Pin No.	Period
	1b	8	1 µs
	1a	6	2 µs
	2b	8	4 µs
	2a	6	8 µs
10&20	3b	8	16 µs
9&19	3a	6	32 µs
8&18	4b	8	64 µs
7&17	4a	6	128 µs
6&16	5b	8	256 µs
5&15	5a	6	512 µs
4&14	6b	8	1024 µs
3&13	6a	6	2048 µs
2&12	7b	8	4096 µs
1&11	7a	6	8192 µs
	8b	8	16384 µs
	8a	6	32768 µs

Note that IC8a is permanently connected to the AND gate and determines the time base of 16,400 micro-seconds which is equal to the 16 microsecond delay for beginning the count (the width of the 'clear' pulse), plus the 16,384 microsecond zero level gate output from IC8a. The frequency-select switches connect the AND gate to either the normal or the complementary outputs of the fifth through the fourteenth flip-flops in the chain of sixteen. When the 'clear' pulse occurs, all sixteen normal flip-flop

outputs go to the "0" level (see Figure 17). When the clear pulse ends, the counter begins counting. Since the two-megahertz (2MHz) crystal oscillator is running asynchronously, there is a one-half microsecond uncertainty in the reference period of 16,400 microseconds. Figure 17 is a timing diagram showing the initial state of the counter after the 'clear' pulse ends. The initial timing is not affected by the set point. Figure 18 is a timing diagram showing the final state of the counter for a frequency set point of 58.01 hertz. The 'clear 'pulse is shown for reference only. The AND gate output is shown as an eight microsecond (8μs) wide pulse occurring 17,240 microseconds after the start of the 'clear' pulse. The AND gate output is high when all eleven inputs are high. If any gate input is low, the gate output will be low. For the example shown in Figure 18, the normal outputs "1" of the 8, 64, 256, and 512 flip-flop stages and the complementary outputs "0" of the 16, 32, 128, 1024, 2048 and 4096 flip-flop stages are switched into the AND gate. The normal output of the "16386" stage is permanently connected to the eleventh input of the AND gate. Control of the AND gate is by the "0" level inputs and the order of sequence is as follows:.

Microseconds	Control input	Control Pulse Width Microseconds
0 to 16	Clear pulse	16
16 to 16400	IC8-6 normal output	16384
16400 to 16912	IC6-8 normal output	512
16912 to 17168	IC5-6 normal output	256
17168 to 17232	IC4-6 normal output	64
17232 to 17240	IC3-8 normal output	8

Since the 'clear' pulse period (or zero crossings of the input signal) is greater than the reference time period of 17,240 microseconds, an underfrequency condition will be detected by the AND gate output pulse occurring once every cycle of the input sine wave. All sixteen stages of the counter are shown switching from zero to five volts for simplicity. Actually, the first eight stages (lC1 through lC4) operate between zero and five volts but the final eight stages (lC5 through lC8) operate between five and ten volts (5V - 10V). Arranging the counter in this manner allows the DC current drain of the counter to be cut in half. Interfacing is accomplished by five volt (5V) reference diode ZD2 (for clear pulse), ZD3 (for stage 8 to stage 9 connection) and ZDll (for AND gate connection between stage 8 and stage 9).

The AND gate output pulse is only eight microseconds (8 μs) wide and must be stretched to about 30 milliseconds. Q5 and Q6 amplify the pulse to a level capable of charging C13 from zero to 10 volts in less than one microsecond (<1 μs). The decay of the voltage on C13 is determined by R30. The normal decay time from 10 to 5 volts is about 30 milliseconds. However, as long as an underfrequency pulse is received each cycle, C13 its continually recharged to 10 volts and thus maintains the input to IC10A above the five-volt (5 V) reference level. An input greater than five-volts (<5V) to IC10A turns off the output transistor stage of IC10A and allows C14 to charge toward ten volts (10V). The charge time is determined by R32 in series with the potentiometer R4 (mounted off the board). When the C14 voltage exceeds the five volt level, the output of IC9D turns on, and Q7 is then turned on, energizing the telephone relay coil. The telephone relay contacts energize the target seal-in unit and the proper circuit breaker is opened.

The trip-delay time is measured from the first eight microsecond (8 μs) underfrequency pulse from the AND gate to the closing of the telephone relay contacts. Since the first underfrequency pulse occurs after one whole cycle of underfrequency has elapsed, a time equal to the trip set point period should be added to the measured time. If this is done, the theoretical trip-delay time is from the first positive zero crossing of the input voltage.

The AC undervoltage detector operates on a full-wave rectified signal from transformer TA. The rectification is done by D45 and D46. Series resistors R1 and R2 (on the chassis), R20 and R21 make a voltage divider circuit for attenuating the rectified sine wave. When R20 is fully counterclockwise (MIN setting), the maximum signal is obtained from the voltage divider. Therefore, the input signal must go lower in value before Q4 is continuously cut off. An undervoltage condition prevents the five-volt (5V)

reference diode, ZD18, from conducting and turning on Q4. A time delay of approximately 28 milliseconds occurs after detection of an undervoltage. The reset time of the under voltage circuit is less than a quarter cycle of the input signal. The undervoltage control is from the output transistor in IC9C and when it is turned on, it clears all stages of the counter, resets the TIME DELAY 1 and TIME DELAY 2 capacitors (C14 and C20 respectively) and disables the RESTORE inverter, IC10D. The power supply for the DC models (A suffix) consists of two (2) five-volt reference diodes, ZD25 and ZD26. Current limiting is by R3 (SFF31A) or R3/R6 (SFF32A) and the tapped external resistor.*

The self-contained power supply for the AC models (C suffix) is on the chassis, and consists of an isolation transformer, TB, a full-wave bridge rectifier, D1, D2, D3, D4, a capacitor filter, C1, and a 10VDC three-terminal regulator, IC1. The AC power supply is operable down to 50% of rated input voltage. Since the AC power supply provides regulated 10 VDC for the main printed circuit card, ZD25 is not required on AC models. The load current required for IC5 through IC8 provides the bias current for ZD26.

* The RESTORE SUPERVISION card is mounted at the rear of the relay and provides a means of externally supervising the operation of TR2. Energization of the reed relay (RS) closes a contact that completes the internal coil circuit of TR2. The DC control power for the RESTORE SUPERVISION board is selected by a jumper switch . Proper DC control power polarity must be maintained. If the RESTORE SUPERVISION feature is not used, the jumper switch is used to short-circuit the reed relay contacts (RS position).

CONSTRUCTION

CASE

The components of each relay are mounted on a cradle assembly that can be easily removed from the relay case. The cradle is locked in the case by means of latches at the top and bottom. The electrical connection between the case blocks and cradle blocks is completed through removable connection plugs. See Figure 20. Separate testing plugs can be inserted in place of connection plugs to permit testing the relay in its case. The cover is attached to the front of the case and includes two interlock arms that prevent the cover from being replaced until the connection plugs have been inserted.

The case is suitable for semiflush mounting on panels. Hardware is available for all panel thicknesses up to two inches. A panel thickness of 1/8 inch will be assumed unless otherwise specified on the order. Outline and panel drilling dimensions are shown in Figures 21 and 22.

Two printed circuit boards contain most of the circuit components. The main underfrequency card is vertically mounted on the front of the relay by two screws and two hexagonal studs holding the nameplate. Connections to the card are made with two connection blocks. Use care when removing or attaching the connector blocks to ensure that they are properly aligned laterally and that the pins are straight and enter the connector properly. Each electrical-card connection is made through a double set of wires and connectors.

The RESTORE SUPERVISION card is a small card horizontally mounted on the rear of the relay by two screws. This card is only used on the SFF32 models. Connections to the board are soldered to the turret standoffs.

The target seal-in units are front-mounted above their respective telephone relay tripping units. Target contacts and tap settings are easily accessible from the front of the relay.

The telephone relays are mounted above the main printed-circuit card and the armature and contacts are easily accessible from the front of the relay.

The time-delay potentiometers are mounted in the center of the relay above the main printed-circuit board. Each potentiometer has a screw slot and is equipped with a lock nut.

*Revised since last issue

* The input transformers, power resistors and surge-suppression components are all mounted in the rear of the relay. AC-powered models contain a power supply transformer, rectifier, capacitor and regulator mounted in the rear of the relay. The regulator is mounted to an aluminum heat sink with high thermal conductivity heat sink compound, and tightened to the proper torque for maximum heat transfer.

RECEIVING, HANDLING AND STORAGE

These relays, when not included as a part of a control panel, will be shipped in cartons designed to protect them against damage. Immediately upon receipt of a relay, examine it for any damage sustained in transit. If injury or damage resulting from rough handling is evident, file a damage claim at once with the transportation company and promptly notify the nearest General Electric Sales Office.

Reasonable care should be exercised in unpacking the relay in order that none of the parts are injured, nor the adjustments disturbed.

If the relays are not to be installed immediately, they should be stored in their original cartons in a place that is free from moisture, dust, and metallic chips. Foreign matter collected on the outside of the case may find its way inside when the cover is removed and cause trouble in the operation of the relay.

ACCEPTANCE TESTS

GENERAL

The relay should be examined and tested upon delivery to make sure that no damage has been sustained in shipment and that the relay functions properly. If the examination or acceptance tests indicate that readjustment is necessary, refer to the section on SERVICING.

The following tests may be performed as part of the installation of the relay, at the discretion of the user. Since most operating companies use different procedures for acceptance and for installation tests, the following section includes all applicable tests that may be performed on the relays.

VISUAL INSPECTION

Check the nameplate stamping to make sure that the model number agrees with Table I.

Remove the relay from its case and check that there are no broken or cracked molded parts or other signs of physical damage, and that all the screws are tight.

MECHANICAL INSPECTION

1. The armature and contacts of the seal-in unit should move freely when operated by hand. There should be at least ten (10) mils wipe on the seal-in unit contacts.

CAUTION:	**Mechanical adjustment of the target seal-in is not recommended. Improper adjustment of the telephone relay or target seal-in may affect seismic performance.**

2. The target in the seal-in unit must come into view and latch when the armature is operated by hand and should unlatch when the target release lever is operated.

3. The telephone relay units used in these relays should be checked to have a contact gap of at least 10 mils and a contact wipe of 5 mils. The contact wipe may be checked by inserting a 5 mil shim between the armature and pole piece and operating the armature by hand. The normally-open contacts should make contact with the shim in place when the armature is operated by hand.

4. Make sure that the fingers and shorting bars in the relay cradle and case blocks agree with the internal connections diagram. The internal connections diagrams are included here as Figures 6, 7, 8 and 9.

CAUTION:	**Every circuit in the drawout case has an auxiliary brush. It is especially important on current circuits and other circuits with shorting bars that the auxiliary brush be bent high enough to engage the connecting plug or test plug before the main brushes do. This will prevent CT secondary circuits from being open-circuited during insertion of the connecting plug.**

DRAWOUT CASE

Since all drawout relays in service operate in their cases, it is recommended that they be tested in their cases or an equivalent steel case. In this way any magnetic effects of the enclosure will be accurately duplicated during testing. A relay may be tested without removing it from the panel by using a 12XLA13A test plug. This plug makes connections only with the relay and does not disturb any shorting bars in the case. Of course, the 12XLA12A test plug may also be used. Although this test plug allows greater testing flexibility, it also requires CT shorting jumpers and the exercise of greater care, since connections are made to both the relay and the external circuitry.

CAUTION:	**When hi-potting the SFF relay, remove all wiring from Terminal 6. The reason is that surge capacitors are only rated for 600 VDC continuous and the hi-pot voltage may damage the capacitor.**

POWER REQUIREMENTS, GENERAL

All alternating-current-operated devices (AC) are affected by frequency. Non-sinusoidal waveforms can be analyzed as a fundamental frequency plus harmonics of the fundamental frequency. It follows that alternating-current devices (relays) will be affected by the application of non-sinusoidal waveforms.

Therefore, in order to test alternating current relays properly it is essential to use a sine wave of current and/or voltage. The purity of the sine wave (i.e., its freedom from harmonics) cannot be expressed as a finite number for any particular relay; however, any relay using tuned circuits, RL or RC networks, or saturating electromagnets (such as time-overcurrent relays) would be affected by non-sinusoidal wave forms.

Similarly, relays requiring DC control power should be tested using DC, and not full-wave rectified power. Unless the rectified supply is well filtered, many relays will not operate properly, due to the dips in the rectified power. Zener diodes, for example, can turn off during these dips. As a general rule, the DC source should not contain more than 5% ripple.

TARGET/SEAL-IN UNIT TAP SETTING

When trip-coil current falls within the range of 0.2 to 2.0 amperes at minimum control voltage, the tap screw of the target seal-in unit should be set in the low-ampere tap. When the trip coil current ranges from 2 to 30 amperes at minimum control voltage, the tap screw should be placed in the 2.0 ampere tap. The tap screw for the seal-in unit is the screw holding the right-hand stationary contact of the seal-in unit. To change the seal-in unit tap setting, first remove the relay connection plugs. Then take a screw from the left-hand stationary contact and place it in the desired tap. Next, remove the screw from the other, undesired, tap and place it back in the left-hand contact. This procedure is necessary to prevent the right-hand stationary contact from getting out of adjustment. Screws should **never** be left in **both** taps at the same time.

TARGET/SEAL-IN UNIT CHECK

The pickup and dropout of the target seal-in unit can be tested as follows.

1. Connect the proper relay studs to a DC source, ammeter, and load box so that the target coil current can be controlled over a range of 0.1 to 2.0 amperes DC.

2. Short the TR contacts by manually closing the telephone relay contacts.

3. Increase the current slowly until the seal-in unit picks up. See Table IV for correct pickup values.

4. Release the telephone relay; the seal-in unit should remain in the picked up position.

5. Decrease the current slowly until the seal-in unit drops out. See Table IV for correct dropout values.

TABLE IV

UNIT	TAP	PICKUP AMPERES	DROPOUT AMPERES
0.2/2.0	0.2	0.15 - 0.195	0.05 or more
	2.0	1.50 - 1.95	0.5 or more

FREQUENCY SETPOINT CHECK

If a variable-frequency oscillator is not available, the relay operation can be checked using a normal 60 hertz input by setting the plug switches to 0000100001 (60.10 hertz) and checking for trip action. Change the plug-switch setting to 0000100010 (59.981 hertz) and check for **no** trip action. If chatter is encountered in either of the preceding checks, try the next higher 0000100000 (60.038) or lower 0000100011 (59.952) setting, which should provide a stable trip or no-trip state respectively.

NOTE: When checking the frequency setting, if highest accuracy is required, the time delay should be set at minimum. This is necessary because the relay will not trip unless the highest frequency during the trip time delay is lower than the set point. If the AC power source has slight variations in frequency, the frequency indication of the AC power source will usually be the average rather than the highest frequency, and this indicated value will not be the true operating point of the relay.

TIME-DELAY CALIBRATION

The time delay is best measured with a dual-trace storage oscilloscope. A normal single-trace oscilloscope may be used if external trigger input is provided, but it is more difficult to obtain the desired results.

The time delay is measured from the detection of the first underfrequency pulse until the TR telephone relay contacts close. The underfrequency pulse is easily measured by attaching a 10 megohm probe to R29 on the UF board for the F1 time delay (TD1) or R41 for the F2 time delay (TD2) (see figures 24 and 25). Reference can be obtained from the lower end of C15. The test arrangement is shown in Figure 19.

For the SFF32 series, set the relay in MODE I (SW21 on the UF board in TRIP 2 position and RESTORE SUPERVISION, also on the UF board, in RS position) for the time-delay calibration test. Set the desired frequency set point and follow the test sequence listed in Figure 19. The oscilloscope should be triggered on positive DC, and either from EXT TRIGGER or from CHANNEL A. Use a 10 megohm input impedance probe for attachment to R29 and R41. Adjust the TIME DELAY 1 or TIME DELAY 2 potentiometers for desired time delay, and lock. Check the time delay again after locking the potentiometer, and readjust if necessary.

For periodic testing, a test set-up is shown in Figure l9B. This method does not consider the point in the voltage cycle where the underfrequency condition is applied, nor is any attempt made to be consistent in starting the underfrequency condition at the same point for successive readings. Thus the time delay can vary up to one cycle of the set-point frequency. For time delays greater than 500 milliseconds, this variation in the start time is less than five percent (<5%).

***CAUTION:** **Do not set the time delay to the full CCW (minimum) position. Misoperation may occur when AC is switched off if the time delay is below 70 milliseconds.**

INSTALLATION PROCEDURE

INTRODUCTION

The relay should be installed in a clean, dry location, free from dust and excessive vibration, and well lighted to facilitate inspection and testing.

The relay should be mounted on a vertical surface. The outline and panel drilling dimensions are shown in Figures 21 and 22.

The internal connection diagrams for the relays are shown in Figures 6, 7, 8 and 9. Typical external connection diagrams are shown in Figures 11, 12, 13 and 14.

CAUTION: **DC -powered relays must use the proper external resistor. Do not use resistors from former SFF models.**

SURGE GROUND AND RELAY CASE GROUND CONNECTIONS

***CAUTION:** **One of the mounting studs or screws should be permanently connected to ground by a conductor not less than No. 12 AWG (≥ 12AWG) copper wire or its equivalent. This connection is made to ground the relay case. In addition, the terminal designated as "surge ground" on the internal-connections diagram must be tied to the station ground bus for the surge suppression networks in the relay to perform properly. This surge ground lead should be as short as possible, to ensure maximum protection from surges (preferably ten inches or less (≤10") to reach a solid ground connection).**

With terminal 6 connected to ground, "surge ground" is connected electrically to the relay case. The purpose of this connection is to prevent high-frequency transient potential differences from entering the solid-state circuitry. Therefore, with terminal 6 connected to ground the surge capacitors are connected between the input terminals and the case. **Caution** must be exercised when hi-potting between these terminals and the case.

*Revised since last issue

CAUTION:	**The surge capacitors used in this relay are not suitable for AC hi-pot testing, thus the surge ground lead must be removed from terminal 6 when high-potting.**

The surge capacitors are not subjected to high-frequency surge potentials of any appreciable level as their impedance at surge frequencies is very low, less than one ohm (1Ω) usually, and the various source and circuit impedances along the surge path to the relay usually limit the surge currents to less than 25 amperes. Therefore, the surge voltage drop across a surge capacitor is small.

Surge capacitors of sufficient voltage rating to pass relay hi-pot tests are physically large; too large in fact to allow use of the required numbers inside most component relays as surge filter elements. We are continually monitoring developments in this area in an effort to be able to respond to requests for such ratings. To date, no practical capacitor of suitable compactness has been found.

Hipot is defined by ANSI C37.90 under the section entitled "Dielectric Tests".

TEST PLUGS

The relay may be tested without removing it from the panel, by using a 12XLA13A test plug. This plug makes connections only with the relay and does not disturb any shorting bars in the case. Of course, the 12XLA12A test plug may also be used. Although this test plug allows greater testing flexibility, it also requires CT shorting jumpers and the exercise of greater care, since connections are made to both the relay and the external circuitry. Additional information on the XLA test plugs may be obtained from the nearest General Electric Sales Office.

ELECTRICAL TESTS AND SETTINGS

Most operating companies use different procedures for acceptance tests and for installation tests. The section under ACCEPTANCE TESTS contains all necessary tests, which may be performed as part of the installation procedure.

Procedures for setting the relay are discussed in the SERVICING section in this book.

SERVICING

GENERAL

Before removing the cover, remove any dust or foreign matter that has accumulated on the top of the cover. Otherwise it may find its way inside when the cover is removed and cause trouble in the operation of the relay.

TARGET/SEAL-IN UNIT TAP SETTING

Refer to the section of this same title under ACCEPTANCE TESTS for details on changing taps.

CONTACT CLEANING

For cleaning contacts, a flexible burnishing tool should be used. This consists of a flexible strip of metal with an etch-roughened surface, resembling in effect, a superfine file. The polishing action is so delicate that no scratches are left, yet corroded material will be removed rapidly and thoroughly. The flexibility of the tool ensures the cleaning of the actual points of contact

Contacts should not be cleaned with knives, files or abrasive paper or cloth. Knives or files may leave scratches, which increase arcing and deterioration of the contacts. Abrasive paper or cloth may leave minute particles of insulating abrasive material in the contacts, thus preventing closing. The use of

contact cleaning sprays or liquids should be avoided because some of these liquids may leave deposits in portions of the relay that may be injurious to materials or components.

The burnishing tool described above can be obtained from the factory.

PERIODIC CHECKS AND ROUTINE MAINTENANCE

In view of the vital role of protective relays in the operation of a power system it is important that a periodic test program be followed. It is recognized that the interval between periodic checks will vary depending upon environment, type of relay, and the user's experience with periodic testing. Until the user has accumulated enough experience to select the test interval best suited to his individual requirements, it is suggested that the points listed under ACCEPTANCE TESTS be checked at an interval of from one to two years.

The telephone-type relay units should be checked to see that they operate smoothly and that their contacts are correctly adjusted.

With each telephone-relay unit de-energized, each normally-open contact should have a gap of 0.010 to 0.015 inch. Each normally-closed contact should have wipe (overtravel after contact) of 0.005 inch. This can be observed by deflecting the stationary contact member toward the frame.

In the energized position each normally-open contact should have approximately 0.005 inch wipe. This can be checked by inserting a shim between the armature and pole piece, and operating the armature by hand. Use an 0.0025 shim for the TR relays. The normally-open contacts should close before the residual screw or armature strikes the shim.

RENEWAL PARTS

It is recommended that sufficient quantities of renewal parts be carried in stock to enable the prompt replacement of any that are worn, broken, or damaged.

It is not recommended that renewal parts obtained from sources other than the General Electric Company be used. Many of the parts that appear superficially similar to parts generally available have special features or construction that is not apparent on inspection. This is true in some cases even though the parts may have the same manufacturer's part number. Other parts, while the same as those generally available, are specially selected or tested for their specific applications.

Should a printed-circuit card become inoperative, it is recommended that this card be replaced with a spare. In most instances, the user will be anxious to return the equipment to service as soon as possible and the insertion of a spare card represents the most expeditious means of accomplishing this. The faulty card can then be returned to the factory for repair or replacement.

Although it is not generally recommended, it is possible with the proper equipment and trained personnel to repair cards in the field. This means that a trouble-shooting program must isolate the specific component on the card that has failed. By referring to the internal-connection diagram for the card, it is possible to trace through the card circuit by signal checking, and hence, determine which component has failed. This, however, may be time consuming and if the card is being checked in place in its unit, as is recommended, will extend the outage time of the equipment.

CAUTION: **Great care must be taken in replacing components on the cards. Special soldering equipment suitable for use on the delicate solid-state components must be used, and, even then, care must be taken not to cause thermal damage to the components, and not to damage or bridge over the printed circuit buses. The repaired area must be re-covered with a suitable high-di-electric plastic coating to prevent possible breakdowns across the printed-circuit buses due to moisture or dust.**

ADDITIONAL
CAUTION: Dual in-line integrated circuits are especially difficult to remove and replace without specialized equipment. Furthermore, many of these components are used in printed-circuit cards that have bus runs on both sides. These additional complications require very special soldering equipment and removal tools, as well as additional skills and training, which must be considered before field repairs are attempted.

When ordering renewal parts, address the nearest Sales Office of the General Electric Company, specify quantity required, name of the part wanted, and the complete model number of the relay for which the part is required.

LIST OF FIGURES

*Revised since last issue

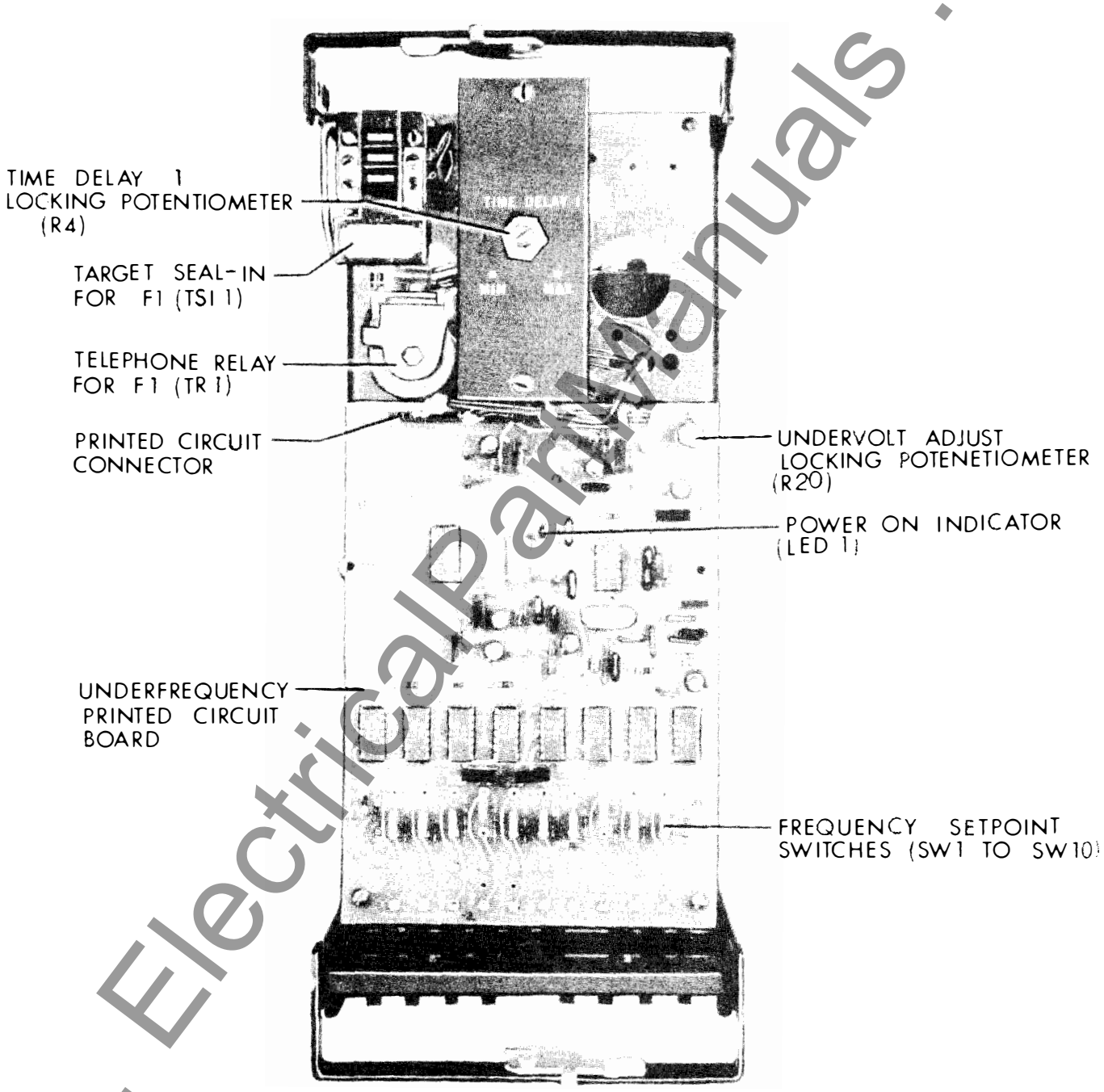


Figure 1 (8043419) SFF31C - Front View Removed from Case

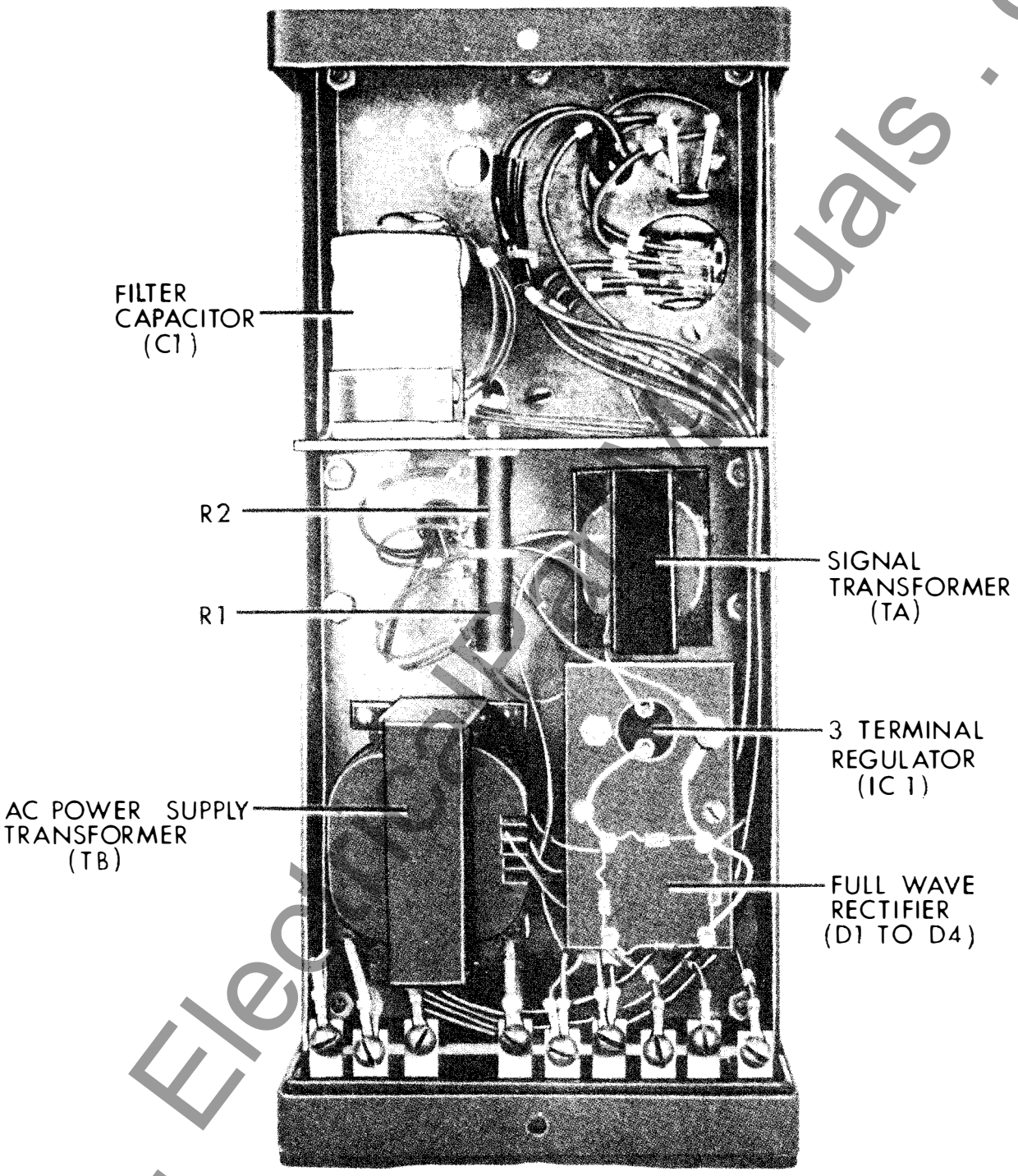


Figure 2(8043420) SFF31C - Rear View Removed from Case

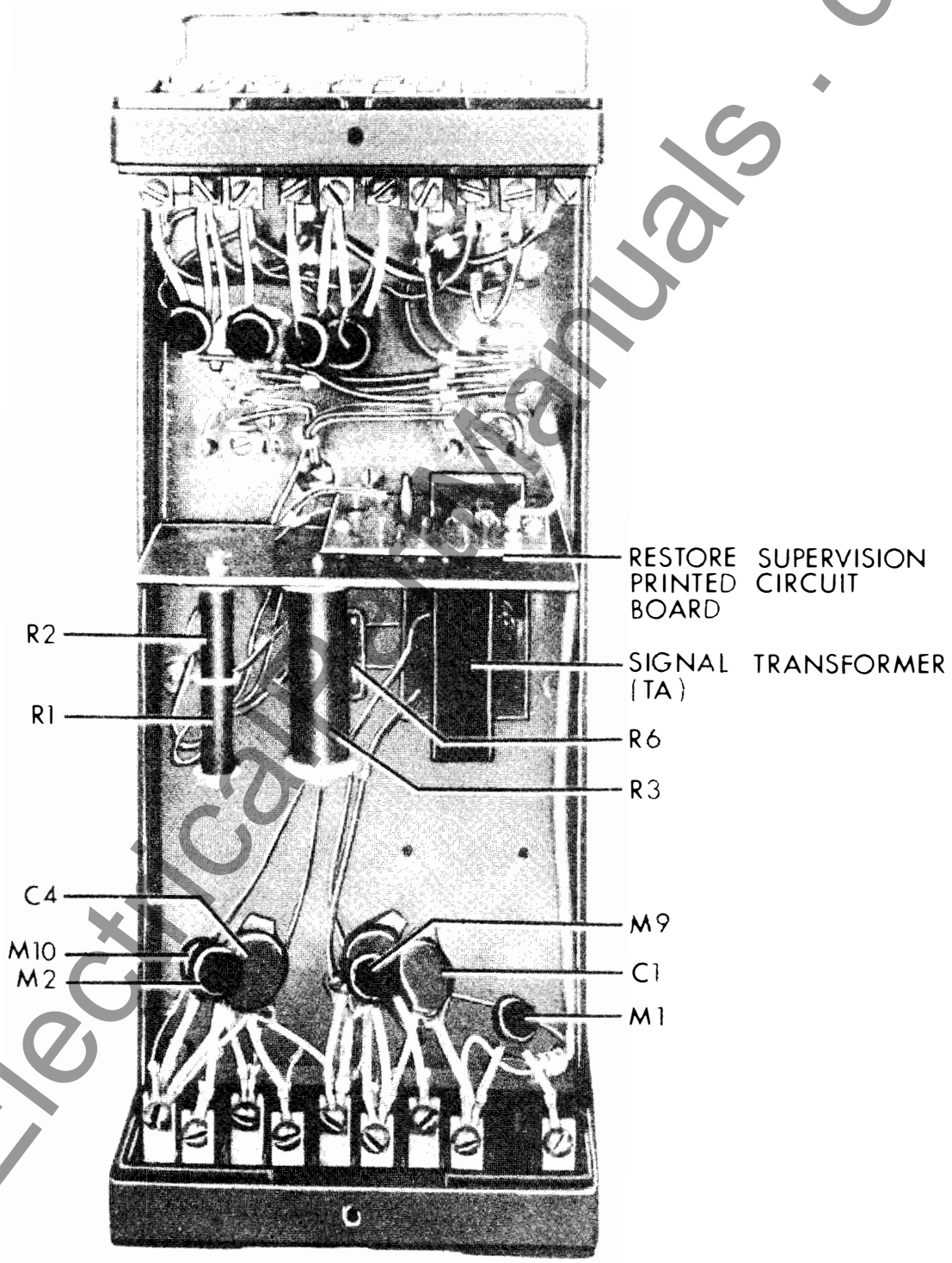


Figure 3 (8043418) SFF32A - Rear View Removed from Case

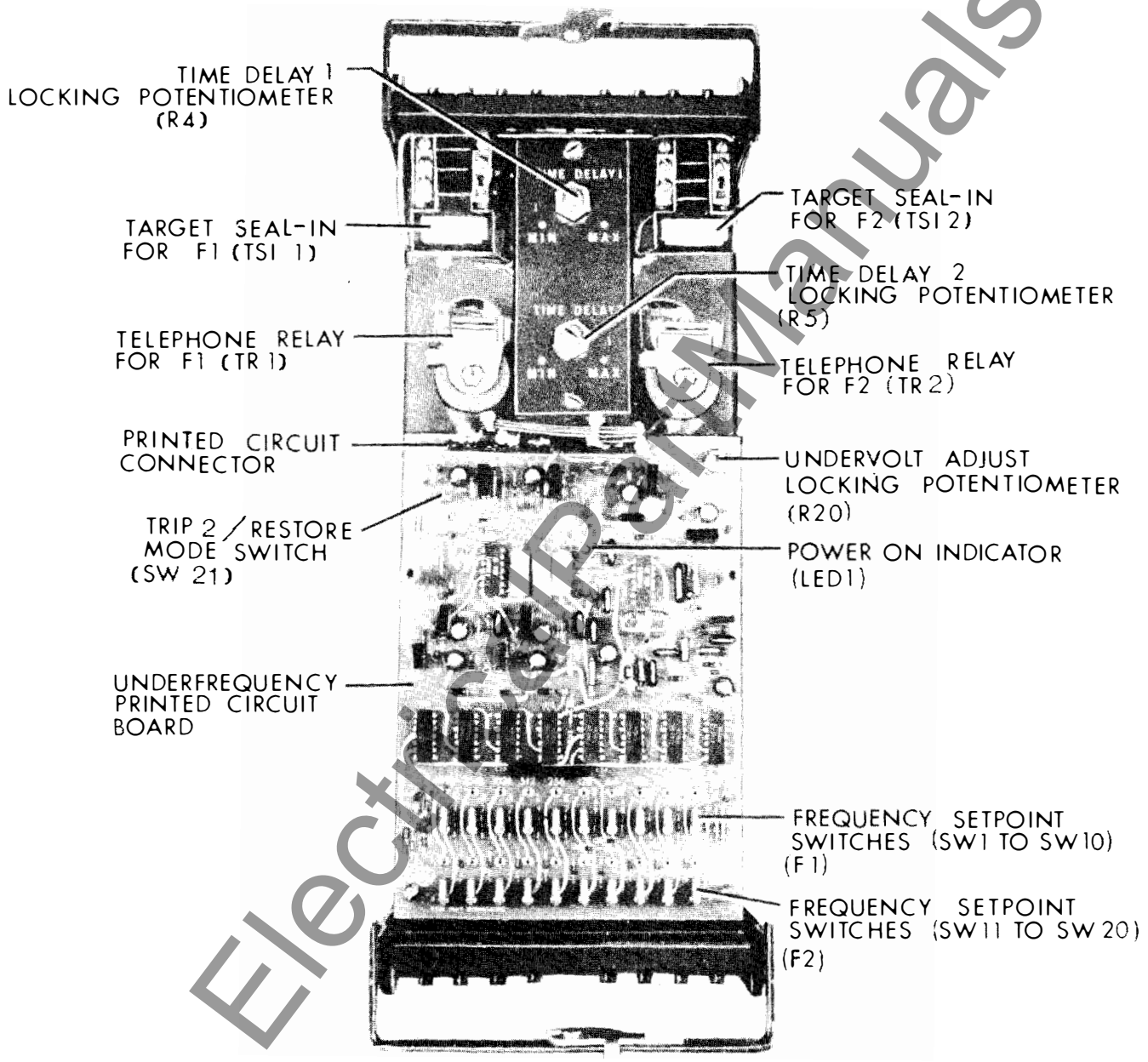


Figure 4 (8043402) SFF32C - Front View Removed from Case

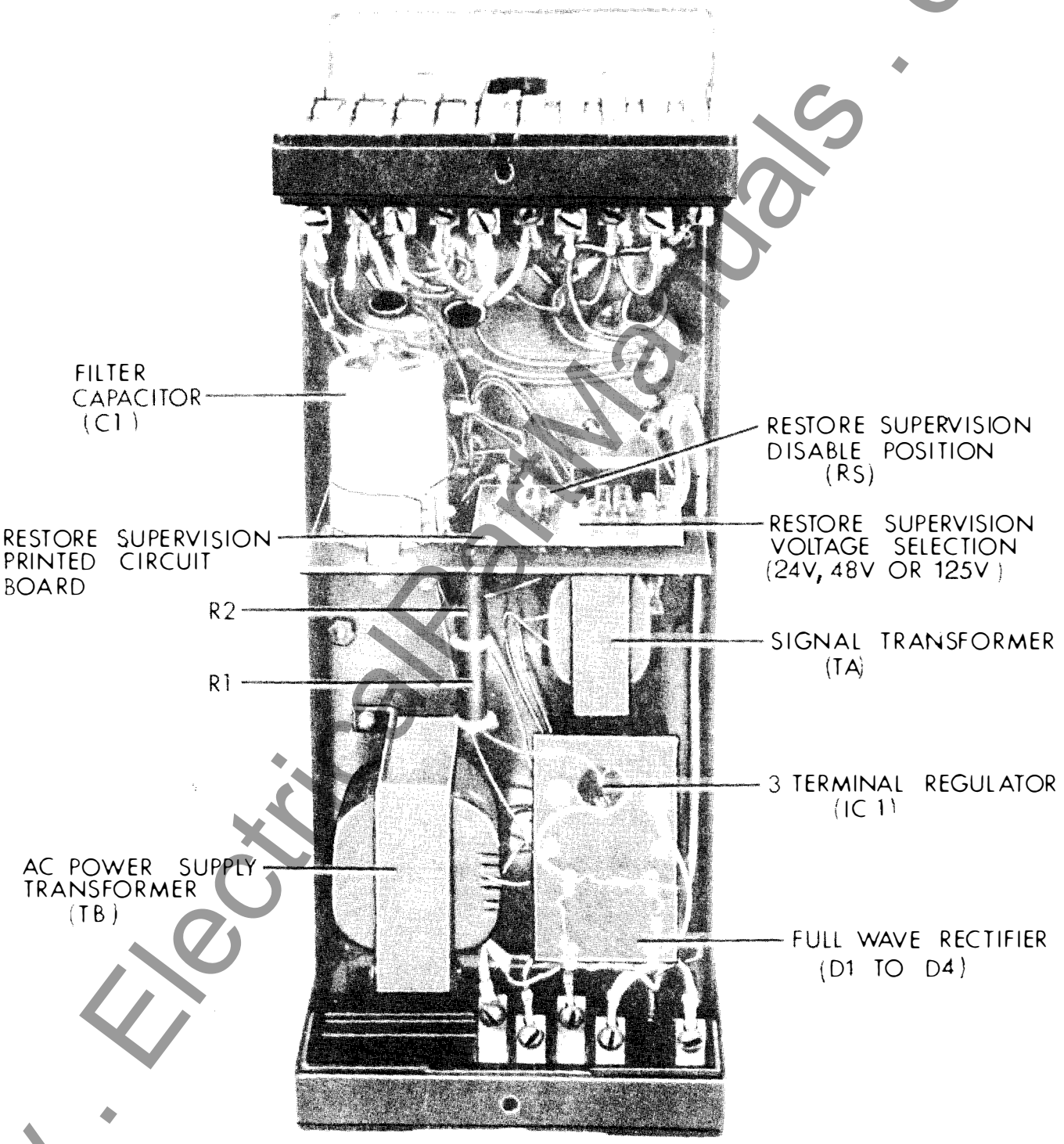
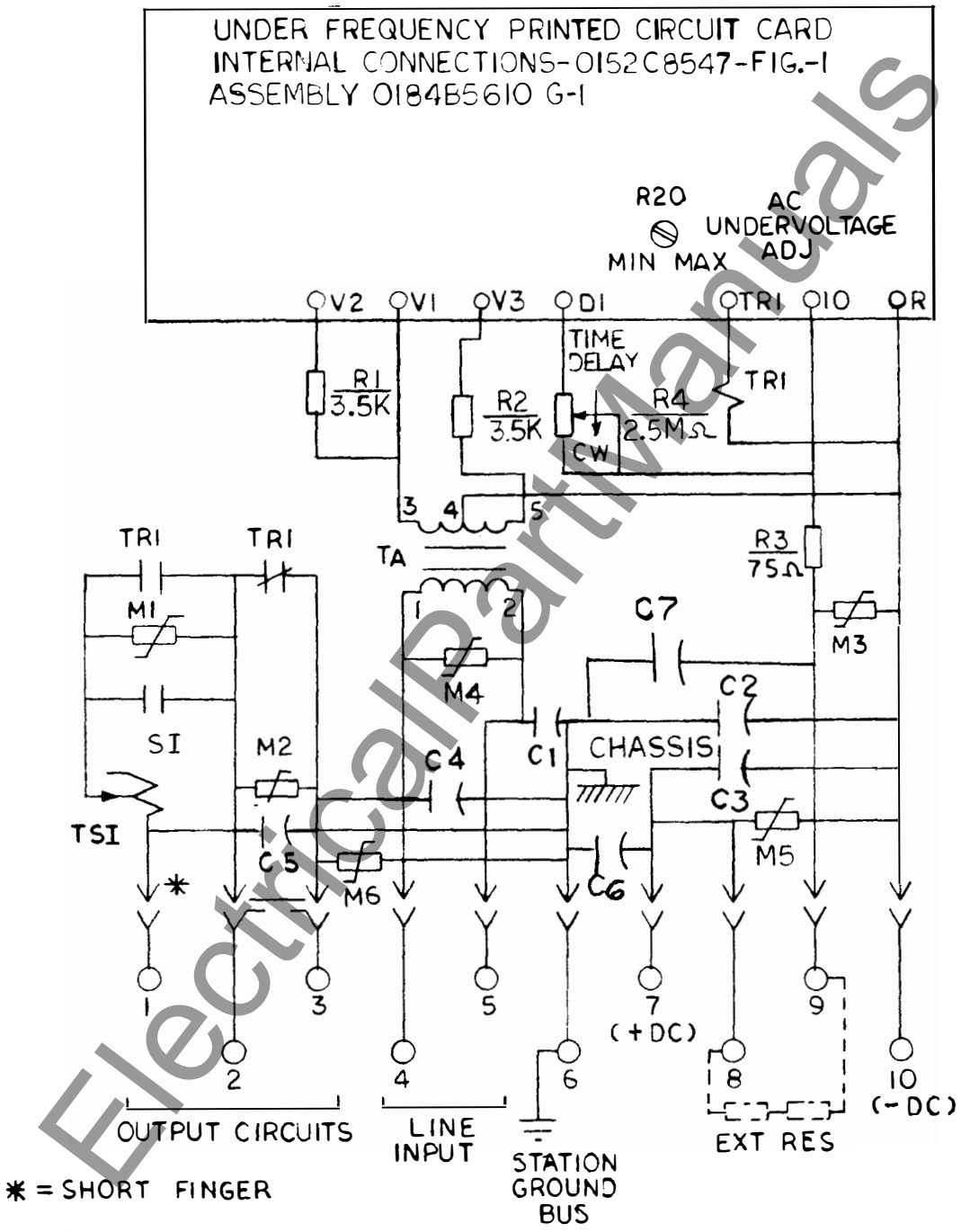


Figure 5 (8043403) SFF32C - Rear View Removed from Case



* Figure 6 (0273A9084-2) SFF31A Internal Connections - Front View

*Revised since last issue

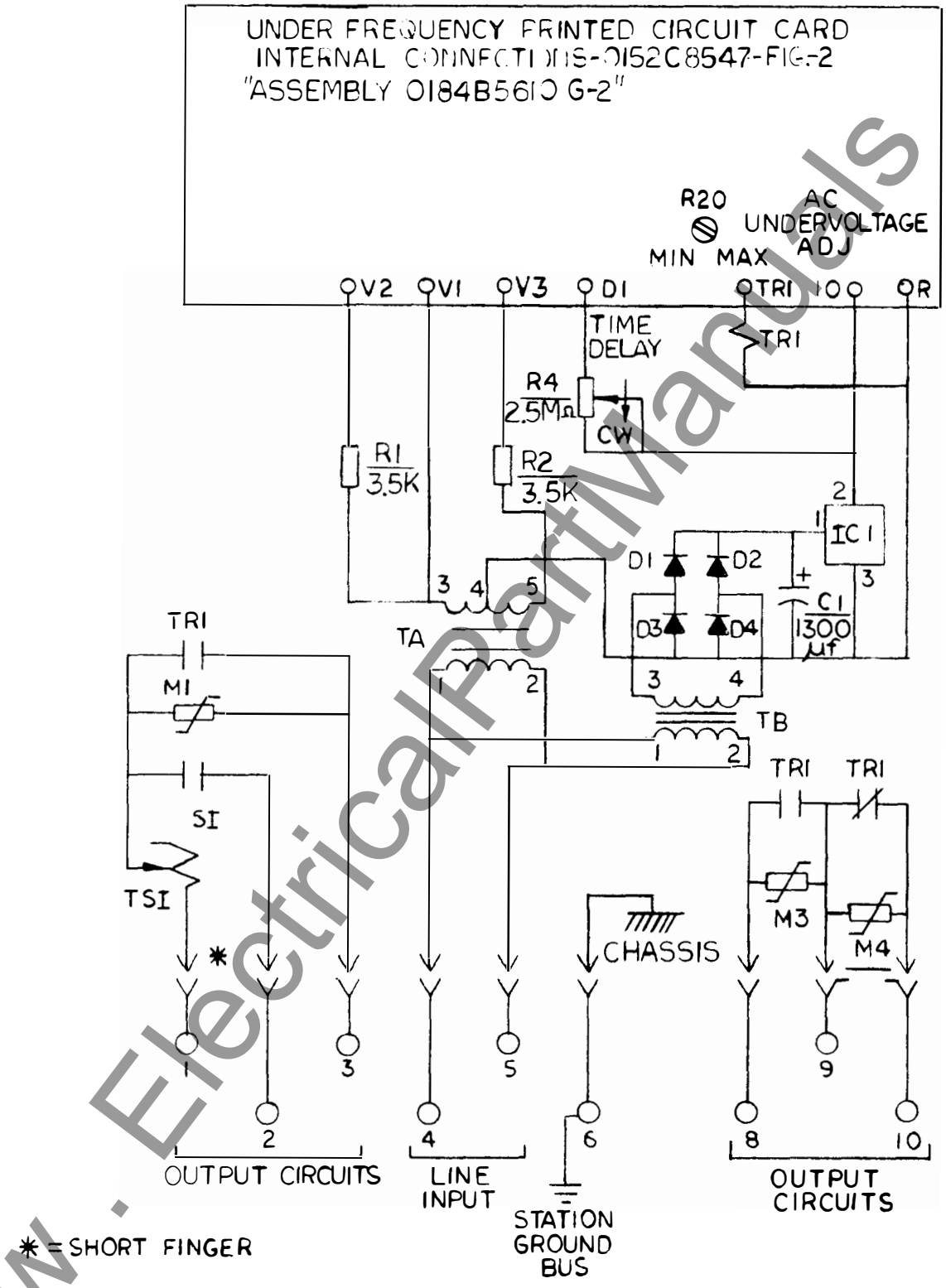


Figure 7 (0273A9085-1) SFF31C Internal Connections - Front View

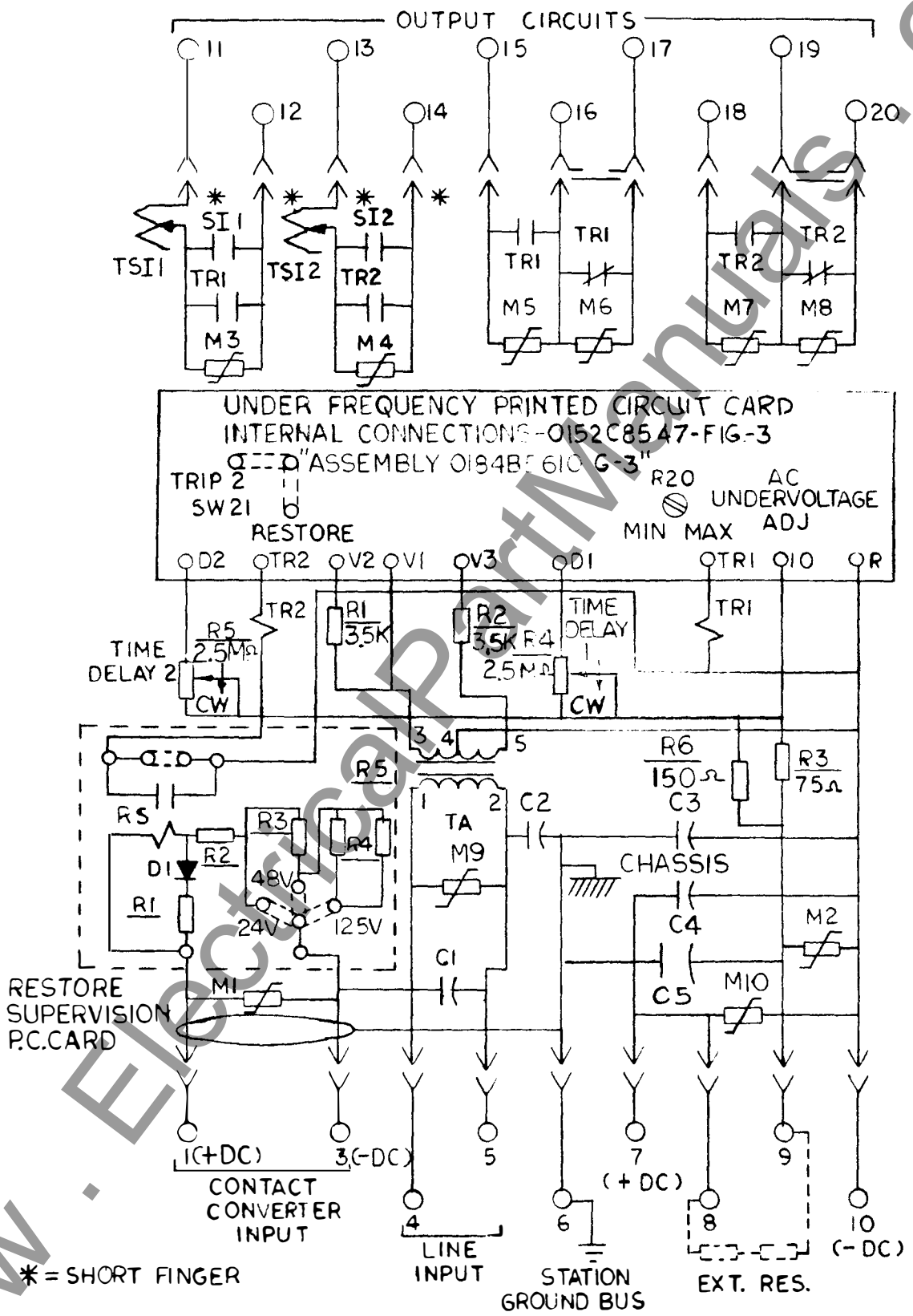


*Figure 8 (0273A9086-4) SFF32A Internal Connections - Front View

*Revised since last issue

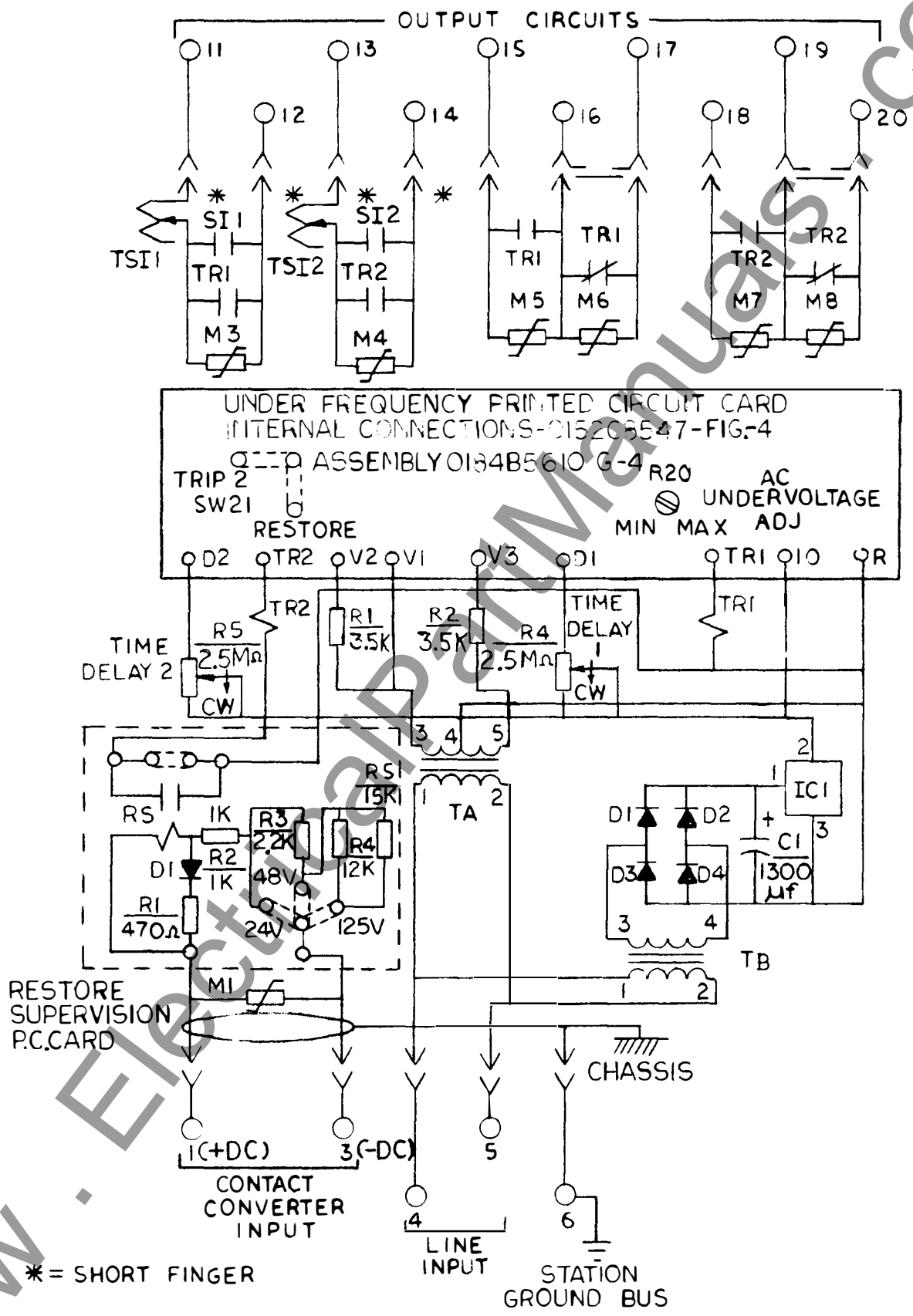


Figure 9 (0273A9087-1) SFF32C Internal Connections - Front View

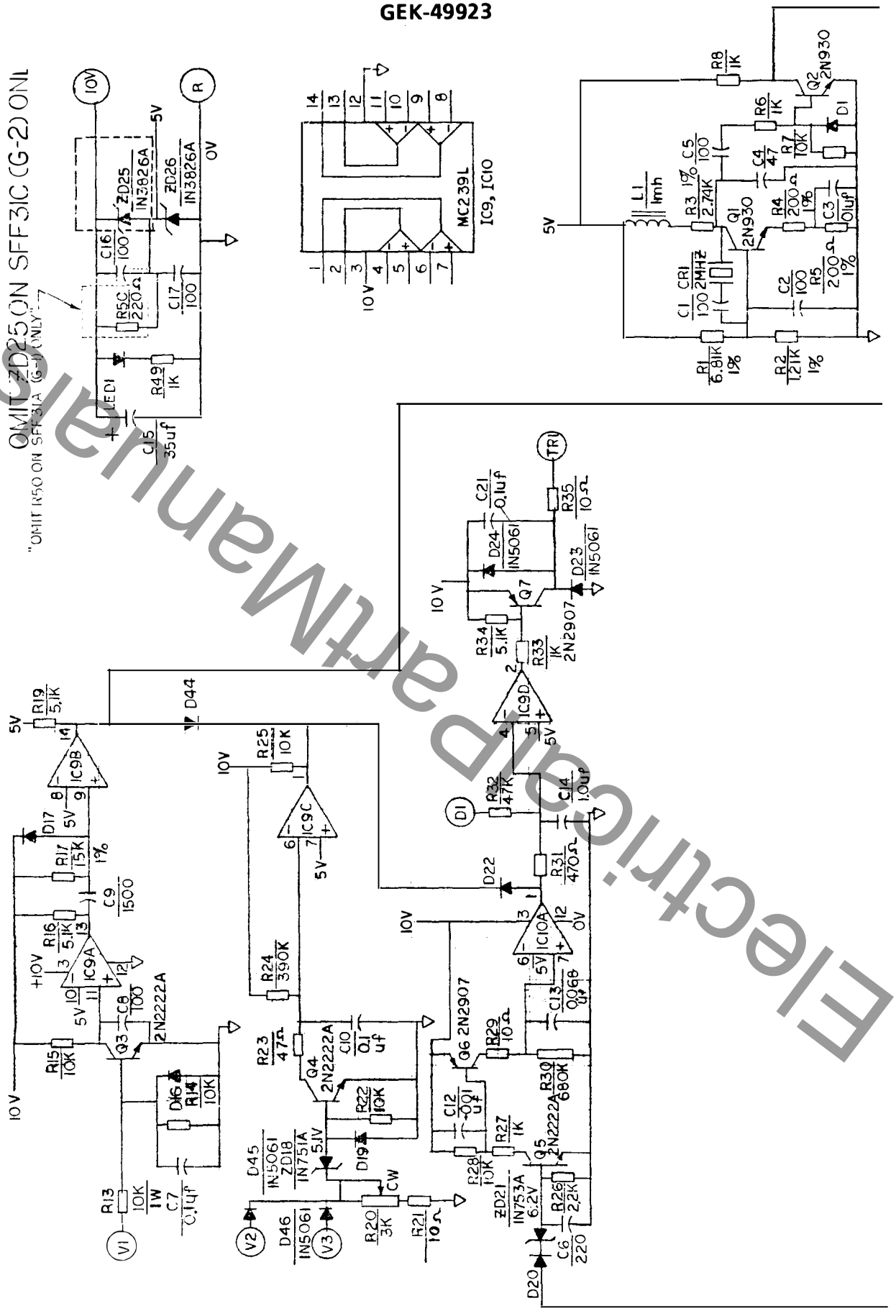


Figure 10A (0152C8547 Sh.1[2]) SFF31 Underfrequency Board Internal Connections

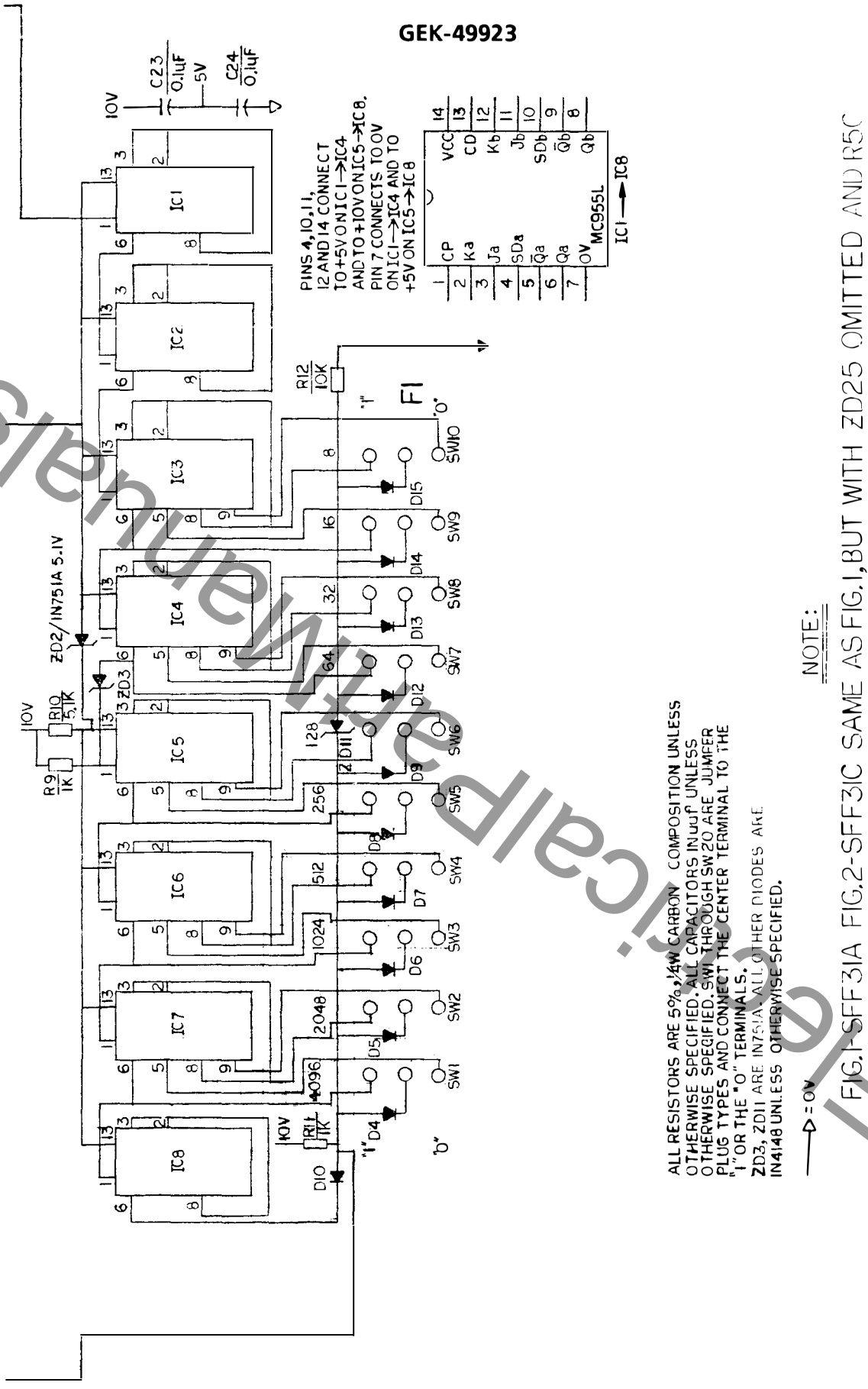


*Figure 10B (0152C8547 Sh.1[2]) SFF31 Underfrequency Board Internal Connections, continued

*Revised since last issue

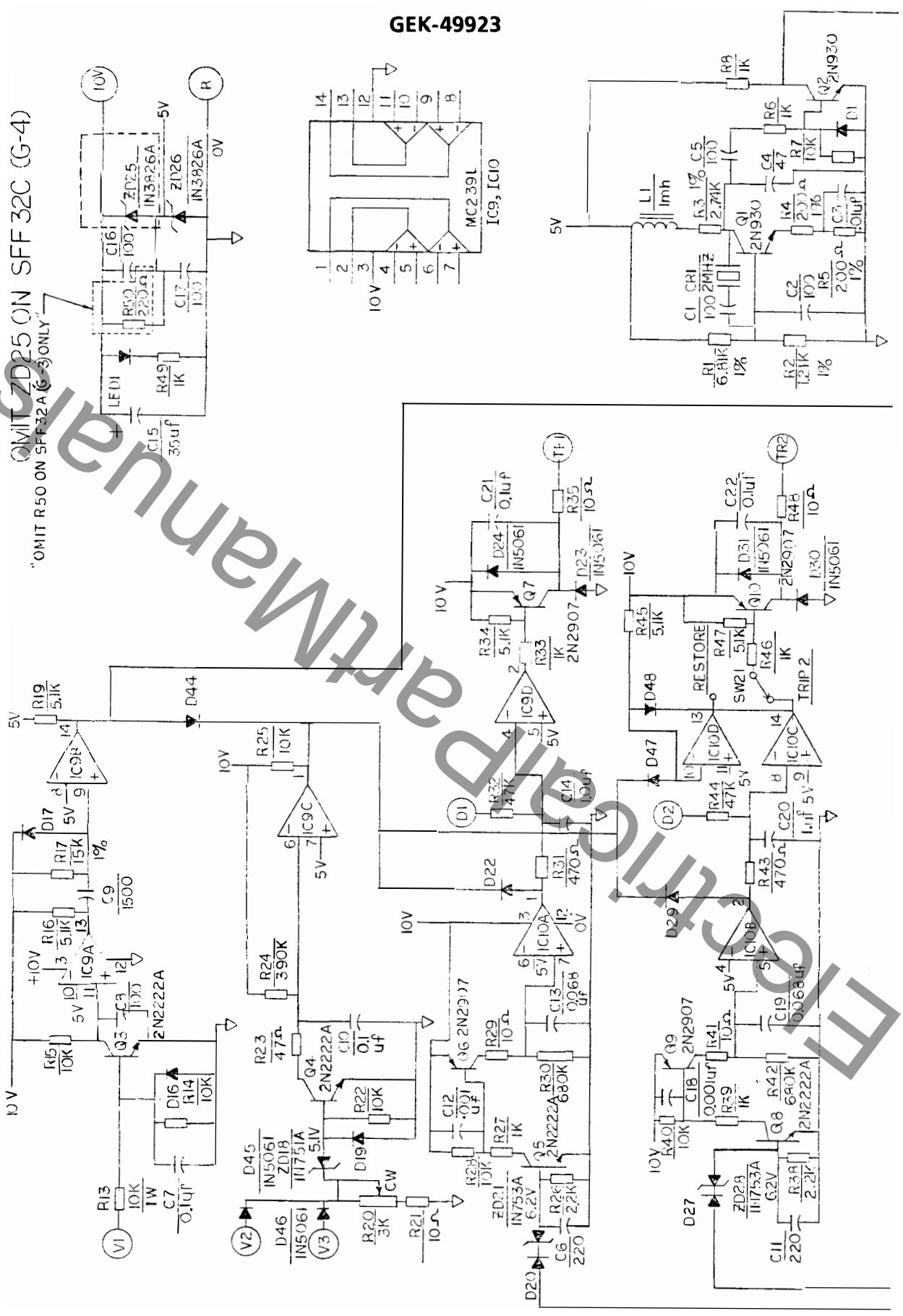


*Figure 10C (0152C8547 Sh.2[2]) SFF32 Underfrequency Board internal connections

*Revised since last issue

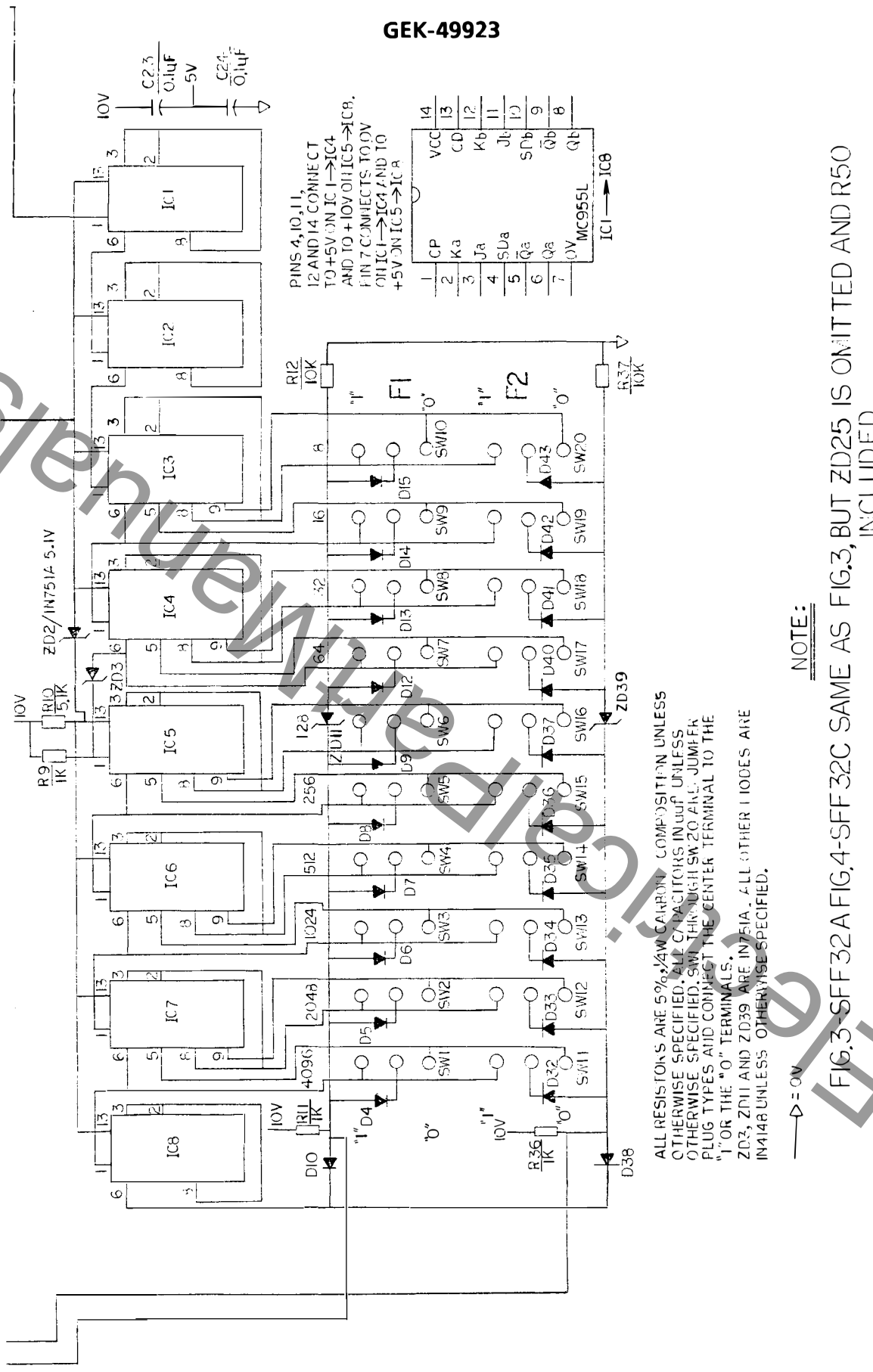


*Figure 10D (0152C8547 Sh.2[2]) SFF32 Underfrequency Board Internal Connections, continued

*Revised since last issue

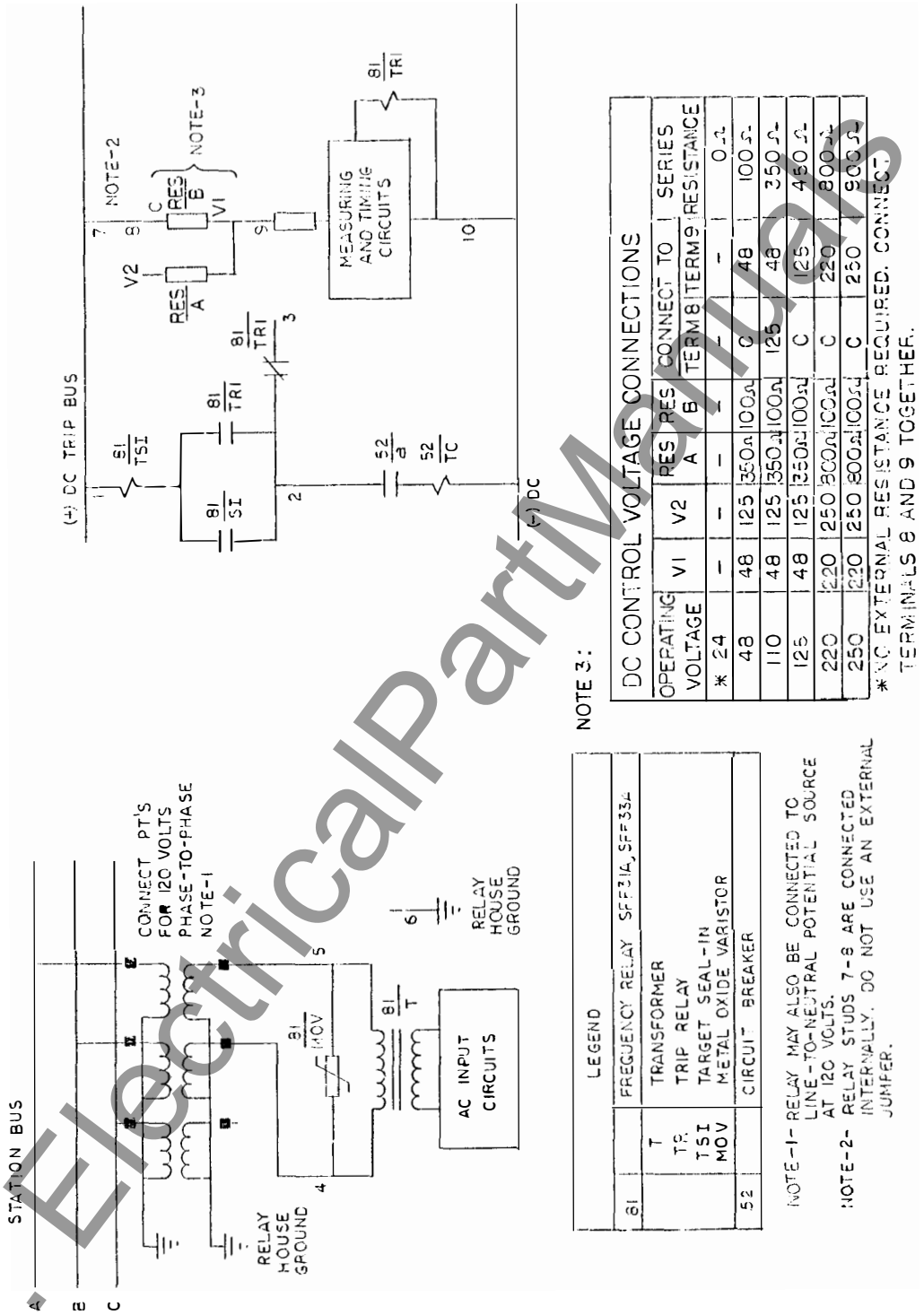


*Figure 11 (0108B9171-4) SFF31A External Connections

*Revised since last issue

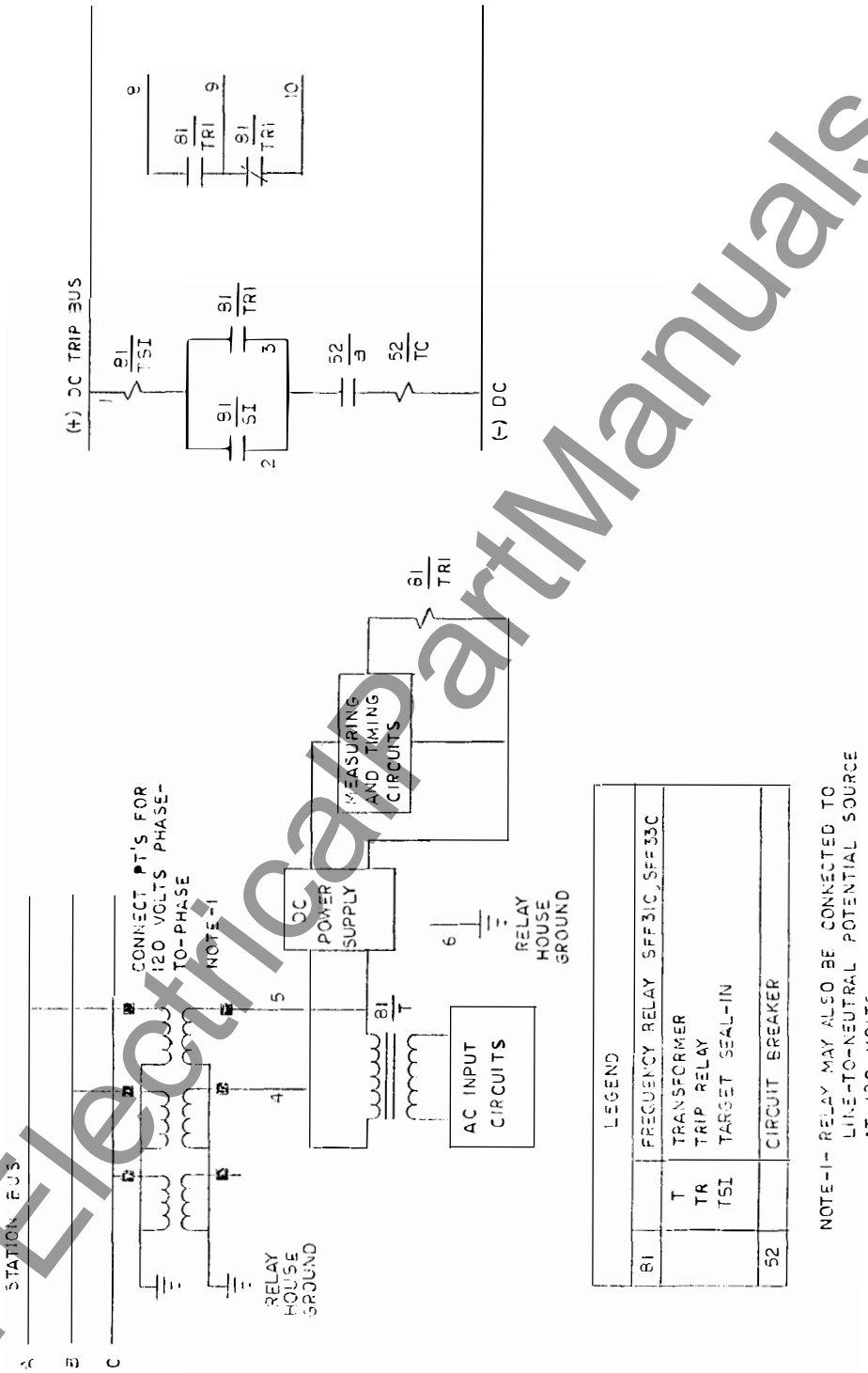


*Figure 12 (0108B9172-1) SFF31C External Connections

*Revised since last issue

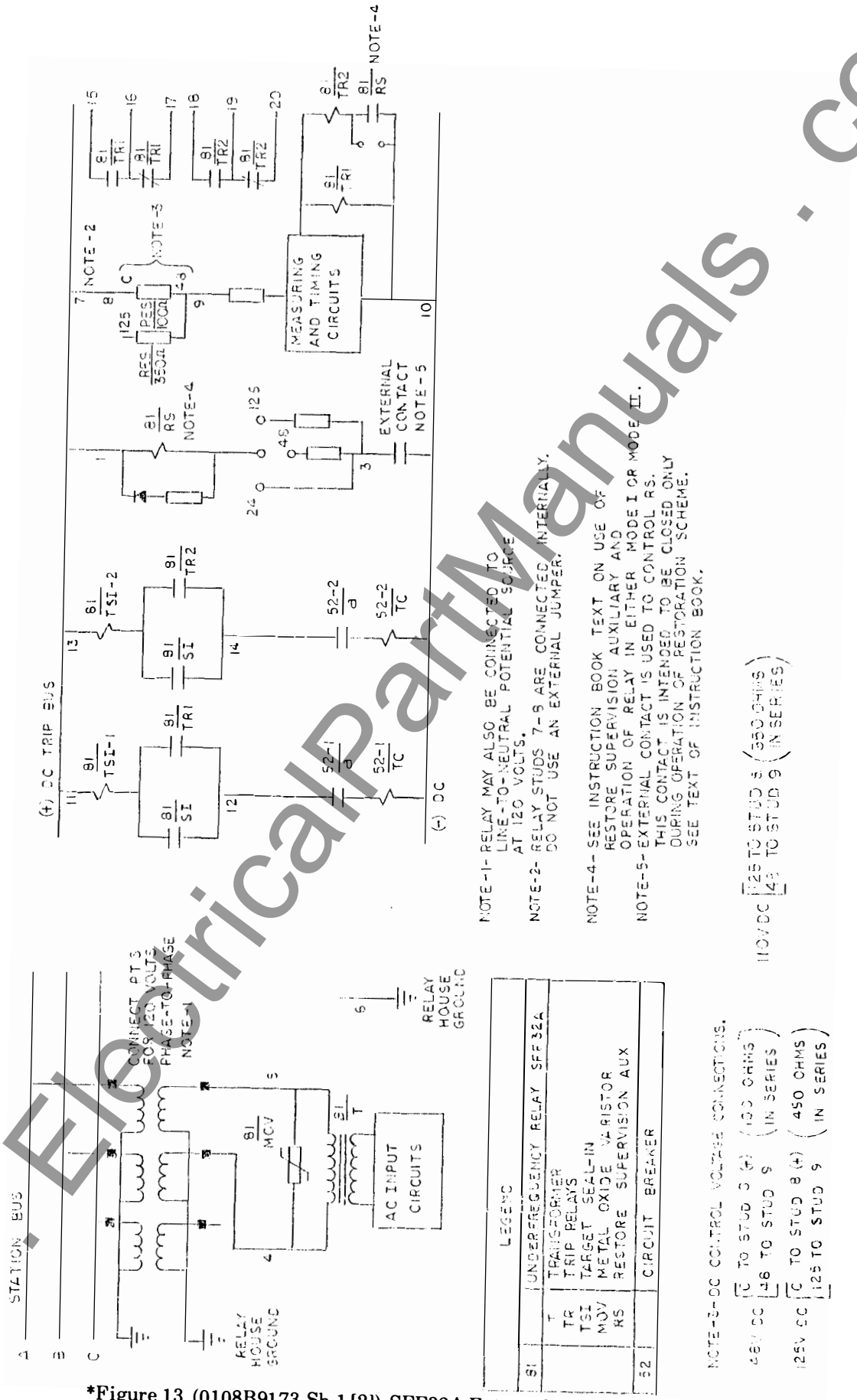


*Figure 13 (0108B9173-Sh.1 [2]) SFF32A External Connections

*Revised since last issue

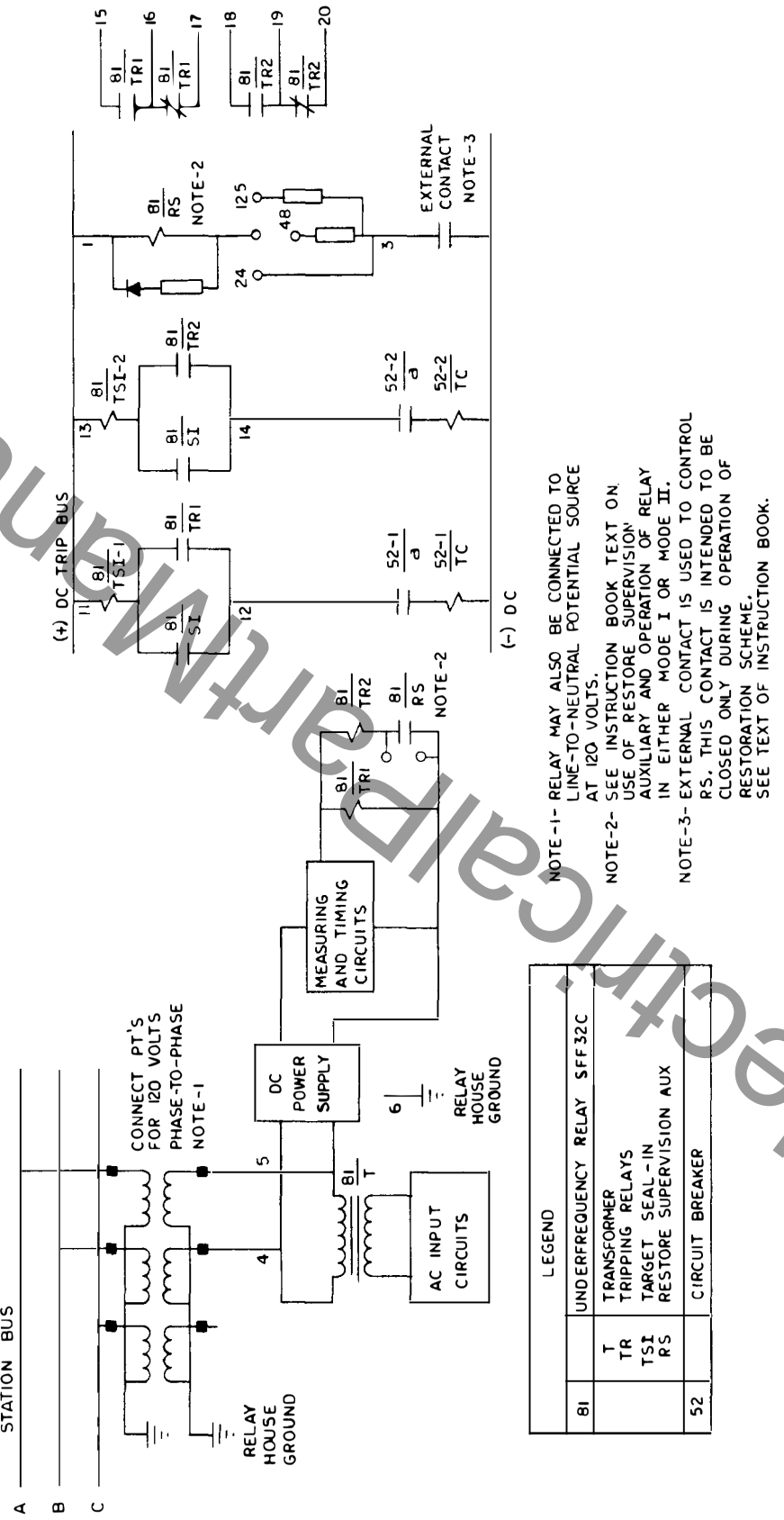


Figure 14 (0108B9174) SFF32C External Connections

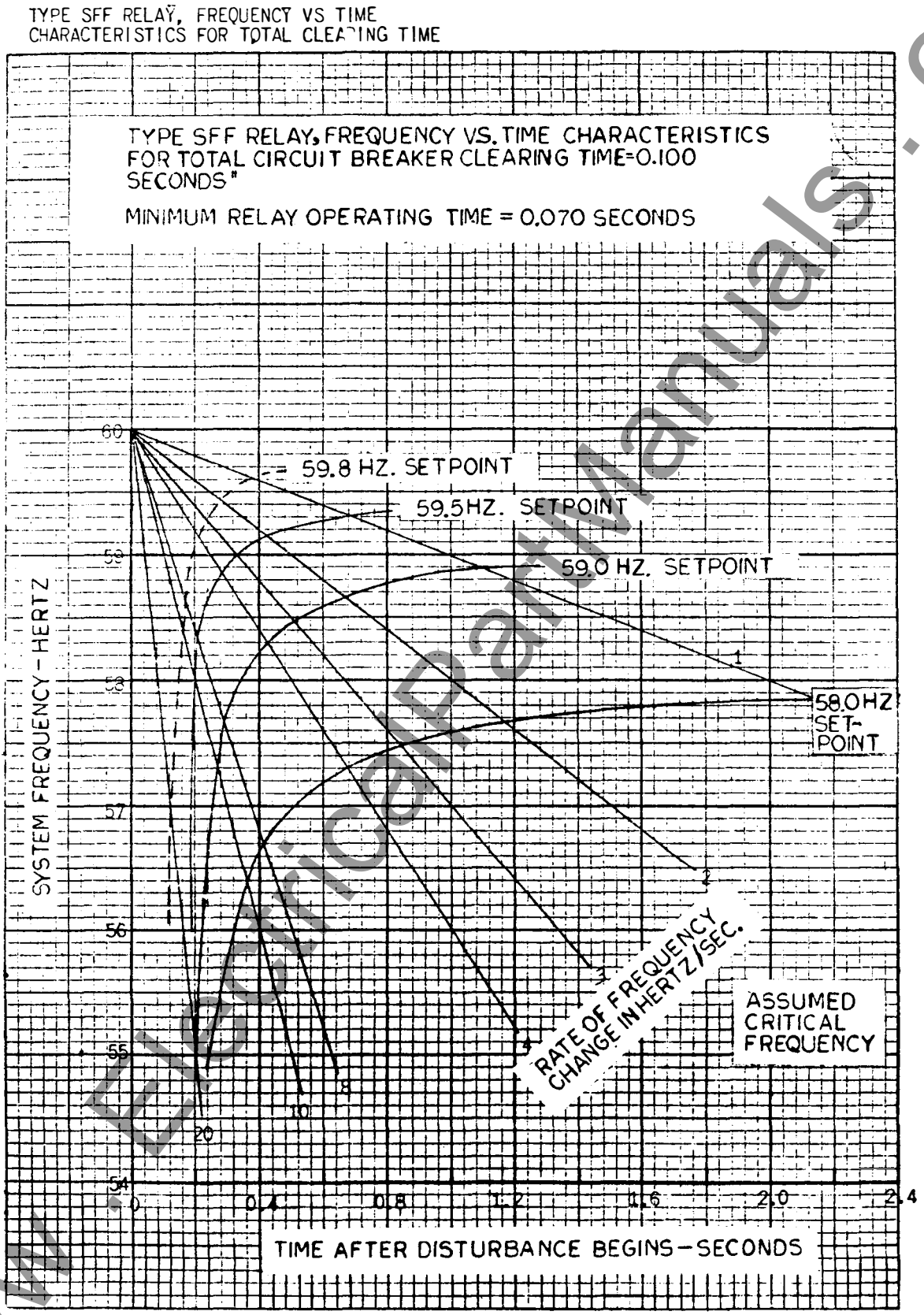


Figure 15 (0208A3902-2) Rate of Frequency Change Versus Frequency Break Point

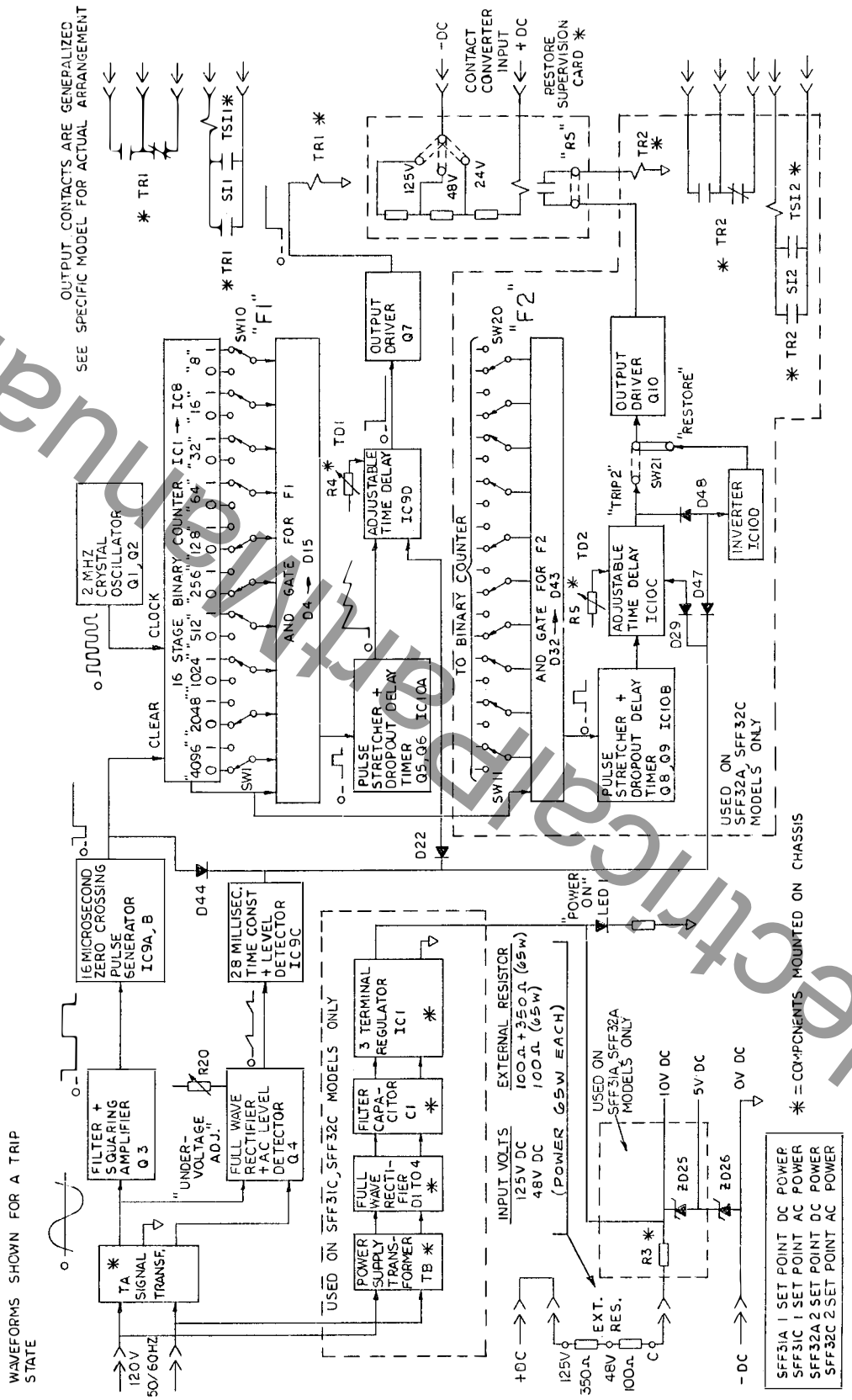


Figure 16 (0108B9170Sh.1 [1]) SFF Block Diagram

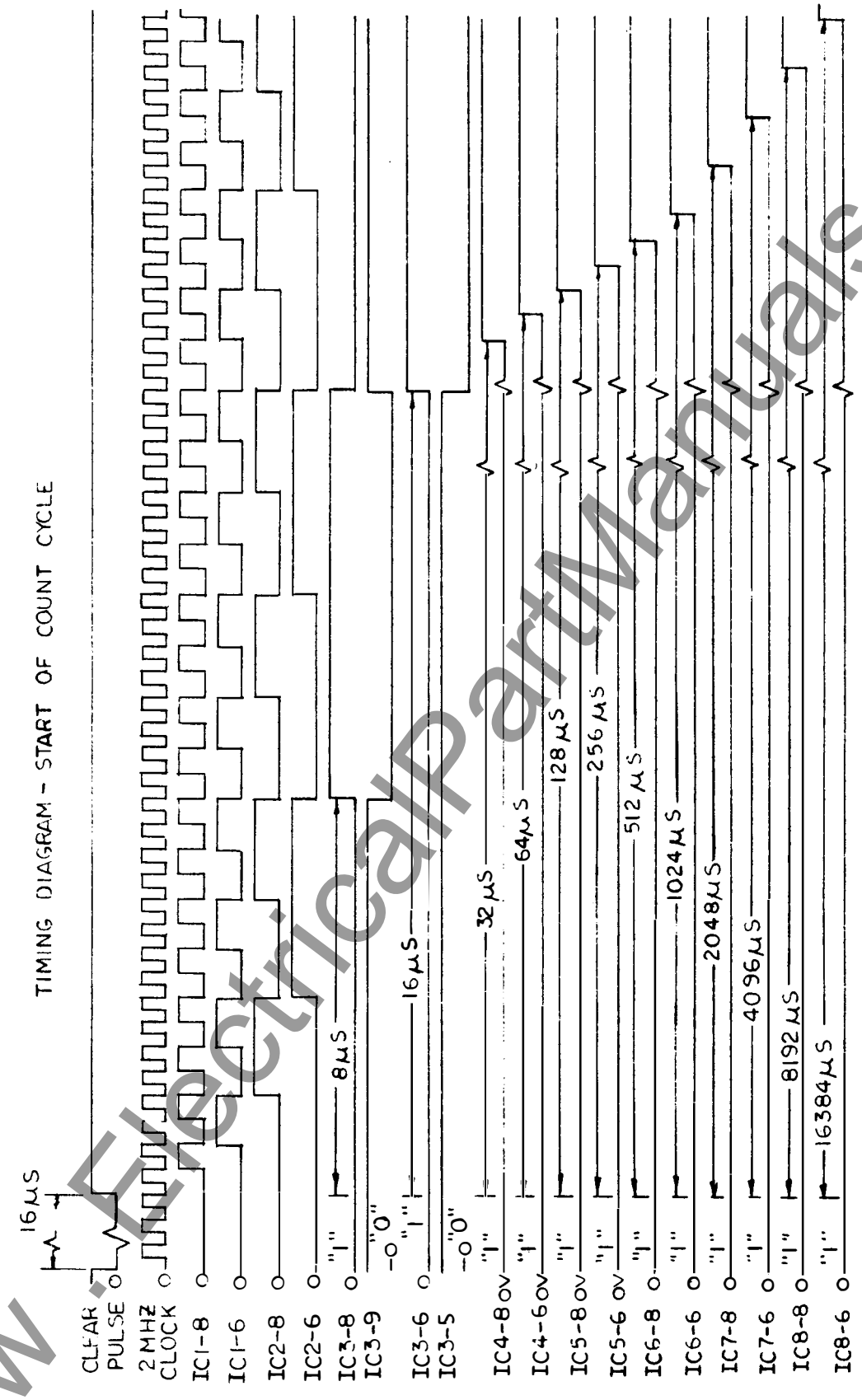


Figure 17 (0273A9562) Timing Diagram - Start of Count Cycle

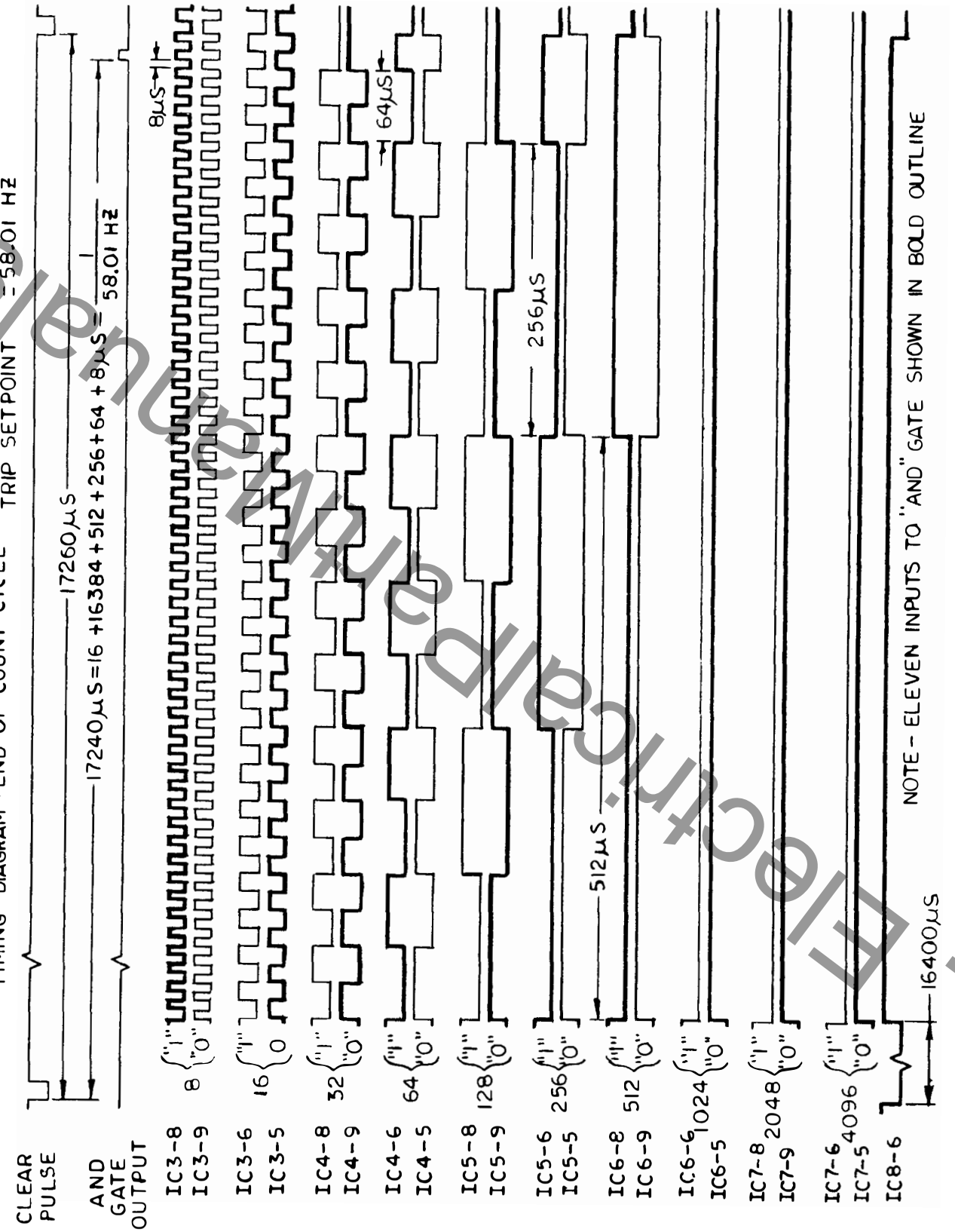
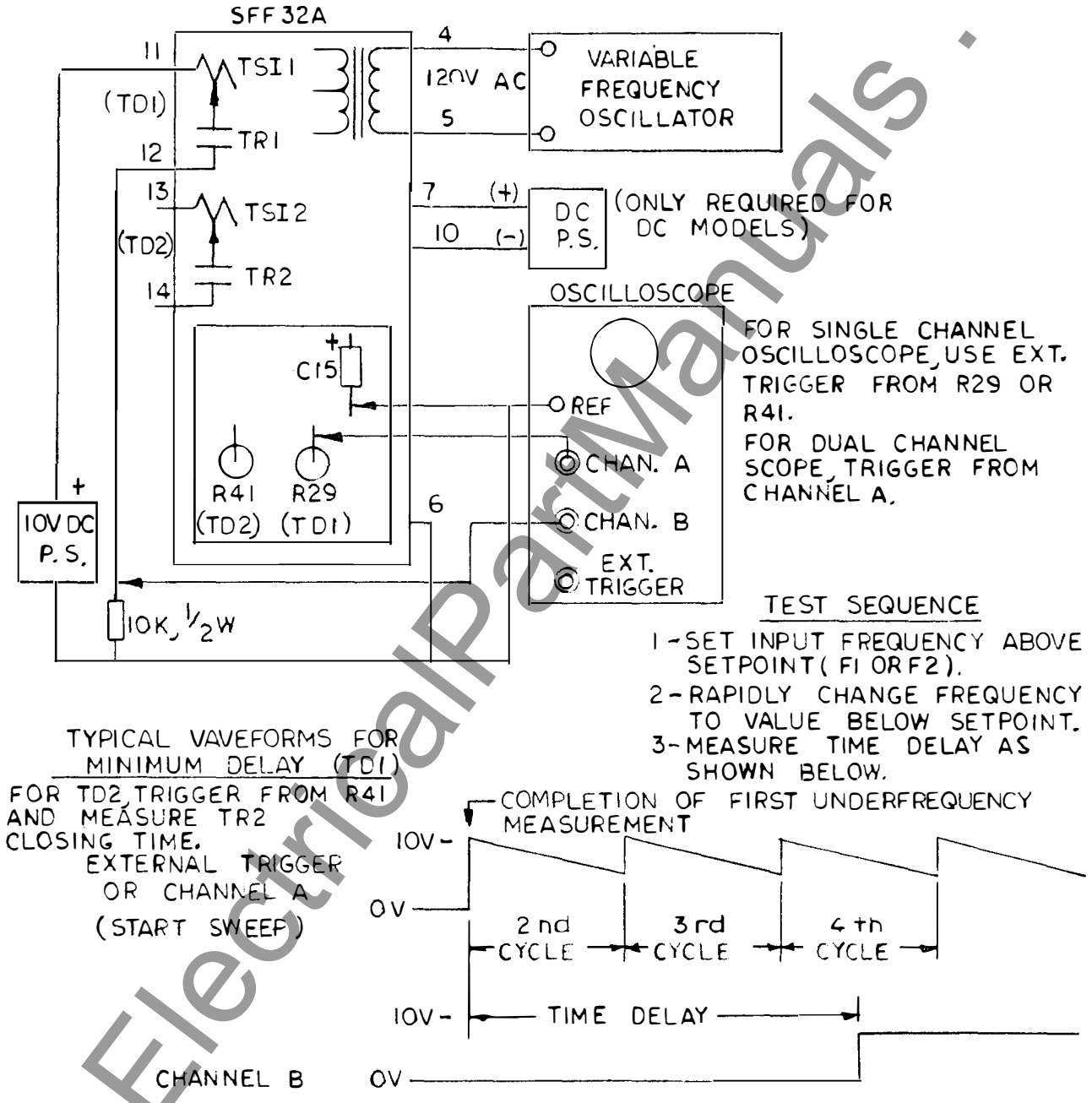


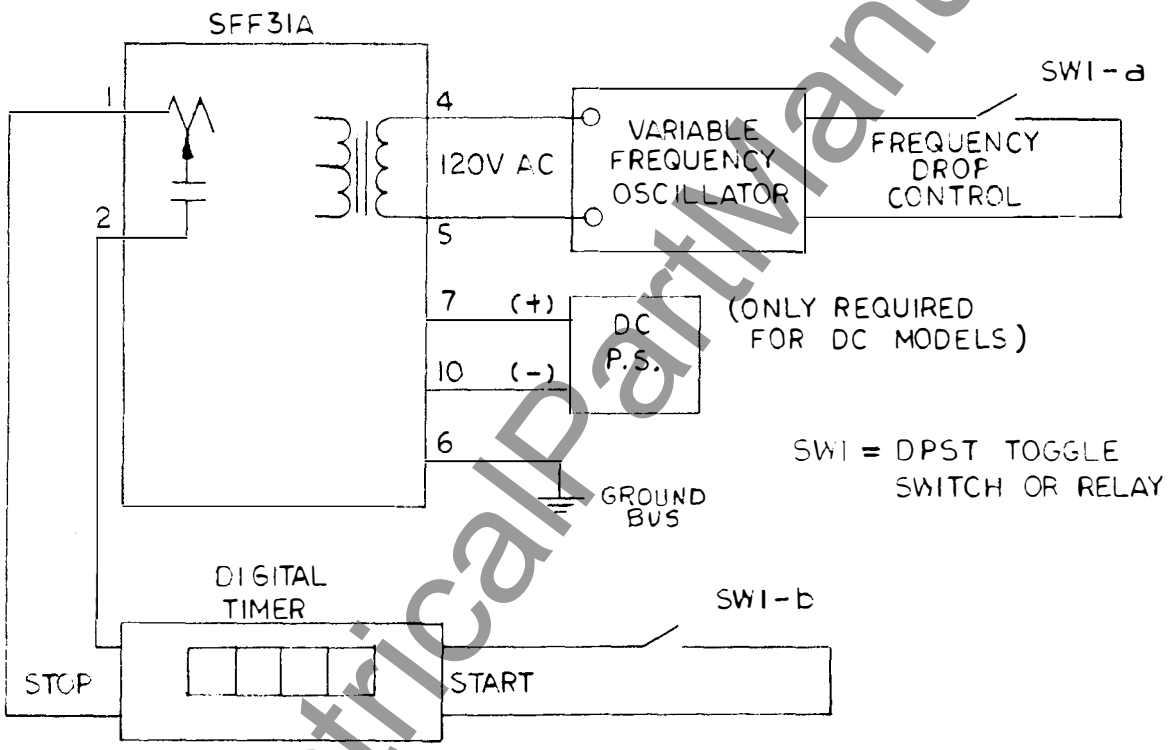
Figure 18 (0273A9563) Timing Diagram - End of Count Cycle



NOTE - ADD SETPOINT PERIOD TO TIME DELAY FOR TOTAL TIME MEASURED FROM START OF FIRST UNDERFREQUENCY CYCLE.

*Figure 19A (0273A9564-Sh.1 [1]) Time-Delay Calibration Test Connections

*Revised since last issue



TEST SEQUENCE

1- SET INPUT FREQUENCY ≈0.10 HZ ABOVE SETPOINT (SW1 OPEN).
2- CLOSE SW1 CAUSING VARIABLE FREQUENCY OSCILLATOR TO DROP FREQUENCY BELOW SETPOINT.
3- MEASURE TIME DELAY RECORDED ON DIGITAL TIMER.

*Figure 19B (0273A9580-1) Typical Time-Delay Periodic Test

*Revised since last issue

Figure 20 (8025039) Drawout Case - Contact Assembly

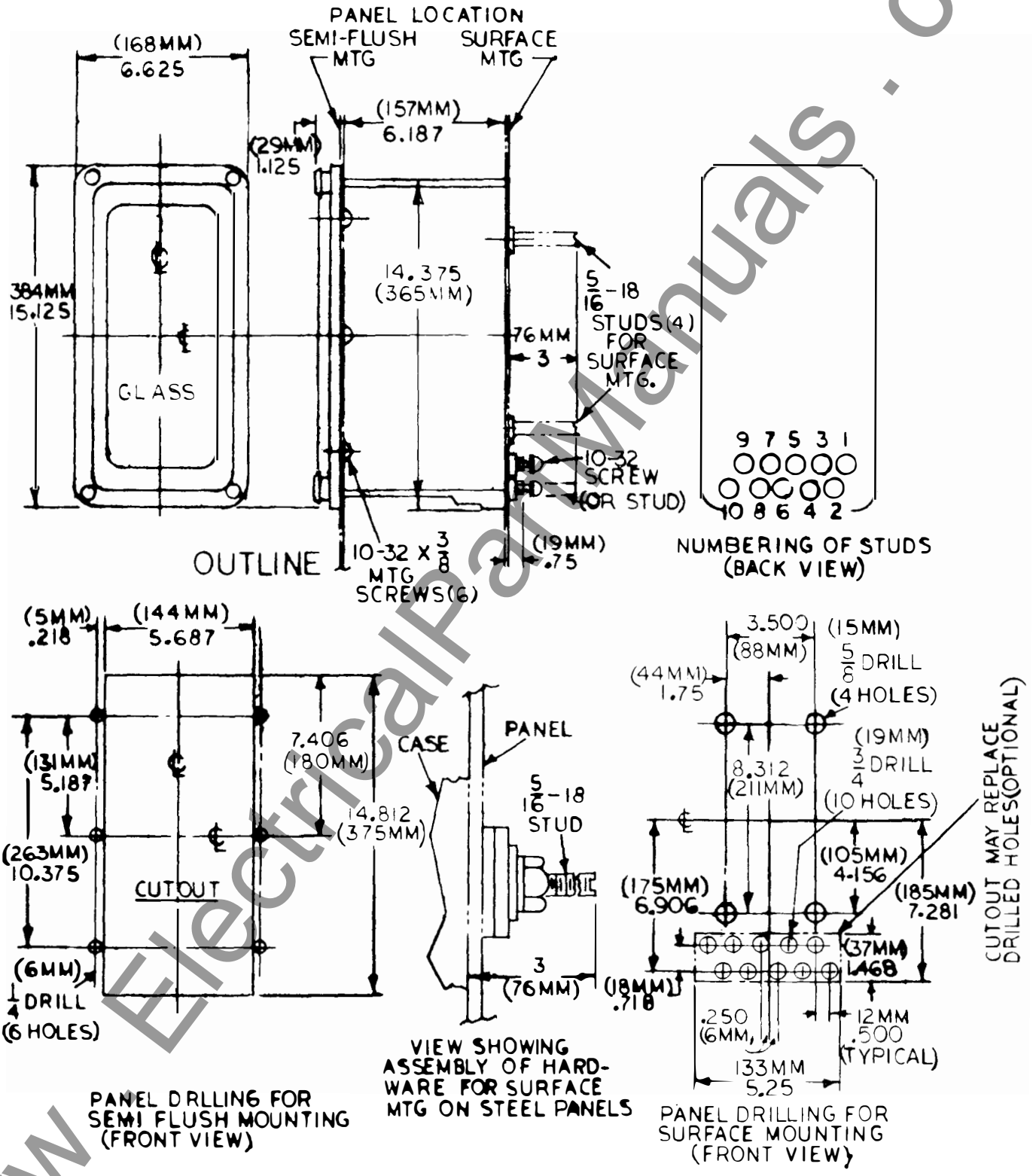


Figure 21 (K-6209273-4) Outline and Panel Drilling - M1 Case

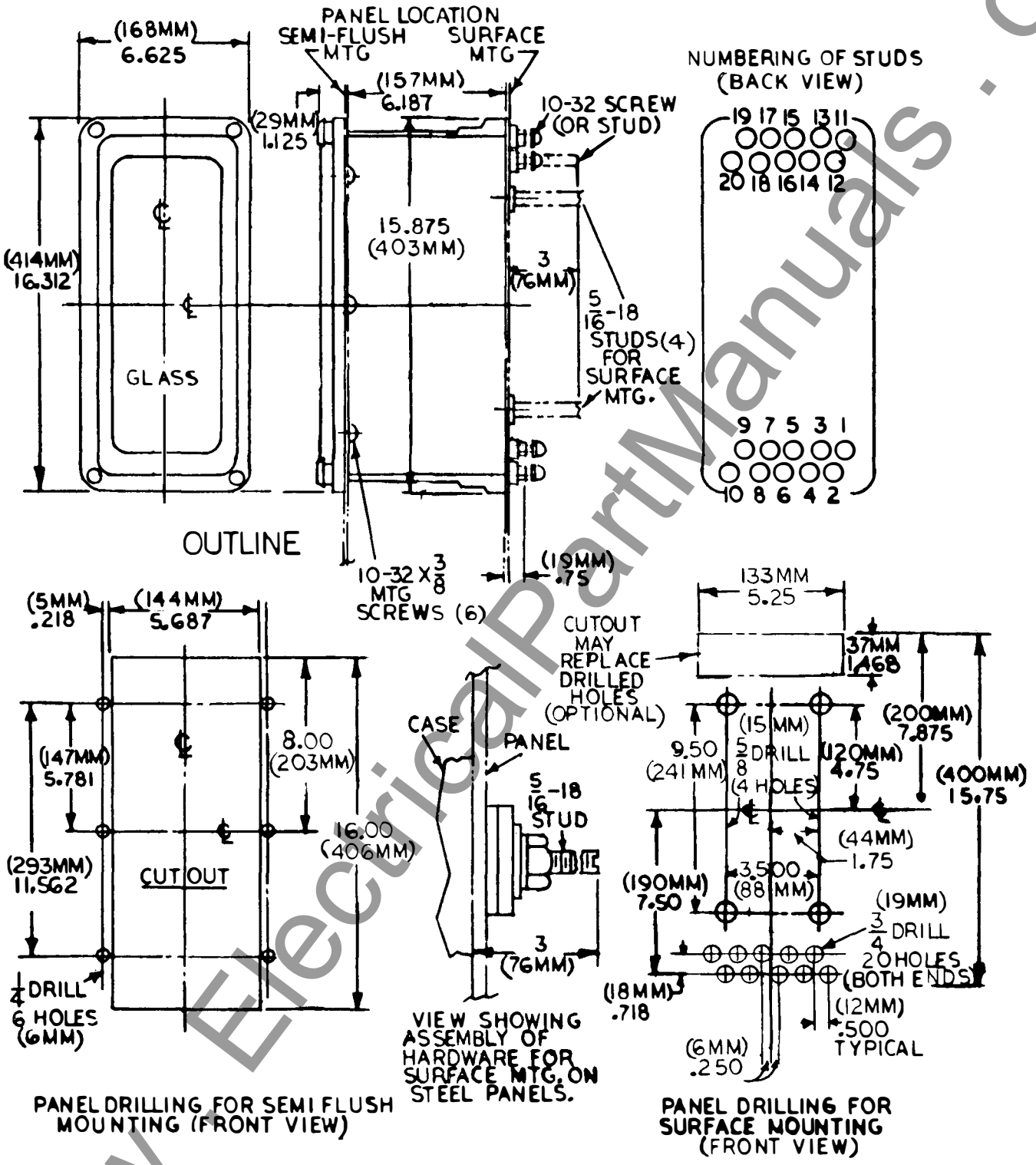


Figure 22 (K-6029274-4) Outline and Panel Drilling - M2 Case

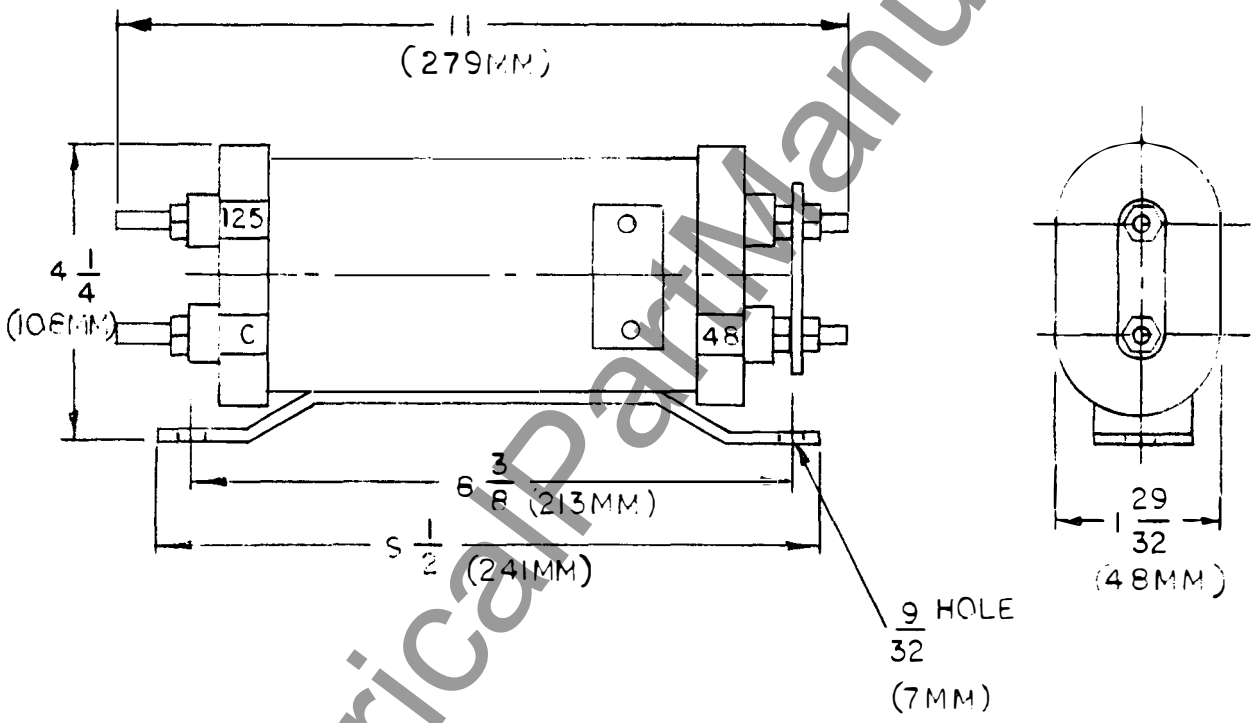


Figure 23A (0273A9565 Sh.1[1]) Outline for External Resistor, 48-125 VDC

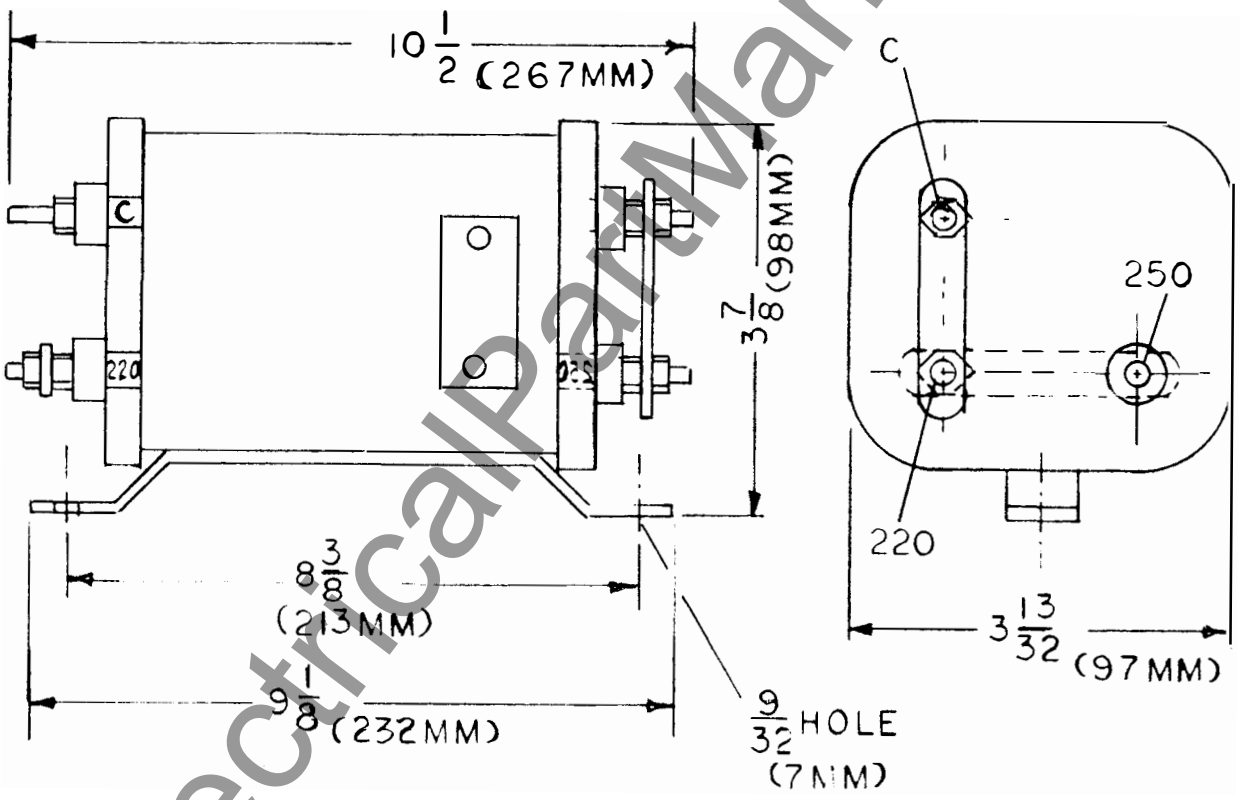


*Figure 23B (0273A9565 Sh.4) Outline for External Resistor, 220-250 VDC

*Revised since last issue

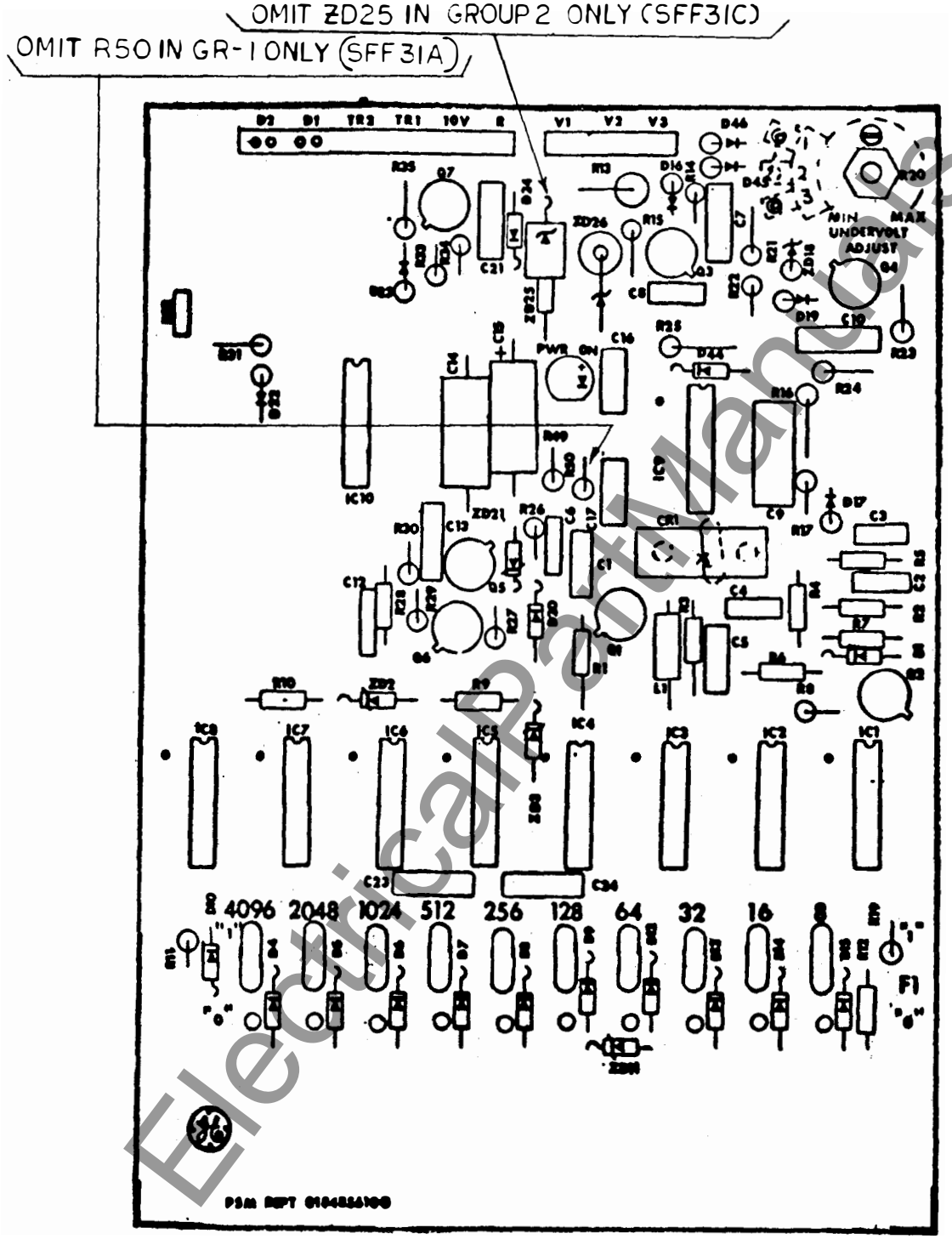


*Figure 24 (0273A9590 Sh.1 [1]) SFF31 Underfrequency Board Assembly

*Revised since last issue

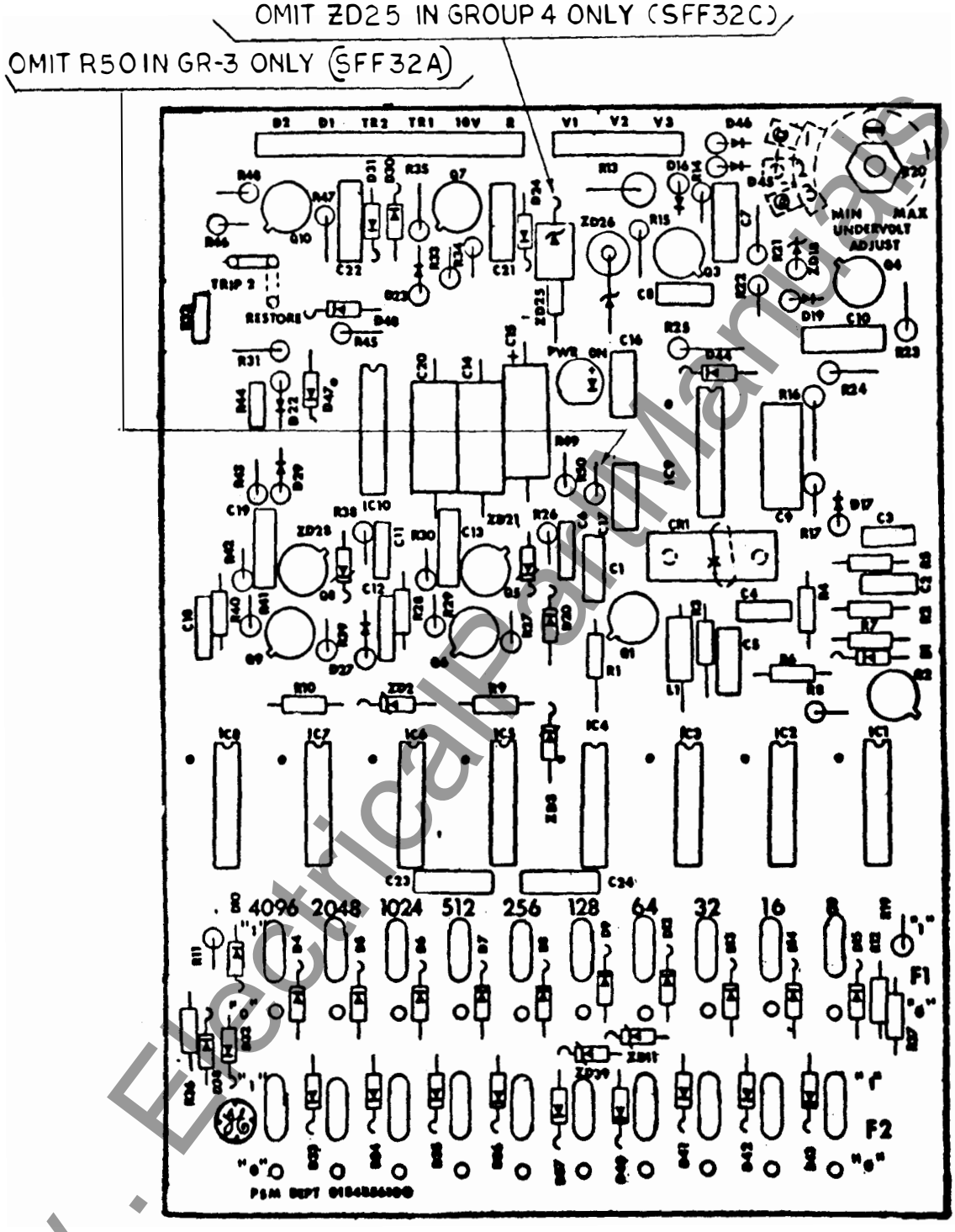


*Figure 25 (0273A9590 Sh.2) SFF32 Underfrequency Board Assembly

*Revised since last issue

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