STATIC BREAKER BACK-UP RELAY

TYPE SBC53A
SBC53B
SBC53C

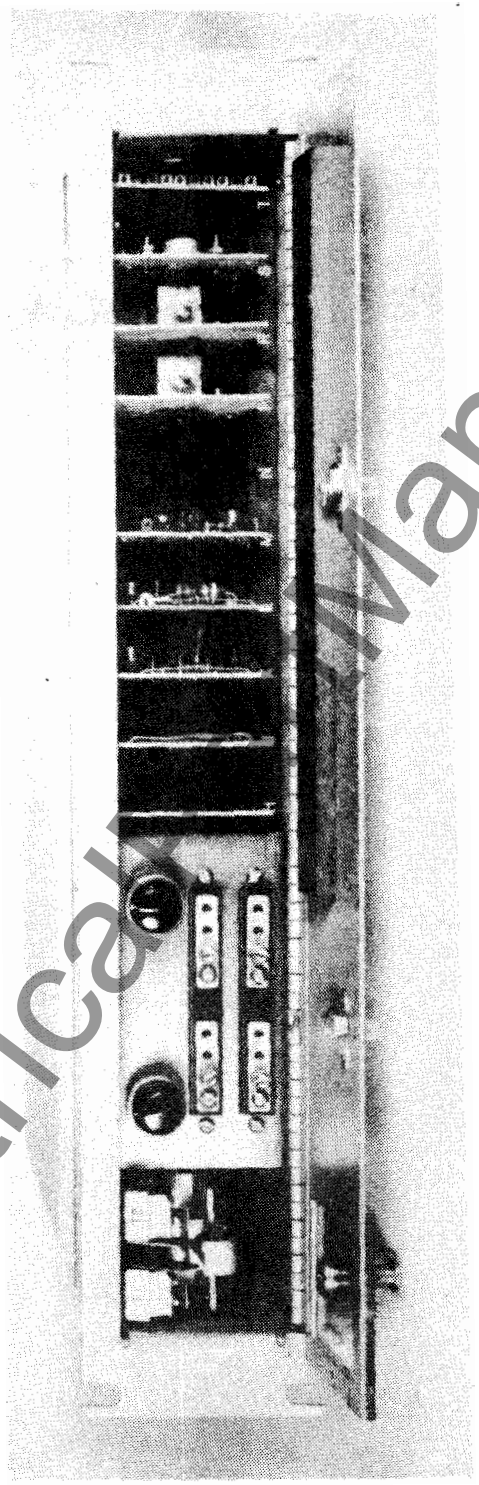

Fig. 1 (8043372) Type SBC53C Relay, Front Cover Removed (Front View)

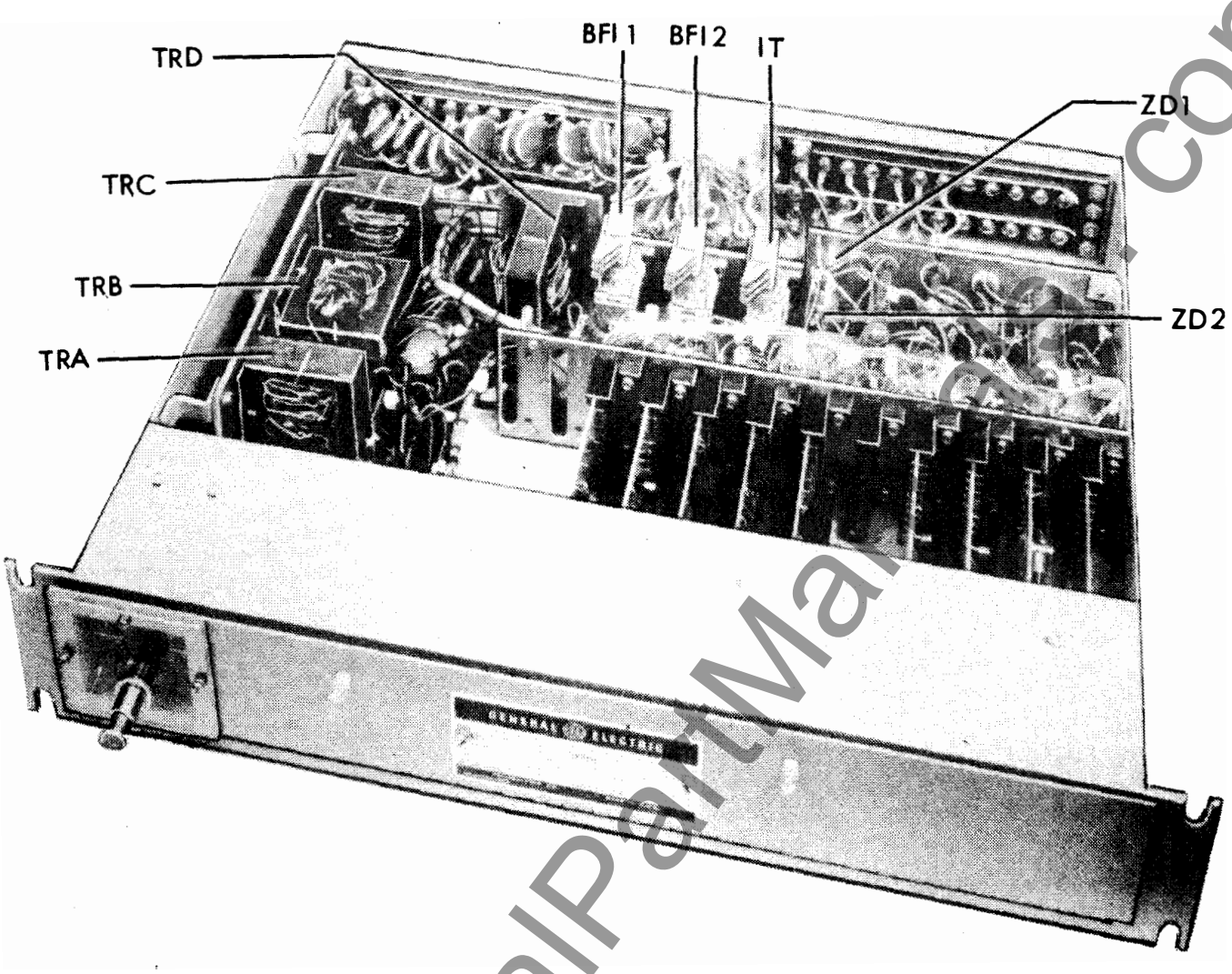

Fig. 2 (8043373) Type SBC53C Relay, Top Cover Plate Removed (Elevated Three-quarter View)

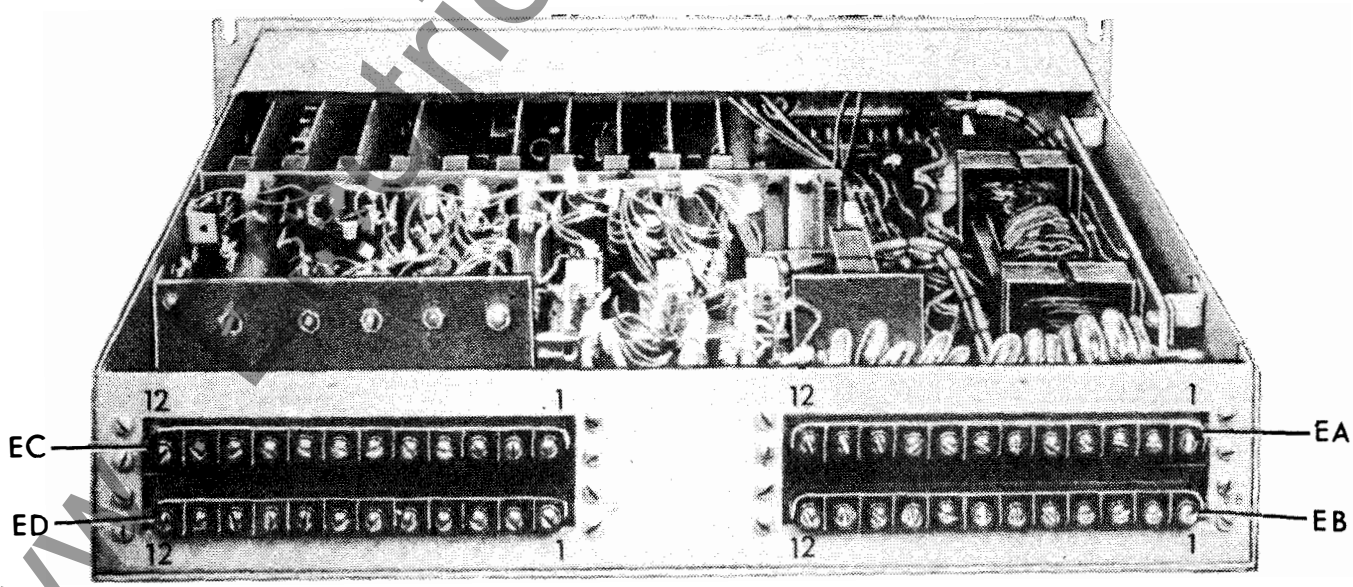

Fig. 3 (8043374) Type SBC53C Relay, Top Cover Plate Removed (Elevated Rear View)

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STATIC BREAKER BACK-UP RELAY
TYPE SBC53A, SBC53B AND SBC53C

INTRODUCTION

The type SBC53 relay is a rack mounted static breaker failure relay designed to provide system back-up protection in the event of a circuit breaker failure.

This relay incorporates the major requirements of a breaker failure back-up scheme, high security and capability for fast closing times. This relay is applicable with any of the several bus/breaker arrangements in general use and over a wide range of fault current conditions which may be encountered. One type SBC53 relay is required for each breaker.

DESCRIPTION

The SBC53 relay is mounted in a 19-inch rack unit. The SBC53 relay has the following components and features.

1. Input provisions for a contact initiation (BFI, 62X, 62Y) that activates the power supply and the relay.

2. A fast reset current detector with two independently adjustable pickup settings for phase (I_A, I_B, I_C) and ground ($3I_0$) currents.

3. An adjustable timer to provide time for the primary breaker to operate correctly.

4. Six electrically separate contact output circuits (BFT1 and BFT2) with two circuits having electromechanical series targets for tripping the back-up breakers.

5. Three electrically separate instantaneous trip (IT) contacts.

6. A contact converter and AND-OR logic are provided on the B and C models.

7. A regulated power supply with protection against low DC input.

8. Surge suppression on all AC and DC input circuits.

MODEL	INTERNAL CONNECTIONS	COMPONENT LOCATION DIAGRAM	EXTERNAL CONNECTIONS AND LOGIC
SBC53A	4	7, 8	9
SBC53B	5	7, 8	10
SBC53C	6	7, 8	11

APPLICATION

The type SBC53 static breaker failure relay is intended for application on a per breaker basis. That is, there is one breaker failure relay associated with each breaker in a bus array. On this basis the current inputs to a particular SBC53 relay must come from CT's that measure the current in the associated breaker. The trip outputs must be routed to initiate the tripping (or transferred tripping) of all breakers necessary to clear the fault upon failure of the breaker associated with the SBC53 relay. This routing will depend upon the bus breaker arrangement.

The listing in Table 1 covers the bus arrangements that are in common use today. They are the single-bus single-breaker, double-bus double-breaker, breaker-and-a-half, and ring-bus arrangements; and they are shown in Figs. 12, 13, 14 and 15 respectively. Each listing in Table 1 indicates the assumed fault location, the breaker which is assumed to have failed, the contact initiation indicates the assumed fault location, the breaker which is assumed to have failed, the contact initiation that activates the SBC53, and which breakers or lock-out relays should be tripped by the BFT contacts. For example, in a single-bus-single breaker arrangement (Fig. 12), if breaker #2 is to be protected, the SBC53 relay receives the currents associated with breaker #2. The contact initiation is from the protective relays of line B. If breaker #2 fails for a fault at F1, the SBC53 relay operates and BFT contact #1 trips the bus lock-out relay. For another example consider the ring-bus arrangement that is shown in Fig. 15. If breaker 1 is to be protected the SBC53 relay receives the currents associated with breaker 1. The contact initiation is from the protective relays of line A for a fault at F1. For a fault at F2 the protective relays of line B provide the contact initiation. Assuming breaker 1 fails for a fault at F1, the SBC53 relay operates and the BFT contacts trip the following; BFT #1 trips breaker 2 and BFT #2 trips breaker 6. BFT #3 trips the lock-out relay that transfer trips breakers 7 and 8 and blocks reclosing of 2 and 6.

TABLE I

BUS AND BREAKER ARRANGEMENT	FIG. #	FAULT LOC.	FAILED BREAKER	CURRENT FROM ASSOC. BREAKER	CONTACT INITIATION FROM	BFT CONTACT #1 TRIPS	BFT CONTACT #2 TRIPS	BFT CONTACT #3 TRIPS
Single Bus-Single Bkr.	12	F1	2	2	Line B	Bus Lock-out Relay	-	-
Double Bus-Double Bkr.	13	F1 or F2	3	3	Line B or North Bus	North Bus Lock-out Relay	Brkr 4	Lock-out relay that transfer trips line B & blocks reclosing of Brkr 4.
Double Bus-Double Bkr.	13	F1 or F3	4	4	Line B or South Bus	South Bus Lock-out Relay	Brkr 3	Lock-out relay that transfer trips line B & blocks reclosing of Brkr 3.
Breaker and a half	14	F1 or F3	4	4	Line A or North Bus	North Bus Lock-out Relay	Brkr 5	Lock-out relay that transfer trips brkr 10 & blocks reclosing of brkr 5.
Breaker and a half	14	F1 or F2	5	5	Line A or Line B	Breaker 4	Brkr 6	Lock-out Relay that transfer trips brkrs. 10 & 11 & blocks reclosing of brkrs 4 & 6.
Breaker and a half	14	F2 or F4	6	6	Line B or South Bus	South Bus Lock-out Relay	Brkr 5	Lock-out relay that transfer trips brkr 11 & blocks reclosing of brkr 5.

BUS AND BREAKER ARRANGEMENT	FIG. #	FAULT LOC.	FAILED BREAKER	CURRENT FROM ASSOC. BREAKER	CONTACT INITIATION FROM	BFT CONTACT #1 TRIPS	CONTACT #2 TRIPS	BFT CONTACT #3 TRIPS
Ring Bus	15	F1 or F2	1	1	Line A or Line B	Breaker 2	Brkr 6	Lock-out relay that transfer trips brkrs. 7 & 8 & blocks reclosing of brkrs 2 & 6.

In the application of the SBC53 relay probably the most important consideration is the setting of the main timer. Fig. 16 illustrates all the times involved from the instant the fault occurs until the back-up circuit breakers operate to clear the fault. This total time must be short enough to enable the system to maintain stability and to limit as much as possible the damage to the faulted equipment. On the other hand, the total time should be sufficiently long to permit a long enough setting on the breaker failure timer to insure the security of the scheme for normal conditions where the primary circuit breaker clears the fault.

In general, it is a good practice to set the SBC53 timer so that the overall time of operation (including the pickup time of the current detector and the operating time of the BFT output relay) provides for ample margin without infringing on stability limit in the event of a breaker failure. The IEEE Relay Committee recommends at least three cycles of margin.

It is apparent from Fig. 16 that for any given total operating time of the SBC53, reducing the drop-out time of the current detector will increase the margin. Thus, it is recommended for applications where margins of less than three cycles are contemplated that drop-out times be reduced by reducing the setting of the fill-in timer of the current detector. The reduction in drop-out time must be compatible with the acceptable minimum pickup of the current detector. (See Fig. 19.)

The pickup of the current level detector should be set for 67 percent or less of the minimum fault current for which the breaker failure protection must operate. It should be recognized that the function of the current detector is to establish whether or not current is flowing in the associated circuit breaker. In this sense the most sensitive setting is desirable. However, if the settings are such that the current detector is picked up on load, the security of the scheme is reduced since any error in testing, etc., that applies DC to the relay could result in an undesired trip-out.

Another factor in the selection of a pickup setting for the current detector is the type of circuit breaker involved. Some circuit breakers insert resistors in the circuit when clearing a fault. This resistor current is maintained for a significant time and may have a substantial magnitude. For such applications the pickup setting of the current detector should be coordinated with the main timer setting to insure that this resistor current does not result in a false trip. Note that the drop-out to pickup ratio of the current detector in all these relays is higher than 95 percent.

Under normal conditions the SBC53 relays do not have DC applied. Thus, the SBC is normally immune to any response to environmental electrical transients. DC is applied via BFI or 62X functions only when a fault occurs on a line associated with the breaker being protected.

SBC53A

This relay model operates in the following manner: when the power supply is activated the level detector produces an output that energizes the A/O timer. If the timer is energized longer than its setting, it indicates that the primary breaker has failed to clear the fault. The timer should be set long enough to give the breaker a chance to trip but short enough to ensure system stability and maximum continuity of service by operating faster than remote second zone relays. Once the A/O timer operates it energizes a transistor switch that in turn picks up BFT. If the primary breakers had cleared the fault then both the contact initiation (BFI, 62X, 62Y) and the level detector would have dropped out before the timer could have timed out and no back-up tripping would take place.

SBC53B

The SBC53B relay is similar to the 53A except for the addition of a contact converter CC1. The function of the contact converter is to convert a contact operation into a signal that is compatible with the logic circuit of the SBC53 relay. By closing an external contact DC is supplied to the contact converter and an output signal is produced from CC1 once the power supply is activated by the contact initiation (BFI, 62X, 62Y). The signal from CC1 supervises the A/O timer in one of two ways. The choice depends on

the position of the link that precedes the A/O timer. If the link is placed in the OR position, the A/O timer is controlled by an output from the level detector or an output from CC1. The timer will reset only if both the level detector and CC1 reset or the contact initiation resets. If the link is placed in the AND position, the A/O timer is controlled by an output from the level detector and an output from CC1 via the AND2 logic function. For this case the A/O timer will reset if either the level detector or CC1 resets or the contact initiation resets. The IN/OUT link controls the level detector input to both the OR and the AND gates. The IT relay can be operated from either the level detector, the contact converter or the AND/OR gate output.

SBC53C

The SBC53C is similar to the SBC53A except a B/O timer is added. The A/O timer is operated directly from the level detector and is completely separate from the B/O timer. BFT1 is operated from the A/O timer and BFT2 is operated from the B/O timer. The B/O timer is operated from either the AND or the OR gate output where the gate inputs are (1) level detector output and (2) the contact converter output. The IN/OUT link may be used to isolate the level detector from the AND/OR gates.

RANGES

PHASE CURRENTS

Pickup current is continuously adjustable from one to ten amperes on any phase by means of tap adjustments and a rheostat.

Tap Ranges:

1A - 2A)
2A - 4A) See Fig. 1 for tap selections.
4A - 10A)

GROUND CURRENT

Pickup current is continuously adjustable from 0.5 to 5 amperes by means of a tap adjustment and a rheostat.

Tap Ranges:

0.5A - 1.0A)
1.0A - 2.0A) See Fig. 1 for tap selections
2.0A - 5.0A)

TIMER

A/O timer (50 - 500 milliseconds). Rheostat location is on the printed circuit card.

B/O timer (50 - 500 milliseconds). Rheostat location is on the printed circuit card.

RATINGS

The SBC53 current circuits are rated at 10 amps continuously, and have one second thermal rating of 210 amps.

CAUTION: WHEN HI-POTTING THE SBC53 REMOVE ALL EXTERNAL WIRING FROM TERMINALS EA1, EB1, EC1 AND ED1. DO NOT HI-POT THESE TERMINALS. THE REASON IS THAT CAPACITORS C1 - C12 ARE RATED FOR 600 VDC AND THE HI-POT VOLTAGE MAY DAMAGE THE CAPACITORS.

The breaker failure tripping telephone relay (BFT) is continuously rated at nameplate rated DC supply voltage. Table II lists the ratings of the six electrically separate BFT contacts.

TABLE II

BFT CONTACT RATINGS

RATING	CONTINUOUS CURRENT AMPS	TRIP DUTY AMPS	INTERRUPTION CURRENT (AMPS) INDUCTIVE**	NON-INDUCTIVE
125V DC	3	30	0.5	1.5
250V DC	3	30	0.25	1.0
115V 60 HZ	3	30	0.75	2.0
230V 60 HZ	3	30	0.50	1.5

**The inductive rating is based on the inductance of an average trip coil.

The rating of the electromechanical targets (T1 and T2) is one amp.

SURGE WITHSTAND CAPABILITY

The SBC53 relay will withstand the following test voltage waveform without incorrect operation or damage to any component.

The test voltage waveform consists of a high frequency damped oscillation with a frequency of 1.5 megahertz. The source has an internal impedance of 150 ohms. The initial value (zero to peak) is 2500 volts and the damping is such that the envelope of the waveform decays to half the initial value (1250 volts) in 6.0 microseconds. The test voltage is applied between relay surge ground and each of the other relay terminals.

BURDENS

The AC burden for each of the current transformer circuits is tabulated in Table III for five amperes of 60 hertz current through each basic current setting range, minimum and maximum respectively.

The overall battery drain at relay terminals EB9 and EB11 is itemized in Table IV for three voltages.

CHARACTERISTICS

Aside from the logic functions there are four (4) basic units the characteristics of which are important to the application of the SBC53 relay. These are noted below.

TABLE III

5 AMP, 60 HERTZ BURDEN

BASIC RANGE	P.U. SETTING (AMPS)	VOLT-AMPS I^2Z (I=5 AMPS)	IMPEDANCE (OHMS)	POWER-FACTOR (LAGGING DEGREES)
Phase (1-2A)	1	0.54	0.021	21
Ground (0.5-1A)	0.5	1.12	0.045	14
Phase (1-2A)	2.0	0.51	0.021	23
Ground (0.5-1A)	1.0	1.1	0.044	34
Phase (2-4A)	2.0	0.34	0.014	15
Ground (1-2A)	1.0	0.57	0.023	19
Phase (2-4A)	4.0	0.33	0.014	18
Ground (1-2A)	2.0	0.54	0.022	27
Phase (4-10A)	4.0	0.27	0.011	19
Ground (2-5A)	2.0	0.38	0.016	18
Phase (4-10A)	10.0	0.27	0.011	20
Ground (2-5A)	5.0	0.38	0.015	26

TABLE IV

BATTERY DRAIN

RATED DC	DC DRAIN (MILLIAMPS)
48 VDC	135
125 VDC	130
250 VDC	115

POWER SUPPLY

The SBC53 relay covered by this book, contains a regulated power supply. This power supply regulates the voltage to the logic functions so that they perform properly over a range of applied DC voltage from 80 percent to 110 percent of rated voltage. The power supply card also provides defense against operation for grounding of relay terminal EB9. The power supply card must see greater than 60 percent of battery voltage before the power supply will be switched on.

OUTPUT RELAY (BFT1 and BFT2)

The trip output of the SBC53 relay consists of two high speed telephone relays with several contacts. The contacts will close within 1/4 cycle of the instant that the coil circuit is energized from the logic. However, a shorter pulse of energization may also cause the output relay to close its contacts. This is in effect "overtravel". The overtravel of the output relay is less than two milliseconds. The drop-out time of the output relay is somewhat longer than two cycles.

TIMER

The timer in the SBC53 relay is extremely accurate and repeatable in performance. At any given temperature and setting the timer will repeat its timing operation to within plus or minus two percent of its setting. Over the entire range of applied DC voltage from 80 to 110 percent of rating or temperature from -20 to +60 degrees centigrade, the timer will hold its setting to within plus or minus five percent of setting.

The timer in the SBC53 relay has a very quick reset. If the input to the timer is removed for a time in the order of 0.2 milliseconds or longer it will reset completely. Thus, in order for the timer to time out it requires a continuous unbroken input for the complete timing cycle.

CURRENT DETECTOR

The current detector in the SBC53 relay is comprised of magnetic input circuits for each phase current and $3I_0$, pickup setting potentiometers, one level sensing circuit, and a fill-in timer. See Fig. 18. The level sensing circuit produces an output when the instantaneous magnitude of the input exceeds its fixed pickup sensitivity. The output will go away as soon as the instantaneous magnitude of the input gets below its fixed drop-out level which is greater than 95 percent of the pickup level. The fill-in timer will produce an output as soon as a signal appears at its input. This output will persist until the input from the level sensing circuit goes away and the adjustable timer delayed drop-out setting on the fill-in timer expires.

As will be noted from Fig. 18 the input to the level sensing circuit is provided with four transactor circuits. The voltage output from each transactor is proportional to the respective current inputs. The outputs of the transactors are individually rectified and the phase circuits are separated from the ground ($3I_0$) circuit. A portion of each of the two circuits is supplied to the level sensing circuit via potentiometers. Since the sensitivity of the level sensing circuit is fixed by design, the pickup settings for phase and ground currents are made independently by means of the two potentiometers in conjunction with the current tap selection. Note, that since the output of all three phase bridge rectifier circuits are in parallel, the level detector responds to the highest of the three phase currents.

For a phase-to-phase or phase-to-ground fault or single-phase test simulation, the voltage applied to the input of the level sensing circuit will be a full wave rectified signal. This signal starts at zero magnitude, builds up to a maximum on a sine wave curve, and then drops off on a sine wave curve to zero magnitude. This is repeated as long as the current input conditions exist. It is obvious that the output of the level sensing circuit cannot be continuous under these conditions since it will, regardless of the magnitude of the input, drop out twice each cycle every time the rectified input approaches and passes through zero. It is for this reason that the fill-in timer is employed to "ride over" these gaps in output from the level sensing circuit. The amount of fill-in time required will depend on the magnitude of

the input to the level sensing circuit. The range of pickup adjustment as given under the section on RATINGS is based on the assumption that the fill-in timer will be set for (8.7 milliseconds) something longer than a half-cycle dropout so that a continuous output from this timer will be obtained when the peak value of the input signal to the level sensing circuit is just equal to the sensitivity of that circuit. This is the normal factory setting of the fill-in timer and it results in a "drop-out" time of the current detector that is about 10 milliseconds. (See Fig. 19). The drop-out time is somewhat longer than the fill-in time because of the stored energy in the magnetic circuits after the current disappears.

As was noted above, the main timer required continuous input for the duration of its settings in order to time out. Thus, a continuous output is required from the fill-in timer. If faster overall drop-out time of the current detector is required, it is necessary to reduce the fill-in timer setting. With this reduced fill-in timer setting and no other change, a higher input current will be required into the current detector circuits in order to produce a continuous output from the fill-in timer. (See Fig. 20). It is important to note that pickup of the current detector is defined as the RMS sine wave current applied at the input of the relay that produces a continuous output from this detector for the given fill-in timer setting. It should be recognized that in making the pickup setting only single phase current inputs should be used. Three phase current inputs tend to fill in the gaps so that the input to the level sensing circuit never goes to zero (see Fig. 21).

In summation, the normal factory setting on the fill-in timer is set for approximately nine milliseconds. With this setting the drop-out time of the current detector will be about ten milliseconds. The range of pickup adjustment will be as given under the section on RATINGS. If faster drop-out times are desired, the fill-in timer must be set for a shorter time and this in effect raises the pickup of the relay. This relationship is illustrated in Fig. 17. Pickup current is defined as the RMS sine wave current required to produce a continuous output from the current detector.

Since in the application of the SBC53 relay, no DC voltage is applied until after the associated line relays operate, there will be some slight operating delay in the pickup of the current detector. Fig. 22 indicates the maximum and minimum operating times as a function of current as a multiple pickup setting. The variation in time is a result of the instant in the current cycle at which the DC is applied. Note that these curves apply for single-phase fault or single-phase test currents. For three-phase faults or three-phase test currents the minimum time curve will apply regardless of the incident angle of the current at the instant the DC is applied.

SETTINGS

The following settings must be made in the SBC53 relay covered by this book. The settings should be made in the order in which they are listed below.

1. Current detector fill-in timer setting
2. Main time-delay setting (A/O)
3. Secondary time-delay setting (B/O)
4. Phase current pickup setting.
5. Ground current pickup setting
6. Link position settings

The section under APPLICATION itemized the considerations involved in the selection of settings for items 1 - 5 above.

There are reasons for the order listed above in which the settings should be made. These reasons and other considerations are noted below.

It is important that the fill-in timer setting be made first because, as explained in the section under CHARACTERISTICS, the pickup range of the current detector will vary depending on this setting. The section under ACCEPTANCE TESTS describes exactly how this setting should be made or checked.

The next setting to be made is the time delay of the main timer. Since in the field the SBC53 relay does not normally have DC voltage applied, the current detectors are not operating regardless of magnitude of current until BFI or 62X contacts close to apply DC. This means that before the timer can start timing

it is necessary for the fault detectors to pick up. For this reason it is necessary to set the main timer so that the overall time from the instant the DC voltage is applied to the relay until an output is obtained from the BFT contacts is equal to the desired time delay. This test must be performed with current into the relay prior to applying the DC.

The magnitude of this current is an important consideration in this setting. Since the current detector cannot pick up until the instantaneous magnitude of the input current exceeds its sensitivity, there can be some variation in timing on a statistical basis depending on what instant in the current cycle the DC voltage is applied. In order to limit this variation it is recommended that the input current to the relay be selected in the range of five to ten times the pickup setting. Thus, for setting this timer it is suggested that single phase current be fed into the ground circuit with the ground pickup setting on the minimum possible setting. This input current should then be selected to be about five to ten times the RMS value required to get a continuous output from the current detector. This arrangement will limit the statistical variation to some fraction of a millisecond. The circuit and the instructions to make these settings are given in the section under ACCEPTANCE TESTS.

It should be noted that with the above settings the relay will, for severe faults, operate in the set time. For low current faults it may get a few milliseconds slower which is in the direction to provide slightly more margin for these faults where stability and damage considerations are considerably less onerous.

The SBC53C has two timers (A/O and B/O). The B/O timer can be set independently of the A/O timer and the IN/OUT link should be IN and the AND/OR link should be in the OR position.

After setting the time delays the pickup settings on phase and ground currents should be made as indicated under ACCEPTANCE TESTS. The considerations related to the actual settings to select have been discussed in the section under APPLICATION.

OPERATING PRINCIPLES

INTRODUCTION

The operating sequence of logic signals for the SBC53 can be followed with the aid of the internal connections diagram as shown in Figs. 4, 5, and 6.

PRINTED CIRCUIT CARDS

The following sections describe the operation of the printed circuit cards. Table V shows the printed circuit card internal included in SBC53 model.

TABLE V

Printed Circuit Card Internals Figure									SBC Model
PC-1	PC-2	PC-3	PC-4	PC-5	PC-6	PC-7	PC-8	T	
23	24		26		28	29	30	31	53A
23	24		26	27	28	29	30	31	53B
23	24	25	26	27	28	29	30	31	53C

PC-1 CARD (Level Detector with Adjustable "FILL-IN)

The operational amplifier's inverting input is biased at approximately +2.4 volts DC. While the input at TP3 is below this level, TP has a negative voltage level present. As this (non-inverting input) signal becomes more positive than the 2.4 VDC, the Op-Amp swings positive and drives Q1 on.

In a quiescent dropped out state then, TP3 is a negative zero signal; Q1 is off, Q2 is off, the unijunction oscillator P1, C3 and Q3 are oscillating; Q5 is off; Q6 is on and the signal at TP4 is zero. When TP3 comes high, Q1 goes on, the unijunction oscillator stops oscillating and the capacitor C3 is fully discharged, Q2 comes on, Q4 stays non-conducting, Q5 comes on, Q6 goes off, and the output at TP4 comes high.

Now as the TP3 signal goes toward zero again, Q1 goes off, Q2 remains conducting by virtue of the previously conducting Q5 and feed back loop D3, D4 and R14. The C3 capacitor begins to charge with the (R10+P1) X (C) time constant, and the output signal remains on.

When the C3 capacitor voltage reaches the firing level of the unijunction, a pulse is generated thus turning on the SCR Q4, which turns off Q5, resets the feed back circuit, drives Q6 on and yields a zero output voltage. In effect, the circuitry after the Op-Amp provides the adjustable "Fill-in" time (time-delay drop-out) described elsewhere in this text.

In practice, the RC time constant is factory set such that the time delay on the card (P1 adjustment) is slightly greater than 1/2 cycle on a 60 hertz basis (i.e., approximately 8.7 milliseconds).

Since the A/O timer resets in less than 1/4 milliseconds, this "Fill-In" time plus energy decay time in the magnetics both contribute to the total drop-out time shown in Fig. 19.

PC-2 Card (A/O timer) Card Slot P (or R for SBC53B)

In the quiescent off state (not timing) Q1 is off, Q2 is on, C3 is fully discharged, Q4 is off.

In the timing state, Q1 is turned on by the presence of an input signal. Q2 is off and C3 is charging thru R7 and the rheostat. At pickup, C3 is charged to approximately 6.5 volts and Q4 turns on. The output is on Pins #8 and #9 except for the SBC53C where the jumper is set on "1" and the output only appears on Pin #8.

The timing range for the A/O timer is from 50 to 500 milliseconds and is adjusted by a 0.75 meg ohm linear potentiometer on the card.

PC-3 Card (B/O timer) Card Slot R

The PC-3 card is the same as the PC-2 card except the output is only from Pin #9.

PC-4 Card (Instantaneous Trip (IT) Card Slot K

The (IT) function can be selected from either the level detector, AND/OR gate or the contact converter.

During quiescent operation, Q1, Q2 and Q3 are all off. A positive level turns on Q1, Q2 and Q3 and the output contacts #7 & #9 close.

PC-5 Card (Contact Converter, Logic Gates AND/OR) Card Slot L

This card consists of one two-input AND gate, one two-input OR gate, and a contact converter input.

One of the card inputs is from the contact converter and is fed to one input of the AND gate and one input of the OR gate. The other card input goes through a link for disconnecting if required and is then fed to an input of the AND gate and an input of the OR gate. A link on the single output terminal selects either the AND or the OR gate output.

The contact converter input has a link to select the proper operating voltage.

PC-6 Card (Output Reed Switch and Neutral Current Bridge) Card Slot J

The output reeds are energized by a zero voltage input at either Pin #5 or #6. The Pin #5 input closes the output contacts at Pins #8 and #9. Pin #6 input closes the output contacts at Pins #7 and #9.

A full wave bridge has inputs on Pins #2 and #4 and a positive output from Pin #3.

PC-7 Card (Three Full Wave Bridges) Card Slot H

This card functions as a full wave bridge for the three phase and residual transactor secondary circuits.

The inputs and outputs are noted below:

PHASE	INPUT PIN	OUTPUT PIN
A	3, 4	10
B	5, 6	10
C	7, 8	10

Reference is Pin 2

Note that the three(3) phase outputs are logically "ORed" on this board at output Pin 10. In short, this means that the phase voltage of greatest magnitude in time will prevail at the output Pin 10.

PC-8 Card (Zener Regulated Power Supply) Card Slot S

The Y card provides a regulated source of ±10.2 VDC to the relay logic. A level detector set at 60 to 80 percent of the DC input disables the power to the SBC in case of accidental grounding of the battery.

Test Card - Card Slot T

A test card is inserted in slot T and brings out all ten terminals of the socket. Refer to the internal connection for test point location on a particular model.

CURRENT DETECTORS

The three phase elements (I_A, I_B, I_C... the outputs of which are combined in logical OR) and the residual element ($3I_0$) are independently adjustable from the front of the relay in continuous increments as follows:

PHASE	RESIDUAL
1-2A	0.5-1A
2-4A	1-2A
4-10A	2-5A

The four (4) links at the bottom of the relay provide for the above listed discrete ranges of adjustment, while the two (2) rheostats provide for the continuous adjustment within a range. The four tap blocks are identified as I_A, I_B, I_C, and $3I_0$ respectively; and range selection for the three position tap blocks increases from left to right. The seven (7) lines scribed on the nameplate associated with each rheostat indicates an approximate current detector pickup level calibration (factory) in multiples of the base pickup as follows reading clockwise: 1.0, 1,2, 1.4, 1.6, 1.8, 2.0, 2.5 X (base pickup).

Note that these pickup calibration marks apply to the factory convention of setting the current detector with 8.7 millisecond "fill-in" time.

The following two examples demonstrate the current detector setting calculation using the calibration marks. The assumption is, of course, that the current detector has an undisturbed factory calibration.

1. The I_A tap block screw is in the middle position (range 2-4A). The phase rheostat knob is pointing at the fourth mark from the left (1.6X range base). Since the relay is in the range 2-4A the range base equals 2A. Multiplying the range base by the calibration mark multiple, we have: Pickup: 1.6 X 2 = 3.2A. So, approximately 3.2A RMS through the I_A current circuit is the level of current necessary to pick up the current detector. Similarly, the above applies for B and C phase current.

2. The residual ($3I_0$) tap block screw is in the right position (range 2-5A). The $3I_0$ rheostat knob is pointing at the second calibration mark from the left (1.2X base range). Since the relay is in the range 2-5A, the $3I_0$ range base equals 2A. Multiplying the range base by the calibration mark multiple, we have: Pickup: 1.2 X 2 = 2.4A. So, approximately 2.4A RMS through the $3I_0$ current circuit level of residual current is necessary to pick up the current detector.

ACCEPTANCE TESTS

Immediately upon receipt of the relay an inspection and acceptance test should be made to insure that no damage has been sustained in shipment and that the relay calibrations have not been disturbed. If the examination or test indicates that readjustment is necessary, refer to the section on SERVICING.

CAUTION: WHEN HI-POTTING THE SBC53 REMOVE ALL EXTERNAL WIRING FROM TERMINAL EA1, EB1, EC1, ED1. DO NOT HI-POT THESE TERMINALS. THE REASON IS THAT CAPACITORS C1-C12 ARE RATED FOR 600 VDC AND THE HI-POT VOLTAGE MAY DAMAGE THE CAPACITORS.

These tests may be performed as part of the installation or acceptance tests at the discretion of the user. Since most operating companies use different procedures for acceptance and installation tests, the following section includes all applicable tests that may be performed on these relays.

Setting or checking all SBC relays consists of the following tests and these tests must be performed in the following order.

FILL-IN TIMER SETTING

The fill-in timer is essentially an adjustable drop-out timer which is factory set to 8.7 milliseconds. Other fill-in times less than 8.7 milliseconds are obtainable, but lowering the fill-in raises the pickup level as shown on the graph of Fig. 17. As an example, if the fill-in time of five milliseconds is required and set, then the five millisecond fill-in pickup level is approximately 1.24 times the 8.7 millisecond setting. (See Fig. 17 and the CHARACTERISTICS section for other parameters).

The timer and its associated adjustment potentiometer are located on the PC-1 card. Set up the test circuit shown on Fig. 32 and perform the following:

1. Apply rated DC to relay terminals EB-9 and EB-10.

2. Make the oscilloscope and contact circuits described on Fig. 32 being certain to observe the caution that the scope power cord is ungrounded. The reason for this latter caution is the relay signal reference is at a different potential than the system ground.

Opening the normally open contact in the circuit removes signal from the timer input and thereby allows for fill-in timer measurement.

Place the scope in an external triggering mode with negative slope and note that upon opening the depressed normally open contact, a positive signal goes to about zero volts in about 8.5 - 9.0 milliseconds. If the measurement is less than or greater than this range, correctly set the time to precisely 8.7 milliseconds by adjusting the potentiometer of the PC-1 card.

CURRENT DETECTOR PICKUP TEST

Having checked or adjusted the fill-in time setting, set up the test current circuit of Fig. 33.

Connect an oscilloscope such that the vertical input is connected to TP4 and reference is connected to TP1. The oscilloscope power cord should be ungrounded.

The following test is for a fill-in time setting of 8.7 milliseconds:

1. Set all current tap blocks as follows:

I_A	1-2A
I_B	1-2A
I_C	1-2A
$3I_0$	0.5-1

2. Set both current rheostat pointers to the 1X range base (first calibration line going clockwise).

3. Apply current to the I_A terminals per Fig. 33 until the oscilloscope indicates a continuous DC output. The input current shall be approximately one (1) ampere.

4. Repeat three (3) above for phase B and C.

5. Apply current to the $3I_0$ terminals per Fig. 33 until the oscilloscope indicates a continuous DC output. The input current shall be approximately 0.5 amps.

6. Using the procedure above, check the other taps and multiples of current settings.

To test the current detector pickup for fill-in times less than 8.7 milliseconds use the above procedure except that the pickup currents will be higher and have approximate values per Fig. 17. Also, see CHARACTERISTICS section for other parameters.

CURRENT DETECTOR PICKUP SETTING

Use the procedure of the previous section except set the current rheostats to the desired current pickup and secure the rheostats.

A/O OR B/O TRIPPING TIMERS

The "A" or "B" signifies a continuously adjustable pickup time delay in the range of 50 to 500 milliseconds. The "O" signifies that the timer resets "instantaneously" (in reality, in less than 200 microseconds).

Set up the AC, DC and oscilloscope connections shown in Fig. 34. Apply the current to the ground circuit on the 0.5 tap at X1 base pickup. Observe the following two cautions:

CAUTION:

1. THE SYSTEM SIDE CIRCUITS OF THE BFT CONTACTS MUST BE REMOVED BEFORE THE TEST CONNECTIONS ARE MADE (USE OF AN XLA TEST PLUG IS RECOMMENDED).

2. THE OSCILLOSCOPE MUST NOT BE GROUNDED...USE A THREE-TO-TWO PRONG POWER CORD ADAPTER. THE REASON FOR THIS LATTER CAUTION IS THAT RELAY REFERENCE IS NEAR (-) DC POTENTIAL AND GROUND POTENTIAL IS GENERALLY ABOUT 1/2 DC POTENTIAL.

To check or set the timer, use the following procedure:

Set the test current into the relay at 5X pickup. Upon closing the BFI contact of Fig. 34, the scope trace is initiated. Note that since rated DC voltage is triggering the scope, the trigger feature should be operated in the attenuated mode. After the timer under test (A/O or B/O has timed out and the BFT relay has operated, the BFT contacts close and the scope trace goes to zero volts. The time from trace initiation until the signal goes to zero is the breaker failure tripping time.

1. SBC53A (A/O) Initiate timing of the relay as explained above by closing the BFI contact. Set the length of tripping time by adjusting the A/O potentiometer.

2. SBC53B (A/O) Card is in R position. Initiate timing by closing the contact converter (EB11) input to (+) DC. The logic link on PC-5 should be in the OR position. Set the length of tripping time by adjusting the A/O timer potentiometer. The output contacts are BFT2.

3. SBC53C (A/O and B/O) The A/O timer is adjusted the same as the SBC53A model. The B/O (card slot R) is adjusted the same as the A/O timer in the SBC53B.

LOGIC FUNCTIONS, SETTINGS AND TESTS

Having set the current detectors and the A/O timer, perform the following tests using the Fig. 33 test circuit for the I_A configuration. Let the test current be 1.5X current detector pickup.

SBC53A - No additional tests

SBC53B and SBC53C - Keep switch (s_1) closed.

Place the logic link in the OR position. Check that by either applying test current alone or closing the AUX contact alone or by doing both, the BFT relay operates.

Place the logic link in the AND position. Check that the BFT relay operates only when the test current is applied and the AUX contact is closed simultaneously.

Place the logic link in the required mode of operation.

INSTALLATION PROCEDURE

INTRODUCTION

The location should be clean and dry, free from dust and excessive vibration, and well lighted to facilitate inspection and testing.

The relay should be mounted on a vertical surface. The outline and panel diagram is shown in Fig. 35.

The internal connection diagram for the relay is shown in Figs. 4, 5 and 6. The wiring diagram is given in Figs. 9, 10 and 11.

One of the mounting studs or screws should be permanently connected to surge ground by a conductor not less than No. 12 AWG gage copper wire or its equivalent.

The relay may be tested without removing it from the panel by using a 12XLA13A test plug. This plug makes connections only with the relay and does not disturb any shorting bars in the case. Of course, the 12XLA12A test plug may also be used. Although this test plug allows greater testing flexibility, it also requires CT shorting jumpers and the exercise of greater care since connections are made to both the relay and the external circuitry. Additional information on the XLA test plugs may be obtained from GEI-25372.

All alternating current operated devices are affected by frequency. Since non-sinusoidal waveforms can be analyzed as a fundamental plus harmonics of the fundamental frequency, it follows that alternating current devices (relays) will be affected by the applied waveform. Therefore, in order to properly test alternating current relays it is essential to use a sine wave of current.

CAUTION: WHEN HI-POTTING THE SBC53 REMOVE ALL EXTERNAL WIRING FROM TERMINALS EA1, EB1, EC1, ED1. DO NOT HI-POT THESE TERMINALS. THE REASON IS THAT CAPACITORS C1-C12 ARE RATED FOR 600 VDC AND THE HI-POT VOLTAGE MAY DAMAGE THE CAPACITORS.

Since most operating companies use different procedures for installation tests, the section under ACCEPTANCE TESTS contains all necessary tests which may be performed as part of the installation procedure at the discretion of the user.

The minimum suggested tests are as follows:

TIMER TEST

Test per timing test as explained in section titled ACCEPTANCE TESTS.

CURRENT DETECTOR PICKUP SETTING

Set up the test current circuit of Fig. 33.

Place an oscilloscope on TP4 as an indication of current detector pickup. Note that a "0" volt signal denotes dropout and a positive DC signal represents current detector pickup.

As a quick check on each of the relay calibration marks, perform the following:

Place all current tap block screws in the middle position.

I_A	2-4A
I_B	2-4A
I_C	2-4A
$3I_0$	1-2A

Place both current rheostat pointers to the first calibration line (i.e., 1X range base).

Apply test current to each of the four current circuits per Fig. 33 and adjust the current level until the "A" card TP4 indicates that the current detector has just picked up. The current levels should be as follows for the four circuits: 1.9-2.1A RMS phase circuits---0.95-1.05A RMS residual circuit.

Having selected the phase and residual current detector settings to be used on the system (1-10A for phase and 0.5-5A for residual) set the tap plugs to the appropriate range selection: as an example a 6A phase setting should use the third tap block range (4-10A). Set up the I_A current circuit of Fig. 33, and set the RMS value of current to the desired current detector pickup level exactly. Slowly adjust the phase rheostat till the current detector just picks up. Check that the current detector pickup level on the remaining two phases is plus five percent of the original setting. Lock the phase rheostat and be sure that the current detector setting has not drifted in the interim. Arrange the $3I_0$ current circuit of Fig. 33, and calibrate the residual rheostat until the current detector just picks up. Lock the residual rheostat, and check that the operate level has not changed.

PERIODIC CHECKS AND ROUTINE MAINTENANCE

In view of the vital role of protective relays in the operation of a power system it is important that a periodic test program be followed. It is recognized that the interval between periodic checks will vary depending upon environment, type of relay and the user's experience with periodic testing. Until the user has accumulated enough experience to select the test interval best suited to his individual requirements it is suggested that the points listed under INSTALLATION PROCEDURE be checked at an interval of from one to two years.

CONTACT CLEANING

For cleaning relay contacts, a flexible burnishing tool should be used. This consists of a flexible strip of metal with an etched-roughened surface resembling in effect a superfine file. The polishing action is so delicate that no scratches are left, yet it will clean off any corrosion thoroughly and rapidly Its flexibility insures the cleaning of the actual points of contact. Do not use knives, files, abrasive paper or cloth of any kind to clean relay contacts.

SERVICING

Should servicing of the relay become necessary, follow the test procedures as explained in the section titled ACCEPTANCE TESTS, for calibration and test of the relay. Telephone relay contact cleaning is located in the section titled PERIODIC CHECKS AND ROUTINE MAINTENANCE. Also, see section on RENEWAL PARTS for servicing printed circuit cards.

CONSTRUCTION

The SBC53A relay is packaged in an enclosed metal case with a hinged front cover and a removable top cover. The case is suitable for mounting on a standard 19 inch rack. The outline and mounting dimensions of the case are shown in Fig. 35.

On the rear of the case are four 12 point terminal strips, EA, EB, EC, and ED.

There are eight printed circuit cards and one test card in the SBC53 relay. The location of these cards is given in the component location diagram in Fig. 8. For the identification of the test points refer to the internal connection diagram in Figs. 4, 5 and 6.

RECEIVING, HANDLING AND STORAGE

These relays will normally be supplied as a part of a static relay equipment, mounted in a rack or cabinet with other static relays and test equipment. Immediately upon receipt of a static relay equipment, it should be unpacked and examined for any damage sustained in transit. If injury or damage resulting from rough handling is evident, file a damage claim at once with the transportation company and promptly notify the nearest General Electric Sales Office.

Reasonable care should be exercised in unpacking the equipment. If the equipment is not to be installed immediately, it should be stored indoors in a location that is free from moisture, dust, and metallic chips, and severe atmospheric contaminants.

Just prior to final installation the shipping support bolt should be removed from each side of all relay units, to facilitate possible future unit removal for maintenance. These shipping support bolts are approximately eight inches back from the relay unit front panel. Static relay equipment, when supplied in swing rack cabinets, should be securely anchored to the floor or to the shipping pallet to prevent the equipment from tipping over when the swing rack is opened.

RENEWAL PARTS

It is recommended that sufficient quantities of renewal parts be carried in stock to enable the prompt replacement of any that are worn, broken, or damaged.

Should a printed circuit card become inoperative, it is recommended that this card be replaced with a spare. In most instances, the user will be anxious to return the equipment to service as soon as possible and the insertion of a spare card represents the most expeditious means of accomplishing this. The faulty card can then be returned to the factory for repair or replacement.

Although it is not generally recommended, it is possible with the proper equipment and trained personnel to repair cards in the field. This means that a trouble-shooting program must isolate the specific component on the card which has failed. By referring to the internal connection diagram for the card, it is possible to trace through the card circuit by signal checking and, hence determine which component has failed. This, however, may be time consuming and if the card is being checked in place in its unit, as is recommended, will extend the outage time of the equipment.

CAUTION: GREAT CARE MUST BE TAKEN IN REPLACING COMPONENTS ON THE CARDS. SPECIAL SOLDERING EQUIPMENT SUITABLE FOR USE ON THE DELICATE SOLID-STATE COMPONENTS MUST BE USED AND, EVEN THEN, CARE MUST BE TAKEN NOT TO CAUSE THERMAL DAMAGE TO THE COMPONENTS, AND NOT TO DAMAGE OR BRIDGE OVER THE PRINTED CIRCUIT BUSES. THE REPAIRED AREA MUST BE RECOVERED WITH A SUITABLE HIGH-DIELECTRIC PLASTIC COATING TO PREVENT POSSIBLE BREAKDOWNS ACROSS THE PRINTED CIRCUIT BUSES DUE TO MOISTURE OR DUST.

ADDITIONAL CAUTION: DUAL IN-LINE INTEGRATED CIRCUITS ARE ESPECIALLY DIFFICULT TO REMOVE AND REPLACE WITHOUT SPECIALIZED EQUIPMENT. FURTHERMORE, MANY OF THESE COMPONENTS ARE USED ON PRINTED CIRCUIT CARDS WHICH HAVE BUS RUNS ON BOTH SIDES. THESE ADDITIONAL COMPLICATIONS REQUIRE VERY SEPCIAL SOLDERING EQUIPMENT AND REMOVAL TOOLS AS WELL AS ADDITIONAL SKILLS AND TRAINING WHICH MUST BE CONSIDERED BEFORE FIELD REPAIRS ARE ATTEMPTED.

When ordering renewal parts, address the nearest Sales Office of the General Electric Company, specify quantity required, name of the part wanted, and the complete model number of the relay for which the part is required.

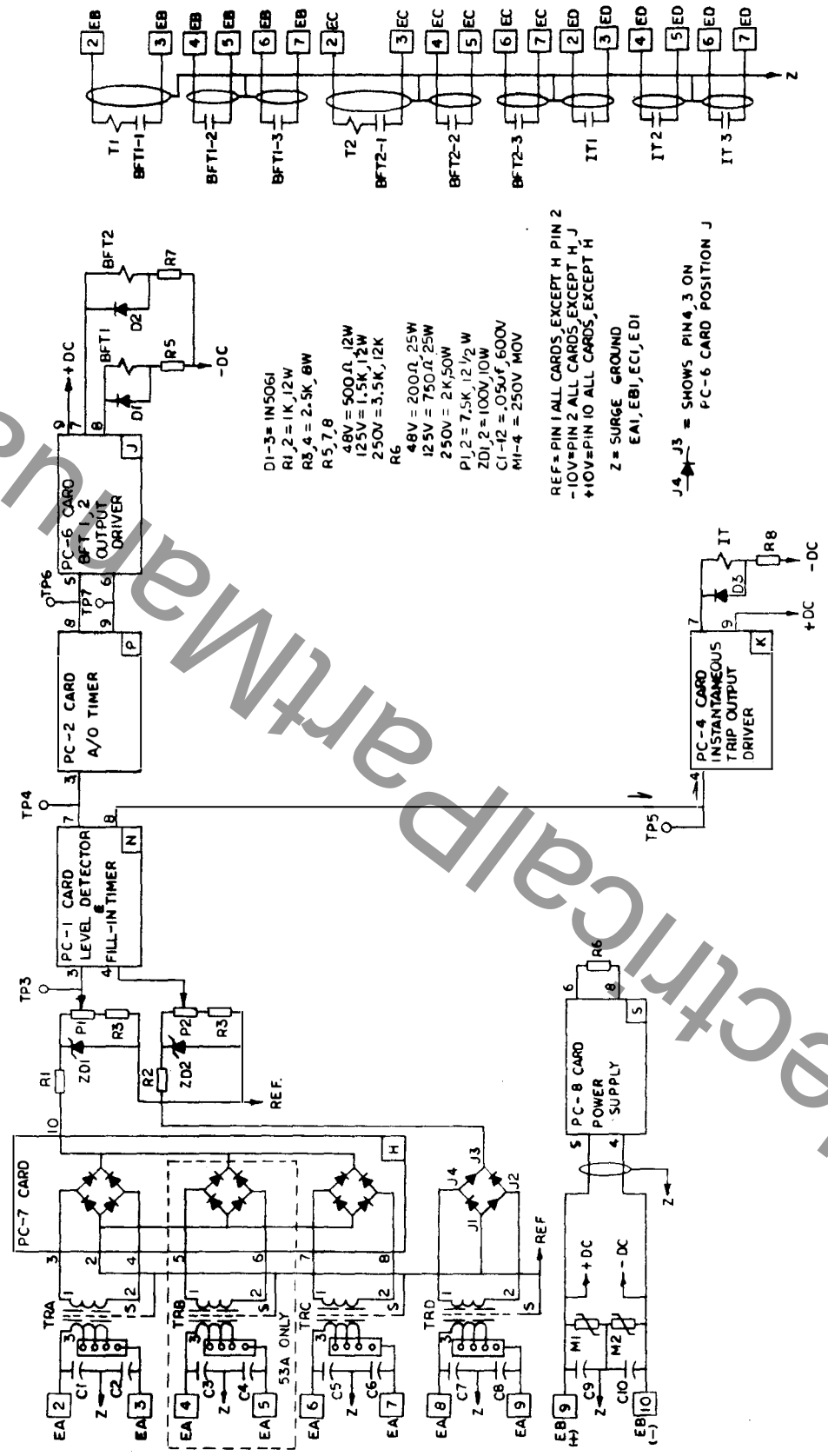


Fig. 4 (0108B8991-0) Internal Connections SBC53A

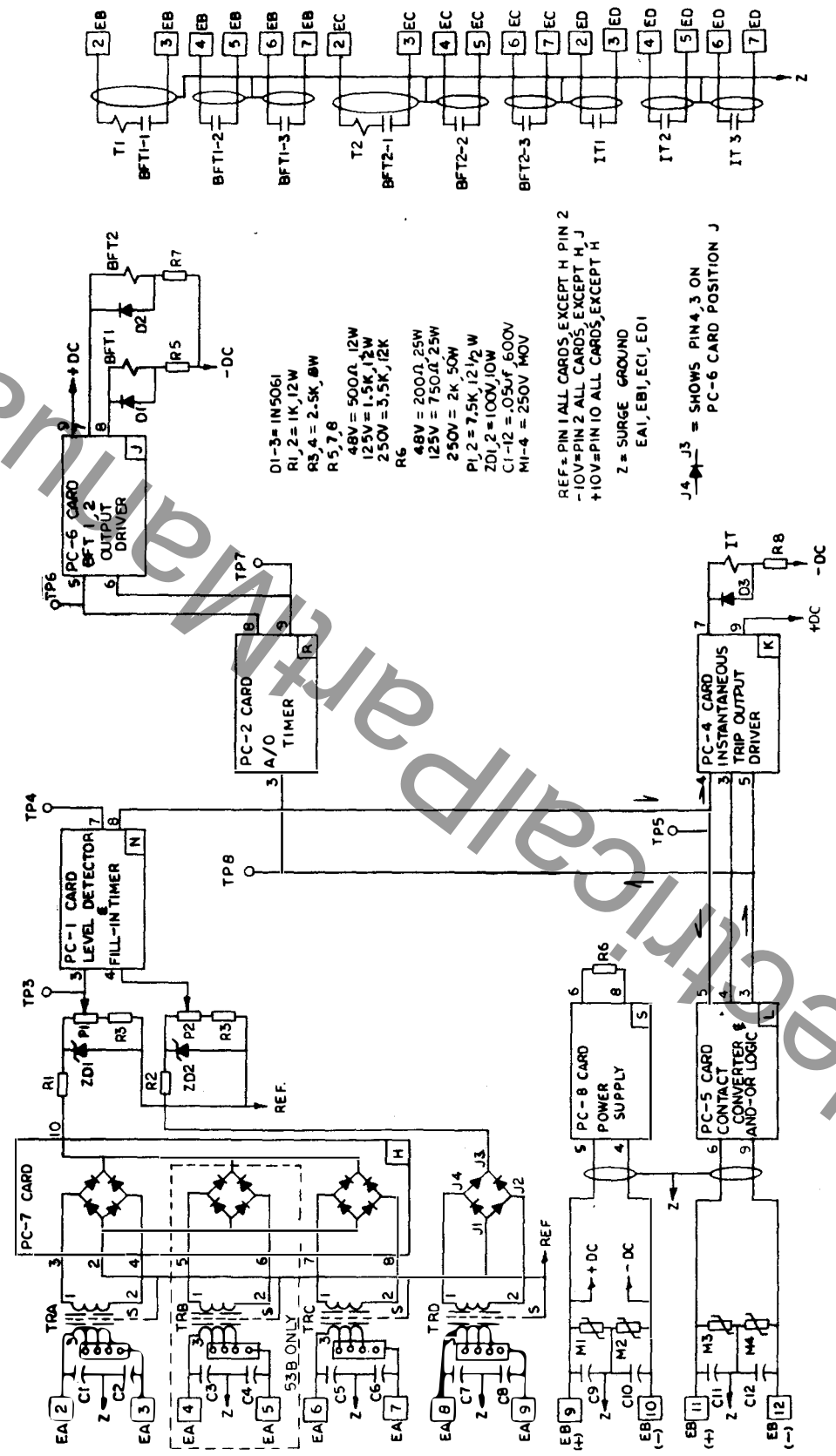


Fig. 5 (0108B8992-0) Internal Connections SBC53B

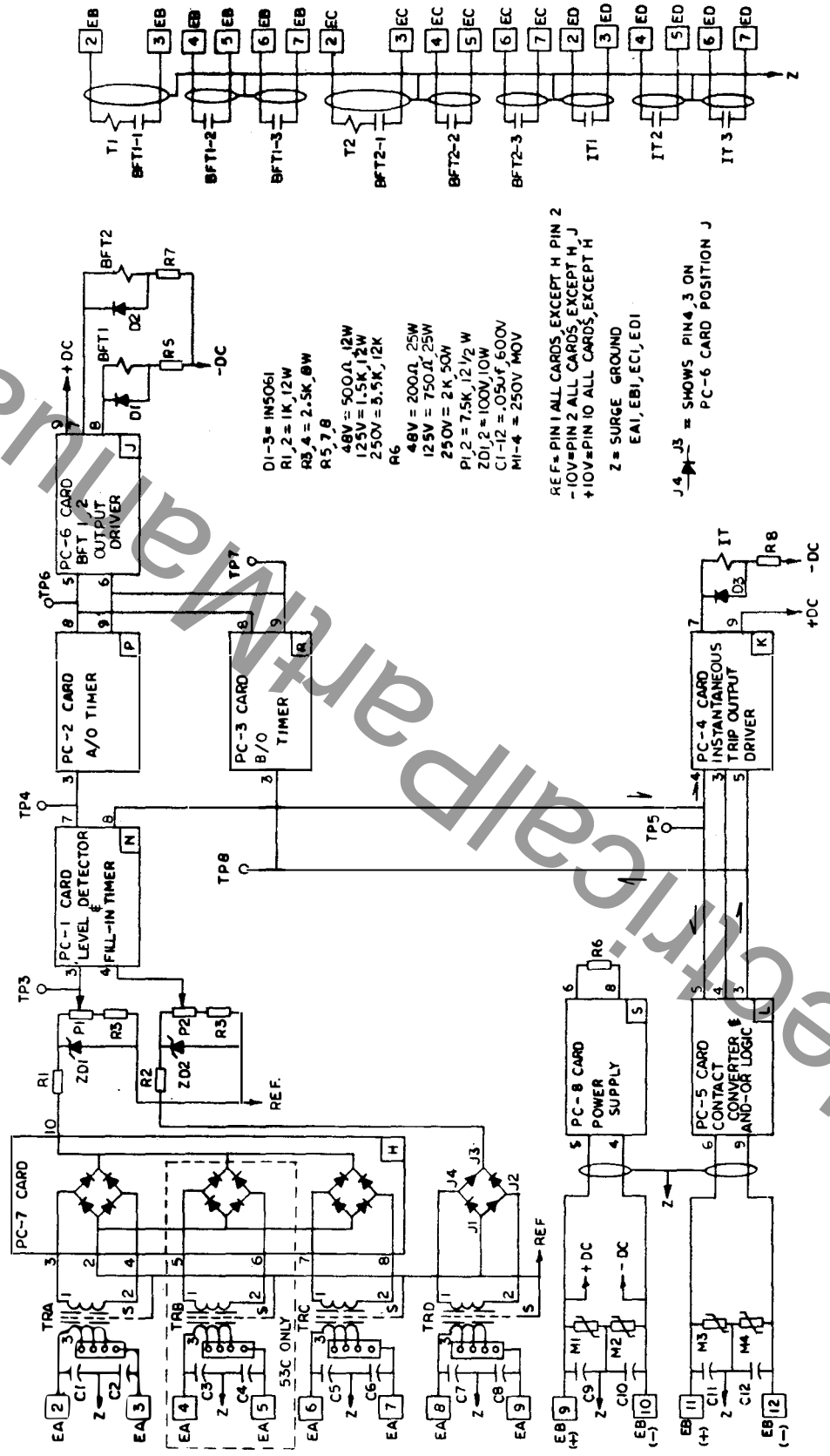


Fig. 6 (0108B8993-0) Internal Connections SBC53C

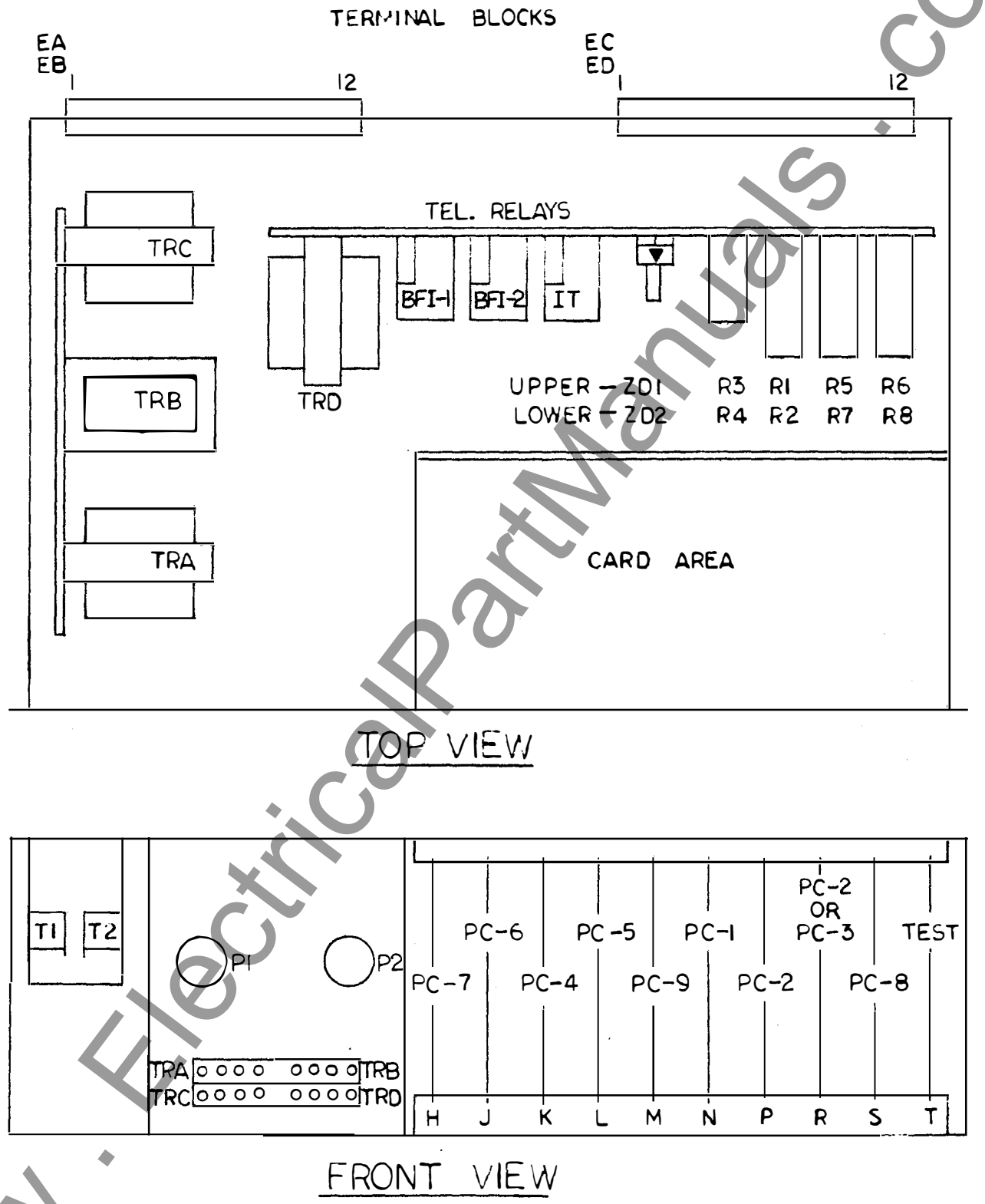


Fig. 7 (0275A1349-0) Component Location Diagram

53A	53B	53C	Card Nomenclature
N	N	N	PC-1
P	R	P	PC-2
-	-	R	PC-3
K	K	K	PC-4
-	L	L	PC-5
J	J	J	PC-6
H	H	H	PC-7
S	S	S	PC-8
T	T	T	Test

Fig. 8 Card Index

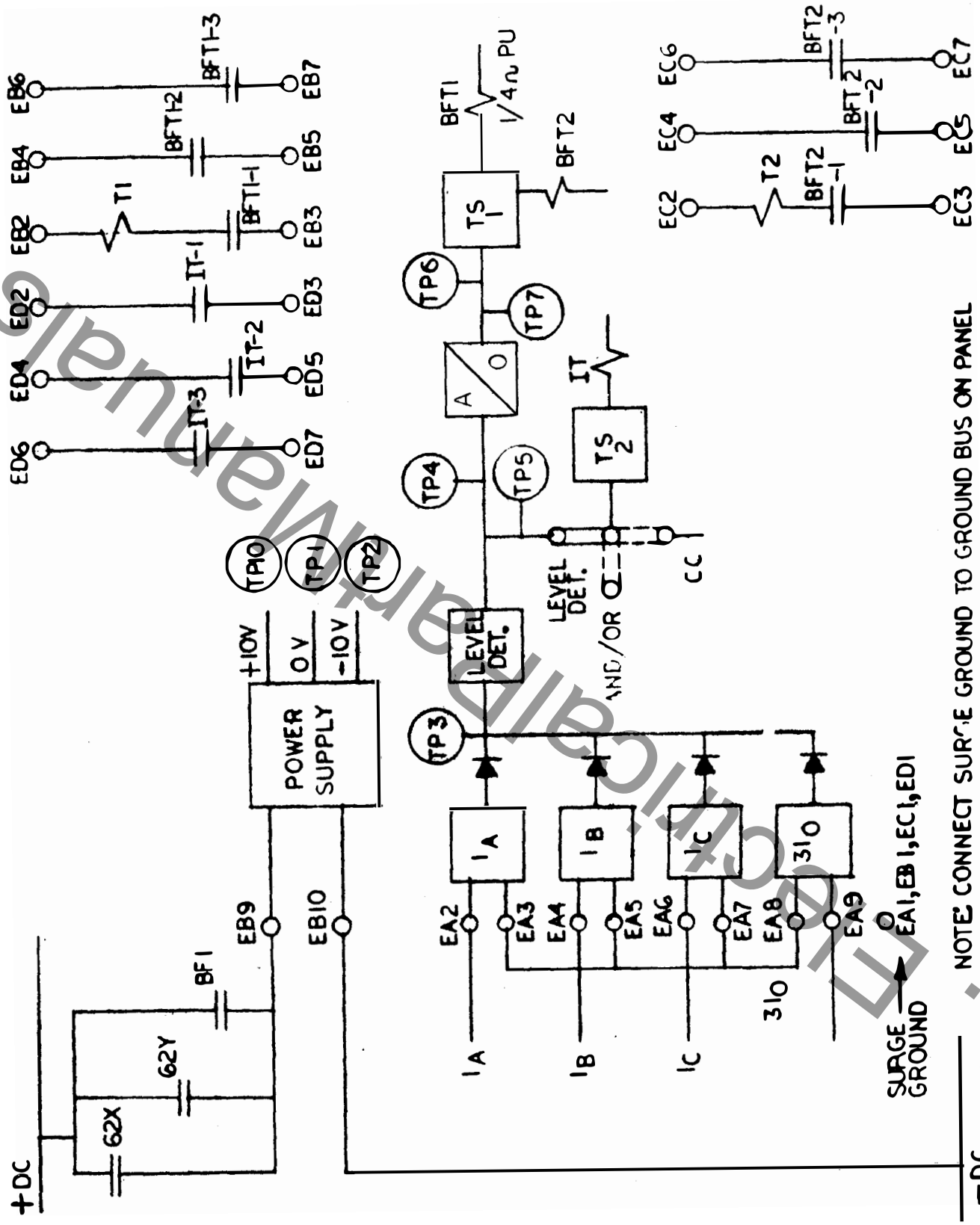


Fig. 9 (0273A9151-0) External Connections SBC53A

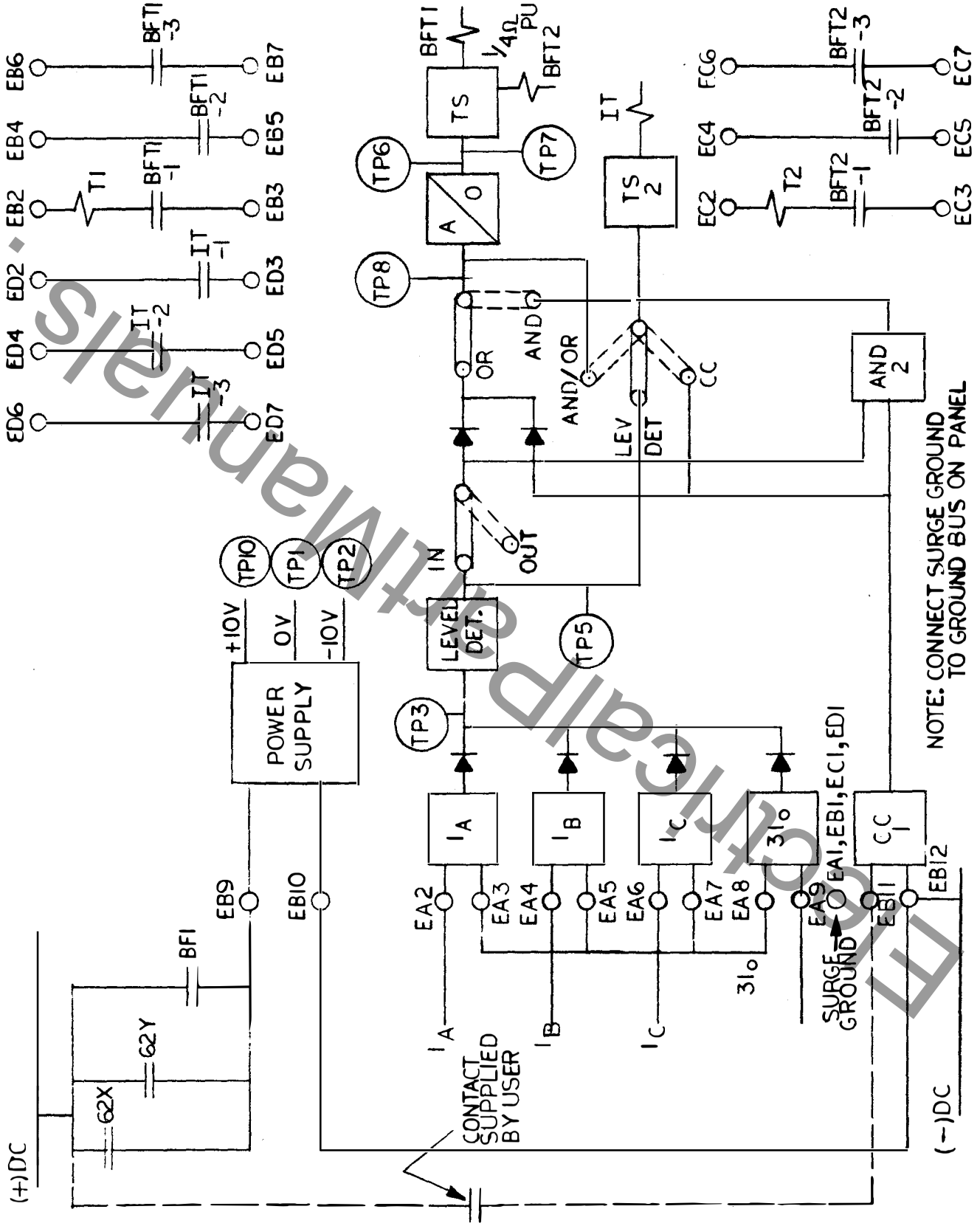


Fig. 10 (0273A9152-0) External Connections SBC53B

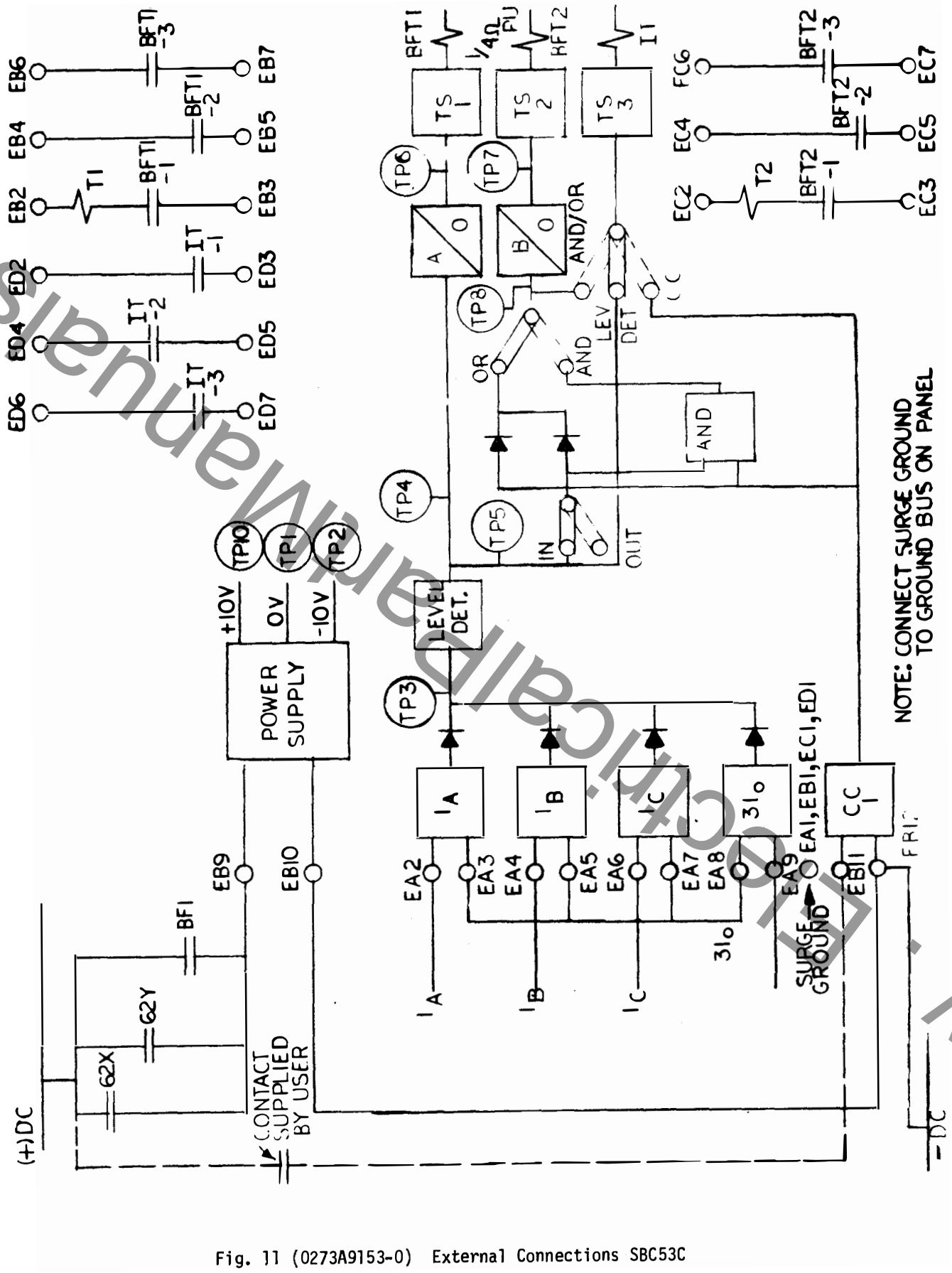


Fig. 11 (0273A9153-0) External Connections SBC53C

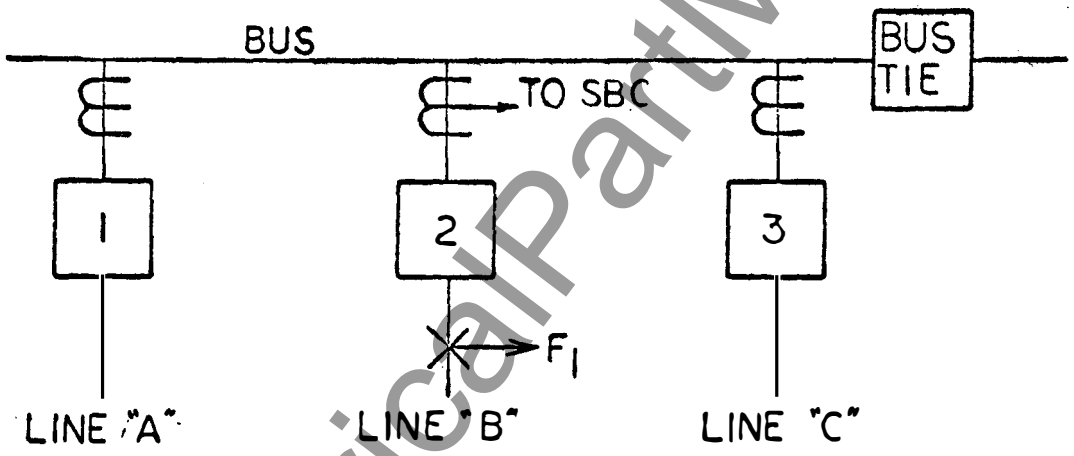


Fig. 12 (0246A2279-1) Relay Application, Single Breaker

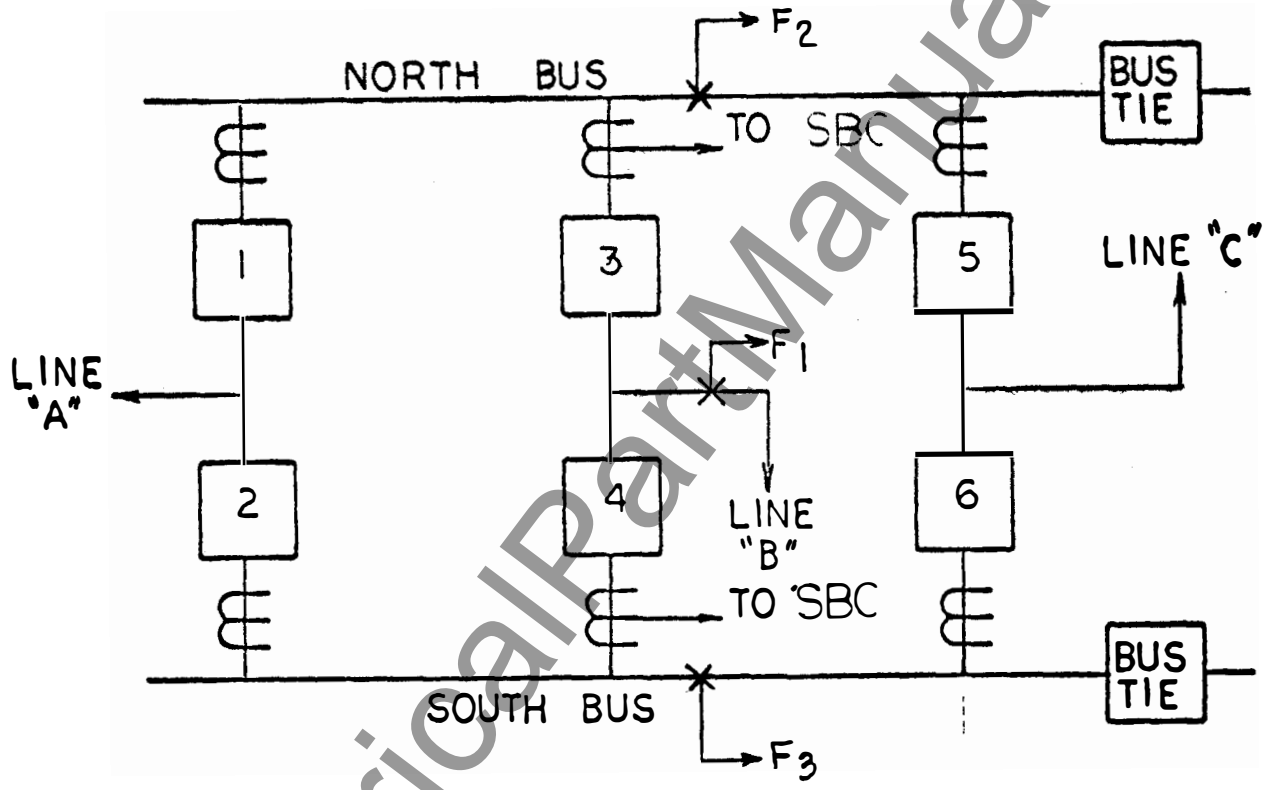


Fig. 13 (0246A2277-2) Relay Application, Double Bus, Double Breaker

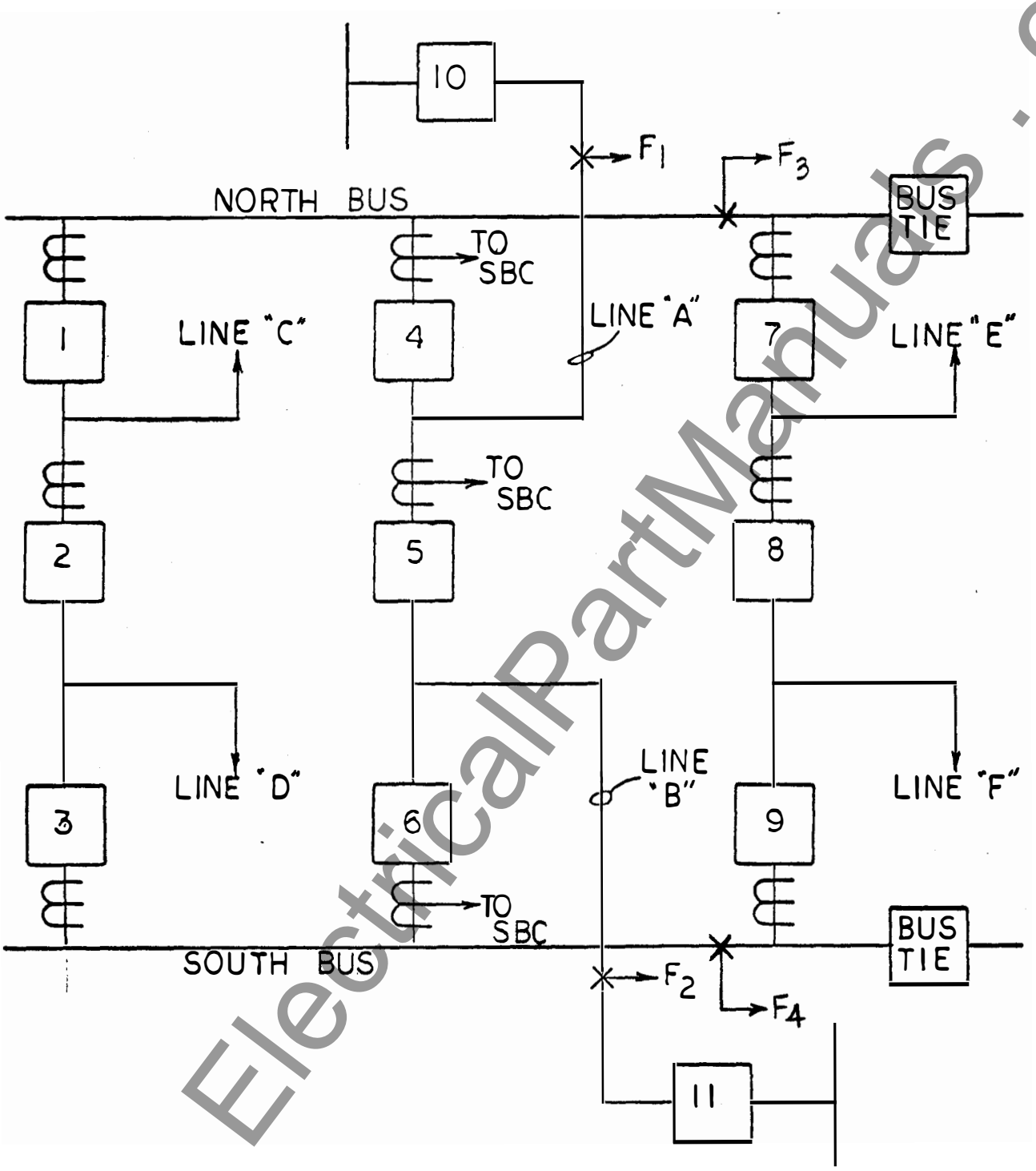


Fig. 14 (0246A2280-2) Relay Application, Breaker and a Half

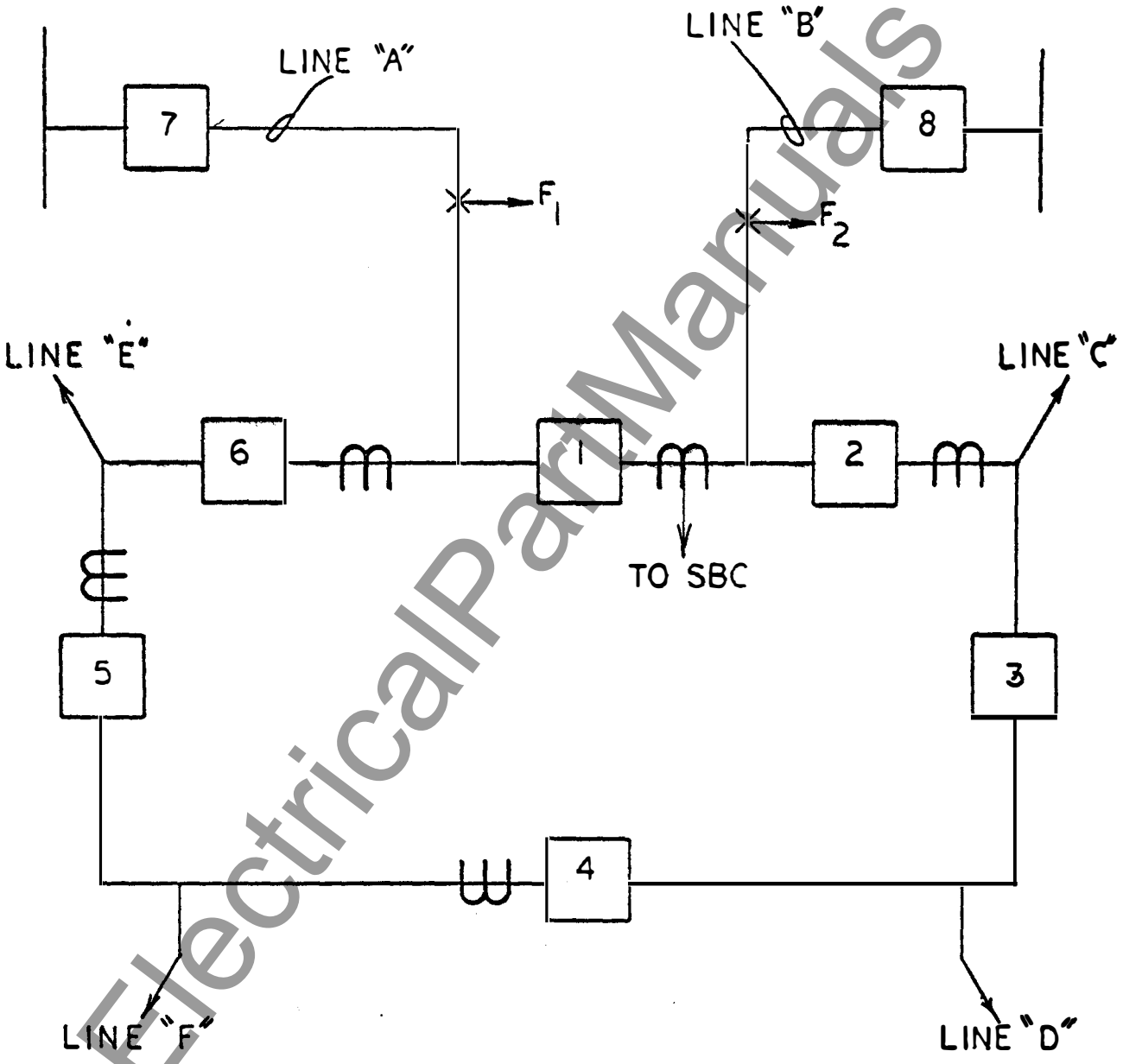


Fig. 15 (0246A2278-1) Relay Application, Ring Bus

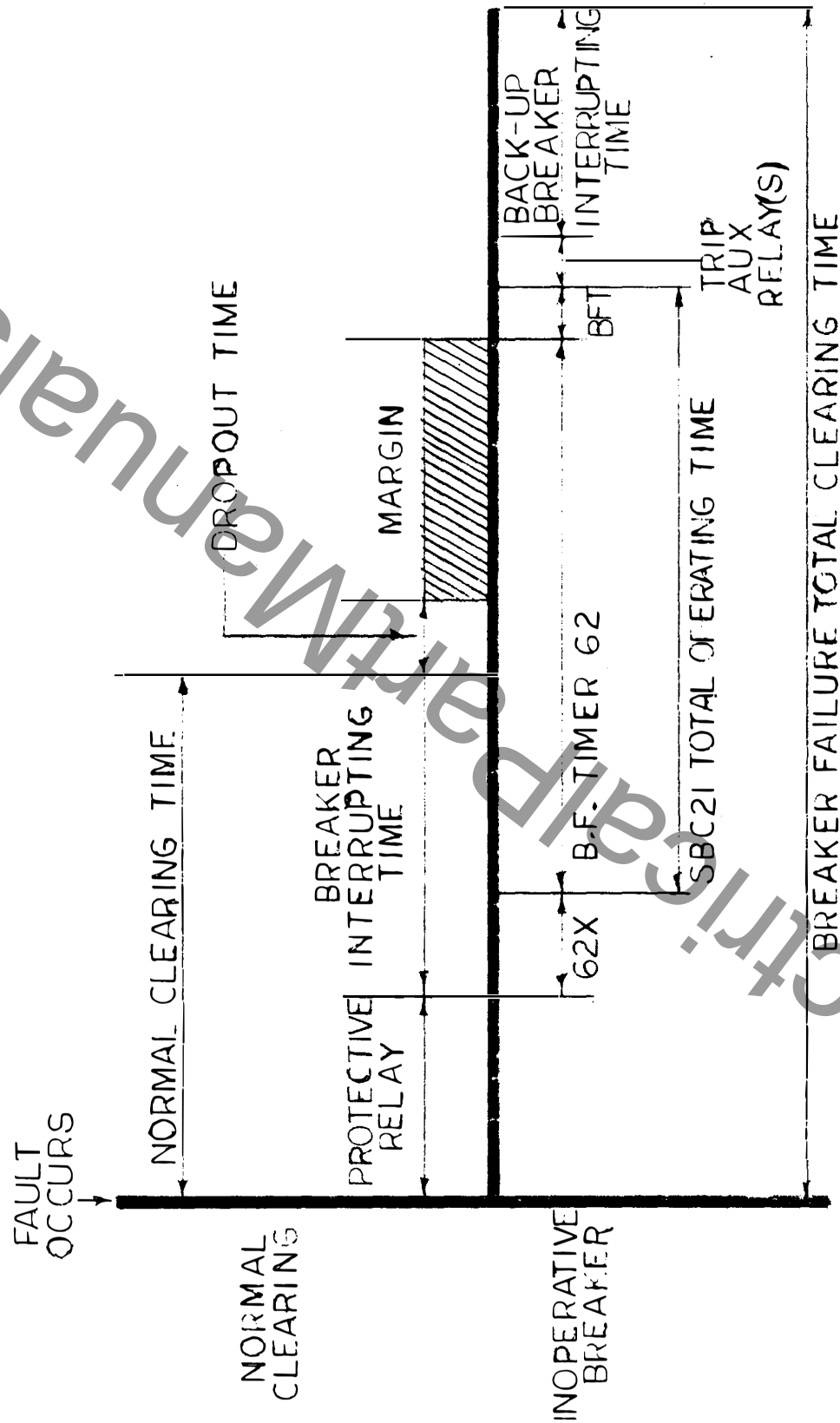


Fig. 16 (0227A7128-1) Breaker Failure Time Unit for the SBC Relay

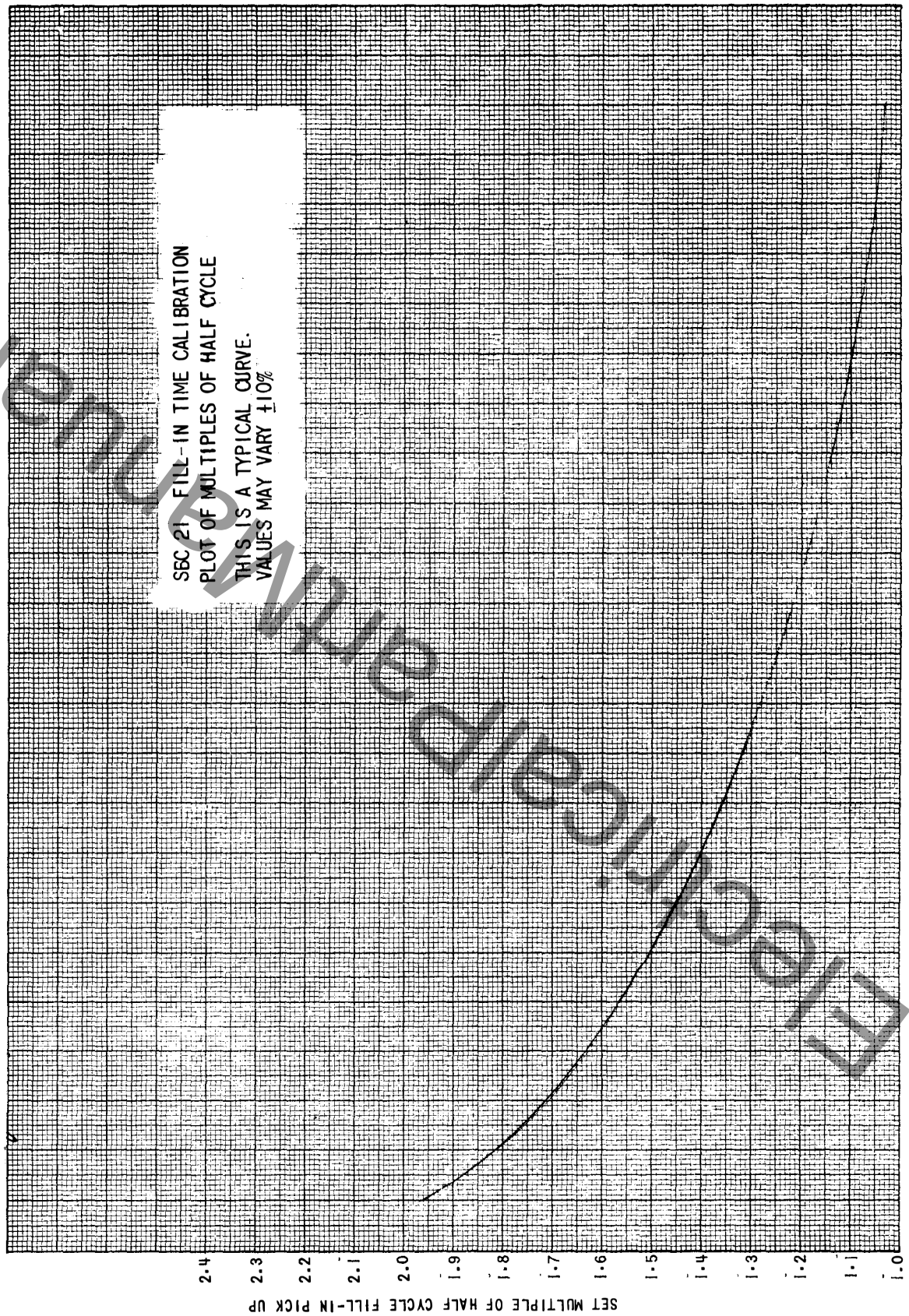


Fig. 17 (0246A2206-1 Sh. 1) Fill-in Time Calibration Graph for the SBC Relay

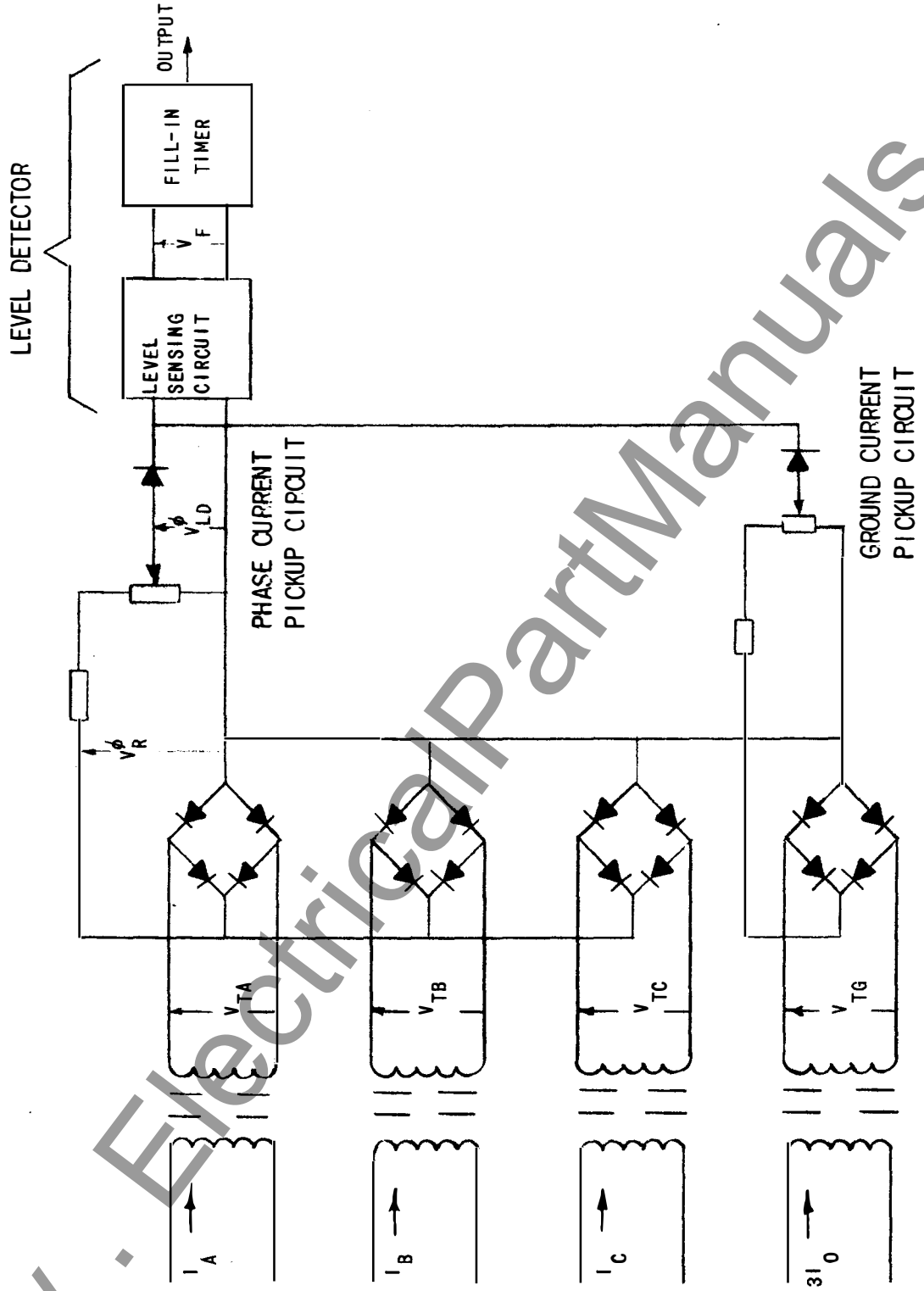


Fig. 18 (0246A2272-0) Current Detector Circuit for the SBC Relay

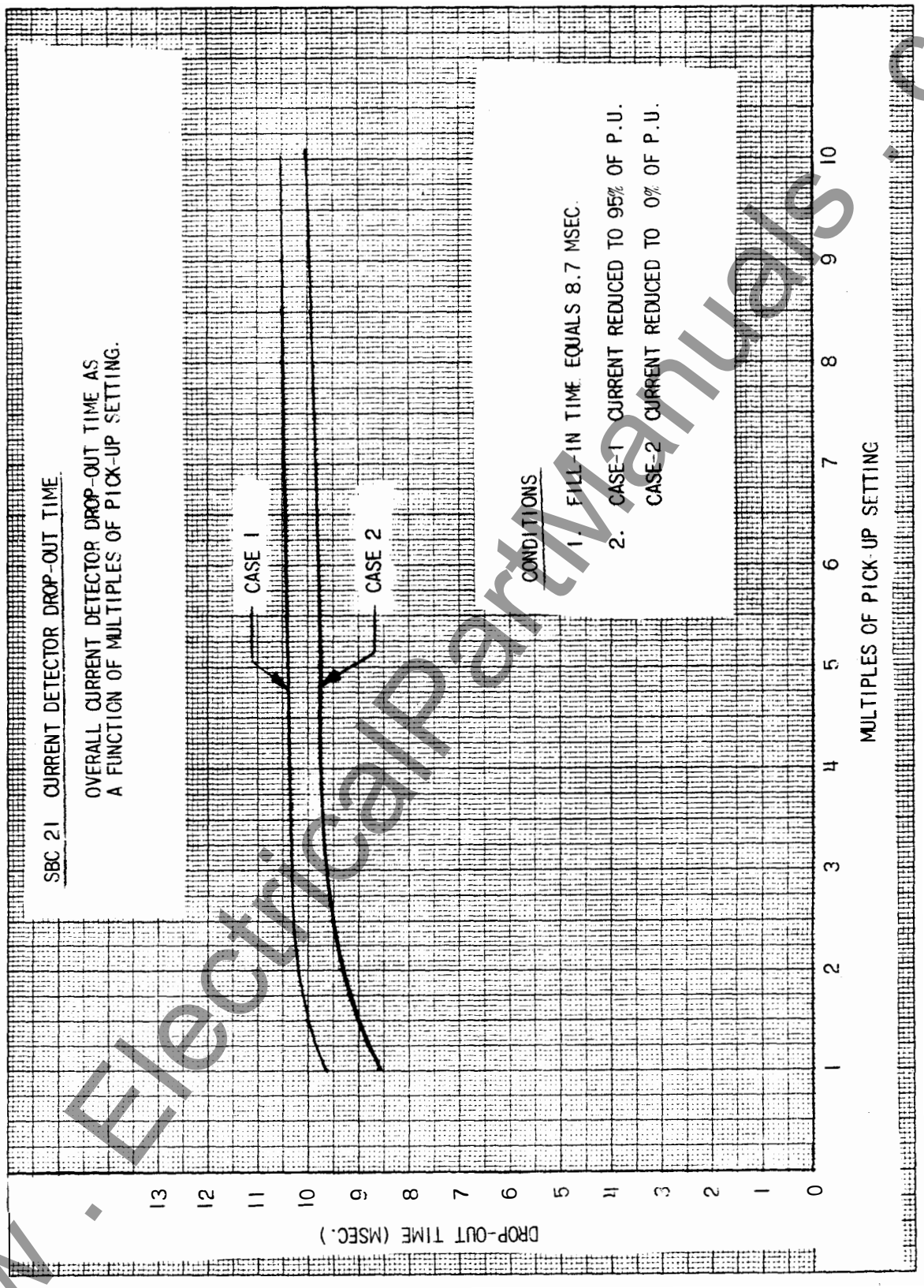


Fig. 19 (0246A2206-1, Sh. 4) Current Detector Drop-out Time Graph for the SBC Relay

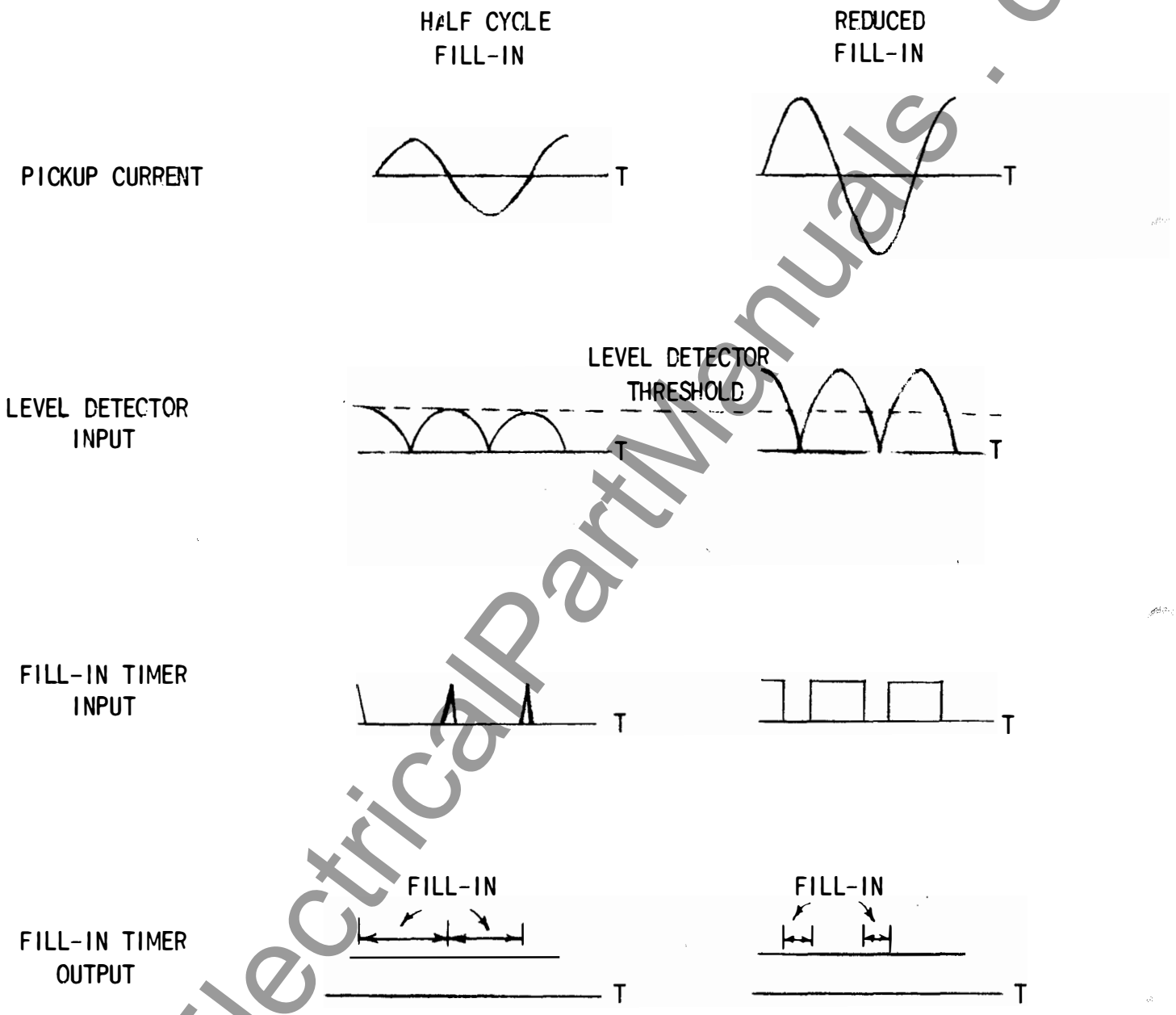


Fig. 20 (0246A2273-0) Current Detector Pickup Current for Reduced Fill-in Times for the SBC Relay

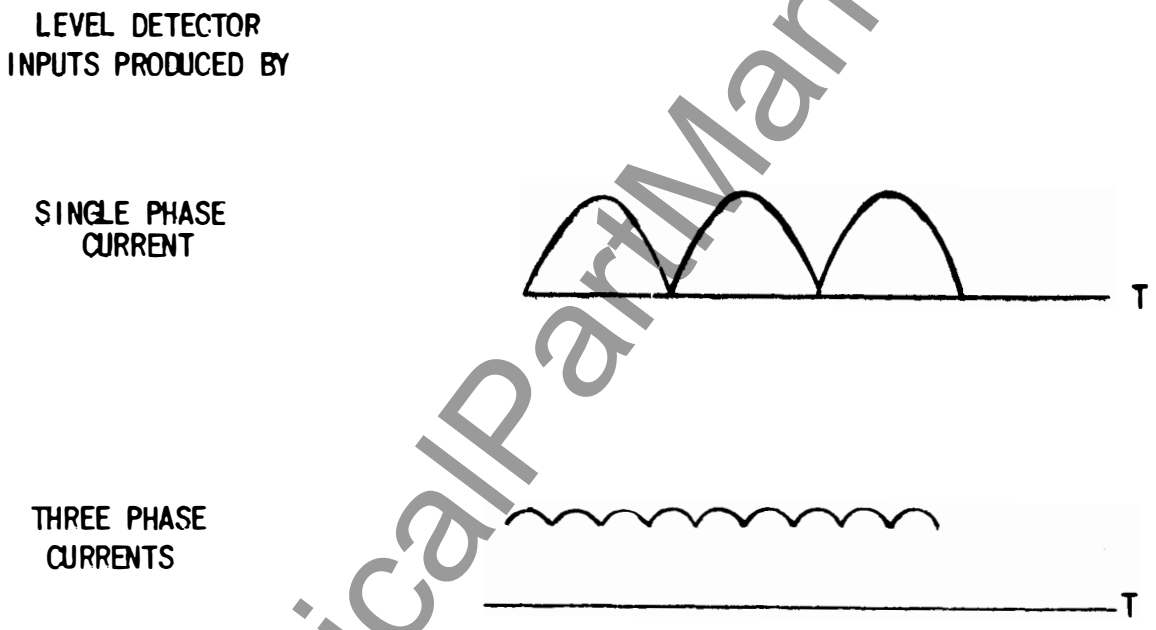


Fig. 21 (0246A2274-0) Current Lead Detector Inputs Produced by Single Phase and Three Phase Currents

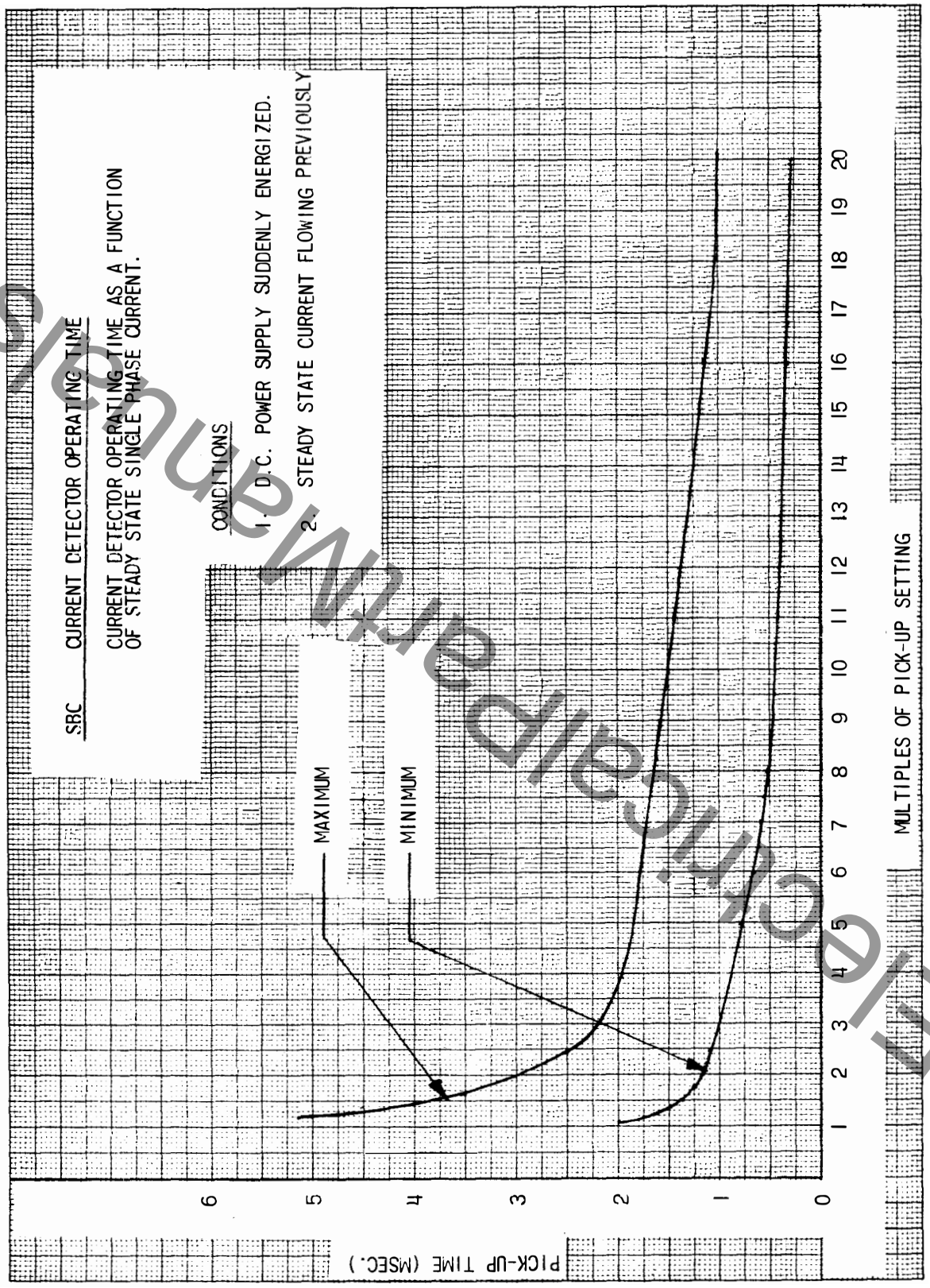


Fig. 22 (0246A2206-1, Sh. 3) Current Detector Operating Time for the SBC Relay

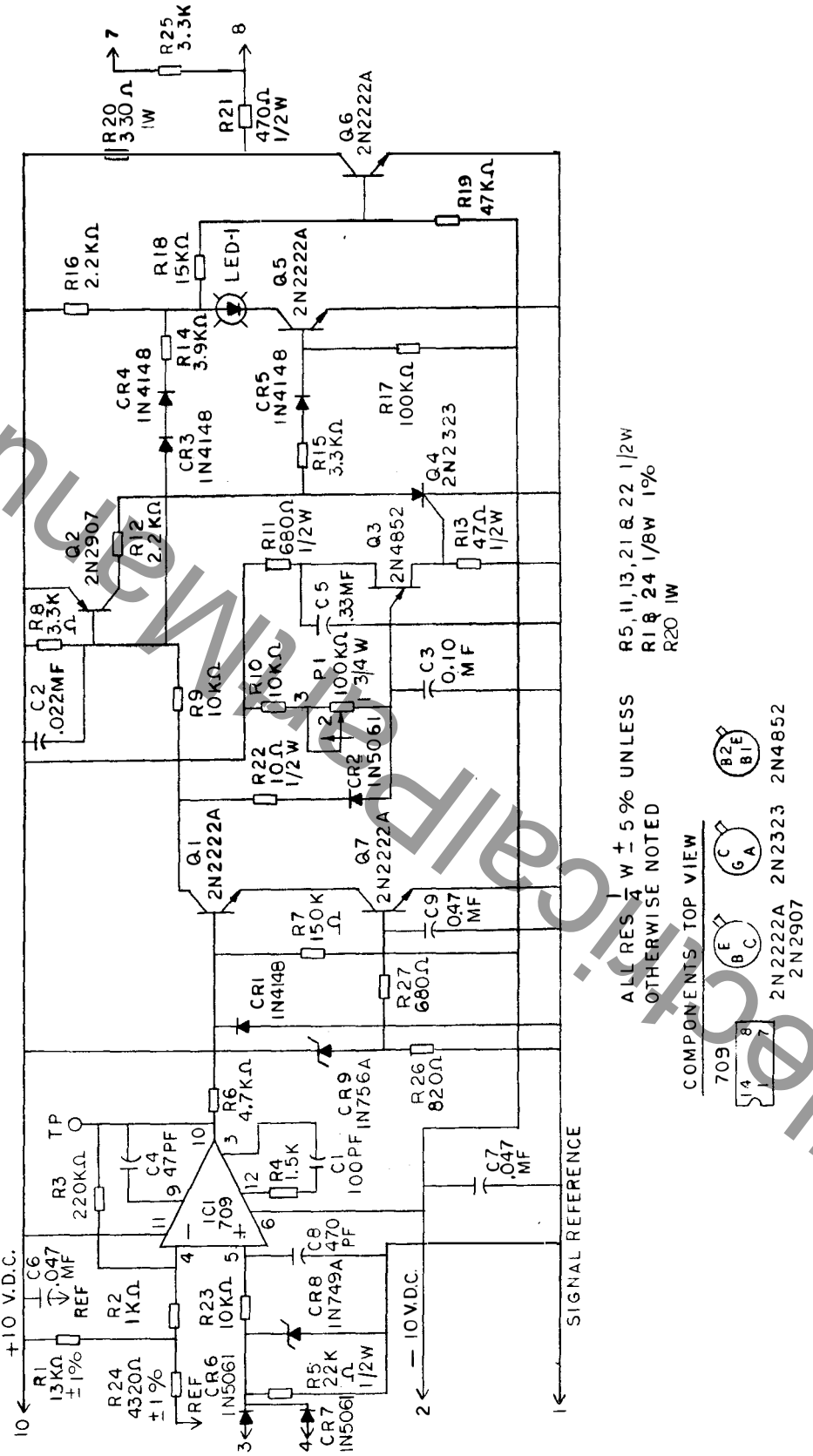


Fig. 23 (0184B5702-1) Level Detector (PC-1)

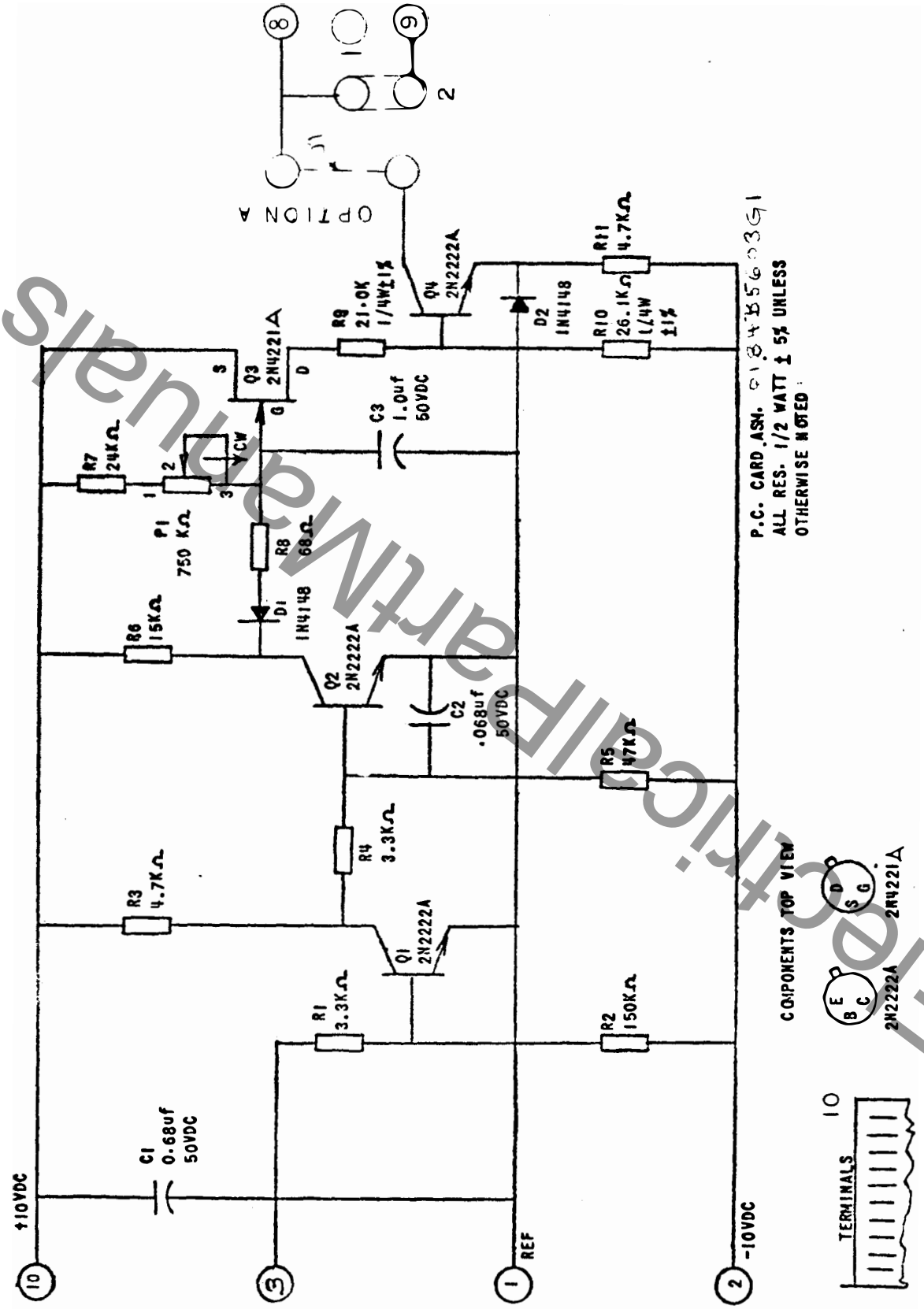


Fig. 24 (0184B5703-1) A/O Timer (PC-2)

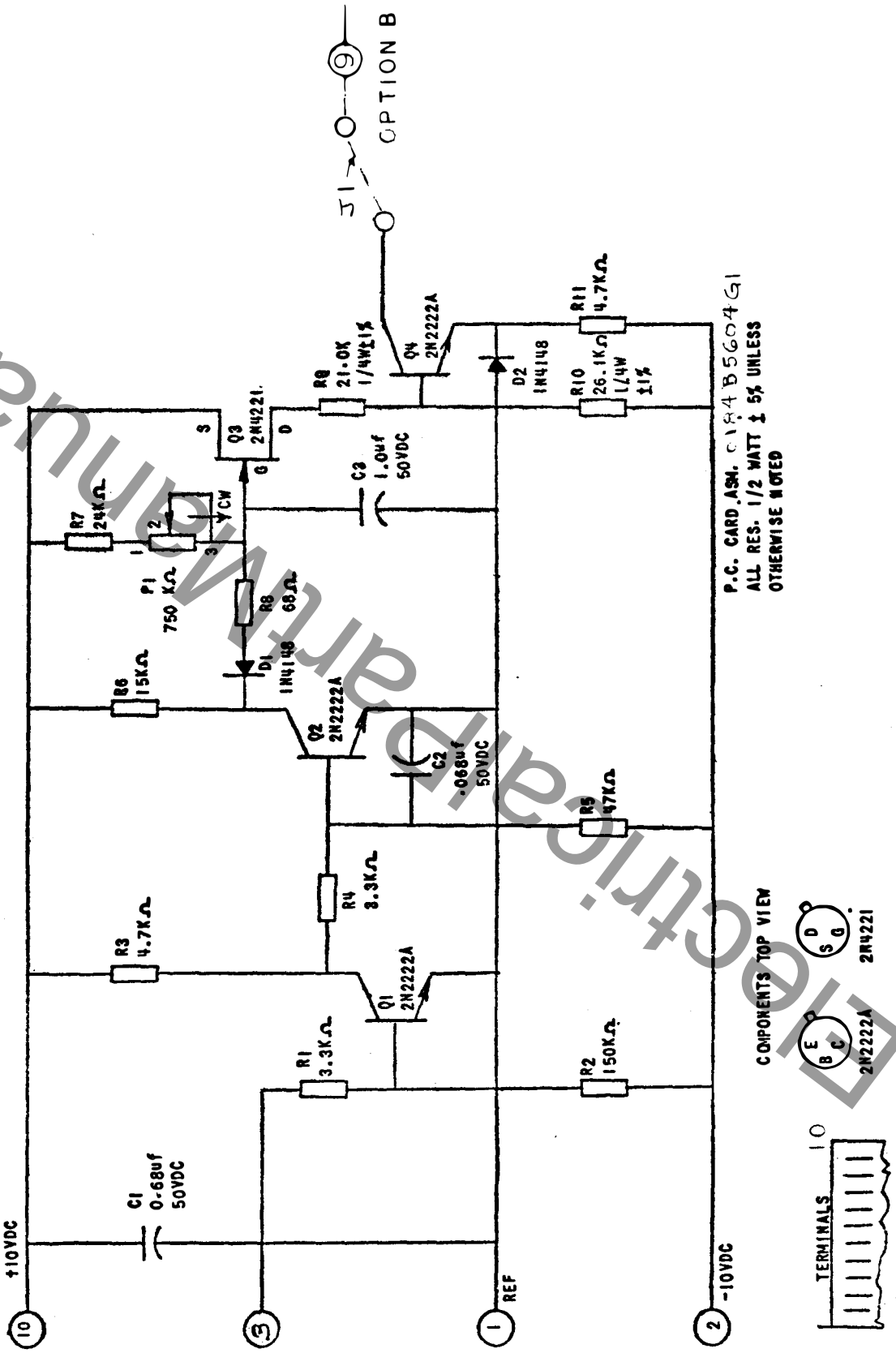


Fig. 25 (0184B5704-1) B/O Timer (PC-3)

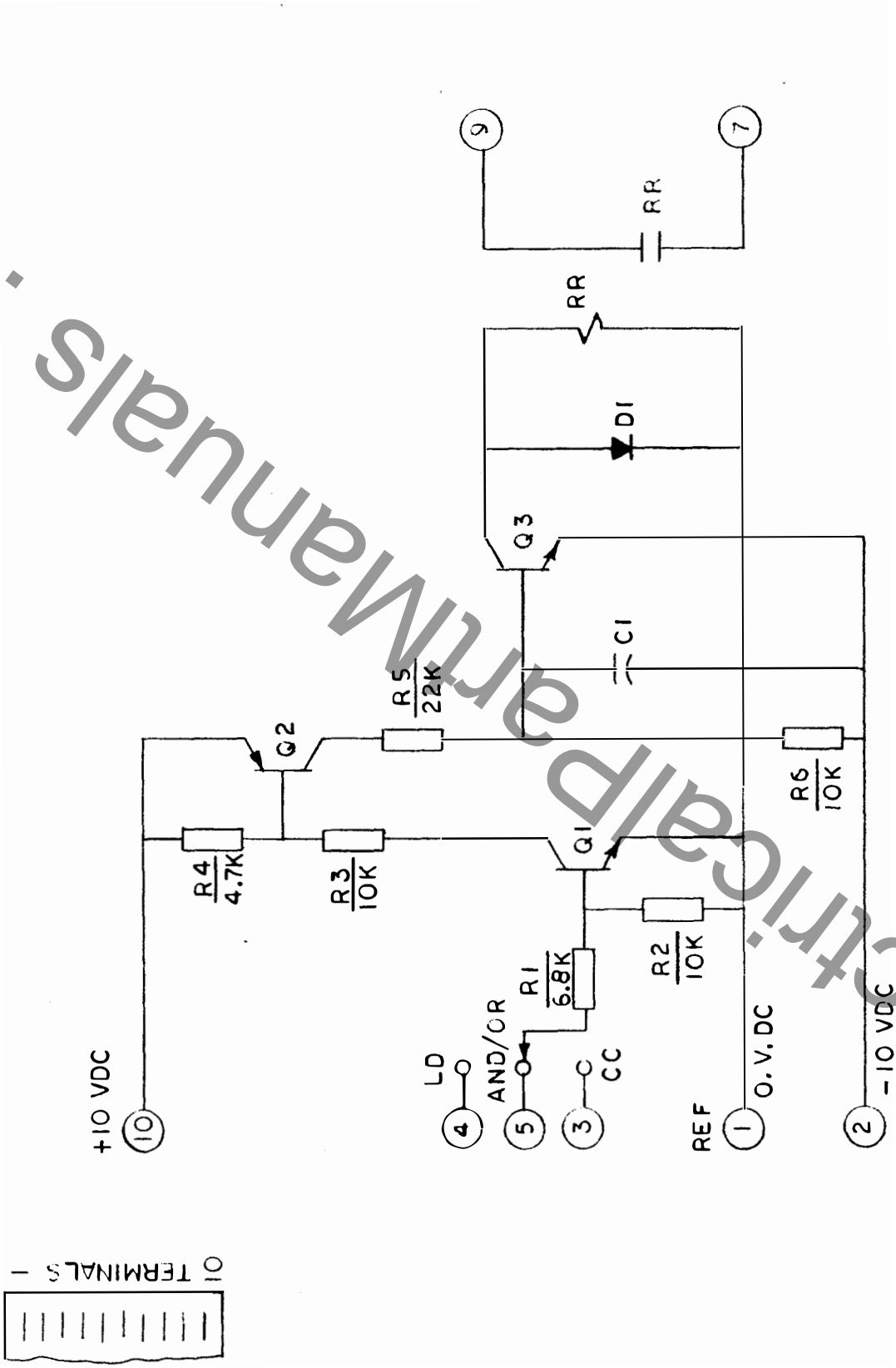


Fig. 26 (0269A3094-0) Instantaneous Trip (PC-4)

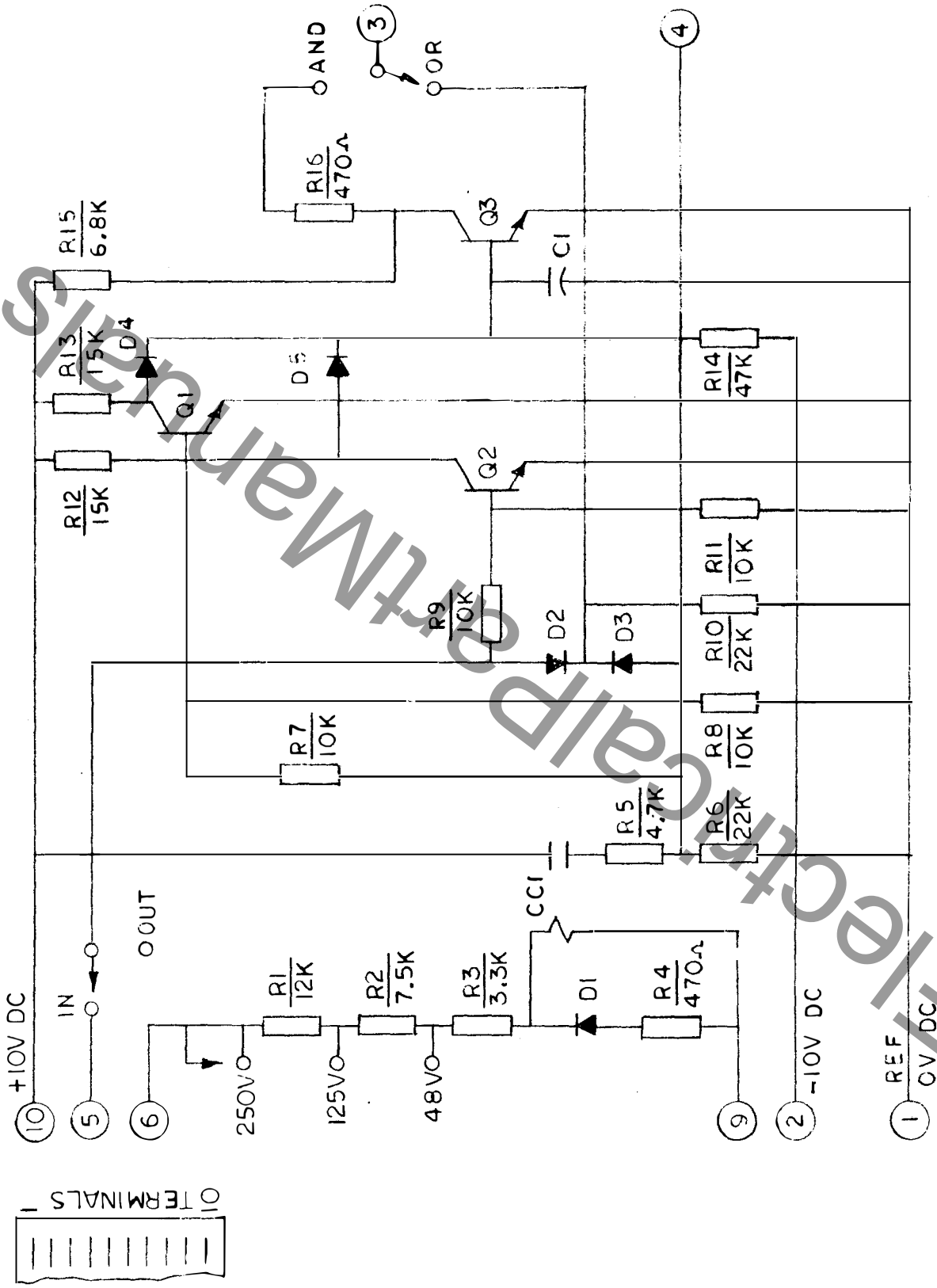


Fig. 27 (0269A3095-0) Contact Converter, Logic Gates (PC-5)

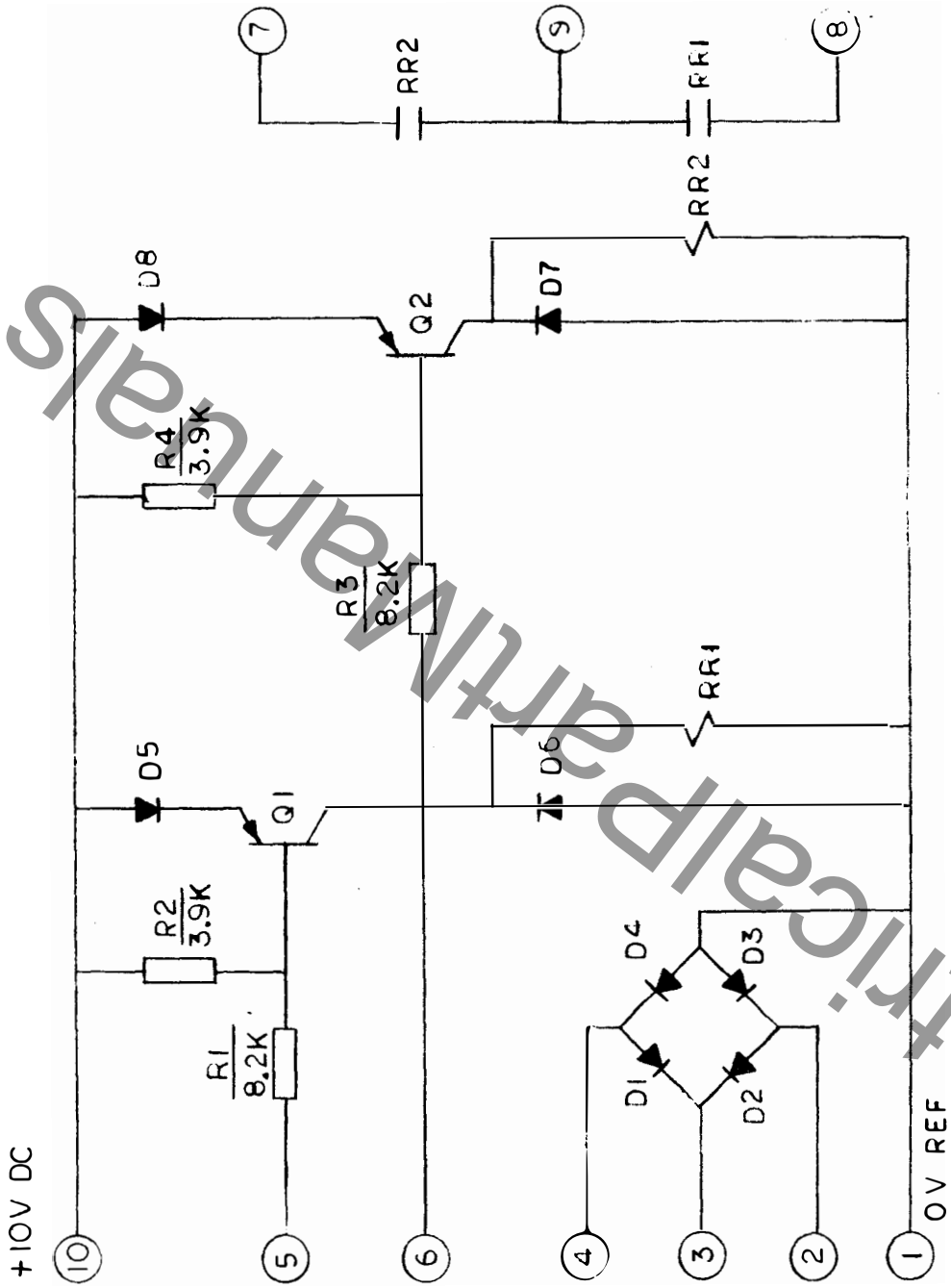


Fig. 28 (0269A3096-0) Output Reed Switch, $3I_0$ Bridge PC-6

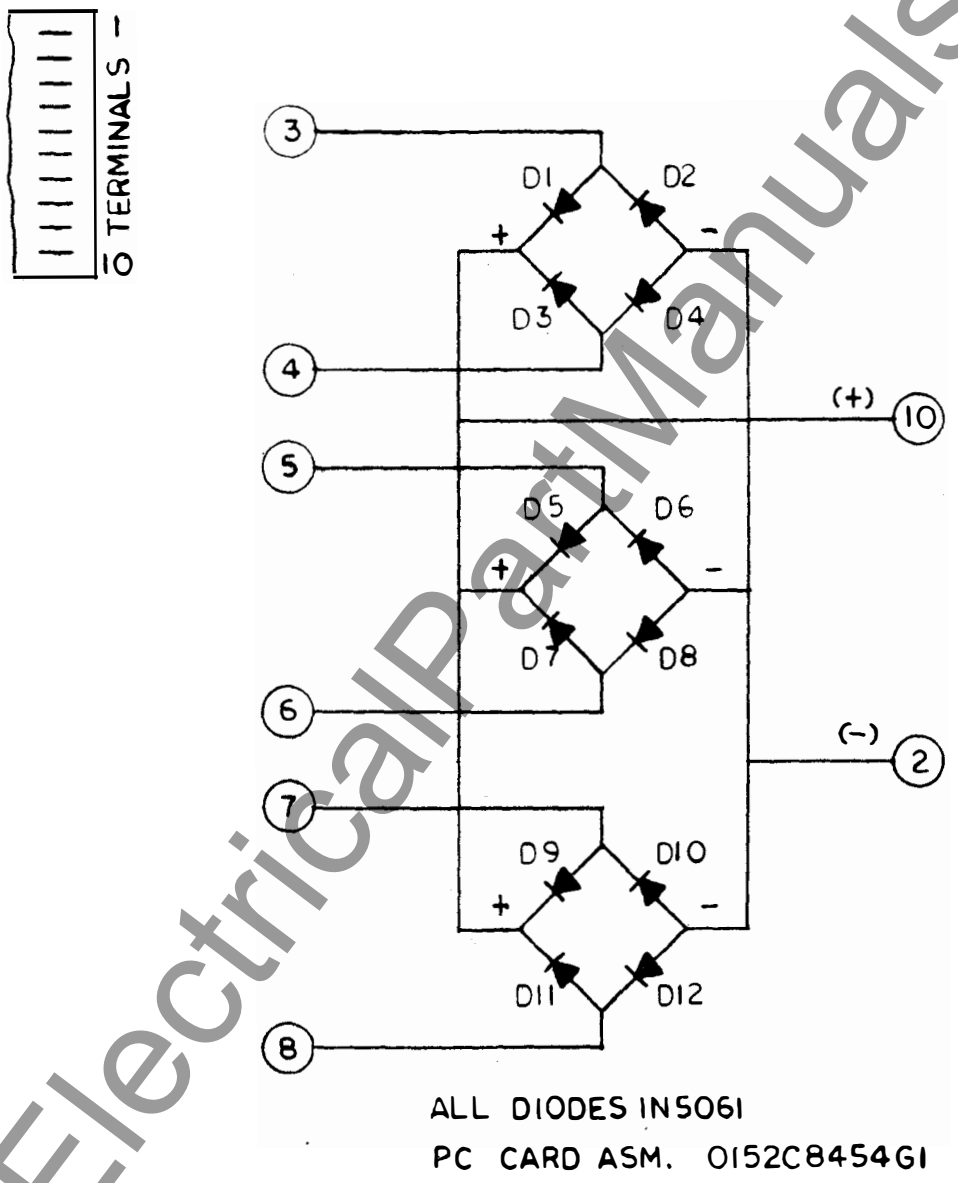
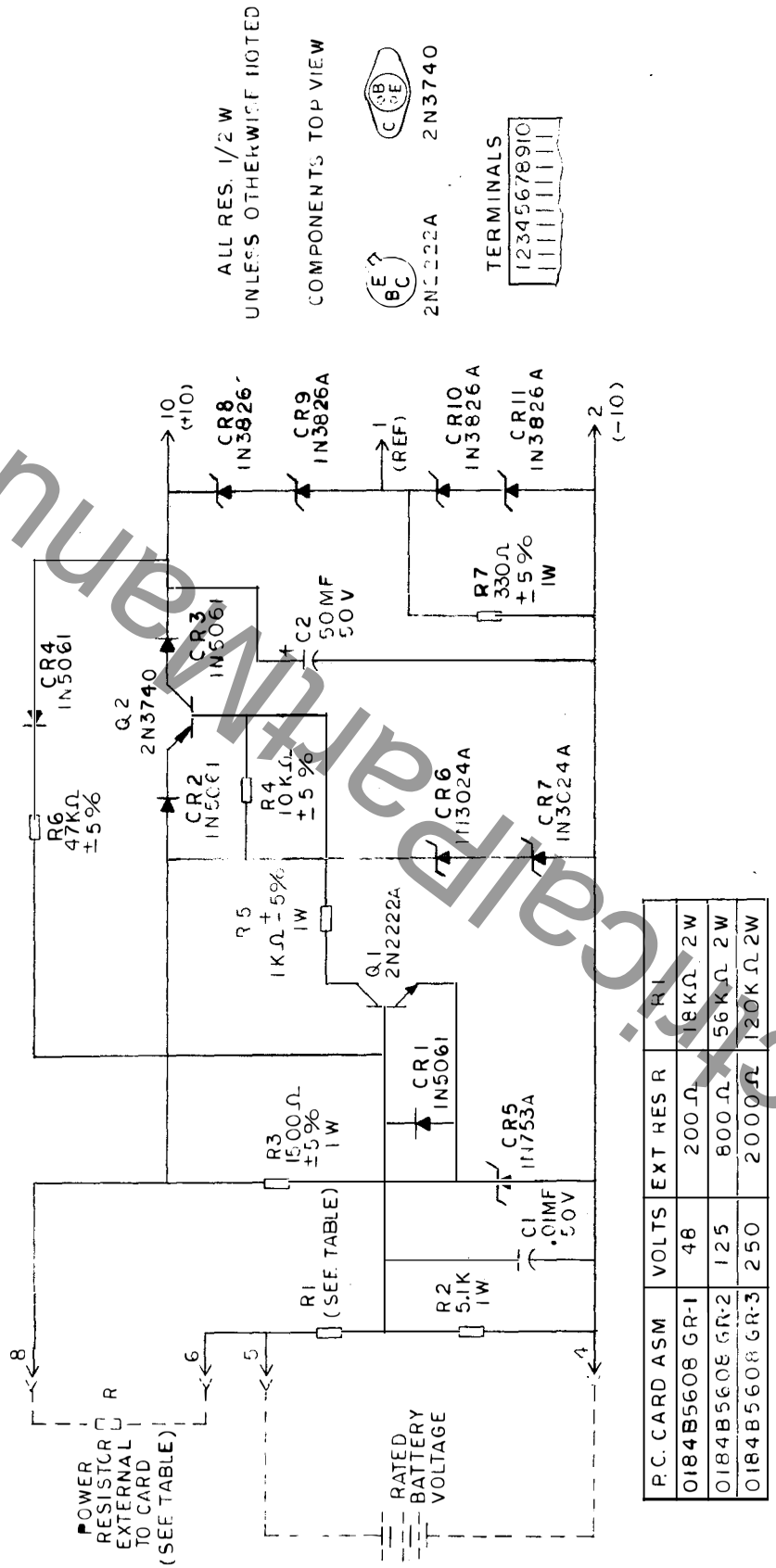
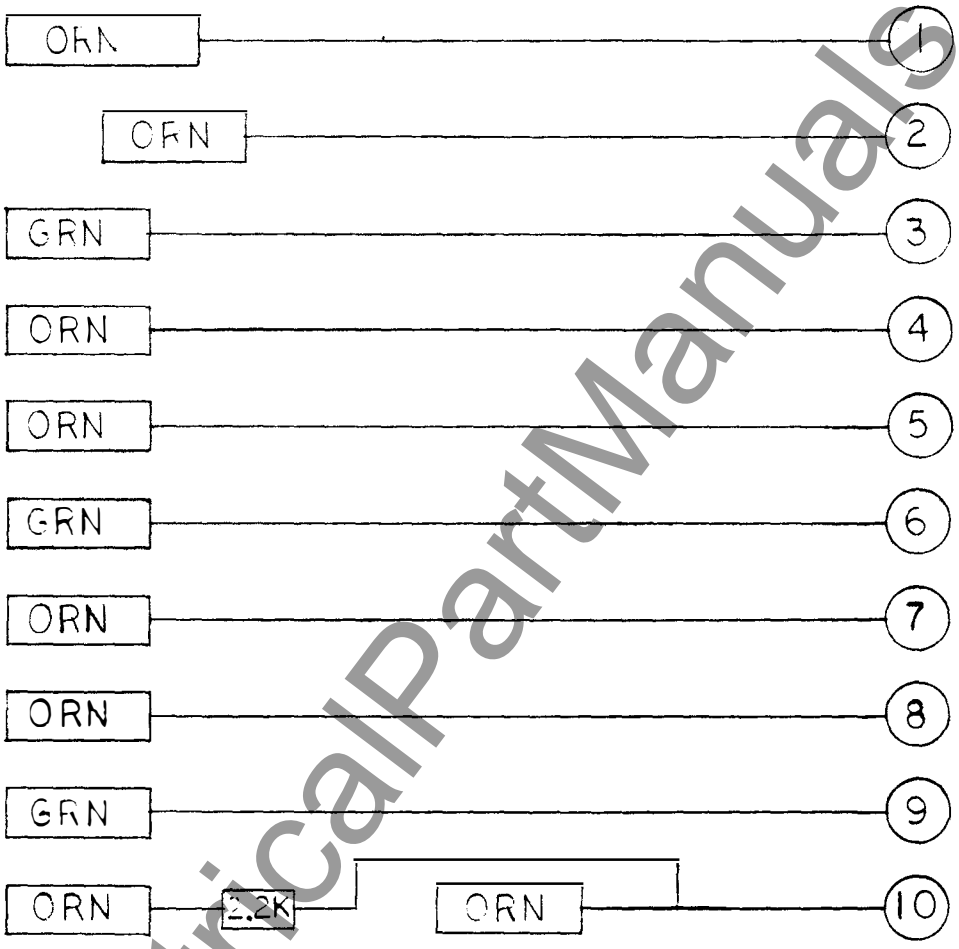


Fig. 29 (0269A3097-0) Phase Diode Bridges, PC-7



P.C. CARD ASM	VOLTS	EXT RES R	R1
0184B5608 GR-1	48	200 Ω	18KΩ 2W
0184B5608 GR-2	125	800 Ω	56KΩ 2W
0184B5608 GR-3	250	2000Ω	120KΩ 2W

Fig. 30 (0184B5708-1) Power Supply, PC-8



TEST CARD ASSEMBLY 0149C7259 G-3

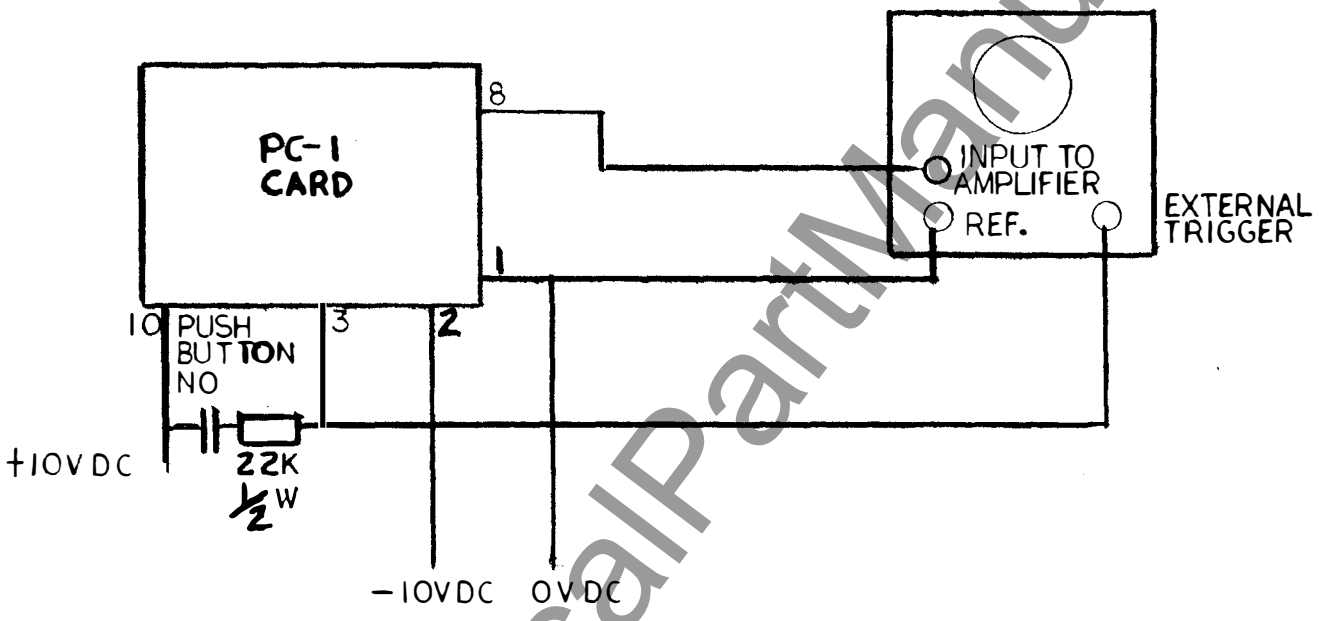
Fig. 31 (0273A9188-0) Test Card, T

INSTRUCTIONS:

1.- APPLY 10V DC TO TERMINALS 10(+) AND 1(-). APPLY -10V DC TO TERMINALS 2(-) AND 10(+)

2.- CONNECT OSCILLOSCOPE AND CONTACT CIRCUITS AS SHOWN BELOW.

3.- BE SURE SCOPE POWER CORD IS UNGROUNDED.



TIMING PROCEDURE

PLACE THE SCOPE IN A NEGATIVE SLOPE EXTERNAL TRIGGERING MODE.

DEPRESS THE N.O. CONTACT AND NOTE THAT UPON RELEASING THE CONTACT THE SCOPE TRACE INITIATES.

FROM FACTORY CALIBRATION, A POSITIVE SIGNAL AT TERMINAL 8 SHOULD GO NEGATIVE IN 8.5-9 MILLISECONDS AFTER TRACE INITIATION.

TO ALTER OR READJUST THIS SETTING TURN THE POT. ON THE CARD CW TO INCREASE FILL-IN TIME OR CCW TO DECREASE THE TIME.

Fig. 32 (0273A9189-0) SBC Test Circuit for Fill-in Timer

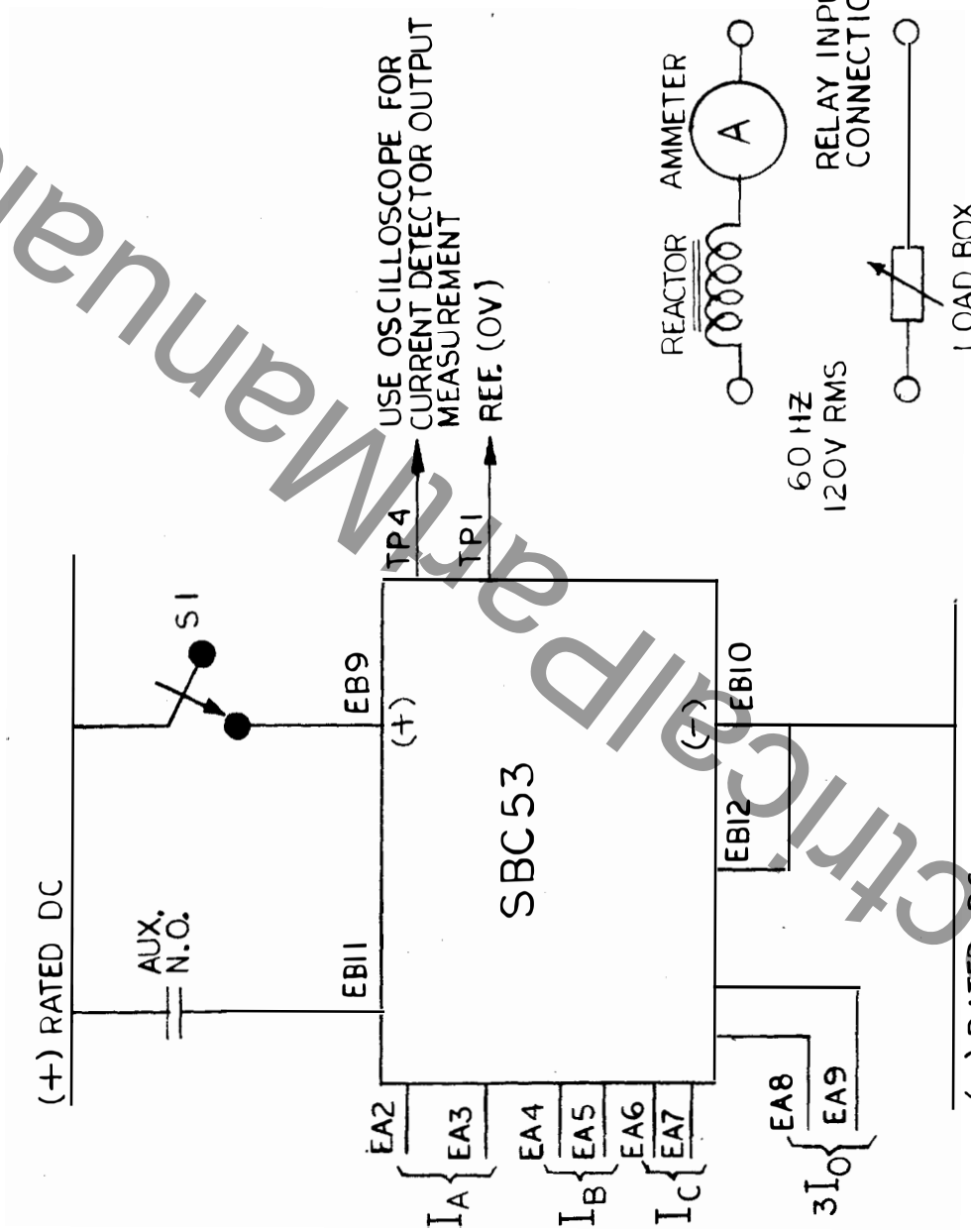


Fig. 33 (0273A9190-0) SBC Test Circuit for Current Detector

CAUTION: REMOVE EXTERNAL CONNECTIONS FROM EB2, EB3 BEFORE TESTING.

a.) SET AMMETER CURRENT (A) TO 5X PICKUP CURRENT LEVEL.

b.) INITIATE TIMING SEQUENCE BY CLOSING THE BFI CONTACT.

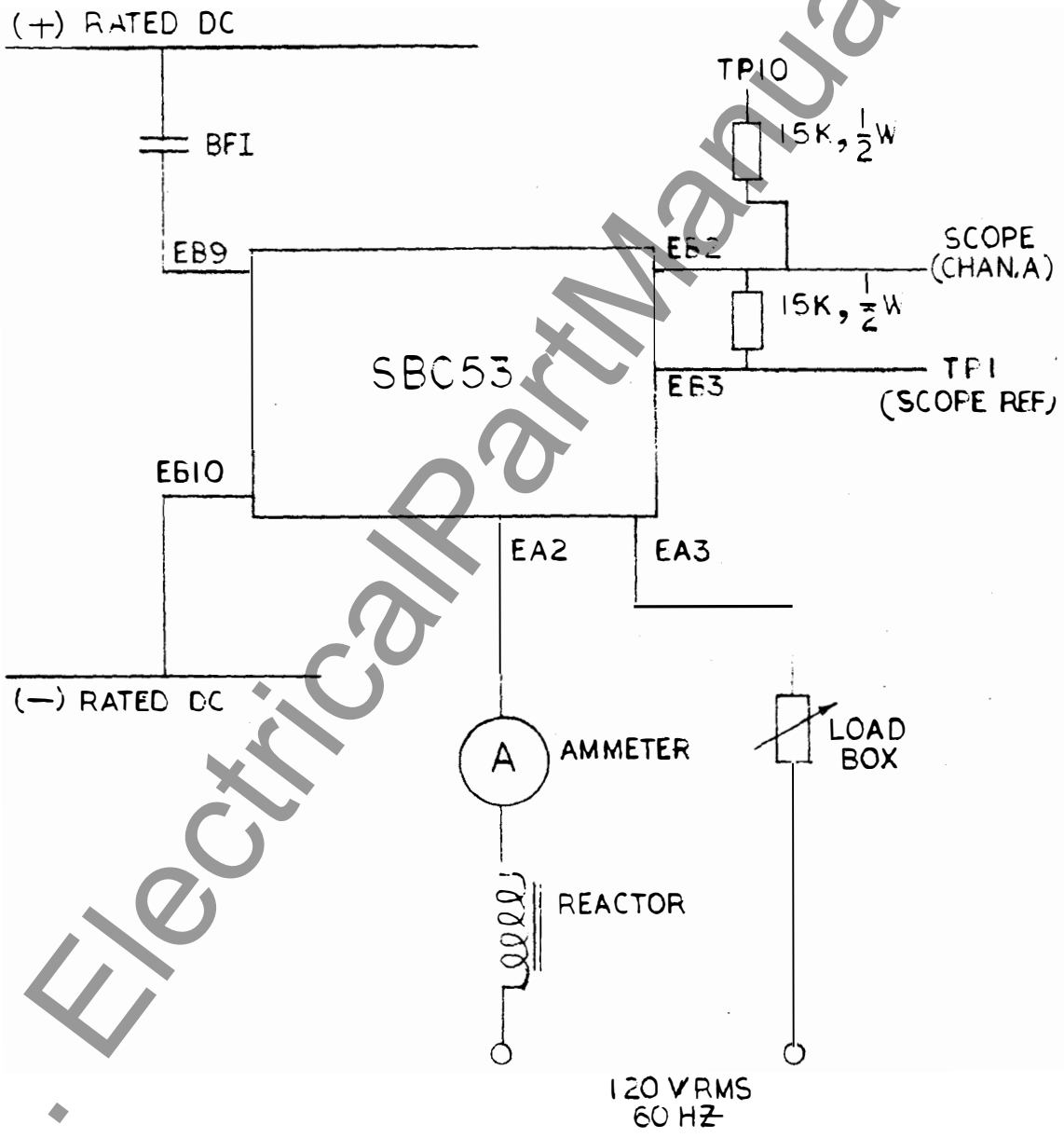


Fig. 34 (0273A9191-0) SBC Test Circuit for Overall Timer

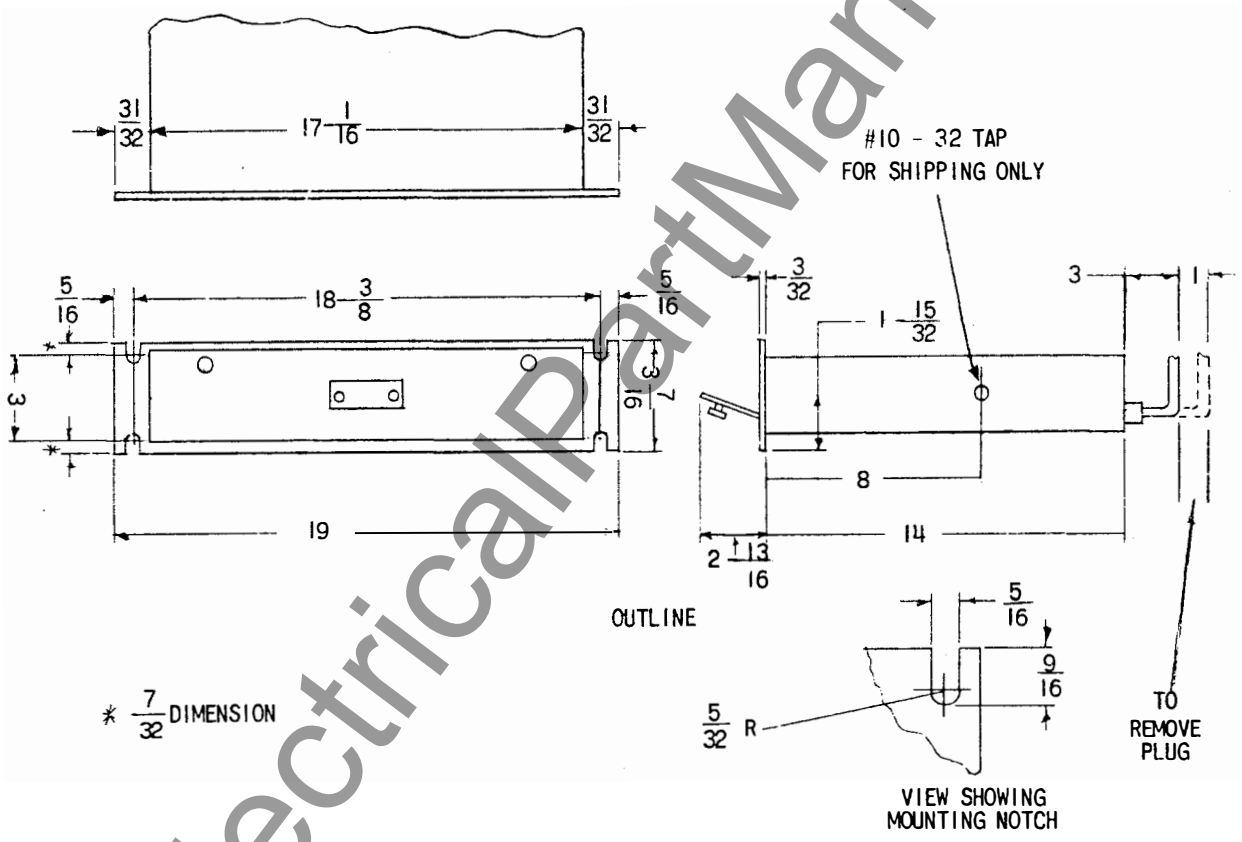


Fig. 35 (0227A2036-0) Outline & Mounting Dimensions

Meter and Control
Business Department

6-88

General Electric Company
205 Great Valley Parkway
Malvern, PA 19355