MICRO-PRODAC THYRISTOR INTERFACE (PTI) BOARD
S#1939A92G01

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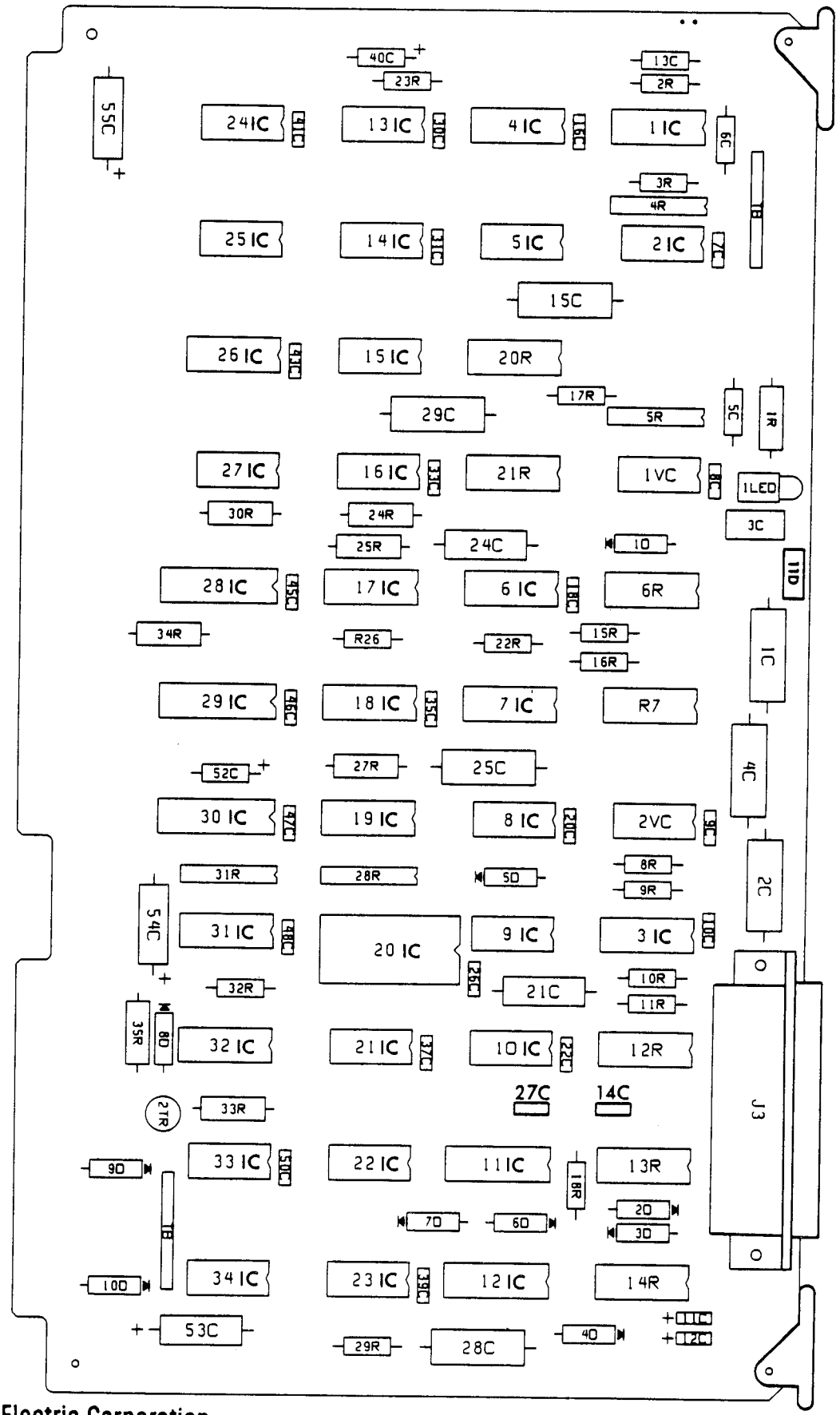

Westinghouse Electric Corporation

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1.0 INTRODUCTION

The MICRO-PRODAC Thyristor Interface (PTI) Board is a part of the MICRO-PRODAC motor drive control and regulator system. The PTI board is the interface between that microprocessor-based system and the thyristor power supply (TPS) of the motor drive. The PTI provides thyristor gating signals to the TPS and monitors the condition of the three-phase supply for undervoltage, phase loss and incorrect phase rotation faults. In addition, diagnostic information is provided to determine the working state of the gate pulse generator and amplifier, the phase-locked-loop and the "OK" condition of the PTI itself.

The PTI will interface to single or three-phase converters, at 50 or 60 hertz, two or four quadrant without modification. Twelve pulse or circulating current systems require two PTI boards. The PTI will drive MOD-80 Thyristor Gate Driver (TGD) boards. A single phase synchronizing voltage is required, but in three phase applications proper fault detection requires three phase signals.

1.1 Reference Drawings and Figures

1.	PTI Bill of Materials	1939A92
2.	PTI Schematic	4954C64
3.	PTI Assembly View	4961C90
4.	MICRO-PRODAC Standards and Conventions	8449A73
5.	MICRO-PRODAC Product Description	8450A02
6.	MOD-80 Digital Gate Pulse Generator with Large Scale Integration	1914A26
7.	PTI Block Diagram	Figure 1, page 4
8.	PTI Memory Map	Figure 2, page 6
9.	PTI Variable Definitions	Table 1, page 5
10.	GPG Transfer Function	Figure 3, page 9

2.0 FUNCTIONAL DESCRIPTION

This section will describe the operation of the PTI board in enough detail to apply the board properly. Refer to the PTI block diagram (Figure 1) and PTI Memory Map (Figure 2) where needed. The schematic (Appendix 1) may also be referenced by page number (ex: Page A).

2.1 Bus Interface

A full description of bus interfacing is contained in reference four (see Section 1.1). The PTI board is memory mapped in a 16 bit address space. The board will respond to addresses in a 256 byte range (256 bytes = one "page") between 8000 hexadecimal and 8FFF hexadecimal[1]. The exact page of the sixteen possible pages in that space is selected by four board select wires on the P2 connector mounted in the card cage. The P2 connector must be wired so that the board select lines have a binary code equal to the cage slot number. Henceforth, PTI addresses will be referred to as 8N00 to 8NFF hex where N is the slot number (between 0 and F hex).

Figure 2 illustrates the PTI Memory Map. Data on the PTI are either 8 or 16 bit words. The gate angle reference and board status are 16 bits; all other commands are 8 bits. The map shows all board addresses, many of which are not actually used or are duplicates (images) of other addresses. Table 1 lists the preferred address and type of data for each variable.

The PTI board drives bus lines INH1/ and INH2/ which means that any system ROM or RAM on other boards will be inhibited when PTI boards are addressed. This allows memory boards with large address blocks to be shadowed by I/O boards like the PTI between 8000 and 8FFF hex.

The PTI drives the transfer acknowledge handshake line XACK/ with no wait states generated.

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[1]Hexadecimal refers to a base-16 number system, and henceforth is abbreviatred HEX or -H suffix (ex: 8000H).

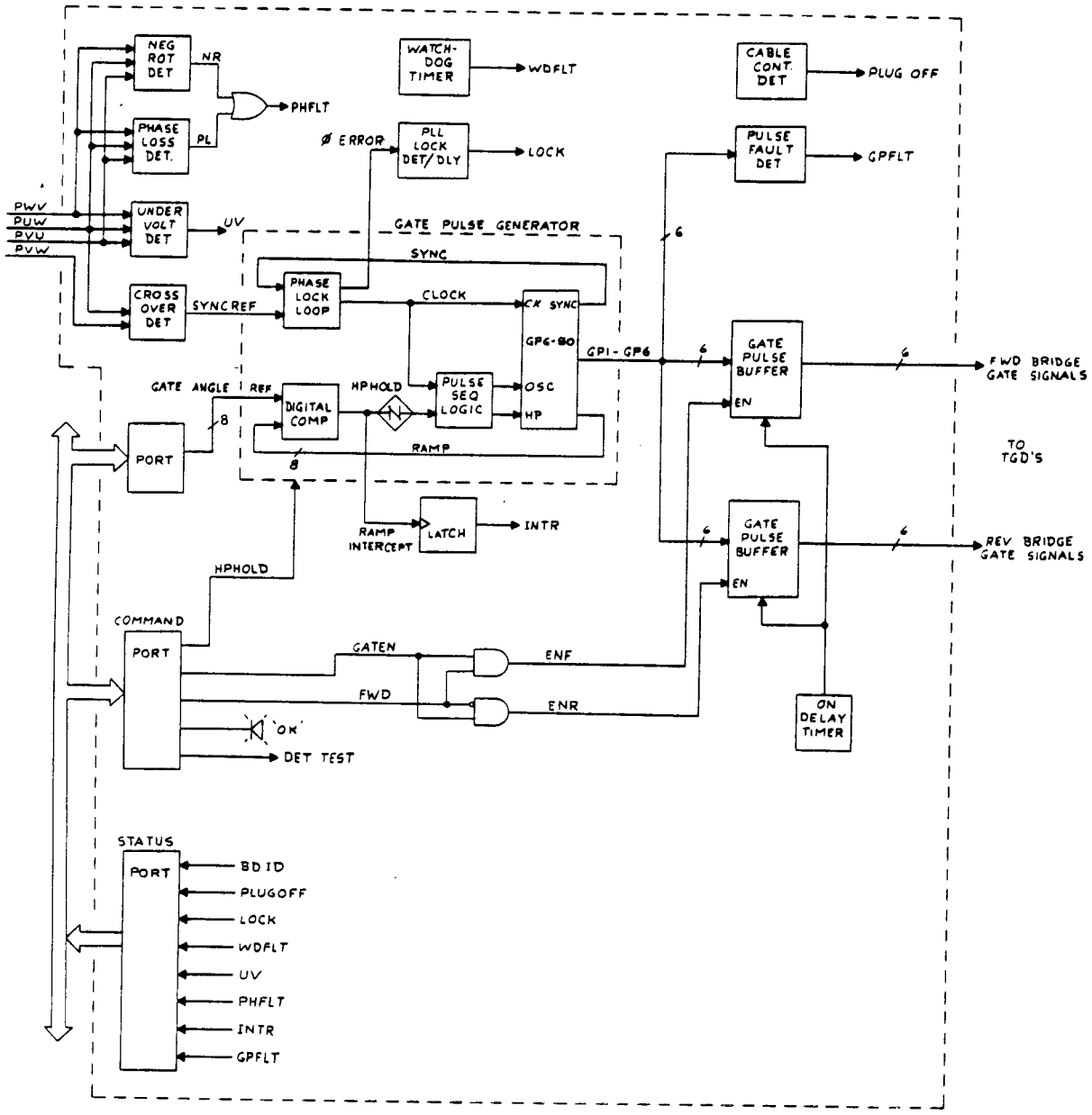

FIG. 1
PTI BLOCK DIAGRAM

VARIABLE	ADDRESS	TYPE	DESCRIBED
BDID	8N00	BYTE	2.4
BDSTATUS	8N00	WORD	2.4
BDRESET	8N08	DONT CARE[2]	2.5
GATEANGLEREF	8N10	INTEGER	2.5
TEST	8N29	LOGICAL[3]	2.5
GATEN	8N2B	LOGICAL[3]	2.5
REV	8N2C	LOGICAL[3]	2.5
HPHOLD	8N2D	LOGICAL[3]	2.5
INTREN	8N2E	LOGICAL[3]	2.5
OK	8N2F	LOGICAL[3]	2.5
PRICHNL	8N30	BYTE	2.5
INTRRST	8N37	DONT CARE[2]	2.3

TABLE 1: VARIABLE DEFINITIONS

2.2 Board Reset

The PTI board is held reset during power-on settling times by the bus signal INIT/. The RESET signal controls the gate pulse generator, command ports, diagnostic timers and watch-dog timer. The RESET signal can also be generated by software at any time by writing to the board reset address (BDRESET - 8N08H)[2].

In addition, a local power-on hold off circuit works specifically to disable the gate pulse drivers for 50 milliseconds (see schematic sheet D). This circuit prevents even narrow transient pulses from reaching the thyristors and causing false turn-on.

Do not operate the PTI board without a CPU board in the same cage. Without the CPU board, no INIT/ signal is generated and the power-up state of the PTI is then unknown. Forward or reverse gate pulses (not both) may be generated at any gate angle.

2.3 Interrupt Generation

The PTI board can operate in the free-running mode with no CPU intervention, or in the interrupt mode. In the latter case, the PTI interrupts the CPU whenever it is time to fire the next thyristor. Thus the CPU can decide whether to allow firing at that time, or perform some action (such as measuring current or checking timing) beforehand.

The Gate Pulse Generator (see section 2.7) raises a signal INTR whenever the digital ramp is greater than the digital gate angle reference. The low-to-high transition of INTR clocks a flip-flop to the set state creating the interrupt request signal INTRQST. Note that when the reference exceeds the GPG advance endstop limit the interrupt may not coincide with the actual gating. When the reference exceeds the retard limit, an interrupt cannot be generated since the ramp is never greater than the reference.

Signal INTRQST will create an interrupt on the bus as directed by the priority control logic. The status of INTRQST can be read in the board status word (BDSTATUS - 8N00H BIT D8).

The INTRQST flip-flop is reset by two methods. After board reset, the interrupt enable command signal (INTREN-8N2EH) is low which holds INTRQST low regardless of any other condition. Thus to operate in the interrupt mode, INTREN must be set high. The second method is writing to the interrupt reset port (INTRRST-8N37H)[2]. This action resets the INTRQST flip-flop until the next low-to-high transition of INTR.

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[2]This variable is "don't care" data; that is, the action of writing any data to this address is sufficient to generate the intended control action regardless of the value of data.

[3]Logical data is byte data where FF hex is true, 00 hex is false, and all other values are not allowed.

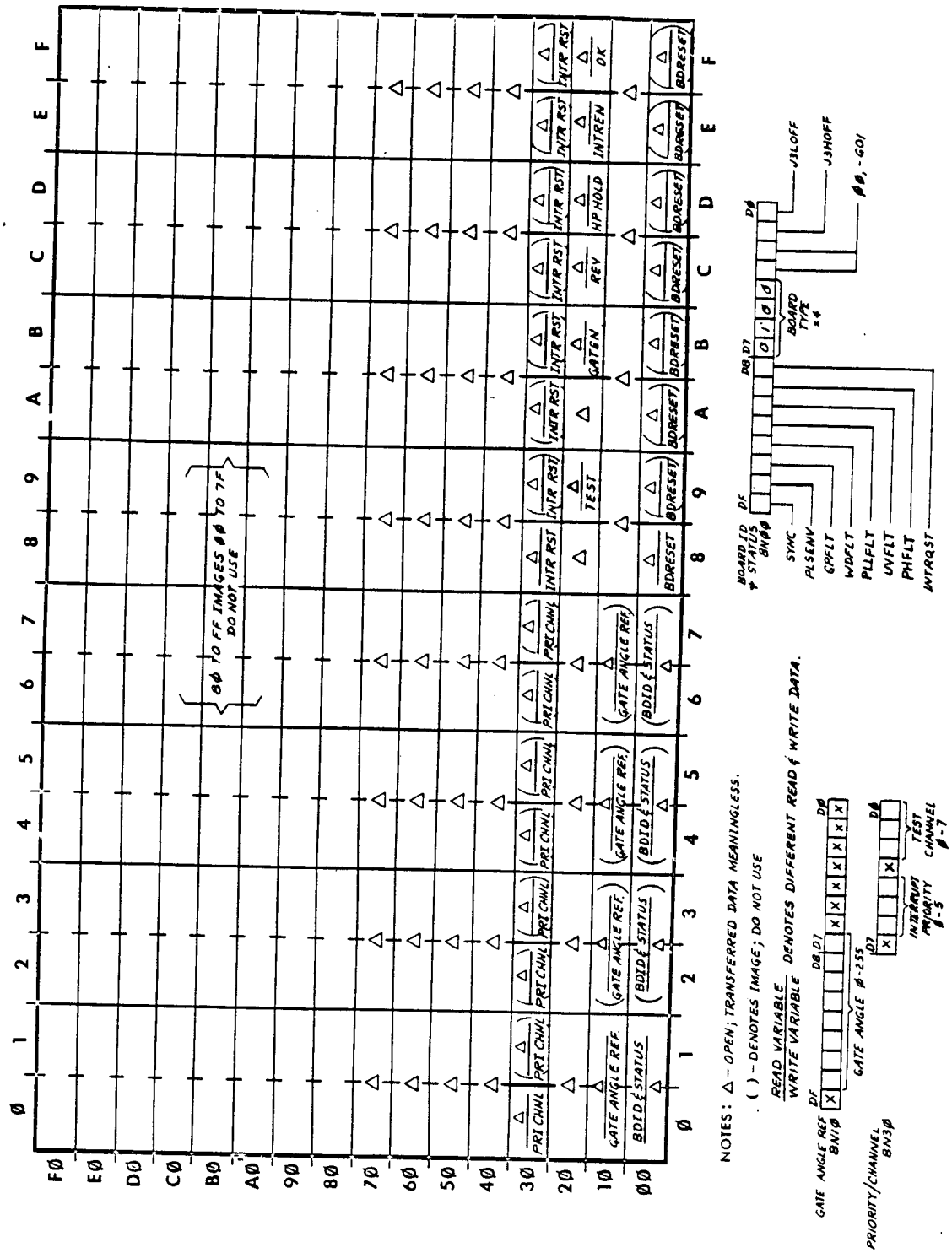


FIG. 2 PTI MEMORY MAP

2.4 Board ID and Status Port

A full description of the Board ID can be found in reference 4 (see section 1.1). The PTI board ID can be read as a byte, or as the lower half of the board status word BDSTATUS, at address 8N00H in either case. The status can only be read as a 16-bit word. The status word will be explained here.

Bits D0 and D1 are cable continuity status bits. See section 2.11.

Bits D2 and D3 denote the group number, or variations in the standard design. The -G01 version is always 00 in these bits.

Bits D4 to D7 are the board type number. All thyristor interface boards are type 4.

Bit D8 is interrupt request status (see section 2.3).

Bit D9 is phasing fault status (see section 2.9).

Bit DA is undervoltage fault status (see section 2.8).

Bit DB is phase-lock fault status (see section 2.10).

Bit DC is watchdog fault status (see section 2.13).

Bits DD and DE are gate pulse fault status (see section 2.12).

Bit DF is the sync. from the GPG (see section 2.7).

2.5 Command Ports

The PTI command ports include the gate angle reference, the interrupt priority and test channel port, and the logical variables for test mode, gate enable, bank selection, hard-pulse hold off, interrupt enable and OK light control. Refer to the PTI Memory Map, figure 2.

The gate angle reference at address 8N10H is a sixteen bit signed integer variable. However, only the eight highest bits are significant, and the sign bit is ignored. The transfer function for this variable is shown in Figure 3 but it is noted here to use caution when programming. The transfer function is discontinuous at zero and therefore limits should be applied to the gate angle reference to avoid wraparound effects.

The PRI/CHNL port is a byte variable containing the interrupt priority number 0 to 5 and the diagnostic test channel number 0 to 7 as shown in figure 2. When changing one of the numbers, use caution so as not to disturb the other. The interrupt priority number steers an interrupt request (see section 2.3) to the corresponding bus line. The proper bus line is determined by system configuration for each PTI board in the system. Use of the test channel is described in section 2.12.

After board reset, the gate angle reference is at full advance limit and should be preset to the proper angle in software. The interrupt priority is reset to INT0, and the test channel is reset to six.

The logical commands TEST, GATEN, REV, HPHOLD, INTREN, and OK are called logical variables because their value is either true or false, that is 0FFH or 00H respectively. All are reset to the false condition.

TEST is a command to enter the test mode wherein the phase-lock, undervoltage and phase fault detectors are made to indicate fault conditions. These detectors can be tested at any time provided system software ignores the fault status and provided sync voltage is correctly applied to the PTI. See sections 2.8, 2.9 and 2.10.

GATEN is the command to enable gate buffers. When set to true gate pulses immediately appear at the PTI outputs. When set to false the gate pulses immediately cease unless a hard-pulse has begun, in which case the pulse finishes and then the buffers are disabled. GATEN is thus similar to GPS/ in MOD-80 systems, except it is not latched in hardware. See section 2.14.

REV is the command to select reverse bank gating for dual converters. When set to false, the forward bank is selected. The PTI contains no other reversing logic, and so GATEN should be set false for a time before and after switching REV. See section 2.14.

HPHOLD is called hard-pulse hold. When set to false, the GPG works in a normal fashion firing the next thyristor and creating an interrupt at the moment the ramp exceeds the reference. When HPHOLD is set to true, the GPG creates the same interrupt but does not fire the next thyristor until HPHOLD is again set to false (or until the hardware retard endstop is exceeded). Thus HPHOLD allows the CPU to take action, such as current measurement, immediately prior to firing the next hard-pulse. See section 2.7.

INTREN is interrupt enable as explained in section 2.3.

OK is the command to turn on the green "OK" LED. See section 2.15.

2.6 Sync Zero Crossing Detector

The sync filter and zero crossing detector are very similar to MOD-80 circuits (see reference 6). The input filter phase delay is about 75 degrees for 50 or 60 hertz inputs. The GPG-80 chip compensates for this delay. Two equal valued resistors at the X1 and XSYNC inputs permit the creation of a phase shifted signal midway between two input sinewaves. When one signal is available which has the phase relationship required for synchronization it is connected to both X1 and XSYNC to form a simple tee filter. A comparator with 50 millivolts hysteresis is used to detect zeroes of the filtered input and convert to square waves.

The nominal input voltage for X1 and XSYNC is 20.0 volts RMS with respect to PSC.

2.7 Gate Pulse Generator

The gate pulse generator consists of the phase-locked loop, the GPG-80 LSI chip, a digital comparator and some support circuitry. The operation is similar to the MOD-80 DGPG circuitry in reference 6 with some exceptions as noted here.

The phase-locked loop function and dynamic response is identical to MOD-80. One change was made to facilitate addition of a phase-lock detector (see section 2.10). This change results in the GPG running at very low frequency when sync voltage is removed. In MOD-80, the GPG would stop completely for that condition.

Since the GPG-80 chip cannot be reset, software must be provided to clear the internal counters. MOD-80 had separate hardware for this function. After power and sync voltage have been applied to the PTI several cycles should elapse with the GPG-80 gating at less than 100 degrees. Thus the PTI should be reset (which sets gate angle to full advance) and the CPU should wait until the PLL detector (which contains a delay of several cycles) indicates the "locked" condition. At this time the GPG-80 is fully cleared and ready to use. Note that this clearing procedure is only required after power is applied to the PTI.

The comparator circuit is digital as compared to the analog MOD-80. Thus the digital angle reference must be transferred from the CPU to the GPG. Since these two circuits are running asynchronously, the gate angle reference port contains a flip-flop that holds the comparator output off for 40 microseconds or less after a new reference has been transferred. The 40 microsecond jitter is one clock period of the GPG, and only occurs when the new reference is transferred at the same instant a thyristor is to be gated.

The transfer function of the GPG is shown in figure 3. The input can be positive or negative integers (not both) from 0 to 32,767. The output gating angle is linear from -7.5 degrees to +217.5 degrees. Advance endstop is at -7.5 degrees; retard endstop at +217.5 degrees, and tailend chop at +225 degrees. Software endstops are strongly recommended to prevent problems with interrupt generation when that mode is used (see section 2.3). Note that if hard-pulse hold is used to temporarily delay thyristor gating, it will be overridden by the retard endstop limit (see section 2.5). Also HPHOLD will introduce 40 microseconds of delay after it is set false before the thyristor will be gated.

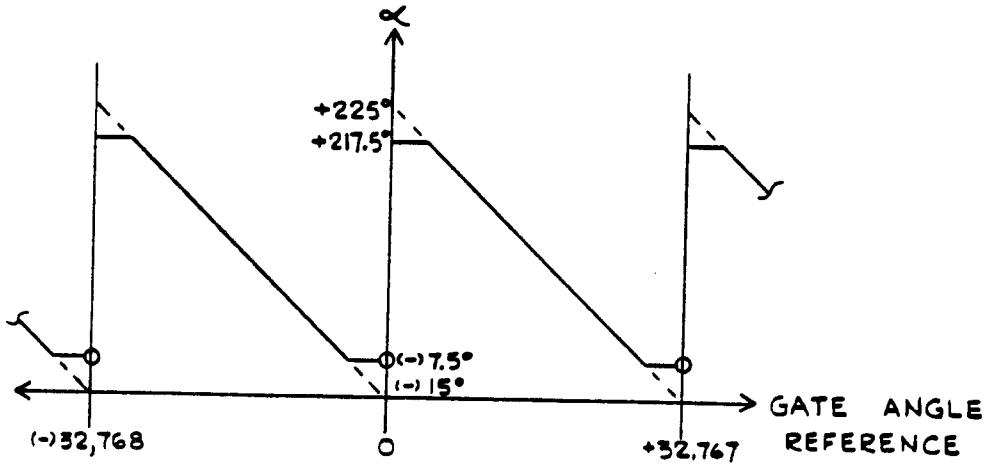


FIGURE 3

GPG TRANSFER FUNCTION

2.8 Undervoltage Detector

The undervoltage detector monitors the AC power line via feedback from the sync transformer. The nominal input voltage for this detector is 20.0 volts RMS with respect to PSC for each input. The detector will indicate undervoltage for inputs less than 70 ±5% of nominal. The detector provides some filtering such that instantaneous removal of nominal sync voltages would cause undervoltage indication after a delay of 21 ±5 milliseconds (filter TC = 51 MS).

The circuit measures the peak value of the sync voltage. Three phase systems use half wave three phase rectification of the sync voltages on inputs X1, X3 and X5. Single phase systems use full wave single phase rectification of inputs X1 and X3 (X5 is left open or jumpered to X3). Because of the peak reading detector, undervoltage will still read correctly in the presence of a phase loss fault in three phase systems.

The status of the undervoltage detector UVFLT can be read at the RDSTATUS address 8N00H BIT DA. If the logical variable TEST is set true then UVFLT is forced high. When TEST is set false UVFLT resumes its correct status.

2.9 Phase Fault Detector

The phase fault detector combines phase loss and negative phase rotation faults into one fault signal called PHFLT. The phase loss detector is fast and will respond to loss of one phase within one-half cycle. In single phase systems the detector correctly indicates phase loss all the time. The detector compensates for changes in the peak value of line voltage and will indicate correctly in the presence of undervoltage down to 40% of the nominal 20V RMS input.

The negative rotation detector expects the voltage at X3 input to lead the voltage at X5 by 120 degrees. Should the line phase sequence be incorrect X3 will lag X5 and PHFLT will indicate the error. This detector also compensates for changes in line voltage.

When a drive is first commissioned, a PHFLT error cannot distinguish between negative rotation and phase loss. A measurement is required to correct the problem. However, once the phase rotation is known to be correct, any future PHFLT errors are likely to be only phase loss failures.

The status of PHFLT can be read at the BDSTATUS address 8N00H BIT D9. If the logical variable TEST is set true then PHFLT is forced high. When TEST is set false PHFLT will resume the correct status.

2.10 Phase Locked Loop (PLL) Fault Detector

The PLL fault detector monitors the phase error of the GPG phase locked loop (see section 2.7). If that error is greater than 45 degrees a fault is indicated immediately. If the phase error becomes smaller than 17 degrees the fault signal is removed after a delay of approximately 110 milliseconds. This time delay must be used at power up to allow the gate pulse generator to clear after the sync voltage is applied. Thus, the total time before the GPG is ready will be the capture and lock time of the PLL plus the 110 millisecond delay.

The status of PLLFLT can be read at the BDSTATUS address 8N00H BIT DB. If the logical variable TEST is set true then PLLFLT is forced high. When TEST is set false PLLFLT resumes its correct status after the normal time delay.

2.11 Cable Continuity Fault Detector

There are two signals on the PTI used to determine that the board front connector and cable have continuity. These signals are LATC and HATC (low end attached and high and attached). Provided that +12 to +30 volts DC is tied to these signals at the remote end of the cable then continuity status signals J3LOFF and J3HOFF will be low. If the voltage drops below 6 volts DC or is removed on either line then the appropriate status signal goes high indicating the high or low end of the connector is off. By switching voltages on or off at the remote end of the cable other diagnostic conditions can be monitored by these status lines.

The status signals J3LOFF and J3HOFF can be read at the BDSTATUS or BDID address 8N00H BITS D0 and D1 respectively.

2.12 Gate Pulse Fault Detector

The gate pulse fault detector allows the PTI board operation to be tested thoroughly using system software in off-line modes. It also provides a single status bit GPFLT that can be monitored on-line giving an overall indication that the PTI is working.

An eight channel selector is programmed to look at the six gate pulses, the picket fence clock, and PSC. The selected signal is fed to two retriggerable one-shot timers. The first timer fills in the spaces between picket fence pulses resulting in a signal that is the envelope of the gate pulse waveform. This signal is called PLSENV. The second timer fills in the spaces between envelope signals and so outputs a steady signal GPFLT that is always low if the PLSENV is switching correctly. Thus GPFLT is a usable indication of a working PTI provided that the GPG is cleared properly and the test channel is set to any of the gate pulses.

Test channels are selected as described in section 2.5. The signals corresponding to each channel are as follows:

Ch 0	GPG Clock	VCOCLK
Ch 1	Gate Pulse 1	GP1
Ch 2	Gate Pulse 2	GP2
Ch 3	Gate Pulse 3	GP3
Ch 4	Gate Pulse 4	GP4
Ch 5	Gate Pulse 5	GP5
Ch 6	Gate Pulse 6	GP6
Ch 7	PSC	PSC

After board reset channel six is selected. Initially PLSENV is low and GPFLT is high, but these signals eventually assume their normal state.

Selecting channel zero allows testing of the GPG clock and also verifies operation of the diagnostic timers. In this mode PLSENV is always high and GPFLT is always high. These signals should be monitored continuously over a full line cycle either by counting six interrupts or by reading the SYNC signal which has a one cycle period.

Selecting channels one through six allows testing of the GPG functions. By comparing PLSENV timing to the SYNC signal the following tests can be made for each of the gate pulses:

- o Hard-pulse timing
- o Picket fence operation
- o Phase angle adjustment
- o Tail end chop
- o Gate pulse duty cycle

In this mode, GPFLT should always be low, and should be monitored continuously over a full line cycle.

Selecting channel seven switches PSC to the timer inputs causing PLSENV to be low and GPFLT to be high when measured continuously over a full line cycle. This verifies proper timer operation. When changing modes allow sufficient time for the timers to reach their new correct state.

Signals GPFLT, PLSENV and SYNC can be read at the BDSTATUS address 8N00H Bits DD, DE and DF respectively. Refer to reference 6 for gate pulse timing. SYNC undergoes a low-to-high transition at 75 degrees.

2.13 Watchdog Timer

A watchdog timer is provided that will disable gating in 25 milliseconds if gating was enabled and if gate angle reference updating ceases for any reason. Should a watchdog fault occur it is latched and can only be reset by a board reset (see section 2.2).

Detailed operation of the watchdog sequence is best described by the following statements.

1. A watchdog fault WDFLT can never occur when GATEN is low (i.e. gating disabled).
2. Any time the gate angle reference port is written-to or updated, the watchdog timer is retriggered to the beginning of its 25 millisecond period.
3. A watchdog fault will occur and be latched only if the watchdog timer times out to the end of its 25 millisecond period while GATEN is high (gating enabled).
4. Once WDFLT occurs gating is held disabled immediately until the fault is cleared by a board reset.
5. The watchdog timer is not reset when gating is disabled but continues to the end of its period. Provided that GATEN is still low at that time no WDFLT will occur.

Signals are available on the P2 edge connector to generate and read watchdog faults. These may be used for redundant protection, or in the event of power supply failure or other external events, to disable gating quickly and surely.

The status of WDFLT can be read at the BDSTATUS address 8N00H bit DC.

2.14 Gate Pulse Buffers

The gate pulse buffers are used to interface between PTI logic levels and Thyristor Gate Driver (TGD) boards. Other functions include bank selection and guaranteed hold-off of gate pulses while the logic power supply is turning on.

The buffers accept logic inputs from 5 volt logic and can drive loads up to 30 volts DC. The output drivers are open collector types, and pull up resistors are provided on board. The pull up voltage must be supplied to the PTI from the load power supply. Optionally, if the pull up voltage is 15 or 24 VDC it may be applied to the P2 edge connector on the appropriate pins. This arrangement would allow observation of the output pulses on an oscilloscope even though the J3 front connector was off. The current rating for each output is 100 milliamps max.

Bank selection is accomplished by enabling only one set of buffers at a time (or neither set if GATEN is low). The logical variable REV controls which bank is selected. Note that there is no reversing sequence logic on the PTI. That logic must be done in software, and probably requires that GATEN be set low during reversals. After board reset, the forward bank is selected. See section 2.5.

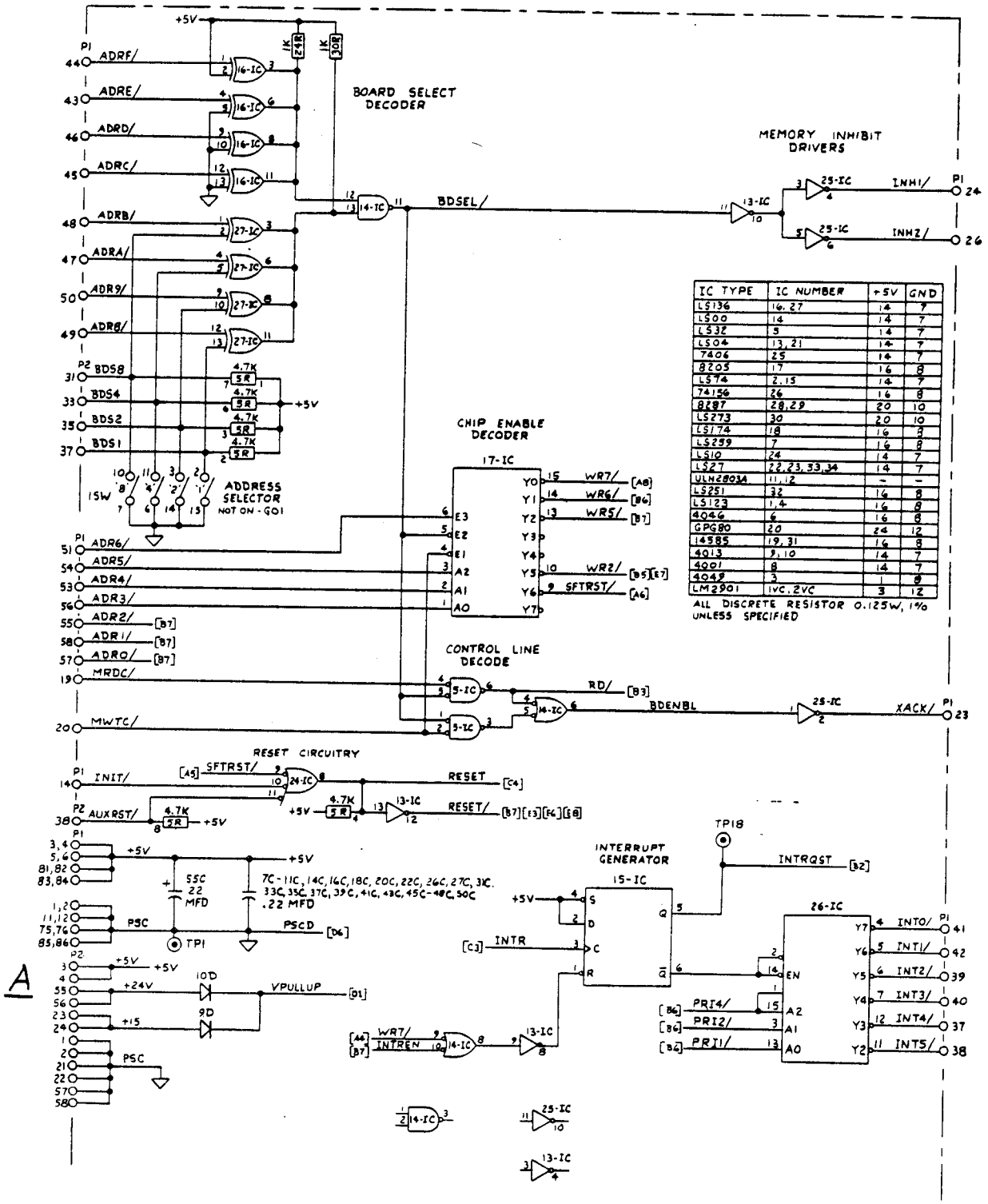
The power-up holdoff circuit will keep the output buffers disabled whenever the 5 volt logic supply is below 3.2 volts, and includes a 40 millisecond delay while the suppply rises to its final value. This delay is sufficient to keep the gates off until the bus signal INIT/ becomes active and resets the entire PTI board. Should the supply ever drop below 3.2 volts, the output buffers will be quickly disabled. No alarm is provided for this occurence since the system is obviously in the process of failing or being turned off.

2.15 OK Light

The OK light is a green LED which should be on whenever the PTI board is judged to be operating correctly. It should be turned off only when the PTI card itself is diagnosed as faulty. Do not use the OK light to indicate system faults such as undervoltage, phase fault, etc. This would confuse service personnel and violate the MICRO-PRODAC standards.

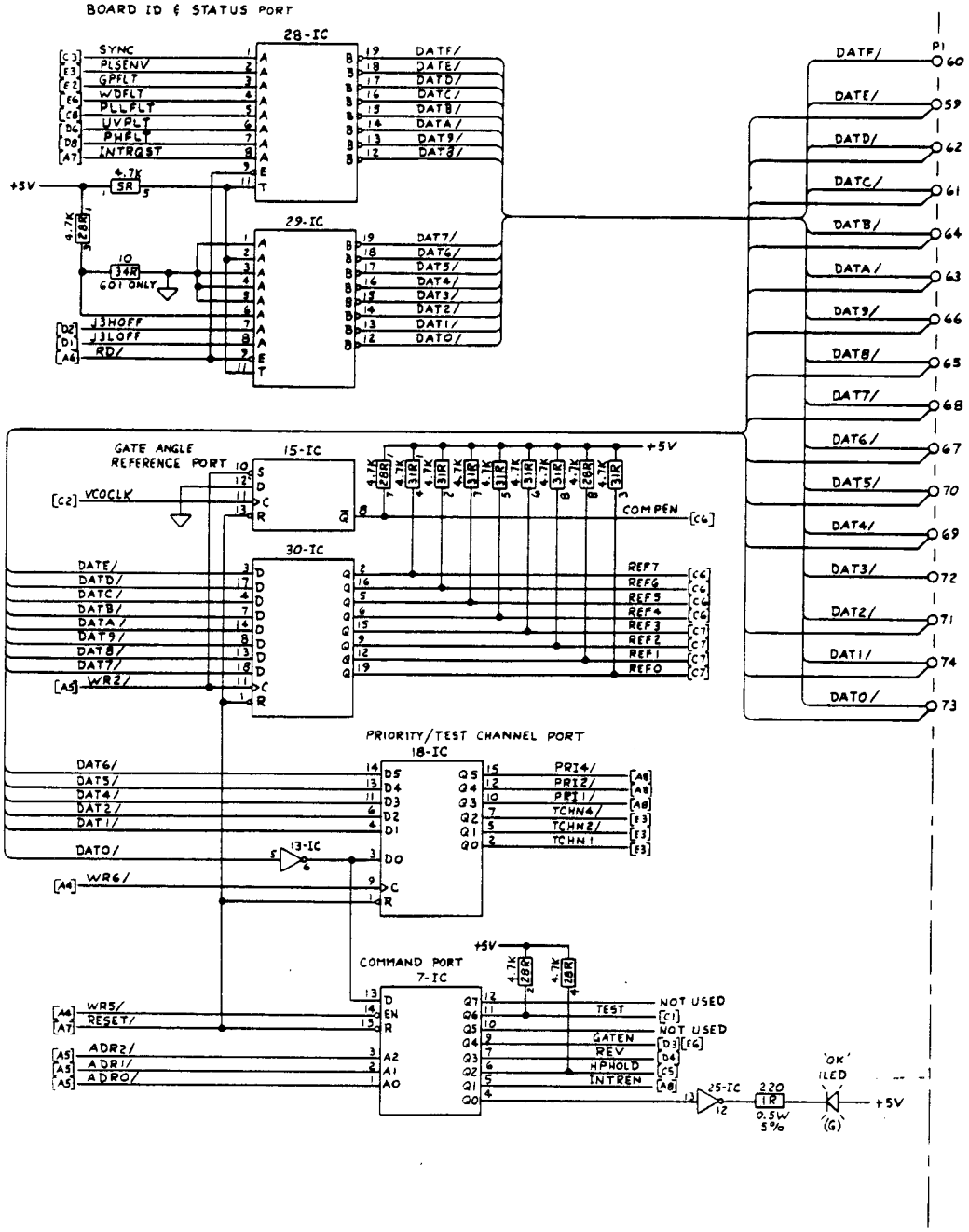
OK is a logical variable at address 8N2FH. True data turns the light on; false turns it off. After board reset, the light is off.

APPENDIX A1



IC TYPE	IC NUMBER	+5V	GND
LS136	16, 27	14	7
LS00	14	14	7
LS32	5	14	7
LS04	13, 21	14	7
7406	25	14	7
8205	17	16	8
LS74	2, 15	14	7
74156	26	16	8
8287	28, 29	20	10
LS273	30	20	10
LS174	18	16	8
LS259	7	16	8
LS10	24	14	7
LS27	22, 23, 33, 34	14	7
ULN2803A	11, 12	–	–
LS251	32	16	8
LS123	1, 4	16	8
4046	6	16	8
GPG80	20	24	12
14585	19, 31	16	8
4013	9, 10	14	7
4001	8	14	7
4049	3	1	8
LM2901	IVC, 2VC	3	12

ALL DISCRETE RESISTOR 0.125W, 1% UNLESS SPECIFIED


BOARD ID & STATUS PORT
28-IC
29-IC
SYNC
PLSENV
GPFLT
WDFLT
PLLFLT
UVPLT
PWFLT
INTRQST
DATF/
DATE/
DATD/
DATC/
DATB/
DATA/
DAT9/
DAT8/
DAT7/
DAT6/
DAT5/
DAT4/
DAT3/
DAT2/
DAT1/
DAT0/
J3HOFF
J3LOFF
RD/
GOT ONLY
+5V
P1
GATE ANGLE
REFERENCE PORT
15-IC
VCOCLK
COMPEN
30-IC
WR2/
REF7
REF6
REF5
REF4
REF3
REF2
REF1
REF0
PRIORITY/TEST CHANNEL PORT
18-IC
WR6/
PRI4/
PRI3/
PRI2/
PRI1/
TCHN4/
TCHN3/
TCHN1
13-IC
COMMAND PORT
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WR5/
RESET/
ADR2/
ADR1/
ADR0/
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REV
HPHOLD
INTREN
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5%
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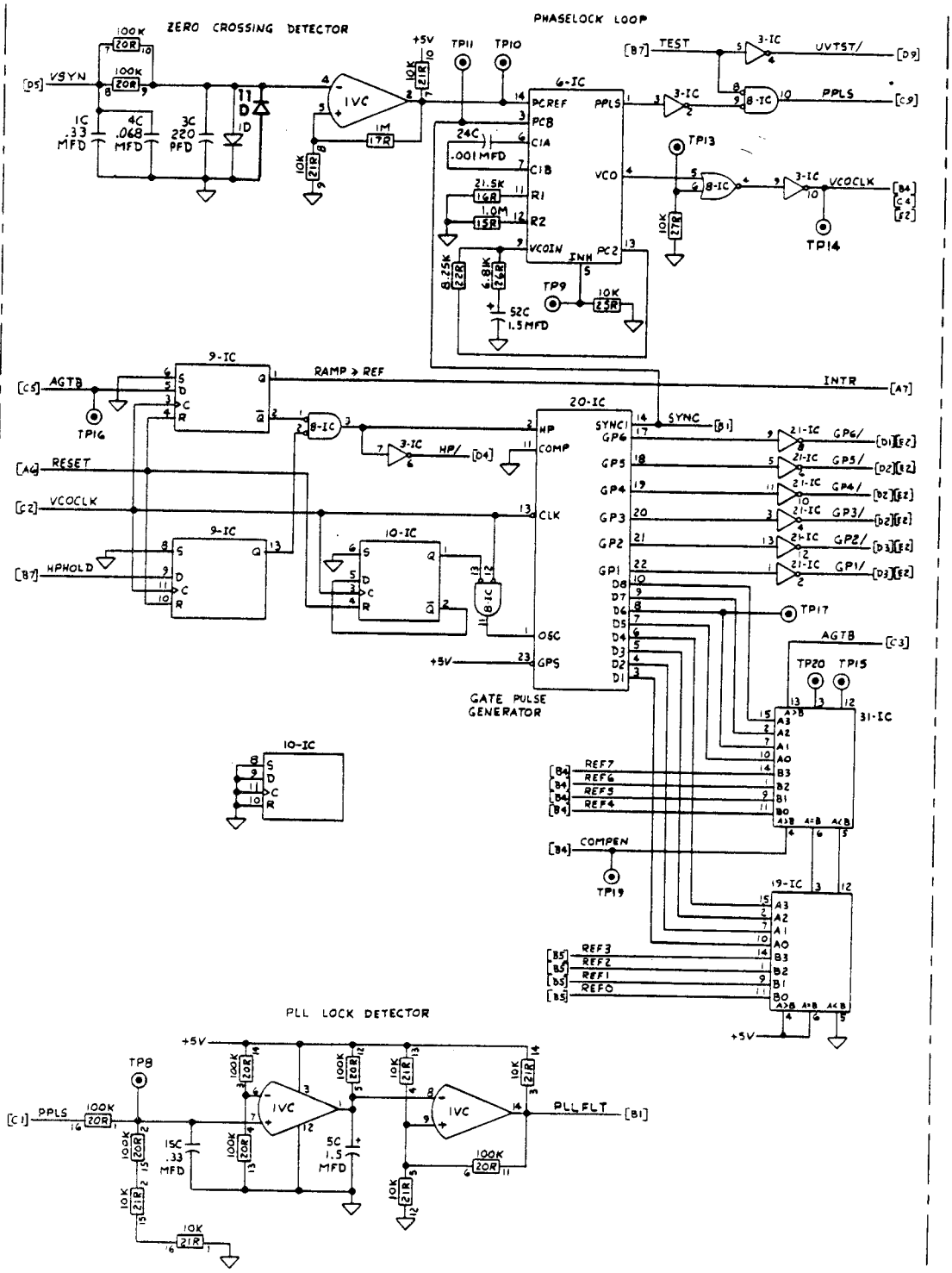
LED
(G)

B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PHASELOCK LOOP
PLL LOCK DETECTOR
GATE PULSE GENERATOR
VSYN
PPLS
TEST
UVTST/
VCOCLK
INTR
RAMP > REF
AGTB
RESET
HPHOLD
HP/
SYNC
COMPEN
REF7
REF6
REF5
REF4
REF3
REF2
REF1
REF0
PLLFLT
TP8
TP9
TP10
TP11
TP13
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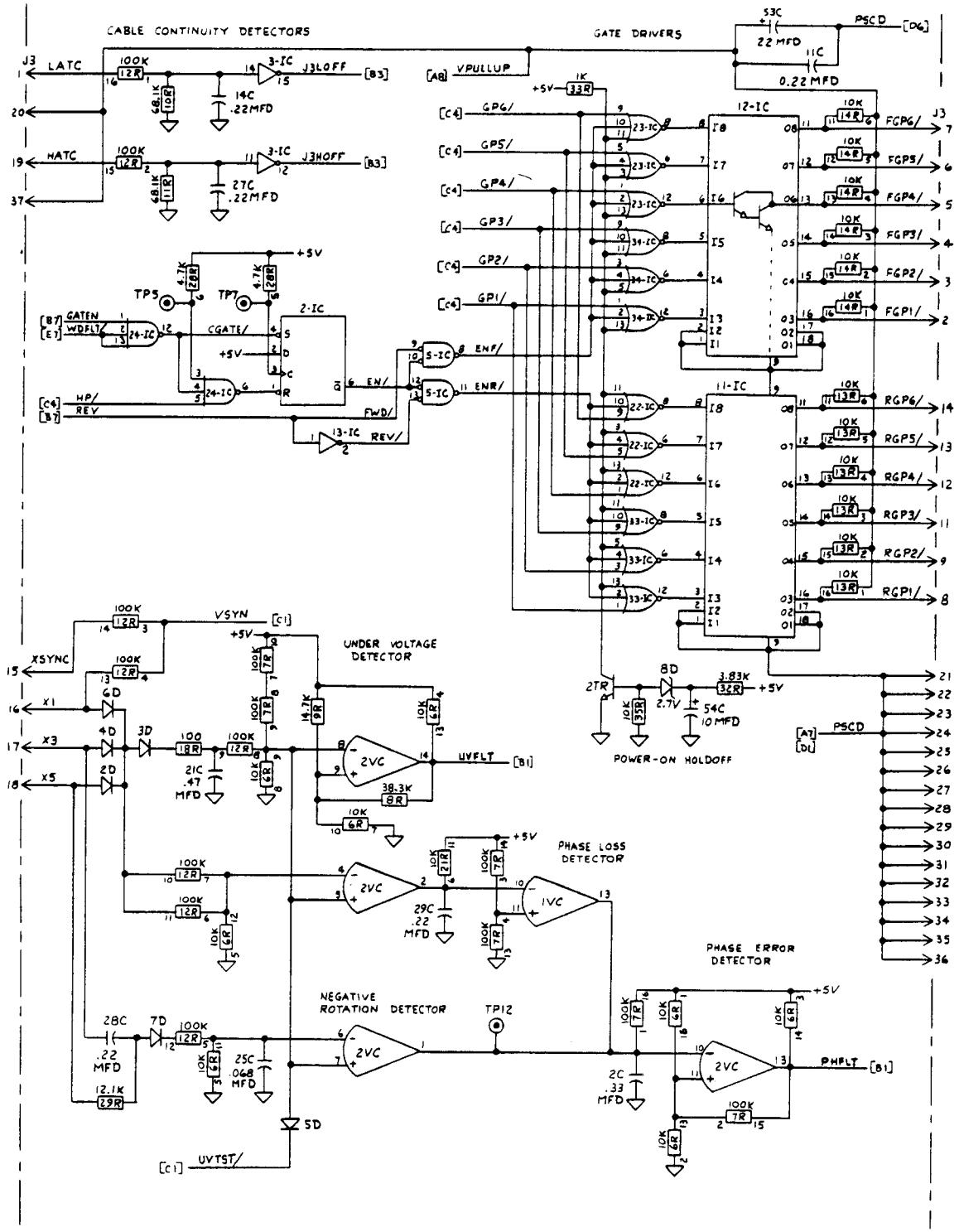
CABLE CONTINUITY DETECTORS
GATE DRIVERS
PSCD
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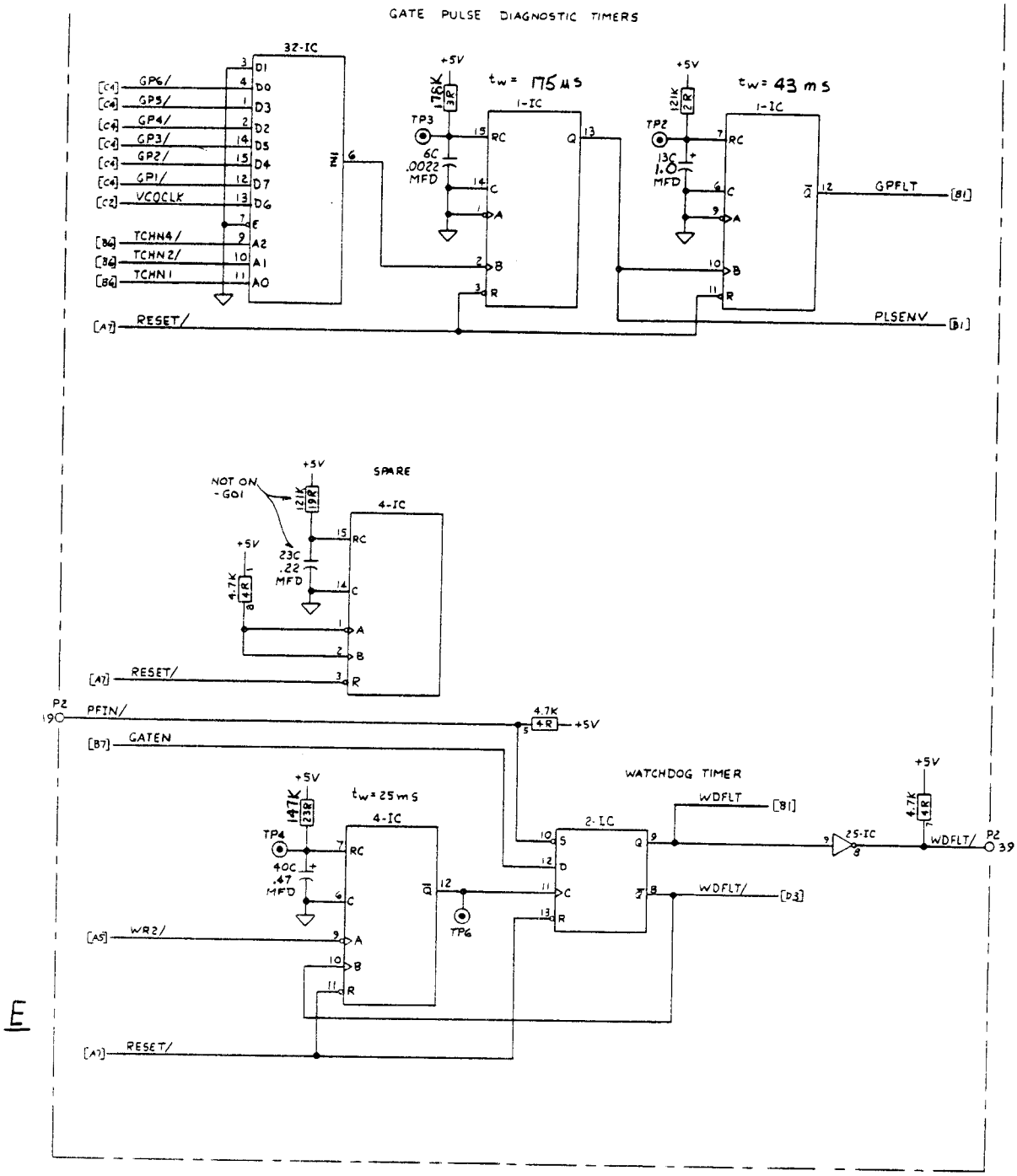
0.22 MFD
LATC
HATC
J3LOFF
J3HOFF
VPULLUP
GP6/
GP5/
GP4/
GP3/
GP2/
GP1/
FGP6/
FGP5/
FGP4/
FGP3/
FGP2/
FGP1/
RGP6/
RGP5/
RGP4/
RGP3/
RGP2/
RGP1/
TP5
TP7
GATEN
WDFLT
CGATE/
EN/
ENF/
ENR/
HP/
REV
FWD/
REV/
VSYN
XSYNC
X1
X3
X5
UNDER VOLTAGE DETECTOR
UVFLT
POWER-ON HOLDOFF
PHASE LOSS DETECTOR
PHASE ERROR DETECTOR
NEGATIVE ROTATION DETECTOR
TP12
PHFLT
UVTST/

D


GATE PULSE DIAGNOSTIC TIMERS
32-IC
GP6/
GP5/
GP4/
GP3/
GP2/
GP1/
VCOCLK
TCHN4/
TCHN2/
TCHN1
RESET/
+5V
tw = 175 ms
1-IC
TP3
.0022 MFD
tw = 43 ms
TP2
1.0 MFD
GPFLT
PLSENV
NOT ON -GO1
SPARE
4-IC
.22 MFD
P2
PFIN/
GATEN
WATCHDOG TIMER
tw = 25 ms
TP4
.47 MFD
2-IC
WDFLT
WDFLT/
WR2/
TP6
25-IC
E

APPENDIX 2

Specifications (0 - 50°C)

	MIN	NOM	MAX	UNITS
I. Input				
Sync voltage	5.0	20.0	50.0	VRMS
Sync frequency	47	50/60	63	HERTZ
Continuity Detector Hi	7.0	-	30.0	VDC
Continuity Detector Lo	-1.0	0.	3.0	VDC
II. Gate Outputs				
Output Voltage Lo (at 100 mA)	0	-	1.0	VDC
Output Voltage Hi	0	-	30	VDC
Output Current Hi (at 30V)	0	-	1.0	mADC
Rise Time (2K Pull up resistor)	-	-	10.0	uS
Fall Time	-	-	1.0	
Picket Fence Frequency (at 60 Hz)	-	11.5	-	KHZ
Picket Fence Duty Cycle	-	25	-	%
Hard Pulse Width (at 60 Hz)	-	43.4	-	uS
III. Power Supply				
Logic Voltage	4.75	5.00	5.25	VDC
Logic Current	-	0.300	0.375	ADC
Pull Up Voltage	12	-	30	VDC
Peak Pull Up Current (at 30V)	0	-	7	mADC
Average Pull Up Current (at 30V)	0	-	0.5	mADC

Cont'd

APPENDIX 2 (CONT'D)

IV. Gate Angle Output for All Reference Levels

0.	32.	64.	96.	128.	160.	192.	224.
217.5000	195.0000	165.0000	135.0000	105.0000	75.0000	45.0000	15.0000
1.	33.	65.	97.	129.	161.	193.	225.
217.5000	194.0625	164.0625	134.0625	104.0625	74.0625	44.0625	14.0625
2.	34.	66.	98.	130.	162.	194.	226.
217.5000	193.1250	163.1250	133.1250	103.1250	73.1250	43.1250	13.1250
3.	35.	67.	99.	131.	163.	195.	227.
217.5000	192.1875	162.1875	132.1875	102.1875	72.1875	42.1875	12.1875
4.	36.	68.	100.	132.	164.	196.	228.
217.5000	191.2500	161.2500	131.2500	101.2500	71.2500	41.2500	11.2500
5.	37.	69.	101.	133.	165.	197.	229.
217.5000	190.3125	160.3125	130.3125	100.3125	70.3125	40.3125	10.3125
6.	38.	70.	102.	134.	166.	198.	230.
217.5000	189.3750	159.3750	129.3750	99.3750	69.3750	39.3750	9.3750
7.	39.	71.	103.	135.	167.	199.	231.
217.5000	188.4375	158.4375	128.4375	98.4375	68.4375	38.4375	8.4375
8.	40.	72.	104.	136.	168.	200.	232.
217.5000	187.5000	157.5000	127.5000	97.5000	67.5000	37.5000	7.5000
9.	41.	73.	105.	137.	169.	201.	233.
216.5625	186.5625	156.5625	126.5625	96.5625	66.5625	36.5625	6.5625
10.	42.	74.	106.	138.	170.	202.	234.
215.6250	185.6250	155.6250	125.6250	95.6250	65.6250	35.6250	5.6250
11.	43.	75.	107.	139.	171.	203.	235.
214.6875	184.6875	154.6875	124.6875	94.6875	64.6875	34.6875	4.6875
12.	44.	76.	108.	140.	172.	204.	236.
213.7500	183.7500	153.7500	123.7500	93.7500	63.7500	33.7500	3.7500
13.	45.	77.	109.	141.	173.	205.	237.
212.8125	182.8125	152.8125	122.8125	92.8125	62.8125	32.8125	2.8125
14.	46.	78.	110.	142.	174.	206.	238.
211.8750	181.8750	151.8750	121.8750	91.8750	61.8750	31.8750	1.8750
15.	47.	79.	111.	143.	175.	207.	239.
210.9375	180.9375	150.9375	120.9375	90.9375	60.9375	30.9375	0.9375
16.	48.	80.	112.	144.	176.	208.	240.
210.0000	180.0000	150.0000	120.0000	90.0000	60.0000	30.0000	0.0000
17.	49.	81.	113.	145.	177.	209.	241.
209.0625	179.0625	149.0625	119.0625	89.0625	59.0625	29.0625	-0.9375
18.	50.	82.	114.	146.	178.	210.	242.
208.1250	178.1250	148.1250	118.1250	88.1250	58.1250	28.1250	-1.8750
19.	51.	83.	115.	147.	179.	211.	243.
207.1875	177.1875	147.1875	117.1875	87.1875	57.1875	27.1875	-2.8125
20.	52.	84.	116.	148.	180.	212.	244.
206.2500	176.2500	146.2500	116.2500	86.2500	56.2500	26.2500	-3.7500
21.	53.	85.	117.	149.	181.	213.	245.
205.3125	175.3125	145.3125	115.3125	85.3125	55.3125	25.3125	-4.6875
22.	54.	86.	118.	150.	182.	214.	246.
204.3750	174.3750	144.3750	114.3750	84.3750	54.3750	24.3750	-5.6250
23.	55.	87.	119.	151.	183.	215.	247.
203.4375	173.4375	143.4375	113.4375	83.4375	53.4375	23.4375	-6.5625
24.	56.	88.	120.	152.	184.	216.	248.
202.5000	172.5000	142.5000	112.5000	82.5000	52.5000	22.5000	-7.5000
25.	57.	89.	121.	153.	185.	217.	249.
201.5625	171.5625	141.5625	111.5625	81.5625	51.5625	21.5625	-7.5000
26.	58.	90.	122.	154.	186.	218.	250.
200.6250	170.6250	140.6250	110.6250	80.6250	50.6250	20.6250	-7.5000
27.	59.	91.	123.	155.	187.	219.	251.
199.6875	169.6875	139.6875	109.6875	79.6875	49.6875	19.6875	-7.5000
28.	60.	92.	124.	156.	188.	220.	252.
198.7500	168.7500	138.7500	108.7500	78.7500	48.7500	18.7500	-7.5000
29.	61.	93.	125.	157.	189.	221.	253.
197.8125	167.8125	137.8125	107.8125	77.8125	47.8125	17.8125	-7.5000
30.	62.	94.	126.	158.	190.	222.	254.
196.8750	166.8750	136.8750	106.8750	76.8750	46.8750	16.8750	-7.5000
31.	63.	95.	127.	159.	191.	223.	255.
195.9375	165.9375	135.9375	105.9375	75.9375	45.9375	15.9375	-7.5000