INPUT ISOLATION BOARD

S#1640A29

I. INTRODUCTION

This card contains six circuits, each of which serves as an attenuator, isolator and filter for coupling external high level logic signals into 5 or 15 volt controllers. The input signals are the presence or absence of some defined AC or DC voltage. These signals usually indicate an open or closed contact on some external device.

Table 1 shows the input voltages which can be used with the different styles of this card, as well as the logic type into which each style interfaces. The operate times for each style are also given.

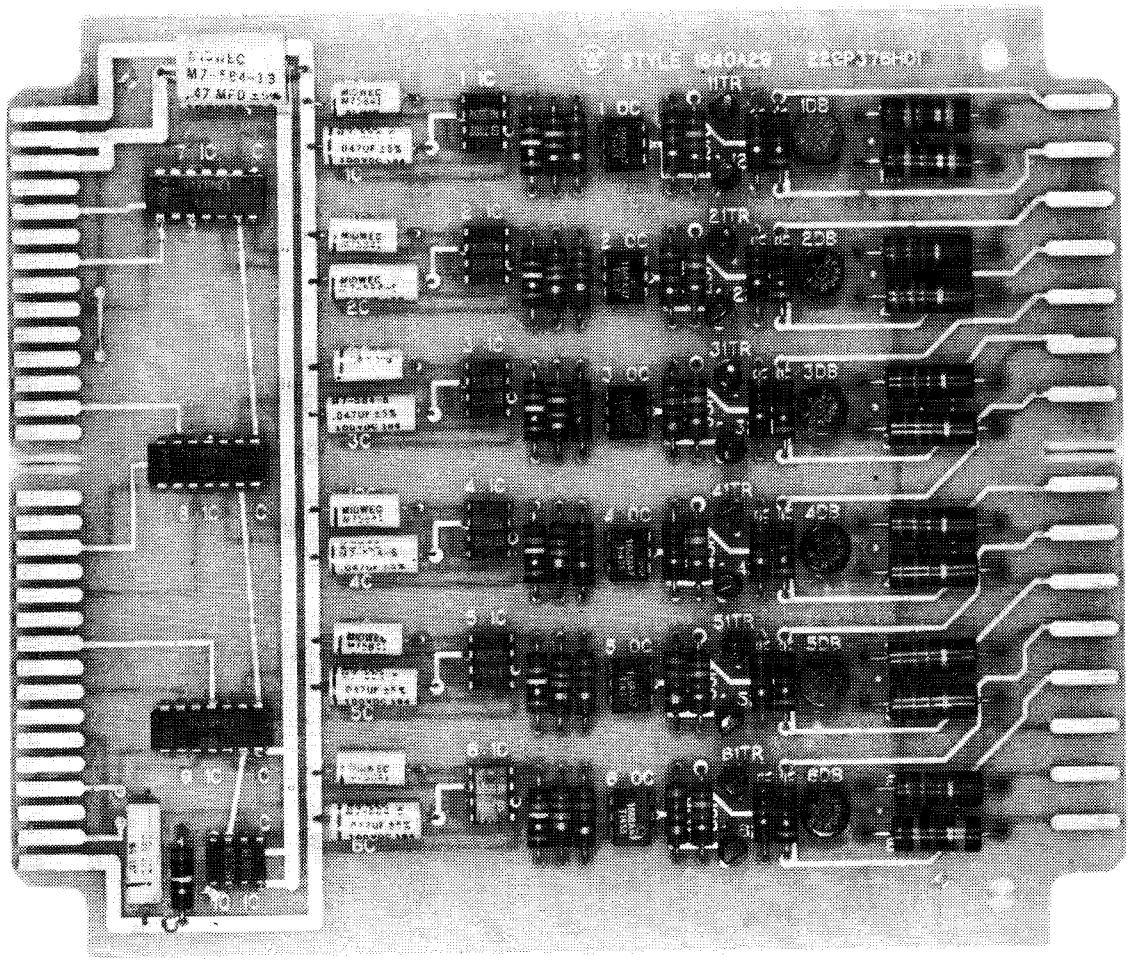

FIGURE 1

EFFECTIVE DATE: December 1975

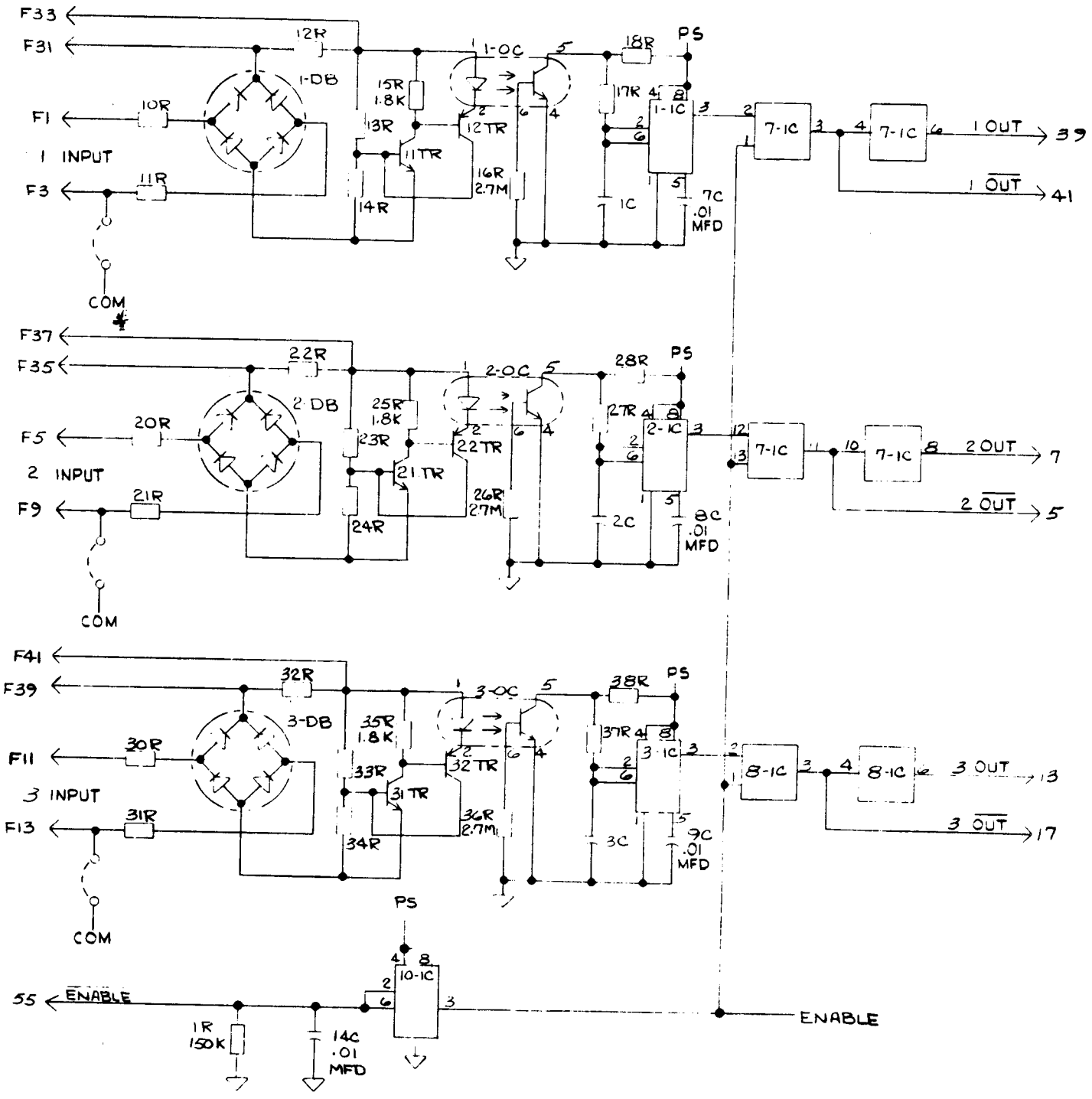
F33
F31
12R
1-DB
F1
10R
1 INPUT
F3
11R
COM
15R
1.8K
13R
11TR
14R
12TR
16R
2.7M
1-OC
18R
PS
17R
1-IC
1C
7C
.01
MFD
7-IC
7-IC
1 OUT
39
1 OUT
41
F37
F35
22R
2 DB
F5
20R
2 INPUT
F9
21R
COM
25R
1.8K
23R
21TR
24R
22TR
26R
2.7M
2-OC
28R
PS
27R
2-IC
2C
8C
.01
MFD
7-IC
7-IC
2 OUT
7
2 OUT
5
F41
F39
32R
3-DB
F11
30R
3 INPUT
F13
31R
COM
35R
1.8K
33R
31TR
34R
32TR
36R
2.7M
3-OC
38R
PS
37R
3-IC
3C
9C
.01
MFD
8-IC
8-IC
3 OUT
13
3 OUT
17
PS
55
ENABLE
1R
150K
14C
.01
MFD
10-IC
ENABLE

FIG. 2(a)

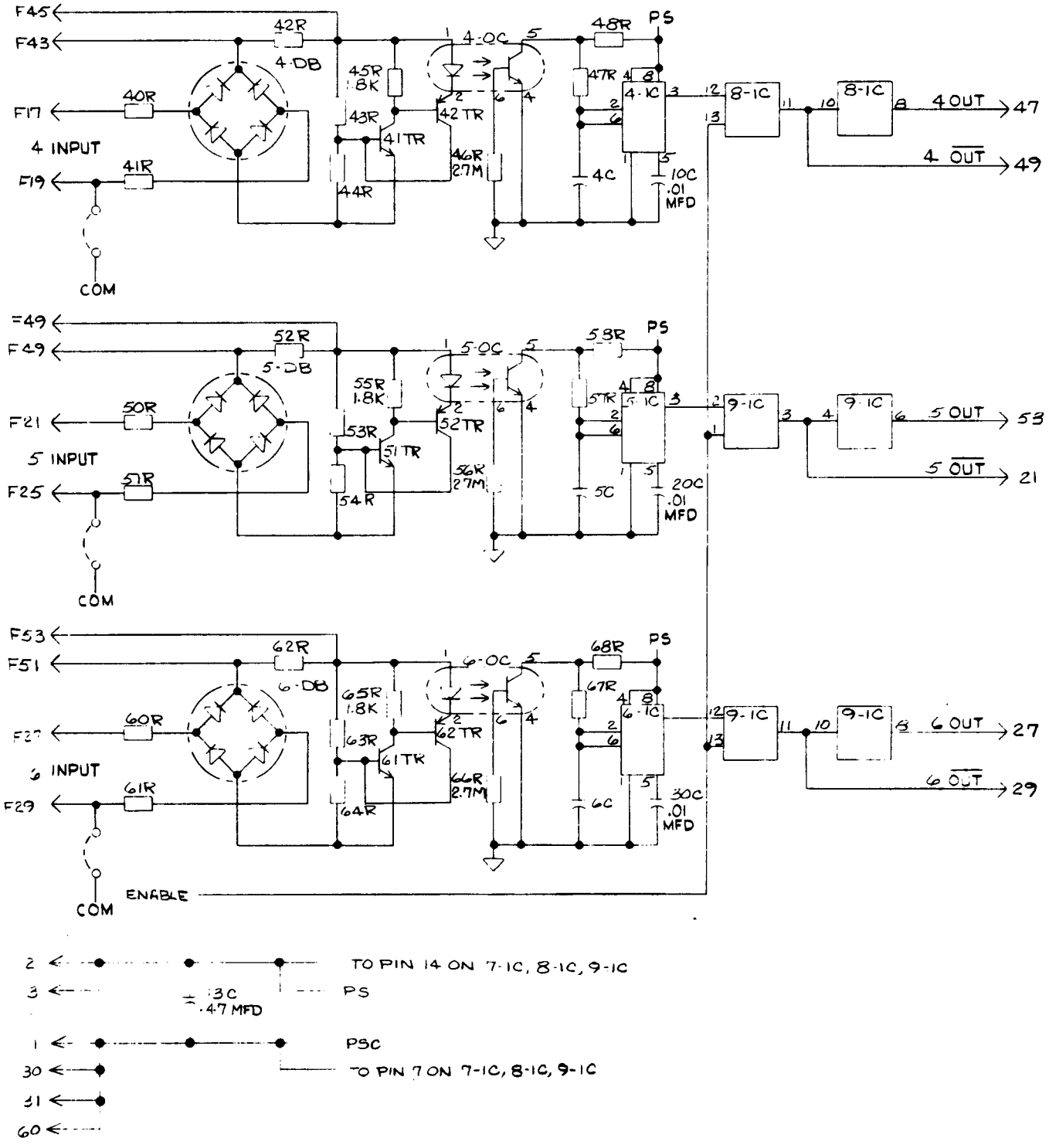
F45
F43
42R
4-DB
48R
PS
4-OC
45R 1.8K
47R
4-IC
8-IC
8-IC
4 OUT
47
F17
40R
43R
42 TR
41 TR
4 INPUT
F19
41R
46R 2.7M
4C
10C .01 MFD
4 OUT
49
44R
COM
F49
52R
5-DB
58R
PS
5-OC
55R 1.8K
57R
5-IC
9-IC
9-IC
5 OUT
53
F21
50R
53R
52 TR
51 TR
5 INPUT
F25
51R
56R 2.7M
5C
20C .01 MFD
5 OUT
21
54R
COM
F53
62R
6-DB
68R
PS
6-OC
65R 1.8K
67R
6-IC
9-IC
9-IC
6 OUT
27
F27
60R
63R
62 TR
61 TR
6 INPUT
F29
61R
66R 2.7M
6C
30C .01 MFD
6 OUT
29
64R
COM
ENABLE
2
3
13C .47 MFD
PS
TO PIN 14 ON 7-IC, 8-IC, 9-IC
1
PSC
30
31
60
TO PIN 7 ON 7-IC, 8-IC, 9-IC

FIG. 2(b)

	INPUT VOLTAGE	LOGIC POWER SUPPLY VOLTAGE	OPERATE TIMES (MILLISECONDS, TYPICAL) PICKUP	OPERATE TIMES (MILLISECONDS, TYPICAL) DROPOUT	ONE SIDE OF INPUTS CONNECTED TOGETHER	INPUT CURRENT (ma)
G01	110 VAC ±25% 110 VDC ±20%	5 VDC ±10%	4 - 8 4	11 - 15 15	No	8 ±25% 8 ±20%
G02	20 - 60 VDC	5 VDC ±10%	0.7	1.2	No	4 - 15
G03	110 VAC ±25% 110 VDC ±20%	12 - 16 VDC	4 - 8 4	11 - 15 15	No	8 ±25% 8 ±25%
G04	11 - 28 VDC	5 VDC ±10%	0.7	1.2	No	6 - 21
G05	20 - 50 VAC 20 - 60 VDC	5 VDC ±10%	4 - 8 4	11 - 15 15	No	4 - 13 4 - 15
G06	20 - 50 VDC 20 - 60 VDC	12 - 16 VDC	4 - 8 4	11 - 15 15	No	4 - 13 4 - 15
G07	20 - 60 VDC	12 - 16 VDC	0.7	1.2	No	4 - 15
G08	110 VAC ±25% 110 VDC ±20%	5 VDC ±10%	4 - 8 4	11 - 15 15	Yes	8 ±25% 8 ±20%
G09	110 VAC ±25% 110 VDC ±20%	15 VDC ±10%	4 - 8 4	11 - 15 15	Yes	8 ±25% 8 ±20%

TABLE 1

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When an input voltage within the defined voltage range is present at the input terminals, the OUT terminal is a LOGIC 1 (high level) and the $\overline{\text{OUT}}$ terminal is a LOGIC 0 (low level). If the input voltage is not present, or if the $\overline{\text{ENABLE}}$ input is at a LOGIC 1, or both, then the OUT terminal is a LOGIC 0 and the $\overline{\text{OUT}}$ terminal is a LOGIC 1. See definitions of LOGIC 0 and LOGIC 1 below.

The circuit ignores all input voltages below a threshold level, typically 1/2 of the nominal input voltage.

Power Supply Current (typical): G01, G02, G04, G05, G08: 5VDC ± 40 ma
G03, G06, G07 15VDC ± 100 ma.

Logic Loading: Each OUT terminal will drive 8 logic loads.

Each $\overline{\text{OUT}}$ terminal will drive 7 logic loads.

The $\overline{\text{ENABLE}}$ input should be considered 1 logic load. If left unconnected, this input assumes the low (LOGIC 0) state.

The above logic loads refer to DTL loads(5volt logic) or HTL loads (15 volt logic).

The inputs card can also be used to interface with CMOS circuits.

Logic Level Definitions:

	G01,G02,G04,G05,G08		G03,G06,G07		
A logic 1 state is defined as:	+5.5V	to +2.6V	+16V	to	+12.5V
A logic 0 state is defined as:	0.0V	to +0.5V	0.0V	to	+1.5V

III. DESCRIPTION OF OPERATION

Refer to the first of the six inputs shown in the scheme (top of Figure 2(a)).

In order to get a LOGIC 1 signal on the 1 OUT terminal 39, a voltage as defined in Table 1 must be applied across the INPUT terminals F1 and F3 (terminals with F prefixes are located on the front edge of the board, away from the backplane). If the applied input is an AC voltage, the signal is rectified by the diode bridge 1-DB. A visible light-emitting diode (VLED) is typically connected between terminals 31 and 33, anode on 31, and the rectified input current (as limited by resistors 10R and 11R) flows through the VLED, through 12R and through the voltage divider 13R and 14R. Whenever sufficient current flows to raise the voltage across 14R to approximately 0.6 volts, 11TR turns on which turns on 12TR and causes current to flow in the infra-red light-emitting diode (IR LED) of the coupler. Current flowing in the IR LED causes the phototransistor to conduct current, which discharges capacitor 1C through 17R. When the voltage across 1C drops to 1.7 volts, the output of timer 1-IC (pin 3) rises to a high state, giving a LOGIC 0 output on terminal 41 ($\overline{1\ \text{OUT}}$) and a LOGIC 1 output on terminal 39 (1 OUT). With AC inputs, current in the optical coupler is derived from the rectified but unfiltered sine-wave input voltage. The current in the photoransistor is therefore pulsing at 120 hz (for 60 hz inputs). During the time when current in the phototransistor is off, 1C begins to charge. But the charging time constant τ = (17R +18R) X 1C is approximately 10msec., so the capacitor does not charge to a very high voltage before it is discharged again through the phototransistor at the next half-cycle of the input current. Only when the input voltage is removed does 1C charge to the 3.4 volt threshold voltage of the timer 1-IC. At this time the outputs change back to their initial states. The capacitor stays charged to about 4 to 5 VDC until the next time the input voltage is present.

When the $\overline{\text{ENABLE}}$ input is driven to the LOGIC 1 state, all six circuits are inhibited so that the OUT terminals become LOGIC 0 and the $\overline{\text{OUT}}$ terminals become LOGIC 1, regardless of the presence or absence of voltage on the individual inputs.

IV. SERVICE

Personnel familiar with electrical equipment utilizing semiconductors can isolate most problems using an oscilloscope, multimeter, and information contained in relative instruction leaflets.

Semi-automatic equipment is available at the factory to test static and dynamic performance of all edge-connected, printed circuit boards. Generally, repair of boards is facilitated by returning them to :

Westinghouse Electric Corporation
Industrial Equipment Division
P. O. Box 225
Buffalo, New York 14240

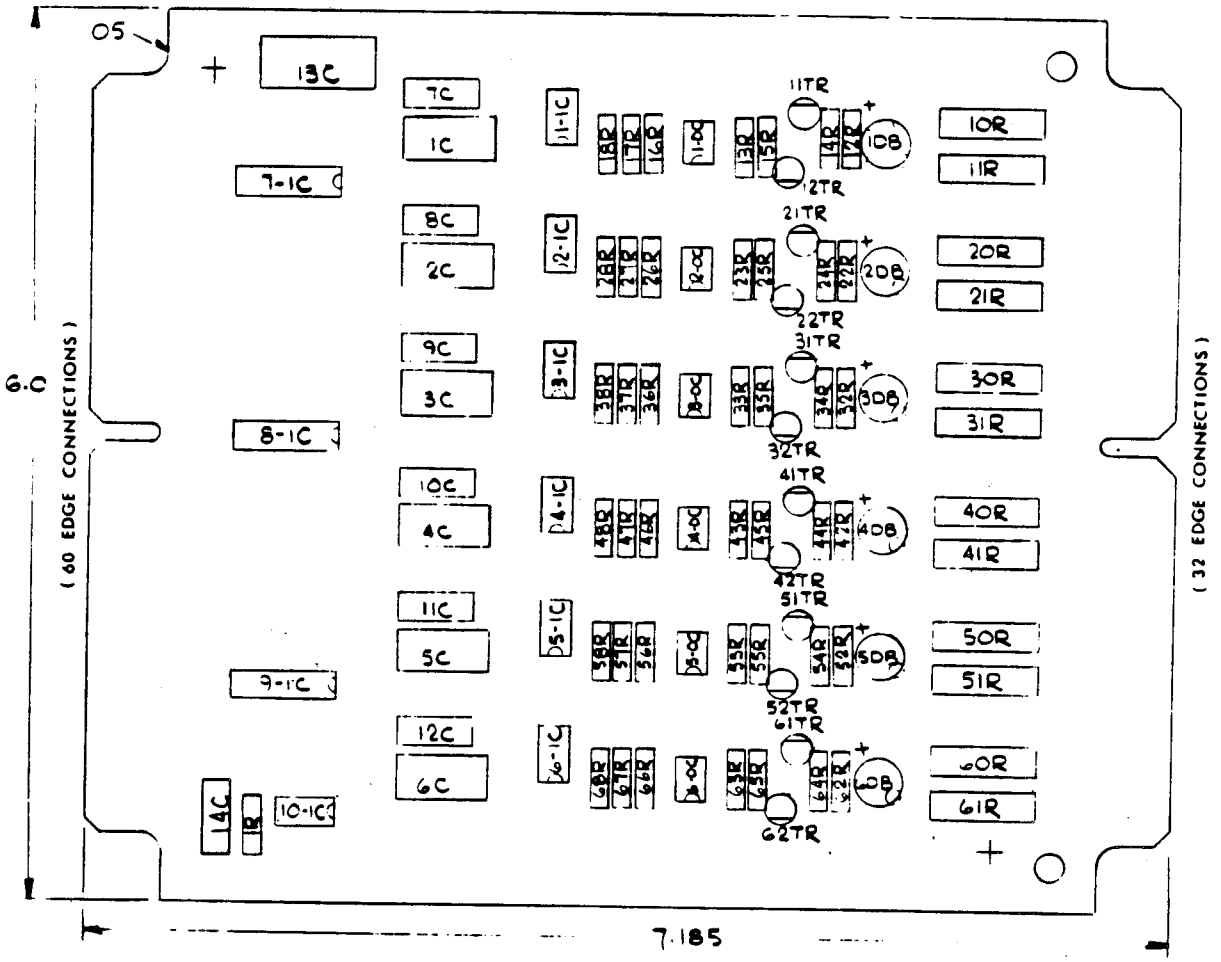

FIGURE 4