

## C-56 GATE CONTROL SYSTEM

## I. INTRODUCTION

The C-56 gate control system consists of one gate control transformer S#1295A25, three gate pulse generator (GPG) boards S#1326A15, the gate driver section of the voltage controller (VC) printed circuit board S#1326A16 et.al, a portion of the reversing logic (RL) printed circuit board S#1326A14, all of which are on the basic regulator assembly S#1339A24 et. al.; the pulse distribution (PD) panel S#1339A06 et. al., several components mounted adjacent to each main thyristor, and the interconnecting wiring, all of which are on the thyristor power modulator (TPM) assembly S#1339A19 et. al. The system provides six accurately-spaced pulses which require no tracking adjustment, inherent line voltage compensation, a fixed bias which "slides" with changes in line voltage maintaining a constant bias gating angle, three interchangeable GPG boards with no adjustments, a gating angle retardation limit (for single-converter motor field supplies) which "slides" with changes in line voltage, and double pulsing (to be explained below).

This material describes the functions of the various circuits. The generation of a typical gate pulse, for example--pulse #2, will be traced from the gate driver input signal  $V_C$  to thyristor #2 in the TPM. It must be recognized that the circuitry described here is contained in several parts of the C-56 regulator and is not a distinct module which could be used unchanged for other applications. It should also be noted that the schematic diagrams presented in this material are not complete and not necessarily up to date. They will, however, serve the instructional purpose intended here.

## II. DESCRIPTION OF OPERATION

Figure 1 is a block diagram of the gate control system.

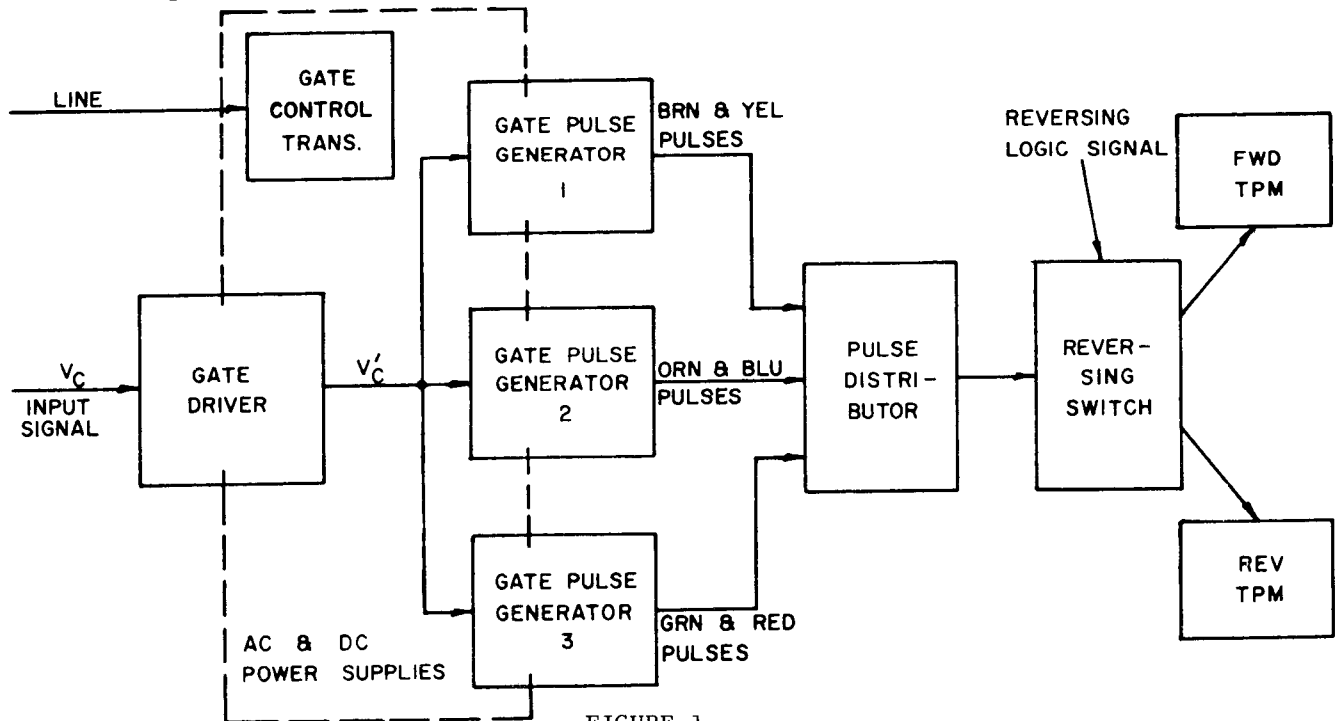
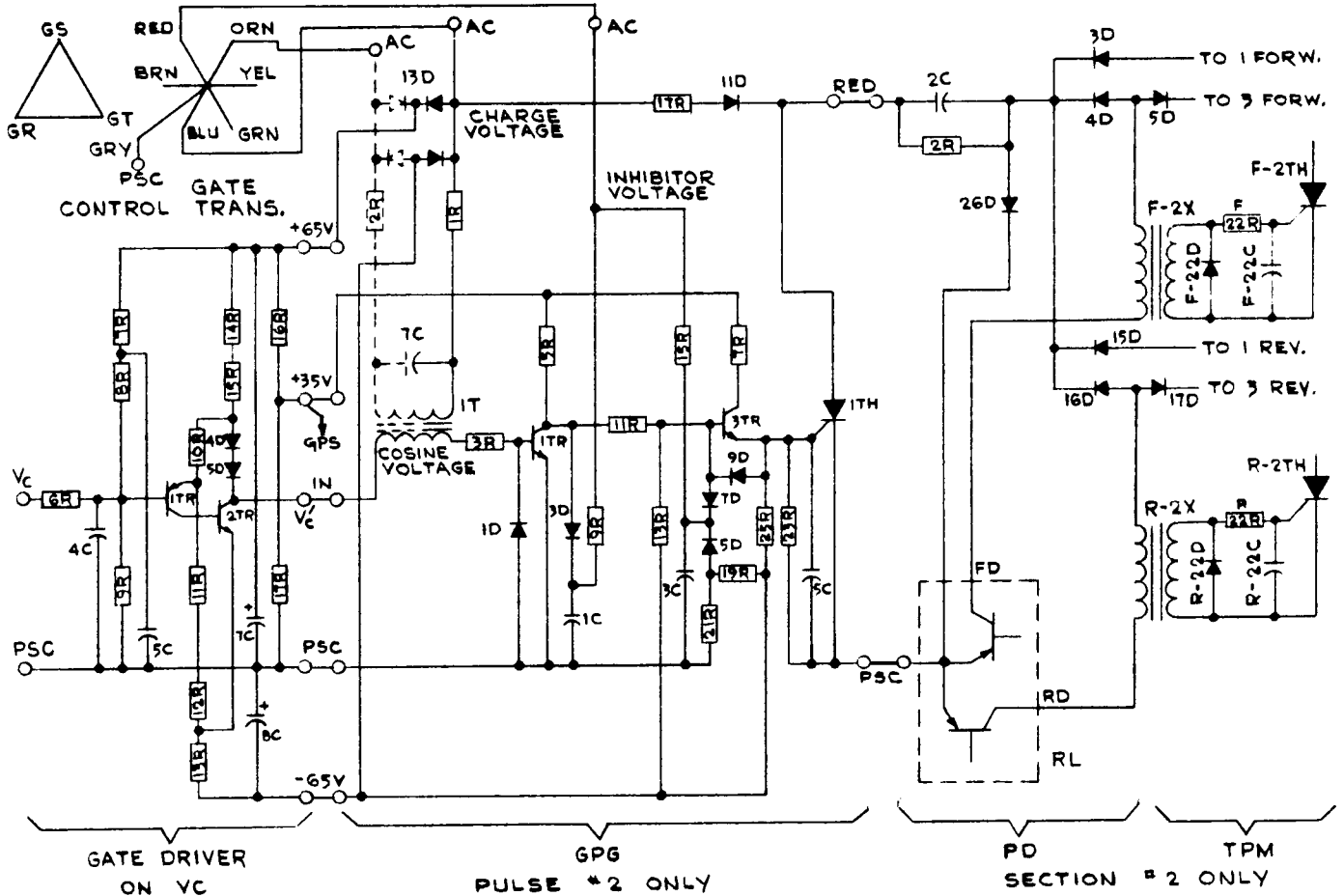


FIGURE 1

Figure 2 shows the circuitry required for generating pulse #2.



## B. Gate Driver

This circuit consists of a 100  $\mu$ sec. filter (6R and 4C on VC), an input network, and a gain-of-two amplifier.

1. Input Network - The circuit consisting of 7R, 8R, 9R, and 5C on VC provides two functions:
  - a. A filtered bias, which for zero-volts input to the GD, provides a GD output voltage of approximately:
    - (1) for dual converters and single-converter armature supplies: 7 volts.
    - (2) for single-converter field supplies: 0.7 volts.
  - b. An attenuation of approximately:
    - (1) for dual converters and single-converter armature supplies: 0.8.
    - (2) for single converter field supplies: 0.5.
  - c. A gating angle retardation limit of approximately  $155^\circ$  for single-converter field supplies.
2. Gain of Two Amplifier - This feedback amplifier compares the input voltage on the base of transistor 1TR with the feedback voltage obtained at the junction of resistors 10R and 11R. The error signal is amplified by the current gains of transistors 1TR and 2TR. Diodes 4D and 5D provide temperature compensation for the base-emitter junction of transistor 1TR. The remaining resistors and capacitors in the circuit set dc bias conditions for the transistors.

## C. Gate Pulse Generator

The GPG is fed by three sine waves, an input signal  $V_C'$ , and a dc collector supply voltage of approximately 35 volts.

1. AC Power Supply - Figure 3 shows the phase relationship between the cosine voltage, the charging voltage, and the inhibiting voltage. The half cycles during which each sine wave acts is shown solid, while the inactive portion is dotted.

The gating angle,  $\alpha$ , is measured from the point when the anode voltage on the main thyristor first goes positive. Pulsing is restricted to approximately  $10^\circ < \alpha < 170^\circ$  for dual converters and single-converter armature supplies, &  $10^\circ < \alpha < 155^\circ$  for single-converter field supplies. The point  $\alpha = 155^\circ$  is referred to as the gating angle retardation limit.

The cosine voltage, as explained above, is obtained from the  $60^\circ$  filter consisting of 1R, 2R, and 7C. The position of the inhibitor is set by components 9R, 1C, 15R, and 3C. The charging voltage is limited by resistor 17R. Diodes 3D, 7D, 5D, 9D, and 11D determine the active portions of the inhibitor and charge voltages respectively.
2. Circuit Operation - At the point in time when the algebraic sum of the input voltage to the GPG,  $V_C'$ , and the cosine voltage cross zero volts in the range  $10^\circ < \alpha < 170^\circ$ , transistor switch 1TR shuts off, causing a positive voltage to appear on the collector. This voltage appears at a reduced value on the base of transistor switch 3TR causing the latter

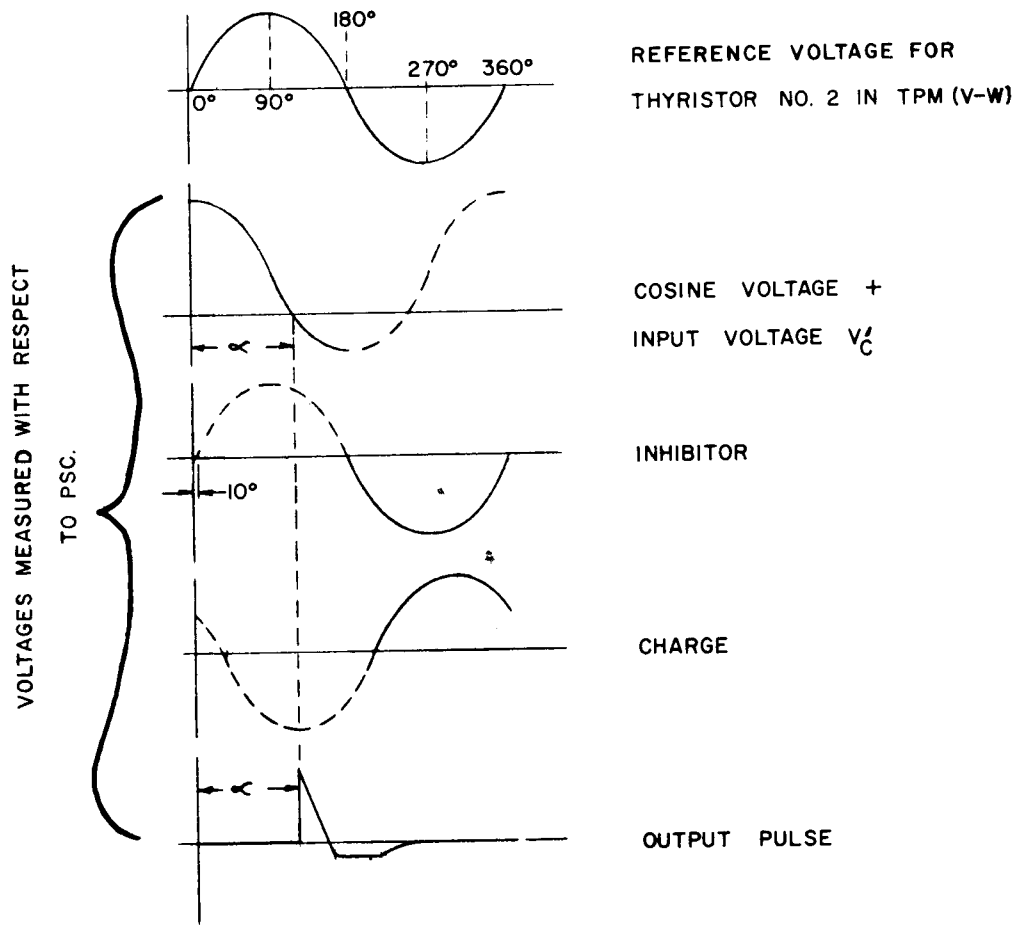


FIGURE 3

to turn on. The emitter-follower action of transistor 3TR causes 1TH to fire. Capacitor 2C on the PD board discharges causing a pulse to appear across the pulse transformer F-2X on the TPM.

During the period  $180^\circ < \alpha < 370^\circ$ , pulsing must not occur. This is accomplished by the inhibitor which pulls the collector of 1TR negative through diode 3D regardless of the signal on the base of the transistor. At the same time, turn off of the thyristor (silicon-controlled switch) is insured by pulling the gate of 1TH negative to approximately -3 volts through diode 5D and voltage divider 15R and 25R. Other components on the GPG board set dc bias levels for transistors, protect base-emitter and gate-cathode junctions, and provide noise filtering.

#### D. Pulse Distributor

1. Capacitor Discharge Circuit - The pulse generation circuit on the GPG boards and the PD board could be simplified as in Figure 4 and then would generate a single pulse each cycle. In Figure 4, the charging voltage

charges capacitor 2C during the time  $180^\circ < \alpha < 360^\circ$ . The capacitor voltage remains constant as soon as diode 11D becomes reverse biased. A capacitor discharge pulse is generated across pulse transformer 2X during the period  $10^\circ < \alpha < 170^\circ$  each time thyristor 1TH fires.

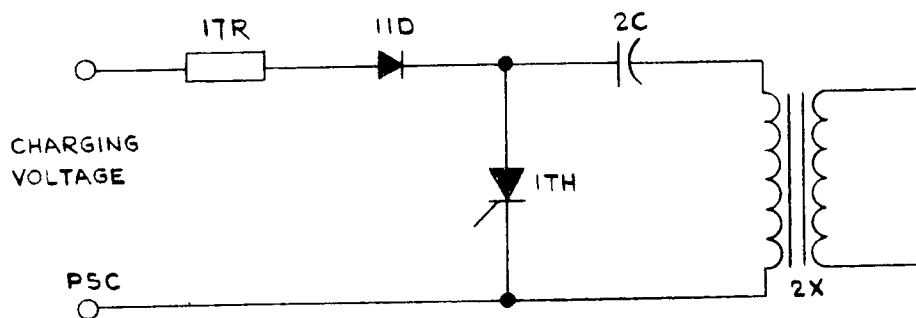


FIGURE 4

2. Double Pulsing - The power converter requires that two thyristors conduct during each commutating period. The circuit described thus far does not meet this requirement--the power converter would never start up because only one thyristor is fired at a time. Also, current could not flow during discontinuous current operation. In order to satisfy the gating requirements of the power converter and to obviate the need for a wide pulse risetime requirement), double pulsing is used. With this scheme, each main thyristor in the TPM is gated twice: first by the GPG section of the same phase as the main thyristor; second,  $60^\circ$  later, by the GPG section of the succeeding phase. The circuitry, which accomplishes this, is the steering diode array shown in Figure 5.

Choosing any pulse transformer, one can see that it is pulsed by a firing circuit of its own color and  $60^\circ$  later by the following firing stage. The dotted lines show the current paths when the thyristor in the red section of the GPG fires; the broken lines show the current paths when the thyristor in the orange section of the GPG fires.

3. Reversing - Note that one side of each pulse transformer primary lead in Figure 5 ties to a common point FD and returns to PSC of the GPG. If this line is broken, pulsing stops. Dual-converter operation is accomplished by using a second TPM with a second set of pulse transformers and steering diodes. The common point of the pulse transformer primaries on the second set is denoted RD and must likewise connect to PSC on the GPG for pulsing to occur. A static reversing switch connects FD to PSC and RD to a large negative pulse-suppressing bias voltage for forward converter operation. These connections are reversed for reverse converter operation. Figure 6 shows the brown, red, and orange pulse distribution circuits with a standard double-pole, double-throw switch symbolizing the static reversing switch.

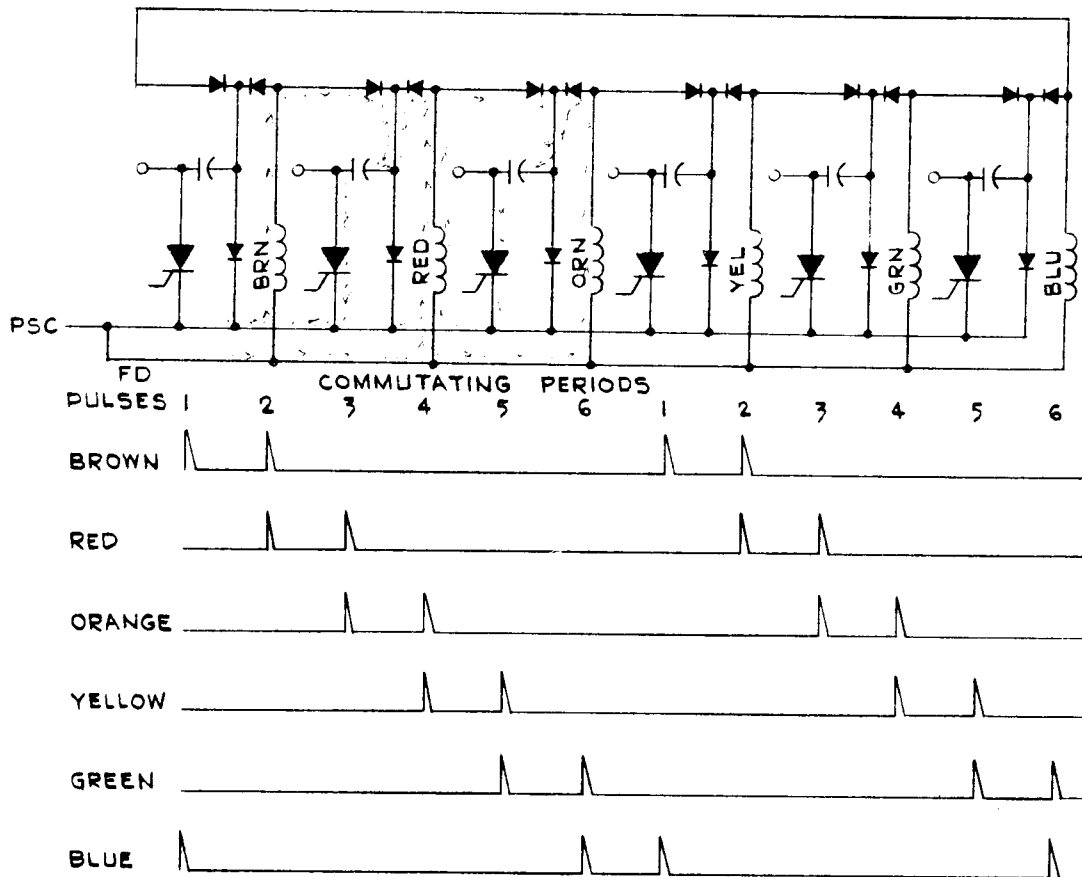


FIGURE 5

Other components in this section for the forward converter are resistor 2R\* which acts as a bleeder for capacitor 2C, diode F-22D which protects the gate-cathode junction of thyristor F-2TH, resistor F-22R which limits the gate pulse current drawn by thyristor F-2TH and capacitor F-22C which in conjunction with F-22R provides noise filtering. Shielded cables are used for pulse transmission between the GPG in the basic regulator cage and the PD mounted on front of the TPM in order to avoid crosstalk and pickup problems. For short runs of pulse-carrying conductors, such as the internal TPM wiring, twisted-pair cables suffice.

### III. TROUBLESHOOTING AND SERVICE

The failures which can occur in the gate control system may be of three types:

- (1) absence of pulse when there should be a pulse,
- (2) presence of pulse when there should not be a pulse, and
- (3) pulse in wrong position.

In each case, using an oscilloscope, the offending board must be localized and a spare inserted in its place. Note that color-coded wiring is used throughout the gate control system to facilitate troubleshooting. The resistor color code assigns the cables to the various pulses one through six. In dual converters, white/color twisted pairs are used for the forward channel and black/color twisted pairs are used for the reverse channel.

\*Refer back to Figure 2.

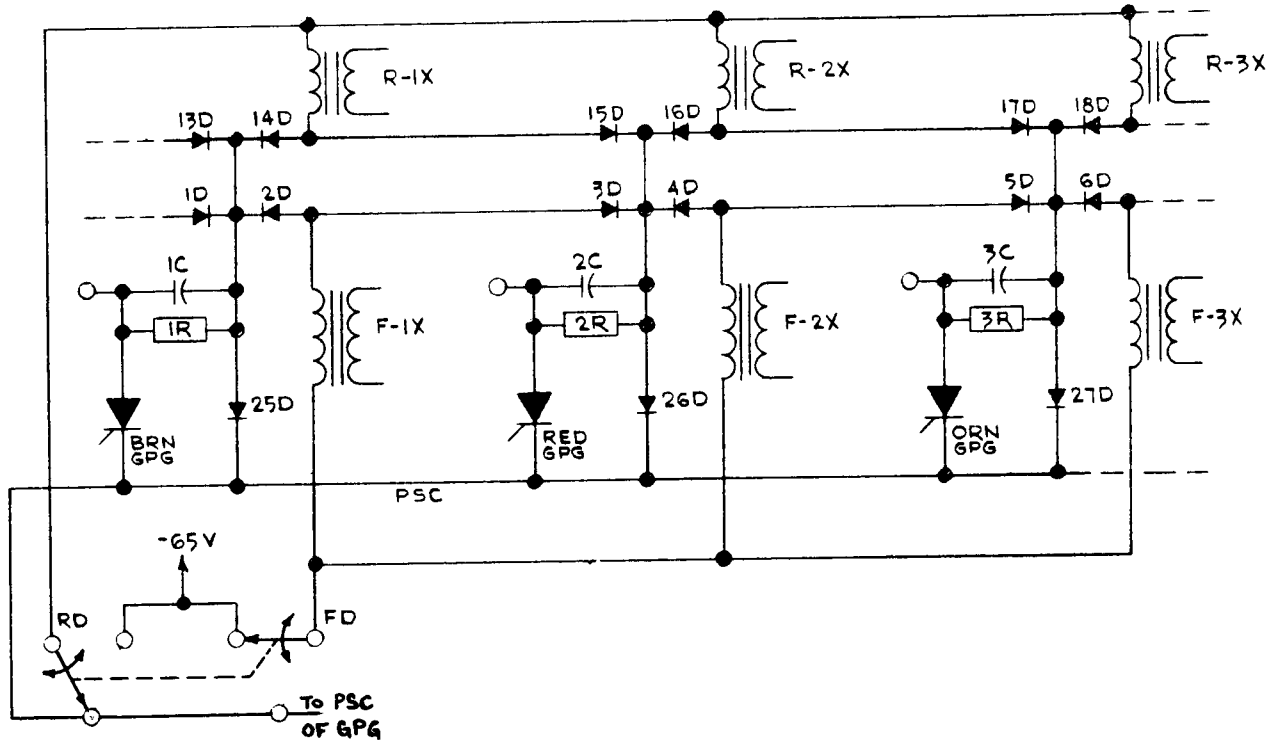


FIGURE 6

Generally, repair is facilitated by returning the faulty board to Westinghouse Electric Corporation, Industrial Systems Divison, P.O. Box 225, Buffalo, New York 14240. Special test equipment must be used to check proper operation of the repaired board.

#### IV. CHARACTERISTICS AND RATINGS FOR GPG (Three Boards S#1326A15 Required)

### A. Power Supply

1. Three-phase, 60 Hz, 460V  $\pm 10\%$  or 230V  $\pm 10\%$ : Use gate control transformer 1295A25G01. Line currents required with the 230-volt connection are less than 125 ma.
2. Three-phase, 50/60 Hz, 380V  $\pm 10\%$  or 550V  $\pm 10\%$ : Use gate control transformer 1295A25G02.

### B. Output

1. Six pulses per cycle accurately spaced  $60^\circ \pm 2^\circ$  apart at  $\alpha = 90^\circ$ .

## Westinghouse Electric Corporation

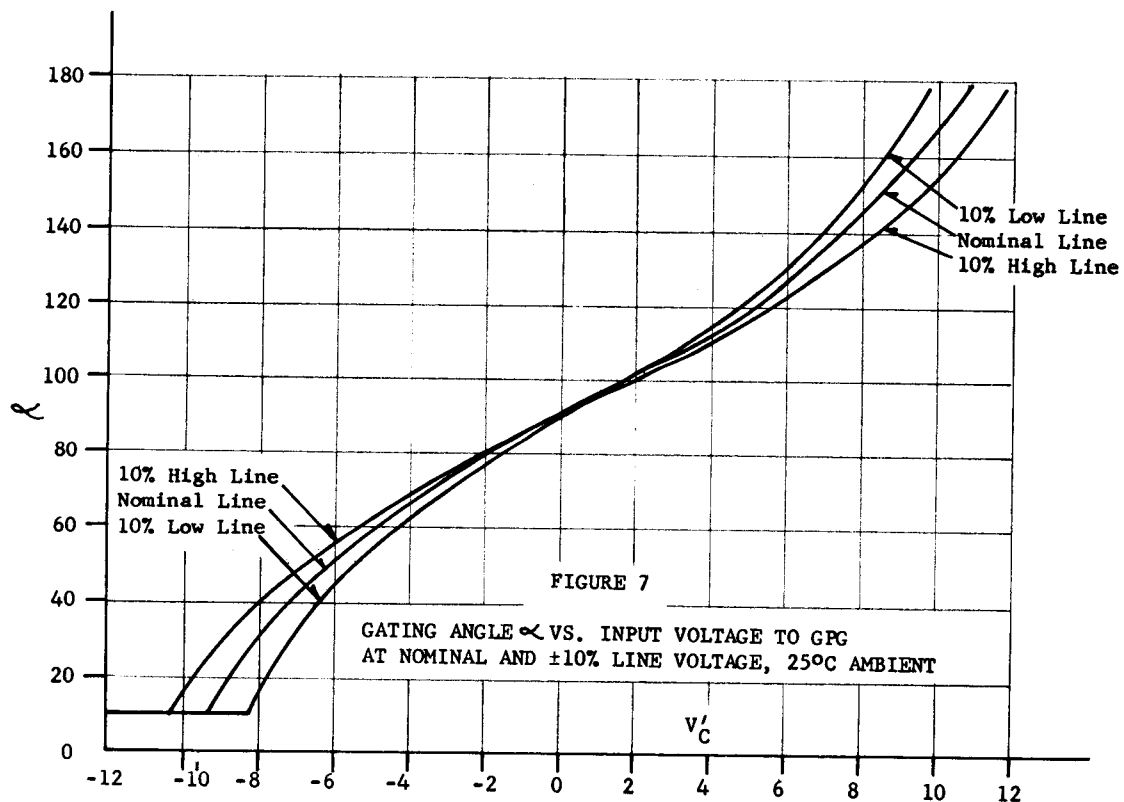
2. The GPG is capable of driving one, two, three, or four pulse distribution (PD) panels in either single converters or dual converters.
3. The pulses have the following characteristics as measured across a dummy load of 8.2 ohm  $\pm 5\%$  connected to the pulse transformer secondary on the PD panel.
  - a. Peak amplitude 12.5 volts minimum.
  - b. Risettime between 10% and 70% of peak voltage, 1 microsecond maximum.
  - c. Pulsewidth at 5 volts, 150 microseconds minimum.

C. Input

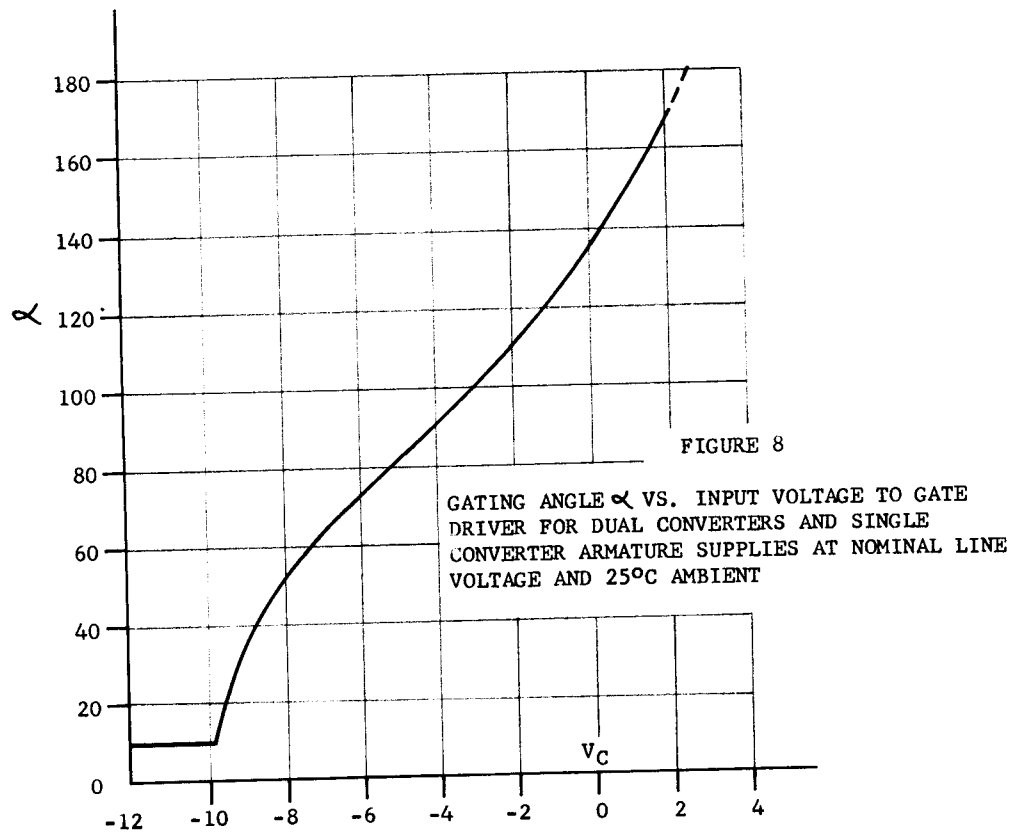
1. Intended to be controlled by the gate driver section of the voltage controller (VC) board or by an operational amplifier having a low output impedance.
2. Typical transfer curves are given in figures 7, 8, and 9.

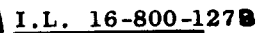
D. Ambient Temperature

0° to 55°C ambient temperature measured at gate pulse generator printed circuit boards.









## I. INTRODUCTION

This material describes the functions of the various circuits. The generation of a typical gate pulse, for example--pulse #2, will be traced from the gate driver input signal  $V_c$  to thyristor #2 in the TPM. It must be recognized that the circuitry described here is contained in several parts of the C-56 regulator and is not a distinct module which could be used unchanged for other applications. It should also be noted that the schematic diagrams presented in this material are not complete and not necessarily up to date. They will, however, serve the instructional purpose intended here.

Figure 1 is a block diagram of the gate control system.



Figure 2 shows the circuitry required for generating pulse #2.

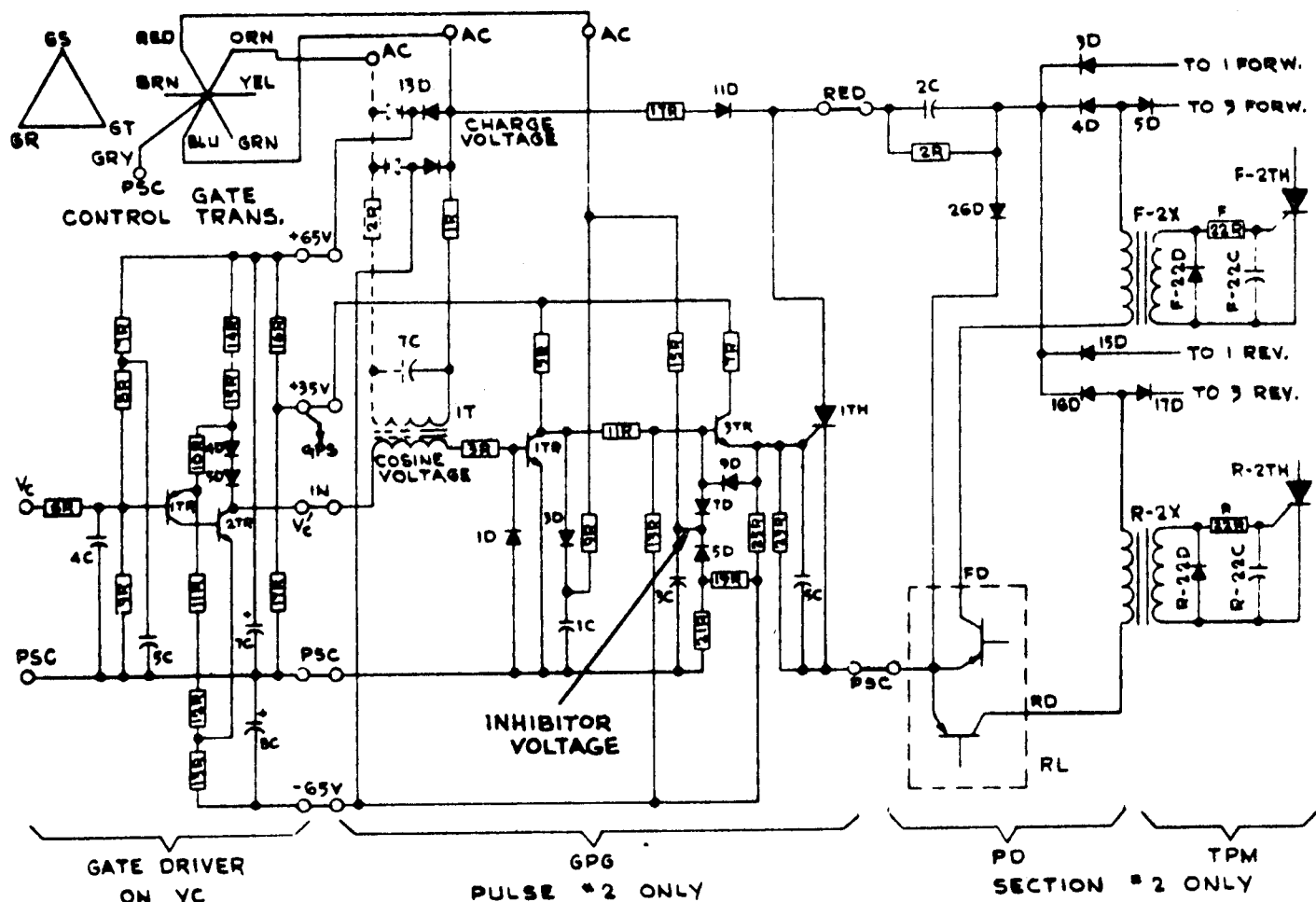


FIGURE 2

#### A. AC and DC Power Supplies

1. Gate Control Transformer has a six-phase, star-connected secondary with each phase-to-centertap voltage approximately 50 volts rms. The primary is a delta for  $\Delta$  -  $\Delta$  thyristor power transformers, and the primary voltage is equal to the line voltage GR-GS-GT. The six sine waves available at the secondary of the gate control transformer are used for inhibiting and charging on the three GPG boards. In addition, the line-to-line voltages available on each leg of the gate control transformer are filtered 60° through components 1R, 2R, and 7C on the GPG and transformed through toroid 1T to approximately 20 volts peak to peak measured between the secondary and centertap.
2. DC Power Supply - The six sine waves from the gate control transformer are also applied to three bridge rectifier combinations 13D on the three GPG boards producing a positive and negative 65-volt supply. These dc potentials are slightly filtered on the VC panel by capacitors 7C and 8C; a lower voltage, approximately 35 volts, is produced by the voltage divider consisting of resistors 16R and 17R on panel VC. During gate pulse suppression, this 35-volt potential is shorted to PSC.

## B. Gate Driver

This circuit consists of a 100  $\mu$ sec. filter (6R and 4C on VC), an input network, and a gain-of-two amplifier.

1. Input Network - The circuit consisting of 7R, 8R, 9R, and 5C on VC provides two functions:
  - a. A filtered bias, which for zero-volts input to the GD, provides a GD output voltage of approximately:
    - (1) for dual converters and single-converter armature supplies: 7 volts.
    - (2) for single-converter field supplies: 0.7 volts.
  - b. An attenuation of approximately:
    - (1) for dual converters and single-converter armature supplies: 0.8.
    - (2) for single converter field supplies: 0.5.
  - c. A gating angle retardation limit of approximately  $155^\circ$  for single-converter field supplies.
2. Gain of Two Amplifier - This feedback amplifier compares the input voltage on the base of transistor 1TR with the feedback voltage obtained at the junction of resistors 10R and 11R. The error signal is amplified by the current gains of transistors 1TR and 2TR. Diodes 4D and 5D provide temperature compensation for the base-emitter junction of transistor 1TR. The remaining resistors and capacitors in the circuit set dc bias conditions for the transistors.

## C. Gate Pulse Generator

The GPG is fed by three sine waves, an input signal  $V_c'$ , and a dc collector supply voltage of approximately 35 volts.

1. AC Power Supply - Figure 3 shows the phase relationship between the cosine voltage, the charging voltage, and the inhibiting voltage. The half cycles during which each sine wave acts is shown solid, while the inactive portion is dotted.

The gating angle,  $\alpha$ , is measured from the point when the anode voltage on the main thyristor first goes positive. Pulsing is restricted to approximately  $10^\circ < \alpha < 170^\circ$  for dual converters and single-converter armature supplies, &  $10^\circ < \alpha < 155^\circ$  for single-converter field supplies. The point  $\alpha = 155^\circ$  is referred to as the gating angle retardation limit.

The cosine voltage, as explained above, is obtained from the  $60^\circ$  filter consisting of 1R, 2R, and 7C. The position of the inhibitor is set by components 9R, 1C, 15R, and 3C. The charging voltage is limited by resistor 17R. Diodes 3D, 7D, 5D, 9D, and 11D determine the active portions of the inhibitor and charge voltages respectively.
2. Circuit Operation - At the point in time when the algebraic sum of the input voltage to the GPG,  $V_c'$ , and the cosine voltage cross zero volts in the range  $10^\circ < \alpha < 170^\circ$ , transistor switch 1TR shuts off, causing a positive voltage to appear on the collector. This voltage appears at a reduced value on the base of transistor switch 3TR causing the latter

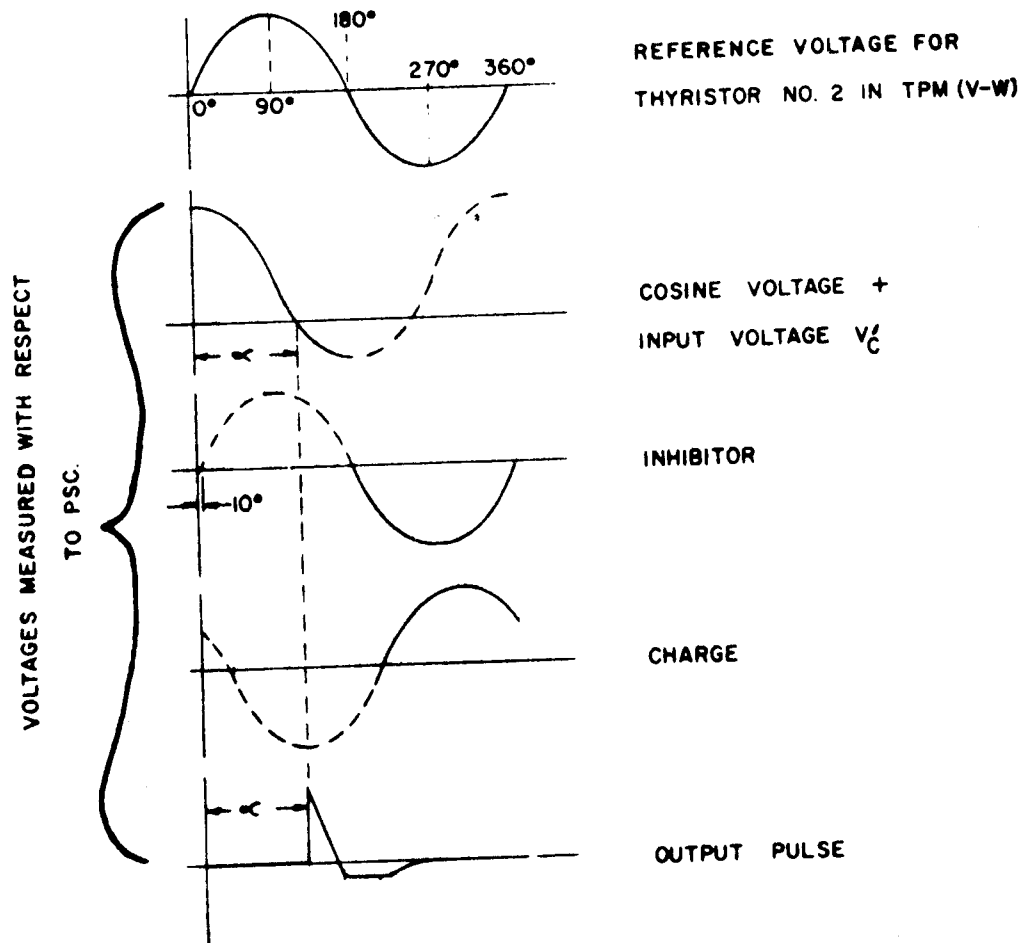


FIGURE 3

to turn on. The emitter-follower action of transistor 3TR causes 1TH to fire. Capacitor 2C on the PD board discharges causing a pulse to appear across the pulse transformer F-2X on the TPM.

During the period  $180^\circ < \alpha < 370^\circ$ , pulsing must not occur. This is accomplished by the inhibitor which pulls the collector of 1TR negative through diode 3D regardless of the signal on the base of the transistor. At the same time, turn off of the thyristor (silicon-controlled switch) is insured by pulling the gate of 1TH negative to approximately -3 volts through diode 5D and voltage divider 15R and 25R. Other components on the GPG board set dc bias levels for transistors, protect base-emitter and gate-cathode junctions, and provide noise filtering.

#### D. Pulse Distributor

1. Capacitor Discharge Circuit - The pulse generation circuit on the GPG boards and the PD board could be simplified as in Figure 4 and then would generate a single pulse each cycle. In Figure 4, the charging voltage

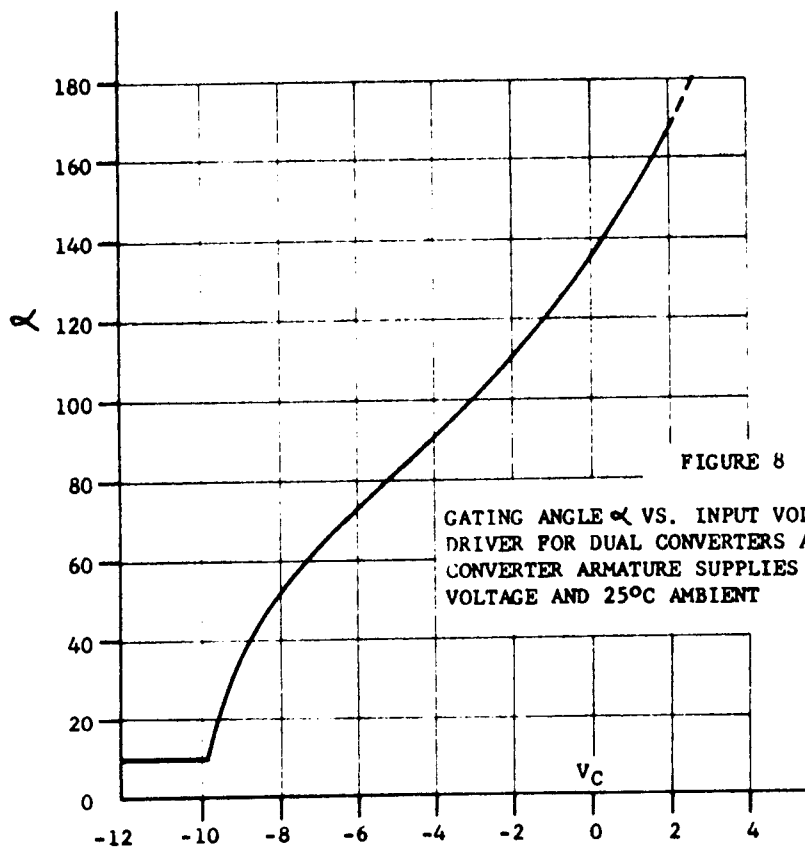


FIGURE 8

GATING ANGLE  $\alpha$  VS. INPUT VOLTAGE TO GATE  
DRIVER FOR DUAL CONVERTERS AND SINGLE  
CONVERTER ARMATURE SUPPLIES AT NOMINAL LINE  
VOLTAGE AND 25°C AMBIENT

