



INPUT ISOLATION BOARD

S#1640A29

I. INTRODUCTION

This card contains six circuits, each of which serves as an attenuator, isolator and filter for coupling external high level logic signals into 5 or 15 volt controllers. The input signals are the presence or absence of some defined AC or DC voltage. These signals usually indicate an open or closed contact on some external device.

Table 1 shows the input voltages which can be used with the different styles of this card, as well as the logic type into which each style interfaces. The operate times for each style are also given.

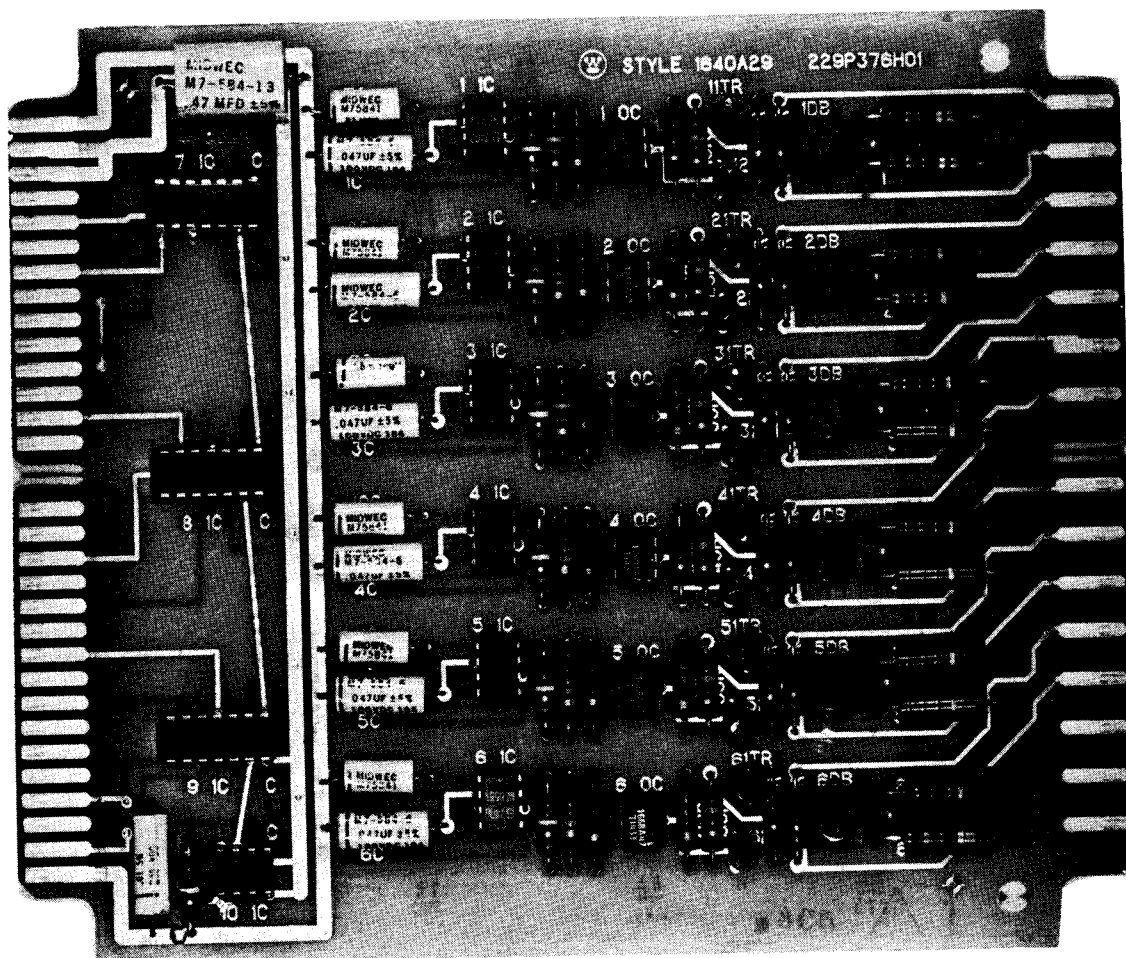


FIGURE 1

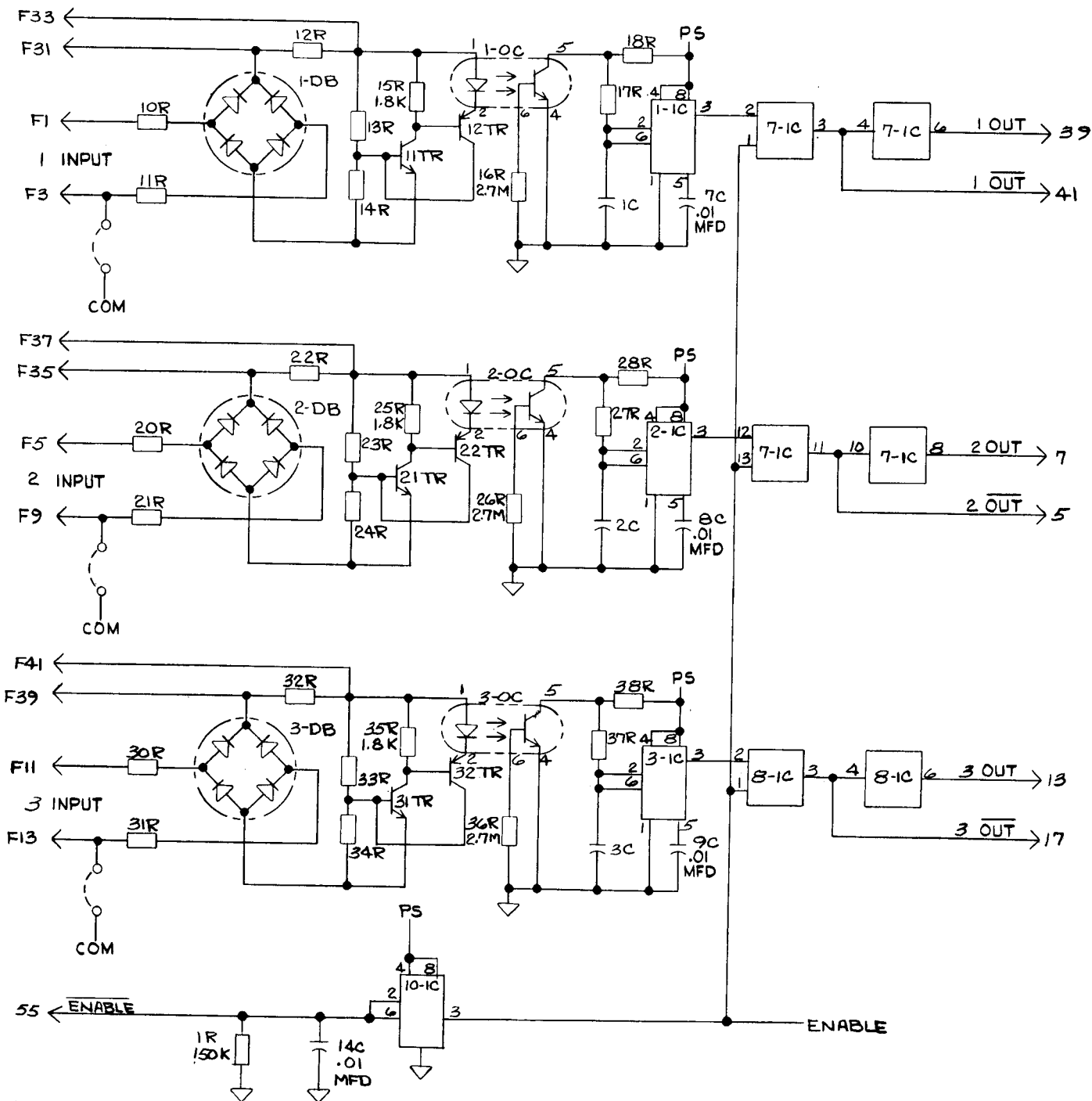


FIG. 2(a)

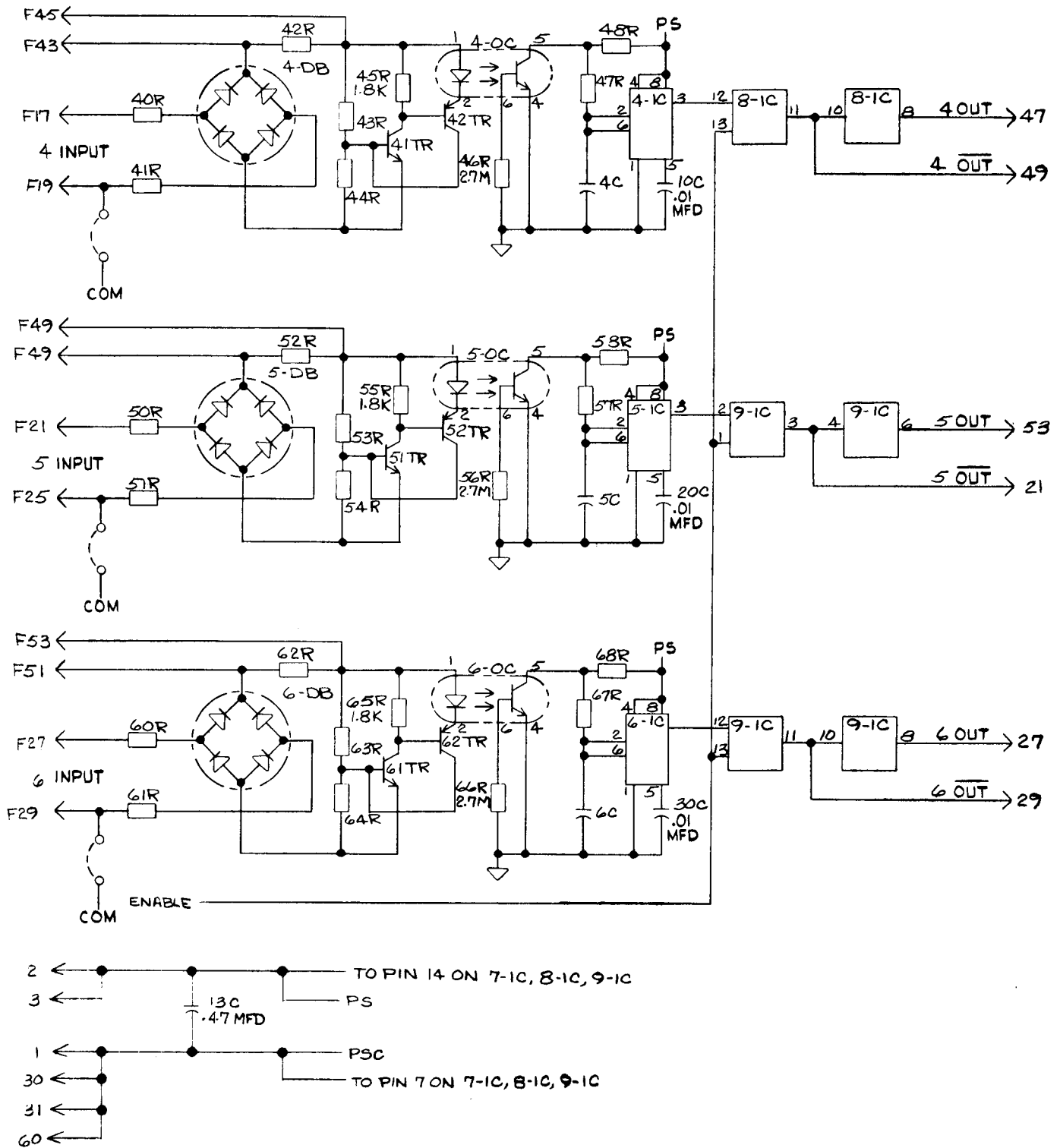


FIG. 2(b)

II. APPLICATION INFORMATION

	INPUT VOLTAGE	LOGIC POWER SUPPLY VOLTAGE	OPERATE TIMES (MILLISECONDS, TYPICAL)		ONE SIDE OF INPUTS CONNECTED TOGETHER	INPUT CURRENT (ma)
			PICKUP	DROPOUT		
G01	110 VAC $\pm 25\%$ 110 VDC $\pm 20\%$	5 VDC $\pm 10\%$	4 - 8 4	11 - 15 15	No	8 $\pm 25\%$ 8 $\pm 20\%$
G02	20 - 60 VDC	5 VDC $\pm 10\%$	0.7	1.2	No	4 - 15
G03	110 VAC $\pm 25\%$ 110 VDC $\pm 20\%$	12 - 16 VDC	4 - 8 4	11 - 15 15	No	8 $\pm 25\%$ 8 $\pm 25\%$
G04	11 - 28 VDC	5 VDC $\pm 10\%$	0.7	1.2	No	6 - 21
G05	20 - 50 VAC 20 - 60 VDC	5 VDC $\pm 10\%$	4 - 8 4	11 - 15 15	No	4 - 13 4 - 15
G06	20 - 50 VDC 20 - 60 VDC	12 - 16 VDC	4 - 8 4	11 - 15 15	No	4 - 13 4 - 15
G07	20 - 60 VDC	12 - 16 VDC	0.7	1.2	No	4 - 15
G08	110 VAC $\pm 25\%$ 110 VDC $\pm 20\%$	5 VDC $\pm 10\%$	4 - 8 4	11 - 15 15	Yes	8 $\pm 25\%$ 8 $\pm 20\%$
G09	110 VAC $\pm 25\%$ 110 VDC $\pm 20\%$	15 VDC $\pm 10\%$	4 - 8 4	11 - 15 15	Yes	8 $\pm 25\%$ 8 $\pm 20\%$

TABLE 1

When an input voltage within the defined voltage range is present at the input terminals, the OUT terminal is a LOGIC 1 (high level) and the $\overline{\text{OUT}}$ terminal is a LOGIC 0 (low level). If the input voltage is not present, or if the $\overline{\text{ENABLE}}$ input is at a LOGIC 1, or both, then the OUT terminal is a LOGIC 0 and the $\overline{\text{OUT}}$ terminal is a LOGIC 1. See definitions of LOGIC 0 and LOGIC 1 below.

The circuit ignores all input voltages below a threshold level, typically 1/2 of the nominal input voltage.

Power Supply Current: G01, G02, G04, G05, G08: 5VDC \pm 40 ma
(typical)
G03, G06, G07 15VDC \pm 100 ma.

Logic Loading: Each OUT terminal will drive 8 logic loads.

Each $\overline{\text{OUT}}$ terminal will drive 7 logic loads.

The $\overline{\text{ENABLE}}$ input should be considered 1 logic load. If left unconnected, this input assumes the low (LOGIC 0) state.

The above logic loads refer to DTL loads(5volt logic) or HTL loads (15 volt logic).

The inputs card can also be used to interface with CMOS circuits.

Logic Level Definitions:

	<u>G01,G02,G04,G05,G08</u>	<u>G03,G06,G07</u>
A logic 1 state is defined as:	+5.5V to +2.6V	+16V to +12.5V
A logic 0 state is defined as:	0.0V to +0.5V	0.0V to +1.5V

I. DESCRIPTION OF OPERATION

Refer to the first of the six inputs shown in the scheme (top of Figure 2(a)).

In order to get a LOGIC 1 signal on the 1 OUT terminal 39, a voltage as defined in Table 1 must be applied across the INPUT terminals F1 and F3 (terminals with F prefixes are located on the front edge of the board, away from the backplane). If the applied input is an AC voltage, the signal is rectified by the diode bridge 1-DB. A visible light-emitting diode (VLED) is typically connected between terminals 31 and 33, anode on 31, and the rectified input current (as limited by resistors 10R and 11R) flows through the VLED, through 12R and through the voltage divider 13R and 14R. Whenever sufficient current flows to raise the voltage across 14R to approximately 0.6 volts, 11TR turns on which turns on 12TR and causes current to flow in the infra-red light-emitting diode (IR LED) of the coupler. Current flowing in the IR LED causes the phototransistor to conduct current, which discharges capacitor 1C through 17R. When the voltage across 1C drops to 1.7 volts, the output of timer 1-IC (pin 3) rises to a high state, giving a LOGIC 0 output on terminal 41 ($\overline{\text{1 OUT}}$) and a LOGIC 1 output on terminal 39 (1 OUT). With AC inputs, current in the optical coupler is derived from the rectified but unfiltered sine-wave input voltage. The current in the phototransistor is therefore pulsing at 120 hz (for 60 hz inputs). During the time when current in the phototransistor is off, 1C begins to charge. But the charging time constant $\tau = (17R + 18R) \times 1C$ is approximately 10msec., so the capacitor does not charge to a very high voltage before it is discharged again through the phototransistor at the next half-cycle of the input current. Only when the input voltage is removed does 1C charge to the 3.4 volt threshold voltage of the timer 1-IC. At this time the outputs change back to their initial states. The capacitor stays charged to about 4 to 5 VDC until the next time the input voltage is present.

When the $\overline{\text{ENABLE}}$ input is driven to the LOGIC 1 state, all six circuits are inhibited so that the OUT terminals become LOGIC 0 and the $\overline{\text{OUT}}$ terminals become LOGIC 1, regardless of the presence or absence of voltage on the individual inputs.

IV. SERVICE

Personnel familiar with electrical equipment utilizing semiconductors can isolate most problems using an oscilloscope, multimeter, and information contained in relative instruction leaflets.

Semi-automatic equipment is available at the factory to test static and dynamic performance of all edge-connected, printed circuit boards. Generally, repair of boards is facilitated by returning them to :

Westinghouse Electric Corporation
Industrial Equipment Division
P. O. Box 225
Buffalo, New York 14240

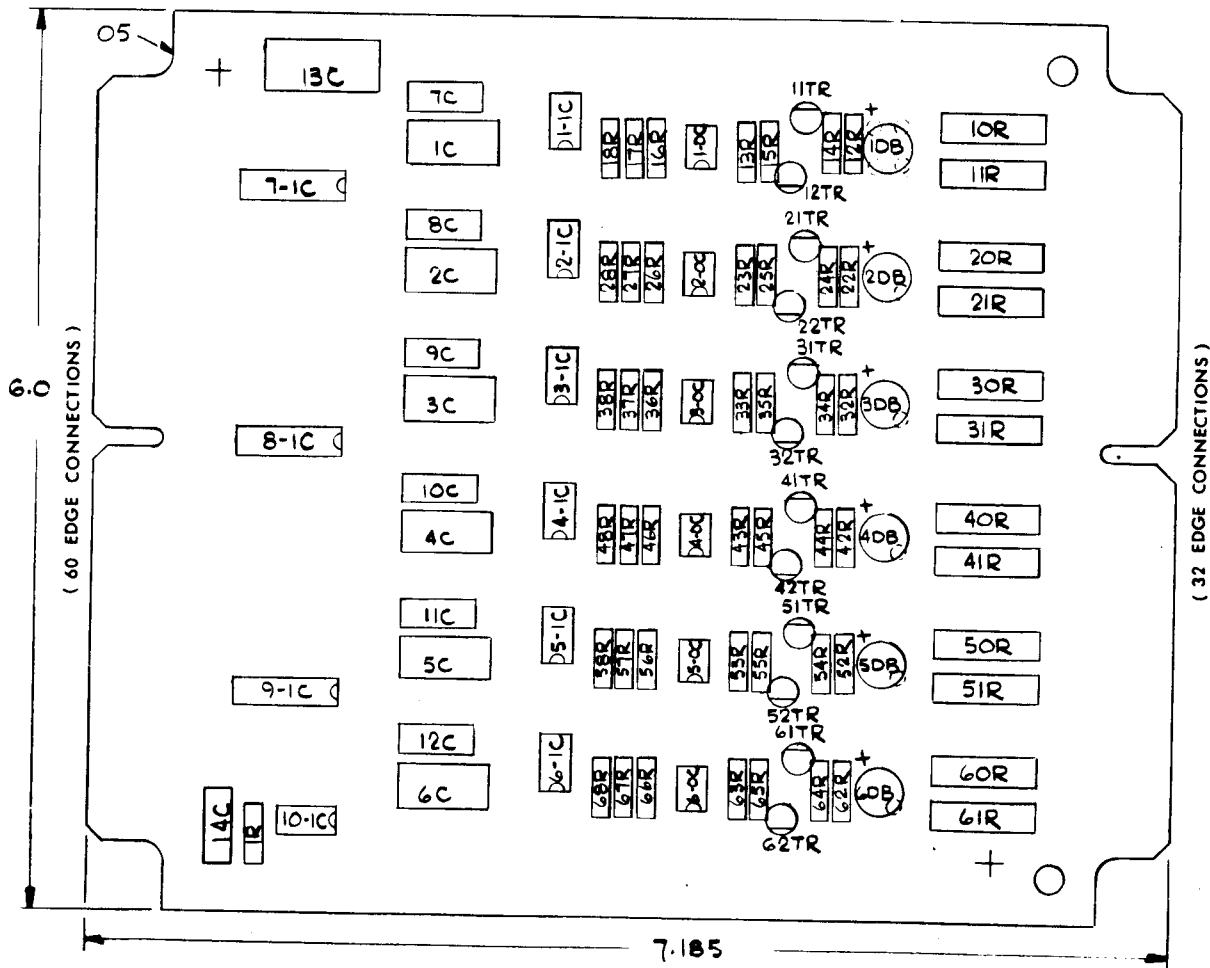


FIGURE 4