GATE CONTROLLER

I. INTRODUCTION

The F80 controller cards are used to provide phase control of a single phase F80 field exciter TPM in either a single converter or a dual converter configuration. The basic F80 cards include the Gate Selector and Driver S#1725A08, the Gate Controller S#1725A09 and the Bank Selector (used only in the dual converter applications) S#1725A10 for field voltage loop, S#1736A33 for field current loop.

The Gate Controller, GC, card performs the following functions:

1. Synchronization with line voltage.
2. Determination of α as a function of an error signal.
3. Current Control - Field.; Voltage Control-Field; Signal Inversion
4. Field loss or over excitation (optional).

Figure 1 is a picture of the GC. A front view locating all components by schematic identification is shown on the last page of the instruction leaflet. NOTE: Drawing 1725A09 is a multi-group assembly and some components will be missing from some style number pc boards.

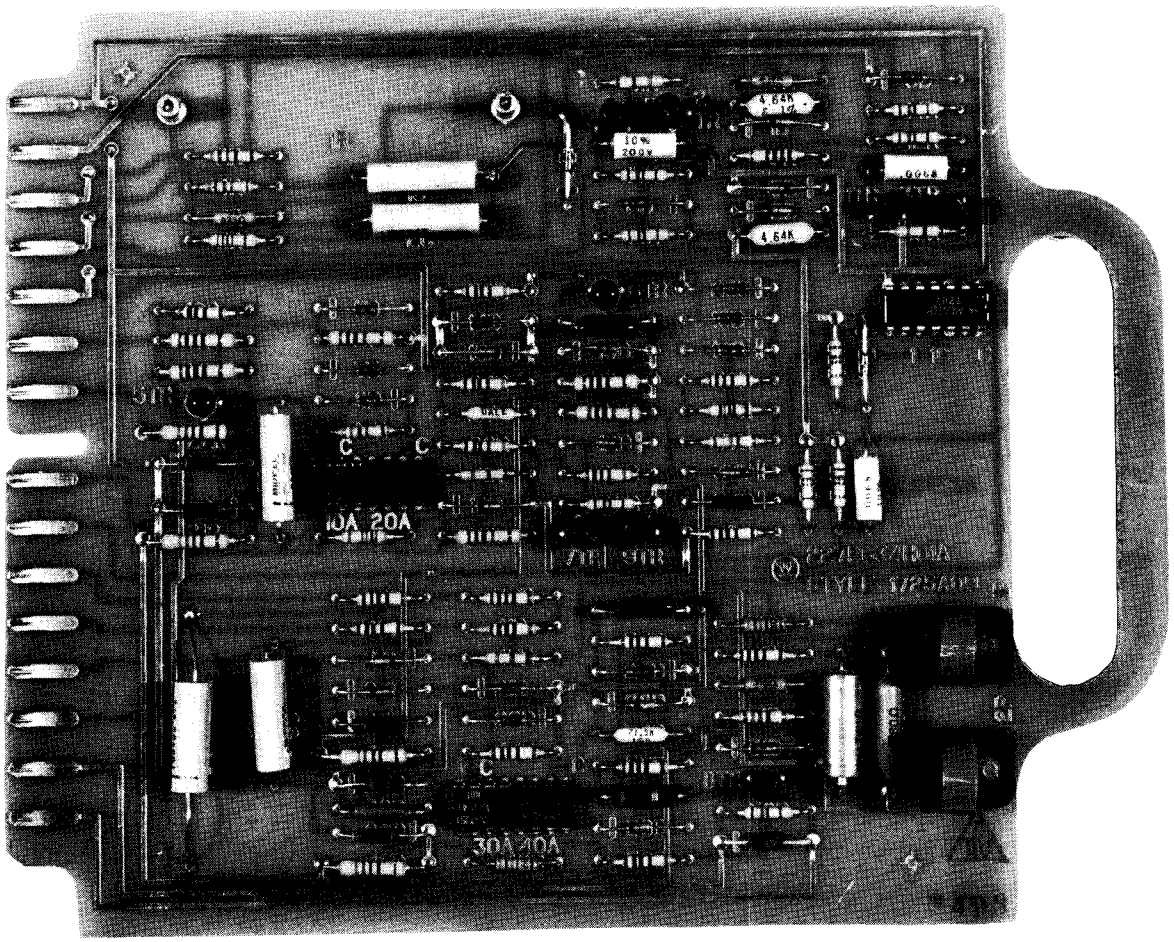

FIGURE 1

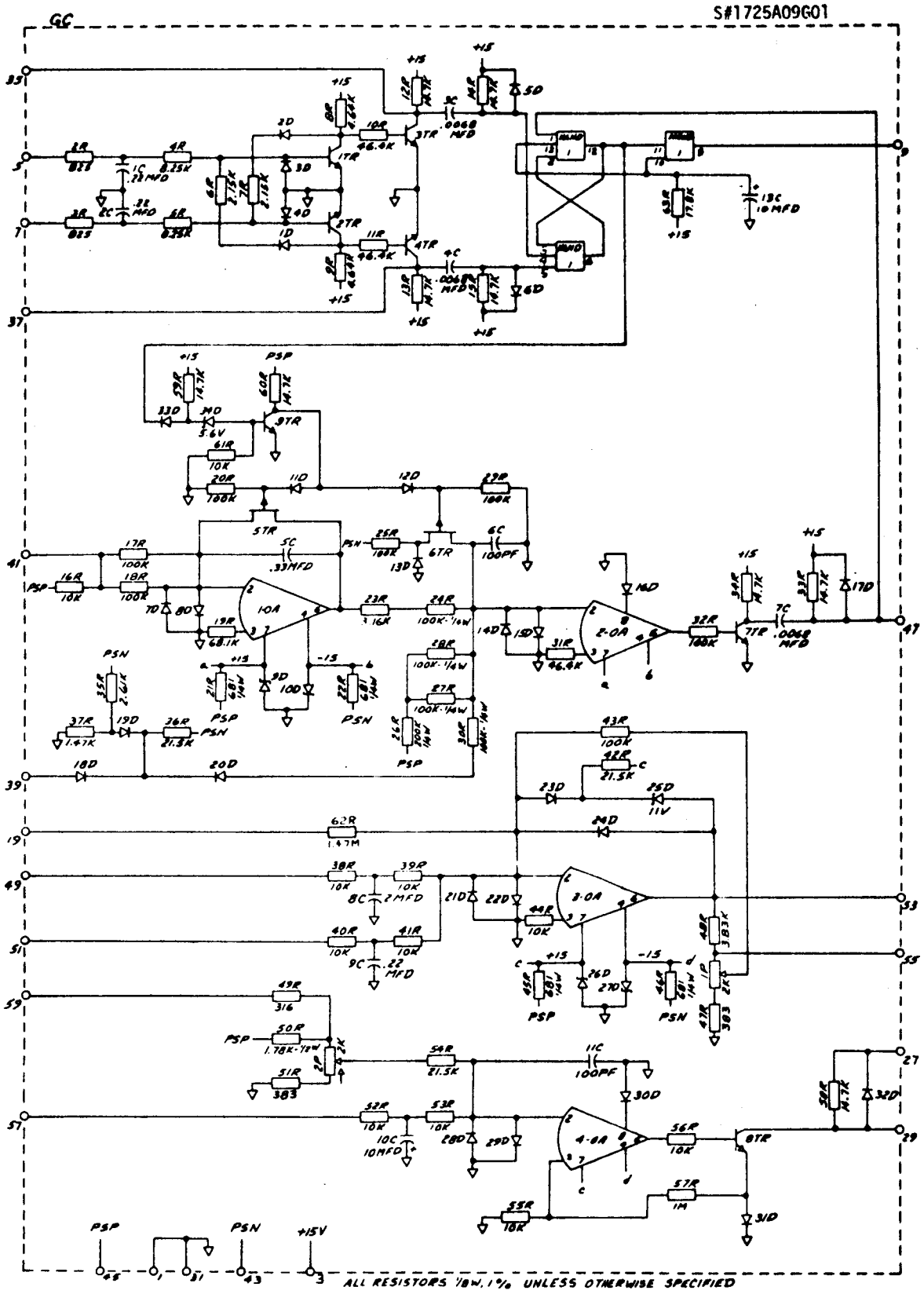
S#1725A09G01
GC
ALL RESISTORS 1/8W, 1% UNLESS OTHERWISE SPECIFIED

FIGURE 2

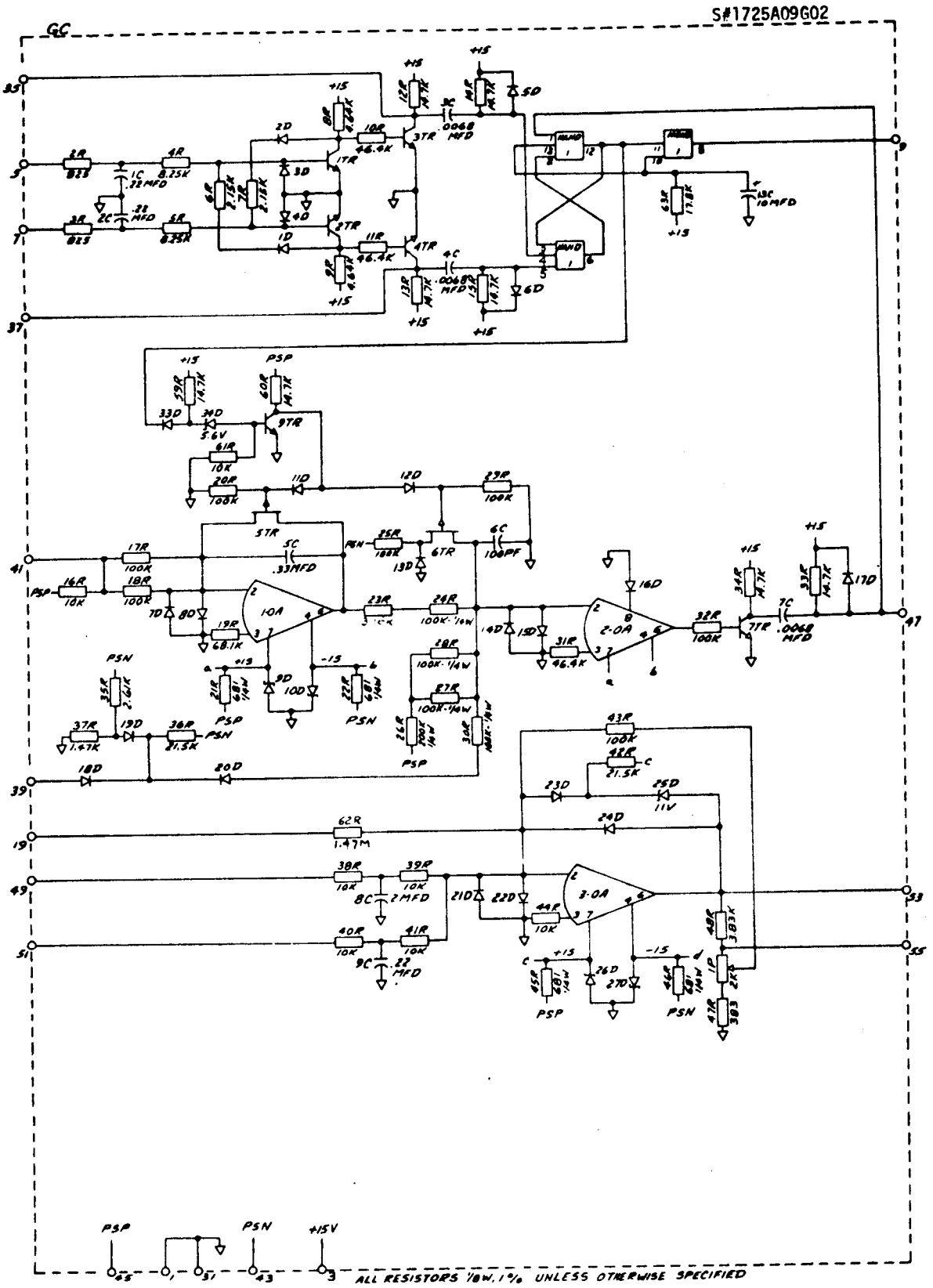
S#1725A09G02
GC
ALL RESISTORS 1/8W, 1% UNLESS OTHERWISE SPECIFIED
PSP
PSN
+15V

FIGURE 3

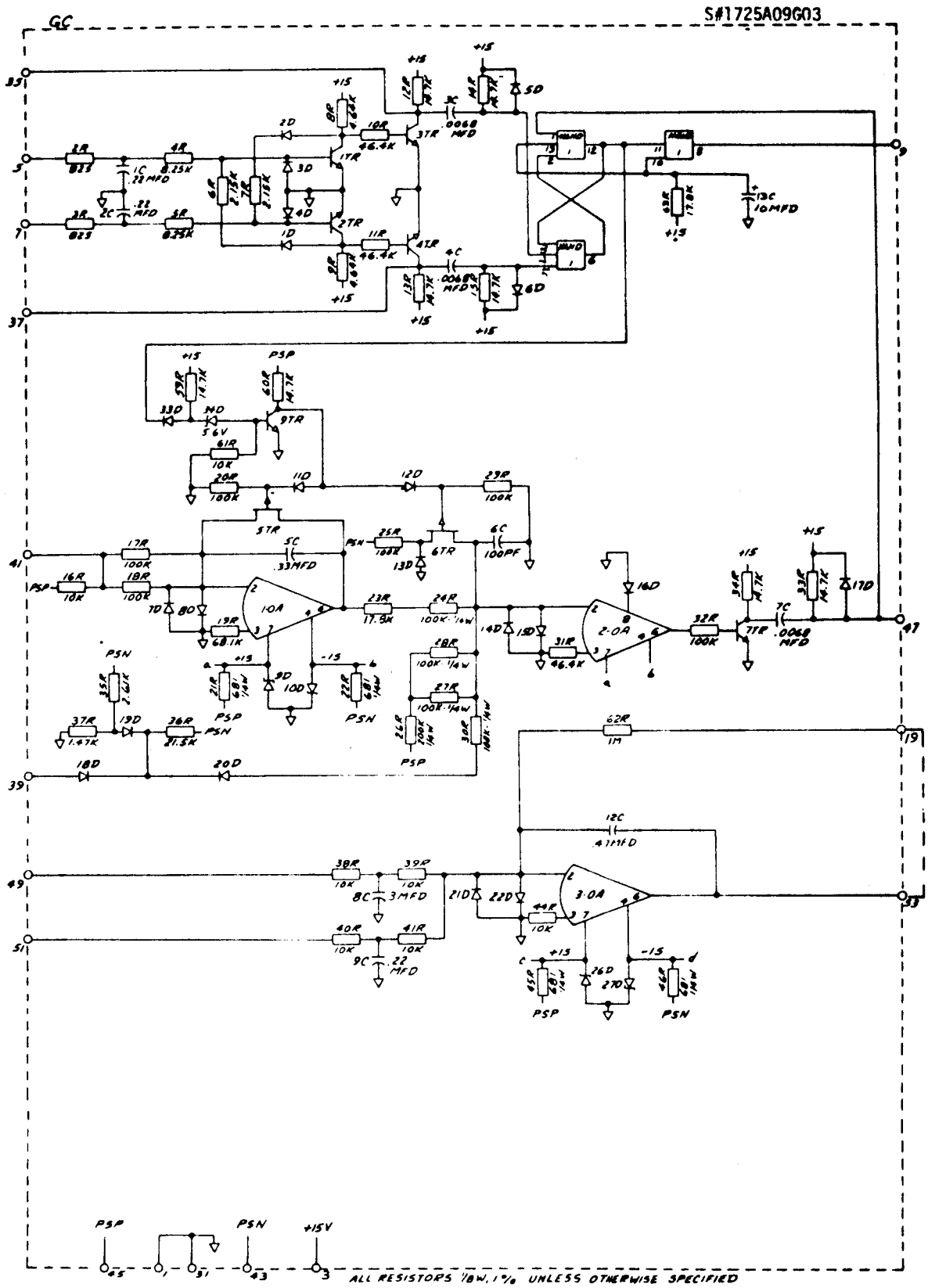
GC
S#1725A09G03
ALL RESISTORS 1/8W, 1% UNLESS OTHERWISE SPECIFIED

FIGURE 4

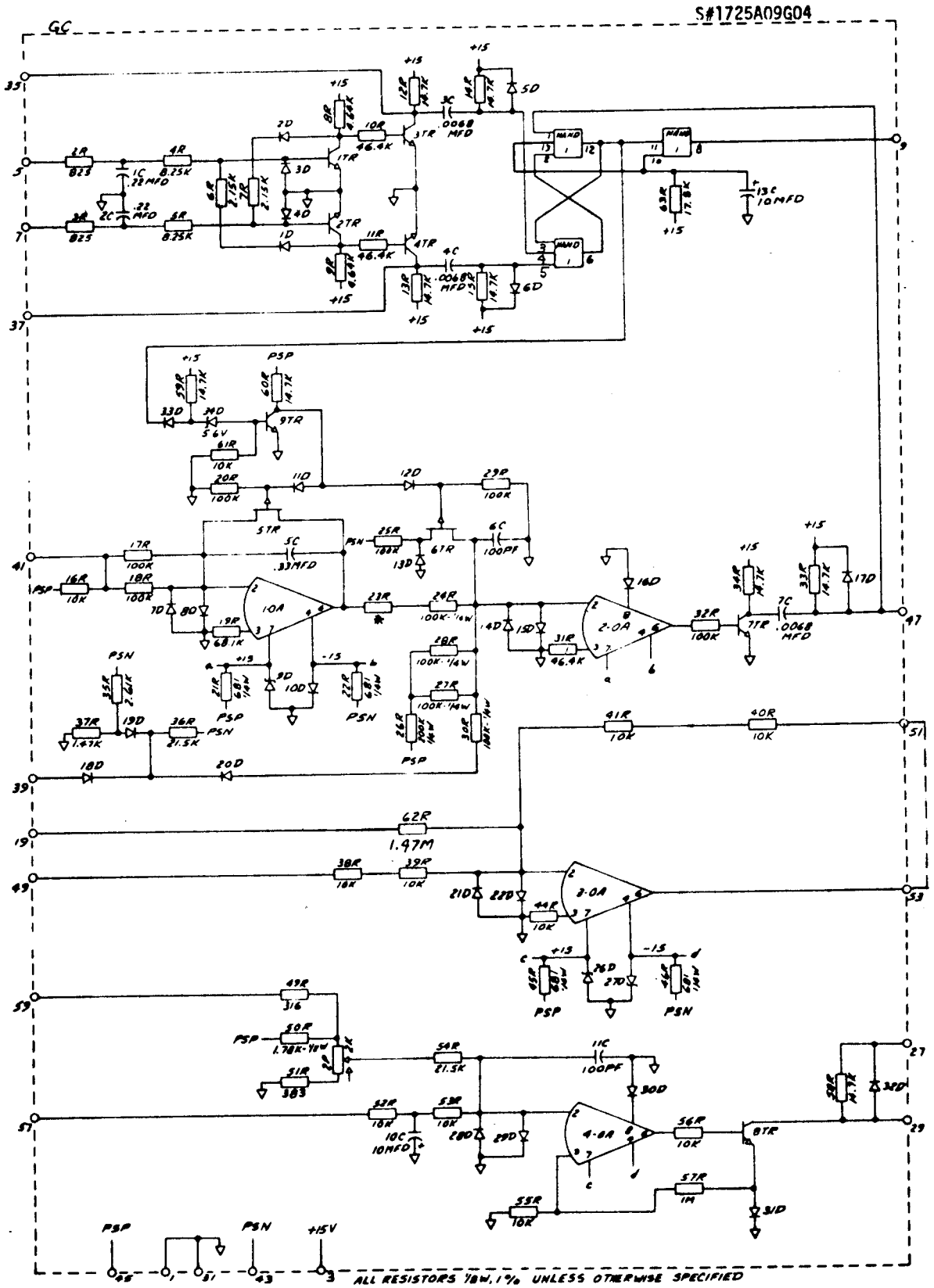

FIGURE 5

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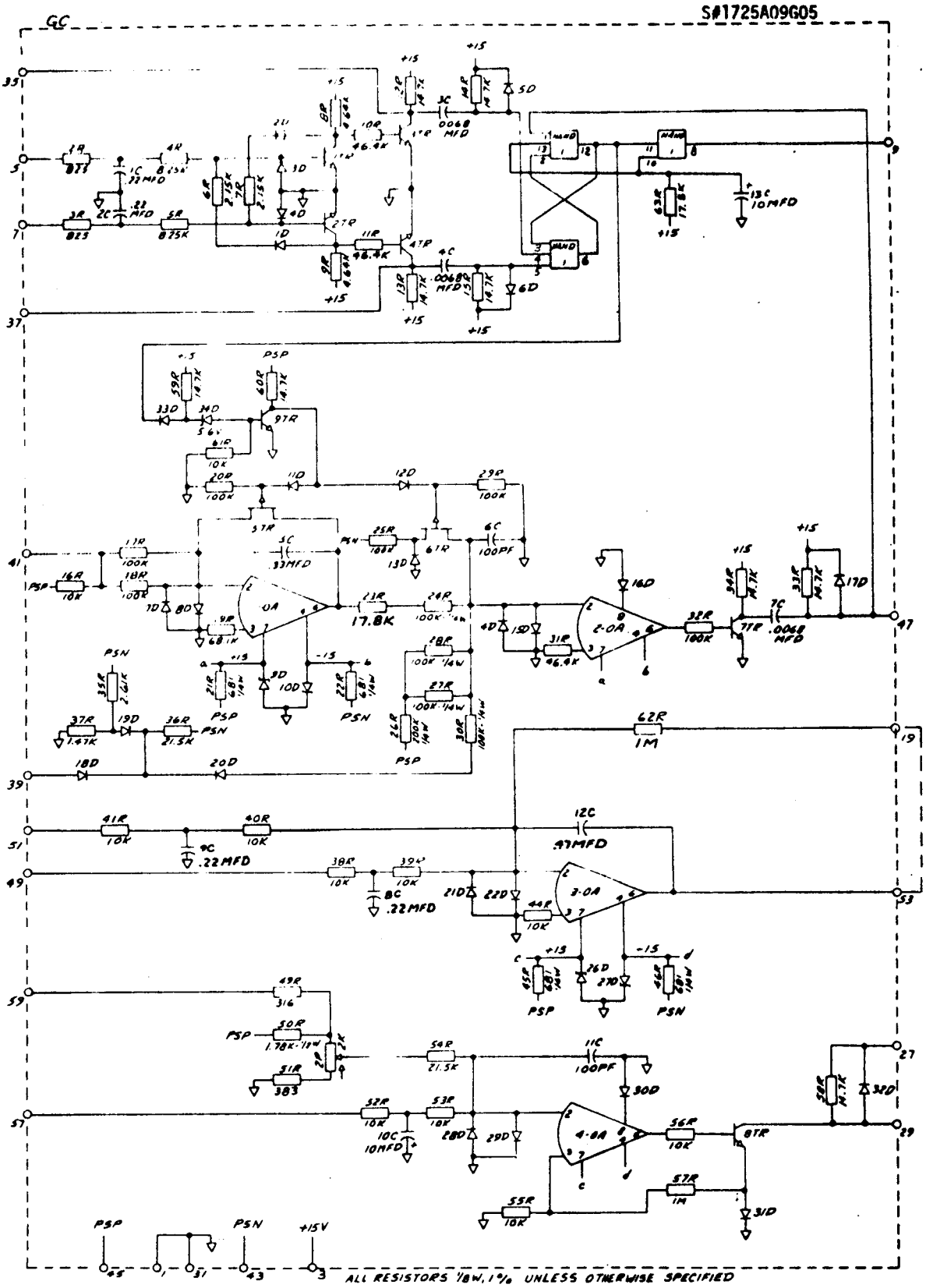

GC
S#1725A09G05
ALL RESISTORS 1/8W, 1% UNLESS OTHERWISE SPECIFIED
PSP
PSN
+15V

FIGURE 6

II. DESCRIPTION OF OPERATION

A. Introduction

The Gate Controller is an interface board which provides coordination for the correct firing of thyristors on the TPM assembly and which translates an error signal into a gating angle position. The generated outputs from this card are used in the Gate Selector and Driver card for gate selection and pulse train generation.

B. Circuit Functionalization (Refer to Figures 2 THROUGH 6)

AC synchronization signals are applied to terminals 5 and 7 of this card from a transformer mounted on the TPM assembly. The secondary of the transformer is center tapped with the center tap tied to terminal 31 (PSC) of the GC card. When the TPM AC voltage U-V is positive, terminal 5 should be positive and terminal 7 should be negative with respect to PSC.

The circuitry of 1TR through 4TR performs the zero crossover function and provides appropriate enables to the GS & D card. Input noise filtering and base-emitter transistor drops generate a delay of approximately 6^{o} in this circuit. 6^{o} after terminal 5 goes positive and terminal 7 goes negative, the logic signals on terminal 35 will change from a "0" to a "1" and on terminal 37 will change from a "1" to a "0". 180^{o} later (6^{o} after U-V goes negative), the logic signals will reverse. The crossover circuit has been designed so that commutation notches in the synchronizing waveform do not effect the status of the circuitry.

1-OA and its associated components form a ramp generation circuit which generates a negative ramp output each half cycle starting from zero volts and ramping negatively at a preset rate. The terminal 41 connection is used to adjust for 50 or 60 hertz base frequency. If the system is operated with 50 hertz AC, terminal 41 should be left open. If the system is operated with 60 hertz AC, terminal 41 should be tied to PSP.

2-OA and its associated components form a comparator circuit. The error signal, zero volts or negative, is applied to terminal 39. This signal, the ramp signal, and a positive fixed bias are compared in this stage for the generation of clock pulses at the desired α point.

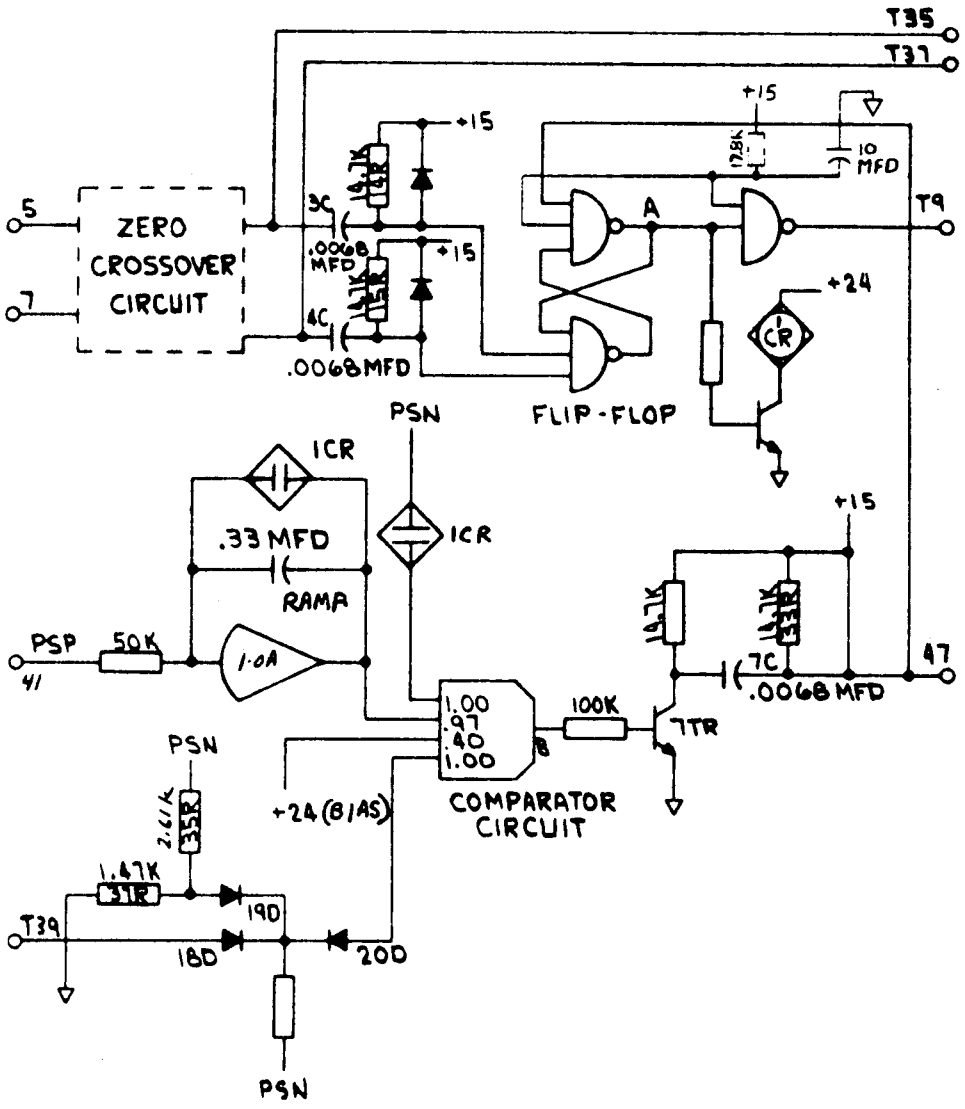
C. Circuit Operation

The functioning of the zero crossover circuit, a flip-flop, the ramp circuit and the comparator circuit are all interrelated. Their operation will be discussed with reference to the simplified schematic of Figure 7

As a starting point, assume that terminal 5 is negative and terminal 7 is positive with terminal 35 being a "0" and terminal 37 a "1". Assume also that the flip flop is in a state such that A is a "1" and, hence, terminal 9 is a zero. While terminal 9 is a zero, clock pulses are amplified in a selected driver on the Gate Selector and Driver card. With A being "1", static relay 1CR should be energized causing the ramp circuit to be reset and injecting a negative input to the comparator maintaining the output signal line B in the "1" state.

When terminal 5 changes from a negative to a positive signal, and terminal 7 changes from a positive to a negative signal, the crossover circuit switches terminal 35 to the "1" state and terminal 37 to the "0" state. The negative transition of the signal on terminal 37 is differentiated (4C & 15R) and used to change the state of the flip flop so that A is a "0", terminal 9 is a "1" and 1CR is de-energized. With 1CR de-energized, the maintaining signal into the comparator is removed and its output B goes from a "1" to a "0"; and, in addition, the ramp circuit is allowed to generate a negative ramp.

The ramp signal increases negatively at a preset rate. The comparator checks the net polarity of the ramp signal, the bias signal, and the error signal on terminal 39. When the net input to the comparator is negative, the output state (B) changes from a "0" to a "1" and transistor 7TR turns on. The negative collector signal is differentiated and applied to T_{47} and the flip flop. The signal on terminal 47 is a short duration, negative going (1 to 0) pulse which is used as the first pulse in the gate pulse train. This negative pulse changes the state of the flip flop so that A is a "1", terminal 9 is a "0", and 1CR energizes. When terminal 9 is a "0", appropriate NANDS on the GS & D card are enabled to pass the first pulse and subsequent clock pulses. When 1CR energizes, the ramp circuit is reset and a signal is injected into the comparator maintaining B in the "1" state.



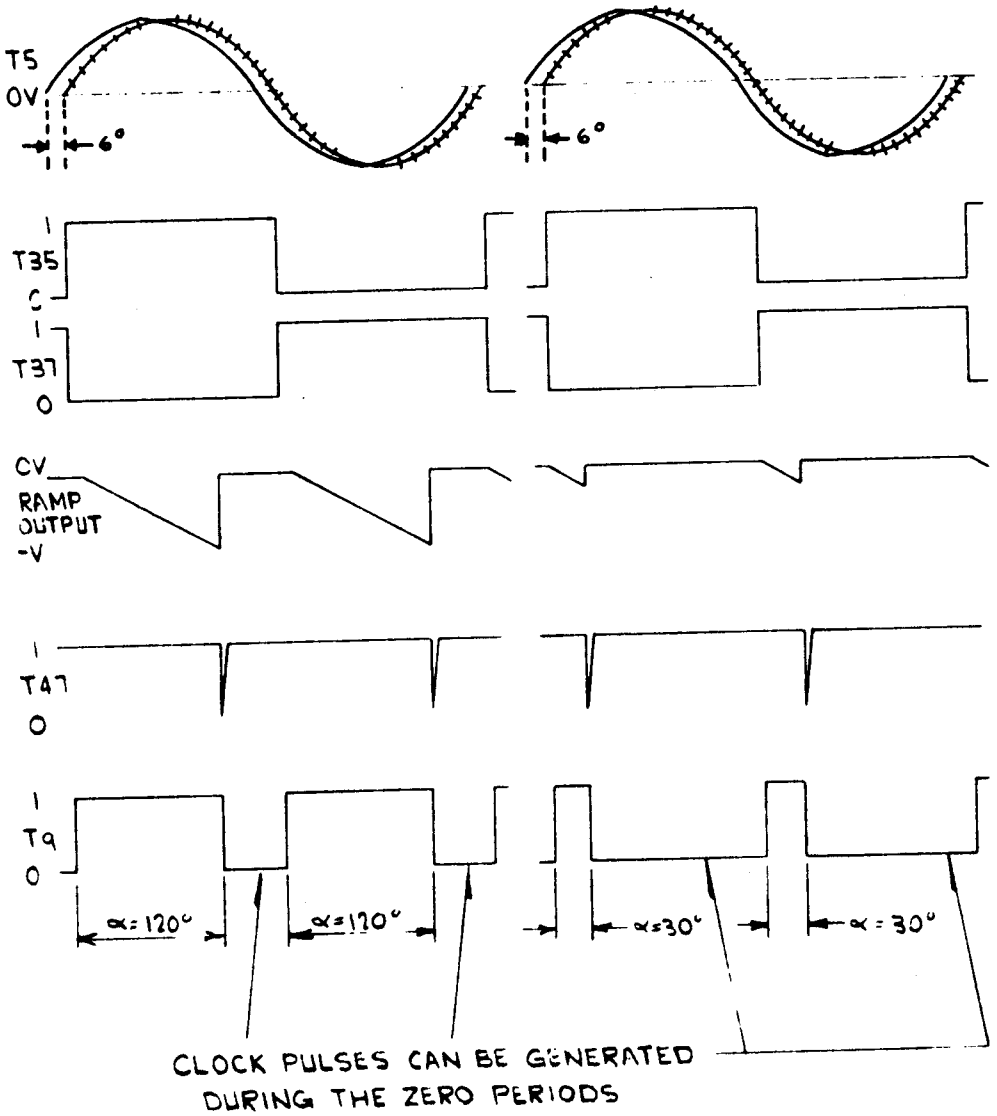
TIMING CIRCUIT

FIGURE 7

When terminal 5 changes from a positive to a negative signal and terminal 7 changes from a negative to a positive signal, the logic signals on terminals 35 and 37 switch from a "1" to a "0" and from a "0" to a "1" respectively. The negative transition of terminal 35 is differentiated and changes the state of the flip-flop: A becomes a "0" and the cycle as already discussed repeats.

Each half cycle causesa repeat functioning of the circuitry of Figure 7. With power and synchronizing voltage applied, the signals on terminals 35, 37 and 9 should always be changing and a negative pulse should be generated on terminal 47 each half cycle.

The firing angle α changes as a function of the error signal on terminal 39. α is restricted by the input diodes 18D, 19D and 20D, and the bias voltage produced by 35R and 37R and by the input scaling to the comparator. Figure 8 shows the waveforms of this card for two different settings. Maximum α occurs when the input to terminal 39 is zero volts; minimum α occurs when the input to terminal 39 is -9.6V.



TIMING DIAGRAM FOR FIGURE 7

FIGURE 8

D. Field Current Control G01 and G02

3-0A and its associated components comprise a proportional controller with adjustable gain. This controller is the field current controller with the reference (positive) signal +If* being applied to terminal 51 and the feedback (negative) signal -If being applied to terminal 49. Terminal 19 is a test input. The error signal on terminal 53 should be wired on the backplane to terminal 39. Gain is adjusted with 1P with an optional jumper between terminals 53 and 55 being used to change the gain range.

E. Field Voltage Control G03 and G05

3-0A and its associated components comprise a proportional controller with a fixed delay of 0.47 secs. This controller is the field voltage controller with the reference signal ($-v_f^*$) being applied to terminal 49 and the feedback signal ($+v_f$) being applied to terminal 51. The amplified error signal output must be applied to the signal conditioning circuitry of the Bank Selector before it is returned to terminal 39 of the Gate Controller. Terminals 19 and 53 must be interconnected on the backplane.

F. Signal Inversion G04

3-0A and its associated components comprise a unity gain inverting amplifier. This amplifier can be used to generate $+I_f$ for use in outer loop control.

G. Field Loss or Overexcitation

40A and its associated circuitry operate as a detector for either a field loss or an overexcitation function. This circuitry is used on G01,G04 and G05. The trip point is adjustable with 2P. Tying terminal 59 to PSC changes the operating range. The output transistor (8TR) can drive a relay or logic circuitry with the appropriate connections being made to terminals 27 and 29.

In the field loss mode, the output relay will de-energize if the field current drops below the set point. In the overexcitation mode, the output relay will energize if excessive current is generated.

III. CHARACTERISTICS AND RATINGS

Synchronization Voltage:

18V RMS to PSC

Range of α:

G01, G02, G04	G03*, G05*	
α max = 147^o	α max = 169^o	T_{39} @ 0.0V
α min = 11^o	α min = 11^o	T_{39} @ -9.6V

*Voltage limit pot must restrict α well within these limits.

Current Controller:

Reference Time Constant	1.1ms
Feedback Time Constant	10ms
Gain adjustable with 1P	
5 to 31	T_{53} jumpered to T_{55}
13 to 81	T_{55} open

Voltage Controller

Reference Time Constant	15ms
Feedback Time Constant	1.1ms
Delay	0.47 msec

Field Loss/Over excitation Trip Voltages:

Adjustable with 2P

-2.06V to -12.20V	T_{59} open
-0.48V to - 3.02V	T_{59} @ PSC

Field Loss/Over excitation Output:

$\|VT_{57}\|$ > V trip	T_{29} goes low
With T_{27} @ +15V	T_{29} can drive 15V logic
With T_{27} @ RP	T_{29} can drive a KU relay

Power Supplies:

PSP	+24V	±	.1V	@	40ma max.
PSN	-24V	±	.1V	@	40ma max.
+15	+15V	±	1.5V	@	20ma max.

Allowable Operating Temperature:

$0^{o}C$ to $55^{o}C$

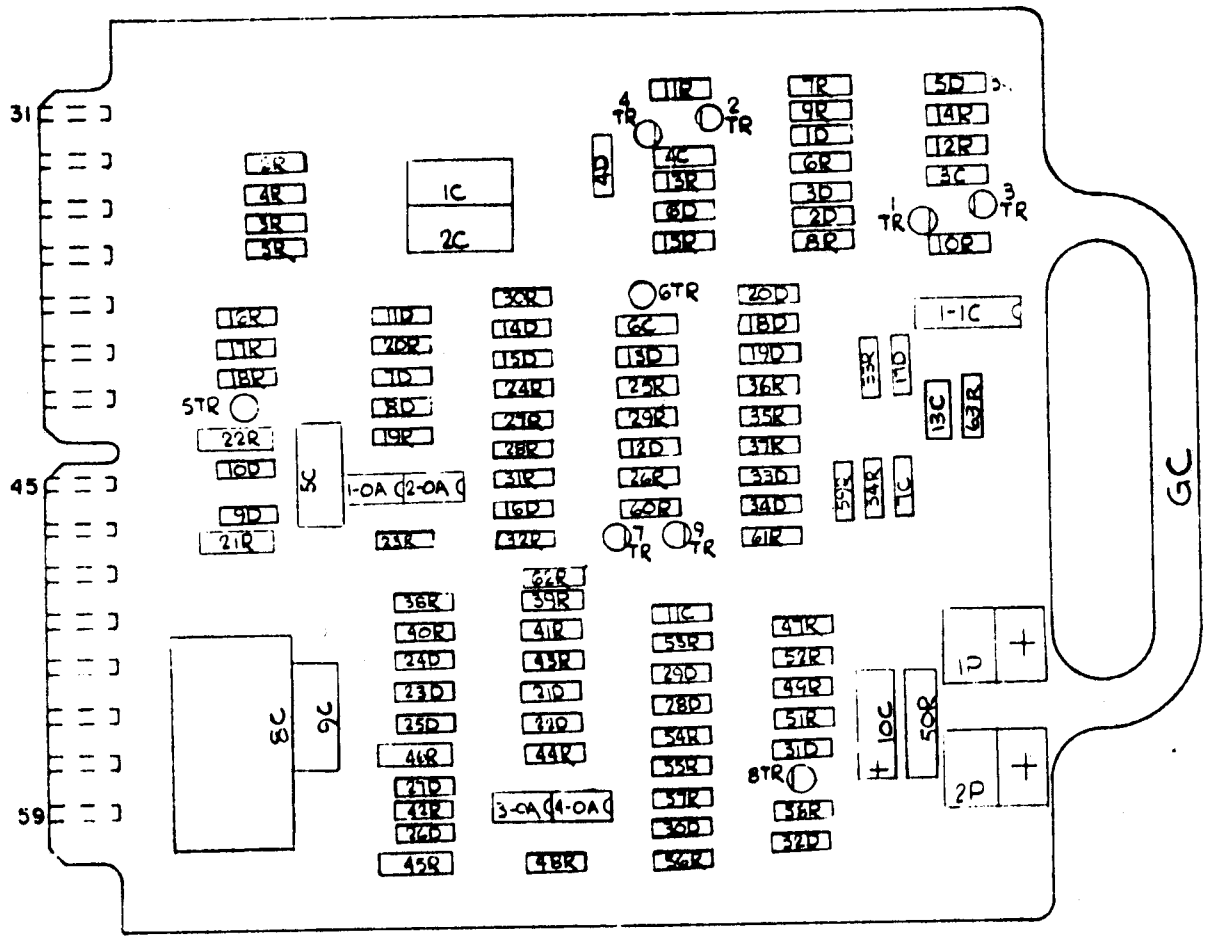


FIGURE 9