MODEL QB/11 PLUS, QB11B
SOLID STATE PROGRAMMABLE CONTROLLERS

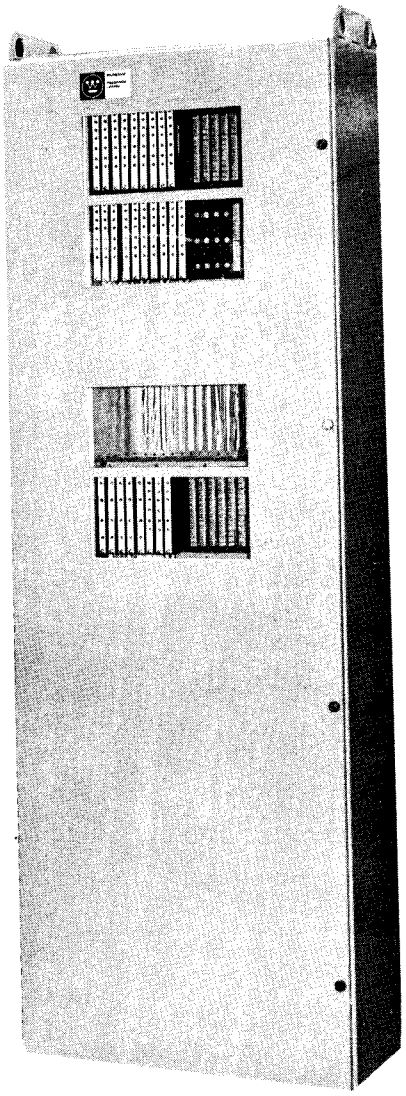


FIGURE 1
QB/11 PLUS PROGRAMMABLE CONTROLLER

EFFECTIVE DECEMBER 1976 SUPERSEDES I.L. 16-800-264

Figure 2

QB11B PROGRAMMABLE CONTROLLER

INDEX

I. INTRODUCTION

This controller is the standard QUARTERBACK Model 11 Programmable Controller. Normally, the con.roller (often called the Model QB/11 requires only four types of circuit boards -- input isolat.on boards, output Triac boards, logic boards, and timers. The controller is programmed us ng convenient English language logic statements. The program is compiled off-line and the results reside in the backplane wiring of the controller. Figure 1 depicts the QB11+ and Figure 2 depicts the QB11B.

II. APPLICATION

The QB/11 is designed as an economical replacement for relay systems having approximately 50 to 100 relays for QB11+, 50 to 200 relays for QB11B. QB11B is the preferred design with application of QB11+ reserved for those applications where rear access is not available.

III. DESCRIPTION OF APPARATUS

The QB11+ consists of 2 power supplies, 2 two-row assemblies, incoming-line circuit breaker, terminal blocks, and interconnecting wiring -- all factory assembled in a dust-tight enclosure, Figure 1. Note that the input and output boards are located toward the left hand side of the enclosure. Normally, inputs are in the top cage assembly and outputs are in the bottom cage assembly, although they can be inter-mixed if necessary.

The QB11B consists of a single power supply, a 5 row cage assembly, incoming line circuit breaker, terminal blocks and interconnecting wiring -- in a dust - tight enclosure, The input and output boards are located in the top and bottom row of the cage assembly, additional I/O boards are allocated to the adjacent rows.

The size of QB/11 is determined primarily by the number of inputs and outputs. Although the only way to determine the exact number of logic boards is to program the controller, a very accurate estimate can be made for relay type circuits by adding the number of input boards to the number of output boards and dividing by two. The maximum number of input plus output boards that can be accommodated is 40 for QB11+, 64 for QB11B each input board can accommodate 6 inputs and each output board can accommodate 4 outputs.

In a QB11+ a maximum of 64 total boards can be accommodated plus an additional four outrigger boards for the power supplies.

In a QB11B a maximum of 135 boards can be accomodated, one of which is allocated for the power supply sequencer board.

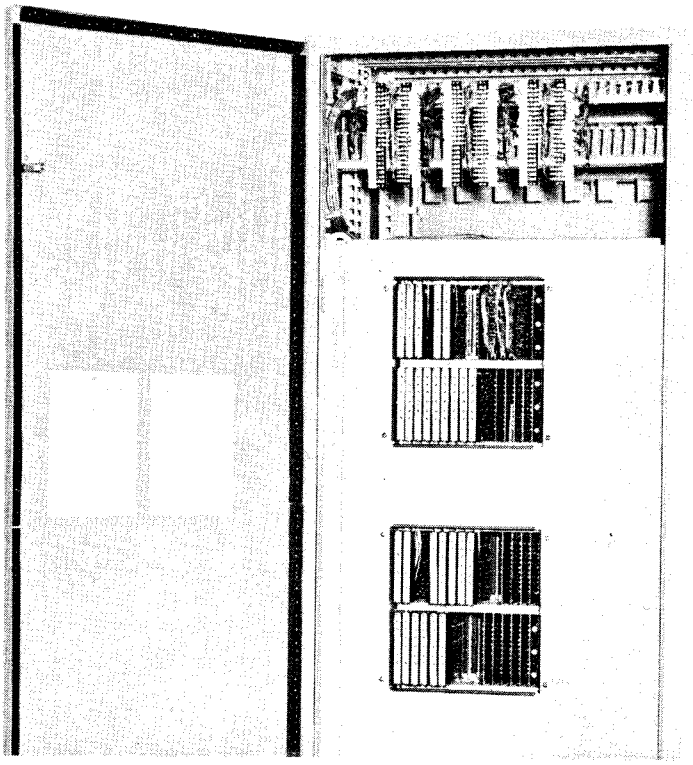


FIGURE 3

Indicating lights are provided on each input and output. Figure 3. The indicating lights are on the front of the input and output boards with the corresponding signal names printed by the computer program on sheets which are placed in plastic envelopes on the inside of the front door.

The input isolation board receives six 110-volt input signals, each of which drives two LED's, Figure 4. One LED provides visual indication of input status, and the other isolates the 110-volt signal from the five-volt logic. The signal from the LED is filtered and amplified to provide the input signal and its complement.

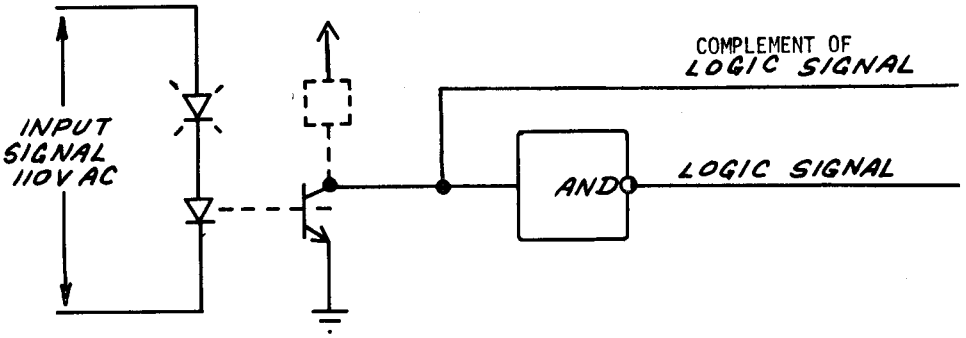


FIGURE 4

The 110-volt output board contains four triac circuits, each having a LED and photo-transistor for isolation, Figure 5. A separate LED provides visual indication of output status. The Triac output is rated for 1.5 amperes continuous current and 10 amperes inrush current. A slow-blow fuse rated 3 amperes is provided on the output board for one side of the line. For a full description, ratings and characteristics, refer to Output Board I.L. 16-800-258.

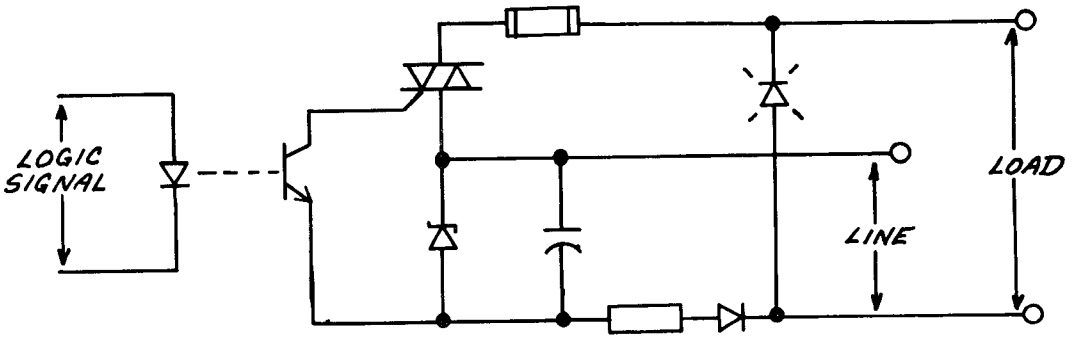


FIGURE 5

The logic board contains 11 three-input AND elements Figure 6. Both the assertion and complement outpu signals are available, as are test points on the front of the board. Each "AND" element can dr ve 8 additional loads. Since the complement of all signals is always available in the controller, the logic element is as efficient in producing the OR function as it is in producing the AND function, Figure 7.

The AND elements are actually composed of four integrated circuit NAND elements. This allows capacitors to be inserted to sedate the logic against noise. The circuit provides a pulse width cut-off point of 20 microseconds, which effectively shields the OB/11 from electrical noise problems that normally occur at a higher frequency.

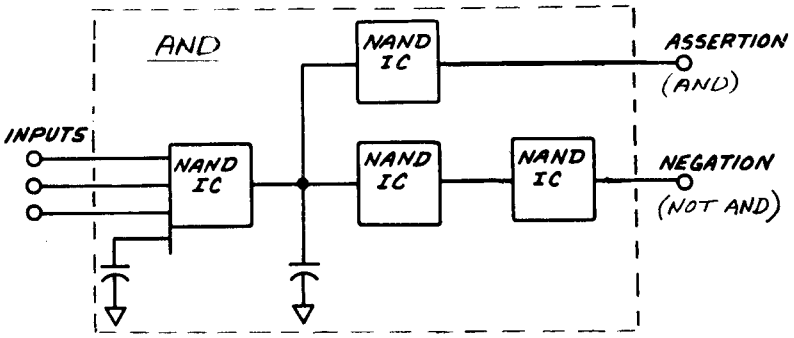


FIGURE 6

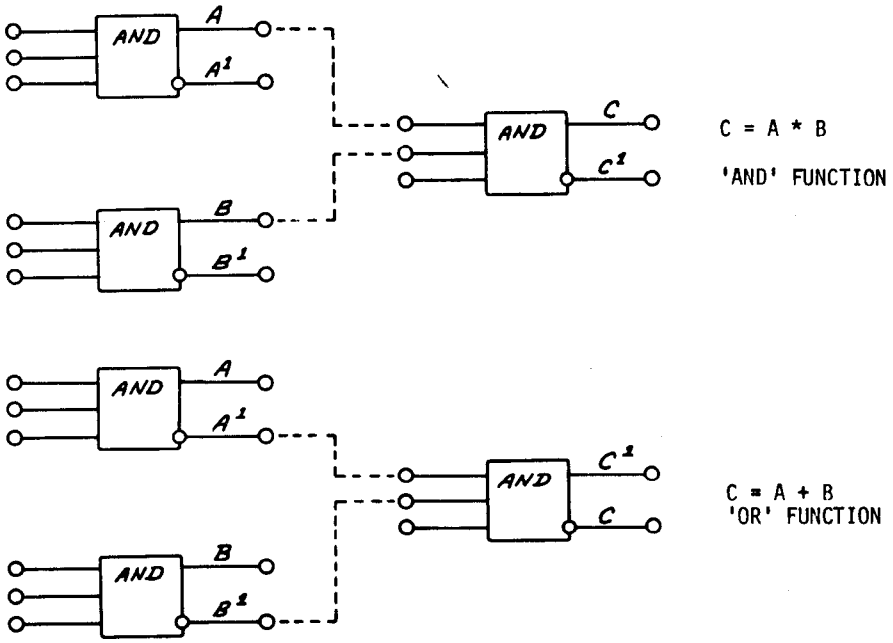


FIGURE 7

Additional output boards are available for special functions. The digital-to-analog converter board is especially useful for providing speed reference signals to variable speed drives. A mercury-wetted relay output board is also available for special functions and to send monitoring information to a remote computer.

An automatic start circuit is provided to initialize seal-in circuits in the "off" position. It is very important that the engineer designing a OB/1 Plus is familiar with this feature. Basically, if a seal in circuit is initiated with a normally open contact and the seal-in circuit is broken with a normally closed contact, the seal will be broken when power is applied to the controller. This is accomplished by delaying input signals a time delay after first applying logic power. This appears to the control that a normally closed contact has been open thus breaking the seal-in. Output power is of course delayed until input power is applied and the logic stable. The sequence is automatically applied when power is applied. For a full description, ratings and characteristics, refer to Sequencer Board I.L. 16-800-259.

Perhaps the most important feature of the QB/11 is the computer-aided design package. The program includes a compiler and a simulation program. Both programs run on the Westinghouse computer at Buffalo. For details on these functions see section on Programming.

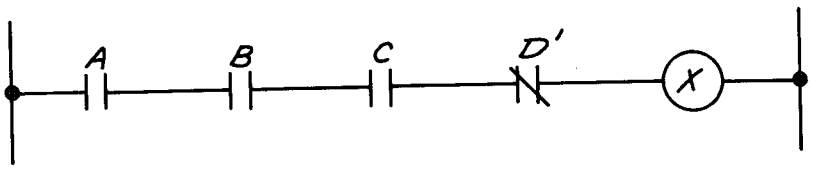
IV. PROGRAMMING PROCEDURE

1. Generation of Equations

The QB-11 is programmed from sets of equations. The equations describe the switching functions to be performed. Each equation is a shorthand statement that specifies the conditions which must exist for a given signal to assume the logical value of '1' to be "turned on" An analogous situation is the relay ladder diagram. Each "rung" of the diagram corresponds to an equation the contact arrangements determine the signal conditions that must exist for the relays to be energized.

The equations involve only the logical concepts of "AND", "OR", and "NOT", so, even though they are written using certain prescribed symbols, their generation is straight forward. The signal corresponding to the relay to be energized is written on the left hand side of the equal sign. The signal conditions which must be satisfied, eg. the relay contact configuration, is written on the right hand side of the equal sign. The symbols used are as follows.

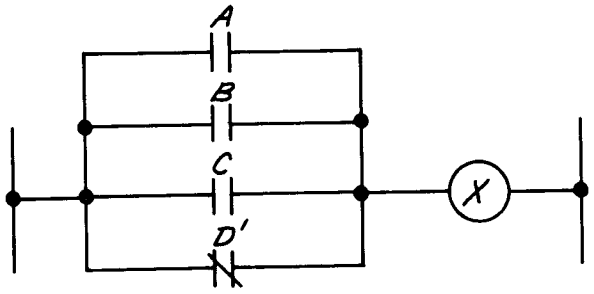
AND (*) The logical "AND" operation in relay circuitry is represented by a series contact string:



In equation format this is written as the expression:

X = A * B * C * D'

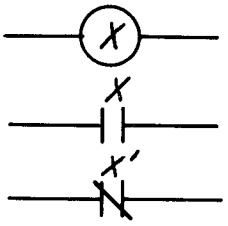
OR (+) The logical "OR" operation in relay circuitry is represented by a group of parallel contacts:



which in equation format becomes the expression

X = A + B + C + D'

NOT (') The logical negation operation in relay circuits is usually represented by normally-closed contacts. If relay X is energized, a normally-closed contact associated with the relay generated the complementary signal.

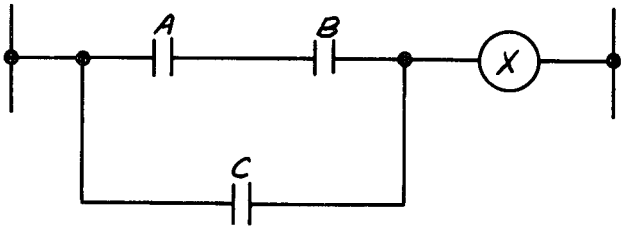


(The normally-open contact represents the actual signal.) In the equation format the logical negation is written:

X-----the signal

X'----The complementary signal or logical negation.

Parentheses () Sets of contacts which effectively become one signal are handled by parenthetical groupings when written as equations. For instance



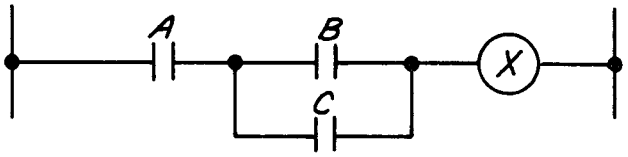
is written in equation format as:

X = (A * B) + C.

The expression

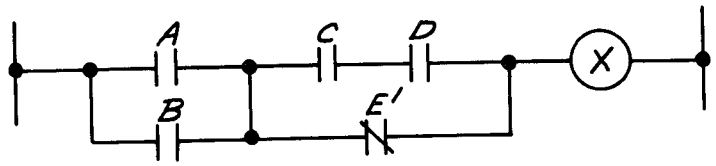
X = A * (B + C)

is logically equivalent to the contact arrangement



Parentheses should be used as necessary to clarify the designer's intent.

Multiple sets of parentheses may be used as required. For example:



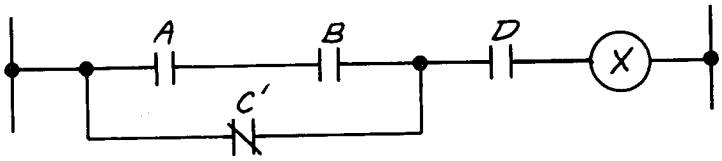
is written:

$$X = (A+B) * ((C * D) + E')$$

In simple cases an equation may be written directly from a normal language statement of the function to be performed. However, until proficiency is developed in handling the equations, the design of more involved circuits can be accomplished in two steps; first by drawing "relay-oriented" schematic, and then by making a "coil-by-coil" conversion from the relay circuit to the equations. As an example of this proceedure consider the following. In English, a circuit is to operate as follows:

"Relay X will be energized if contact D is closed--if signal D is present--and if either (a) contact A and contact B are both closed, or (b) if 'normally-closed' contact C' is closed, or (c) if both of the above conditions prevail".

As a "rung" of a relay circuit diagram this becomes:



In equation form it is written

$$X = ((A * B) + C') * D$$

2. Additional Features

Additional features to be incorporated into the QB-11 circuitry are specified by certain prefixes added to the equations. The following sections on Timers and Outputs require prefixes.

a) Two types of timer boards are available, the Extended Range Timer, and the Single Shot Timer. These are programmed by prefixing (TMxxx) and (TIMEF or TIMEV) respectively to the appropriate logic statement. The type of board required for a particular time range is as follows:

Extended Range Timer (TMxxx)

S#1640A45G01 - 3 per board 1 sec. to 40 min.
S#1640A45G02 - 3 per board 1 sec. to 40 sec.

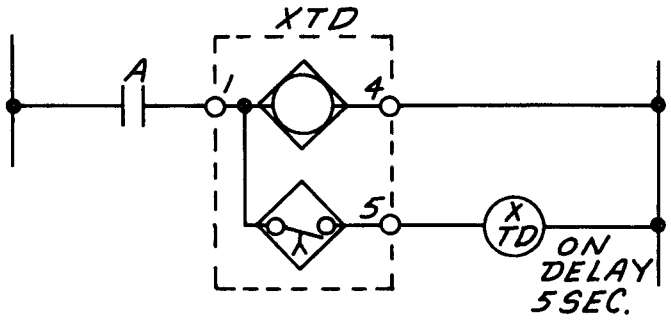
Single Shot Timer (TIMEF or TIMEV)

S#1594A16G01 - 2 per board .15 sec. to .75 sec. (TIMEF)
3 per board .65 sec. to 3 sec. (TIMEV)

An example of two equations using an Extended Range Timer follows:

Time Delay On

If it is desired that the signal generated by the equation (left hand side) appear only after a time has elapsed, the prefix TMxxx is used. In the figure below if "XTD" is to become '1' 5 seconds after A has become '1'. This

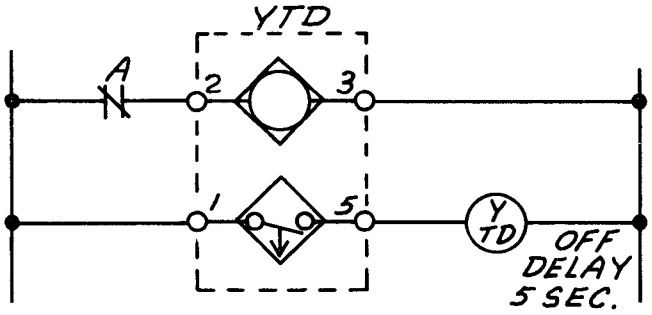


is written in equation format as:

TM005 XTD = A

Time Delay Off

If a signal should remain "on" for a period of time after the conditions causing it have disappeared, the same prefix is used with complemented functions. This



is written in equation format as:

TM005 YTD' = A'

indicates that the signal YTD is to remain a '1' for 5 seconds after the value of A' goes from a '1' to a '0'.

b. Outputs

Two types of output devices are available, the AC switch (TRIAC), and the Hg-wetted relay. These are programmed by prefixing OUTT and OUTR respectively to the appropriate logic statement. If, for instance, Solenoid 1 is to be energized by a TRIAC when Limit Switch 1 closes if either Selector Switch 1 is closed or the system is in "auto", is written as

```
OUTT  SOL1  =  LS1  *  (SW1 + AUTO)
```

The expression indicates that not only is signal SOL1 to be generated, but also that it is to drive an output TRIAC.

3. PROGRAMMING FORMATS

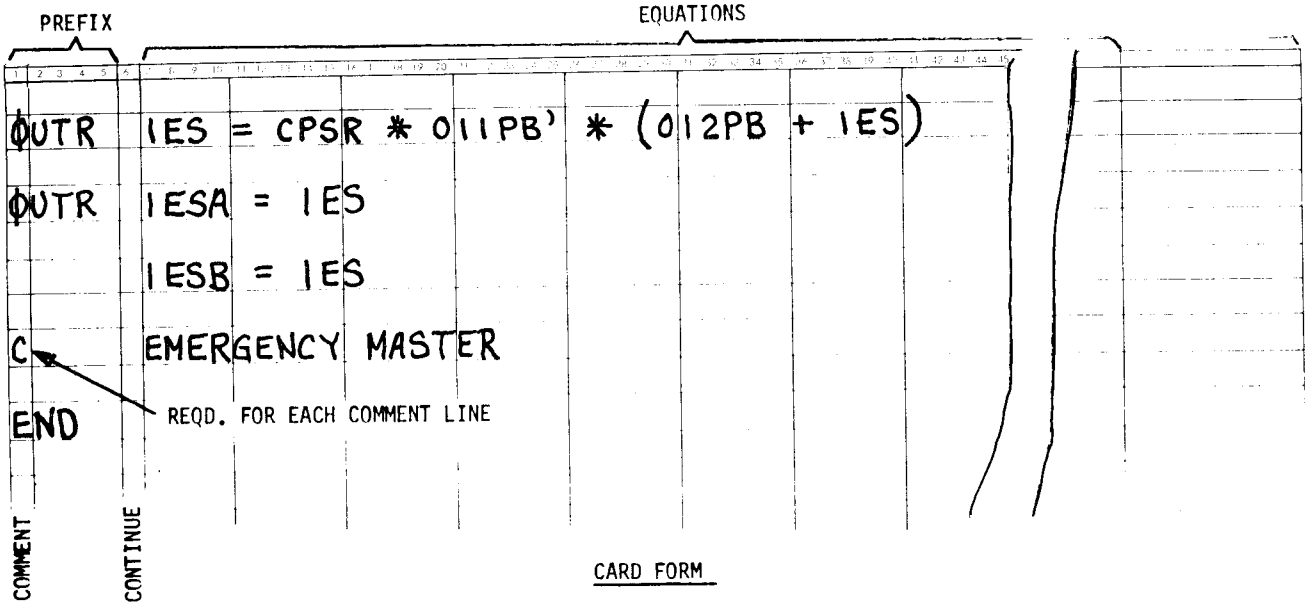
a. Equation Formats

The programming of the QB-11 is facilitated by using a standard card form with 80 columns. All prefixes begin in column 1 and all equations begin in column 7. Equations can not be written beyond column 72. If an equation's length exceeds the column 72 limitation, it may be "continued" by putting the symbol & in column 6 of the next line and continuing in column 7. Up to 9 continuation lines may be used for a given equation.

Blanks may be used for clarity in writing the equation; however, they should not be inserted in symbol names. Symbol names may be up to seven characters long, either alphabetic, or numeric, or both.

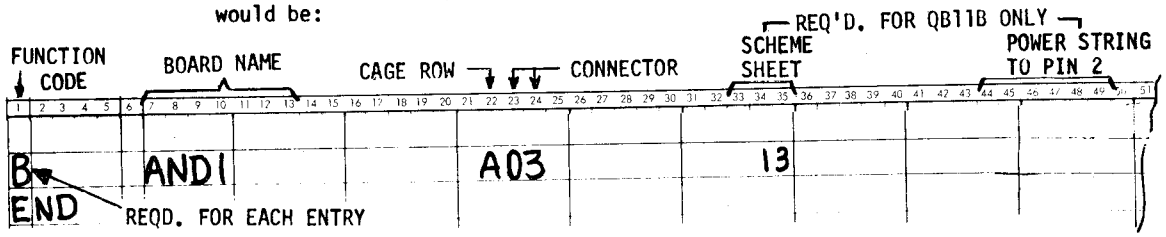
The letter C in column 1 followed by five blanks, (a skip to column 7) indicates that the remainder of the line is a "comment" and not to be processed by the programming system. Comments provide an excellent method of annotating the system logic. Their use is highly recommended. Comments may not appear between the lines of, "continued" equations. However, as many comment lines as necessary may be used.

The end of the set of equations is indicated by the word END beginning in column 1.



b. Cage Layout

The exact cage layout must be specified for each QB-11. This layout is given in a list which makes a one-to-one association between the available printed circuit boards and the cage connectors. The list is prepared on a standard card form. To cause a "AND1" board to be placed in the 'A' row of the cage, connector 03, the list entry would be:



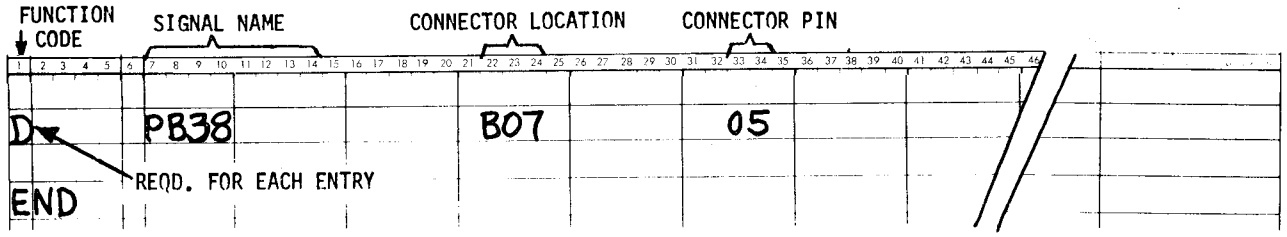
Any "slot" omitted from the list will be assumed to have no connector in it. Any signal assigned to an empty slot will cause the programming system to reject the design.

The available printed circuit boards are:

	BOARD NAME QB11+				BOARD NAME QB11B
BOARD DESCRIPTION	ROW A	ROW B	ROW D	ROW E	ANY ROW
Power Supply Sequencer	PSQ1		PSQ2		PSEQ (C27)
Power Supply Regulator		PSR1		PSR2	
Optical Coupled Input	LDN1	LDN2	LDN1	LDN2	LDN
Logic	AND1	AND2	AND3	AND4	AND
Extended Range Timer (3 @ 1.0 sec. to 40 sec. or 3 @ 1.0 sec. to 40 min.)	TMR1	TMR2	TMR3	TMR4	TMR
Single Shot Timer (2 @ .15 sec. to .75 sec. & 3 @ .65 sec. to 3 sec.	TIME	TIME	TIME	TIME	TIM
Triac Output	TRC1	TRC2	TRC1	TRC2	TRC
Mercury Relay Output	CLR1	CLR2	CLR1	CLR2	CLR
Interconnect Plug H01 to H10	PLUG	PLUG	PLUG	PLUG	PLG
Transmitter Bd.					DIFT
Receiver Bd.					DIER
Power Supply Plug					PWRP (H05)

c. Connection Specification (Optional)

A third set of data, the signal allocation list may be included if desired. This is a tabulation of signal names and their location on the printed circuit board connectors. Such a tabulation, for instance, may specify the Input/Output signals to fix the external connection locations. The preparation of this list is done on a standard card form. If the list is not included, the programming system will automatically supply its own assign ments (alphanumerically). In most situations this is quite adequate. Input/Output signals may be manually assigned in total or selectively.
The formatted line:



would assign signal "PB38" to pin #05 of the connector in slot 07 of cage row 'B'.

It is necessary to know in advance exactly which pins of each individual connector are available for use, and to know exactly how the circuitry of the various printed circuit boards is arranged. It is also necessary that the layout of the cage be known(see Section 3b CAGE LAYOUT).

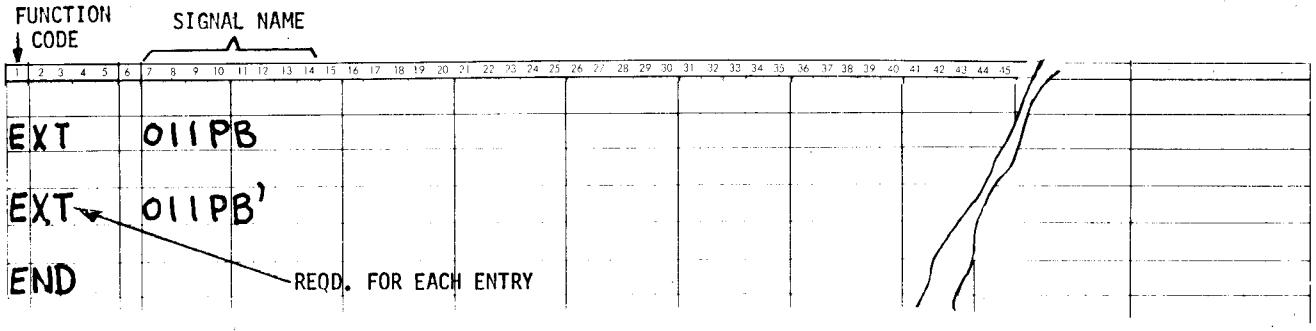
Whether the list is included or not, the word END must be coded beginning in column 1. If there is no list, two lines beginning END would appear in succession (because of the END terminating the cage layout list).

d. External Signals (Optional)

All signals which are not generated by the logic (i.e. do not appear on the left hand side of an equation) must be brought in from the "out side". This may be done in either of two ways: automatically by the computer identifying and assigning the input signal(s) or manually by specifying the signal(s) in question to be an EXT signal.

Incoming signals specified automatically by the computer are always assigned with the unprimed signal name assigned to the direct (Z) output of the input board; the primed signal name is assigned to the complementary (Z') output of the input board. If it is necessary to reverse this signal assignment two things must be done: suppress the automatic generation of the input signal by specifying the signal as an EXT signal and "manually" assigning the signal to the desired connector pin in the manual assignment list.

Signals are specified as EXT signals by generating the list as



The list is terminated by END in column 1.

The EXT list, including the END card, is completely optional.

4. Computer Aided Design Procedure

A QB/11 computer aided design proceedure requires several operations, which follow below in a step by step order.

a. Generate and Process Equations

Logic equations are generated per the Programming Procedure, Section IV. These equations are keypunched and processed thru the computer. A Pre-Processor print out is generated from which the total number of Input, Output and Logic elements required are listed. This list provides some of the information needed to generate the cage layout.

b. Specify Cage Layout

When specifying the cage layout (section 3b), in addition to the board requirements determined by the pre processor, the following information is necessary.

QB11+ Power Supply Sequencer PSQ1 (A01) and PSQ2 (D01)

Always needed in position A01 (This is not on Pre-Processor)
Always needed in position D01 (This is not on Pre-Processor)

Power Supply Regulator PSR1 (B01) and PSR2 (E01)

Always needed in position B01 (This is not on Pre-Processor)
Always needed in position E01 (This is not on Pre-Processor)

QB11B Power Supply Sequencer (C27)

Always needed in Position C27 (This is not on Pre-Processor)

Input Relays (6 per board)

QB11+ LND1 (Row A & D) LND2 (Row B & E)

Preferred locations as follows:

A03	D03 Input Board	Isolated		A09	D09 Input Board	Isolated	
or		or		or		or	
A04	D04 Input Board	Common		A10	D10 Input Board	Common	
A05	D05 Input Board	Isolated		A11	D11 Input Board	Isolated	
or		or		or		or	
A06	D06 Input Board	Common		A12	D12 Input Board	Common	
A07	D07 Input Board	Isolated					
or		or					
A08	D08 Input Board	Common					

Boards shown as pairs must both be of the same type, either common AC or Isolated AC. Isolated AC should use the higher cage connectors (e.g. A11, A12, D11, D12, etc.)

QB11+ LDN (Row A & B)

Preferred locations A01 thru A26, B01 thru B12. Any mix of common and isolated AC is acceptable.

Output Relays (6 per board) or Output Triac Boards (4 per board)

QB11+ CLR1 (Row A & D) CLR2 (Row B & E) TRC1 (Row A & D) TRC2 (Row B & E)

Preferred locations as follows:

B03	E03 Output Board	Isolated		B09	E09 Output Board	Isolated	
or		or		or		or	
B04	E04 Output Board	Common		B10	E10 Output Board	Common	
B05	E05 Output Board	Isolated		B11	E11 Output Board	Isolated	
or		or		or		or	
B06	E06 Output Board	Common		B12	E12 Output Board	Common	
B07	E07 Output Board	Isolated					
or		or					
B08	E08 Output Board	Common					

Boards shown as pairs must both be of the same type either Common AC or Isolated AC. Isolated AC should use the higher cage connectors (e.g. B11, B12, E11, E12, etc.)

QB11B CLR, TRC (Row E)

Preferred locations E01 to E26 with output relays near the D01 end.

Logic Boards (10 ANDS per board)

QB11+ AND1 (Row A) AND2 (Row B) AND3 (Row D) AND4 (Row E)
Are usually located in Cage slots 13 to 18

QB11B AND (Rows A thru E)
Preferred locations positions 14 thru 26 in rows B,C,& D. Boards may be located in any position.

Extended Range Timer (3 per board)

QB11+ TMR1 (Row A) TMR2, (Row B) TMR3, (Row D) TMR4 (Row E)
QB11B TMR (Rows A thru E)
May be located in: Any slots unused in any row.

Single Shot Timer (5 adjustable per board) (All rows)

QB11+ TIME May be located in any slot
QB11B TIM that is unused in any row

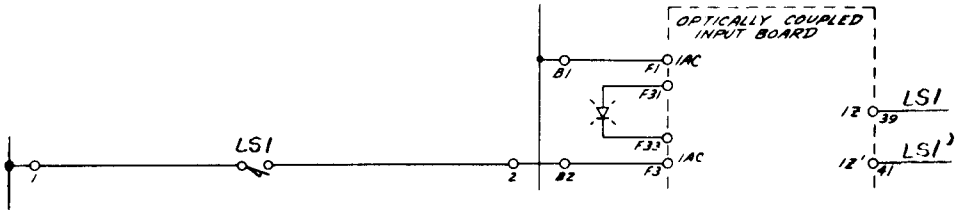
c. Specify "Manual" Connections List

After completing the cage layout it may be necessary to assign certain signals to particular back panel pins:

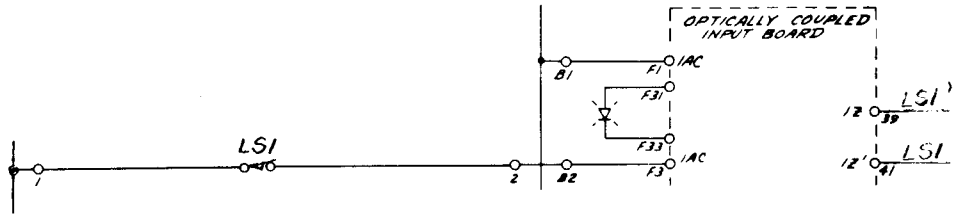
1. To group connections (for example, from a particular operator station customer devices, etc.) to a specific terminal block in the QB/11.
2. To coordinate the logic equations with the input device. For instance with the equation

$$RUN = A * B * LS1'$$

if the device which generates signal LS1 is a normally-open device and if "Run" should be a "1" if the device is not activated, then the input circuit board should be connected



If, however, the device which is to generate signal LS1 is a normally-closed device and "Run" is still to be a "1" if the device is not activated (the same logic equation) then the input circuitry must be



The LS1 & LS1' signals are reversed. The "inverted" assignment must be indicated in this list.

Note: Even If the Manual List is not required, an END card must be included (per section 3c).

d. List External Signals

A cancellation of the computers automatic input signal generation feature (section 3d) is required when signal reversal (section 4c2) is used. Both primed and unprimed signals must be listed. If no cancellations are necessary, no END card is used.

5. Simulation

Simulation is used to prove the design of a logic system. It is executed in much the same way a hardware test would be performed. A prescribed set of input signals are varied in a given sequence and the reaction of the logic-generated signals, described by the equations, is observed. For a full description refer to instruction leaflet on Simulation I.L.16-800-260.

THE PRECEEDING SECTION HAS DISCUSSED THE PROGRAMMING PROCEDURE FOR A QB/11. FOR A SAMPLE RELAY SCHEME AND THE PROCEDURE TO CONVERT IT INTO A QB/11 CONTROLLER REFER TO THE APPENDIX, SECTION VII, OF THIS INSTRUCTION LEAFLET.

V. START-UP PROCEDURE

A. Introduction

The QB/11 is factory checked and is assumed to be a complete, operational unit when delivered to the customer. The QB/11 should require only unpacking, mounting and external wiring.

These instructions provide a step-by-step procedure for a first time start-up of a QB/11 Programmable Controller.

The start-up procedure is recommended as a precaution against damaging any components, within or external to the QB/11.

The procedures should be followed in the specified sequence, checking each step against the schematic diagram. This will develop familiarity with the system and insure proper operation of the drive when the sequence is completed. If difficulty is encountered at any step, the source of the trouble should be determined and corrected before proceding.

Non-standard functions such as special sequencing, interconnection with other drives, etc. which pertain to a specific application are covered by separate instructions.

B. Inspection

Check for any loose wires or assemblies. Check that all cards are firmly inserted in the slots. Check that all front connectors are firmly plugged onto the correct cards.

C. External Connections

1. All input and output signal wiring should be connected to the terminal blocks. These connections should be made according to the external wiring information supplied with the particular QB/11 unit.

2. Before connecting the 115 VAC power input to the terminal block on the left wall of the cabinet, check that breakers 1CB and 2CB on the power panel are open (OFF). The 115 VAC 50/60 Hz power should be connected to terminals 11 and 12 of the block. Terminal 10 should be wired to plant ground.

D. Power Supply Checks

With circuit breaker 2CB open (OFF), close circuit breaker 1CB. If the external 115 VAC supply is active, the red indicator 1IL should come on and the fan will start. With a meter, make the following voltage checks.

1. 115 VAC should be present between the A.C. buses feeding the input terminal block boards. The A.C. buses feeding the output boards should remain de-energized. Fuses 1FU and 2FU on the back of the power supply panel (PS2) feed the A.C. buses for the input boards.

2. Check for +5VDC ± 10% between pin 2 of each card connector and the common bus. (Exception: The power supply sequencer card in slots A01 and D01 on QB11+ requires no voltage on pin2.)

E. Power Supply Sequencing Test

1. Open circuit breaker 1CB and close 2CB. Connect a D. C. Voltmeter (0-10VDC) from pin 2 (positive) of any triac output card to common.

2. Close circuit breaker 1CB. After approximately 8 seconds the D. C. Voltmenter reading should change from 0 volts to +5 volts D. C. and simultaneously the white light 2IL should come on. The A.C. buses feeding the outputs will show 115 VAC across them whenever 1CB and 2CB are both closed.

F. Operational Tests

To simulate any actual operating situations, the following procedures may be used.

1.0 Input Boards

1.1 Preferred Method

To simulate an input contact closure, short together the two terminals on the terminal block which connect to the external input contact being "picked up". The LED indicator will light.

1.2 Alternative Method

To simulate an energized input, connect the input complement signal on the logic backpanel connectors to logic common. These signals are available for any input board S#:640A29 on the pins shown below:

Input Circuit	Pin No.
#1	41
#2	5
#3	17
#4	49
#5	21
#6	29

When an input contact closure is simulated on the logic backpanel by this technique, the LED indicator will not light.

2.0 Output Boards

2.1 To energize a triac output contact, connect the logic complement signal for that output to common by shorting the common to the pins listed below:

Output Circuit	Pin No.
#1	35
#2	41
#3	47
#4	57

The indicator LED will light to indicate an energized output (contact closure) if the A.C. output power is on.

VI. REFERENCES

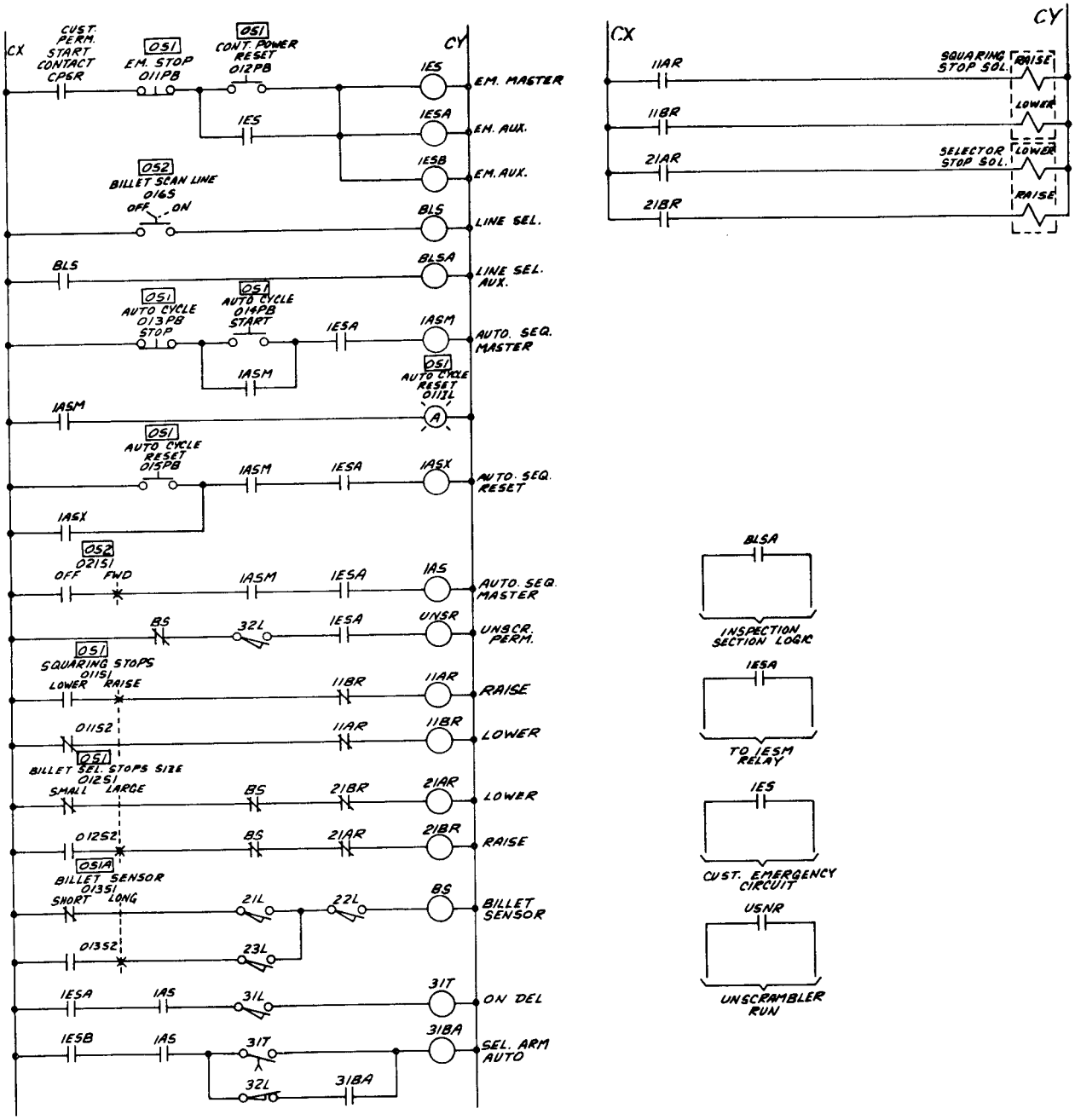
The following is a listing of supporting QB/11 instruction leaflets.

I.L.16-800-258 Output Triac Board
I.L.16-800-259 Power Supply Sequencer Board
I.L.16-800-260 Simulation Program
I.L.16-800-261 Extended Range Timer

VII. APPENDIX

This section pertains to a sample relay schematic and the requirements needed to convert it into a QB/11 schematic.

The following circuits are part of a sample relay schematic.



From the preceding relay schematic the following equations were written.

```
ØUTR   1ES = CPSR * 011PB' * (012PB + 1ES)
ØUTR   1ESA= 1ES
       1ESB= 1ES
C      EMERGENCY MASTER
       BLS = 016S
ØUTR   BLSA= BLS
C      LINE SELECTØR
ØUTR   1ASM= 013PB' * (014PB + 1ASM) * 1ESA
C      AUTØ SEQUENCER MASTER
       1ASX= (015PB + 1ASX) * 1ASM * 1ESA
C      AUTØ SEQUENCE RESET
       1AS = 021S1 * 1ASM * 1ESA
C      AUTØ SEQUENCE MASTER SWITCH
ØUTR   UNSR= BS' * 32L * 1ESA
C      UNSCRAMBLER PERMISSIVE
ØUTT   11AR= 011S1 * 11BR'
C      SQUARING STØP RAISE SØLENØID
ØUTT   11BR= 011S2 * 11AR'
C      SQUARING STØP LØWER SØLENØID
ØUTT   21AR= 012S1 * BS' * 21BR'
C      SELECTØR STOPS SIZE SMALL SØLENØID LØWER
ØUTT   21BR= 012S2 * BS' * 21AR'
C      SELECTØR STØPS SIZE LARGE SØLENØID RAISE
```

```
       BS  = ((013S1 * 21L) + (013S2 * 23L)) * 22L
C      BILLET SENSØR SELECTØR SHØRT-LØNG
TM005  31T = 1ESA * 1AS * 31L
C      SELECTØR ARM AUTØ RAISE ØN DELAY
       31BA= 1ESB * 1AS * (31T + (32L' * 31BA))
C      SELECTØR ARM AUTØ LØWER
END
```

These equations are keypunched and processed thru the computer. The result is a Pre-Processor print out.

Following is some of the data from the Pre-Processor print-out needed to design the QB11.

a. Specify Cage Layout

With this list and information from Cage Layout (section 4b) the total number and type of boards required are obtained. Check that 64 boards maximum are not exceeded.

```
THE NUMBER OF ELEMENTS USED ARE---

ANDS     =        24                    10 ANDS/BOARD (AND1 OR AND2)
SHORT TIMERS  =        0                2 VARIABLE &
LONG TIMERS   =           0             3 VARIABLE/BOARD (TIMER)
TRIACS  =                               4 TRIACS/BOARD (TRCL)
OUTPUT RELAYS    =        5             6 RELAYS/BOARD (CLARE)
INPUT RELAYS       19                   6 INPUTS/BOARD (LEDIN)
EXTENDED RANGE TIMERS   =       1       3 TIMERS/BOARD (TIMR)
```

b. Specify "Manual" Connections

After cage layout has been completed the following options can be performed.

1. With the External Input Signals list and the proper input board MIC schematic, you can manually assign all the input signals (per section 4c1).

```
THE FOLLOWING SIGNALS ARE ASSUMED TO BE EXTERNAL INPUT SIGNALS
 INPUT      SIGNAL      INPUT BUFFER
  NO.        NAME         LOADING

   1        CPSR             1
   2        011PB'           1
   3        011S1            1
   4        011S2            1
   5        012PB'           1

   6        012S1            1
   7        012S2            1
   8        013PB'           1
   9        013S1            1
  10        013S2            1

  11        014PB'           1
  12        015PB'           1
  13        016S             1
  14        021S1            1
  15        21L              1

  16        22L              1
  17        23L              1
  18        31L              1
  19        32L              1
  20        32L'             1
```

2. With the Relay Output list and the proper output board MIC schematic you can manually assign all the output signals

RELAY OUTPUTS---

NUMBER	SIGNAL
1	BLSA
2	UNSR
3	1ASM
4	1ES
5	1FSA

3. With the Triac Output list and the proper output board MIC schematic you can manually assign all the output signals.

Note: The Triac Output list from the computer shows unprimed signals. In order for a Triac Board to be activated a primed signal must be used. Since the Logic boards produce both primed and unprimed signals, you must use the complementary signal from that in this list.

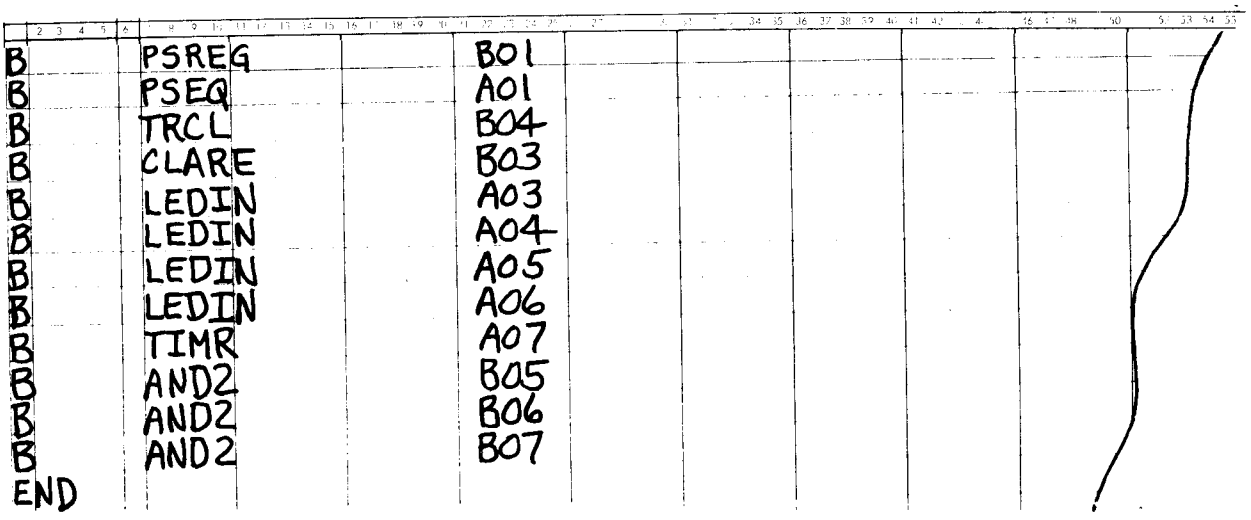
TRIAC OUTPUTS---

NUMBER	SIGNAL
1	11AR
2	11BR
3	21AR
4	21BR

From the preceding Pre-Processor data the following information can be coded.

NOTE: The following coding must start in columns as shown.

CAGE LAYOUT CODING



MANUAL ASSIGNMENT CODING

```
D    011PB'    A03    39
D    012PB'    A03    05
D    013PB'    A03    13
D    014PB'    A03    49
D    015PB'    A03    21
D    11AR'     B04    35
D    11BR'     B04    41
D    1ASM      B03    24
END
```

On this sample, all input/output signals were not assigned. The remainder of input/output signals were assigned by the computer.

The External Signal list is used when reversal of primed and unprimed signals in the Manual Assignment list have been made. In this sample the following signals have been reversed.

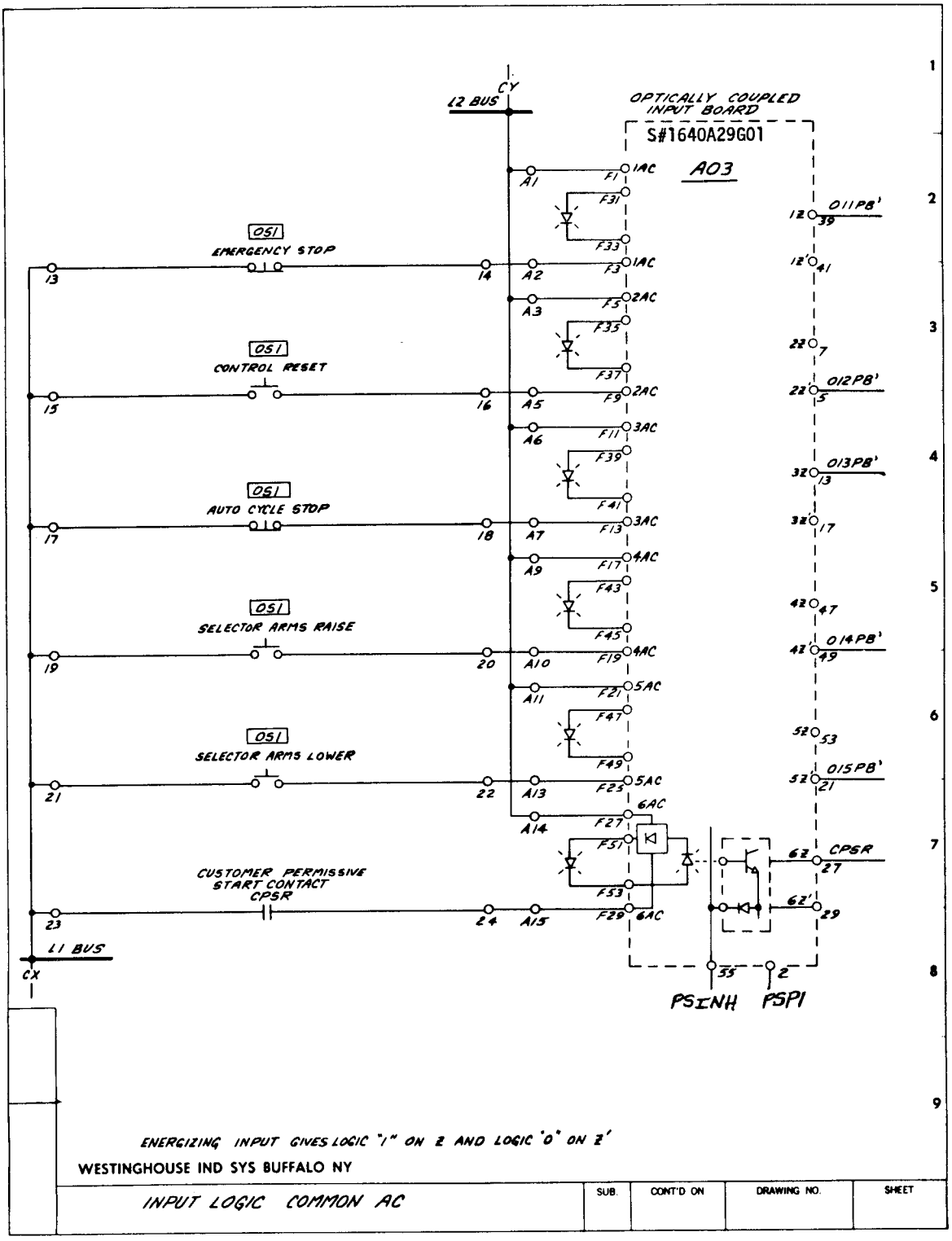
EXTERNAL SIGNALS CODING

```
EXT  011PB
EXT  011PB'
EXT  013PB
EXT  013PB'
END
```

After the above coding is complete and being processed thru the computer, the engineer may complete the schematic. However if the computer is allowed to assign the input/output signals automatically, the schematic can not be completed until the final computer print out is obtained.

c. Schematic Completion

The following is only part of a OB/11 schematic. The A.C. Distribution, +5 VDC Power Supplies and 3 additional Input Logic Sheets have not been shown.



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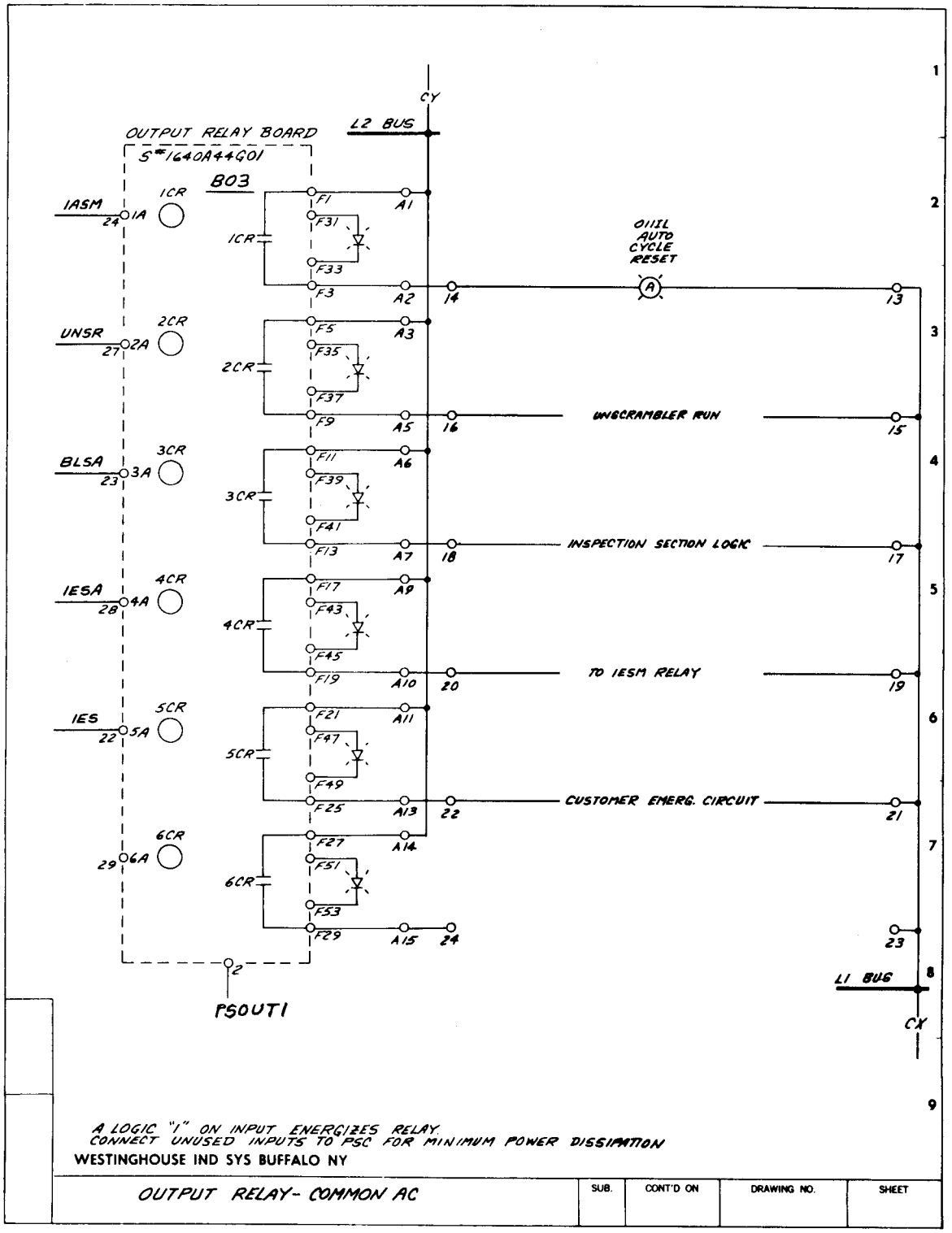
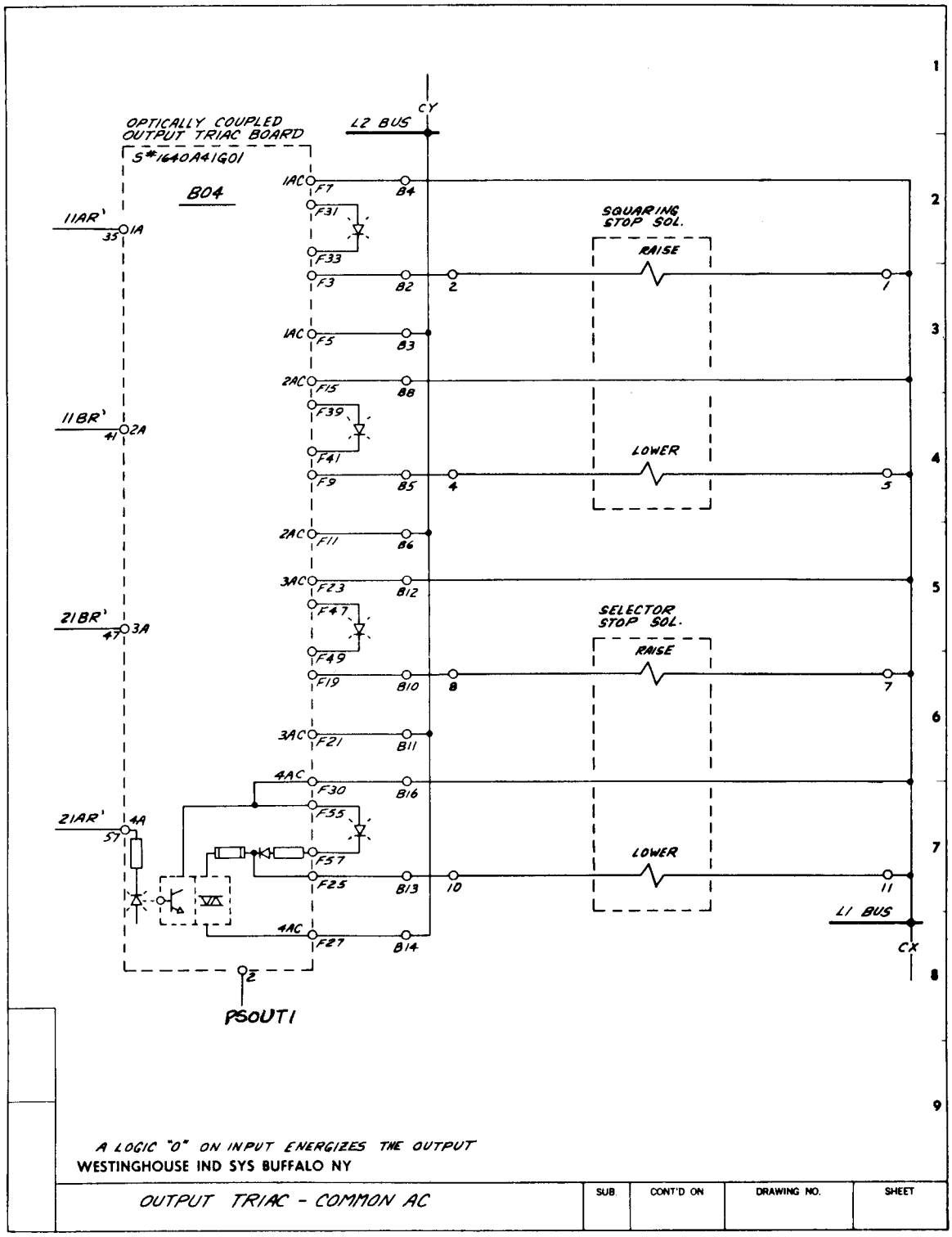

OUTPUT RELAY BOARD
S#1640A44G01
B03
CY
L2 BUS
IASM
24
1A
1CR
UNSR
27
2A
2CR
BLSA
23
3A
3CR
IESA
28
4A
4CR
IES
22
5A
5CR
29
6A
6CR
F1
A1
F31
F33
F3
A2
14
OIIIL
AUTO
CYCLE
RESET
A
13
F5
A3
F35
F37
F9
A5
16
UNSCRAMBLER RUN
15
F11
A6
F39
F41
F13
A7
18
INSPECTION SECTION LOCK
17
F17
A9
F43
F45
F19
A10
20
TO IESM RELAY
19
F21
A11
F47
F49
F25
A13
22
CUSTOMER EMERG. CIRCUIT
21
F27
A14
F51
F53
F29
A15
24
23
2
PSOUT1
LI BUS
CX
1
2
3
4
5
6
7
8
9
A LOGIC "1" ON INPUT ENERGIZES RELAY.
CONNECT UNUSED INPUTS TO PSC FOR MINIMUM POWER DISSIPATION
WESTINGHOUSE IND SYS BUFFALO NY
OUTPUT RELAY- COMMON AC
SUB.
CONT'D ON
DRAWING NO.
SHEET



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This sheet of the schematic is a list of the processed logic equations, from which the required logic circuits are generated. For a schematic representation of a Logic Board see page 28.

NO	ELEMENT TYPE	INPUT NO 1	INPUT NO 2	INPUT NO 3	OUTPUT	COMPLE-
SELECTOR ARM AUTO LOWER						
1	N	1ESB	1AS	ZZZ008	31BA'	31BA
2	N	31T'	ZZZ007'		ZZZ008	ZZZ008'
3	N	32L'	31BA		ZZZ007'	ZZZ007
SELECTOR ARM AUTO RAISE ON DELAY						
4	TMR	TTL001	TTL001		M001ER	
5	N	M001ER			31T'	31T
6	N	1ESA	1AS	31L	TTL001'	TTL001
BILLET SENSOR SELECTOR SHORT-LONG						
7	N	ZZZ006	22L		BS'	BS
8	N	ZZZ004'	ZZZ005'		ZZZ006	ZZZ006'
9	N	013S2	23L		ZZZ005'	ZZZ005
10	N	013S1	21L		ZZZ004'	ZZZ004
SELECTOR STOPS SIZE LARGE SOLENOID RAISE						
11	TRIA				21BR'	
12	N	012S2	BS'	21AR'	21BR'	21BR
SELECTOR STOPS SIZE SMALL SOLENOID LOWER						
13	TRIA				21AR'	
14	N	012S1	BS'	21BR'	21AR'	21AR
SQUARING STOP LOWER SOLENOID						
15	TRIA				11BR'	
16	N	011S2	11AR'		11BR'	11BR
SQUARING STOP RAISE SOLENOID						
17	TRIA				11AR'	
18	N	011S1	11BR'		11AR'	11AR
UNSCRAMBLER PERMISSIVE						
19	CLAR				UNSR	
20	N	BS'	32L	1ESA	UNSR'	UNSR
AUTO SEQUENCE MASTER SWITCH						
21	N	021S1	1ASM	1ESA	1AS'	1AS
AUTO SEQUENCE RESET						
22	N	ZZZ003	1ASM	1ESA	1ASX'	1ASX
23	N	015PB'	1ASX'		ZZZ003	ZZZ003'
AUTO SEQUENCER MASTER						
24	CLAR				1ASM	
25	N	013PB'	ZZZ002	1ESA	1ASM'	1ASM
26	N	014PB'	1ASM'		ZZZ002	ZZZ002'
LINE SELECTOR						
27	CLAR				BLSA	
28	N	BLS			BLSA'	BLSA
29	N	016S			BLS'	BLS
EMERGENCY MASTER						
30	N	1ES			1ESB'	1ESB
31	CLAR				1ESA	
32	N	1ES			1ESA'	1ESA
33	CLAR				1ES	
34	N	CPSR	011PB'	ZZZ001	1ES'	1ES
35	N	012PB'	1ES'		ZZZ001	ZZZ001'

DRAWING	SUB	SHEET NO.	SHEETS

This sheet of the schematic is a list of input equations. These are the exact equations written by the designer.

```
OUTR   1ES = CPSR * 011PB' * (012PB + 1ES)
OUTR   1ESA= 1ES
       1ESB= 1ES
C      EMERGENCY MASTER
       BLS = 016S
OUTR   BLSA= BLS
C      LINE SELECTOR
OUTR   1ASM= 013PB' * (014PB + 1ASM) * 1ESA
C      AUTO SEQUENCER MASTER
       1ASX= (015PB + 1ASX) * 1ASM * 1ESA
C      AUTO SEQUENCE RESET
       1AS = 021S1 * 1ASM * 1ESA
C      AUTO SEQUENCE MASTER SWITCH
OUTR   UNSR= BS' * 32L * 1ESA
C      UNSCRAMBLER PERMISSIVE
OUTT   11AR= 011S1 * 11BR'
C      SQUARING STOP RAISE SOLENOID
OUTT   11BR= 011S2 * 11AR'
C      SQUARING STOP LOWER SOLENOID
OUTT   21AR= 012S1 * BS' * 21BR'
C      SELECTOR STOPS SIZE SMALL SOLENOID LOWER
OUTT   21BR= 012S2 * BS' * 21AR'
C      SELECTOR STOPS SIZE LARGE SOLENOID RAISE
       BS  = ((013S1 * 21L) +(013S2 * 23L))* 22L
C      BILLET SENSOR SELECTOR SHORT-LONG
TM005  31T = 1ESA * 1AS * 31L
C      SELECTOR ARM AUTO RAISE ON DELAY
       31BA= 1ESB * 1AS*(31T + (32L'* 31BA))
C      SELECTOR ARM AUTO LOWER
END
```

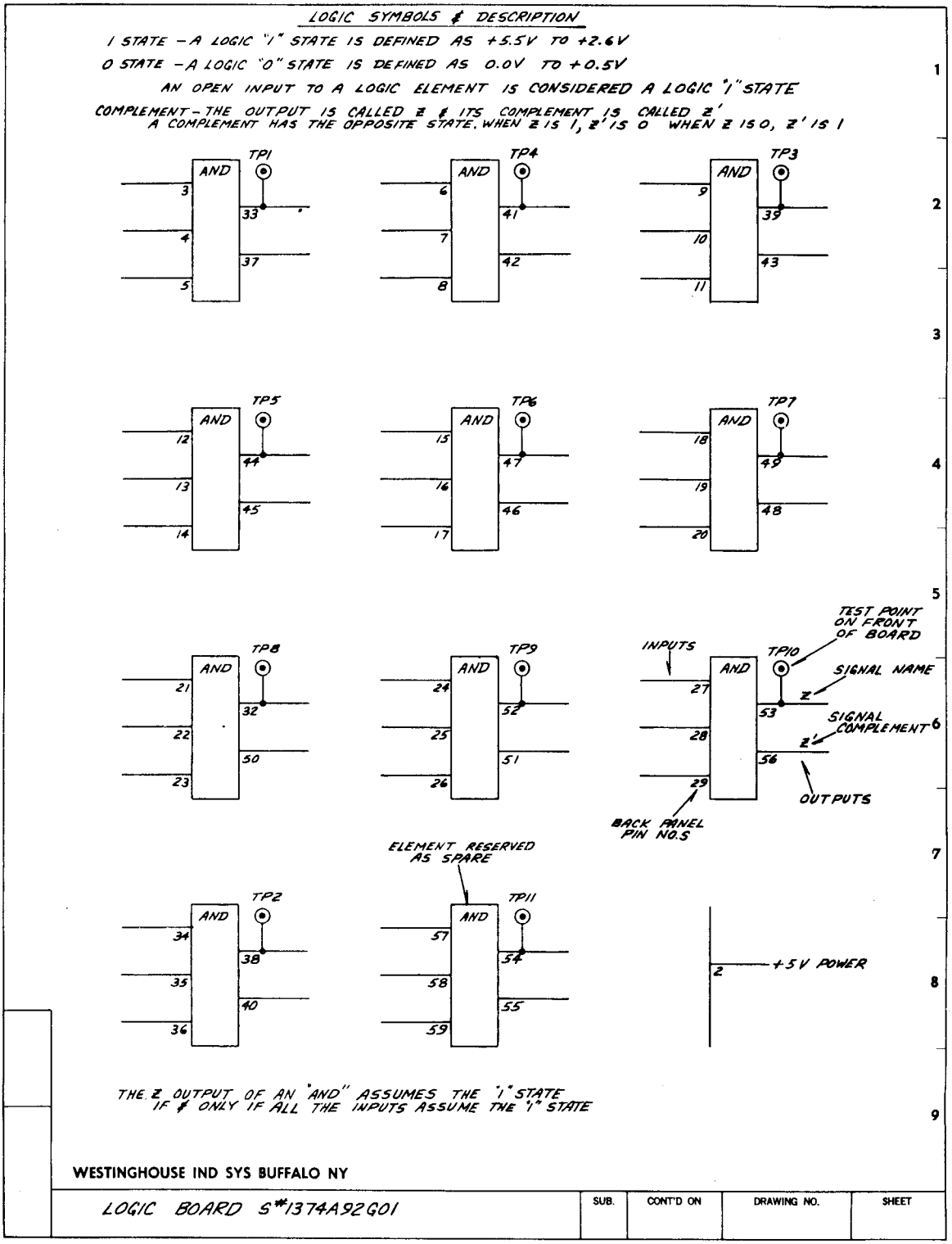
DRAWING	SUB	SHEET NO.	SHEETS

This sheet of the schematic is a list of the back panel wiring (Sorted Signal List).

SORTED SIGNAL LIST

SIGNAL NAME	CON-PIN	CON-PIN	CON-PIN	CON-PIN	CON-PIN	CON-PIN	CON-PIN
BLS	B 5 18	B 5 47					
BLSA	B 3 23	B 5 49					
BS'	B 6 6	B 6 40	B 6 16	B 6 19			
CPSR	A 3 27	B 5 6					
MOO1ER	A 7 10	B 7 6					
PSINH	A 1 6	A 3 55	A 4 55	A 5 55	A 6 55		
PSOUT1	A 1 29	B 3 2	B 4 2				
PSP1A	A 1 33	B 1 3					
PSP1B	A 1 4	B 1 32					
PSP1C	A 1 34	B 1 33					
PSP1	A 1 3	A 3 2	A 4 2	A 5 2	A 6 2		
PSP2A	A 1 57	B 1 6					
PSP2B	A 1 28	B 1 35					
PSP2C	A 1 58	B 1 36					
PSP3A	A 1 48	B 1 39					
PSP3	A 1 18	B 1 9					
PSP4A	A 1 56	B 1 41					
PSP4	A 7 2	A 7					
TTL001	A 7 39						
UNSR	B 3						
ZZZ001							
ZZZ002							

DRAWING	SUB	SHEET NO	SHEETS



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