RAMP FUNCTION GENERATOR DWG #1684A62

I. INTRODUCTION

The Ramp Function Generator card #1684A62 is a rate control circuit which can be used in either a drive controller or in a master director. This card controls the maximum rate at which a reference is applied in the system by changing a step input reference to a ramped output reference. Generally this card is used in conjunction with other sequencing and calibration circuits for proper application of the required signal.

Figure 1 is a picture of the Ramp Function Generator card. A front view locating all components by schematic identification is shown on the last page of the instruction leaflet.

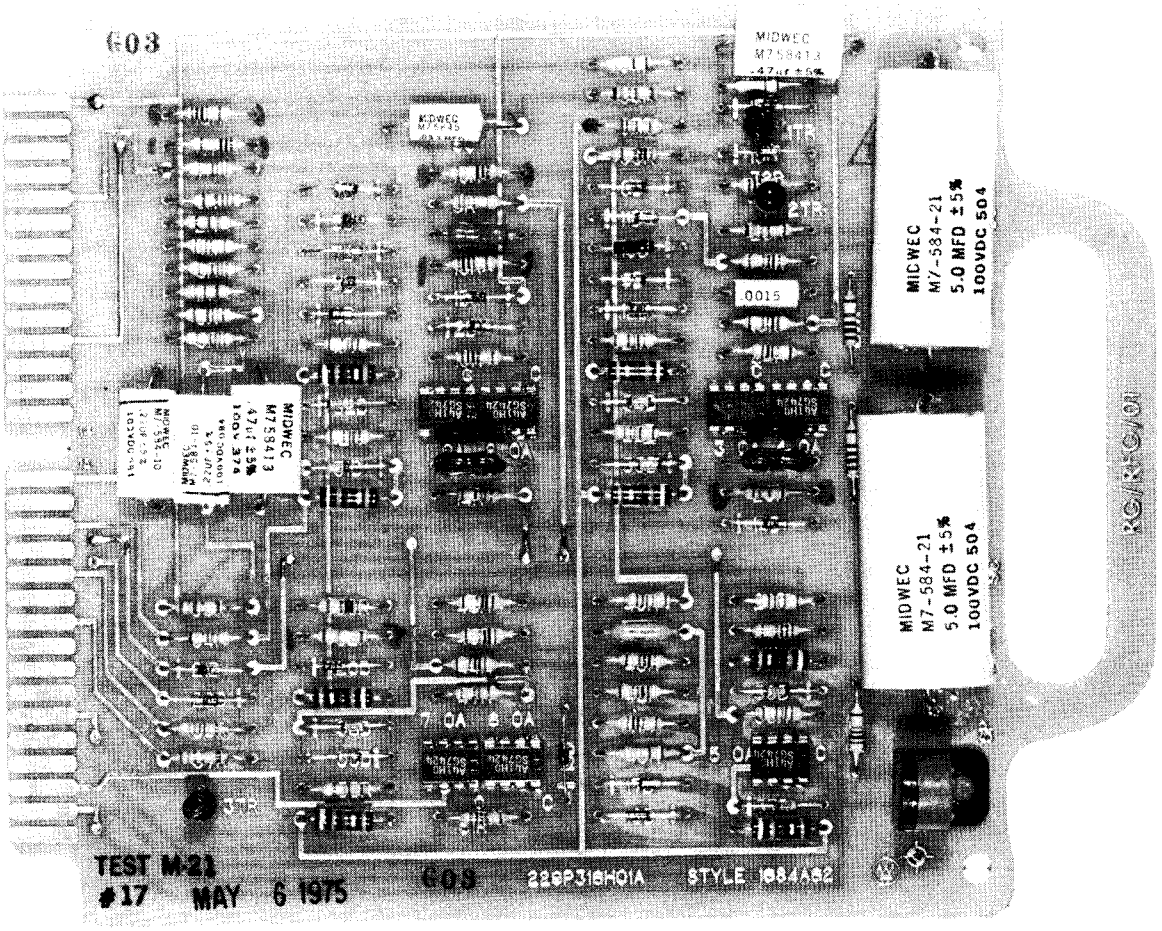


FIGURE 1

EFFECTIVE DATE: June, 1975

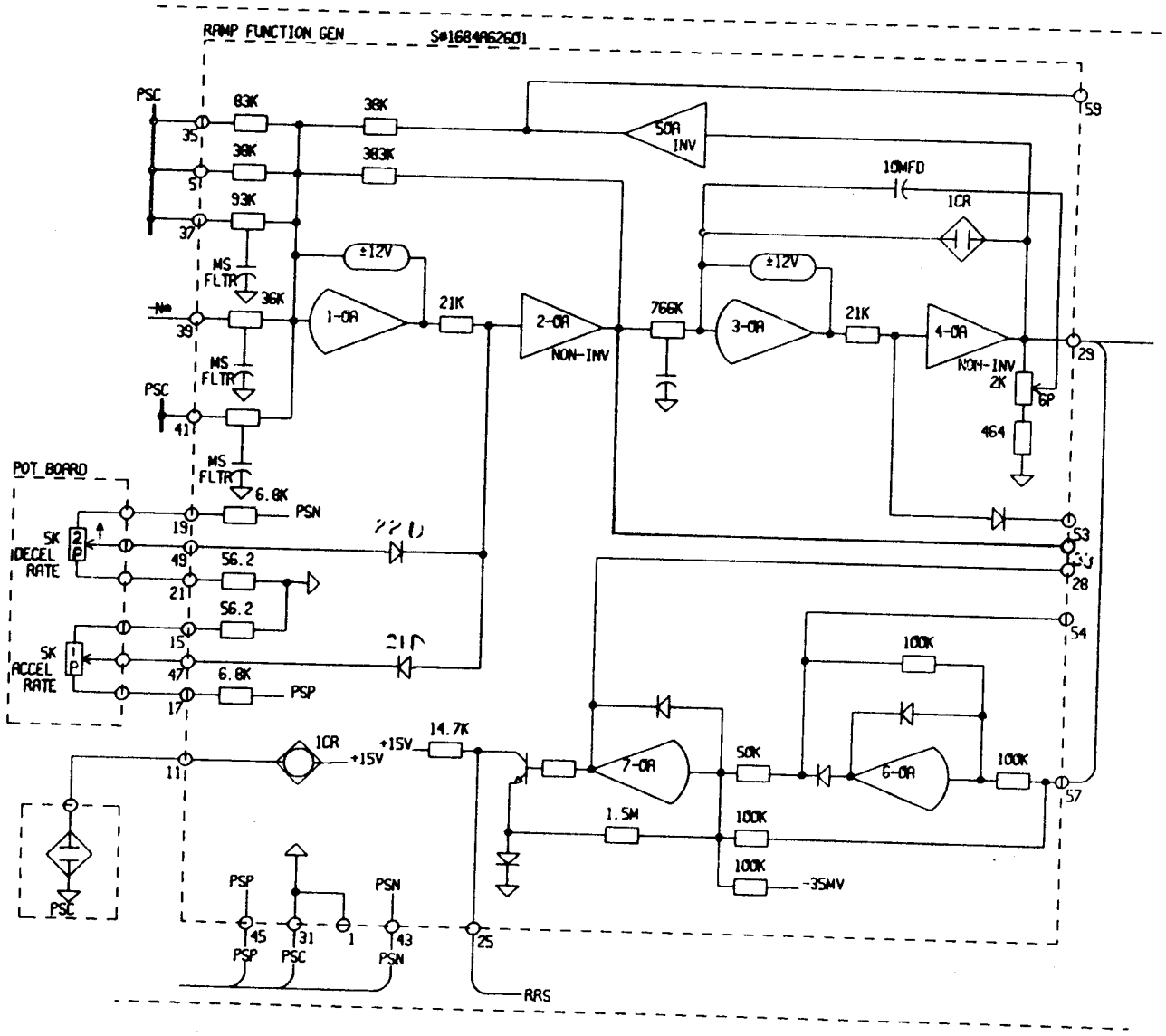


FIGURE 2: SIMPLIFIED SCHEMATIC DIAGRAM

II. DESCRIPTION OF OPERATION

Figure 2 is a simplified schematic representation of the functional circuits on this card: a three amplifier ramp circuit and a zero voltage detector.

Amplifiers 1-0A through 5-0A and the associated components comprise the rate control circuit. Amplifiers 1-0A and 2-0A function as a high gain error amplifying stage. The output from this stage (also on terminal 33) is the time derivative of the output voltage. Externally mounted potentiometers, 1P and 2P as shown on Figure 2, provide adjustable limits on the output signal from the error amplifying stage. Amplifiers 3-0A and 4-0A function as an integrator circuit. Potentiometer 6P can provide a 6 to 1 variation in the integration time constant depending upon the group selected. This stage has a reset function which is applied when a "0" logic signal is applied to terminal 11. A "0" on terminal 11 energizes static relay 1CR whose contacts short out the integrator. If the reset function is used, the appropriate system signal must be applied to terminal 11. Amplifier 5-0A is an inverting buffer which is used to generate the correct polarity signal required in the error amplifying stage.

A step signal at an input terminal (5, 35, 37, 39 or 41) drives 1-0A into limit voltage (±12V) and the input to 2-0A is determined by the voltage limit pots connected to diodes 21D and 22D. The integrator sees a constant error voltage which it integrates. 1-0A stays in limit until the ramped output of 5-0A matches the input reference level. At this time (zero error) 1-0A output goes to zero and the input to the integrator stage is regulated for zero volts.

As this is a rate control circuit, the output signal will follow the input signal in a linear fashion for slowly changing signals. The linear equation for the circuit is:

$$\epsilon_o = \frac{1}{k} \cdot \epsilon_i \cdot \frac{1}{1 + ST}$$

$$k = \frac{R_i}{38} \qquad R_i \text{ in k ohm}$$

$$T = \frac{T_I}{kA} \qquad T_I \text{ integrator time constant}$$

$$A \text{ gain of error amplifier}$$

When the input dv/dt is faster than the integrator output rate, the circuit changes into a non-linear operating mode.

Drawing S#1684A62 is a multi-group assembly drawing. The various group options provide a range of operating ramp times which are required for various applications.

Amplifiers 6-0A and 7-0A and the associated circuitry provide a zero volt detection circuit for the ramp output signal. As shown in Figure 2 the ramp output signal has to be wired to this circuit. An internal bias of 50mV is used as the switching point. If the ramp output is greater than 50mV, transistor 3TR turns off causing a +15V logic signal to appear at terminal 25. When the output voltage is less than 50mV, transistor 3TR turns on and the logic level at terminal 25 switches to zero volts.

III. APPLICATION CONSIDERATIONS

The output of 1-0A is connected to voltage limiting diodes 21D and 22D. 1P and 2P as shown connected provide control of the accel and decel rates by clamping the output voltage of 2-0A. These potentiometers provide a 10:1 adjustment for the limit voltage. For multiple selectable ramp rates, some sequencing method must be used to connect the desired signal levels to the appropriate limit diode. Depending upon the group selected, 6P may provide an additional 6:1 variation in ramp rate.

The output at terminal 29 provides a reference ramp with sharp discontinuities at the beginning and at the end. If these discontinuities are undesirable from an operation standpoint, the output signal must be processed through a time delay circuit.

V. CHARACTERISTICS & RATINGS

A. Power Supplies:

PSP	+24V	±5%	@	95 ma.	Except G07	+15V ±5% @ 50ma	G07 Only
PSN	-24V	±5%	@	90 ma.		-15V ±5% @ 50ma	

B. Inputs:

Terminal #	Volts	Input Impedance	Output Input Gain	Filter Time Const.	Output Signal Type
35	±23.7	82.5k	.464	None	Analog
37	±26.6	92.8k	.413	*	Analog
39	±10.2	35.6k	1.08	1.96ms	Analog
41	±22	76.6k	0.50	4.21ms	Analog
5	±11	38.3k	1.00	None	Analog
57	±11	50k	Not Appl.	None	Logic

* For Groups G01, G02, G03, G05, G07 10.9ms
For Groups G04, G09 2.3ms

C. Outputs:

Terminal #	Volts	Output Loading (Max.)	Signal Type
T29	±11	0.5ma	Analog
T33	±11	4.8ma	Analog
T59	±11	4.6ma	Analog
T25	+15V		Logic "1"
	+.5V		Logic "0"

D. Ramp Rates:

Group No.	Time to Ramp from 0V to 10V Without Voltage Limit at T49, T47	(Pot 6P) α
01 & 07	7.66 sec.	1
02	1.4 sec.	.189
03	2.94 sec.	1
04	20.00 sec.	1
05	20.00 sec.	1
08	0.32 sec.	1
09	0.155 sec.	.189
	6.32 sec.	1
	0.114 sec.	1
	0.013 sec.	.115

E. Output Errors

Errors associated with the offset parameters of 1-0A may cause a worst case error of ±10.5mV to appear on terminal 59. This would be a deviation from the ideal set point.

Errors associated with the offset parameters of 5-0A may cause a worst case error at ±6mV on terminal 29 with respect to terminal 59.

Worst case gain error through the ramp is ±2%.

Worst case gain error due to temperature variation of the gain resistors is ±0.25% over the allowable temperature range.

F. Ramp Rate Variation & Linearity

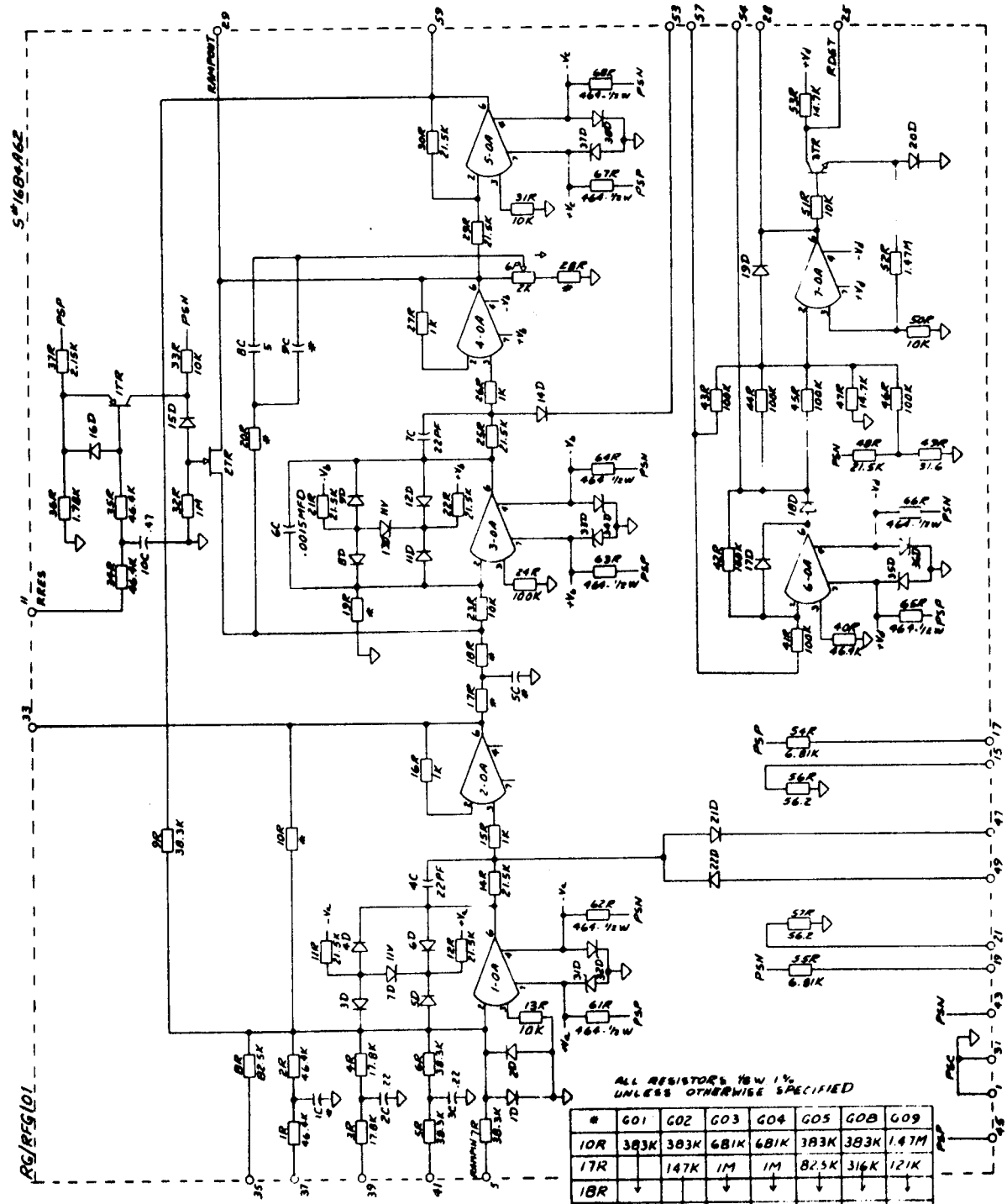
Due to component tolerances: ±6% max.
Due to temperature changes in association with the RC components: ±2.9% max.

Drift characteristics due to offset variation in integrator amplifier: ±10mV/sec.

When the input to the integrator is limited by external pots, diode voltage temperature changes (-3mV/°C max) will cause errors in ramp rates which will have the greatest percentage error at the ±1V level.

For a particular set of conditions (stable temperature) the ramp linearity will be within ±0.1% of the set rate until the first stage comes out of limit at which time the ramp will change to an exponential function in reaching its steady state value.

G. Allowable ambient temperature 0°C to 55°C.



#	G01	G02	G03	G04	G05	G08	G09
10R	383K	383K	681K	681K	383K	383K	1.47M
17R		147K	1M	1M	82.5K	316K	121K
18R							
19R	121K		100K	100K	261K	121K	261K
20R	2.15K	1K	1.78K	1.78K	3.83K	2.15K	1.21K
28R	464	100K	100K	100K	464	100K	261
1C	.47	.47	.47	.1	.47	.47	.1
5C	.1	.15	.033	.033	.047	.15	.01
9C	5	5	5	5	–	5	–

FIGURE 3A: DETAIL SCHEMATIC DIAGRAM

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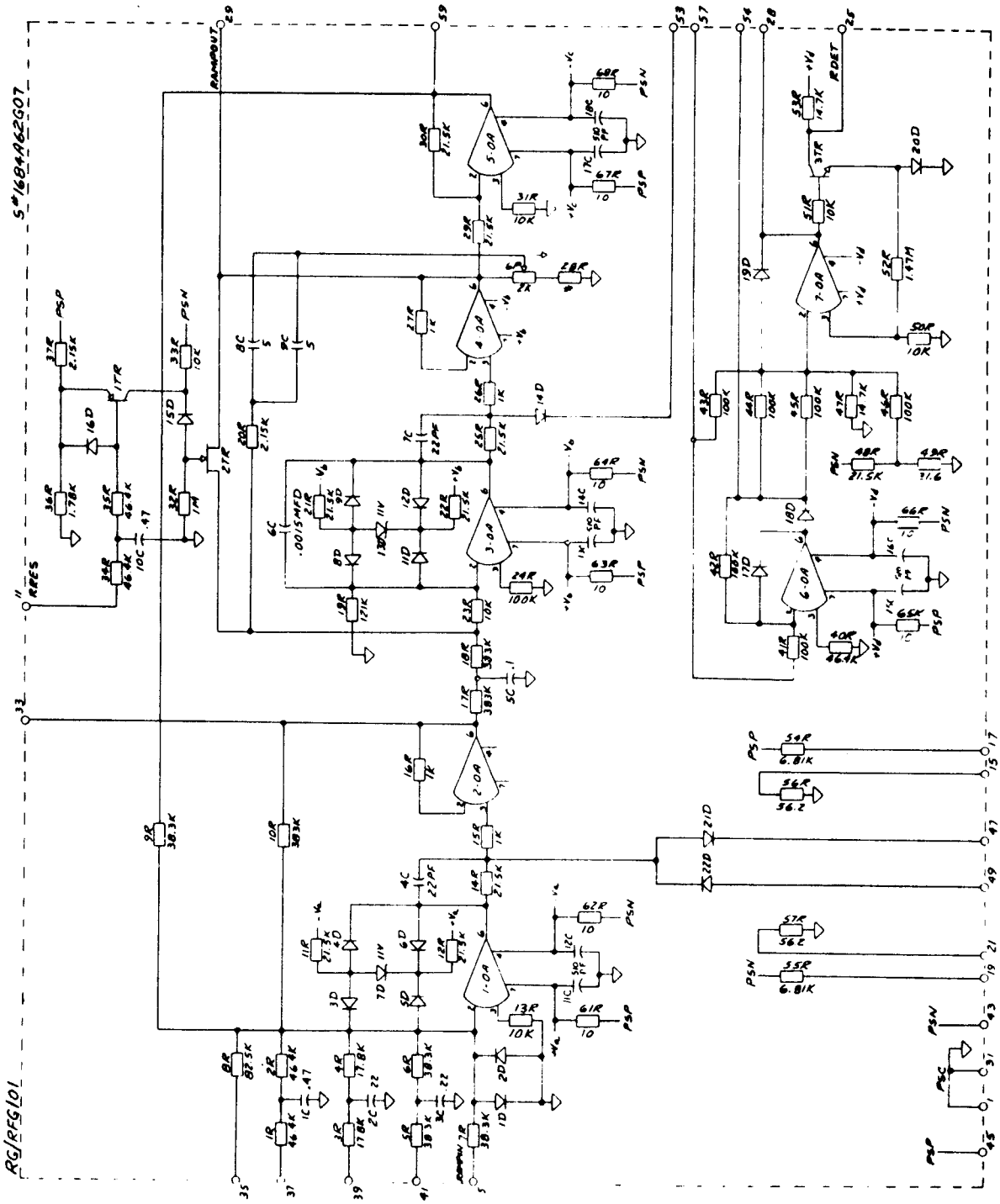
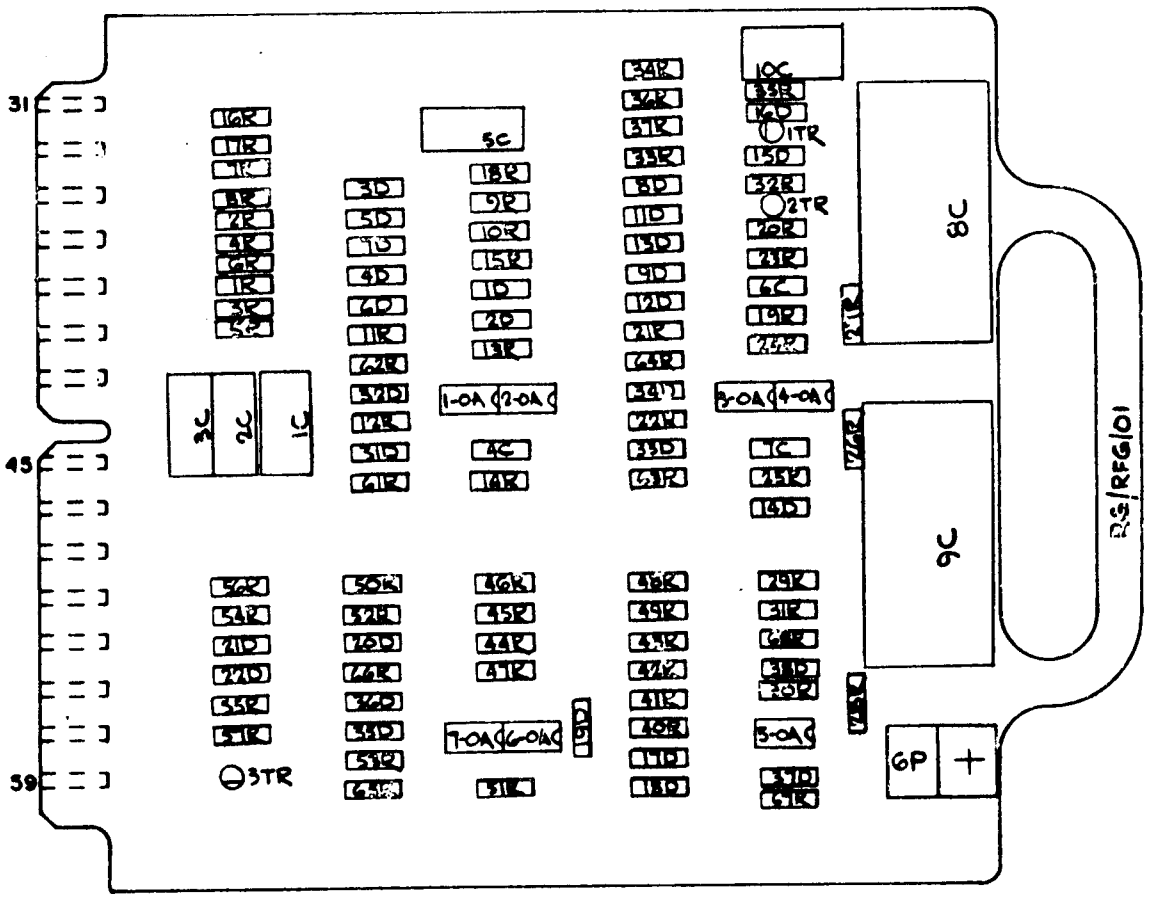


NOTE: POWER SUPPLY VOLTAGES
ARE ±15V FOR G07

FIGURE 3B: DETAIL SCHEMATIC DIAGRAM


31
45
59
3C
2C
1C
5C
8C
9C
1-0A
2-0A
3-0A
4-0A
5-0A
6-0A
7-0A
3TR
1TR
2TR
6P
RS/RFG101