GATE PULSE GENERATOR

I. INTRODUCTION

A general purpose gating system which utilizes a linear ramp for phase control and which can provide phase control ranges of 150°, 180° or 210° is comprised of the Thyristor Gate Driver S#1668A25, the Gate Pulse Generator S#1671A17 and the Gate Synchronizer S#1684A02 (S#1684A05 for 50 hz).

The Gate Pulse Generator (GPG S#1671A17) generates three output pulse trains spaced at 120° intervals for use in a three thyristor power module. A second duplicate GPG is required in a six thyristor power module to provide a total of six output pulse trains spaced at 60° intervals.

Figure 1 is a picture of the GPG. A front view locating all components by schematic identification is shown on the last page of the instruction leaflet.

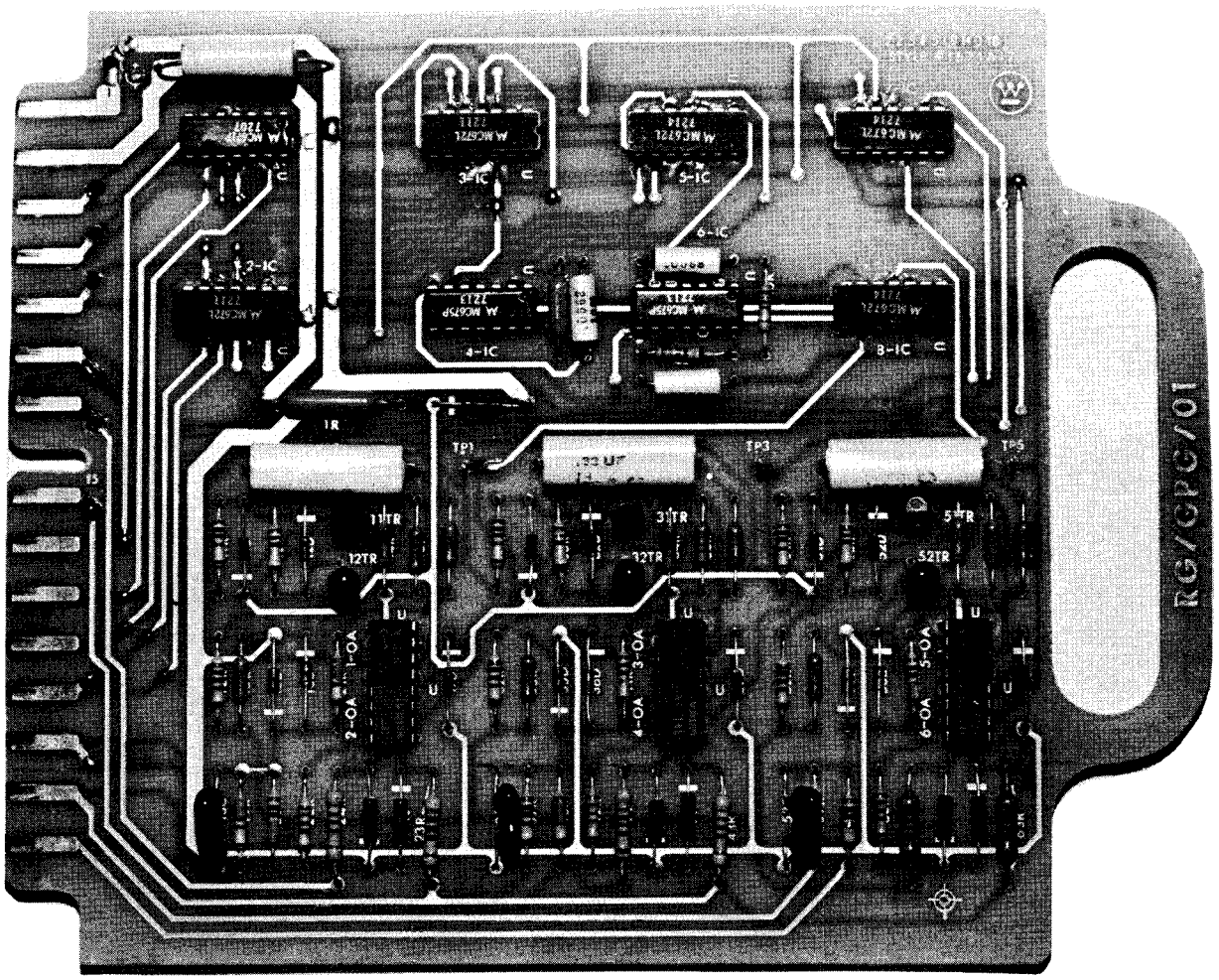

FIGURE 1

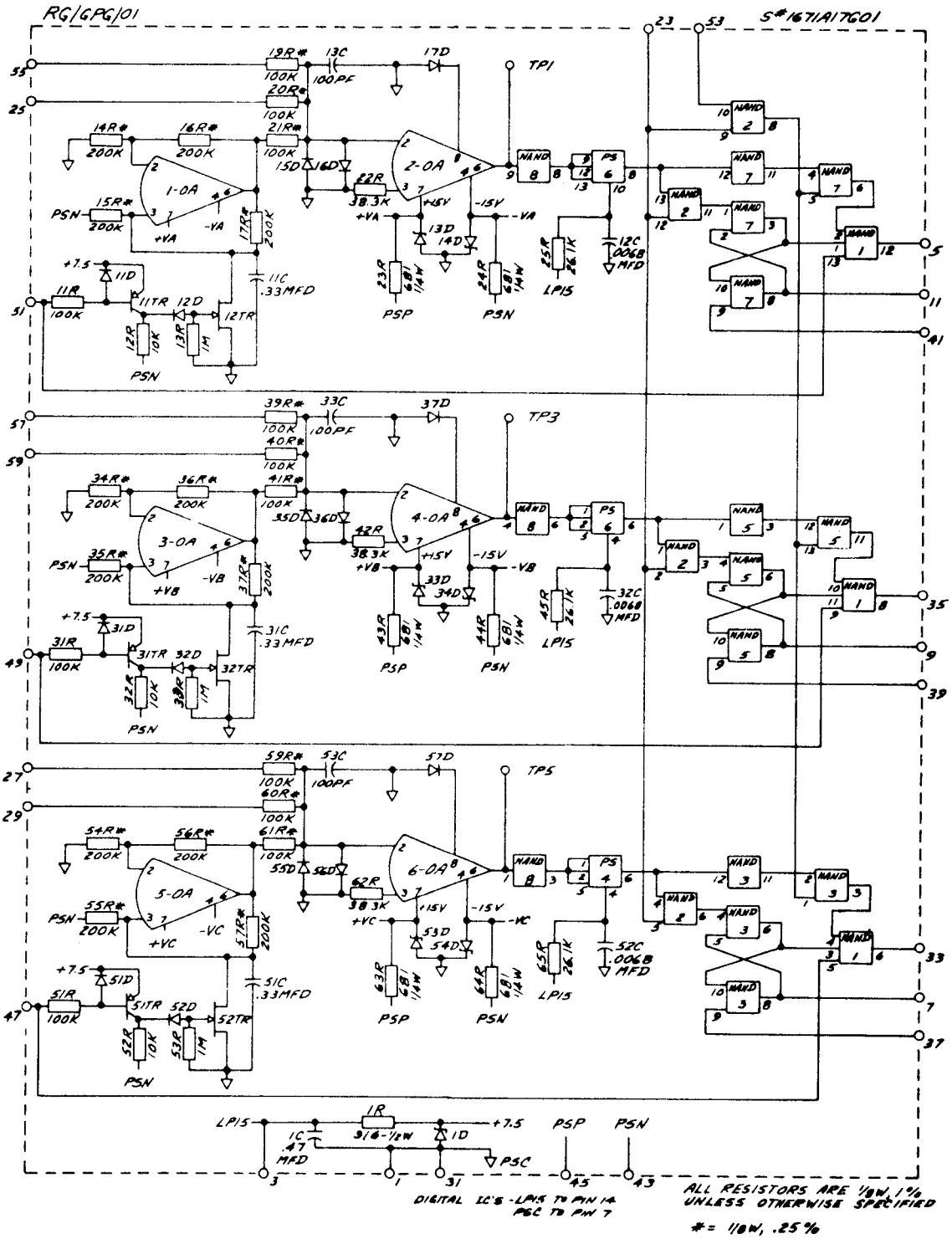
RG/GPG/01
S#1671A17G01
TP1
TP3
TP5
1-0A
2-0A
3-0A
4-0A
5-0A
6-0A
PSN
PSP
LP15
+7.5
-VA
+VA
-VB
+VB
-VC
+VC
+15V
-15V
NAND
PS
DIGITAL LC'S -LP15 TO PIN 14
PSC TO PIN 7
ALL RESISTORS ARE 1/8W, 1%
UNLESS OTHERWISE SPECIFIED
*= 1/8W, .25%

FIGURE 2

II. DESCRIPTION OF OPERATION

A. INTRODUCTION

The Gate Pulse Generator (GPG) is a system which generates gate pulses for power thyristors at the gating angle determined by an input control voltage. The conversion from the input control voltage to the output gating angle is done by the use of a locally generated linear timing ramp. The timing ramp is synchronized to the power thyristor's commutation voltage by an externally supplied synchronizing signal.

Each GPG pc board has three identical generator circuits providing for picket fence pulse trains spaced at 120^0 intervals. For a six pulse system an additional GPG pc board is used. A complete gating system requires a synchronizing function and an amplifier which drives the power thyristor with the picket fence pulse train.

B. DESCRIPTION

1. Gate Pulse Generation

For purposes of illustration a functionalized circuit diagram is provided by Figure 3.

a. Synch.

SYNCH is a digital input signal which is in synchronism with the commutation voltage of the power thyristor whose gating angle is to be controlled. When SYNCH is a logic 1, the static relay (a Field Effect Transistor) is open allowing the capacitor C to be charged by the constant current source I

b. Timing Ramp

The voltage on the capacitor is a highly linear negative going ramp from which the gating angle can be determined. The ramp is fed into voltage comparator VC along with the control voltage V(C)'. The point on the ramp at which the comparator switches from a logic 0 to a logic 1 is controlled by V(C)'. The comparator is reset when SYNCH goes to a logic 0, which closes the static relay discharging capacitor C.

c. 50 μSec Hard Pulse

The logic 1 of the comparator is "shrunk" by the pulse shrinker PS to a pulse 50 μSec long. This pulse serves as the hard first pulse of the picket fence pulse train as well as to set flip-flop 1-FF. The hard pulse is OR'ed with an externally supplied oscillator signal and then this signal is NAND'ed with the Q output of flip-flop 1-FF to form the picket fence pulse train.

The purpose of the 50 μSec hard first pulse is to assure that the initial pulse applied to the power thyristor gate is adequate to gate the device completely ON for any load conditions. The oscillator signal, which contributes the remainder of the pulse train, is not synchronized with the gating angle or any other signal. Therefore, its phase and frequency relationship to the hard pulse is impossible to predict.

d. Ring Counter

Flip-flop's 1-FF, 2-FF and 3-FF are tied together in a ring counter. A flip-flop is turned ON (Q = 1) by its respective set signal (the 50 μSec pulse) and is turned OFF by the turning ON of the succeeding flip-flop. Consequently, the only one of the three channels that may generate a picket fence pulse train at any one time is the one in which the most recent 50 μSec pulse has occurred.

e. Tail end Chop

A third input is provided on the output NAND to prevent the picket fence pulse train from continuing past a critical gating angle regardless whether or not the flip flop has been reset. The action is performed by the negative transition of the SYNCH signals; i.e. when SYNCH = 0 the picket fence pulse train is chopped OFF, hence tail end chop. This feature prevents the power thyristor from being gated for an extended time while it is reverse biased.

Waveforms for a symmetrical three pulse system are shown in Figure 6.

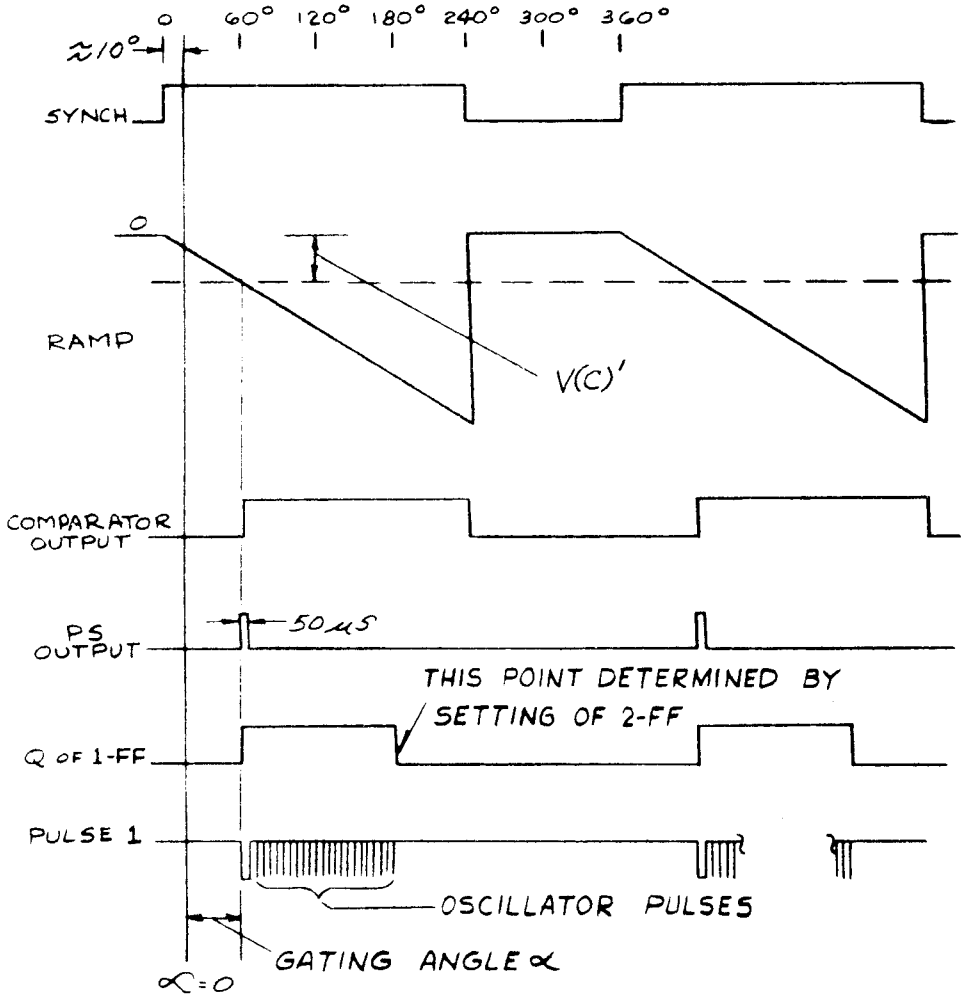

FIGURE 6

Advance and retardation limits on the gating angle α are fixed by voltage limits on V(C)'. The range of control for this system is sufficient for 0 to 210 degrees at 60 or 50 Hz. Note that the SYNCH signal releases the ramp approximately 10 degrees before α = 0. This prevents advance limit from occurring at the starting point of the ramp.

III. CHARACTERISTICS AND RATINGS

	MIN	MAX	UNITS
A. LOGIC DEFINITIONS			
Logic 1	+12.5	+15.0	Volts
Logic 0	0	+1.5	Volts
B. INPUTS			
1. Control Voltage V(C)' range	Preset by Gate Synchronzer		
input impedance/channel	100		k ohms
2. SYNCH switch to logic 1 at α =	-10^{o}	-10^{o}	
switch to logic 0 at α =	230^{o}	230^{o}	
frequency	45	65	Hz
digital load factor/channel		1	
3. $\overline{GPS}$ Logic 0 = Suppression of gate pulses digital load factor (total)		4	
4. OSC Waveform 			
digital load factor (total)		1	
C. OUTPUT			
1. Pulse 1, 2 and 3 Waveform 			
digital load factor/channel		8	
mismatch between channels at max α		4^{o}	
2. Ring Counter terminations (pins 11, 41, 9, 39, 7 & 37) use for interconnection purposes only.			
D. GAIN (over temperature range)			
1. Group 1: at 60 Hz $\alpha/V(C)'$	.51	.53	Rad/Volt
at 50 Hz $\alpha/V(C)'$	.42	.44	Rad/Volt
E. POWER SUPPLY REQUIREMENTS			
PSP (pin 45) Volts	+23	+25	Volts
Current		50	mA
PSN (pin 43) Volts	-23.99	-24.01	Volts
Current		60	mA
LP15 (pin 3) Volts	+13.5	+16.5	Volts
Current		70	mA
F. OPERATING TEMPERATURE	0	+55	^{o}C

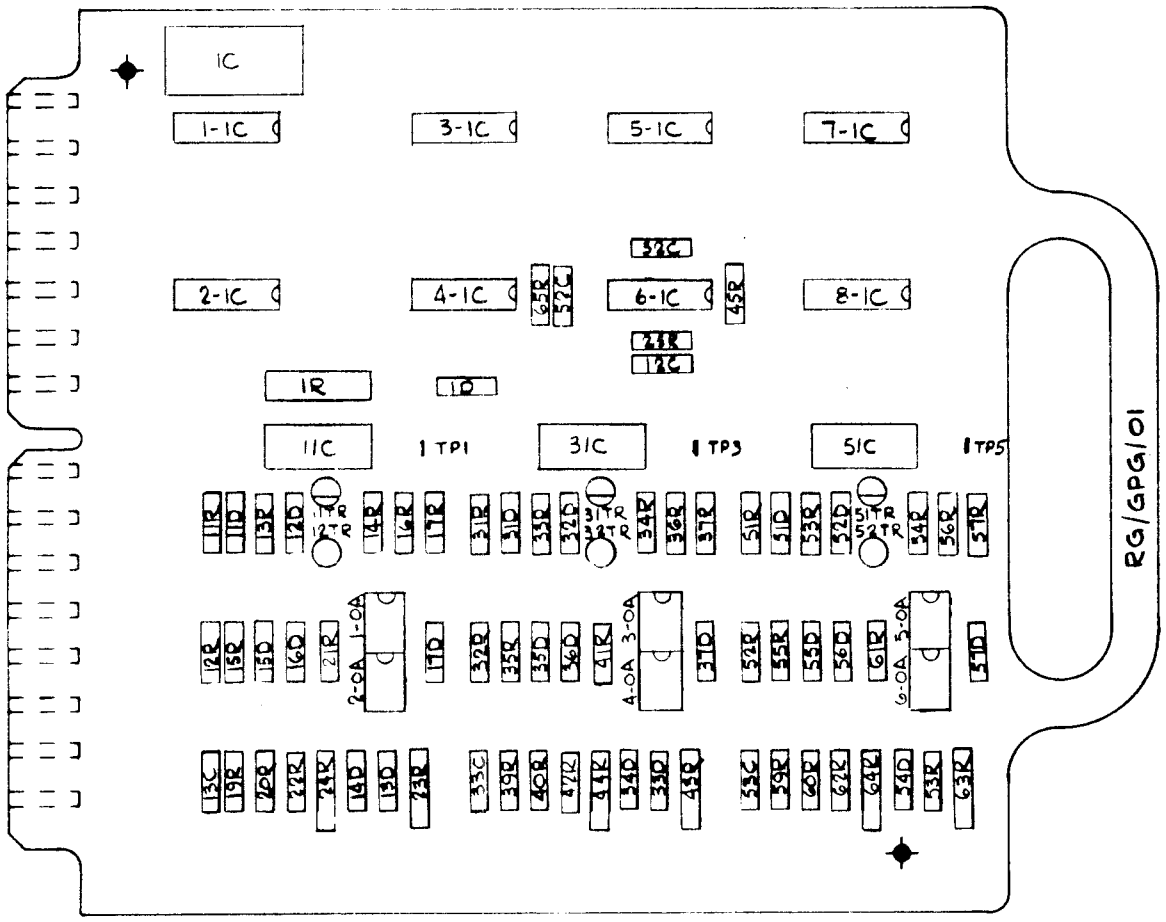
1C
1-1C
3-1C
5-1C
7-1C
2-1C
4-1C
6-1C
8-1C
1R
1D
11C
1 TP1
31C
1 TP3
51C
1 TP5
RG/GPG/01

FIGURE 7