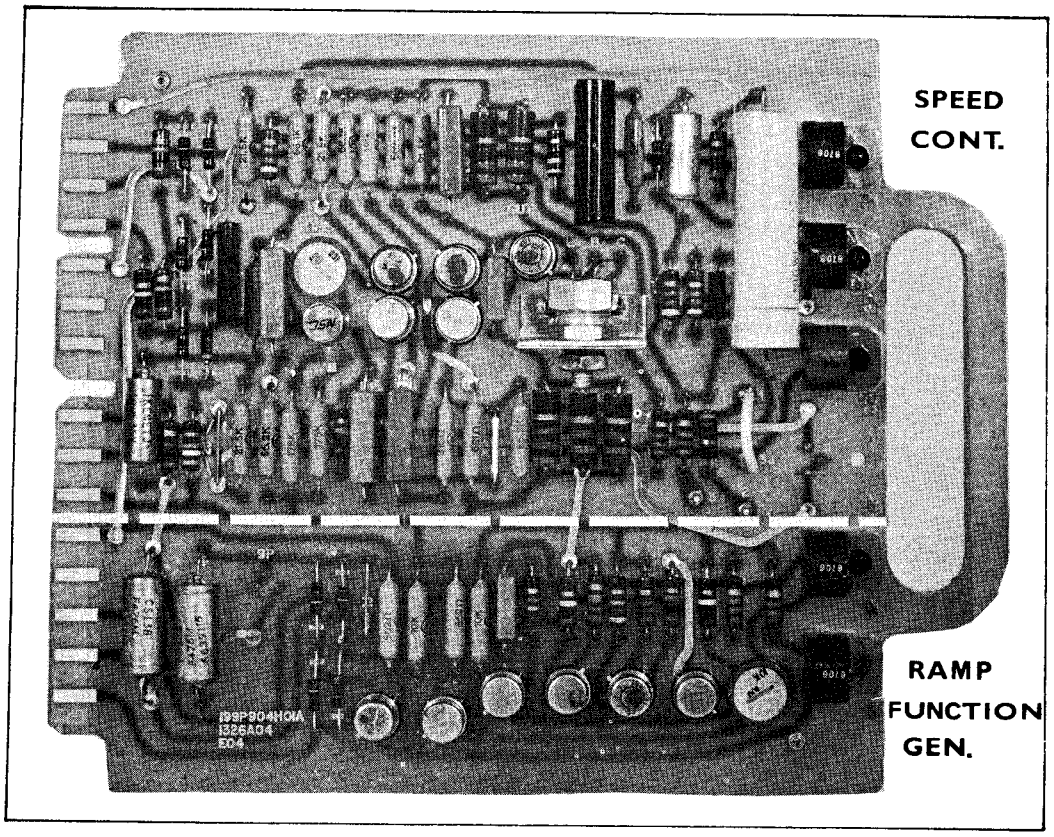
E04 SPEED CONTROLLER & RAMP-FUNCTION GENERATOR
For Use in S-56

I. INTRODUCTION

The speed controller and ramp-function generator card (E04) is one of four printed circuit cards comprising basic armature regulators for S-56 systems. Other standard cards, explained in separate instruction leaflets, are: E01, gate pulse generator; E02, current controller and gate pulse suppression; and E03, voltage controller.



E04 PC BOARD

Figure 1

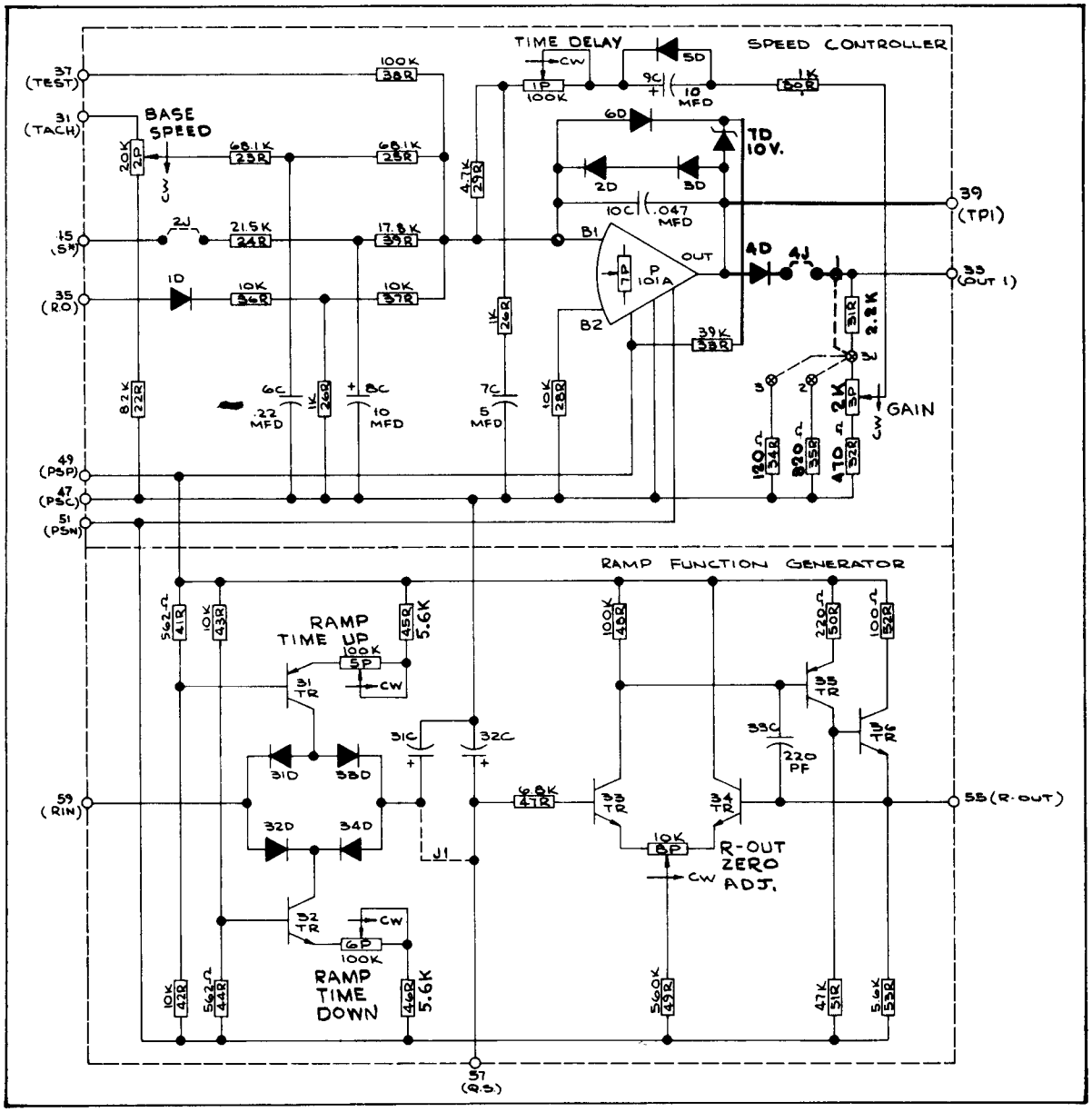
Figure 1 is a picture of the E04 printed circuit card as used in speed regulators with the ramp option. By adding or eliminating components, and changing jumper positions, the same board is used in all S-56 basic armature speed regulators or regulators requiring controlled acceleration and deceleration. Dotted lines delineate the two functions provided by the card which will be explained later in the instruction leaflet.

Printed circuit cards designed for S-56 systems are plug-in cards for insertion into AMP connector-type number 67131-1, or equivalent. Each card type (designated by "E" number) is uniquely keyed to prevent insertion in improper regulator positions. Over-all board dimensions are 6" X 7.6". A handle is machined in the card which facilitates insertion or removal, and

prevents inadvertant component breakage or board contamination. All electrical inputs and outputs are taken through the 15 terminals located at the rear edge of the card. Reading from top of the pc card to the bottom, terminals will always be identified on schematics by numbers 31, 33, 35, 37, ... 59. Potentiometers required for system adjustments are right-angle pots located along the front edge of the pc card.

II. DESCRIPTION

The two functions provided by the E04 card were outlined on Figure 1 and will be explained with reference to the schematic diagram, Figure 2.



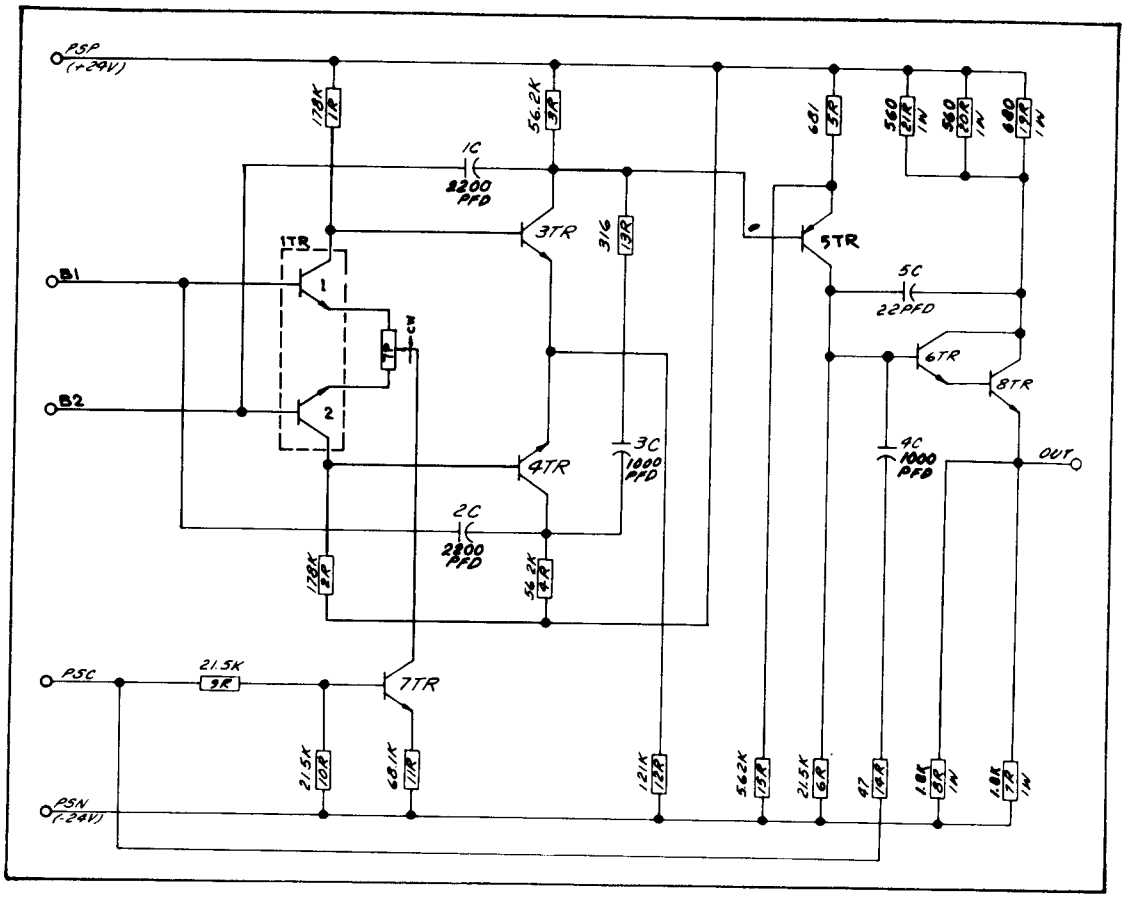
E04 SCHEMATIC DIAGRAM
FIGURE 2

A. Speed Controller

DC amplifier P101A and associated feedback components comprise the speed controller used in S-56 parallel regulators. A general discussion of operational amplifiers is contained in I.L. 16-800-48.

1. P101A

Figure 3 is the schematic diagram of the P101A.



P101A DC AMPLIFIER
FIGURE 3

With B2 connected to PSC through a resistor, a small signal applied to B1 is amplified through three stages. The first two stages are differential stages, including dual transistor 1TR and transistors 3TR and 4TR. The third stage includes transistor 5TR. A dc open-loop voltage gain of 20,000 is achieved by these three stages. The last stage, including 6TR and 8TR, provides current gain for the amplifier.

It should be noted that a plus voltage into B1 gives a minus voltage output. (Output signal inverted.)

Printed in USA

7TR serves as a constant current generator, forcing equal and opposite current changes in sections 1 and 2 of 1TR. A similar effect is provided by resistor 12R on transistors 3TR and 4TR.

The various capacitors, with their related resistors, serve as shaping networks to optimize frequency and phase-shift characteristics of the amplifier.

Balance pot 7P is provided to zero the output of the amplifier for zero input.

2. Controller Function

Feedback components associated with the P101A (see Figure 2) commit its use as a P.I.D. controller. The general form of the transfer equation is:

$$\frac{e_{out\,1}}{e_{TACH}} = -\frac{(1 + T_2p)\,(1 + T_3p)}{T_1p\,(1 + T_4p)}$$

$T_1 = K(23R + 25R)9C \approx 3.0 \times K$

$K \leq 1$ as determined by gain pot 3P and the position of 3J.

$T_2 \approx (1P + 29R + 30R)9C$ -- adjustable by 1P to cancel system mechanical time delays in the range: $1.1s \geq T_2 \geq .06s$.

Response of the speed loop is adjustable by 3P and 1P from approximately 100 ms to 200 ms.

$T_3 \approx (29R + 26R)7C = 28.5$ ms and approximately cancels the armature time delay.

$T_4 \approx 26R \times 7C = 5$ ms noise filter negligible for systems calculations.

Approximations for T_2, T_3, and T_4 above are valid when $1P \geq 10K$.

To prevent the amplifier from saturating, the output voltage is limited to +1V by 2D and 3D, and -10.5V by 6D and zener diode 7D. Diode 5D prevents reverse voltages from being developed across electrolytic capacitor 9C, and capacitor 10C limits the speed controller output response for step inputs.

Diode 4D is the switching diode for the speed controller function. Required reverse biasing of 4D is provided through 18R in the E02 pc board, I.L. 16-800-106. Removable board jumper 4J disconnects the speed controller allowing performance of voltage and current loops to be independently checked.

Terminal 35 is connected to the output of the voltage controller E03, closing a control loop which prevents speed undershoot normally encountered while decelerating under light load. This is further explained in I.L. 16-800-100.

3. Characteristics and Ratings

a) Allowable operating ambient range: 0 to 55°C

b) Output: $V_{OUT\,1}{}_{(35\text{-}47)}$: -10.5 ± 0.7V
$+ 1.0 \pm 0.4$V

I_o max = 5 ma

Drift at B1: 0.01 μA/°C maximum.

Printed in USA

c) DC Power Requirements: +24V ±1.2V --- 50 ma maximum
-24V ±1.2V --- 50 ma maximum.

d) Gain Adjustment Range: 3J pos. 1 --- $5 \geq \frac{1}{K} \geq 1$

3J pos. 2 --- $25 \geq \frac{1}{K} \geq 5$

3J pos. 3 --- $125 \geq \frac{1}{K} \geq 25$

e) With a reference input of 10V (V_{45-47}) at base speed, adjustment of 2P allows tach voltages; $105 \geq V_{31-37} \geq 35V$ to be accommodated.

B. Ramp-Function Generator

The ramp-function generator produces a linear change in output voltage from any abrupt change in input voltage. This is accomplished by providing a constant charge or discharge current to a capacitor.

1. Constant-Current Generator

Transistors 31TR, 32TR, and associated bias networks comprise two constant-current generators which govern the charge and discharge current for 31C and 32C. Magnitude of charging and discharging currents are independently adjustable (by 5P and 6P respectively) and may be calculated by the following equation:

$$i_{charge\ \mu a} = \frac{\left[\left(|V_{psp}| + |V_{psn}| \times \frac{41R}{41R + 42R}\right]\right. - V_{BE\ (31TR)}*}{45R + 5P}$$

V_{BE} = Base emitter drop of 31TR

5P = Resistance of 5P in the emitter circuit

* Discharge current may be calculated in the same manner using components associated with 32TR.

Outputs from the two constant-current generators are switched by diodes 31D, 32D, 33D, and 34D. With no error voltage signal between V_{59} and V_{57}, the difference current between the two generators flows through, or is derived from the input. A positive error voltage (V_{59} plus with respect to V_{57}) reverse biases 31D and 34D shunting the constant current preset by 5P to charge 31C and 32C. Similarly, a negative error voltage reverse biases 32D and 33D forcing the capacitors to discharge the constant current preset by 6P.

The time required to change from one voltage level to another may be calculated from the equation below:

$CV = i\Delta t$

where: C = total capacitance 31C + 32C

V = change in voltage level

i = charge or discharge current as previously calculated.

2. Amplification

Transistors 33TR, 34TR, 35TR, and 36TR form a three-stage power amplifier, whose output (V_{55-47}) follows the voltage across 31C. The input impedance of the amplifier is high, which minimizes loading of the constant-current generators and insures good ramp linearity. A differential amplifier stage (33TR and 34TR) was used as an input stage to minimize drift with changes in ambient temperature. Due to difference in base emitter drops of 33TR and 34TR, there can be an output from the power amplifier with zero input. 8P allows the differential stage to be slightly unbalanced to zero the output.

Terminal 57 is brought out to allow 31C and 32C to be quickly discharged through a low resistance when the drive is turned off. This insures all start ups will begin with zero reference.

Controlled acceleration and deceleration is optional and may be required by voltage, speed, or current regulators. As such, the E04 pc board may consist of only components essential to ramp generation, only the speed controller function, or a combination of the two. Three-coarse ramp ranges are determined by combinations of capacitors for 31C and 32C, each having an adjustment range of 6:1 by 5P and 6P. The seven combinations of board configurations to satisfy all requirements are listed in Figure 4.

Style No.	Eliminated	Jumpers Used	31C	32C	Ramp Time (sec.)
1326A04G01	Speed Controller	1J	47 mfd	47	8 to 50
1326A04G02	Speed Controller	1J	47 mfd	None	4 to 25
1326A04G03	Speed Controller	1J	22 mfd	None	2 to 12
1326A04G04	Ramp-Function Generator	2J, 3J, 4J	None	None	-------
1326A04G05	None	1J, 2J, 3J, 4J	47 mfd	47 mfd	8 to 50
1326A04G06	32C	1J, 2J, 3J, 4J	47 mfd	None	4 to 25
1326A04G07	32C	1J, 2J, 3J, 4J	22 mfd	None	2 to 12

FIGURE 4

3. Characteristics and Ratings

a) Allowable operating ambient range: 0 to 55°C.

b) Output: V_{55-47} = +20V max. (unidirectional)
I_{55-47} = 10 ma maximum.

c) DC power requirements: +24V ±1.2V --- 15 ma maximum
-24V ±1.2V --- 15 ma maximum.

d) Ramp rates:

	Sec. Min.	Sec. Max.
G01 & G05	8	50
G02 & G06	4	25
G03 & G07	2	12

e) Drift: V_{55-47} = +1.5 mv/°C @ V_{55-47} = 0
= +5.0 mv/°C @ V_{55-47} = 20

f) Maximum driving source impedance: 1000 ohms.

III. SERVICE

Personnel familiar with electrical equipment utilizing semiconductors can isolate most problems using an oscilloscope, multimeter, and information contained in relative instruction leaflets.

Semiautomatic equipment is available at the factory to test static and dynamic performance of all edge-connected, printed-circuit cards. Generally, repair of modules is facilitated by returning them to:

Westinghouse Electric Corporation
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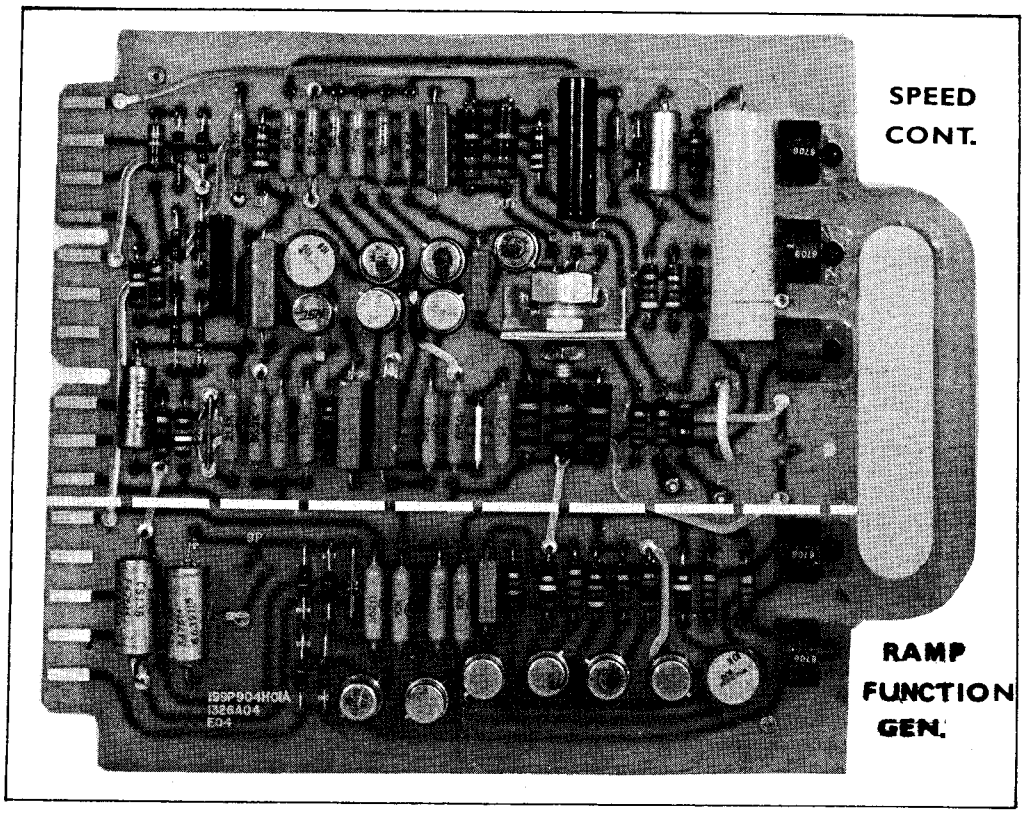

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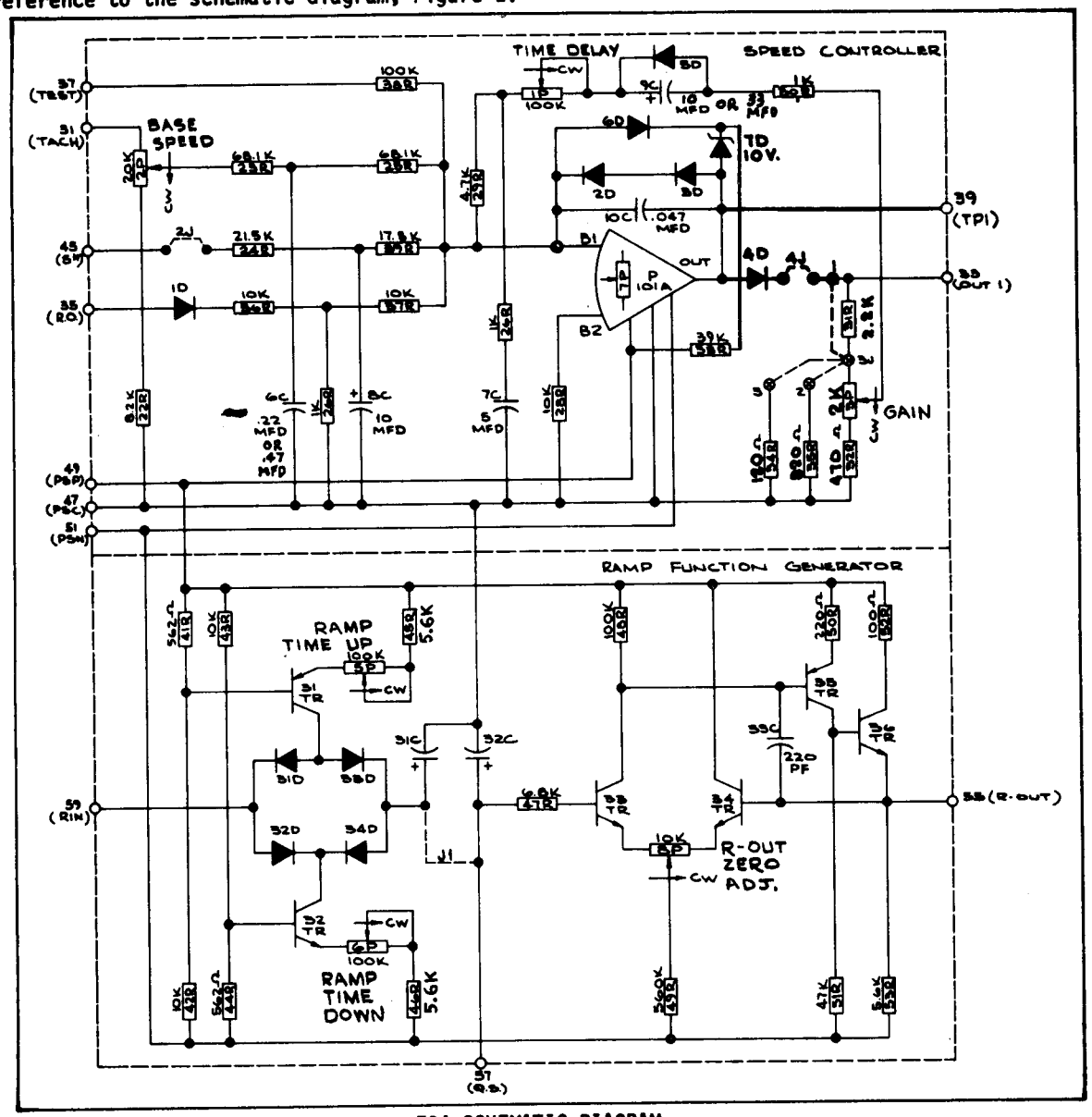

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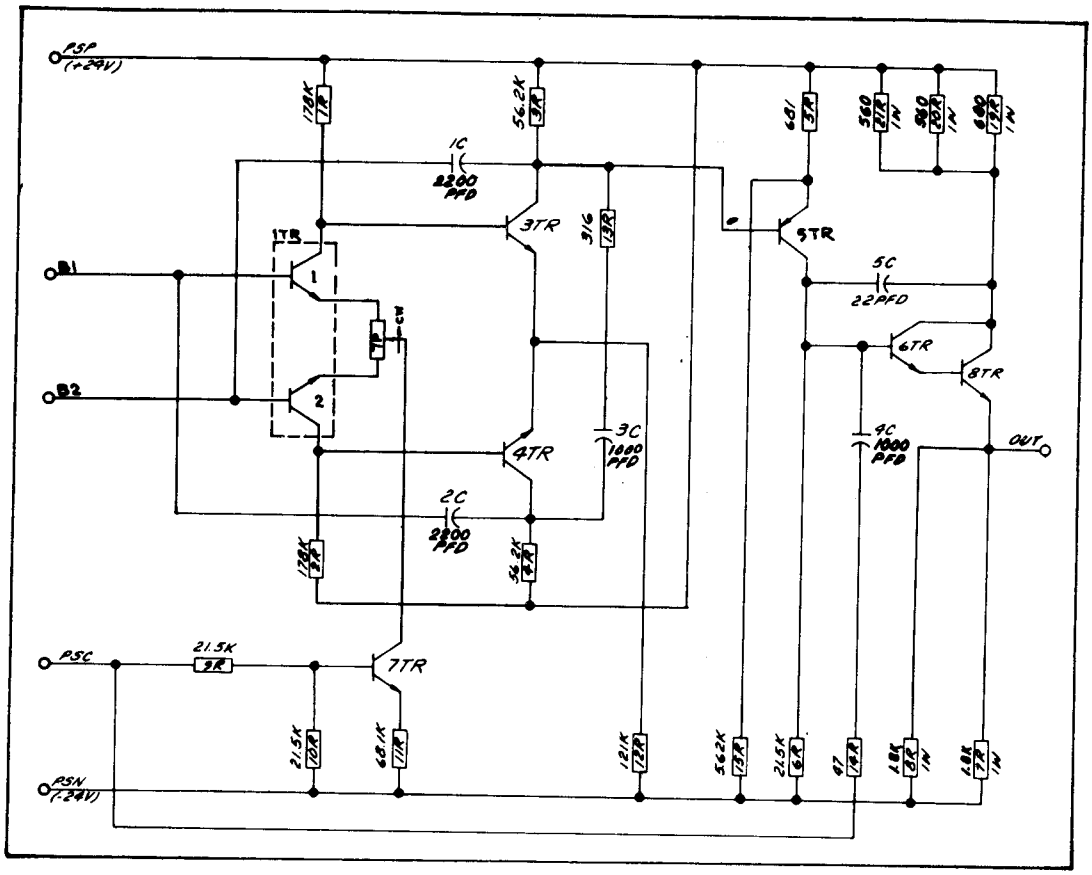

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$3.6s \geq T2 \geq 0.2s$ for G08, G09, G10 & G11

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Drift at B1: 0.01 µA/°C maximum.

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c) DC Power Requirements: +24V ±1.2V --- 50 ma maximum
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1326A04G06	32C	1J, 2J, 3J, 4J	47 mfd	None	4 to 25
1326A04G07	32C	1J, 2J, 3J, 4J	22 mfd	None	2 to 12
1326A04G08	Ramp Function Generator	3J, 4J	None	None	--
1326A04G09	None	1J, 3J, 4J	47 MFD	47 MFD	8 to 50
1326A04G10	32C	1J, 3J, 4J	47 MFD	None	4 to 25
1326A04G11	32C	1J, 3J, 4J	22 MFD	None	2 to 12

FIGURE 4

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I_{55-47} = 10 ma maximum.

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