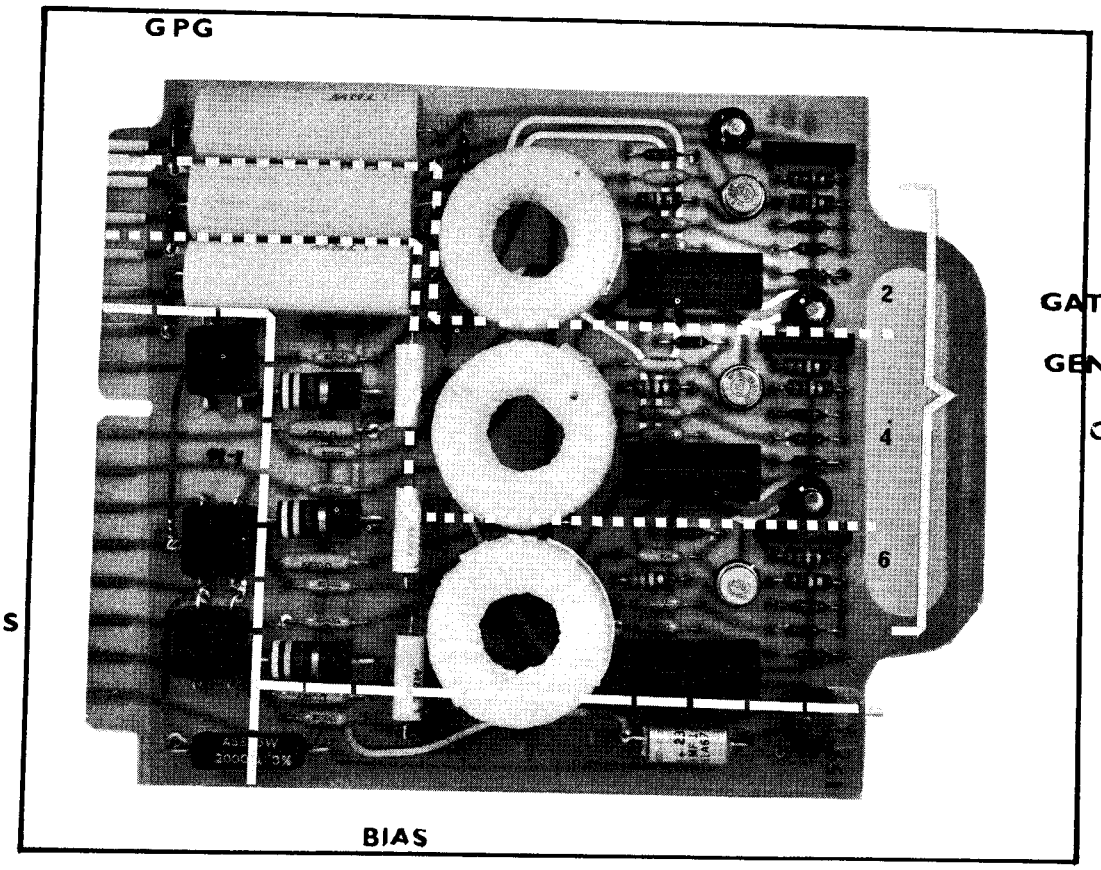
E01 GATE PULSE GENERATOR
For Use In S-56

I. INTRODUCTION

The gate pulse generator card (E01) is one of four printed circuit cards comprising basic armature regulators for S-56 systems. Other standard cards, explained in separate instruction leaflets, are: E02, current controller and gate pulse suppression; E03, voltage controller; and E04, speed controller and ramp-function generator.



E01 PC CARD
FIGURE 1

Figure 1 is a picture of the E01 pc card as used in armature regulators. Two groups are available: G01 for 60 Hz and G02 for 50 Hz. Broken lines delineate the three functions provided by the card which will be explained later in the I.L. (Dotted lines are also used to further breakdown the gate pulse generation to phases.)

Printed circuit cards designed for S-56 systems are plug-in cards for insertion into AMP, connector-type, number 67131-1 or equivalent. Each card type (designated by E number) is uniquely keyed to prevent insertion in improper regulator positions. Over-all board dimensions are 6" X 7.6". A handle is machined in the card which facilitates insertion or removal, and prevents inadvertant component breakage or board contamination. All electrical inputs and outputs are taken through the 15 terminals located at the rear edge of the card. Reading from the top of the pc card to the bottom, terminals will always be identified on schematics by numbers 31, 33, 35, 37 . . . . 59. Potentiometers required for system adjustments are right-angle pots located along the front edge of the pc card.

II. DESCRIPTION

The three functions provided by the E01 card were outlined on Figure 1, and will be explained with reference to the schematic diagram Figure 2.

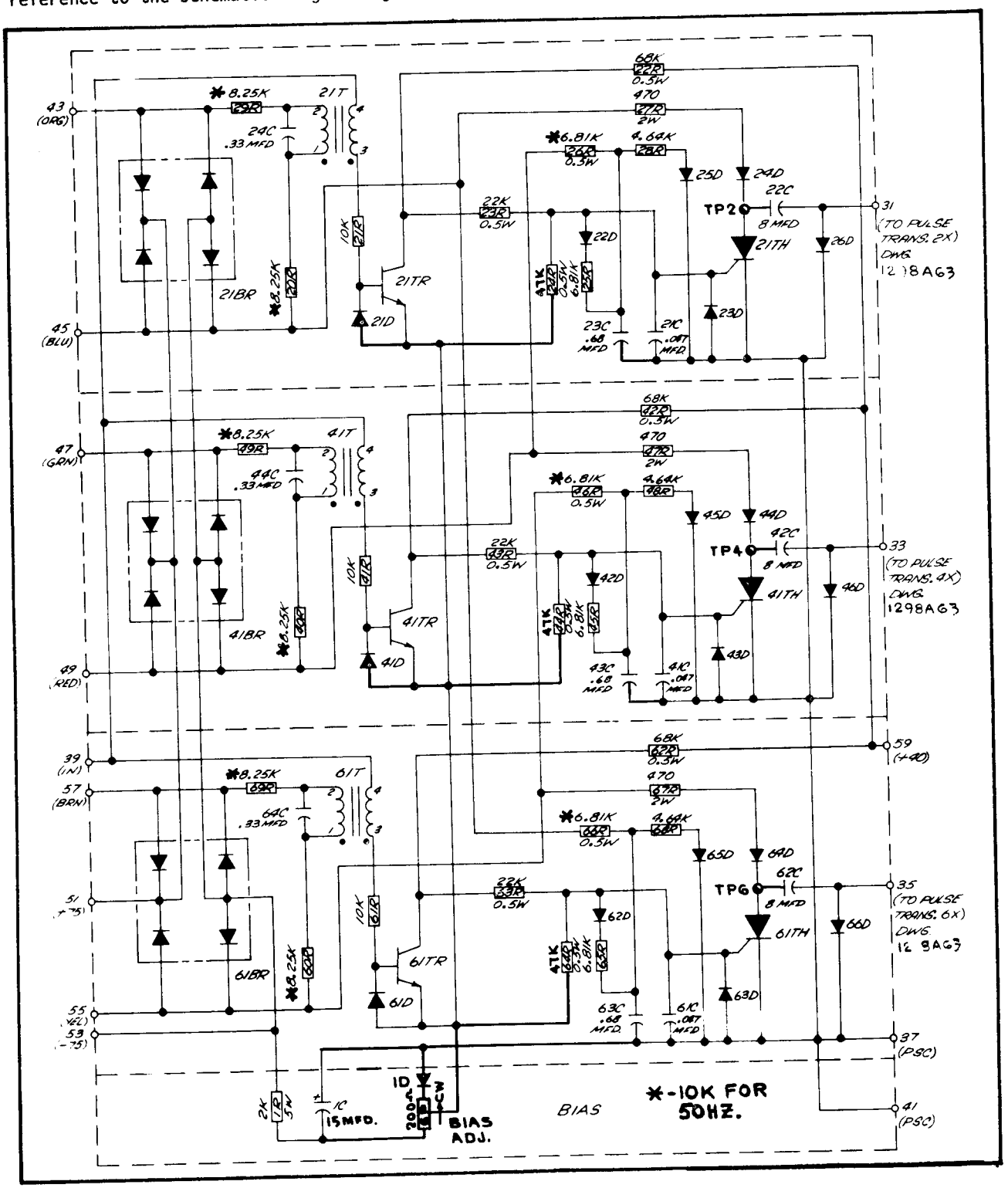


FIGURE 2

Two digits are used to identify most components on the pc card (eg. 21TH, 41TH, 61TH, 63D, 42R, etc.). The prefix digit designates the pulse number while the second digit differentiates between components of the same type. Components in the bias circuit common to all pulse generation are designated by single digits 1C, 1R, etc.

A. Power Supply

A gate control transformer, mounted in the rear of the basic regulator cage assembly, provides six-phase line-to-neutral voltages to terminals 43, 45, 47, 49, 55, 57 and 41 (neutral) of the E01 pc board. These voltages are rectified by two, six-phase, star rectifiers consisting of 21BR, 41BR, and 61BR producing an unregulated ±75 vdc at terminals 51 and 53 respectively. The ±75V is the basis of all dc voltages required by basic S-56 systems.

Regulated ±24 volts for controller modules is provided by zener regulating the ±75 vdc. Zener diodes, and filter networks which provide this function, are located in the rear of the basic regulator cage assembly and are explained in I.L. 16-800-101.

The +75 volts also feeds the E02 card and is reduced by voltage divider action to +40V. This voltage is returned to terminal 59 of the E01 pc card and provides collector voltage for 21TR, 41TR, and 61TR. When gate pulse suppression occurs (see I.L. 16-800-106), the voltage at terminal 59 is reduced to +0.5V, the gate cathode junctions of thyristors 21TH, 41TH, and 61TH are clamped to -0.5V, and further production of gate pulses is inhibited.

The -75 volts is applied to voltage divider 1R, 1P, and forward biased diode 1D developing an adjustable bias for the emitters of transistors 21TR, 41TR, and 61TR. Bias requirements are discussed in the following section.

B. GATE PULSE GENERATION

A phase control range of 180^{o} is required to achieve control of a three-phase bridge circuit from cut off to full output. The controlled interval must be from the point in time the thyristor becomes the most forward biased device in the bridge ($\alpha = 0$) to the point in time the cell next becomes reverse biased ($\alpha = 180^{o}$). Both the phase rotation of input power and the physical location of devices must be known to determine the required control interval.

Figure 3 defines the control interval for thyristor 2, having assumed phase rotation and a bridge configuration as shown. Also shown phase related, are voltage waveshapes within the E01 pc card pertinent to the generation of gate pulse #2. Regardless of main power transformer connections, the above relationship must exist and this is insured by proper selection of the gate control transformer.

Gate pulse generation will be explained with reference to the waveshapes in Figure 3 and Figure 4, a simplified schematic showing only components essential to the production of gate pulse #2.

The positive half cycle of the line-to-neutral voltage between terminal 43 and 41 is used to charge capacitor 22C. As can be seen by Figure 3, this occurs prior to the control interval previously defined. A gate pulse is produced by turning on thyristor 21TH and allowing 22C to discharge through the primary of pulse transformer 2X.

During the 180^{o} preceeding the control interval, gating must not occur. This is insured by the inhibitor voltage V_X which holds the gate of 21TH negative through diode 22D regardless of the signal at the collector of 21TR. The inhibit signal also sets the phase advance limit of approximately $\alpha = 10^{o}$. Pulses phase out at approximately $\alpha = 170^{o}$ due to amplitude distortion of the cosine voltage.

When the base emitter voltage of 21TR goes negative, the transistor cuts off. The resultant increase in collector voltage provides a positive gate to 21TH releasing a gate pulse as previously explained. The point in time cut off occurs is determined by the algebraic sum of the cosine voltage obtained from the 60^{o} filter consisting of 29R, 24C, and 20R, the bias voltage, and the input voltage (V_{39-41}). As both the cosine voltage and bias are a fixed amplitude, phase control is essentially a function of the input voltage.

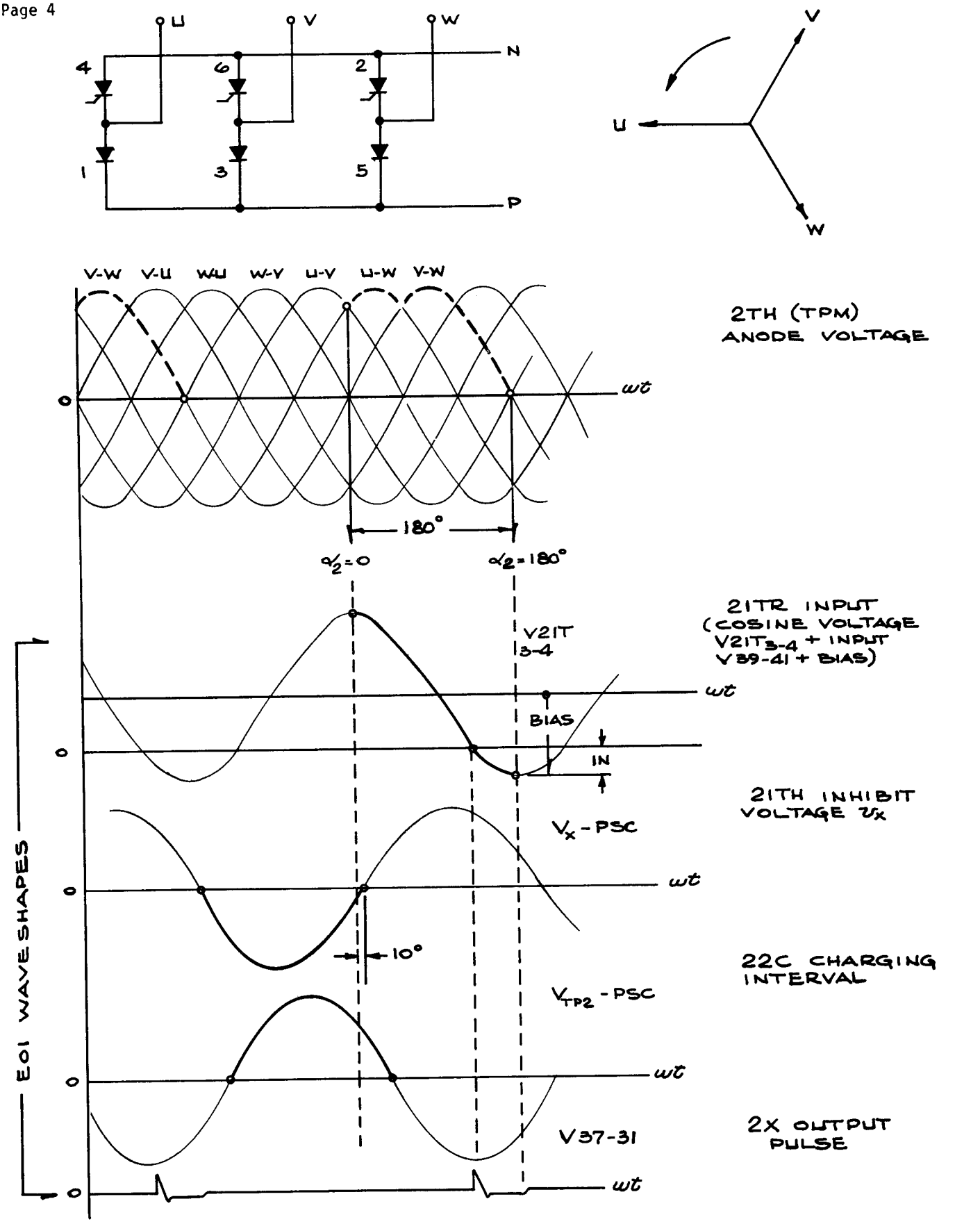
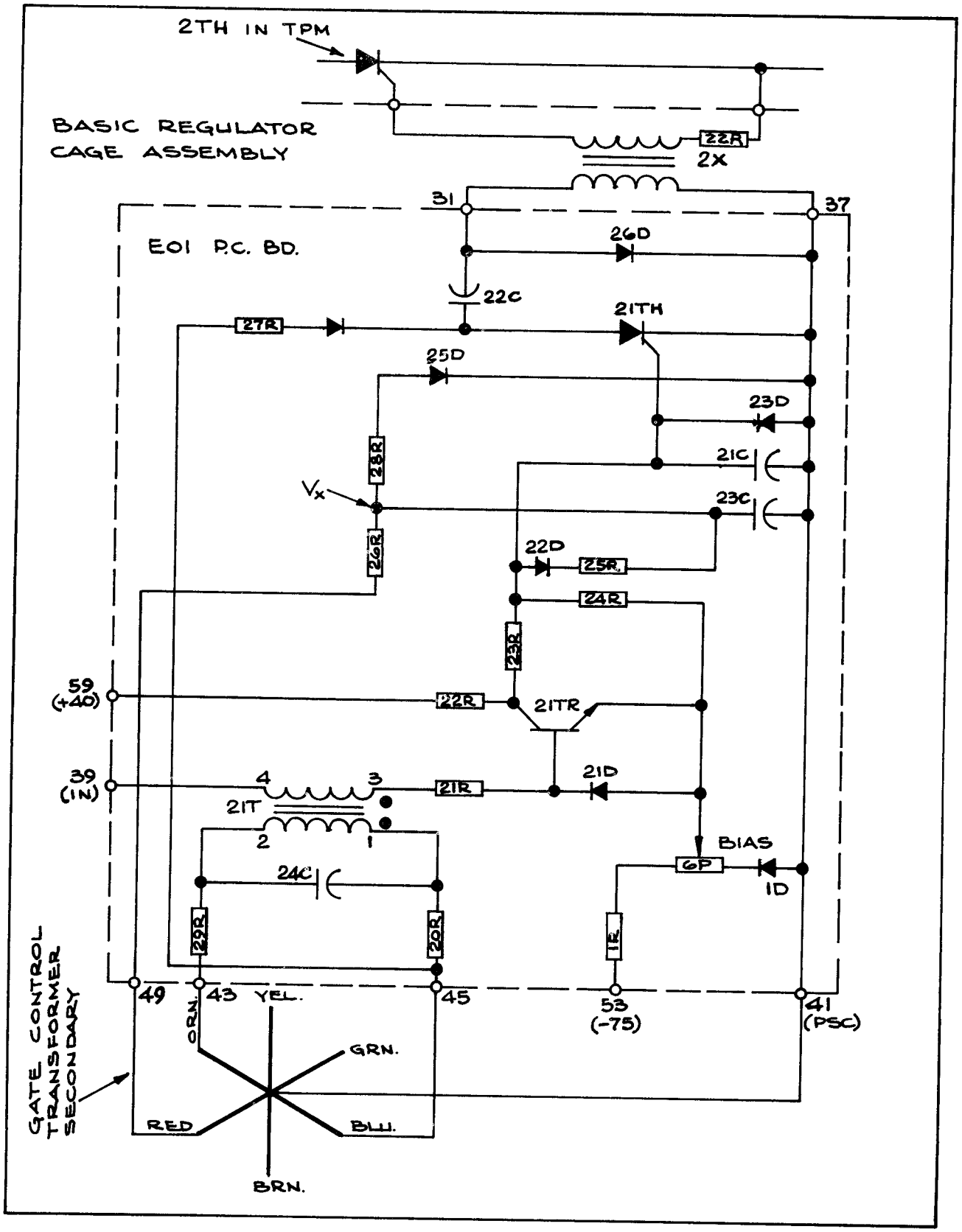

U
V
W
N
P
4
6
2
1
3
5
V-W V-U W-U W-V U-V U-W V-W
wt
0
180°
α2=0
α2=180°
2TH (TPM)
ANODE VOLTAGE
V21T
3-4
21TR INPUT
(COSINE VOLTAGE
V21T3-4 + INPUT
V39-41 + BIAS)
BIAS
IN
21TH INHIBIT
VOLTAGE Vx
Vx - PSC
10°
22C CHARGING
INTERVAL
VTP2 - PSC
V37-31
2X OUTPUT
PULSE
E01 WAVESHAPES

FIGURE 3



SIMPLIFIED SCHEMATIC FOR GENERATION OF GATE PULSE #2
FIGURE 4

Diode 21D limits the reverse voltage across the base emitter junction of 21TR and diode 23D provides the same limit function for the gate cathode junction of 21TH. Capacitor 21C provides noise filtering at the gate cathode junction of 21TH while 16D limits noise feeding back from the power converter to prevent misgating.

C. Bias

With zero volts in (terminal 39 to terminal 41), gate pulses are phased off by adjusting bias voltage to approximately the peak value of the cosine voltage. The typical transfer curve of Figure 5 can then be generated by allowing the input to vary from zero to -12 volts.

Effects of line voltage variations on α are minimized in that both the cosine and bias voltage are allowed to change proportionally. Similarly, temperature effects are minimized by compensating base emitter drops of the transistors with 1D.

D. Characteristics and Ratings

1. Input Power

Printed circuit card 1326A01G01 is used for line frequencies of 60 Hz ±2 Hz and card 1326A01G02 is used for 50 Hz ±2 Hz. Adjustment is made for various line voltages and various power transformer configurations by selecting the proper gate control transformer on the basic regulator cage assembly.

2. Output Tracking

Three pulses per cycle accurately spaced 120^{o} $\pm 2^{o}$ apart at $\alpha = 90^{o}$

3. Output Pulse Characteristics

The following pulse characteristics may be checked at the secondary of the output pulse transformer after connecting a dummy load of 4.7Ω.

(a) Peak amplitude 12 volts minimum.

(b) Pulse width (at 5 volts amplitude) 200 μs minimum.

(c) Rise time between 10% and 70% of peak voltage, 1 μs maximum

(d) Output Power: The gate pulse generator is capable of driving two, size 9 thyristors (drawing 478A223) simultaneously.

4. Input

a. Intended to be controlled by the voltage controller (E03), the current controller (E02) or an operational amplifier having a low output impedance.

b. A typical transfer curve is shown in Figure 5.

5. Ambient Temperature

0^{o} to 55^{o}C ambient temperature measured at the gate pulse generator board.

III. SERVICE

Personnel familiar with electrical equipment utilizing semiconductors can isolate most problems using an oscilloscope, multimeter, and information contained in relative instruction leaflets.

Semiautomatic equipment is available at the factory to test static and dynamic performance of all edge-connected, printed circuit cards. Generally, repair of modules is facilitated by returning them to Westinghouse Electric Corporation, Industrial Systems Division, P.O. Box 225, Buffalo, New York 14240.

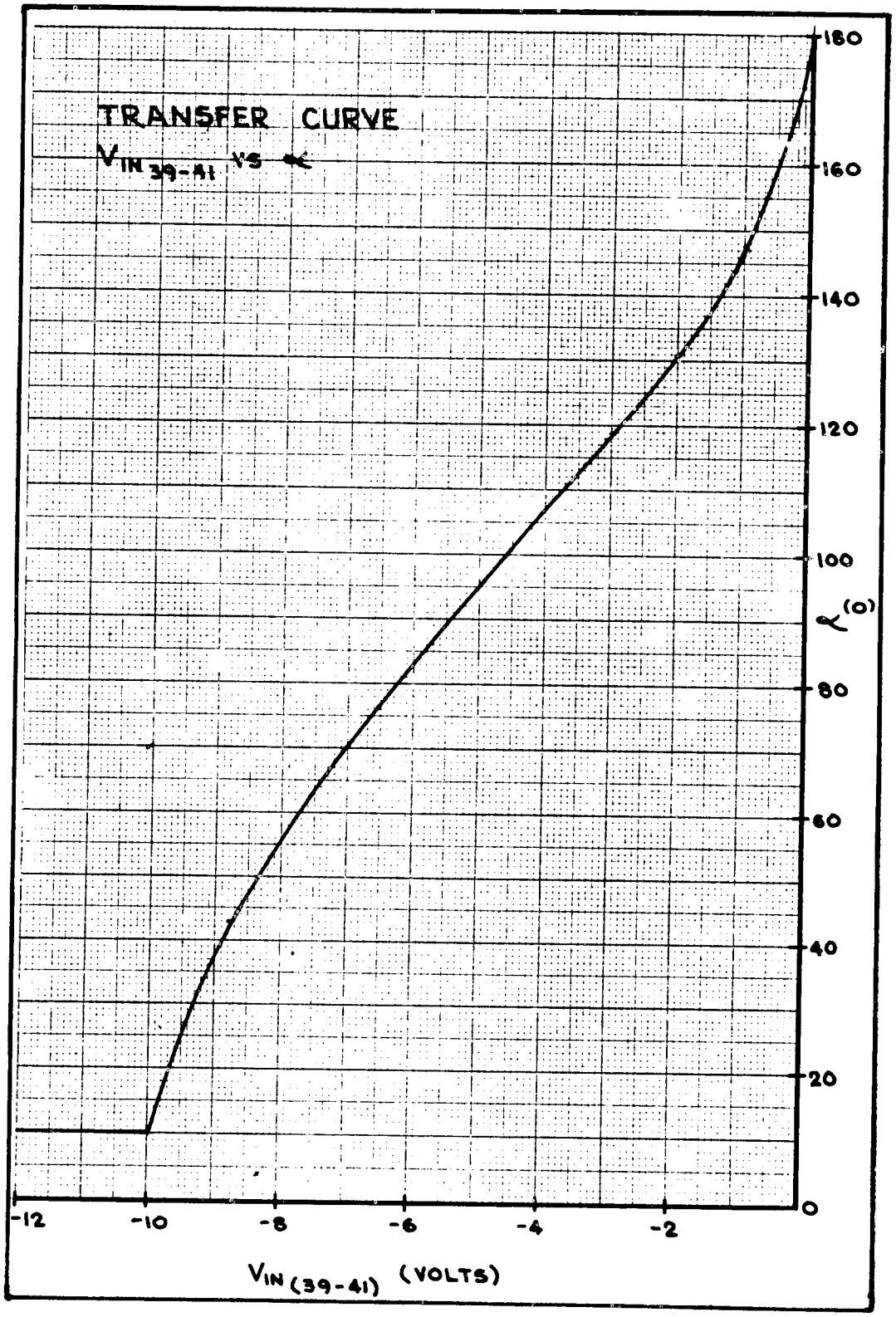

TRANSFER CURVE
$V_{IN\ 39-41}$ VS ∠
180
160
140
120
100
∠(O)
80
60
40
20
0
-12
-10
-8
-6
-4
-2
$V_{IN\ (39-41)}$ (VOLTS)

FIGURE 5