22-1000 REGENERATIVE DRIVE

(C201)
1/4 - 5 HP

INDEX

I. INTRODUCTION

22-1000, single phase, regenerative drives provide a line of adjustable voltage drives for armature excitation of DC machines from 1/4 HP up to and including 5 HP. This drive consists of a suitable DC motor, a motor controller and an operators station (either internal door mounted or external). Motors of 1/4 to 3/4 HP are usually operated at 90 VDC armature/100 VDC field, while 1 to 5 HP motors are operated at 180 VDC armature/200 VDC field. The motor controllers require 50/60 hz single phase AC power; 115 VAC for 90 VDC armature drives and 230 VAC for 180 VDC drives. The tolerance on the AC Line Voltage is +10% -5%.

The drive is a regenerative, full-wave drive. Thus it is capable of four quadrant operation in the speed-torque characteristic providing current and voltage of both polarities. This is made possible by connecting two integrated thyristor power modules (ITPM) back to back in a push-pull arrangement. Each ITPM is capable of two quadrant operation.

The motor controller contains a regulator to perform the functions of voltage control with current limit, or speed control with current limit. Since the back to back ITPM's are identical, the drive has the same current capability in forward and reverse directions. The regulator can be programmed to have different instead of equal forward and reverse current limit settings.

The motor controller features are tabulated below:

1. NEMA 1 (drip-proof) wall mounted cabinet for the entire range. The 3 and 5 HP units are force cooled. Totally enclosed wall mounted cabinets are available from 1/4 HP up to and including 2 HP.

2. The drive is available with either an internal operators station mounted on the door or an external operators station remotely mounted or both (only one operator station may have a speed potentiometer).

3. Plug-in printed circuit (PC) cards using integrated circuits. These cards mount on a single master board.

4. Minimum number of adjustments (all potentiometer adjustments are external to the PC cards and located on the master board).

5. Static sequencing using integrated circuits.

6. Static reversing.

7. Counter EMF voltage control with IR compensation for ±2% load regulation or speed feedback control for ±1% load regulation.

8. Internal independently adjustable current limits (adjustable in both forward and reverse directions from 5 to 150% of rated current).

9. External current limit reference provisions.

10. Integrated power converter modules.

11. Undervoltage protection.

12. Thermal overload protection.

13. AC circuit breaker for positive line disconnect.

14. Line contactor for positive motor disconnect.

15. Optional features:

    a. Follow circuit
    b. Timed accel-decel (adjustments 2-120 seconds)
    c. External operators station
    d. Emergency stop button
    e. Dynamic braking provision (DB resistor is externally mounted)
    f. AC brake control provisions

II. THYRISTOR POWER CONVERTER DESCRIPTION OF OPERATION

A. Phase-Controller Converter Principles

A thyristor power converter is an apparatus which by means of phase-controlled gating of thyristors converts an AC supply line voltage into an adjustable DC voltage. This process is known as rectifing. Inversely, DC voltage can be converted back into the AC line voltage, and this mode of operation is called inverting. The 22-1000 is capable of performing both of these functions.

Figure 1A shows the schematic for one of the IPTM's.

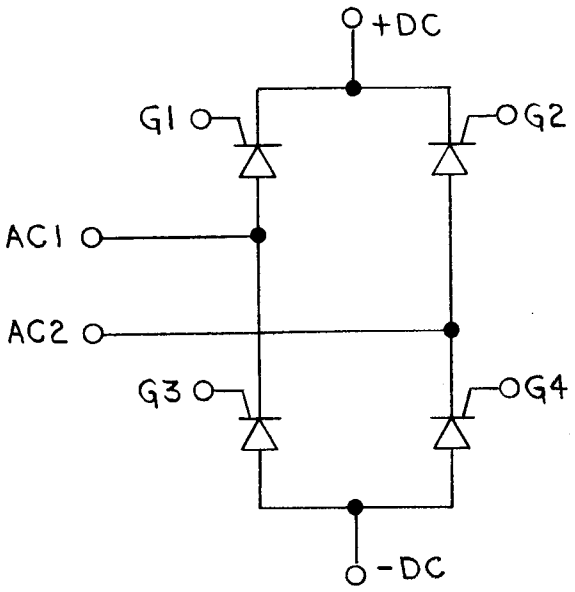

FIGURE 1A

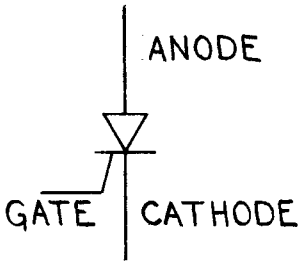

FIGURE 1B

Each ITPM contains four thyristors as well as a voltage suppression unit to clip small line spikes. In order to develop the basic current paths and wave forms the operation of a thyristor will be outlined.

A thyristor is a three-terminal silicon device (Figure 1B). It is capable of blocking both forward and reverse voltages; and when forward biased (anode positive with respect to the cathode), will switch to the conducting state if the gate is supplied a positive signal with respect to the cathode. Once turned on the cell continues to conduct until the voltage across it reverses or the current through it falls below a minimum value---termed the holding current.

With the preceding basic information the significant current paths and waveforms for the power portion of the drive can now be developed. A simplified version of the TPM containing only one ITPM (Figure 2) will be used to develop the time-related waveshapes for two loading conditions. Case I will be for continuous current with a gating angle of $\alpha = 60^0$. Case II will be for discontinuous current, with a gating angle of $\alpha = 90$. Note that α is measured from the point where the anode-cathode voltage of the respective cell swings positive with no CEMF voltage present. A zero degree gating angle occurs when the AC line voltage crosses zero going positive and a 180^0 gating angle occurs when the AC line voltage crosses zero going negative.

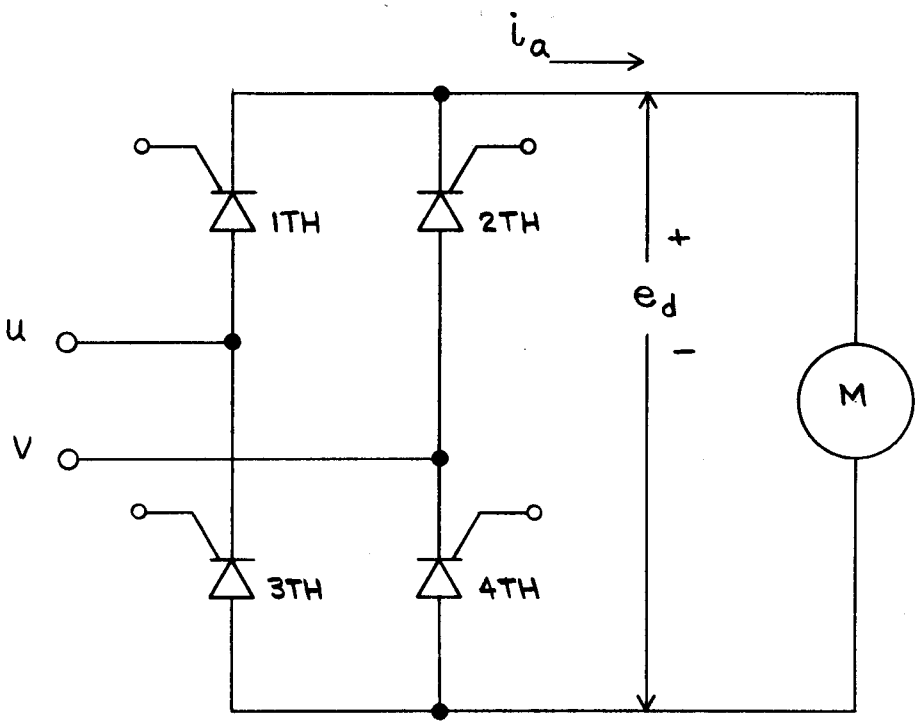

FIGURE 2

Case I Continuous Current Operation

Figure 3 shows the steady state waveshapes for a highly inductive load. The uppermost traces show the output voltages of the ITPM (e_d) related to the incoming line voltage e_{u-v} and e_{v-u}). The second and third traces show the gate pulses, and the steady state current trace (i_a) is shown on the bottom. Initially, all thyristors are assumed to be in the blocking state. At $\alpha = 60^0$ the line voltage e_{u-v} is positive and thyristors 1TH and 4TH are forward biased; and upon receiving a gate pulse at $\alpha = 60^0$ turn on. This establishes a current path from terminal U to terminal V through 1TH, the load, and 4TH. Thyristors 1TH and 4TH continue to conduct for 180^0 even though the line voltage reverses (forward bias is being maintained by the inductive load). At the instant of line voltage reversal thyristors 2TH and 3TH become forward biased but remain in the forward blocking state until receiving a gate pulse at $\alpha = 60^0$ which enables them to turn on.

Once turned on, the load current commutates to thyristors 2TH and 3TH; a reverse voltage is applied to the previously conducting cells forcing them to turn off. Thyristors 2TH and 3TH conduct for 180^0 or until gate pulses are again supplied to thyristors 1TH and 4TH and the cycle is repeated. Assuming a highly inductive load, the dc current will reach a steady state value after a number of cycles. For a gating angle of $\alpha = 0$ the thyristors do not have to absorb any positive voltage and are then comparable to single diodes. While in continuous current operation, it is apparent from the output voltage waveshapes (e_d) that its average value E_d is a function of the gating angle. E_d reaches a positive maximum at $\alpha = 0$, is zero for $\alpha = 90^0$ and assumes negative values back to $\alpha = 180^0$. This transfer curve can be obtained by integrating the waveforms. The result is:

$$E_d = E_{do} \cos \alpha$$

where the saturated output voltage is

$$E_{do} = \frac{2\sqrt{2}}{\pi} \times E_{u-v}$$ where E_{u-v} is the line to line rms ac voltage.

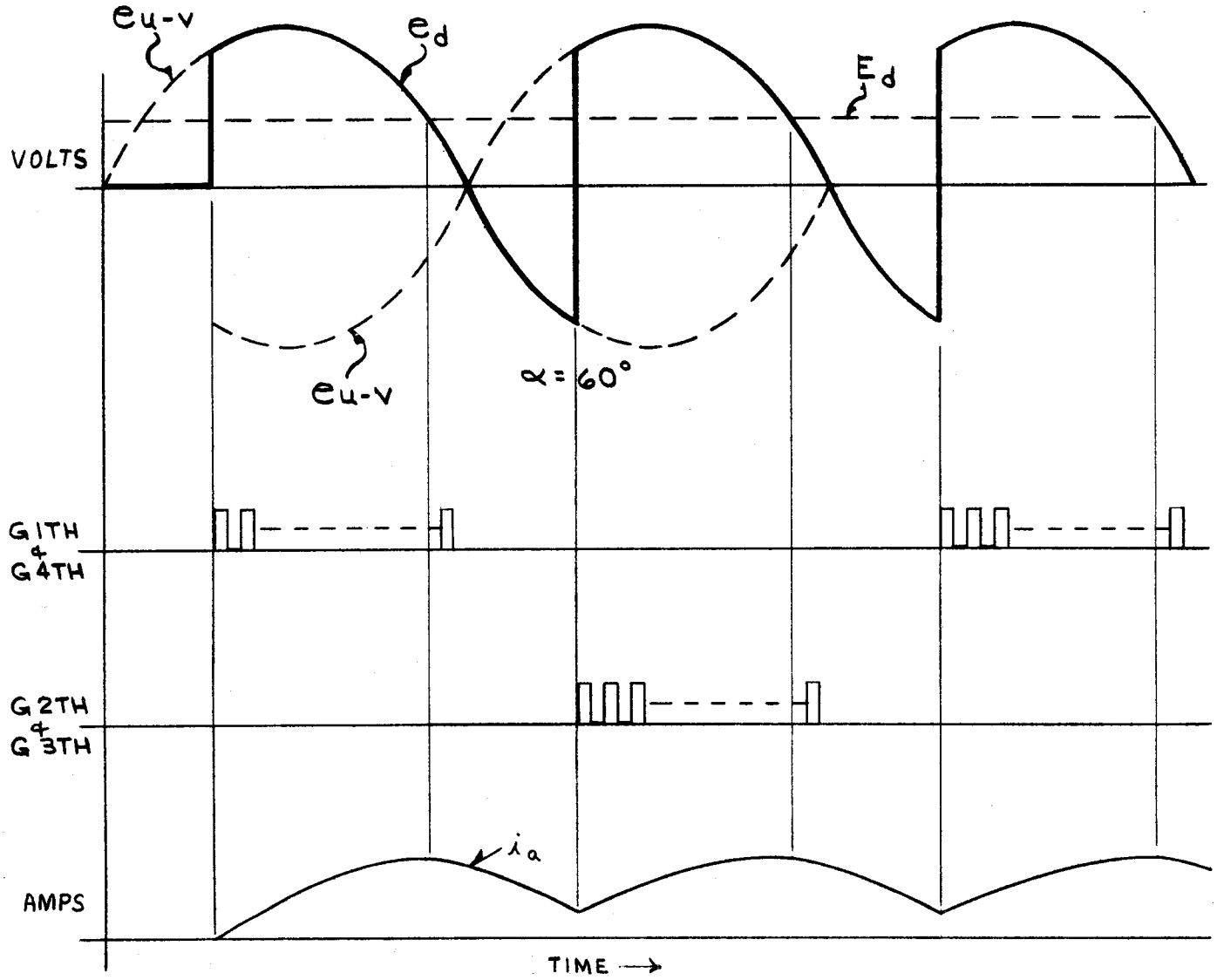

FIGURE 3 WAVESHAPES FOR A HIGHLY INDUCTIVE LOAD

Case II Discontinuous Current Operation

The description in the previous section has been made with the assumption that the dc load current is continuous. In a practical circuit with a dc motor armature, the actual operation always covers the range of discontinuous current and may or may not include the continuous load current range. The operating range depends primarily upon the motor armature inductance and the motor loading.

With the aid of Figures 2 and 4 the initial conduction period for discontinuous current operation will be explained. Initially all thyristors are assumed to be in the blocking state and the motor CEMF voltage is zero. When the line voltage e_{u-v} is positive, thyristors 1TH and 4TH are forward biased; and upon receiving a gate pulse at $\alpha = 90^0$ turn on. This establishes a current path from terminal U to terminal V through 1TH, the load and 4TH.

The current pulse builds up to peak amplitude until e_d goes negative with respect to E_d (the motor CEMF). Then it decays to zero in a positive sinusoidal waveshape. When i_L reaches zero, the thyristors turn off, and e_{dn} then equals CEMF. Because of the motor CEMF voltage and the IR voltage drop in the motor armature the current pulse is not a true sinusoidal waveshape but shifted as indicated in Figure 4.

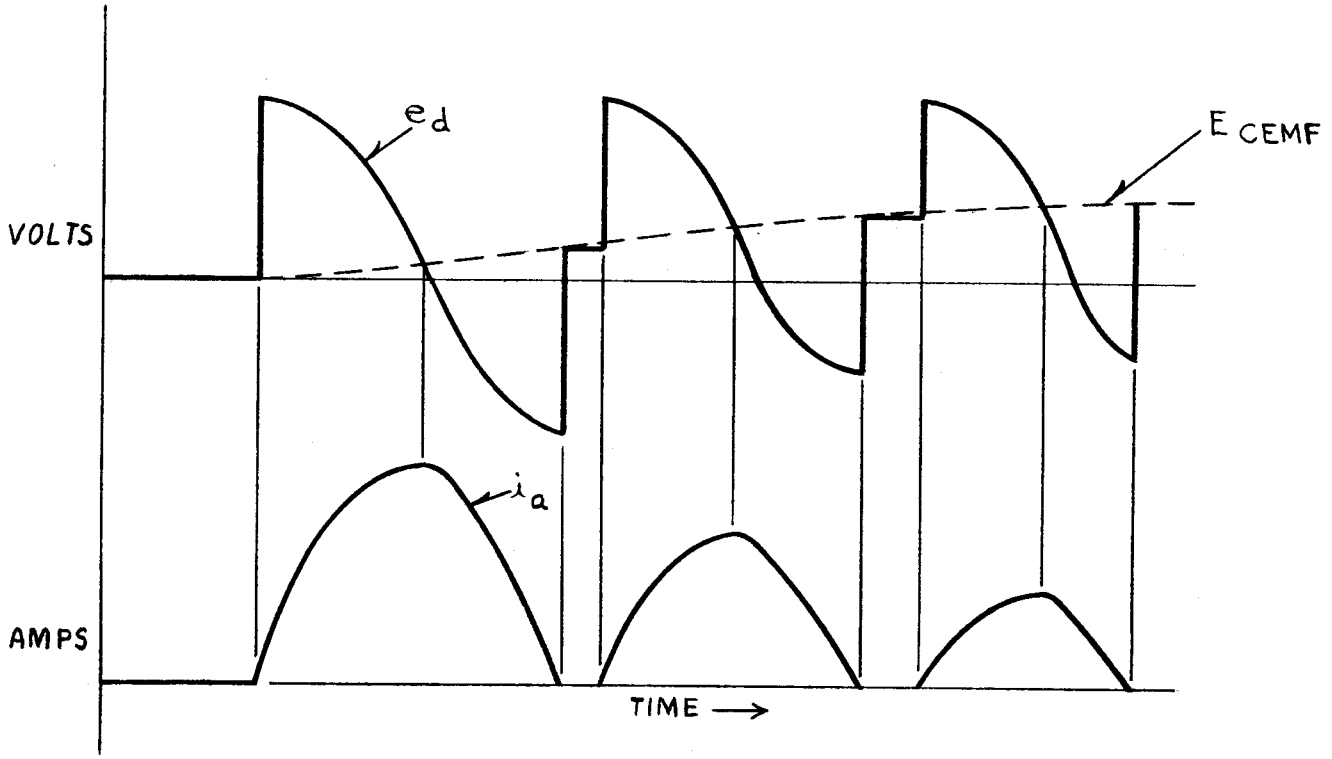

FIGURE 4 INITIAL CONDUCTION PERIOD FOR DISCONTINUOUS CURRENT OPERATION

The armature current causes the motor to rotate which establishes a CEMF voltage. The CEMF voltage is proportional to the motor speed and at rated speed equals the rated motor armature voltage minus IR drops.

Figure 5 shows the waveshapes for discontinuous current operation with a gating angle of 90^0 after the motor has reached a constant speed. The uppermost trace shows the output voltage of the ITPM (e_d) related to the incoming line voltage (e_{u-v} and e_{v-u}) and the CEMF voltage. The second and third traces show the gate pulses and the discontinuous current waveshapes, (i_a) is the bottom trace. The conduction period is established by the volt second areas, such that the volt second area where the applied voltage exceeds the CEMF voltage approximately equals the volt-second area where the applied voltage is less than the CEMF voltage neglecting IR voltage drops. With this basic information the operation during one cycle will be explained. At $\alpha = 90^0$ the magnitude of the AC Voltage is greater than the CEMF voltage. Therefore, thyristors 1TH and 4TH are forward biased. Upon receiving the gate pulse at $\alpha = 90^0$ the conduction period begins. Thyristors 1TH and 4TH turn on and apply the line voltage to the motor armature. Thus the current pulse builds up as previously explained. When the current pulse decays to zero (or below the thyristor holding current) thyristors 1TH and 4TH turn off completing the conduction period. Instantaneously, the motor armature voltage jumps to the CEMF Voltage value. This occurs because all of the thyristors in the ITPM are in the off state and the motor is essentially connected to an open circuit with the motor CEMF Voltage present. It is evident from Figure 5 that thyristors 2TH and 3TH are back biased for a short period of time upon completion of the previously described conduction period because the magnitude of the CEMF voltage exceeds the magnitude of the AC line voltage e_{v-u}. After a short period of time, the line voltage e_{v-u} exceeds the CEMF Voltage causing thyristors 2TH and 3TH to become forward biased. They remain in the forward blocking state until receiving gate pulses at $\alpha = 90^0$. Once turned on thyristors 2TH and 3TH conduct until the forward current extinguishes and the cycle is repeated.

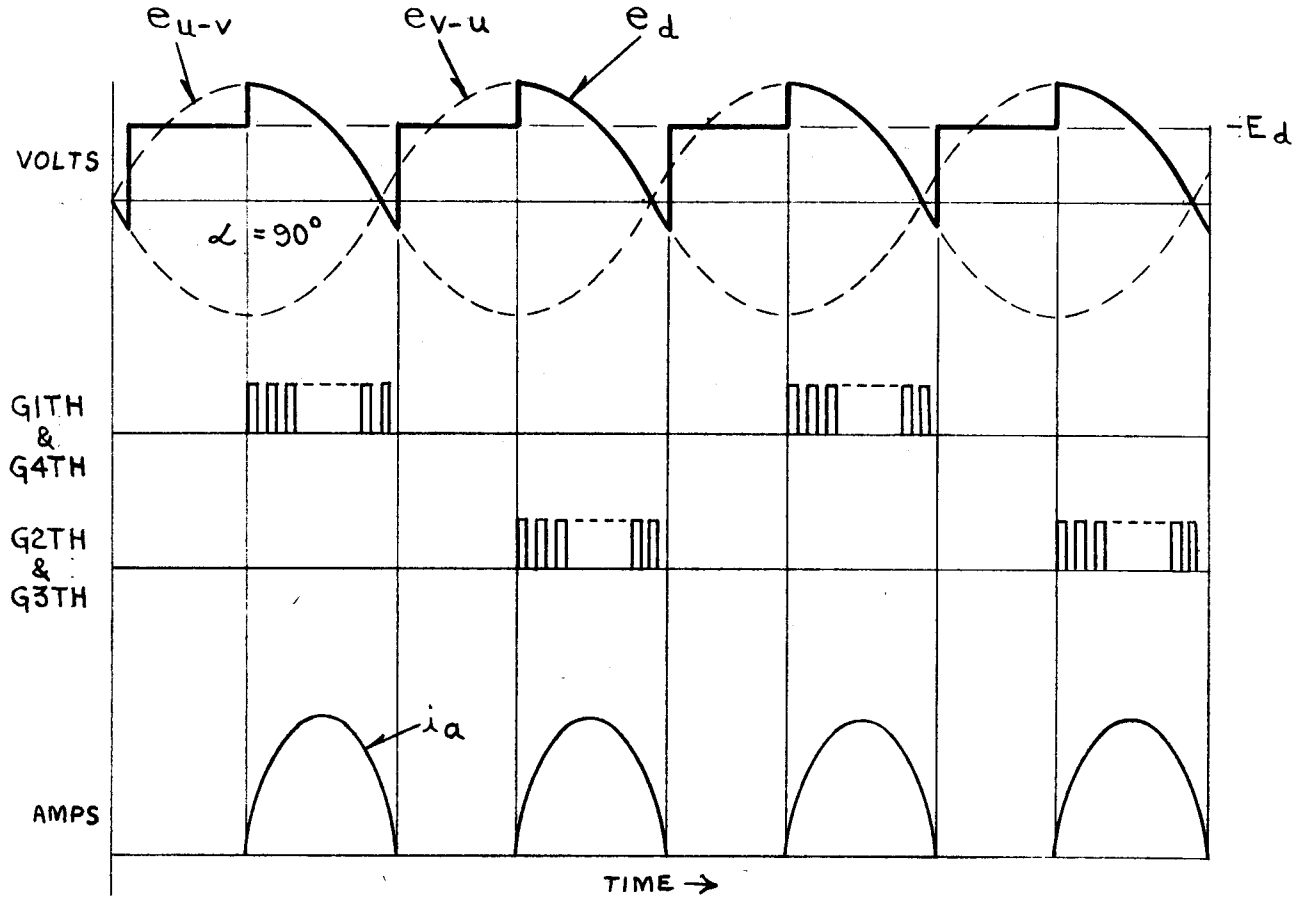

FIGURE 5 WAVESHAPES FOR DISCONTINUOUS CURRENT OPERATION

The simplified power circuit described so far can provide voltage of both polarities when operating in continuous current. The current, however, can only flow in the direction of the rectifying cells.

For a 22-1000, single phase, regenerative drive, a second ITPM is added and connected back-to-back with the appropriate suppression networks as shown in Figure 6. Thus, the 22-1000 is capable of four quadrant operation.

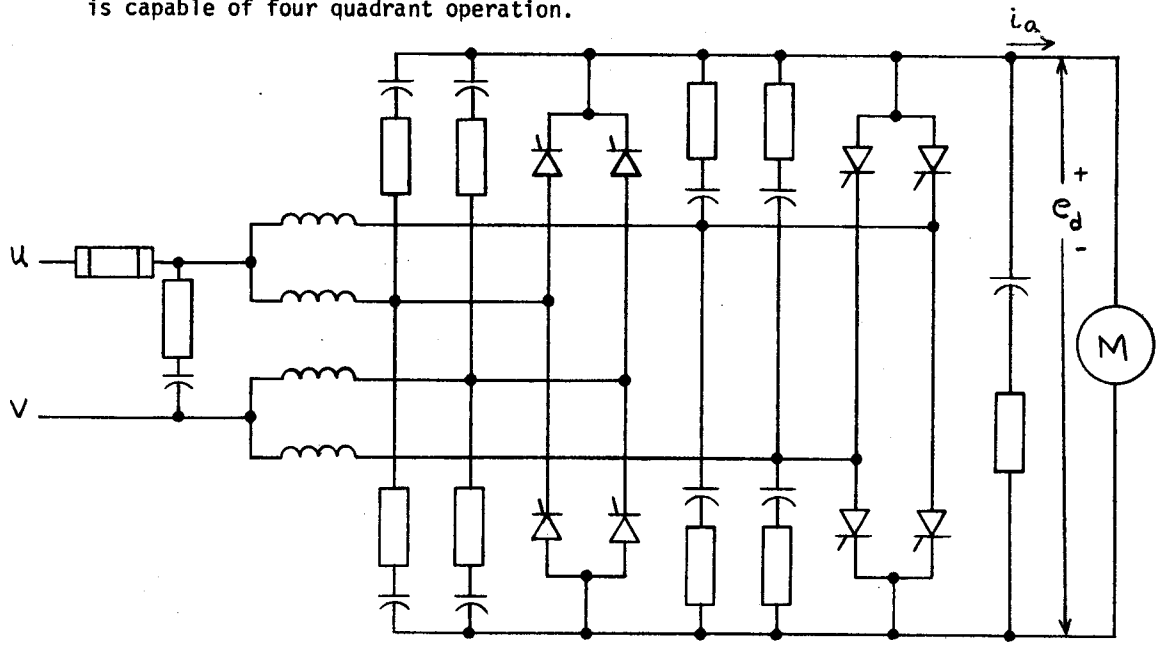

FIGURE 6

The RC networks in conjunction with the AC line ferrite reactors attenuate excessive rates of voltage and current, which otherwise may lead to undesired turn-on or degradation of thyristors. The R-C networks across the ac line and the dc output damp oscillations that would otherwise be produced by the commutation process.

B. Systems Descriptions of Operation

There are several ways to control such a power converter. The principle used in this drive is to use two gating channels, but biased such that current cannot circulate between ITPM's causing short circuits. The operation will now be explained with the help of the system diagrams shown in Figures 7A and 7B.

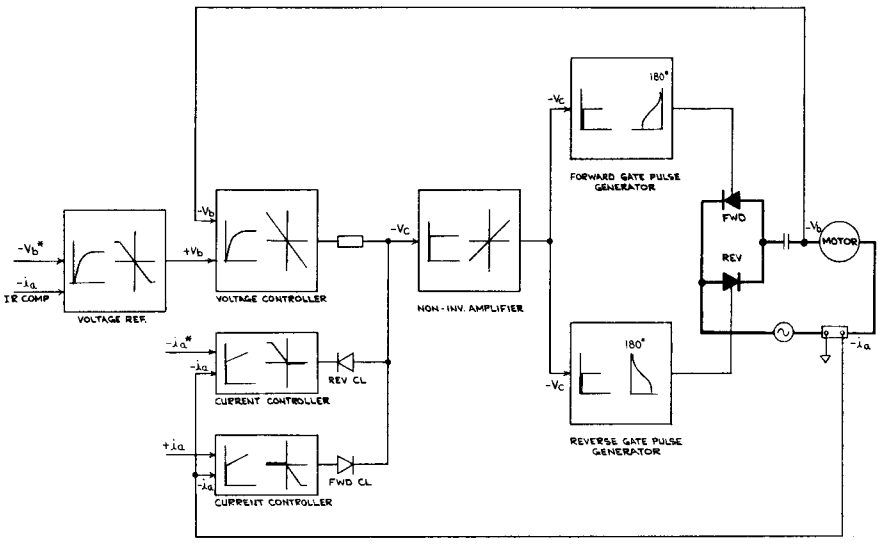

FIGURE 7A CEMF VOLTAGE REGULATED DRIVE

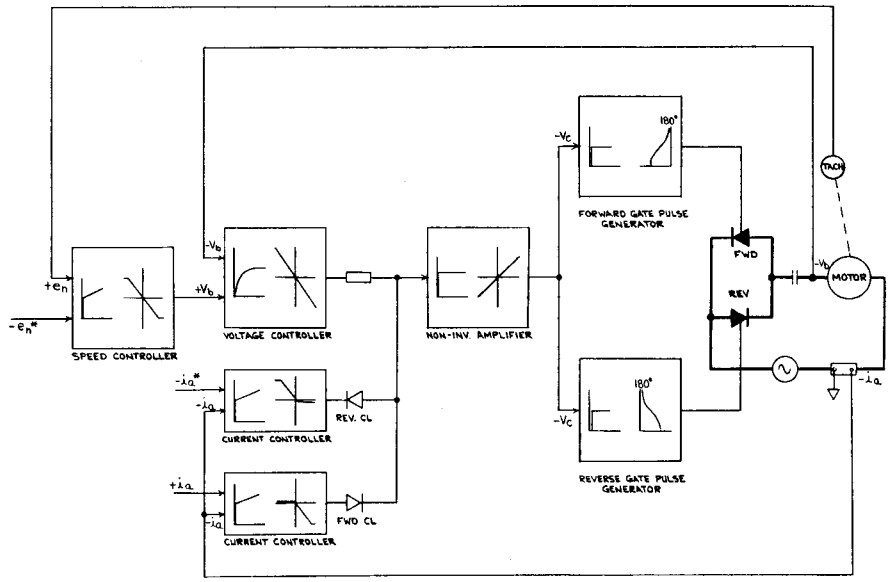

FIGURE 7B SPEED REGULATED DRIVE

The system diagrams show the main control elements of the double converters, with the power circuit in single line diagram form. Figure 7A is the system diagram of a CEMF Voltage regulated drive, while Figure 7B is the system diagram of a speed regulated drive. It is evident from these diagrams that the inner loops (voltage and current) are identical for all applications, but the input controller has different characteristics for each mode of operation. The inner loops consist of a voltage controller, a forward current controller, and a reverse current controller which work in parallel through a common non-inverting output stage. When the motor current is less than the current limit value, either positive or negative, the forward and reverse current controllers stay in their negative and positive saturation limits respectively. The switching diodes are therefore non-conducting and the voltage controller is effective. Should the armature current reach either a positive or a negative limiting value, the corresponding current controller comes out of saturation, assumes control of the output state, and regulates the armature current. Under this condition, the voltage controller is isolated by the high resistance in its output, so it has little or no influence on the converter output. Thus the outputs of the voltage controller and the current controllers are "OR"ed by the non-inverting amplifiers and fed to the Gate Pulse generator.

As previously stated, the gate pulse generator is biased such that circulating current cannot occur. Thus, the forward and reverse ITPM's can not be gated simultaneously. This is accomplished by incorporating a small dead-band into each gating channel, such that when the input to either gate pulse generator ($-V_c$) is zero, no gate pulses are released to either ITPM. When $-V_c$ becomes more negative than the dead band limits, gate pulses are generated by the forward gating channel permitting forward current flow. Vice versa, when $-V_c$ becomes more positive than the dead band limits, gate pulses are generated by the reverse gating channel permitting reverse current flow.

The 22-1000, single phase, regenerative drive requires the same controller board for either a voltage or speed application. This board contains the voltage and current controllers previously discussed as well as the input controller. This controller is connectable as either a proportional amplifier or a PI controller. For a CEMF voltage drive the summing amplifier is connected as a proportional amplifier whose inputs are a dc voltage command signal ($-V_b^*$) and IR compensation signal. For a speed controlled drive the summing amplifier is connected as a PI controller whose inputs are speed command signal ($-e_n^*$) and the tachometer feedback signal ($+e_n$). The IR compensation signal is not used for a speed controlled drive.

Figure 8 shows an oscillogram of a discontinuous current reversal with a step change into the controller reference. The upper trace is the step voltage into the controller reference. The middle trace is the output voltage (V_b) and the bottom trace shows the load current (i_a). At time t_0 the reference voltage polarity is changed, and the motor armature voltage and current begin to decrease. They reach zero at time t_1 and then reverse polarity to accelerate the motor in the opposite direction.

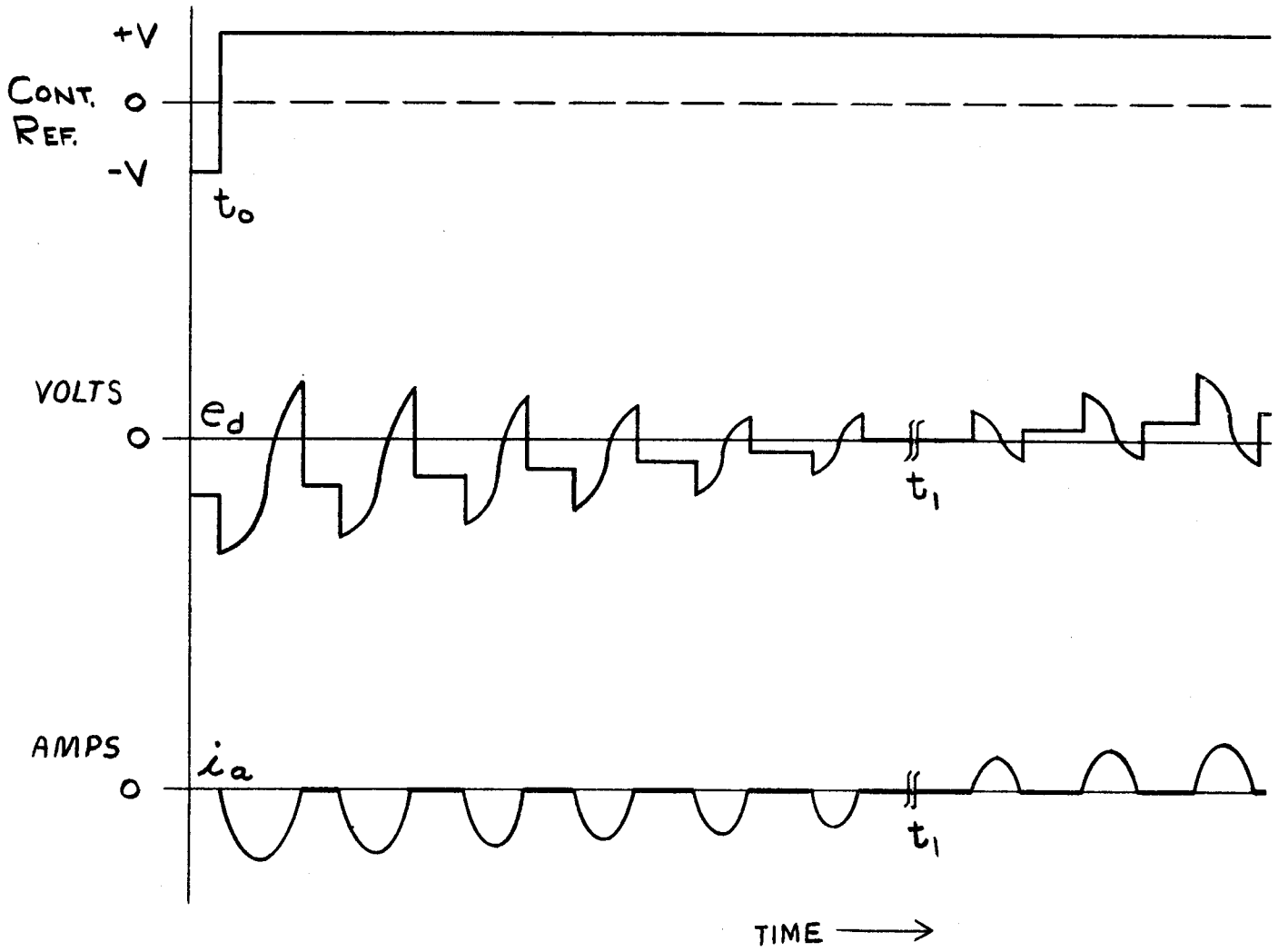

FIGURE 8 DISCONTINUOUS CURRENT REVERSAL

C. Regulator Assembly

The regulator assembly contains both preselected and optional components. This assembly is mounted on the cabinet door. The basic regulator is composed of five printed circuit boards, they are:

1. Master Board
2. Sequencer Board
3. Controller Board
4. Power Supply/± Cosine Board
5. The Gate Pulse Generator Board

Space is provided in the regulator assembly for an optional Ramp/Follow board.

Figure 9A shows total drive interconnection diagram while Figures 9B and 9C show the signal distribution diagrams of the 22-1000, single phase, regenerative drive.

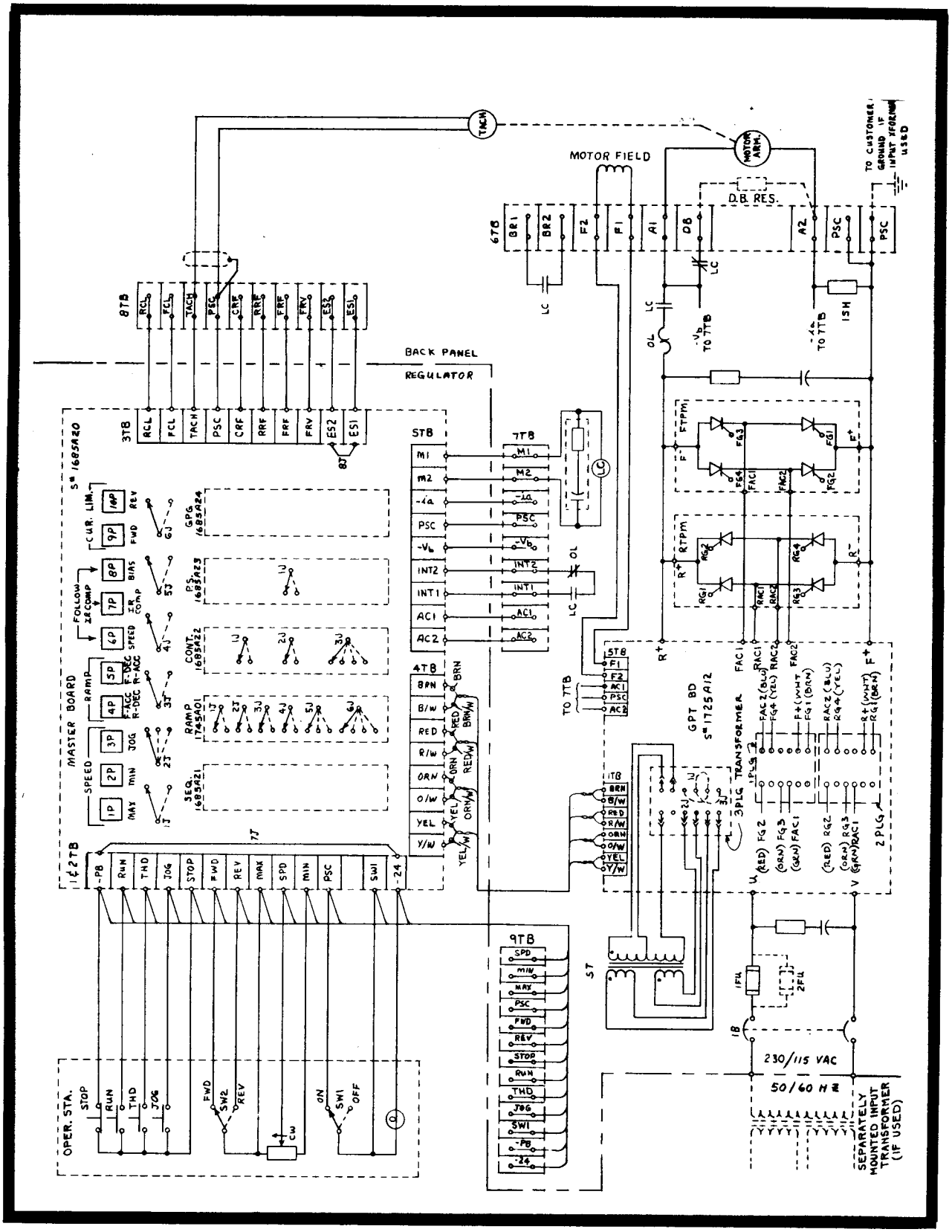

FIGURE 9A INTERCONNECTION DIAGRAM

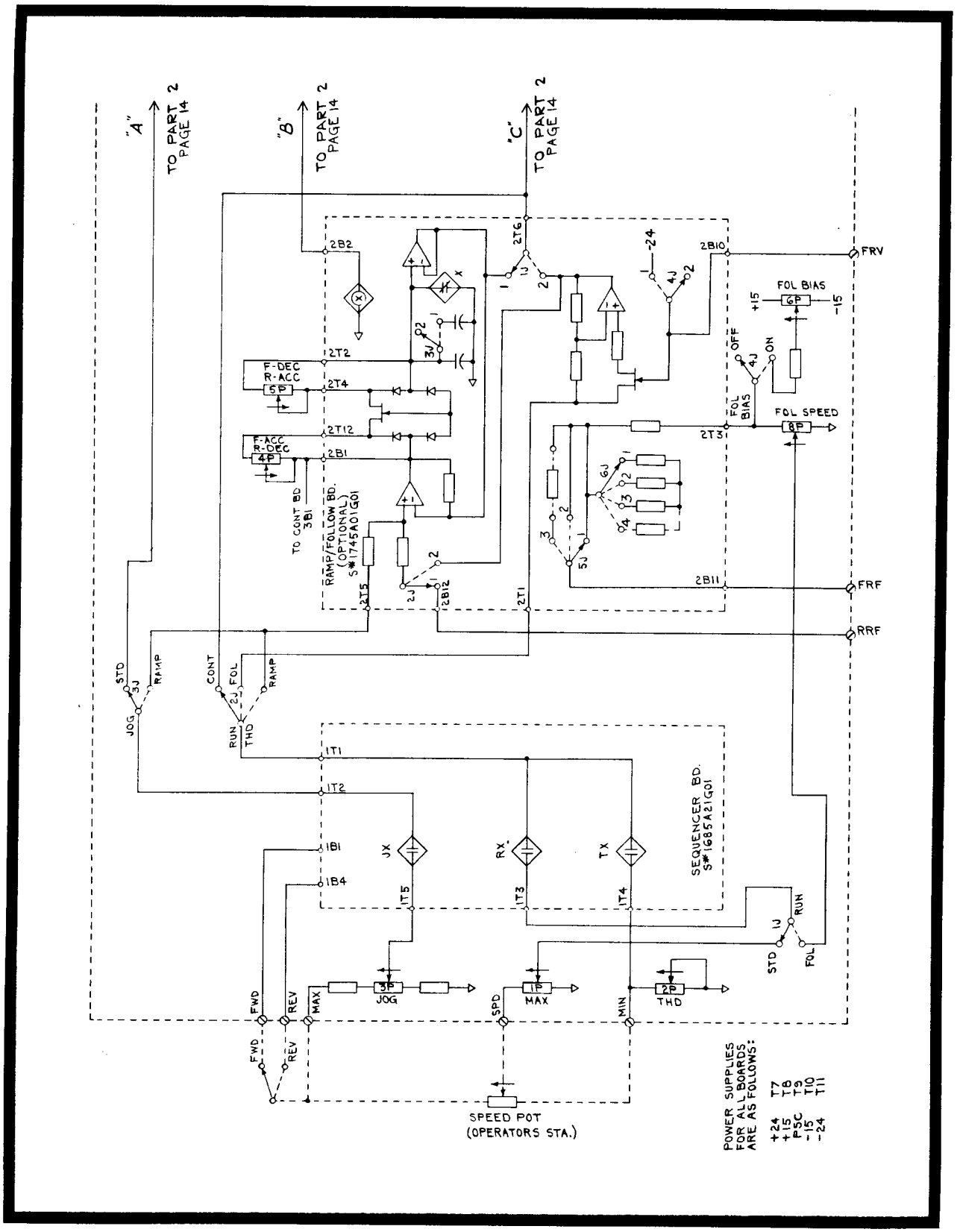

FIGURE 9B SIGNAL DISTRIBUTION DIAGRAM PART 1

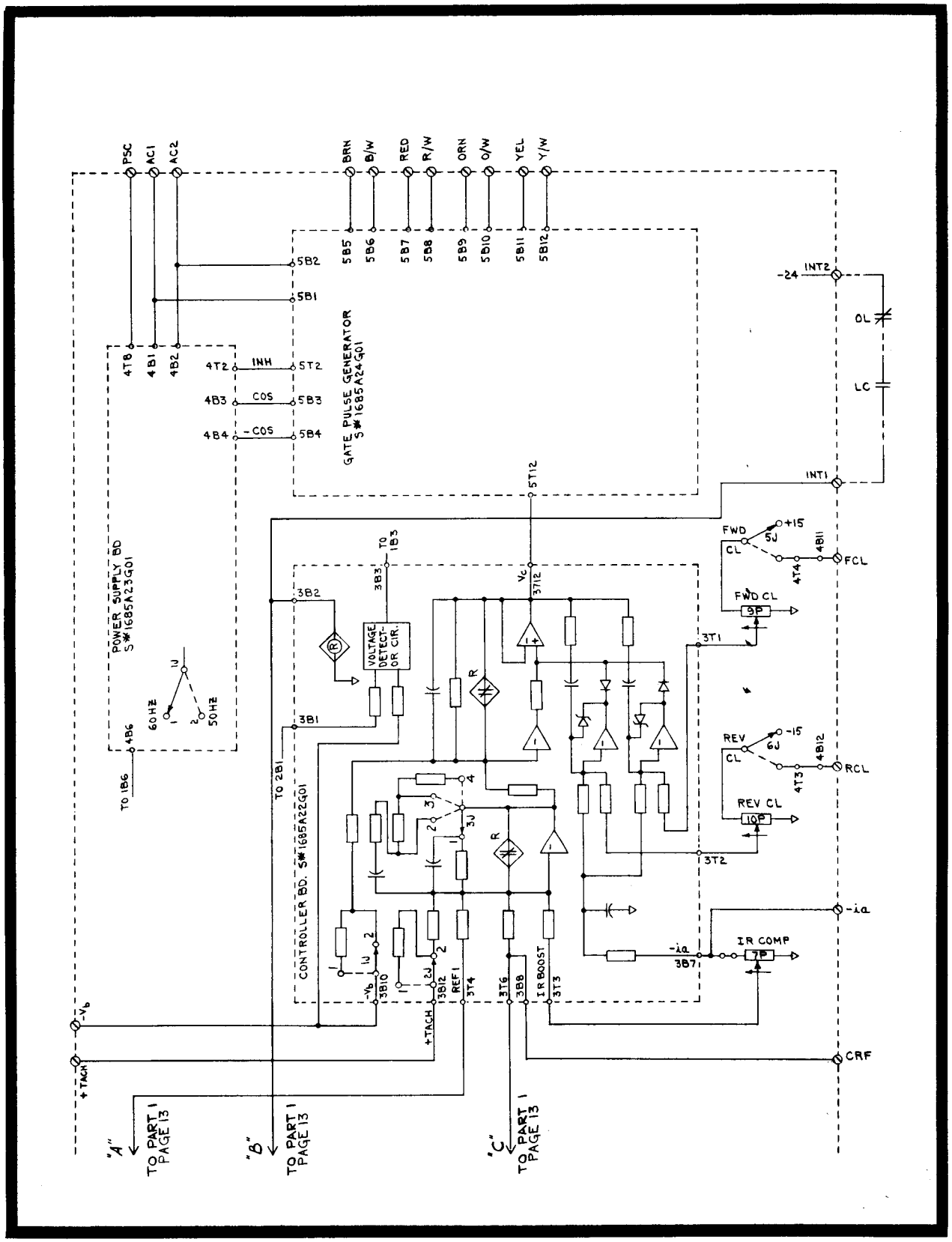

FIGURE 9C SIGNAL DISTRIBUTION DIAGRAM PART 2

1. Master Board

The Master Board serves the same basic needs as the standard card cage. It provides printed circuit board sockets with guide rails for mounting the plug-in Printed Circuit Cards and makes the required interconnections between cards. In addition to these functions, it contains all potentiometer adjustments, 6 reference jumpers, filter capacitors for the ±24VDC supplies and terminal blocks for the regulator inputs and outputs. A schematic diagram of the master board is shown in Figure 10. The interconnection diagram, Figure 9A shows connections to the master board terminal blocks.

The following tabulation verbally identifies the master board potentiometer adjustments. Refer to the simplified schematic Figures 9B and 9C to aid understanding.

a. Potentiometer 1P "MAX" adjusts the maximum run speed when a manual speed pot is used.

b. Potentiometer 2P "MIN" adjusts the minimum run speed when a manual speed pot is used. The minimum run speed is the THD (THREAD) speed.

c. Potentiometer 3P "JOG" adjusts the jog speed from approximately 5% to 20% maximum speed

d. Potentiometer 4P "F-ACC, R-DEC" adjusts the forward-acceleration and reverse-deceleration ramp rates when the timed accel-decel (RAMP) option is included.

e. Potentiometer 5P "F-DEC, R-ACC" adjusts the forward-deceleration and reverse acceleration rate when the timed accel-decel (RAMP) option is included.

f. Potentiometer 6P "FOL SPD" adjusts the maximum speed when the optional follow circuit is used.

g. Potentiometer 7P "IR COMP" adjusts the amount of IR compensation.

h. Potentiometer 8P "FOL BIAS" provides the necessary bias to a follower current signal such that the lowest value of signal current demands zero speed.

i. Potentiometer 9P "FWD CL" adjusts the forward current limit reference from 5 to 150% of rated current.

j. Potentiometer 10P "REV CL" adjusts the reverse current limit reference from 5 to 150% of rated current.

The following tabulation verbally describes the Master Board jumpers and their position. Figures 9B and 9C are simplified schematics showing the functions.

a. Jumper 1J "RUN" is for the run reference. It should be in the "STD" position for all applications except when the optional follow circuit is used. When the optional follow circuit is used, 1J should be placed in the "FOL" position.

b. Jumper 2J "RUN/THD" routes the RUN reference from the sequencer board to reference inputs on the controller board or the Ramp/Follow Board. 2J should be placed in the "STD" position when the optional Ramp/Follow Board is not used. 2J should be in position "RAMP" with the ramp option. 2J should be in the "FOL" position if the optional follow circuit is used with or without the "RAMP" option.

c. Jumper 3J "JOG" permits the Jog reference to go directly to the controller in the "STD" position. The "RAMP" position permits the jog signal to go through the ramp if the optional Ramp/Follow Board is available.

d. Jumper 4J "FOL BIAS" should be in the "OFF" position when a follow bias is not required and in the "ON" position when bias is required for the signal follow option.

e. Jumper 5J "FWD CL" should be in the "INT" position if an external current limit signal is not provided by the customer. If the signal is provided by the customer, it should be in the "EXT" position. 10VDC reference applied to terminal FCL will yield approximately 100% current limit.

f. Jumper 6J "REV CL" --- same as e except a 10VDC reference applied to terminal RCL will yield approximately 100% current limit.

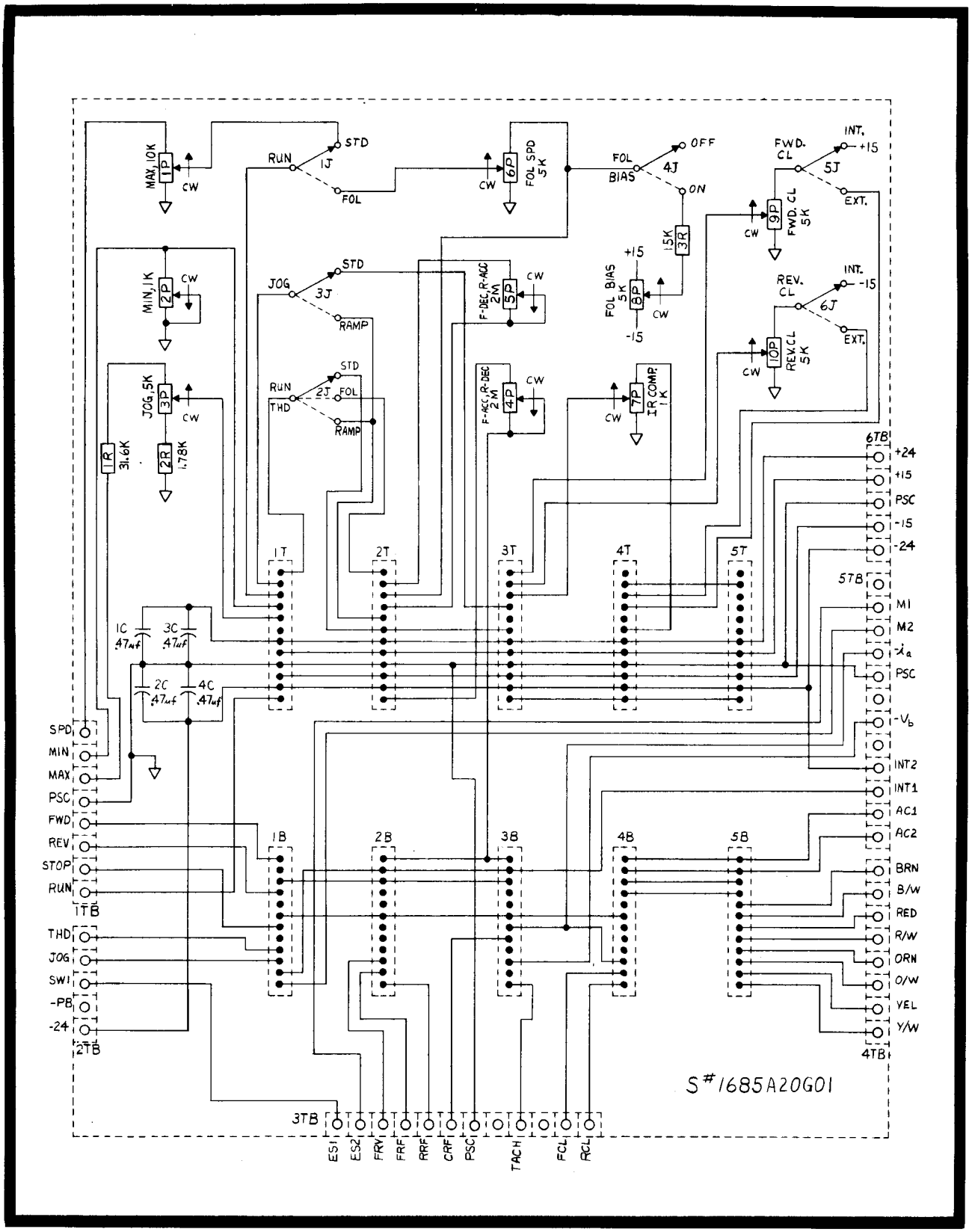

FIGURE 10 MASTER BOARD

2. Static-Sequencer (SEQ.)

Figure 11 is a schematic diagram of this board and Figure 12 is a relay equivalent of the static sequencer.

The board employs high level logic NAND gates in combination with necessary semiconductors and passive components required for static sequencing. It receives signals from the operators station and permits the drive to perform the required function if the system feedback signals are correct. The sequencer controls the contactor located on the back panel and supplies internal references for the controller board and the optional ramp/follow board.

NOTE: THE DIGITAL INTEGRATED CIRCUITS OPERATE FROM PSC TO THE -15VDC REGULATED SUPPLY. Therefore a logic one is zero volts and logic zero is -15VDC with respect to PSC.

The sequencer is capable of supplying the options of jog and thread, as well as the standard run-stop functions. Pin B3 monitors the output of the Voltage Sensor located on the Protection board. This in combination with associated components, prevents picking up or dropping out the contactor if there is a large voltage across the motor armature or the ramp function generator is ramping. The static time delay circuit has a fixed drop out time constant of approximately one-half second after the voltage at pin B3 is more positive than -7.5VDC (pin B3 is more negative than -7.5VDC (-7.5VDC to -15VDC) when the motor CEMF is larger than 20% of rated CEMF voltage). Pin B6 monitors the undervoltage circuit located on the power supply board. During normal operation B6 is held at zero VDC, but if the customer's AC supply drops below 80% of its nominal value, an undervoltage trip occurs and pin B6 is pulled to -15VDC. This initiates a stop and drops out the contactor without a time delay.

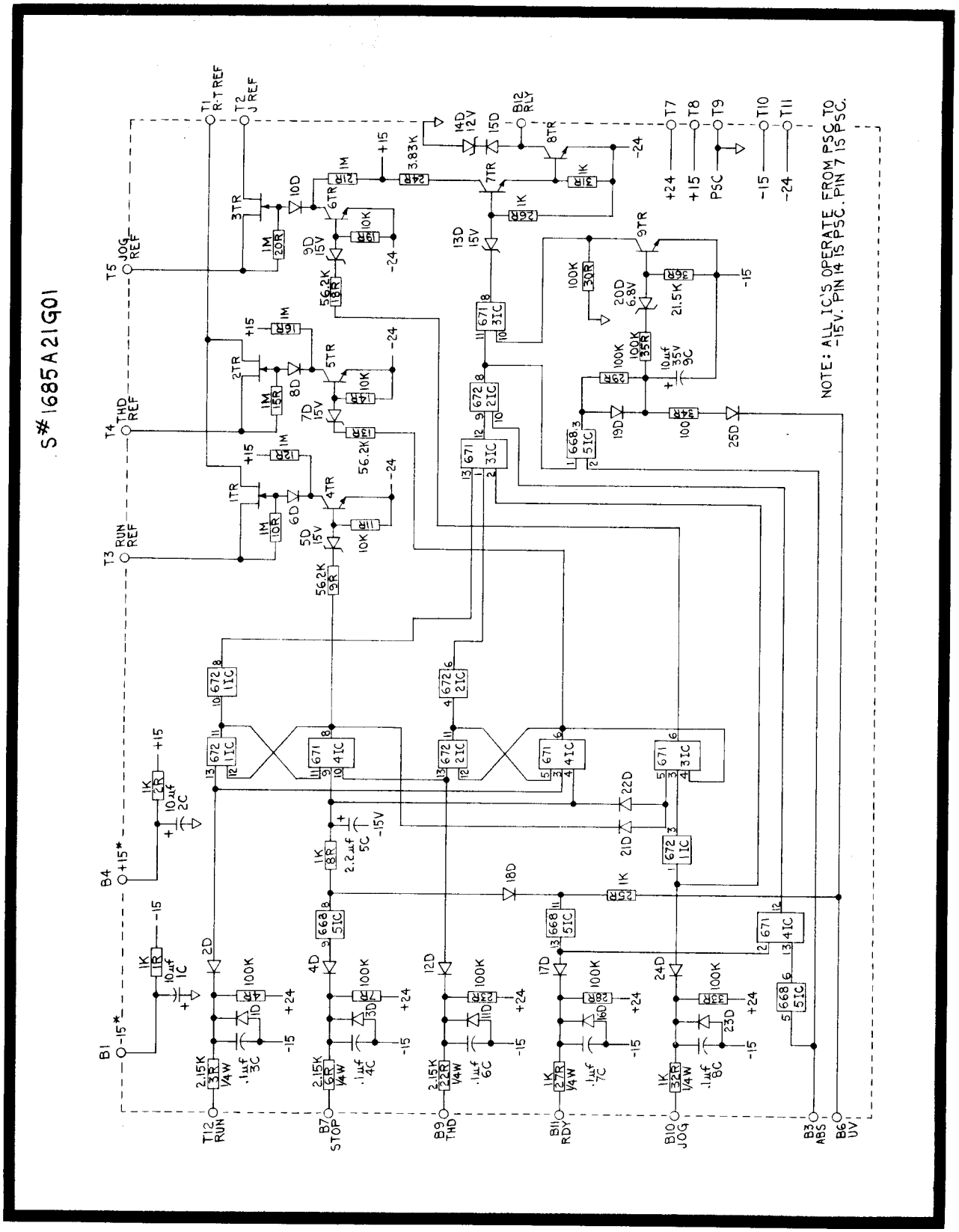

FIGURE 11 STATIC SEQUENCER BOARD

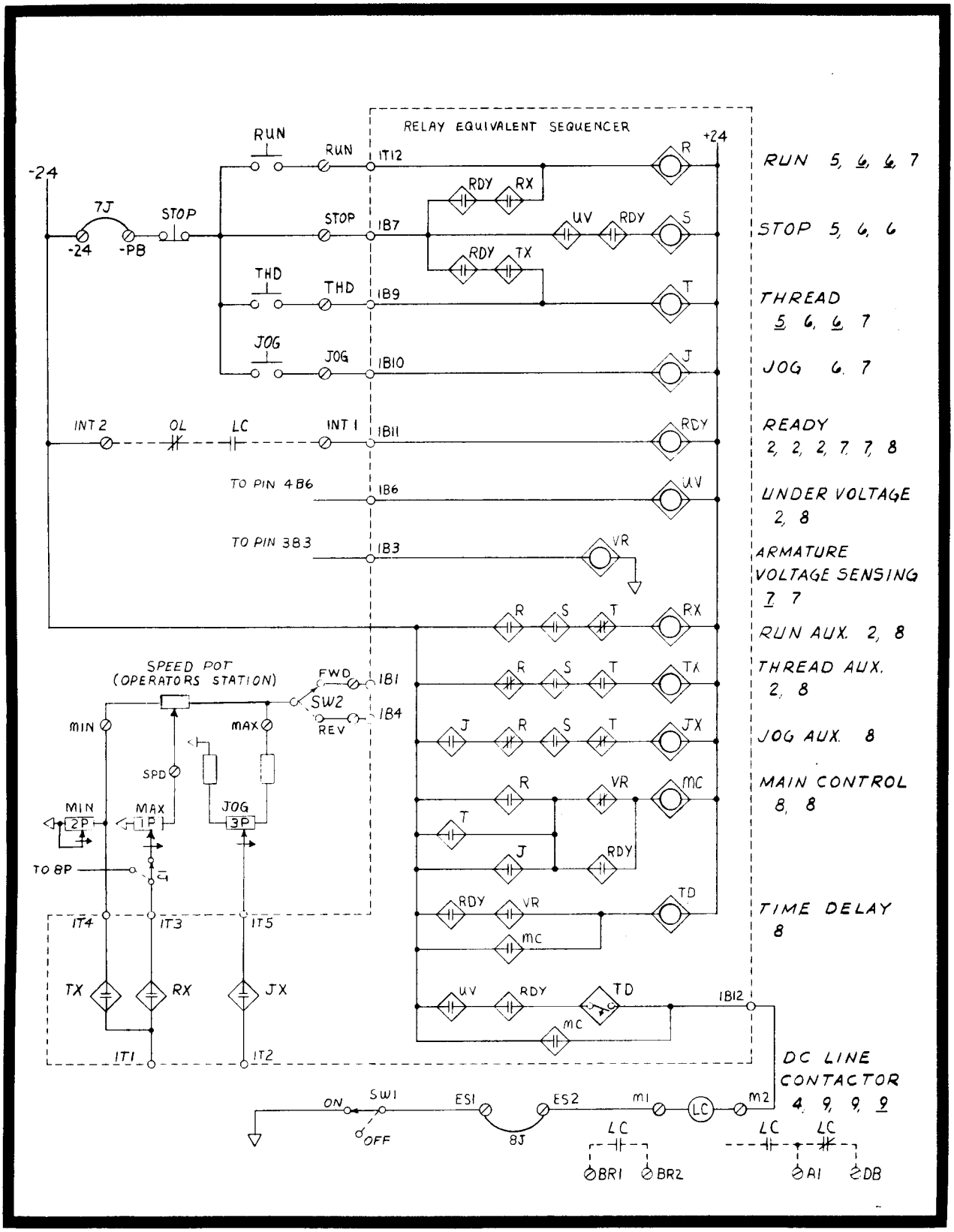

FIGURE 12 RELAY EQUIVALENT OF STATIC SEQUENCER

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3. Controller Board

A controller board schematic is shown in Figure 13. This board consists of an input controller (1-0A), a voltage controller (2-0A), a forward current controller (3-0A), a non-inverting output stage (5-0A) and a voltage sensor (6-0A).

As previously discussed in the system description of operation, the controller board provides parallel voltage and current control. The voltage controller is a proportional amplifier with rate limiting and a small filter on the voltage feedback to reduce spikes. The forward and reverse current controllers are PI controllers with a fixed lead of approximately 20MS which maintains the accuracy of the current loop. The outputs of the voltage controller, the forward current controller, and the reverse current controller are "OR"ed by the non-inverting amplifier. The output of this non-inverting amplifier is used to drive both the forward and reverse gating channels of the gate pulse generator.

The controller board may be used as either a CEMF voltage controller or a speed regulated controller by connecting jumper 3J in the appropriate position. For a CEMF voltage controller jumper 3J is placed in position 1. Thus, the input controller (1-0A) is a proportional amplifier with a rate limiting time constant of approximately 150MS. With 1-0A connected as a CEMF voltage controller, its inputs include the voltage reference signal and the motor armature feedback for IR compensation. If a speed regulated controller is desired, jumper 3J is placed in positions 2, 3, or 4. Thus the input controller is converted to a PI controller. This PI controller has three fixed lead time constants (position 2 provides approx. 20MS lead, position 3 provides approx. 100MS lead, and position 4 provides approx. 500MS lead) to compensate for various loading conditions. Positions 2, 3, or 4 should be used with low inertia loading, medium inertia loading, or high inertia loading respectively. Inputs to the PI controller include the speed reference signal, and the tachometer feedback signal. The "IR Comp" potentiometer on the master board should be turned fully counter-clockwise when the speed control mode is used.

Independent current limit adjustments are provided on the master board. Potentiometer 9P adjusts the forward current limit reference while potentiometer 10P adjusts the reverse current limit.

FET switches 1TR and 2TR provide the reset function for amplifiers 1-0A and 2-0A respectively to insure these amplifiers are held to zero until the contactor is energized.

Jumper 1J and associated components provide the correct voltage feedback and filtering for the Voltage controller (2-0A). 1J should be placed in position 1 for operation with a 180 VDC motor armature and it should be placed in position 2 for operation with a 90 VDC motor armature.

Jumper 2J and associated components provide the correct magnitude of tachometer feedback and a lag of approx. 10MS for stable operation. The components specified above have been sized for a DC tachometer output of 20.8 VDC/1000 RPM. 2J should be placed in position 1 for operation with 2500 and 3500 RPM motors and placed in Position 2 for operation with motors rated at 1750 RPM or less.

The Voltage Sensor (6-0A) and associated components, monitor the CEMF motor voltage and the first stage output of the optional ramp circuit. The output of the sensor is interlocked with the sequencer and the combination prevents picking up the contactor if there is a large voltage across the motor armature. They also permit the drive to regenerate to a stop before the contactor drops out when the stop pushbutton is pushed.

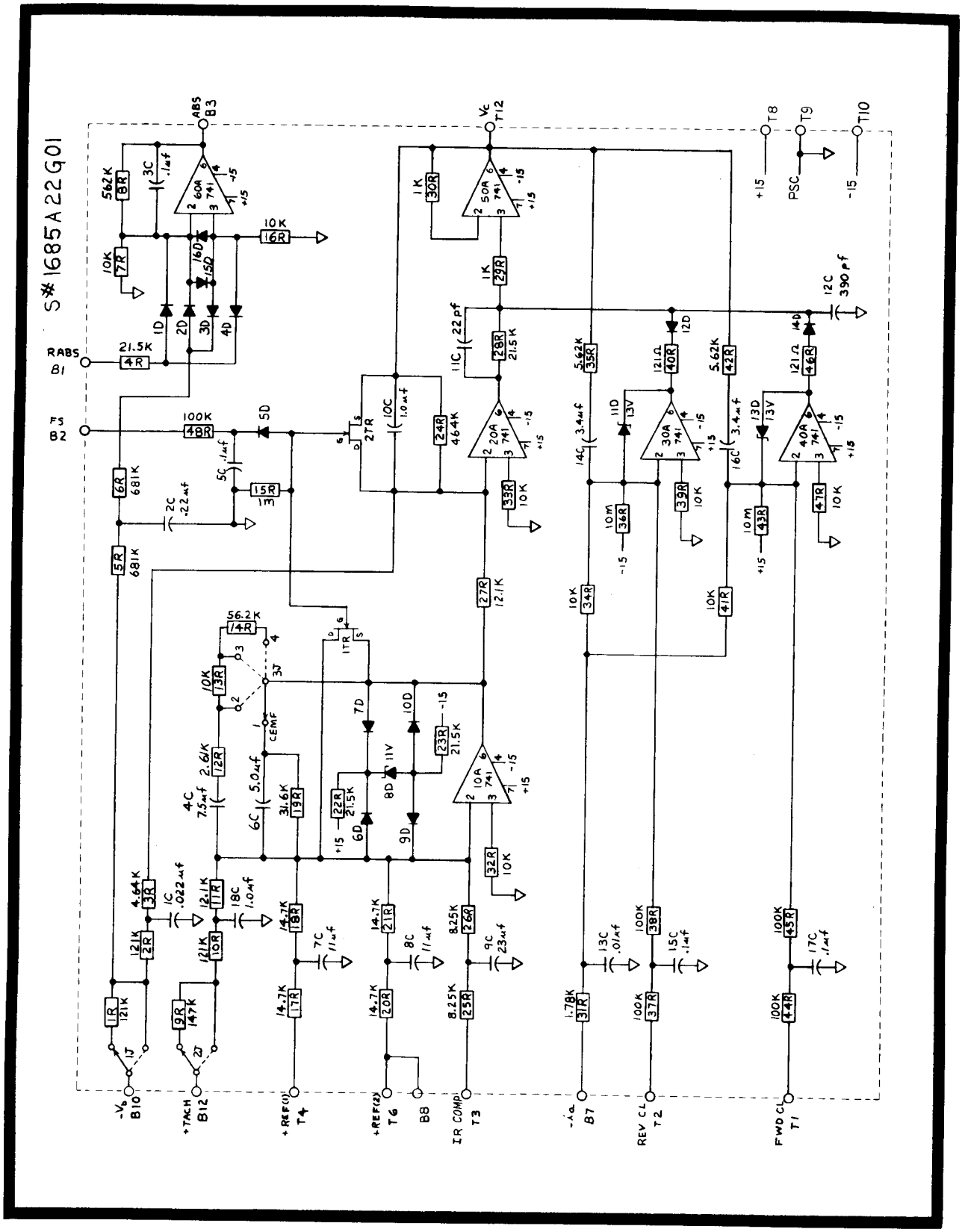

FIGURE 13 CONTROLLER BOARD

4. Power Supply/± Cosine Board

This board performs the functions of an unregulated ±24 VDC power supply, a ± cosine generator, and an undervoltage detector. See Figure 14 for a schematic diagram.

The unregulated ±24 VDC supplies are powered by the timing waves AC1 and AC2. These sine waves are rectified by diodes 1D through 4D to provide DC power where the voltage regulation and ripple are not critical.

The ±15 VDC regulated power supplies are simple series type transistor regulators. Transistors 1TR and 4TR are power amplifier stages. The ±15 VDC regulated supplies are used to supply power for integrated circuits and for reference voltages.

Cosine voltages (approx. 9.5 VP-P) are generated from the synchronizing sine input voltage by a passive filter and the operational amplifier 1-OA used as an integrater. An inverted cosine is available at the output of inverting amplifier 2-OA.

The undervoltage trip circuit can be described as follows. The input signal is decoupled from the -24V supply by diode 7D permitting the full-wave bridge output to appear across 2C and 21R. Other components are sized such that transistors 7TR and 8TR are in the off mode under rated voltage conditions. If the line voltage droops lower than 80% of rated voltage, transistors 7TR and 8TR turn on. Positive feedback holds the fault condition until the line voltage returns to 90% rated value. Transistor 7TR in the "ON' mode transmits an emergency stop signal to the sequencer board. Transistor 8TR inhibits gating when turned on. The circuit will permit a one cycle line dip but will trip if the dip is longer.

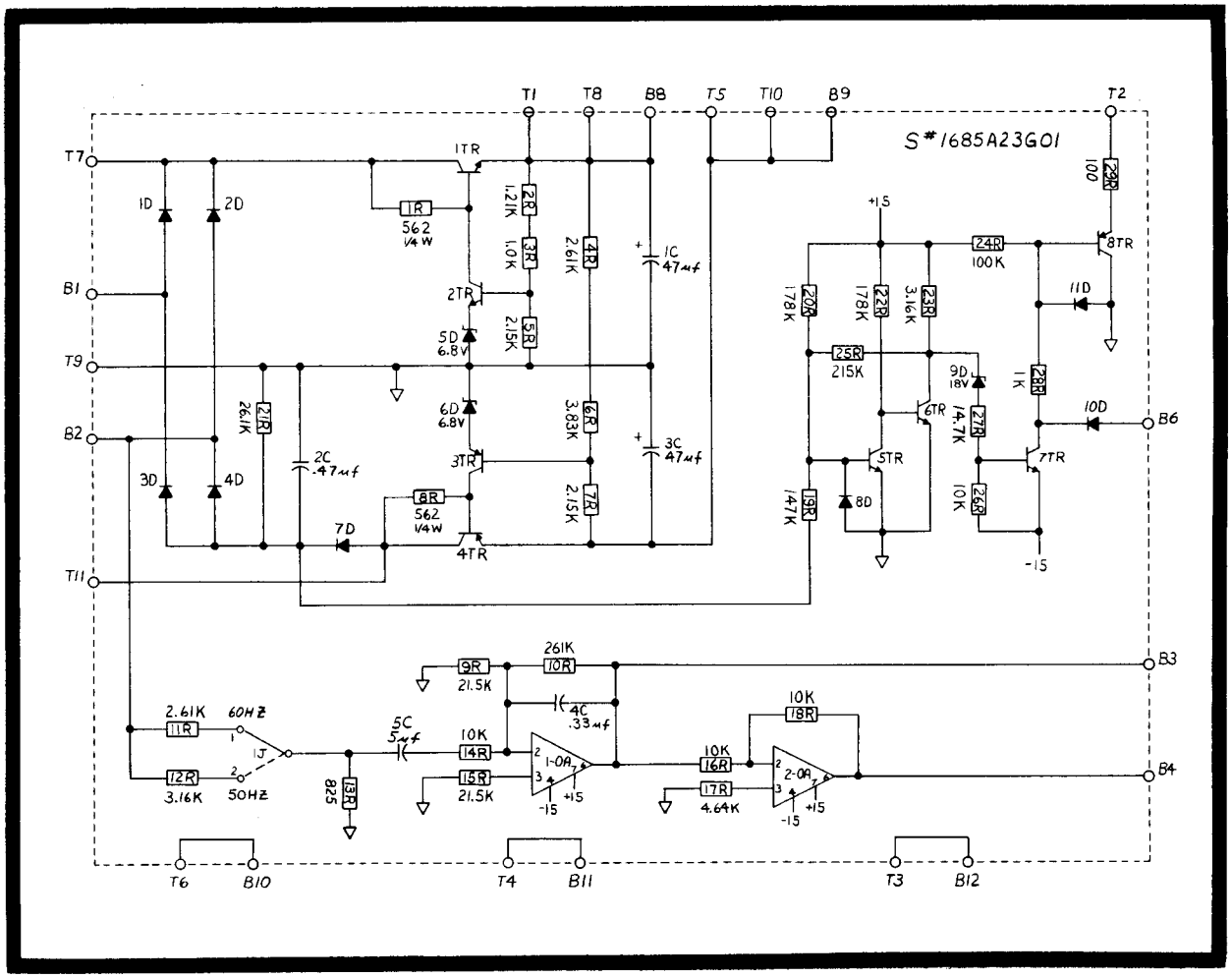

FIGURE 14 POWER SUPPLY/± COSINE BOARD

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5. Gate Pulse Generator (GPG)

A schematic of the GPG is shown in Figure 16. The GPG board contains four similar circuits, of which two form the forward GPG (circuits associated with operational amplifiers 1-OA and 3-OA) and the other two form the reverse GPG (circuits associated with operational amplifiers 2-OA and 3-OA).

Inputs common to all circuits are the controller voltage (V_c), a bias voltage (either ±24V), a 9.5 VP-P cosine wave (which is generated on the power supply board and either positive or negative in polarity), and an inhibit signal (phase shifted sine wave of either positive or negative polarity).

Since the circuits are similar, the operation of the circuit associated with 1-OA will be explained. Figures 15A, B and C show the phase relationship between the thyristor voltage, the cosine voltage, the bias voltage, and the inhibiting voltage. Figure 15D shows the algebric sum of the biasing signals for operational amplifier 1-OA with V_c = OVDC. For this case the algebraic sum is always positive and the output of 1-OA is clamped to approximately -.6V. In this state gate pulses are inhibited. Upon the application of a negative V_c signal of sufficient magnitude to make the algebraic sum negative, Figure 15E, the output of 1-OA switches to +13VDC releasing the initial gate pulse and enabling the picket fence gating to continue until the inhibiting signal dominates (α approx. 195° Figure 15F).

The gating angle responds instantly to the input DC control signal V_c to provide precise timing, and to avoid the insertion of time delays in the feedback control loops.

During the 180° following the forward voltage period, gating is inhibited to avoid reverse dissipation in the thyristors. The inhibiting signal also sets the phase advance limit of approximately α = 15°.

When the input DC control signal V_c demands a phase advance ahead of 15°, pulse generation will continue; the gating angle will remain at 15°.

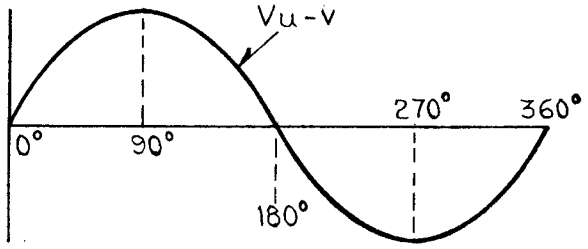

FIG.15A - REFERANCE VOLTAGE FOR THYRISTOR IN FWD ITPM

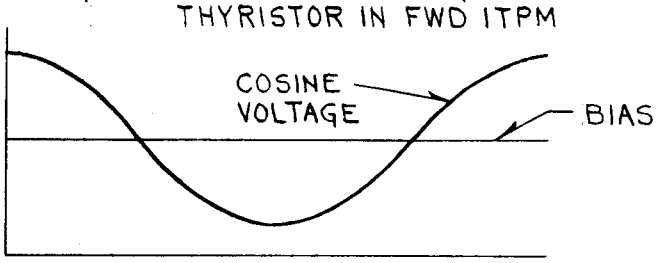

FIG.15B - COSINE & BIAS VOLTAGE

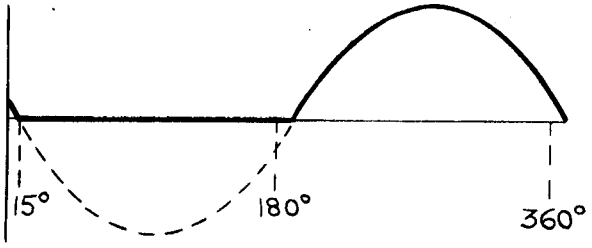

FIG. 15C - INHIBITING VOLTAGE

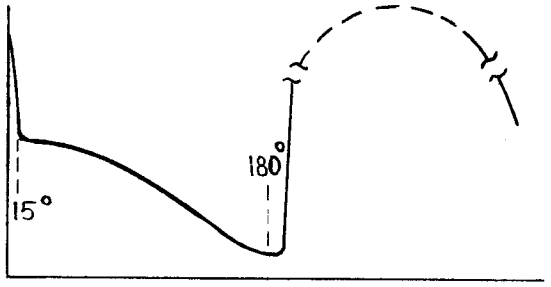

FIG.15D - ALGEBRAIC SUM OF FIG.15B & 15C

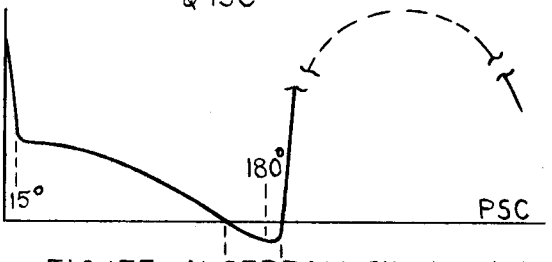

FIG.15E - ALGEBRAIC SUM WITH -V_c

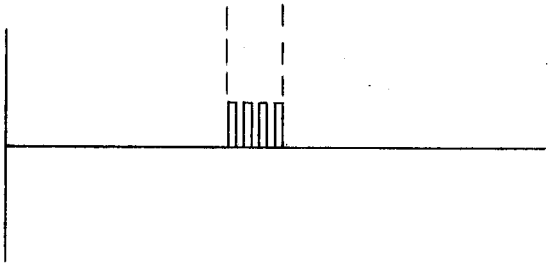

FIG.15F - GATE PULSE TRAIN

FIG.15

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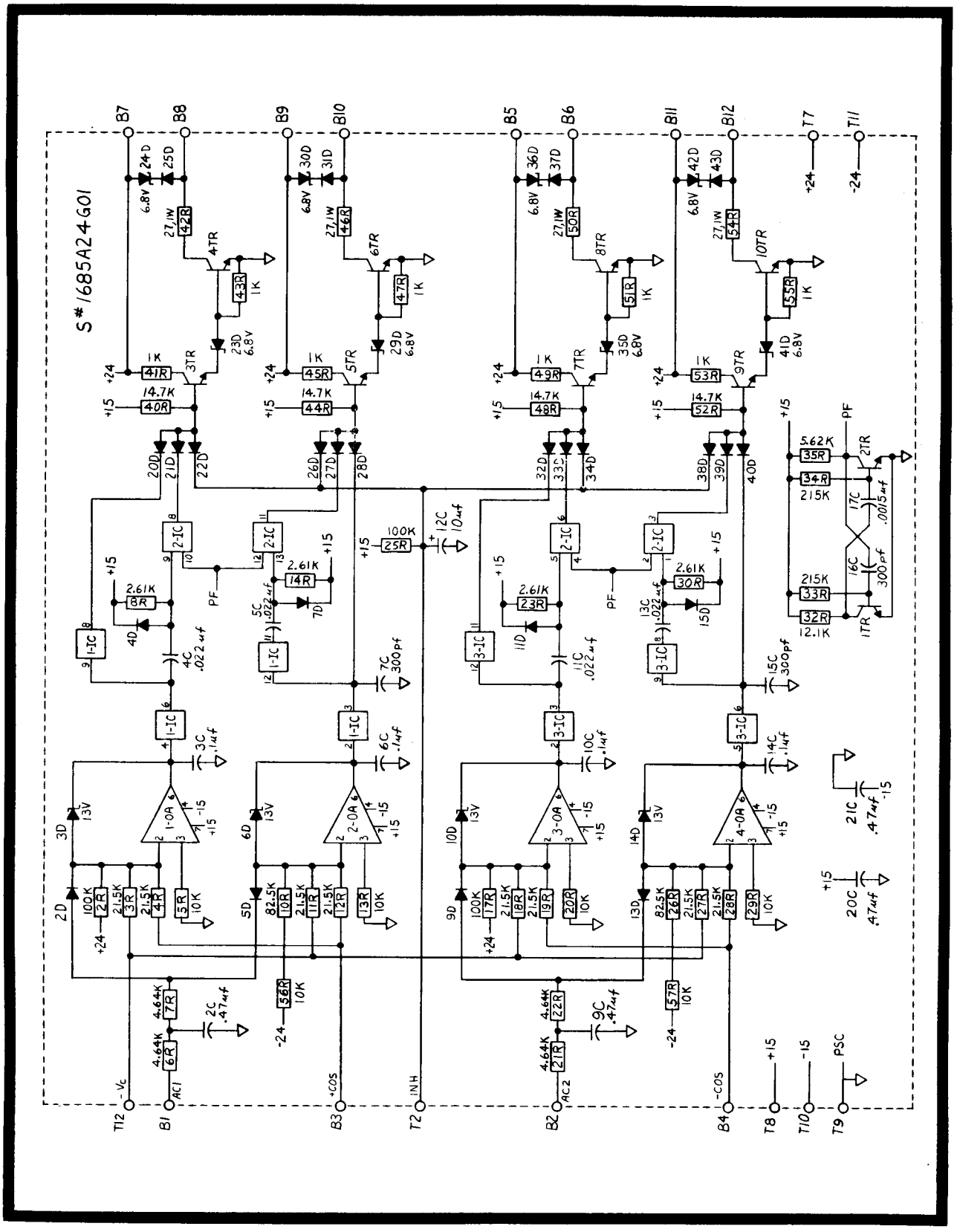

FIGURE 16 GATE PULSE GENERATOR

6. Ramp/Follow Board (Optional)

The schematic diagram of this board is shown in Figure 17. The board contains a Ramp function generator which provides a linear timed accel-decel range of 2 to 120 seconds and the process follow circuit will follow four standard signals without modification.

The 22-1000 Ramp Function Generator is a two amplifier non-inverting ramp generator. Positive and negative ramp rates are independently adjustable by means of 4P and 5P (located on the Master Board), which provide a 20 to 1 variation. Jumper 3J is used to select the ramp range; with 1J in position 2, potentiometers 4P and 5P provide a 0 to ±8V ramp signal in 2 to 40 seconds; with 3J in position 1, potentiometers 4P and 5P provide a 0 to ±8V ramp signal in 6 to 120 seconds.

The process control follow circuit provides an interface between a customer's reference signal (either voltage or current) and the required internal reference circuits. This signal should be connected between terminals PSC and FRF located on Back Panel Terminal Block 8TB. It is routed to the follow circuit via pin 2B11.

The standard input signals are 0 to 10 VDC, 1-5MA, 4-20MA, and 10 to 50 MA. If the drive should be controlled by signals of different magnitudes, the engineer must calculate the necessary dropping or shunt resistor and have it mounted on the turret terminals provided. The output of the process control follow may be inverted by applying -24VDC with respect to PSC to terminal 2B10 via Master Board Terminal FRV or by Jumper 4J. This allows bi-directional speed control from a undirectional reference signal.

The operation of the 6 jumpers contained on this board are as follows:

1. Jumper 1J selects the output of the ramp circuit (position 1) or the output of the follow circuit (position 2) as the speed control reference. Thus, if the follow circuit ONLY is used, 1J should be in position 2. But, if the follow circuit is used in combination with the ramp or the ramp circuit only, 1J should be in position 1.

2. Jumper 2J, position 2, is provided to connect the output of the follow circuit to the ramp input. If this is not required, 2J should be in position 1.

3. Jumper 3J determines the ramp rate range as previously described.

4. Jumper 4J, position 1, provides an inversion in the follow circuit reference polarity. 4J should be in position 2 for a non-inverted follow circuit or if inversion is required by an external switch.

5. Jumper 5J should be connected in position 1 for a miscellaneous voltage signal, position 2 for a 0 to 10VDC signal, and position 3 for a current signal. Note when in position 1, an appropriate resistor must be connected to the turret terminals provided.

6. Jumper 6J provides the correct shunt resistor for a current signal, position 1 should be used for a 1 to 5MA signal, position 2 should be used for a 4 to 20MA signal, position 3 should be used for a 10 to 50MA signal, and position 4 should be used for a miscellaneous current or when a voltage signal is used. For position 4 and a miscellaneous current signal, an appropriate shunt resistor must be connected to the turret terminals provided.

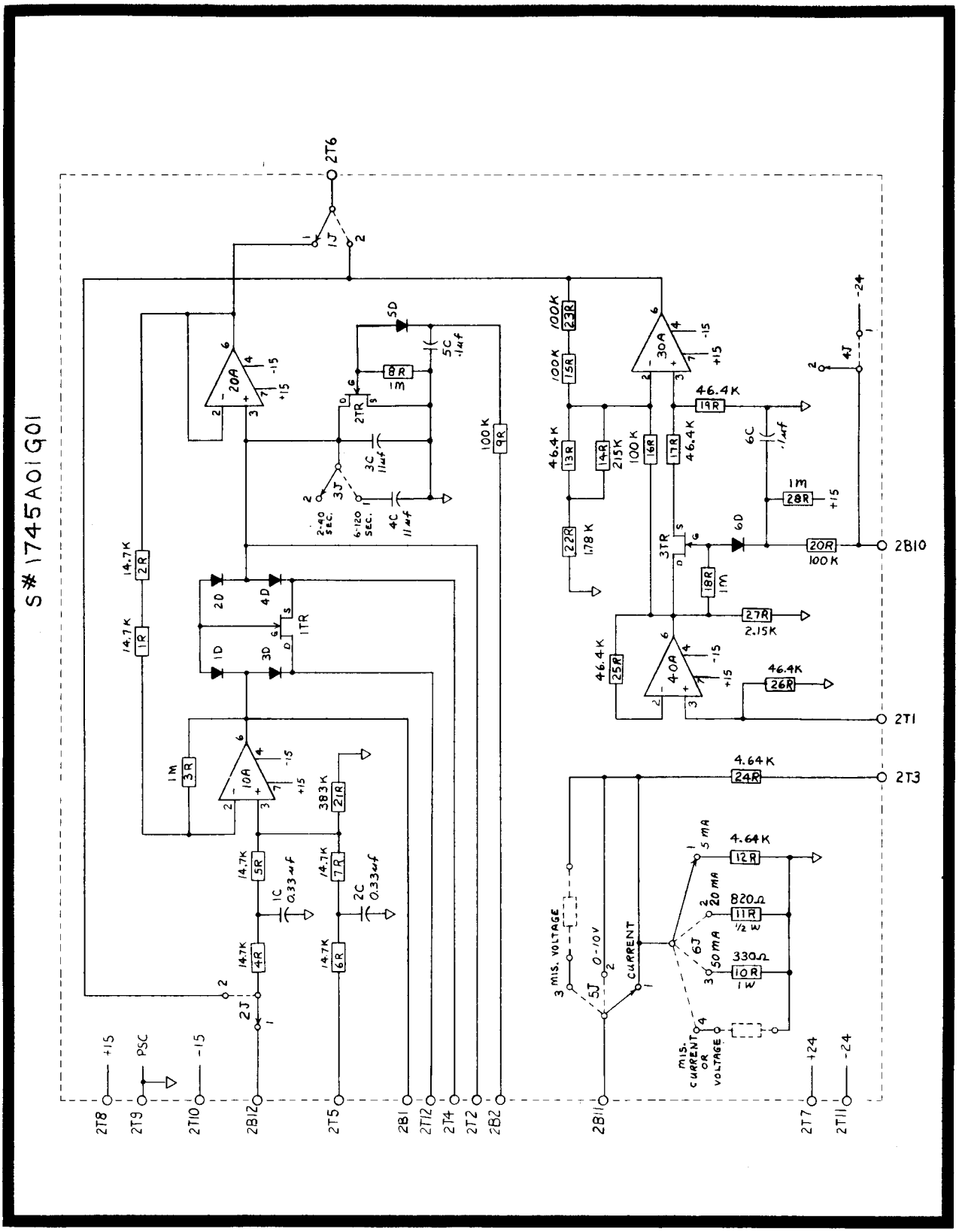

FIGURE 17 RAMP/FOLLOW BOARD

D. Back Panel Assembly

This assembly contains all the power components for a 22-1000, single phase, regenerative drive, as well as the gate pulse transformer printed circuit card. Figure 18 is a schematic diagram of the back panel assembly, and shows all the back panel components interconnected with the exception of the gate pulse transformer circuits whose connections are implied by Figure 19.

The power components contained on the back panel assembly are the fuses, thermal circuit breaker, control transformer, current shunt, line contactor, overload relay, R-C networks, and terminal blocks for customer connections.

The fuses are sized for thyristor protection in the event a fault occurs. They are not an ordinary fuse, but a current-limiting fuse with a high interrupting capacity. Fuses should be replaced with exact duplicate devices.

In addition to the protection provided by the fuses the ac line thermal breaker serves as additional protection and a positive line disconnect for maintenance functions.

The control transformer provides the control power for the regulator assembly. It is connectable for either 230 or 115 VAC operation as indicated in Figure 18.

The current shunt provides a current feedback signal to the regulator. -.5 VDC is the value of the feedback signal for rated current.

The main sequencing device is the dc line contactor between the power converter and the dc motor armature. Its main function is to positively de-energize the motor armature. However, it also provides a power contact for dynamic braking and another power contact for ac brake control. The line contactor has an auxillary contact which is interlocked with the regulator. This interlock maintains the run and thread control circuits after their respective push-buttons are released, and also prevents the application of the speed reference until the contactor is energized.

The thermal overload relay provides long term motor overload protection. The overload contacts are connected in series with the line contactor auxillary contacts such that if an overload trip occurs the regulator is sequenced to the stop mode. The line contactor drops out without a time delay, and the drive has to be manually restarted.

Three terminal blocks are provided on the back panel assembly for customer convenience. Terminal block 6TB is primarily for power connections to the motor armature and field. Terminal blocks 8TB and 9TB provide a means for connecting the external control signals to the regulator assembly. These terminal blocks are connected to terminal blocks 3TB and 2TB of the master board by pre-cabled harnesses.

Figure 9A shows the connections to the regulator for the door mounted operator station. When an external operator station is used, it is connected to the equivalent terminals on 9TB. Terminal block 8TB contains connection points for various control signals as described below:

1. RCL and FCL are used where external control of current limit is required. The application of 10 volts with respect to PSC will provide current limit at 100% current. RCL requires negative voltage, and FCL requires positive voltage.

2. TACH is used to connect the DC tachometer generator for speed regulated drives. The other side of the tachometer generator is connected to terminal PSC.

3. PSC is the power supply common. All control references have one side connected to this point, and the other side connected to their respective input terminals i.e., RCL, FCL, TACH, CRF, RRF, AND FRF.

4. CRF and RRF are test inputs into the controller and optional ramp function generator respectively. They are not normally used.

5. FRV is used in conjunction with the process signal follower option. It can be used to reverse the direction of the motor without reversing the process signal by connecting FRV to terminal -24 on 9TB. This can be done with a jumper or a relay contact.

6. ES1 and ES2 provide a means for connecting an emergency stop contact into the drive. When this contact is momentarily opened, the line contactor will immediately be de-energized. Therefore a normally closed contact is required. When this feature is used, remove jumper 8J from terminals ES1 and ES2 on terminal block 3TB on the master board.

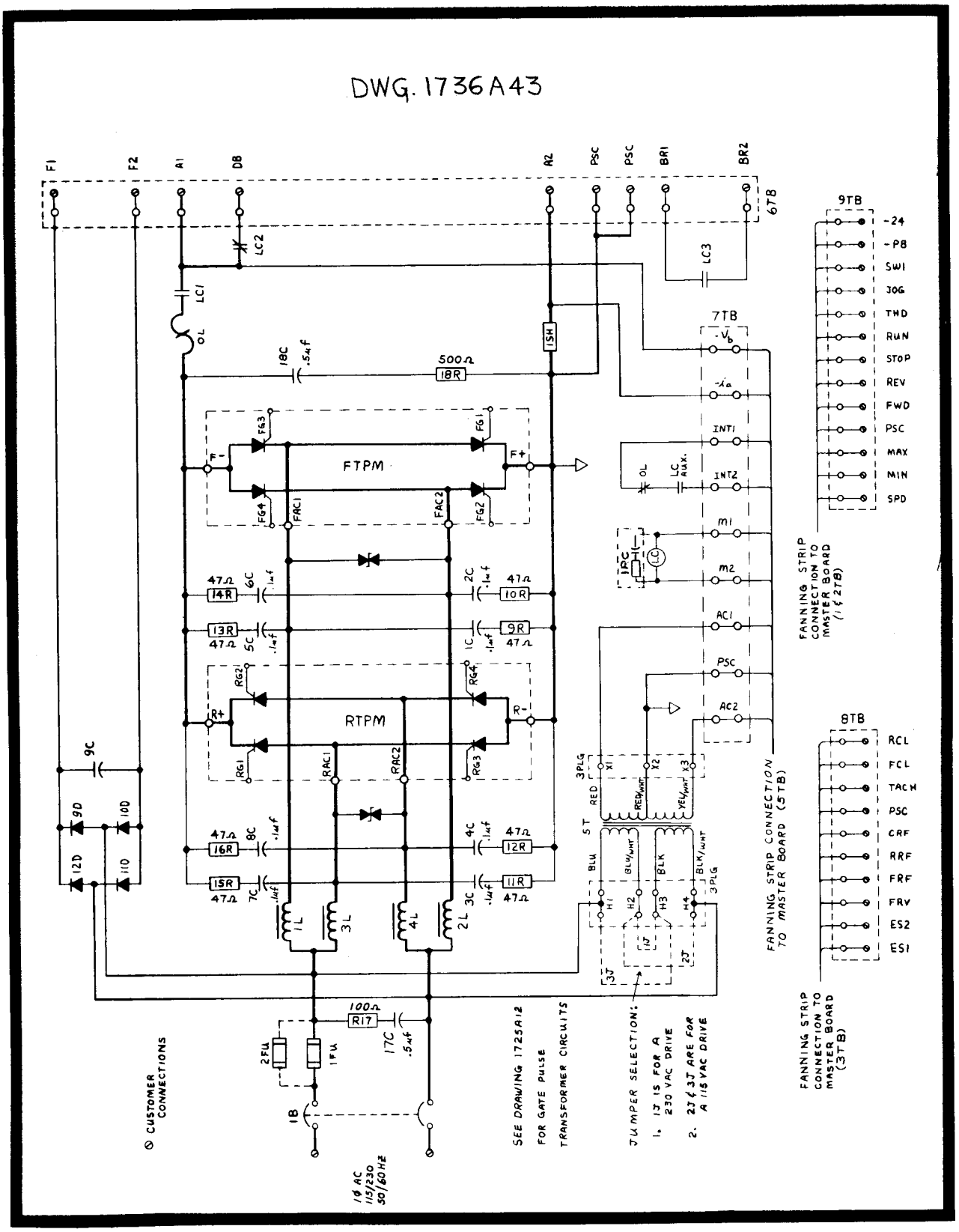

FIGURE 18 BACK PANEL ASSEMBLY

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A schematic diagram of the gate pulse transformer board is shown in Figure 19. This board is a convenient mounting place for the gate pulse transformers and the individual R-C networks associated with the ITPM's. It permits a minimum number of connections to the ITPM's as well as short interconnecting lead lengths. The gate pulses are routed directly from the gate pulse transformers to the forward and the reverse ITPM's via plugs 1PLG and 2PLG respectively. In addition to the above, the ferrite reactors and a constant potential field supply are mounted on the gate pulse transformer board. Also the control transformer terminations are made via 3PLG located on this assembly.

The gate pulse transformers provide the necessary isolation and further shape the gate pulses. These pulses are generated by the gate pulse generator and routed from the master board terminal block 4TB to the gate pulse transformer board terminal block 1TB via a pre-cabled harness.

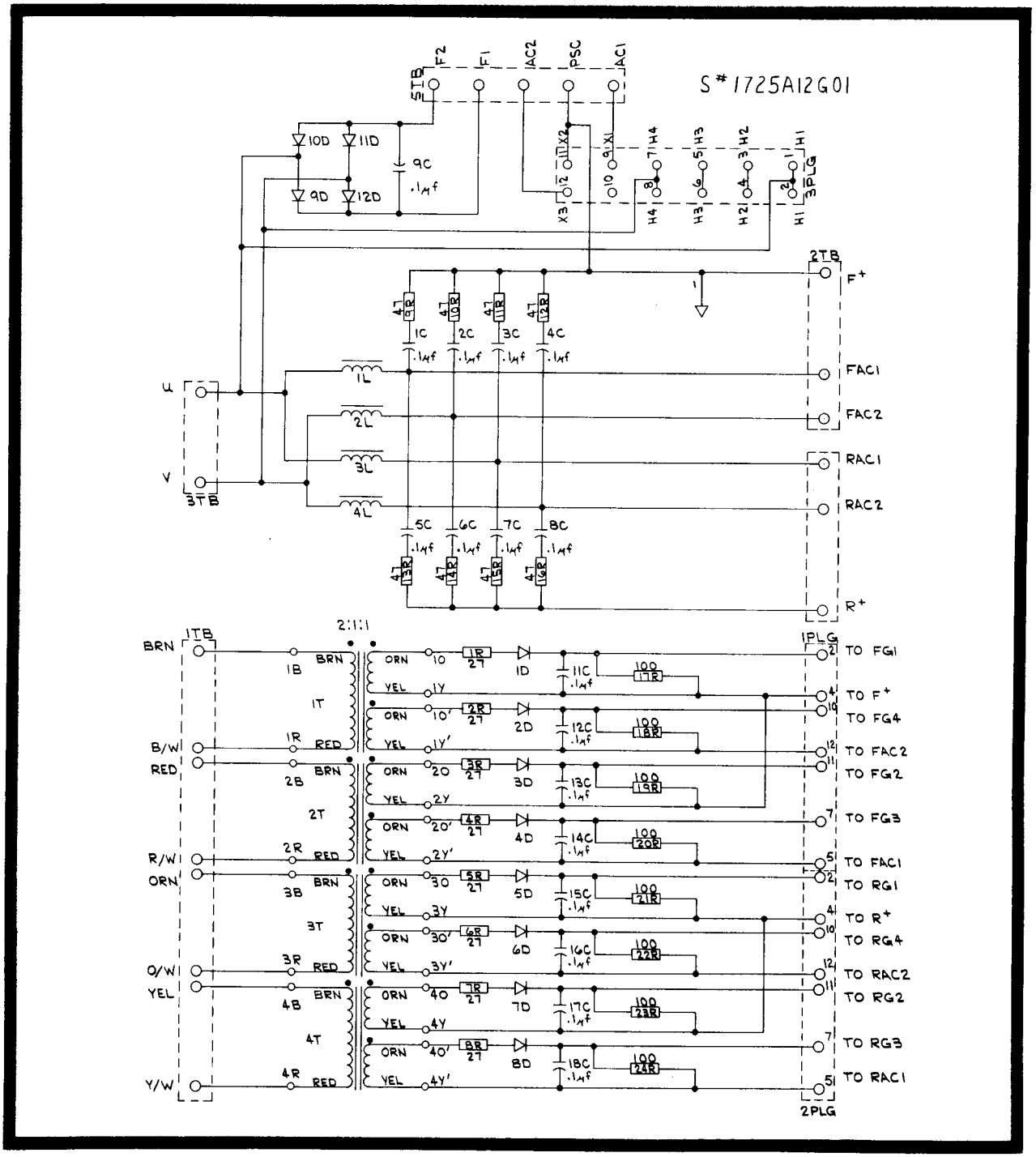

FIGURE 19 GATE PULSE TRANSFORMER BOARD