"22-1000 3Ø REGENERATIVE DRIVE (C600M)"

INDEX

I. INTRODUCTION

C-600M thyristor power systems (TPS) provide a line of controlled-voltage drives for armature excitation of dc machines from 5 HP to 20 HP. The rated armature voltage is 240 volts dc. The TPS consists of a panel and a three phase zig-zag isolation transformer with the neutral of the transformer secondary grounded.

The C-600M panels feature front accessibility, high package density, and a minimum number of adjustments. They include the thyristor power modulator (TPM), regulator cage (gate control, ±24V unregulated supply and ±15V regulated supply, armature controller, static sequencer, calibration board, protection board, optional test kit board, and one slot for an optional board to be used for additional calibration, detectors, etc.,), current shunt, thyristor breaker, and other elements (control transformer, contactor, fuse blocks and customer terminal blocks).

A constant potential or adjustable voltage exciter of 6A rating can be added to the panel. They are used to excite the field of the dc machine whose armature is powered by the main converter.

C-600M TPS are wall mounted open panels with the thyristor transformer separately mounted. In more complex systems the C600M panel may not contain the reference processing and director functions, but they may be contained on separate panels.

II. SCOPE OF APPLICATIONS

Phase-controlled thyristor converter circuits can be classified into three groups. In the semiconverter configuration, only part of the rectifying legs are thyristors; whereas, others are diodes. This yields a power system for one-quadrant operation, which means that neither output voltage nor current is reversible.

In the single-converter configuration, all legs are thyristors. The output voltage is reversible, but not the output current, resulting in two-quadrant operation.

Connecting two single converters back to back, yields a power system with four-quadrant capability providing current and voltage of both polarities. This configuration is named double converter.

C-600M thyristor power systems use double converters of the three-phase, single-way circuit configuration. The forward and reverse converters have the same rating. As three legs are employed, three pulses per cycle are produced in the dc output. Since the ripple content in the armature current contirbutes to motor heating, the motor has to be designed for use in three pulse thyristor drives.

C-600M TPS are designed primarily to provide power for armatures of dc motors where regeneration is required. Where regeneration is not required a 22-1000 semiconverter would probably be used.

The TPS includes the regulator to perform the function of voltage control with current limit, speed control with current limit, or current control with either outer voltage or speed limit. While the converter has the same capacity in forward and reverse direction, the regulator can be programmed to have different instead of equal forward and reverse current limit settings. The command system may be part of the TPS, as is the case in standard applications, or part of a central director in special applications.

Specifications and Ratings are covered in a later section of this I.L.

III. THYRISTOR POWER CONVERTER

A. Phase-Controlled Converter Principles

A thyristor power converter is an apparatus which by means of phase-controlled gating of thyristors (or other controlled rectifier cells) converts an ac supply line voltage into an adjustable dc voltage; this process is known as rectifying. Inversely, dc voltage can be converted back into the ac line voltage; this mode of operation is called inverting. A converter which only can perform one of these functions is called a rectifier or an inverter, respectively.

Once a thyristor is turned on, it can only be turned off by reducing the anode current to a very small value. In the phase-controlled converter, the ac line voltage performs the function to end the conduction period by commutating the anode voltage.

Many converter configurations have been developed. The three-phase, single-way double converter is the type used in C-600M. Figure III-1 shows the elementary schematic for the forward converter. The transformer has a delta primary and zig-zag secondary with the neutral grounded. The zig-zag secondary is necessary to prevent the transformer core from saturating (a situation which could occur if a wye secondary were used and unequal currents should flow in the three thyristor legs). The purpose of the transformer is to adjust the line voltage to the proper level, to provide isolation, to establish a neutral for a current return path, and to introduce inductance into the converter current path. This inductance is required to control the rates of currents during commutation and faults as will be seen later. The load circuit consisting of a counter emf e_a, resistance R_d, and inductance L_d is connected between the dc output of the converter and the neutral of the transformer.

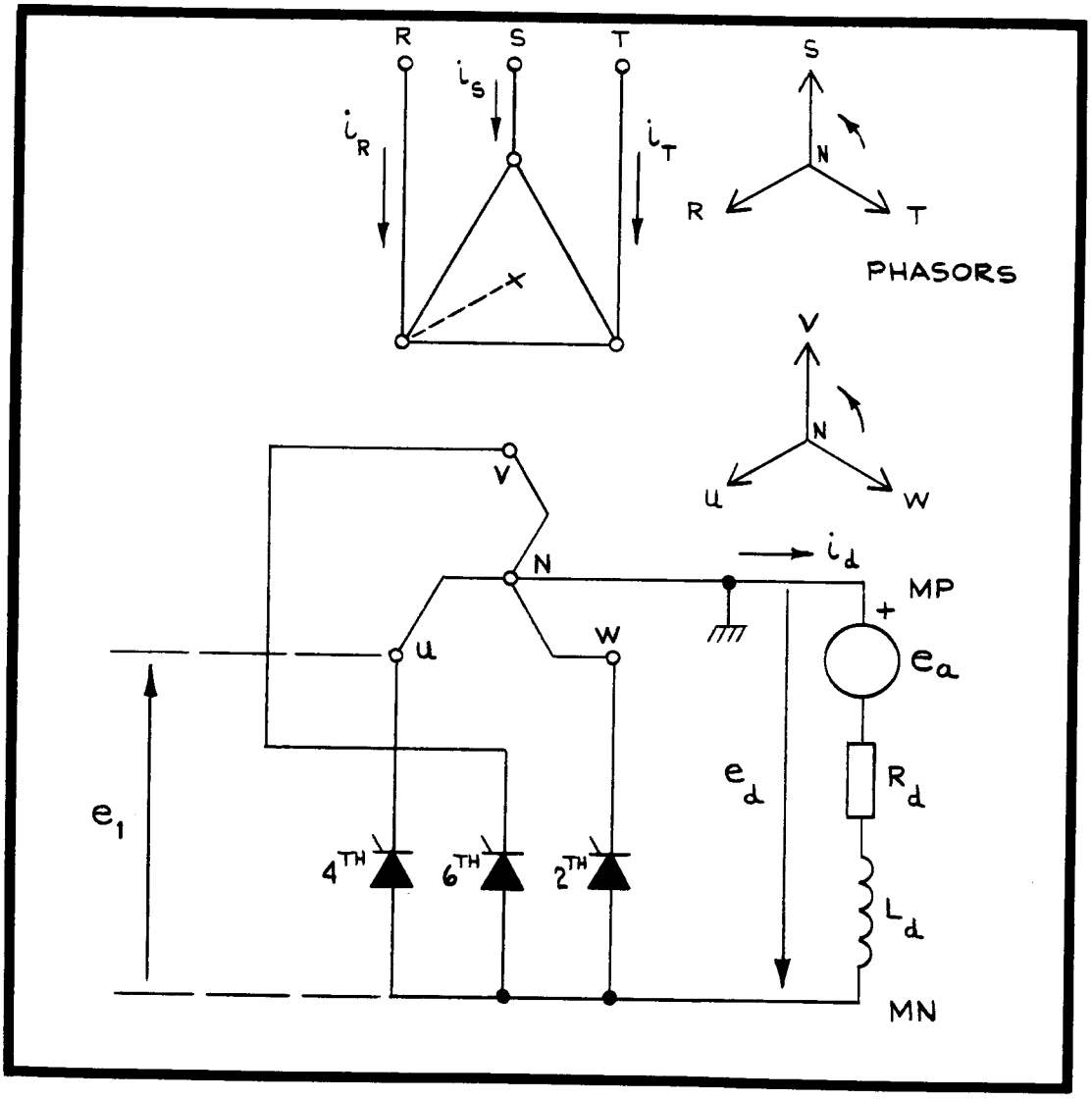

FIGURE III - 1 THREE-PHASE SINGLE-WAY CIRCUIT

The significant current paths and waveforms can now be developed (Figure III-2). The uppermost traces show the secondary phase voltages measured from the neutral to the phase. Initially, all thyristors are assumed to be in the blocking state. At 60° after N - U voltage just exceeds N - W a pulse is applied to thyristor No. 4. Current flows from the neutral (MP) through the load to MN through 4TH to U. However, 120° later a pulse is applied to 6TH. Since the voltage N-V is larger than N-U at this instant current will commutate from 4TH to 6TH. Again 120° later a pulse is applied to 2TH and a similar commutation will take place. Assuming that the load is highly inductive, the dc current will reach a steady value after a number of cycles, and each thyristor will then conduct a 120° wide current block each cycle. The respective waveforms of the thyristor anode-cathode voltages can now be developed. Figure III-2 illustrates this for a gating angle of $\alpha = 60°$. Note that α is measured from the point where the anode-cathode voltage of the respective cell swings positive. Hence for $\alpha = 0$ the thyristors do not have to absorb any positive voltage anymore and are then comparable to single diodes. It is apparent from the waveshapes of the output voltage that its average value E_d is a function of the gating angle. It reaches a maximum at $\alpha = 0$, is zero for $\alpha = 90°$ and assumes negative values back to $\alpha = 180°$. This transfer curve can be obtained by integrating the waveforms. The result is

$$E_d = E_{do} \cos\alpha$$

where the saturated output voltage is

$$E_{do} = \frac{3}{\pi\sqrt{2}} E_u$$

where E_u . . . line to line rms ac voltage.

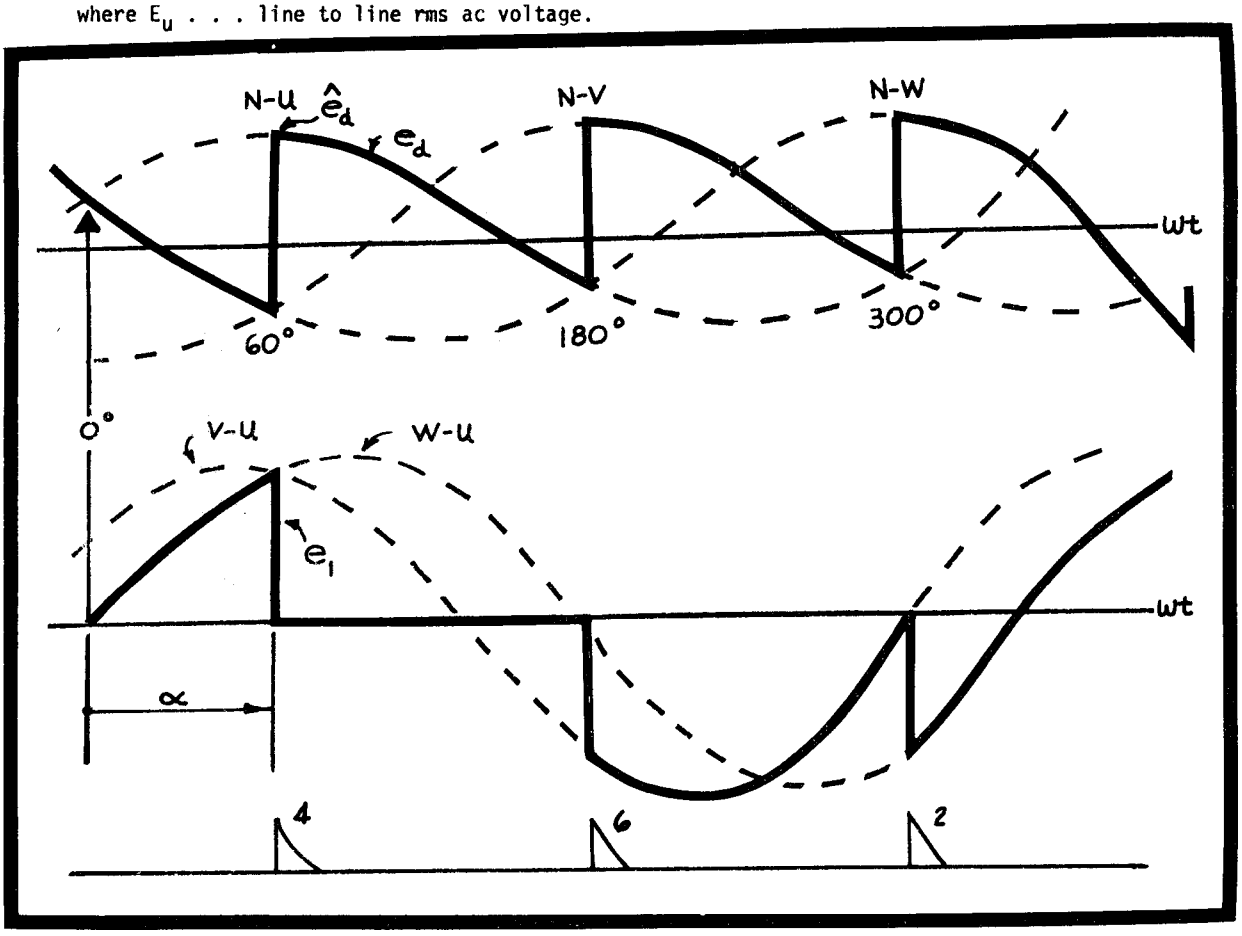

FIGURE III-2
WAVEFORMS OF THYRISTOR CONVERTER AT $\alpha = 60°$

Since the load current cannot reverse, the average power flow will change its sign with the voltage. Rectifier operation ($\alpha < 90^0$) renders motoring in the load circuit whereas inverter operation ($\alpha > 90^0$) requires the load to be generative. Figure III-3 illustrates the range of operation on a time basis. In the beginning, the converter is operated in its rectifying mode with $\alpha = 30^0$. Then α is steadily increased into the inverter mode of operation. The lower trace shows the voltage across one of the thyristor legs.

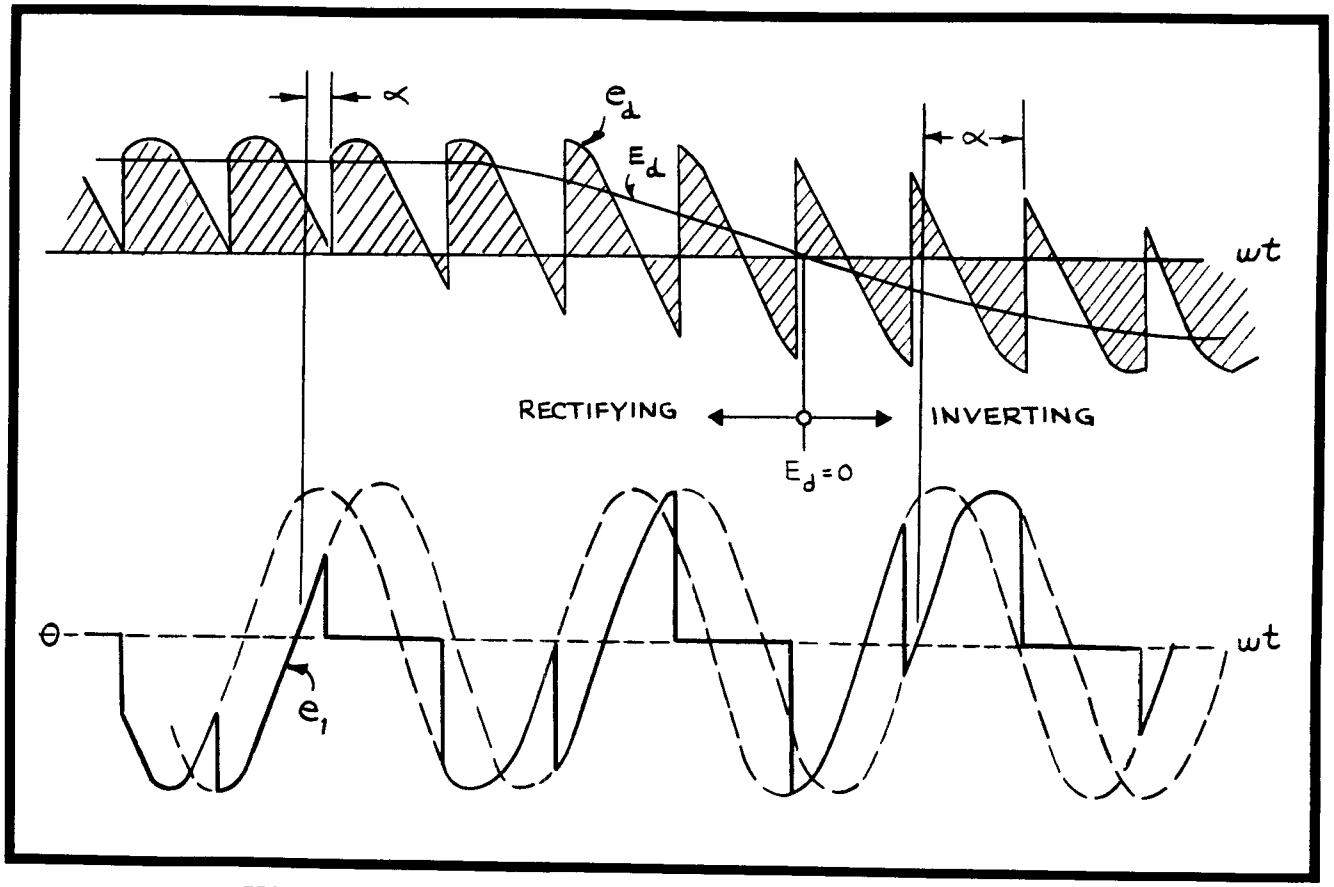

FIGURE III-3 RANGE OF OPERATION ILLUSTRATED ON A TIME BASIS

ON THE LEFT, $\alpha = 30^0$, RECTIFYING MODE. α THEN INCREASES TO INVERTER MODE

Up to this point, the reactances offered by the transformer and the power line have been neglected. This so-called commutating reactance, however, is significant. Instead of instantaneously commutating the load current from one leg to another leg (upon gating of the latter), the current rate is limited and shaped by it. This means that both these legs conduct simultaneously for a period of time, shorting out effectively the ac source. This produces notches in the sinewave measured on points U-V-W, which, in turn, reduce the dc bus voltage.

The description so far has been made with the assumption that the dc load current is continuous. In a practical circuit with a dc motor armature as load, the actual operation always covers the range of discontinuous current at light load levels also. Reducing the load current, one finally reaches a level where the ripple amplitude is high enough to interrupt the current cyclicly. At this transition point, the output voltage E_d rises sharply (keeping α constant) with decreasing load current and aims to a point equal to the peak converter voltage $\hat{e}_d$ at zero load current. This transition point depends on the gating angle α, the inductance and losses in the load circuit.

Commutation from a first leg to a second must always be completed before the anode voltage of the second leg swings negative. If the latter should happen, the commutation is incomplete and the full-load current will commutate back into the first leg. This situation can only arise if the commutation was initiated at a high gating angle (in the inverter range) and if the load current is continuous.

The circuit described so far can provide voltage of both polarities. The current, however, can only flow in the conducting direction of the rectifying cells. This circuit is, therefore, classified as a single converter.

For C-600M a second converter is added and connected to the first in an antiparallel circuit as shown in Figure III-4. Since such a circuit can produce load current in both directions, this circuit is classified as a double converter.

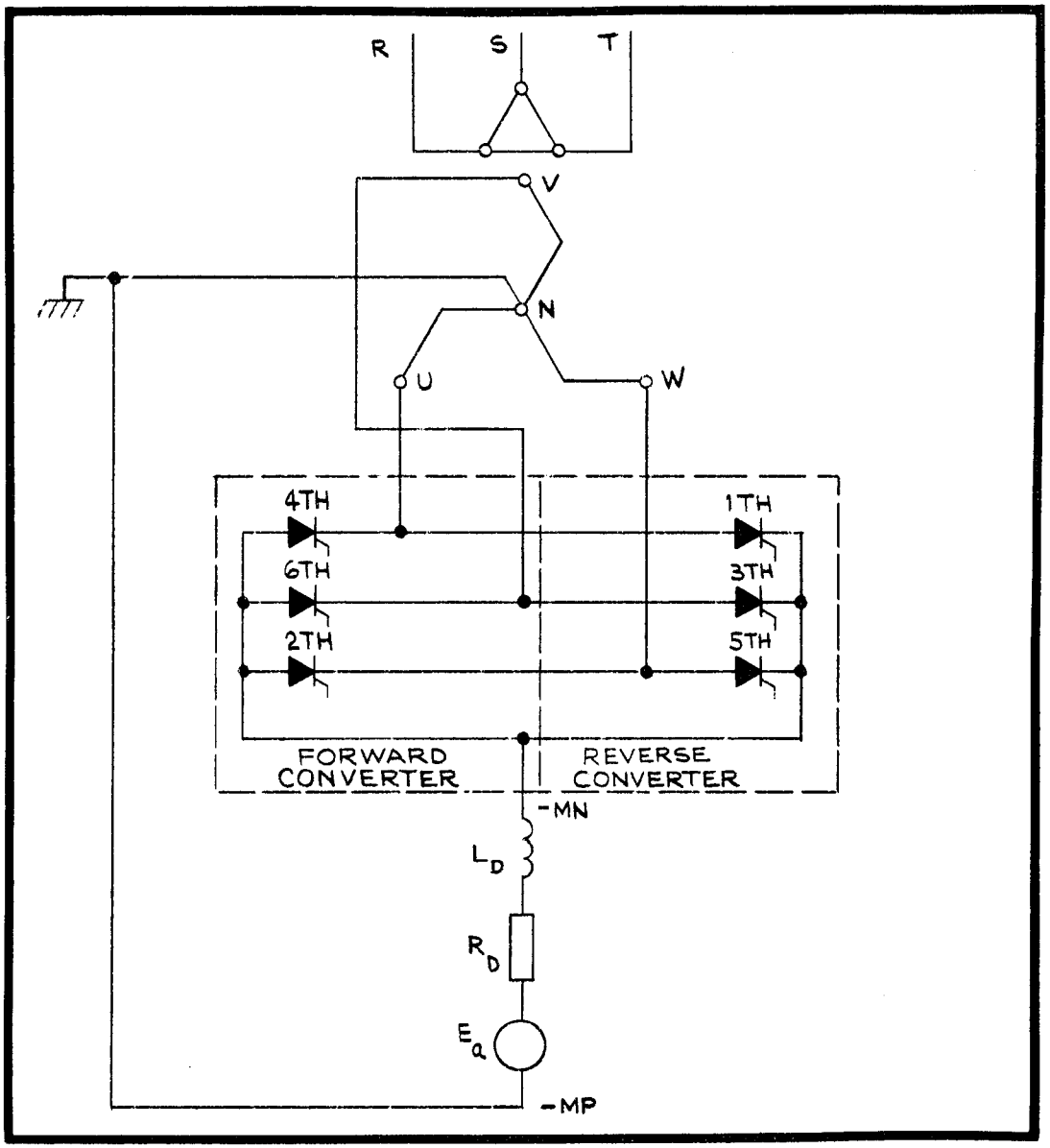

FIGURE III - 4 DOUBLE CONVERTER

There are several ways to control such a double converter. The principle used in C-600 is to use two gating channels, but biased such that circulation current control cannot occur. The operation will now be explained with the help of Figure III-5. The systems diagram shows the main control elements of the double converter, with the power circuit in single line diagram form. An inner current loop is closed. While this regulation loop helps greatly to overcome the nonlinearities of the power converter when going from continuous to discontinuous current, the decrease in gain for the system requires that the voltage or speed controller (immediately prior to the current controller) be of standard design to operate satisfactorily in this varying gain region.

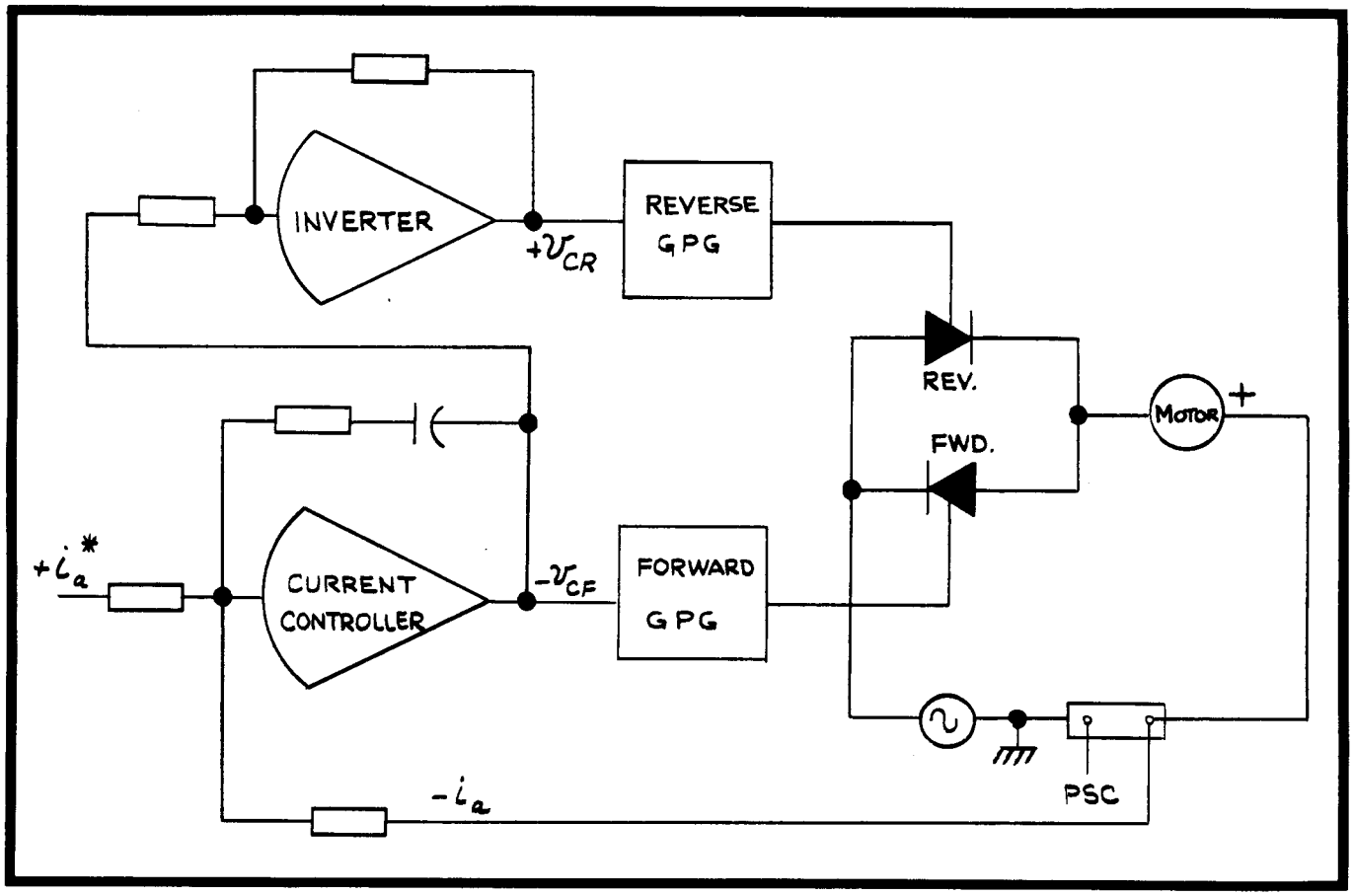

FIGURE III - 5 DOUBLE CONVERTER SYSTEM

The armature current (-ia) is sensed by the shunt and brought to one input of the current controller. There it is compared with the current reference $+i_a^*$ which is applied at a second input. When both inputs are zero, the output ($-v_{CF}$) will be zero as well as the output of the inverter ($+v_{CR}$). The current controller and inverter act together as a differential output amplifier, so when one output goes negative, the other goes positive, and the sum of the outputs is always zero. With both inputs to the GPG's zero, referring to Figure III-6, it can be seen that no current will flow in either converter. When $+i_a^*$ goes positive, $-i_a$ goes negative, and the forward converter phases towards $\alpha = 0^0$, until the current feedback signal -ia matches the reference $+i_a^*$, resulting in forward current.

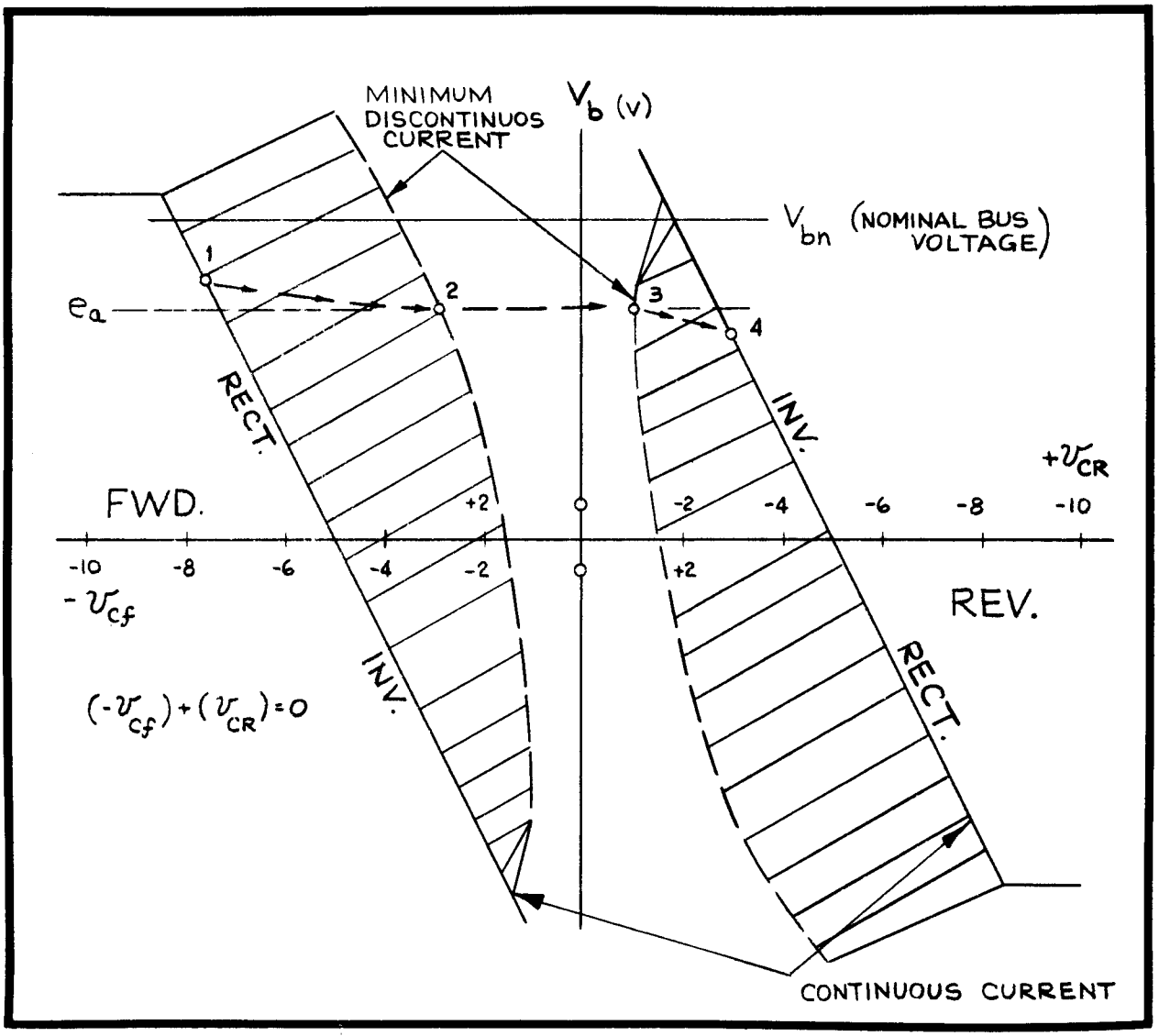

FIG. III - 6 DOUBLE CONVERTER COATED CHARACTERISTICS

With the aid of Figure III-6, a current reversal will be described. The counter emf e_a of the load is assumed to be as shown in Figure III-6 (continuous current is flowing) with the forward converter rectifying at point 1. Suddendly a current reversal is demanded as a result of $+i_a^*$ going from a positive to a negative value. This will cause $-v_{cf}$ to advance toward a positive value and $+v_{CR}$ to advance toward a negative value. At point 2 the forward current will stop altogether and V_b will equal e_a. At point 3, $+v_{CR}$ will have become negative enough to start inverting current in the reverse converter. Finally at point 4, the new quiescent state of reverse current has been reached and $-i_a$ is matching again the reference $+i_a^*$

The opposite sequence of events take place in case of a change from reverse to forward current.

Figure III-7 shows an oscillogram of a current reversal in the double converter with a step change of current reference.

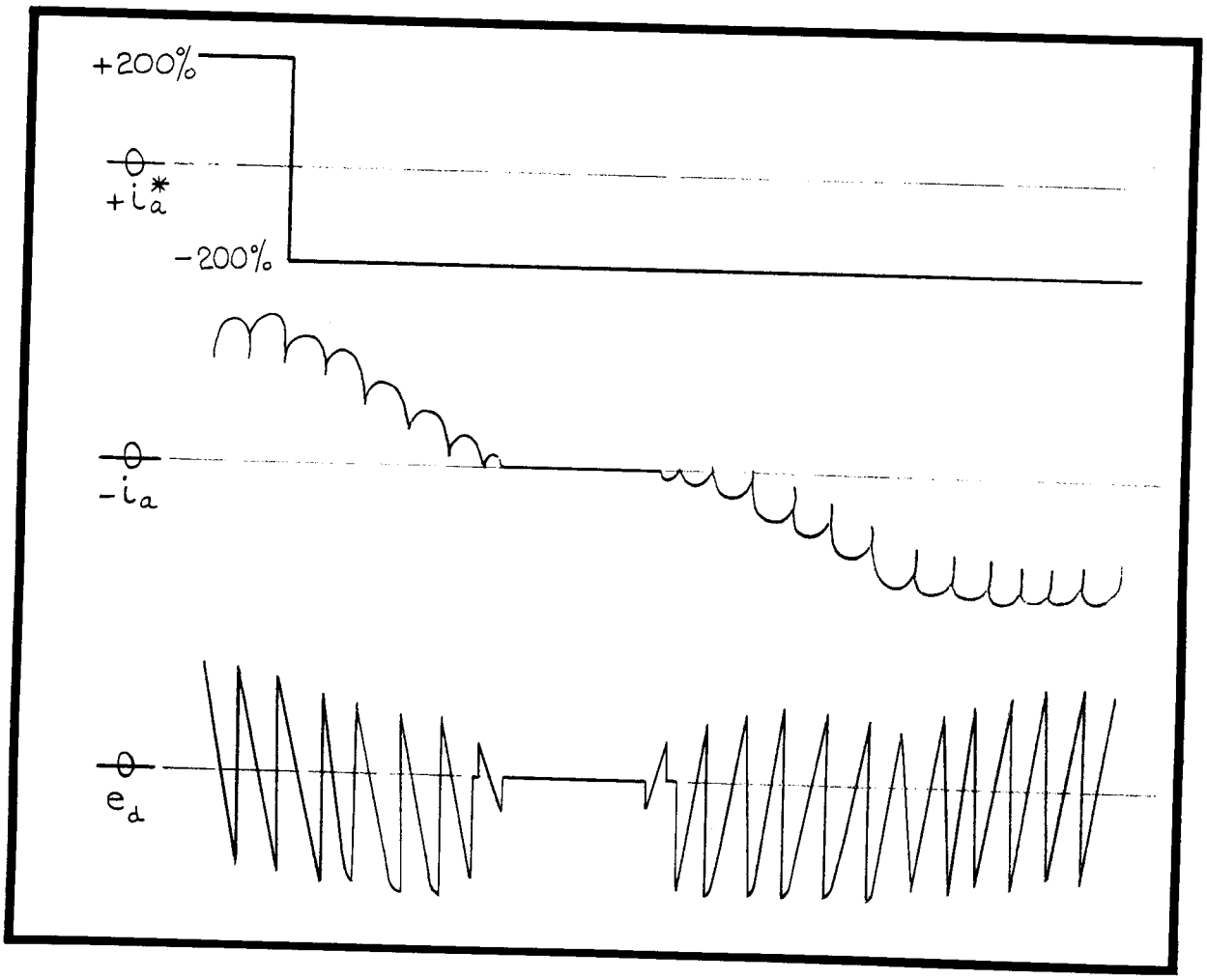

FIGURE III - 7 REVERSAL OF ARMATURE CURRENT

B. Thyristor Power Modulator (TPM)

This modulator assembly includes the thyristors connected in a three-phase, single-way double converter circuit. The schematic diagram is shown on Figure III-8. TPM's employed on drives 5 to 20 HP use power disc thyristors which are clamped between heat sinks allowing single sided cooling. Drives up to 20 HP use natural convection cooling.

The R-C networks connected from the ac lines to the DC output terminal serve to attenuate excessive rates of voltage which otherwise may lead to undesired turn on of thyristors, and to clamp the oscillations that would otherwise be produced by the commutation process. The pulse transformers provide the necessary isolation between thyristors and the proper pulse amplitude.

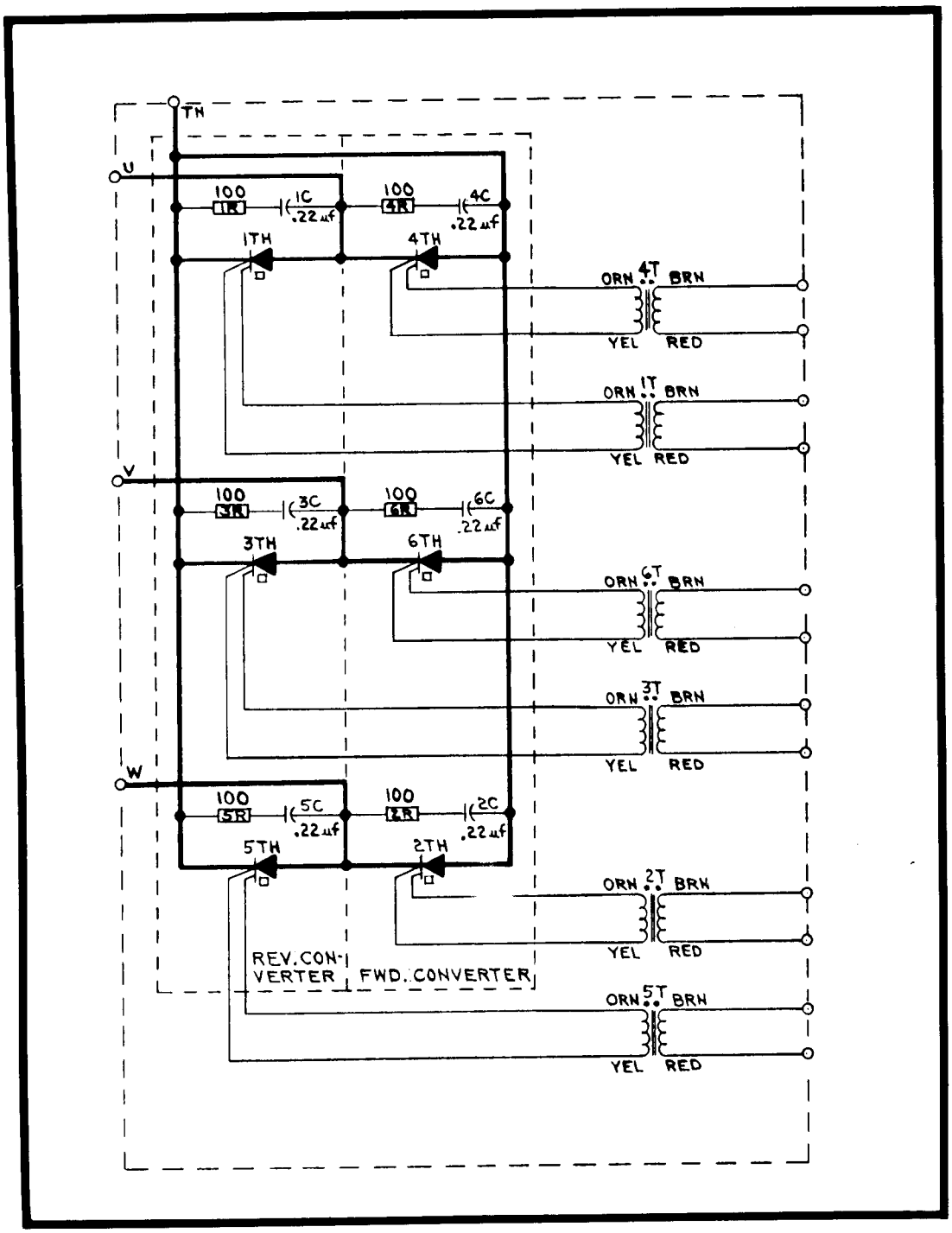

FIGURE III - 8 THYRISTOR POWER MODULATOR

NOTE: The R-C suppressors and gate pulse transformers (GPT) are mounted on printed circuit boards attached to each side of the TPM.

C. Regulator Cage

The regulator Cage contains both preselected and optional components. The sum of the preselected components will be designated as the basic regulator and comes in two types:

1. Voltage Regulator. This includes three single phase transformers connected as a three-phase transformer with a delta primary and star secondary used as both gate control transformer and dc power supply transformer, gate pulse generator board, power supply and phase detector board, static sequencer board, protection board, calibration board, and voltage and current controller (V & CC) board.

2. Speed Regulator. This includes the same equipment as the voltage regulator except a speed and current controller (S&CC) board is substituted for the V&CC board.

In both the V&CC board and S&CC board an external current limit is provided at terminal 43. This provides (with an appropriate external network which may be part of the optional equipment in the cage) a means of current limit recalibration or current control with outer voltage or speed limit.

Space is provided in the regulator cage for one optional plug in board.

Figure III - 9A, 9B, 9C and 9D shows a signal distribution diagram of C600M regulator.

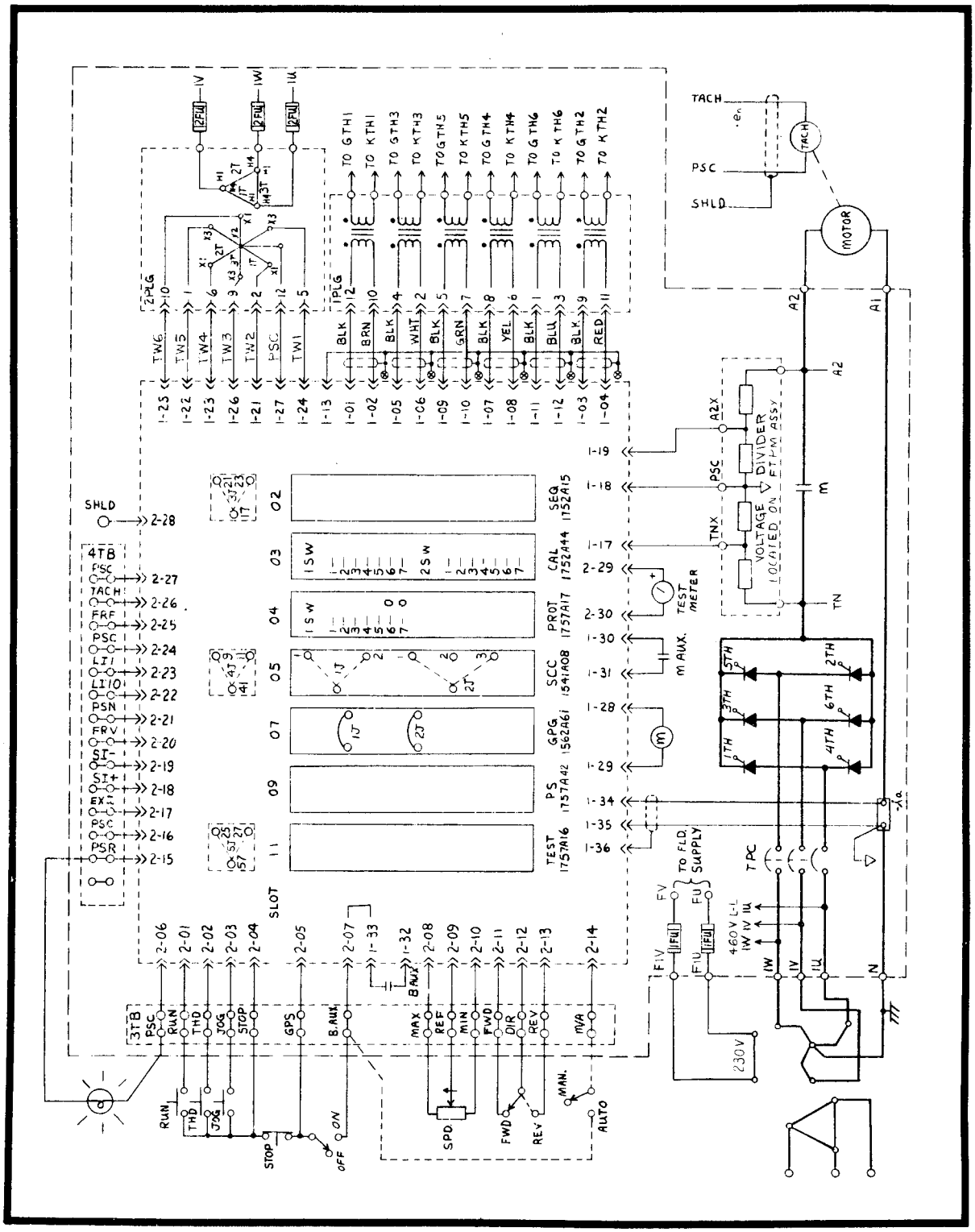

FIGURE III = 9A C600M INTERCONNECTION DIAGRAM

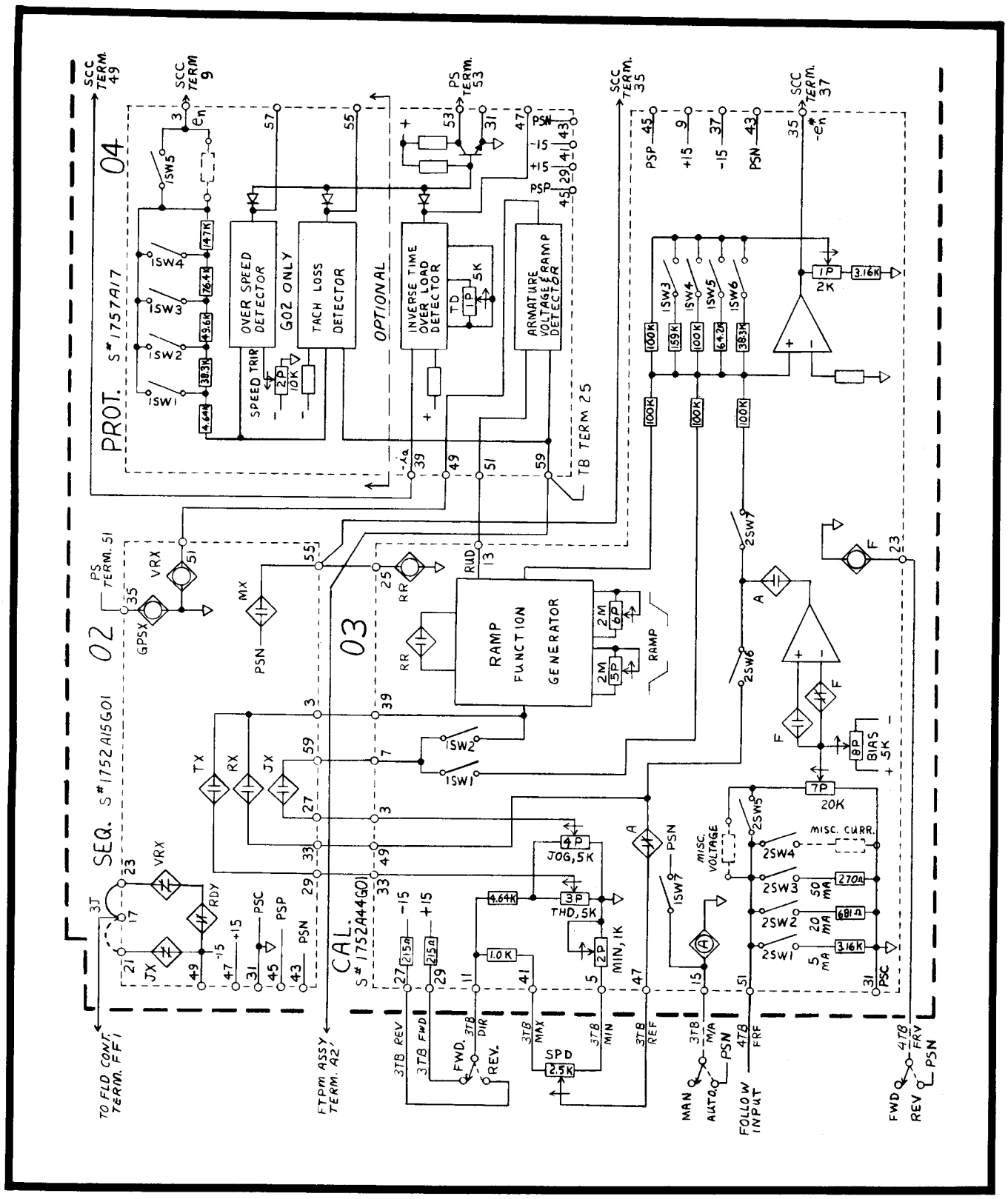

FIGURE III - 9B SPEED OR VOLTAGE REGULATOR SIGNAL DISTRIBUTION PART I

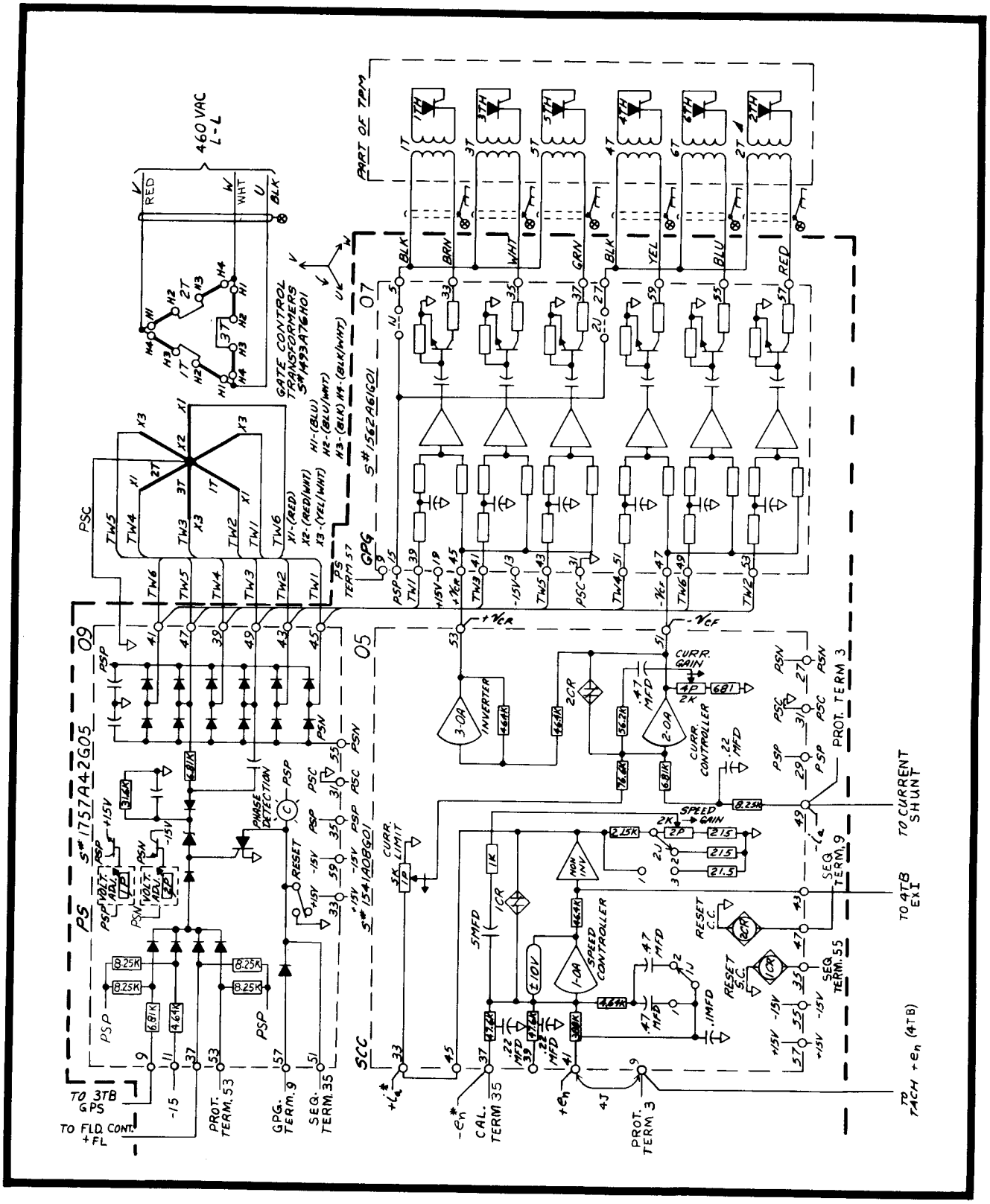

FIGURE III - 9C SPEED REGULATOR SIGNAL DISTRIBUTION PART 2

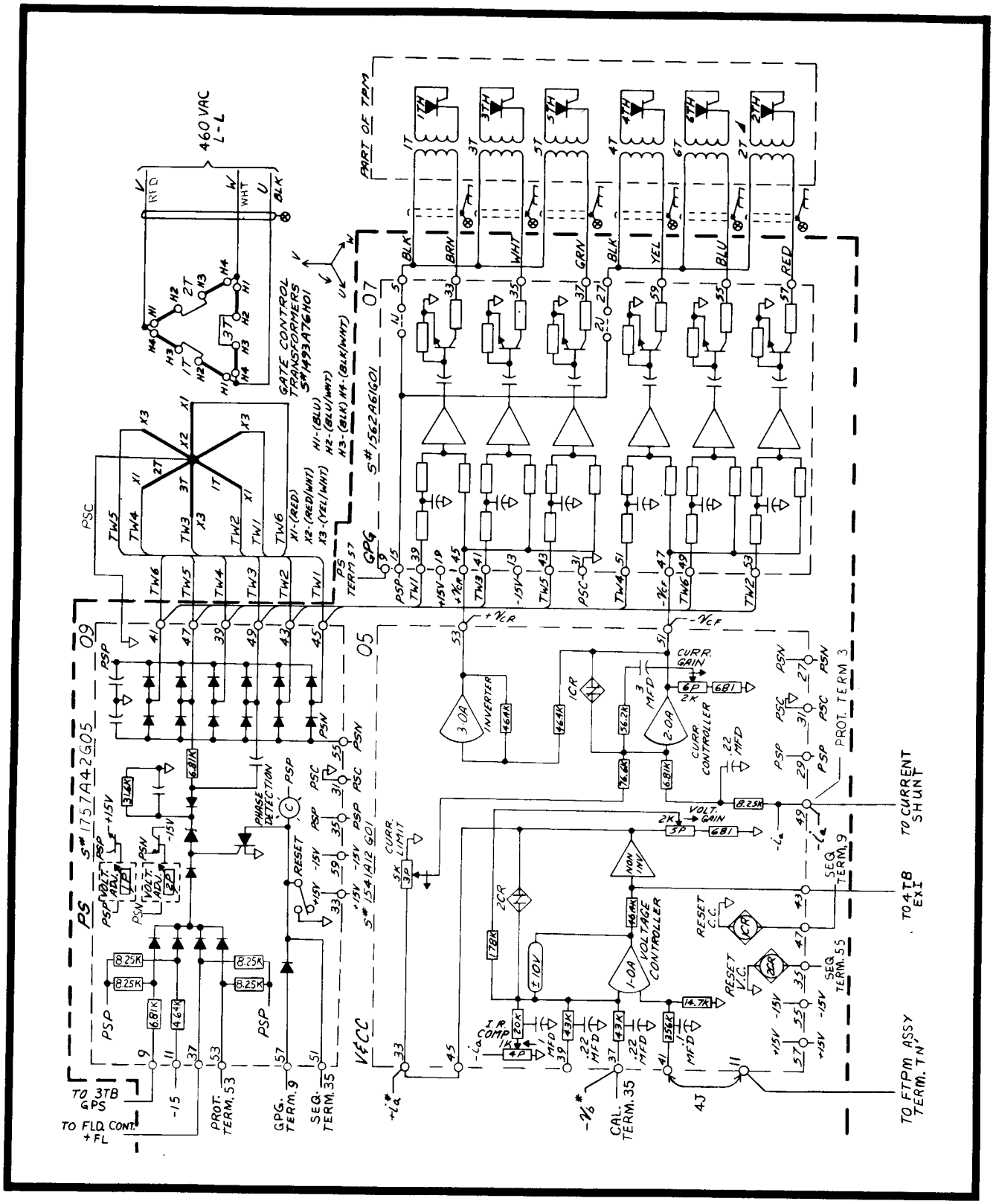

FIGURE III - 9D VOLTAGE REGULATOR SIGNAL DISTRIBUTION PART 2

1. Gate Pulse Generator (GPG)

A schematic diagram of the GPG is shown in Figure III-11. The GPG board contains six identical circuits, of which three form the forward GPG and the other three form the reverse GPG. Inputs common to all circuits are +15V, -15V, PSP, PSC, and GPS which when tied to PSC prohibits any gate pulses from being released. (The initiation of this pulse inhibit function is discussed in a later section covering the power supply and phase detector board.) Inputs to the forward GPG are its control voltage $-v_{cf}$ and three timing waves TW4, TW6, and TW2. Outputs are pulse 4, pulse 6, and pulse 2. Inputs to the reverse GPG are its control voltage $+v_{CR}$ and three timing waves TW1, TW3, TW5, and corresponding output pulses 1, 3, and 5.

A requirement of either GPG is to have three pulses spaced 120^0 apart. The timing waves generated from the six phase star secondary transformer are six identical sine waves displaced 60^0 between TW1...TW2, TW2...TW3, etc. The resulting 120^0 displacement between timing waves to the forward GPG/reverse GPG (TW4...TW6, TW6...TW2/TW1...TW3, TW3...TW5) provides the means to obtain three pulses spaced 120^0 apart over the entire phase shift range under steady state conditions. It must be remembered that the control voltages ($-v_{cf}$, $+v_{CR}$) are generated such that only one can be negative at a time and therefore only one GPG can be on at a time.

A second requirement of either GPG is to limit the dc control voltage so that the pulse cannot advance ahead of $\alpha = 10^0$. This assures that pulses cannot be phased out when demanding a large voltage in the rectification mode which would otherwise result in a sudden loss of voltage. The limit function is provided by the -15V with 17R, 84R, and 8D for the forward GPG and with 14R, 16R and 7D for the reverse GPG. With continuous current flowing this type of limit results in a fixed voltage limit (Figure III-6), and with 10% low line voltage, assures that pulses do not advance ahead of $\alpha = 10^0$. For nominal line voltage the advance limit is approximately $\alpha = 30^0$.

A linear relationship between the input dc control voltage and the output voltage of the power converter is desired ($E_{d/-v_{cf}}$ = constant), assuming continuous current is flowing in the power converter. Since the converter voltage varies as the cosine of the gating angle, the phase position of the output pulses must vary as the inverse cosine of the dc control voltage. This is accomplished by pulsing when the control voltage intersects an appropriate cosine wave. The generation of pulse 4 will be explained with reference to Figure III-10.

Pulse 4 is to be controlled during the period when line W is positive with respect to line U. Timing wave 4 leads W-U by 120^0. Resistor 45R, 46R and capacitor 10C is a 30^0 lag filter which with TW 4 generates cosine wave 4 which leads W-U by 90^0. A positive bias is added through 47R so that when $-v_{cf}$ is zero pulse 4 is biased to $\alpha = 180^0$. Current from the bias, cosine wave, and control voltage is summed at the base of transistor 16TR. When the sum of this current reaches zero, proceeding toward negative values, a pulse is initiated. Transistor 16TR turns off, 18TR turns on, capacitor 11C couples the signal and establishes the pulse width to 19TR, 19TR turns off turning 20TR on for the specified pulse width. Resistor 56R with the pulse transformer establishes the proper power level to gate thyristor 4TH.

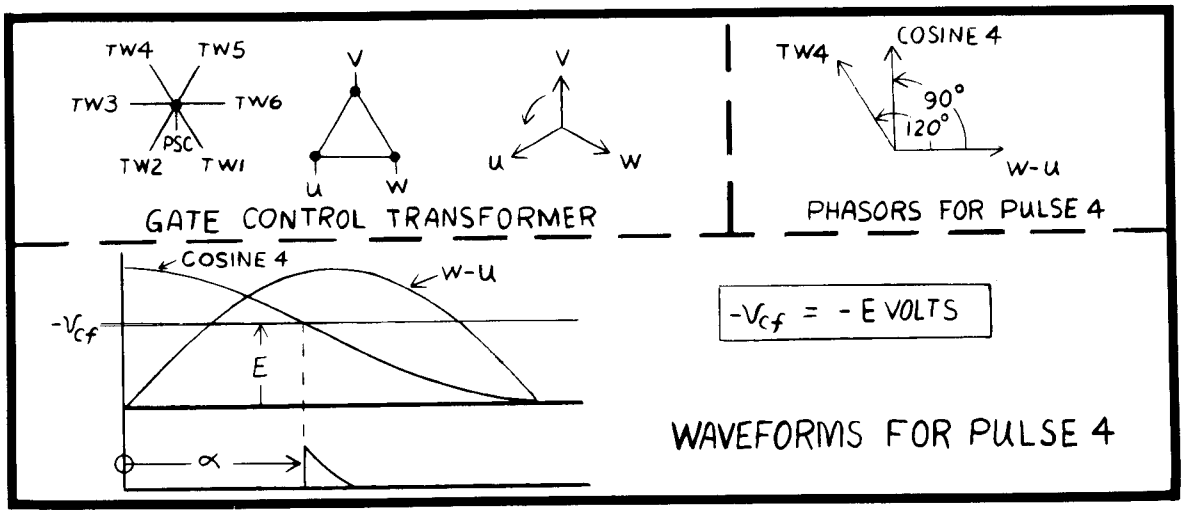

FIGURE III - 10 PHASING FOR PULSE 4

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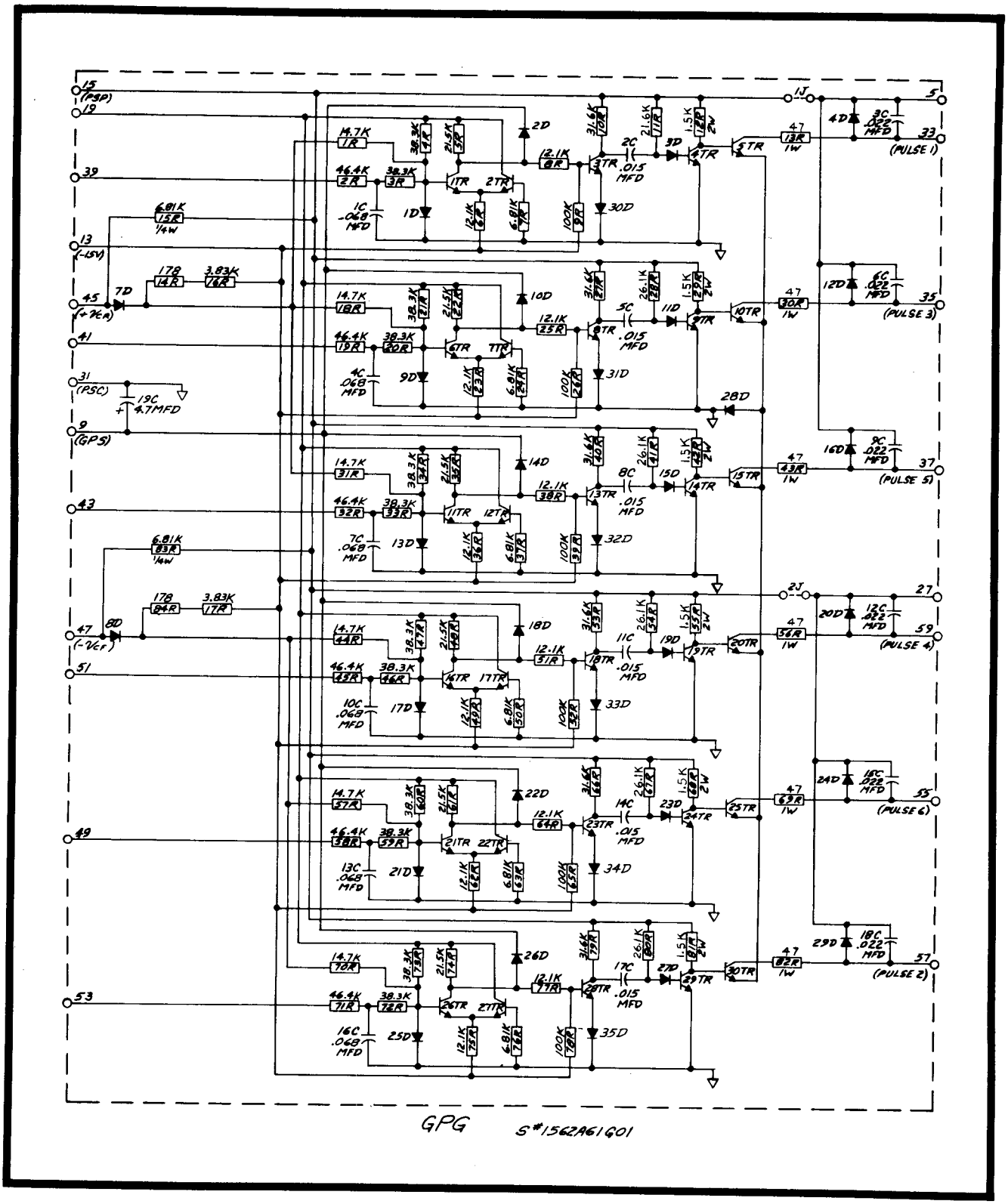

FIGURE III - II GATE PULSE GENERATOR

2. Power Supply and Phase Detector (PS & PD)

This board performs the functions of an unregulated ±24V DC power supply, a regulated ±15V dc power supply, and a phase sequence and missing phase detector. Figure III-12 is a schematic diagram of this board.

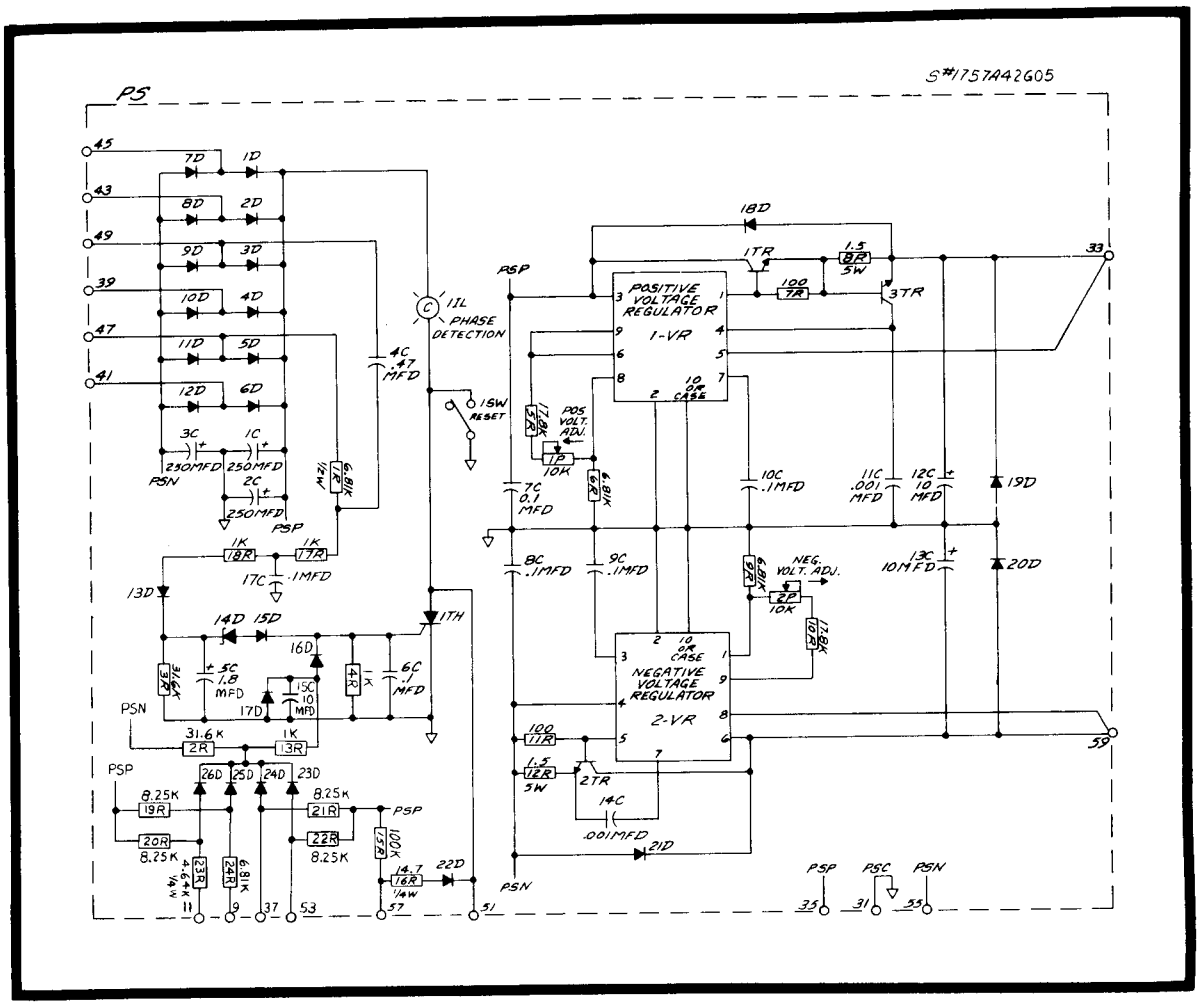

FIGURE III - 12 POWER SUPPLY & PHASE DETECTOR

The unregulated ±24V dc supply is powered by the timing waves TW1, TW2,...TW6. These sine waves are rectified near their peak values by diodes 1D through 12D and charge capacitors 1C, 2C, and 3C. The +24V dc supply is denoted as PSP and the -24V dc supply is denoted as PSN. PSP and PSN supply dc power where voltage regulation and ripple are not critical such as driver stage of the GPG, and input power to the regulated supplies.

The ±15V dc power supplies are controlled by integrated circuit voltage regulators 1-VR and 2VR. Transistors 1TR and 2TR are amplifier stages and are current limited just above 300 ma by associated circuitry. Each supply is short proof for a moderate period of time. potentiometers 1P and 2P are vernier adjustments for the supplies. The ±15V dc regulated supplies are used to supply power for integrated circuit operational amplifiers in the regulator cage and for reference voltages.

Timing waves TW3 and TW5 are applied to the R-C network 1R and 4C. With proper phase sequence (also no phases missing) the amplitude at the output of the R-C network is insufficient to breakover zener diode 14D and trigger thyristor 1TH. With improper phase sequence or missing phases the voltage out of the R-C network increases significantly and will breakovaer 14D triggering 1TH. Thyristor 1TH could also be triggered from external signals brought in at terminals 9, 11, 37 and 53. Firing of 1TH inhibits gate pulses by droping the voltage at terminal 57 to near PSC potential, resets the sequencer to the stop mode, and provides a power not ready signal at terminal PSR located on 4TB.

3. Voltage and Current Controller (V&CC)

This board consists of a voltage controller (1-0A), a current controller (2-0A), and an inverter (3-0A). Figure III-13 is a schematic diagram of this board

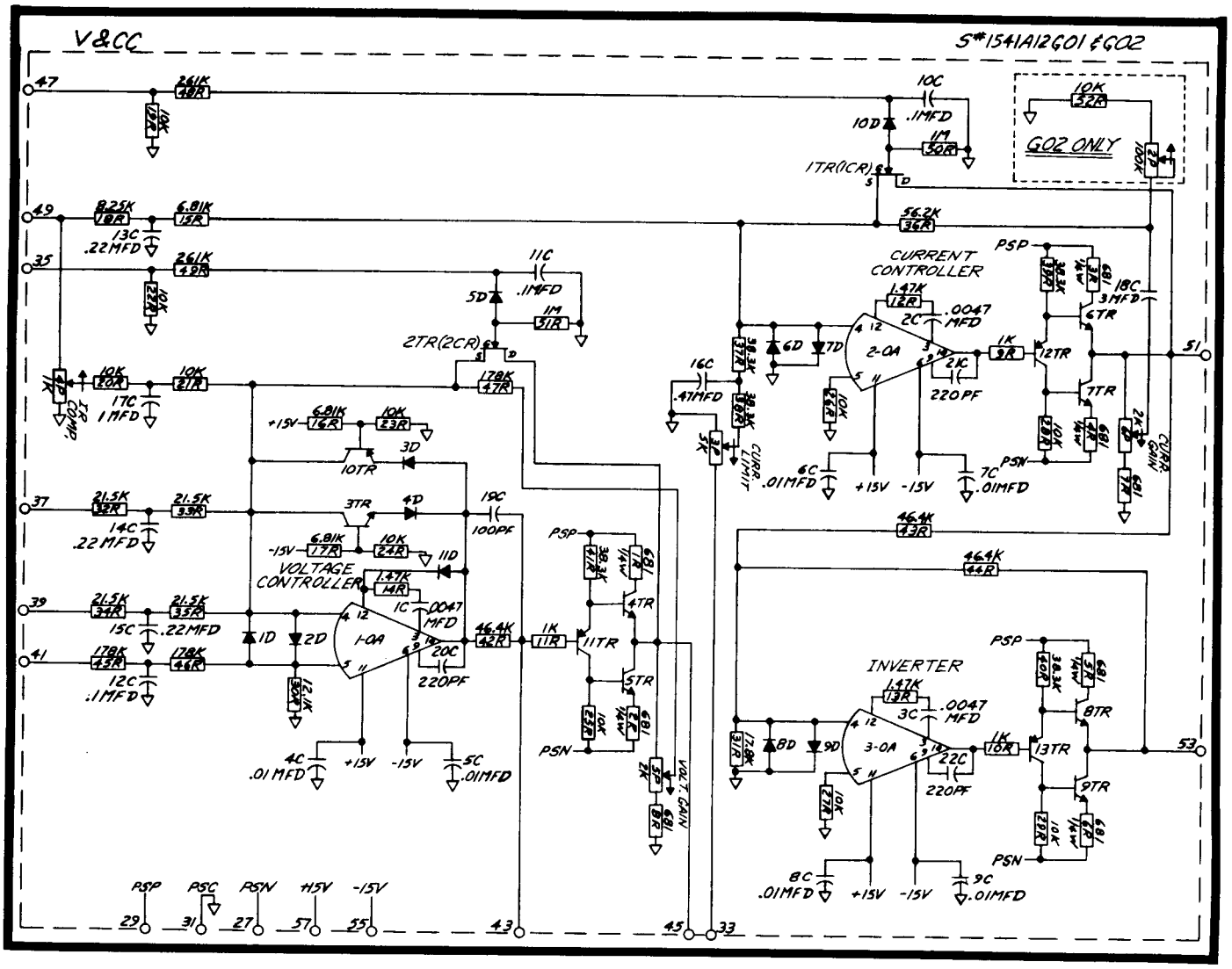

FIG. III - 13 VOLTAGE & CURRENT CONTROLLER

The current controller and inverting amplifier are used as a differential output amplifier to drive both the forward and reverse gating channels of the GPG. The current controller is a PI controller with a fixed lead of 150 ms which maintains steady state accuracy of the current loop. There is a 10 ms filter at the input of the current controller to limit the rate of change of current. Current gain, hence dynamic performance, of the current controller is adjusted by means of pot 6P. A current limit adjustment is provided by pot 3P, and a reset function is provided by FET switch 1TR to prevent amplifier drift during standby conditions (terminal 47 open).

The voltage controller is a proportional amplifier with a 15 ms filter at the voltage feedback to reduce voltage ripple. Voltage controller gain adjustment is provided by potentiometer 5P, which in conjunction with 6P (current controller gain) determines the response of the drive. When a small reference ($-v_b^*$) change is made, the drive would reach the new reference in about .1 sec provided current limit is not reached. IR compensation is provided by 4P. FET switch 2TR provides a reset function for the amplifier. The limiter (approximately ±10V) of the voltage controller provides the current limit reference to the current controller when no external current limit is used.

4. Speed and Current Controller (S&CC)

This board consists of a speed controller (1-OA), a current controller (2-OA), and an inverter (3-OA). Figure III-14 is a schematic diagram of this board.

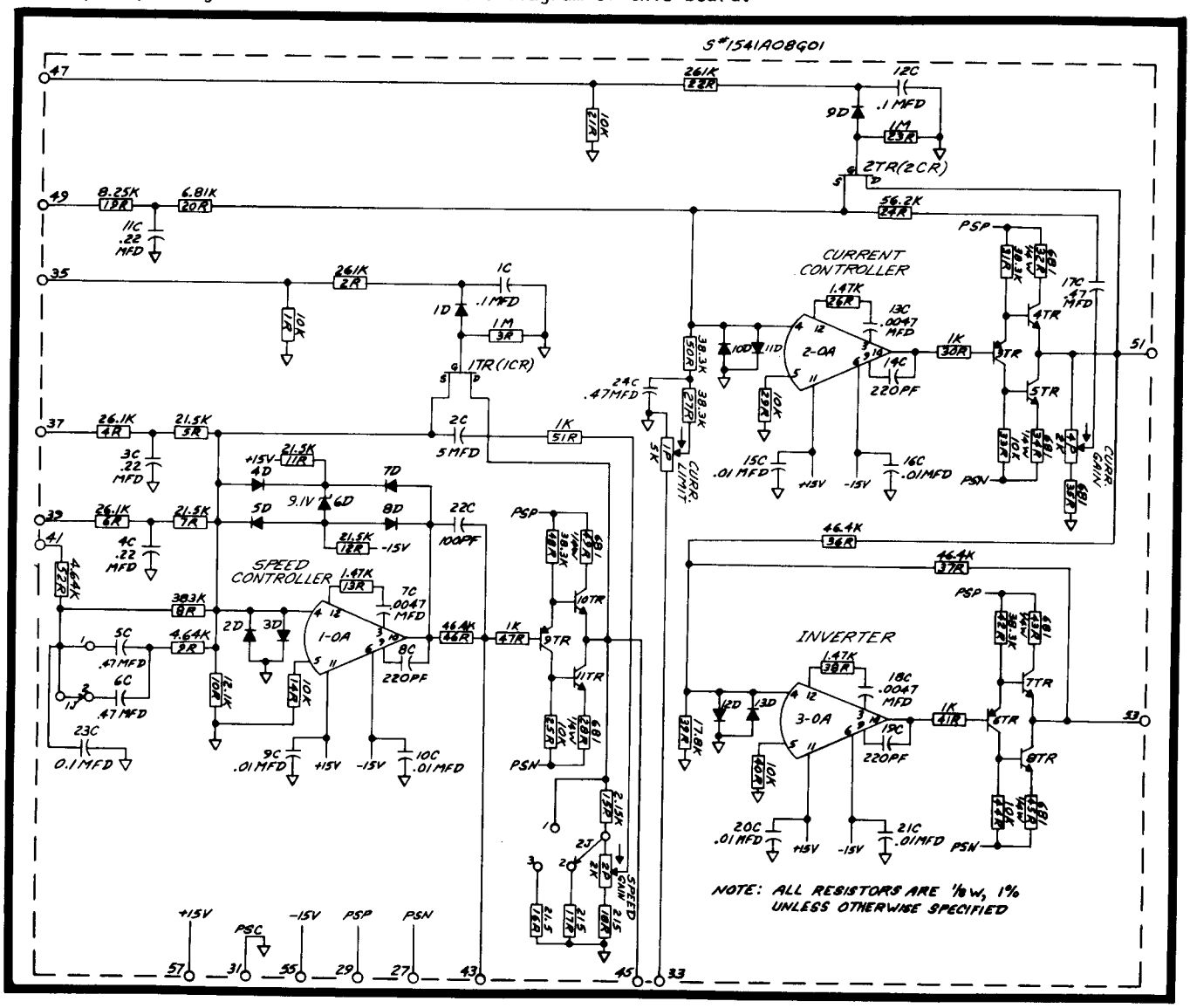

FIG. III - 14 SPEED & CURRENT CONTROLLER

The current controller and inverting amplifier are used as a differential output amplifier to drive both the forward and reverse gating channels of the GPG. The current controller is a PI controller with a fixed lead of 28 ms to compensate for the armature time delay. There is a 10 ms filter at its input to limit the rate of change of current. Current gain, hence dynamic performance, of the current controller is adjusted by potentiometer 4P. A current limit adjustment is provided by pot 1P and a reset function is provided by FET switch 1TR to prevent amplifier drift during standby conditions (terminal 47 open).

The speed controller is a type 1 controller with a small lead in the feedback to approximately cancel the lag at the input of the current controller. A lead of 190 ms or 380 ms, selected by jumper 1J, is provided in the tachometer feedback loop to compensate for the mechanical time constant of the motor. Speed controller gain is adjusted by jumper 2J and pot 2P. Through selection of jumper connection 2J and pot setting 2P, a crossover frequency of 10 rad/sec.... 50 rad/sec can be obtained. A reset function is provided by FET switch 2TR. The speed controller limiter (approximately ±10V) provides the current limit reference to the current controller when no external limit is used.

5. Calibration Board (CAL)

A schematic of the CAL board is shown in Figure III - 15. The board consists of reference potentiometers, a manual/auto mode selector, a scaling amplifier, a ramp function generator, and a follow circuit.

A speed potentiometer (2.5k) when connected to pins 5, 41, and 47 provide full speed range of adjustment, whereas thread (THD-3P) and jog (JOG-4P) adjusts from 0 to 50% speed. Minimum speed pot (2P) adjusts over a 0 to 30% range. Reversing the reference is accomplished by reversing the polarity of the 15 volts supply pin (11) through connection to either pin (29) or pin (27) by using the Forward/Reverse switch.

The "manual" reference (by speed pot) applied at terminal 47 and the "Auto" reference emminating from 5-0A output is switched by transistors 1TR and 2TR to pin 49 where it goes to the Sequencer Card. When manual or normal operation is desired, pin 15 is at zero volts; when "auto" mode is desired, pin 15 is tied to -24 volts. Switches, 2SW6 and 2SW7 allow the follow signal to be routed through or around the ramp function generator respectively. Switches 1SW1 and 1SW2 determines whether the Jog reference is to pass around or through the Ramp Function Generator, respectively.

The "Max" Speed pot 1P adjusts the speed range, in conjunction with calibration op-amp 3-0A and 1SW3 through 1SW6, as follows:

TYPE OF DRIVE	1SW SWITCHES CLOSED	MAX. SPEED ADJUSTMENT RANGE (RPM)
Speed Regulated	3, 4, 5, 6	625 - 1050
Speed Regulated	3, 4, 5	1050 - 1700
Speed Regulated	3, 4	1700 - 2700
Speed Regulated	3	2700 - 4500
Voltage Regulated	3	

NOTE: 1) Maximum speeds are based on a maximum input reference of 10 volts and a tachometer generator voltage of 20.8V/1000 RPM. Maximum speeds are decreased proportionately for a lower maximum input reference.

2) Where the maximum input reference is considerably less than 10V, switches 3, 4, 5, and 6 may be left open and will yield an adjustable speed range of 2933 to 4785 RPM with a 7.5 volt maximum input reference applied.

Other combinations of the above positions are possible, but they will result in overlapping two adjacent ranges of the above.

The signal follow circuitry is comprised of op-amps 4-0A and 5-0A and associated components. Switches 2SW1 through 2SW5 allows following of current reference (i.e., 1-5ma, 4-20ma, 10-50ma) of either polarity or a voltage reference of 0 to ±10VDC. Pot 8P allows biasing out part of the current source reference such that zero reference may be achieved when minimum input current is applied. With full current reference (i.e., 5ma, 20ma, and 50ma) 12 volts reference can be achieved with 7P fully CW. With 1SW1 through 1SW5 open and 38R specified, a miscellaneous voltage may be brought into pin 51. Reversing of the follow signal may be obtained by use of the polarity switch operable by pin 23. With pin 23 at -24 volts the signal polarity at pin 51 is non-inverted. When pin 23 is held at zero volts, the reference polarity of pin 51 is inverted.

Pot 5P adjusts the rate of ramping in the negative going direction (i.e., forward deceleration/reverse acceleration). Pot 6P adjusts rate of positive going signals at the ramp input (i.e., forward acceleration/reverse deceleration). The ramp time is adjustable from 2 to 40 seconds. Pin 25 is used to reset the Ramp. When at -24V the reset is disabled, when at zero volts the reset is enabled.

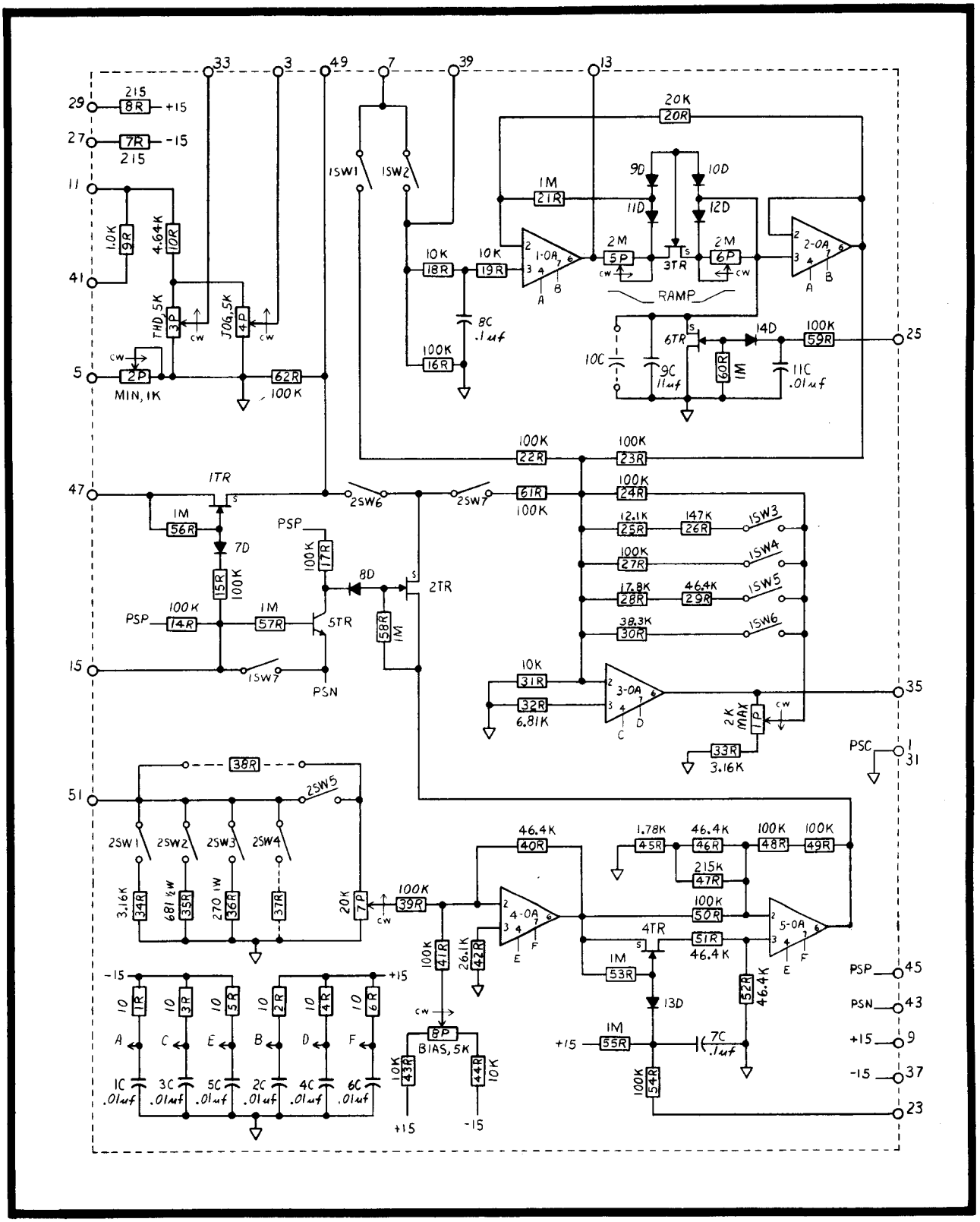

FIGURE III - 15 CALIBRATION BOARD

6. Protection Board (PROT)

A schematic of the PROT. board is shown in Figure III - 16. G01 of this board consists of a static overload circuit and a voltage sensor used for antiplugging. G02 is an option which includes the G01 circuitry plus a tach loss and overspeed detector.

Overload protection is provided by op-amps 1-OA, 2-OA, 3-OA and associated circuitry. The static overload circuitry is designed to provide protection for both Motor and TPM, an improvement over the usual overload relay. Typical points on the trip curve of the static overload circuit are: 150% at one minute, and 200% at 10 seconds, and 115% continuously. Instant tripping occurs on overloads exceeding 225% rated current. Potentiometer 1P adjusts for tolerance of components associated with the timer amplifier, 2-OA. Current feedback (0.5 volts equal to 100% rated current) is fed to pin 39. When 115% I_{dn} is exceeded (i.e., 115% X 0.5V), the bias current to 2-OA is exceeded and 2-OA integrates positively until the bias current of 3-OA is exceeded at which point the output of 3-OA, which is normally in positive saturation switches to a -0.5 volts. Whenever the outputs of either 3-OA, 4-OA or 5-OA go negative from positive saturation transistor 1TR turns off, a signal at pin 53 is fed to the Power Supply board where a GATE PULSE SUPPRESSION function is initiated.

The Voltage Sensor is an absolute value circuit which integrates the CEMF motor voltage and the first stage of the ramp function generator. Whenever the CEMF Voltage (Pin 59) is approximately 20% or more of the rated voltage feedback (75V) or the first stage of the ramp function generator (Pin 51) is greater than 7 volts either positive or negative, the output of 6-OA (Pin 49) will be -7.5V or more negative. This signal is sent to the sequence board which performs antiplugging function.

The optional Tach Loss and Overspeed Detector circuitry is comprised of 5-OA and 4-OA and their associated circuitry respectively. Op-amp 5-OA compares the difference between the tach feedback and voltage feedback signals and compares this to a fixed bias representing roughly 30% of rated bus voltage. If 30% bus voltage is exceeded and the tach signal is not present, the output of 5-OA will switch from positive to negative saturation and gate pulse suppression will be initiated as previously explained. Op-amp 4-OA compares the tach feedback voltage with an adjustable bias (2P). If the feedback exceeds the value set by the bias, gate pulse suppression is again initiated.

The tach loss and overspeed detector portion of the circuit is adjusted as follows:

If the tachometer used in the system has a gain of 20.8V/1000 RPM and if the base speed of the drive is either 500, 650, 850, 1150, or 1750 RPM, then the tachometer input may be applied directly to pin 3 and 1SW adjusted per Table 1.

TABLE 1

INPUT SELECTION TABLE

BASE SPEED OF DRIVE		1SW SWITCHES CLOSED
500 RPM	-	1SW1, 1SW5
650 RPM	-	1SW2, 1SW5
850 RPM	-	1SW3, 1SW5
1150 RPM	-	1SW4, 1SW5
1750 RPM	-	1SW5

If the tachometer used has a gain other than 20.8V/1000 RPM or if the base speed of the drive is other than 500, 650, 850, 1150 or 1750 RPM, then the tachometer input signal must be applied to terminal 3 through a miscellaneous series resistor, Rex, switch 1SW1 must be closed and all others open. The value of Rex may be calculated by the following equation:

$$Rex = \frac{V_t \text{ Base}}{80} - \frac{1}{8} \times 10^6 \text{ ohm}$$

where V_t Base is the tachometer generator voltage at base speed.

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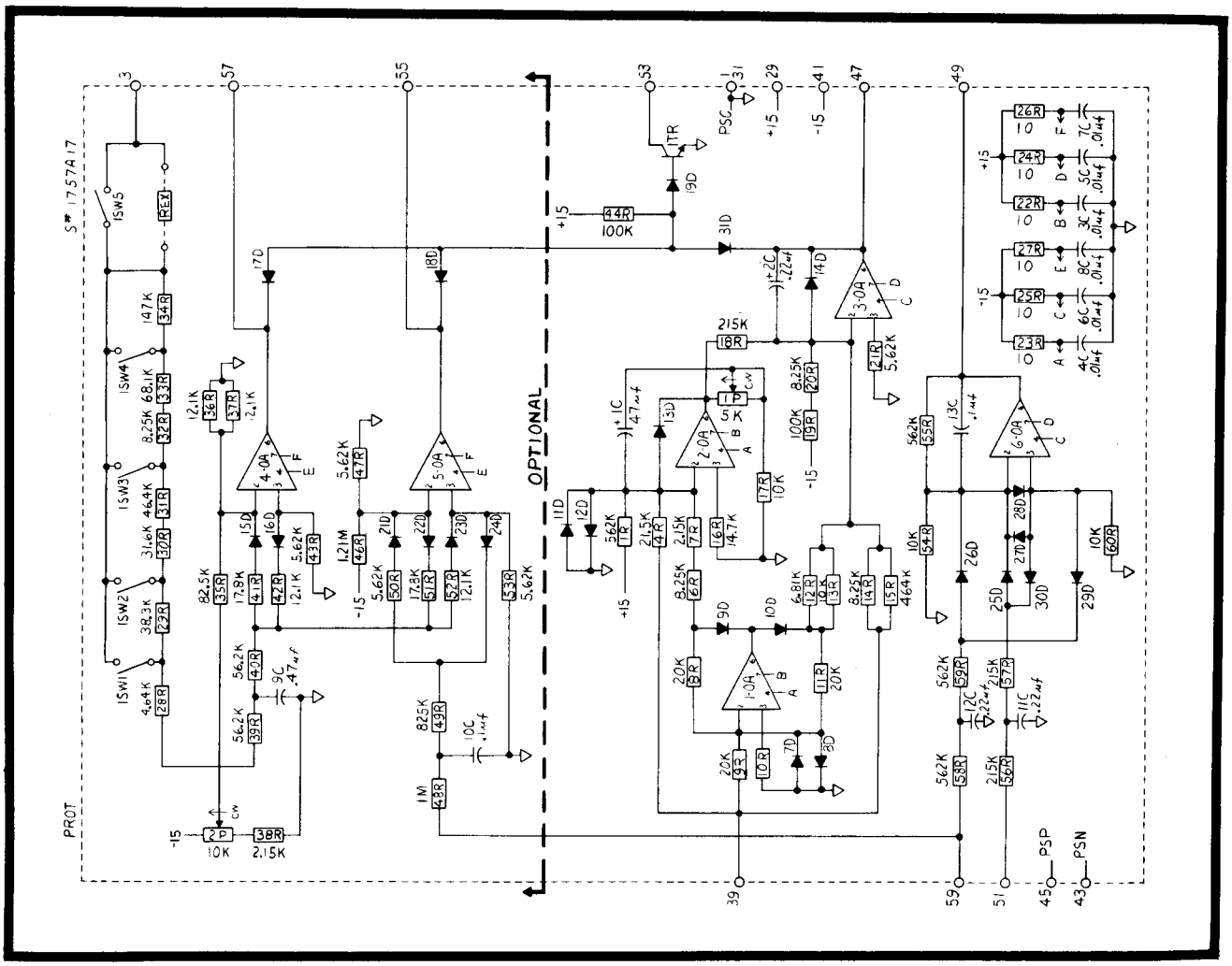

FIGURE III - 16 PROTECTION BOARD

7. Static Sequencer (SEQ.)

Figure III - 17 is a schematic diagram of this board and Figure III - 18 is a relay equivalent of the static sequencer.

The board employs high level logic NAND gates in combination with necessary semiconductors and passive components required for static sequencing. It receives signals from the operators station and permits the drive to perform the required function if the system feedback signals are correct. The sequencer controls the contactor located on the back panel and supplies internal references for the calibration board, the controller board and the field supply.

NOTE: THE DIGITAL INTEGRATED CIRCUITS OPERATE FROM PSC TO THE -15VDC REGULATED SUPPLY. Therefore a logic one is zero volts, & a logic zero is -15VDC with respect to PSC.

The sequencer is capable of supplying the options of jog and thread, as well as the standard run-stop functions. Pin 5 and associated components provide 50mA current sinking capability to energize an optional power supply ready relay. Pins 21 and 23 provide the field economy signals of JOG-only full field and RUN, THD, & JOG full field respectively. Pin 51 monitors the output of the Voltage Sensor located on the Protection board. This in combination with associated components, prevents picking up or dropping out the contactor if there is a large voltage across the motor armature or the ramp function generator is ramping. The static time delay circuit has a fixed drop out time constant of approximately one second after the voltage at pin 51 is more positive than -7.5VDC.

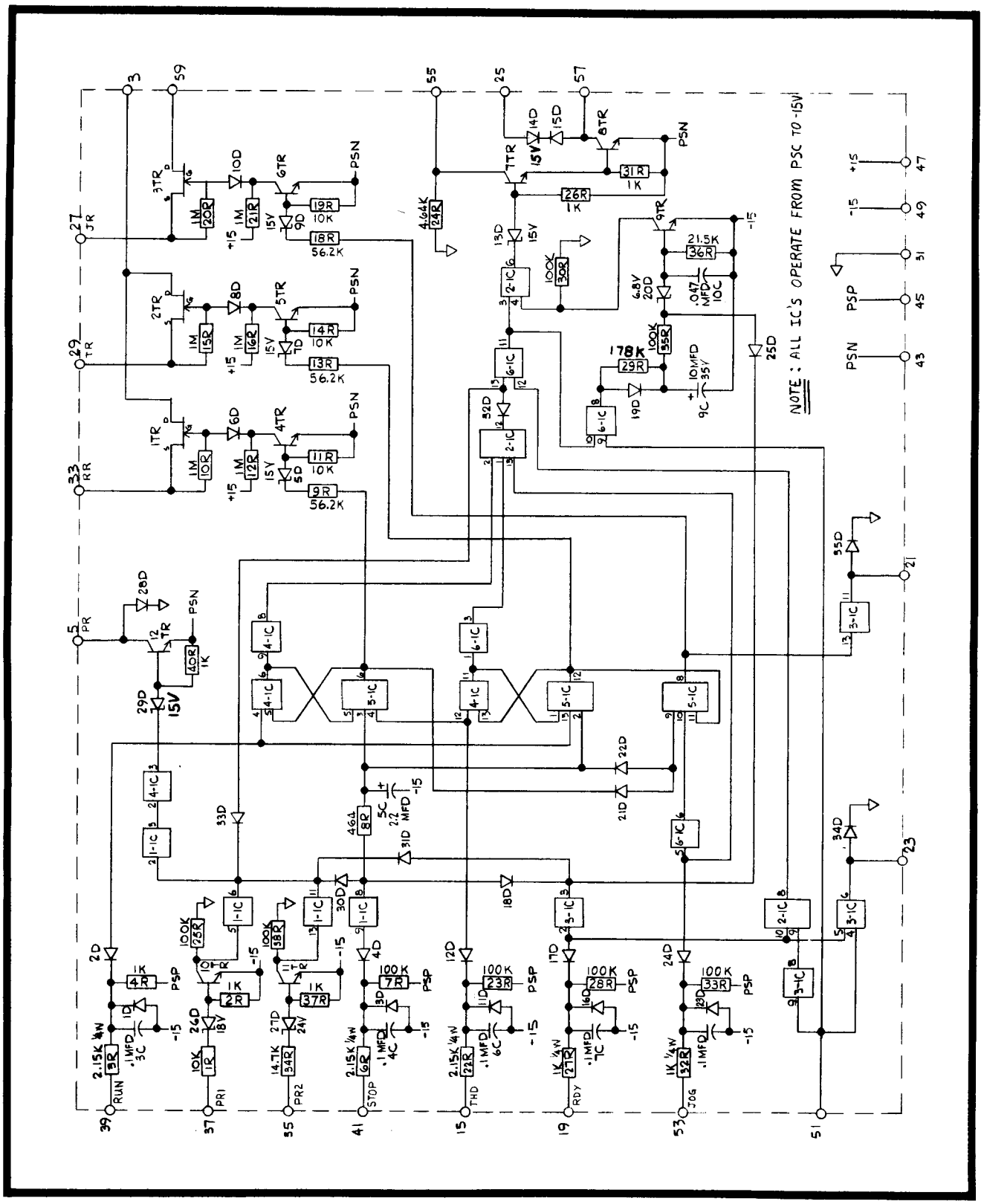

FIGURE III - 17 SEQUENCER

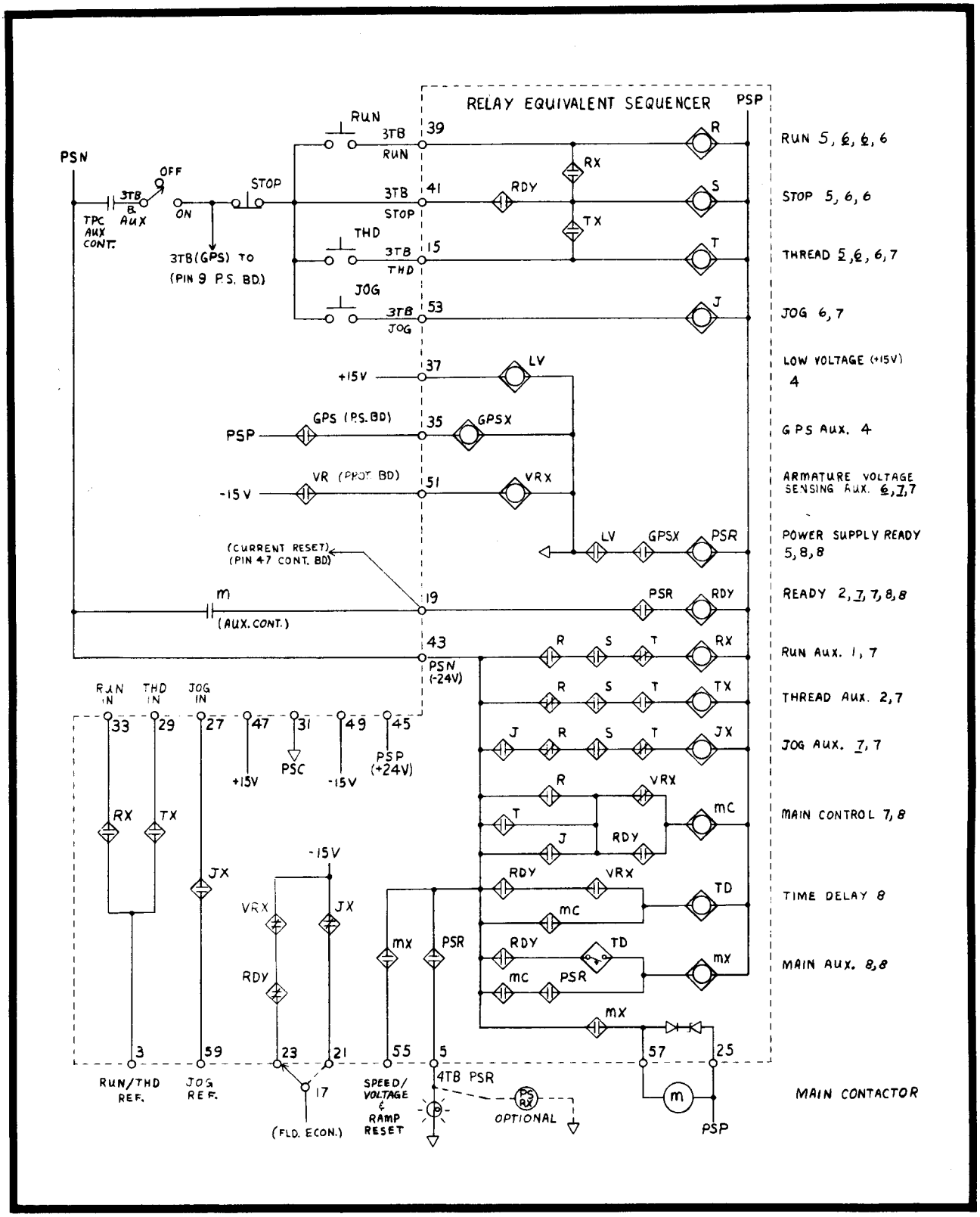

FIGURE III - 18 RELAY EQUIVALENT SEQUENCER

D. Converter Power Circuit Protection

Figure III - 19 shows a single line diagram of the C-600M TPS. The ac voltage is brought from the customer feeder to the thyristor transformer (the customer may use an ac breaker or other disconnect drive in his line). The secondary of the transformer has a single phase tertiary winding used for field excitation. This single phase line has fuses to serve as protective and disconnect functions.

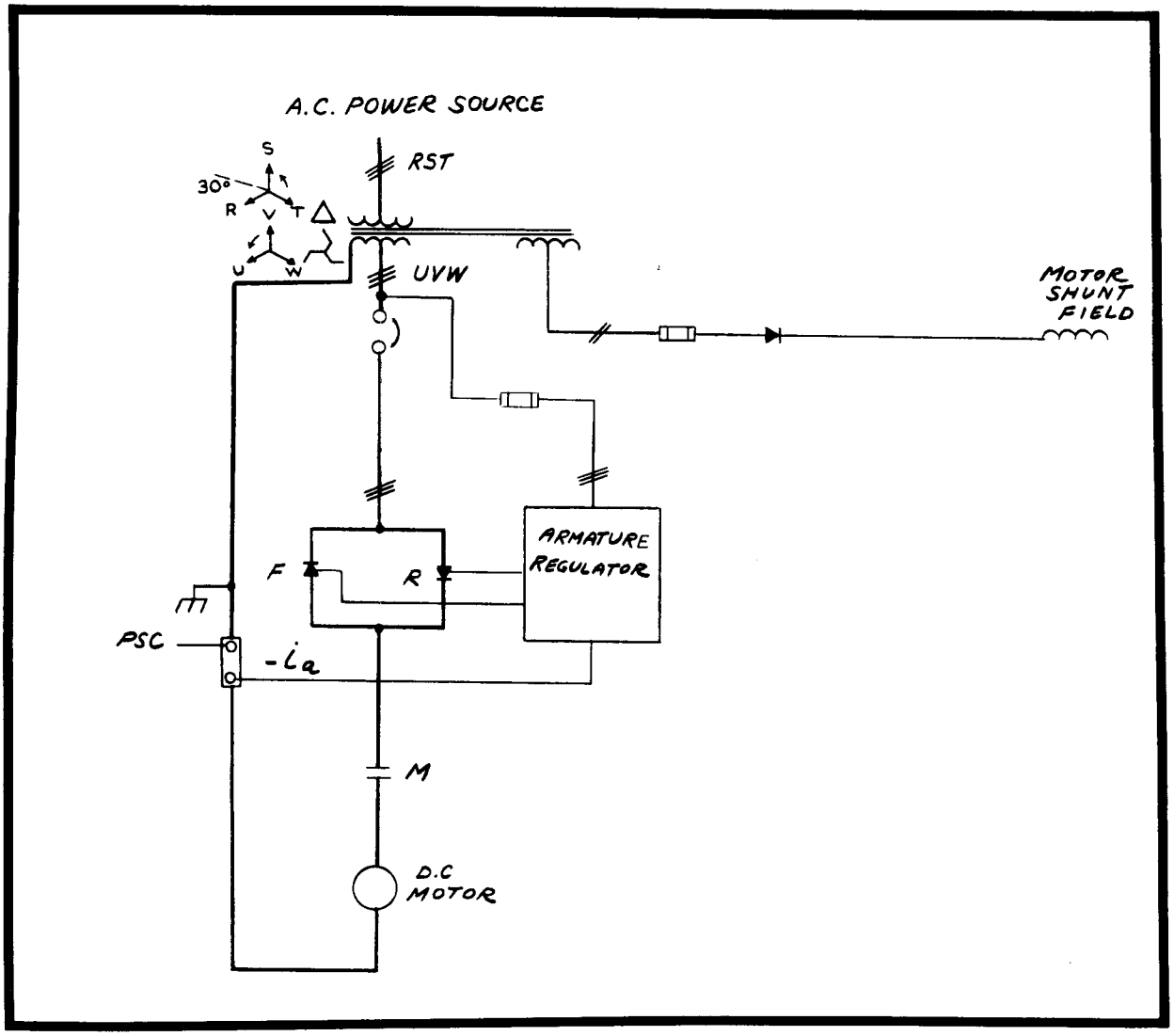

FIGURE III - 19 THYRISTOR POWER SYSTEM

There is a thyristor breaker connected from the secondary of the transformer. This molded-case MCP ac breaker has magnetic trip only, which is set above the current limit rating of the drive. This breaker is coordinated with the impedance of the transformer and serves to protect the thyristors under both ac faults and dc faults (line to line faults and motor to line faults through the neutral of the transformer) should they occur. These faults, by their nature, are of high amplitude but due to rapid magnetic tripping of the breaker are of short duration, and are held below the surge capability of the thyristors.

The shunt provides a current feedback signal to the regulator. The main sequencing device is the dc contactor between the power converter and the dc motor armature. Its main function is to de-energize the motor positively in case of an emergency or if any work is required on the driven machinery.

Normally closed limit switches or other emergency stop interlocks may be inserted in series with the off/on switch and these will drop out the contactor immediately upon initiation, as will operation of the off/on switch, the static overload circuit, the tach loss circuit, the over-speed circuit, or the field loss circuit.

Optional Accessories

The test module (S#1757A16G01) is an option that can be added to the regulator cage to aid in start up and trouble shooting. This module provides an adjustable ±10V test voltage as well as a means of sensing critical voltages. The panel meter used is a zero center meter. A ten position switch, with selected series resistors, allows for monitoring ten different voltages with the single meter.

Test module (S#1757A16G02) includes the G01 circuitry plus a load indicator driver and a tachometer signal absolute value generator. The load indicator has outputs of either 0 to 1mA or 0 to 10 VDC for an suitable external meter and is adjustable from 100% to 300% load. The tachometer signal generator is provided to drive a zero left volt meter whose full scale deflection is compatible with the maximum tachometer voltage.

F. Rating

1. AC Feeder

Standard power system incoming voltages are 230V and 460V - 60 Hz - 3 phase or 380V - 50 Hz 3 phase. Tolerance +10%, -5% on voltage, ±5% on frequency.

2. DC Voltages

Standard dc voltages are 240V for 5 HP...20 HP. These thyristor power systems are able to produce the rated dc voltage at 200% current with 95% line voltage.

3. DC Current

The continuous dc current rating of a TPS depends on several factors such as Thyristor transformer, TPM size, ambient temperature, elevation.

Standard ambient temperature range: 0 to 40°C.

Standard elevation limit: 3300 feet above sea level.

TPS continuous current ratings are at rated current for each horsepower at Standard voltage.

Standard transient current rating is 150% for 1 minute.

The thermal overload is set to protect the motor based on 115% of motor full load current.

4. Regulation

For load changes to rated current and line regulation within that specified:

Voltage Regulator	2%
Speed Regulator	0.25% with standard tach

IV. AUXILIARY FIELD EXCITER

Constant potential and variable voltage field exciters can be added to feed the fields of the dc machines which have their armatures powered by the main C-600M power converter.

A. Adjustable Voltage Field Exciter

The auxiliary field exciter consists of a single phase thyristor power module (TPM), a field controller board, and a CEMF sensor board. It is mounted to the armature TPM assembly.

This system is used for field weakening applications in conjunction with a speed regulated armature supply. The field current is held to rated current below the base speed and then decreases when the armature voltage tries to exceed its rated (crossover) voltage for speeds greater than base speed.

1. Field TPM

The field TPM is a single phase full-wave semiconverter with freewheeling diode. The semiconductors are protected by a R-C network and a surge suppressor. It is supplied 230V ac power from the single phase tertiary winding of the thyristor transformer. The TPM is rated 180V dc maximum and 6 amperes.

2. Field Controller Board

The C600M field supply is a PI current controller with CEMF crossover. The current feedback signal ($-i_{f1}$) is obtained from a sensing resistor in the field circuit. The sensing resistor is selected such that $-i_{f1}$ is .75V to 2.5V at rated field current. This signal is amplified by operational amplifier 3-OA and associated components. Potentiometer 1P is used to adjust the gain of 3-OA such that its output ($-i_f$) equals 2.0V for rated field current.

The field loss indication is provided by operational amplifier 2-OA and associated components which compare the $-i_f$ signal to an adjustable reference obtained from the wiper arm of 2P. Circuit operation is such that transistor 4TR is turned off when the field current drops below the desired level. This initiates a gate pulse suppression in the armature regulator.

Operational amplifier 1-OA provides the voltage reference for the gate pulse generator. It does this by comparing the current or voltage feedback signals (the output of 3-OA or the output of the CEMF sensor respectively), with the internal command reference originating from either 5TR or the wiper arm of 3P. Potentiometer 3P provides a means of adjusting the field strength during standby operation. For full field operation (FF1 = 0 VDC) 5TR is turned on. Thus 5TR and the associated voltage divider provide the full field reference.

The gate pulse generator provides gate pulses to the TPM. The phase angle at which the gate pulses occur is determined by the feedback signals. The control power supply for the field exciter is contained on the field controller board in order to maintain proper field control in the event of an armature regulator failure.

ADJUSTMENTS	POTENTIOMETERS	RANGE
Max. Field Current	1P	Adjust for rated current
Field Loss	2P	0 -45% of rated current
Standby Field	3P	0 -50% of rated current

3. Bus Voltage/CEMF Sensor Board

The bus voltage/CEMF sensor is a differential amplifier. Therefore the output of the sensor is a DC signal proportional to the armature voltage. An absolute value circuit is required to provide the same polarity output regardless of the input polarity. The output of the sensor is approximately 2 volts at rated armature voltage.

The sensor board is piggy-back mounted over the field controller board. The control power supplies originate on the field controller, and are connected by means of jumpers at stab terminals PSP, PSC, and PSN. The input (armature voltagge) is connected to screw terminals on the voltage sensor, while the input (-CEMF 1) is a stab terminal connected to stab terminal-i_{f2} on the controller board.

Two types of sensors are available.

a) The standard voltage sensor is merely a bus voltage sensor which has no adjustments. Component values are pre-selected to provide crossover at 220 to 240 volts.

b) The optional CEMF sensor is used for special applications. It provides adjustment of the crossover voltage (1P) and IR Compensation adjustment (2P). The IR Compensation is usually not connected and therefore not used.

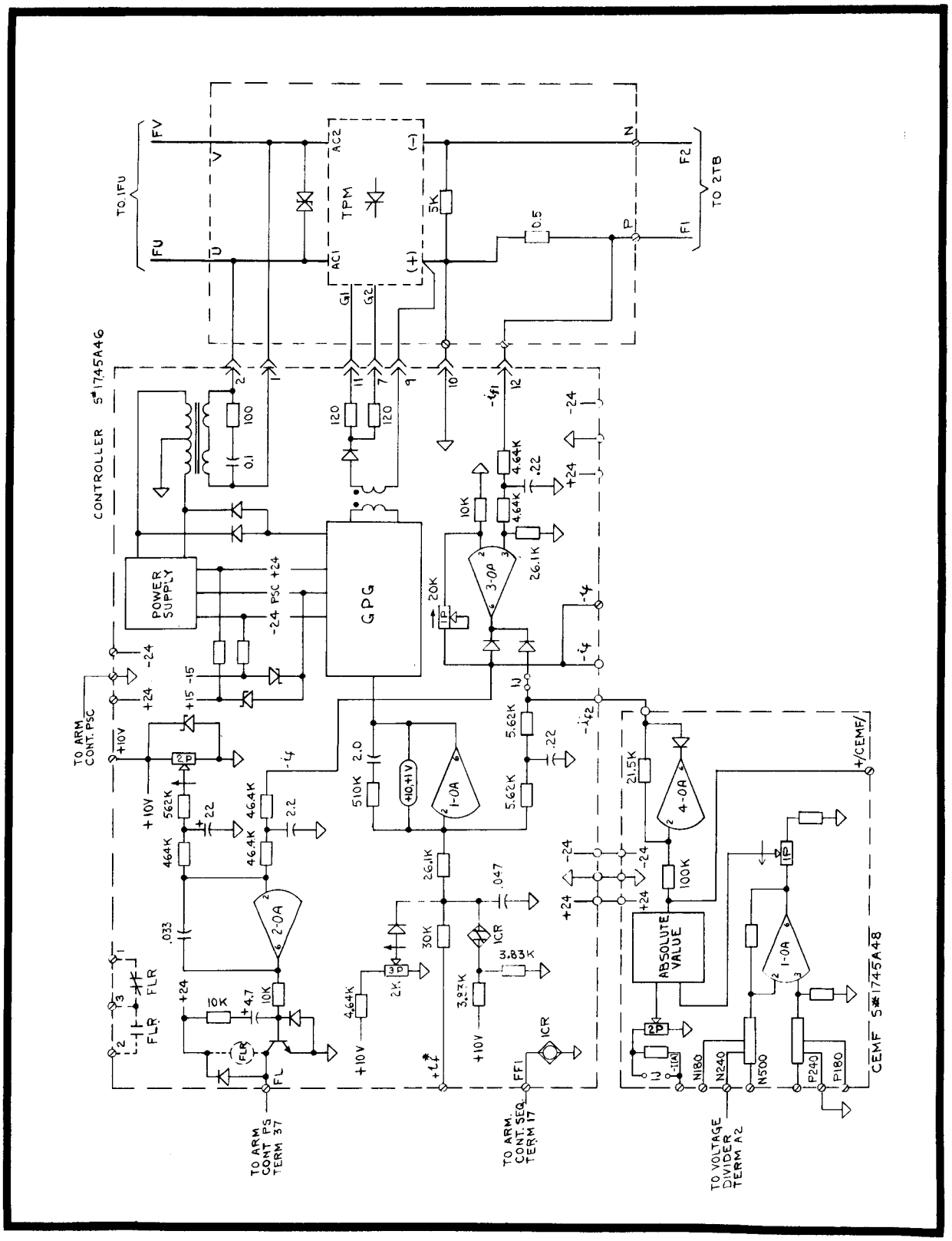

FIGURE III - 20 REGULATED FIELD SUPPLY WITH CEMF CROSSOVER

"22-1000 3Ø REGENERATIVE DRIVE (C600M)"

INDEX

I. INTRODUCTION

C-600M thyristor power systems (TPS) provide a line of controlled-voltage drives for armature excitation of dc machines from 5 HP to 20 HP. The rated armature voltage is 240 volts dc. The TPS consists of a panel and a three phase zig-zag isolation transformer with the neutral of the transformer secondary grounded.

The C-600M panels feature front accessibility, high package density, and a minimum number of adjustments. They include the thyristor power modulator (TPM), regulator cage (gate control, ±24V unregulated supply and ±15V regulated supply, armature controller, static sequencer, calibration board, protection board, optional test kit board, and one slot for an optional board to be used for additional calibration, detectors, etc.,), current shunt, thyristor breaker, and other elements (control transformer, contactor, fuse blocks and customer terminal blocks).

A constant potential or adjustable voltage exciter of 6A rating can be added to the panel. They are used to excite the field of the dc machine whose armature is powered by the main converter.

C-600M TPS are wall mounted open panels with the thyristor transformer separately mounted. In more complex systems the C600M panel may not contain the reference processing and director functions, but they may be contained on separate panels.

II. SCOPE OF APPLICATIONS

Phase-controlled thyristor converter circuits can be classified into three groups. In the semiconverter configuration, only part of the rectifying legs are thyristors; whereas, others are diodes. This yields a power system for one-quadrant operation, which means that neither output voltage nor current is reversible.

In the single-converter configuration, all legs are thyristors. The output voltage is reversible, but not the output current, resulting in two-quadrant operation.

Connecting two single converters back to back, yields a power system with four-quadrant capability providing current and voltage of both polarities. This configuration is named double converter.

C-600M thyristor power systems use double converters of the three-phase, single-way circuit configuration. The forward and reverse converters have the same rating. As three legs are employed, three pulses per cycle are produced in the dc output. Since the ripple content in the armature current contirbutes to motor heating, the motor has to be designed for use in three pulse thyristor drives.

C-600M TPS are designed primarily to provide power for armatures of dc motors where regeneration is required. Where regeneration is not required a 22-1000 semiconverter would probably be used.

The TPS includes the regulator to perform the function of voltage control with current limit, speed control with current limit, or current control with either outer voltage or speed limit. While the converter has the same capacity in forward and reverse direction, the regulator can be programmed to have different instead of equal forward and reverse current limit settings. The command system may be part of the TPS, as is the case in standard applications, or part of a central director in special applications.

Specifications and Ratings are covered in a later section of this I.L.

III. THYRISTOR POWER CONVERTER

A. Phase-Controlled Converter Principles

A thyristor power converter is an apparatus which by means of phase-controlled gating of thyristors (or other controlled rectifier cells) converts an ac supply line voltage into an adjustable dc voltage; this process is known as rectifying. Inversely, dc voltage can be converted back into the ac line voltage; this mode of operation is called inverting. A converter which only can perform one of these functions is called a rectifier or an inverter, respectively.

Once a thyristor is turned on, it can only be turned off by reducing the anode current to a very small value. In the phase-controlled converter, the ac line voltage performs the function to end the conduction period by commutating the anode voltage.

Many converter configurations have been developed. The three-phase, single-way double converter is the type used in C-600M. Figure III-1 shows the elementary schematic for the forward converter. The transformer has a delta primary and zig-zag secondary with the neutral grounded. The zig-zag secondary is necessary to prevent the transformer core from saturating (a situation which could occur if a wye secondary were used and unequal currents should flow in the three thyristor legs). The purpose of the transformer is to adjust the line voltage to the proper level, to provide isolation, to establish a neutral for a current return path, and to introduce inductance into the converter current path. This inductance is required to control the rates of currents during commutation and faults as will be seen later. The load circuit consisting of a counter emf e_a, resistance R_d, and inductance L_d is connected between the dc output of the converter and the neutral of the transformer.

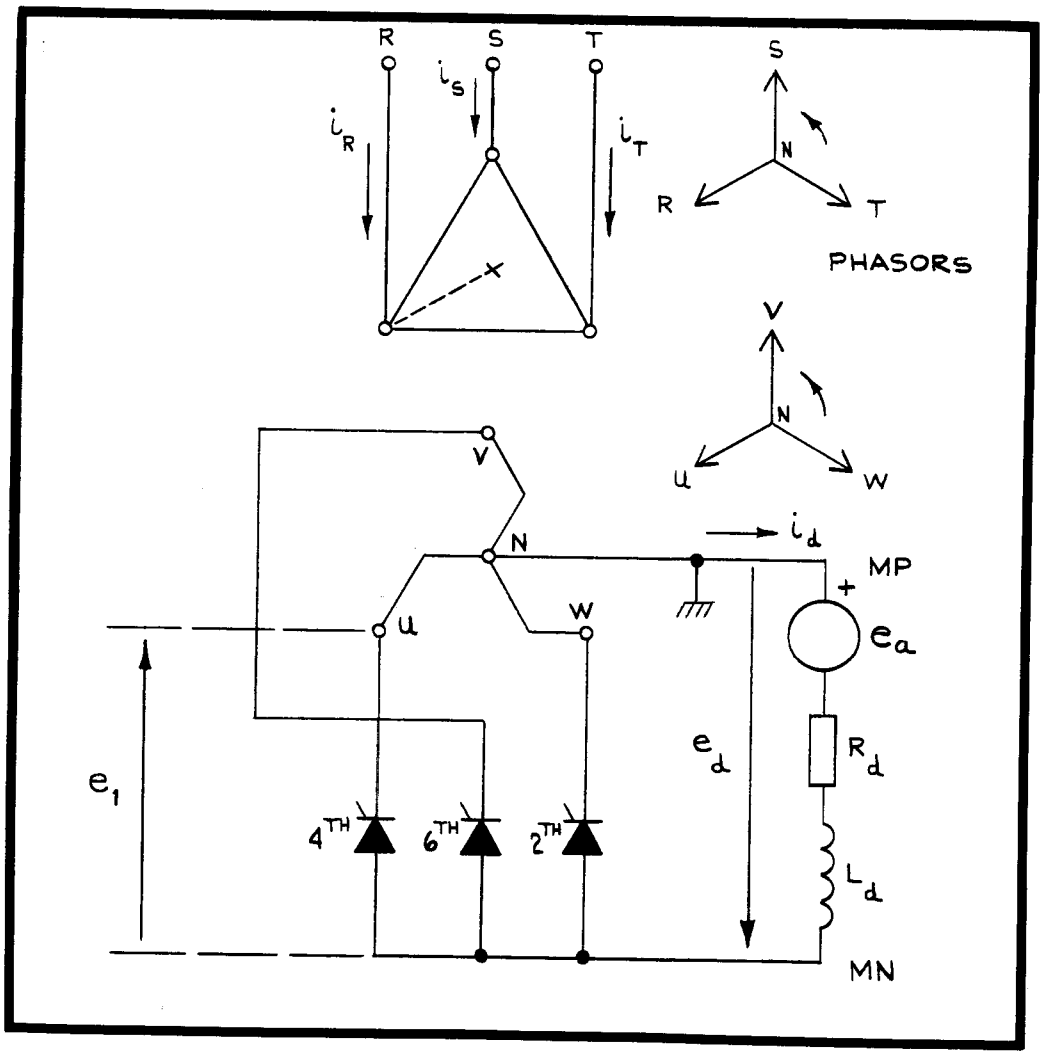

FIGURE III - 1 THREE-PHASE SINGLE-WAY CIRCUIT

The significant current paths and waveforms can now be developed (Figure III-2). The uppermost traces show the secondary phase voltages measured from the neutral to the phase. Initially, all thyristors are assumed to be in the blocking state. At 60° after N - U voltage just exceeds N - W a pulse is applied to thyristor No. 4. Current flows from the neutral (MP) through the load to MN through 4TH to U. However, 120° later a pulse is applied to 6TH. Since the voltage N-V is larger than N-U at this instant current will commutate from 4TH to 6TH. Again 120° later a pulse is applied to 2TH and a similar commutation will take place. Assuming that the load is highly inductive, the dc current will reach a steady value after a number of cycles, and each thyristor will then conduct a 120° wide current block each cycle. The respective waveforms of the thyristor anode-cathode voltages can now be developed. Figure III-2 illustrates this for a gating angle of $\alpha = 60^{\circ}$. Note that α is measured from the point where the anode-cathode voltage of the respective cell swings positive. Hence for $\alpha = 0$ the thyristors do not have to absorb any positive voltage anymore and are then comparable to single diodes. It is apparent from the waveshapes of the output voltage that its average value E_d is a function of the gating angle. It reaches a maximum at $\alpha = 0$, is zero for $\alpha = 90^{\circ}$ and assumes negative values back to $\alpha = 180^{\circ}$. This transfer curve can be obtained by integrating the waveforms. The result is

$$E_d = E_{do} \cos\alpha$$

where the saturated output voltage is

$$E_{do} = \frac{3}{\pi\sqrt{2}} E_u$$

where E_u . . . line to line rms ac voltage.

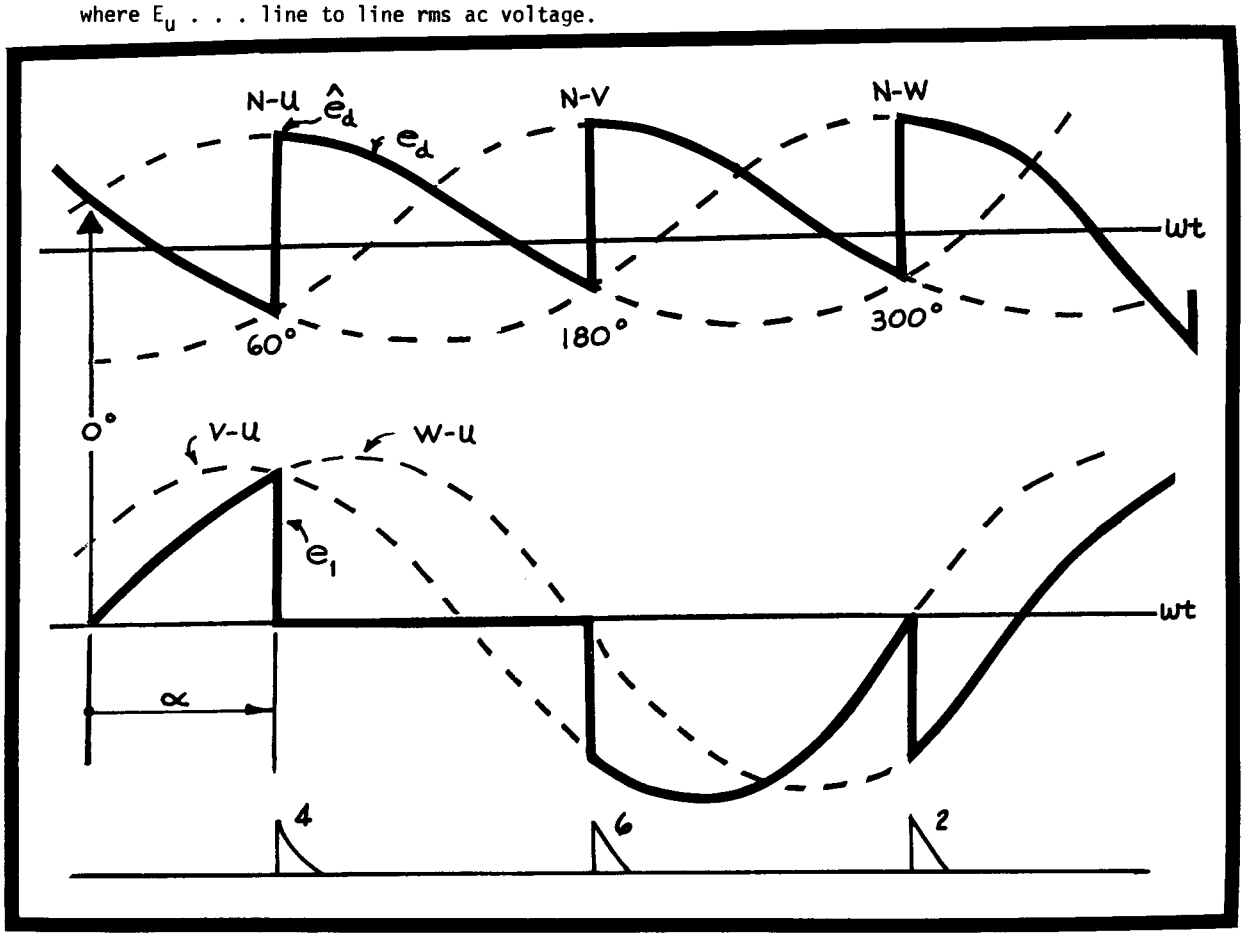

FIGURE III-2
WAVEFORMS OF THYRISTOR CONVERTER AT $\alpha = 60^{\circ}$

Since the load current cannot reverse, the average power flow will change its sign with the voltage. Rectifier operation ($\alpha < 90^0$) renders motoring in the load circuit whereas inverter operation ($\alpha > 90^0$) requires the load to be generative. Figure III-3 illustrates the range of operation on a time basis. In the beginning, the converter is operated in its rectifying mode with $\alpha = 30^0$. Then α is steadily increased into the inverter mode of operation. The lower trace shows the voltage across one of the thyristor legs.

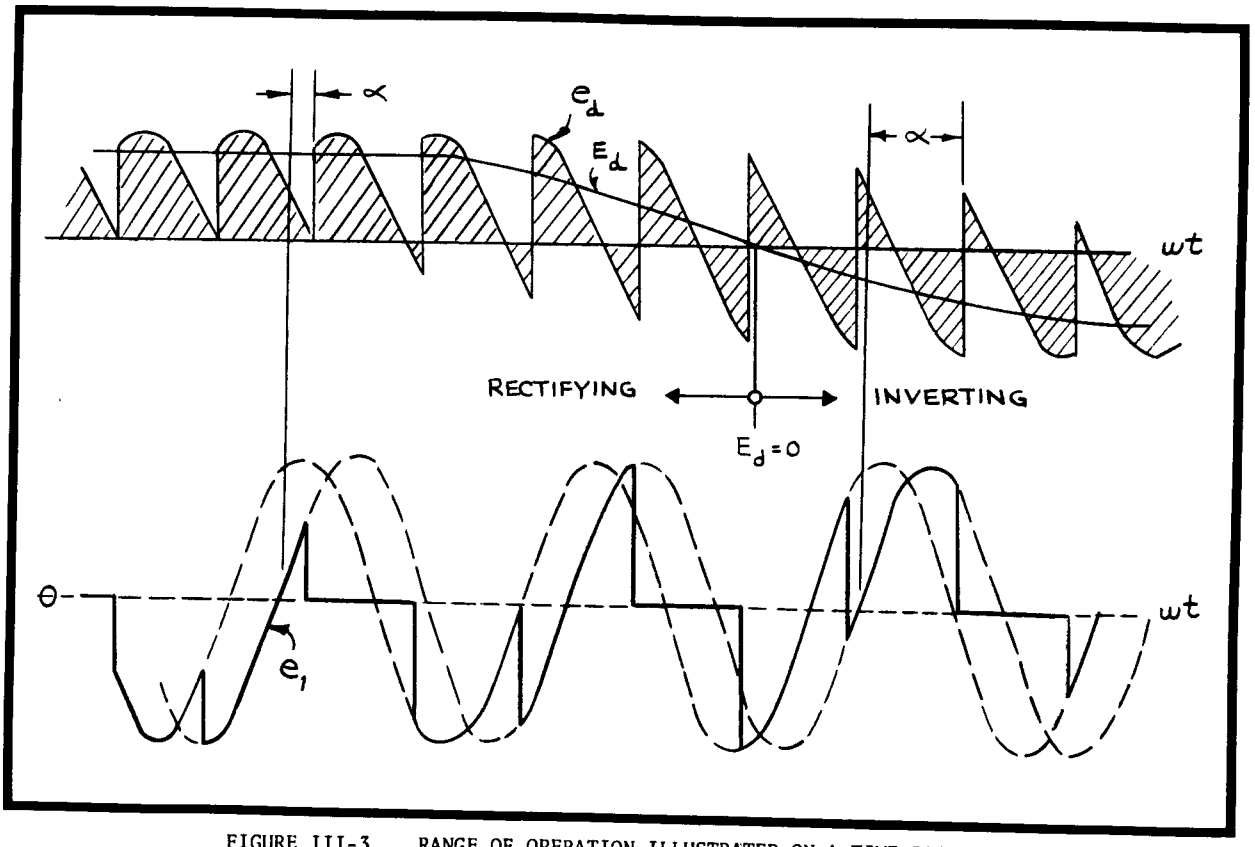

FIGURE III-3 RANGE OF OPERATION ILLUSTRATED ON A TIME BASIS

ON THE LEFT, $\alpha = 30^0$, RECTIFYING MODE. α THEN INCREASES TO INVERTER MODE

Up to this point, the reactances offered by the transformer and the power line have been neglected. This so-called commutating reactance, however, is significant. Instead of instantaneously commutating the load current from one leg to another leg (upon gating of the latter), the current rate is limited and shaped by it. This means that both these legs conduct simultaneously for a period of time, shorting out effectively the ac source. This produces notches in the sinewave measured on points U-V-W, which, in turn, reduce the dc bus voltage.

The description so far has been made with the assumption that the dc load current is continuous. In a practical circuit with a dc motor armature as load, the actual operation always covers the range of discontinuous current at light load levels also. Reducing the load current, one finally reaches a level where the ripple amplitude is high enough to interrupt the current cyclicly. At this transition point, the output voltage E_d rises sharply (keeping α constant) with decreasing load current and aims to a point equal to the peak converter voltage $\hat{e}_d$ at zero load current. This transition point depends on the gating angle α, the inductance and losses in the load circuit.

Commutation from a first leg to a second must always be completed before the anode voltage of the second leg swings negative. If the latter should happen, the commutation is incomplete and the full-load current will commutate back into the first leg. This situation can only arise if the commutation was initiated at a high gating angle (in the inverter range) and if the load current is continuous.

The circuit described so far can provide voltage of both polarities. The current, however, can only flow in the conducting direction of the rectifying cells. This circuit is, therefore, classified as a single converter.

For C-600M a second converter is added and connected to the first in an antiparallel circuit as shown in Figure III-4. Since such a circuit can produce load current in both directions, this circuit is classified as a double converter.

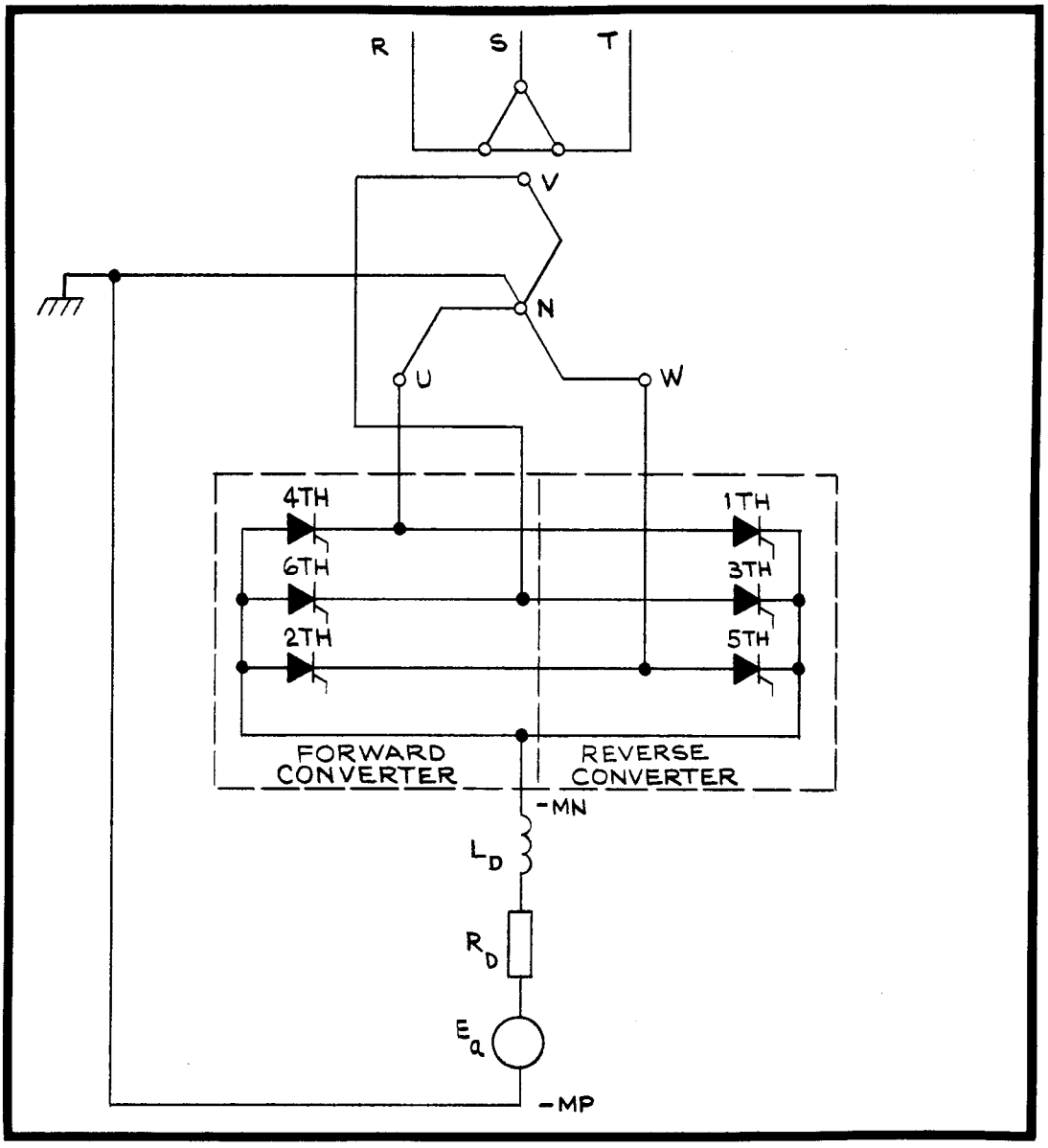

FIGURE III - 4 DOUBLE CONVERTER

There are several ways to control such a double converter. The principle used in C-600 is to use two gating channels, but biased such that circulation current control cannot occur. The operation will now be explained with the help of Figure III-5. The systems diagram shows the main control elements of the double converter, with the power circuit in single line diagram form. An inner current loop is closed. While this regulation loop helps greatly to overcome the nonlinearities of the power converter when going from continuous to discontinuous current, the decrease in gain for the system requires that the voltage or speed controller (immediately prior to the current controller) be of standard design to operate satisfactorily in this varying gain region.

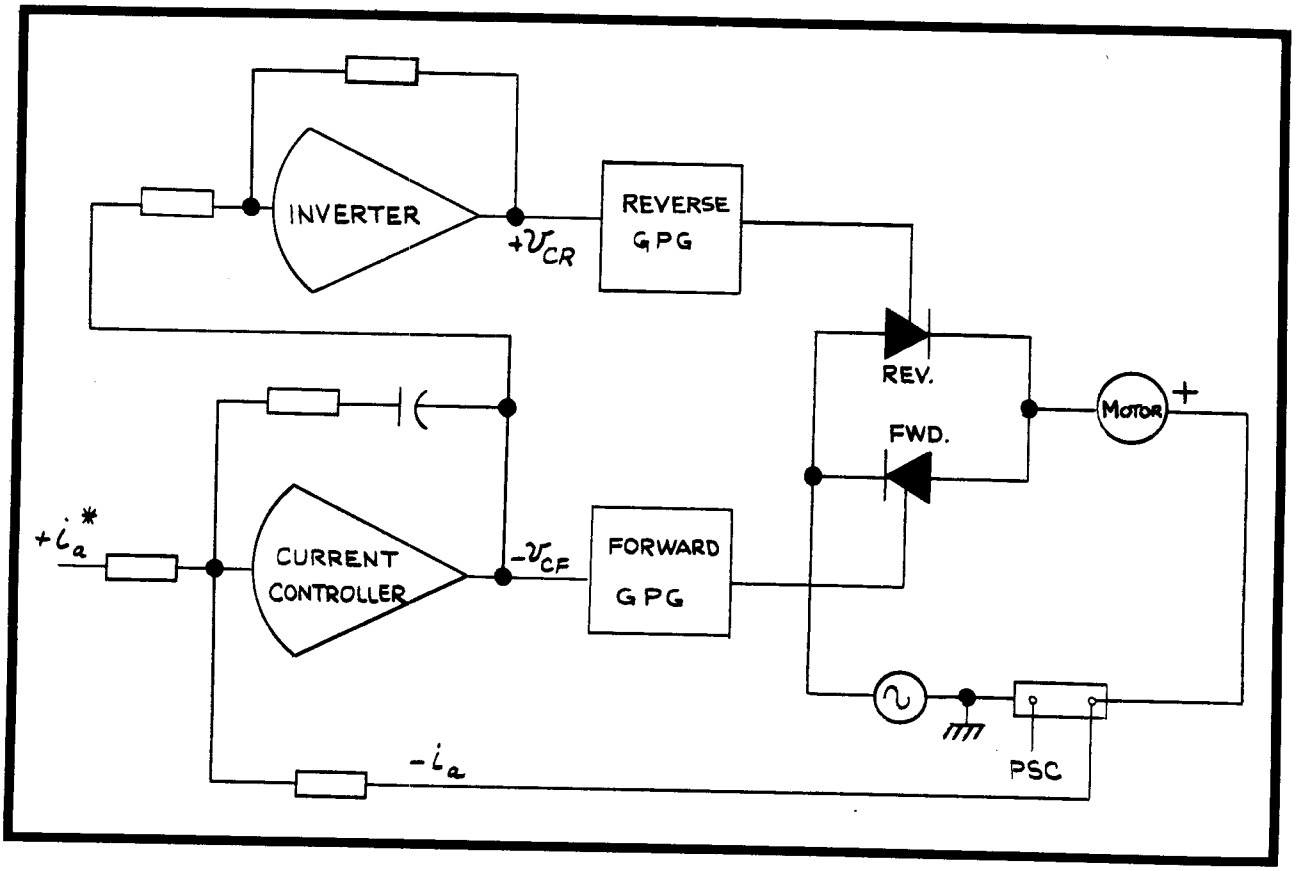

FIGURE III - 5 DOUBLE CONVERTER SYSTEM

The armature current (-ia) is sensed by the shunt and brought to one input of the current controller. There it is compared with the current reference $+i_a^*$ which is applied at a second input. When both inputs are zero, the output ($-v_{CF}$) will be zero as well as the output of the inverter ($+v_{CR}$). The current controller and inverter act together as a differential output amplifier, so when one output goes negative, the other goes positive, and the sum of the outputs is always zero. With both inputs to the GPG's zero, referring to Figure III-6, it can be seen that no current will flow in either converter. When $+i_a^*$ goes positive, $-i_a$ goes negative, and the forward converter phases towards $\alpha = 0^o$, until the current feedback signal -ia matches the reference $+i_a^*$, resulting in forward current.

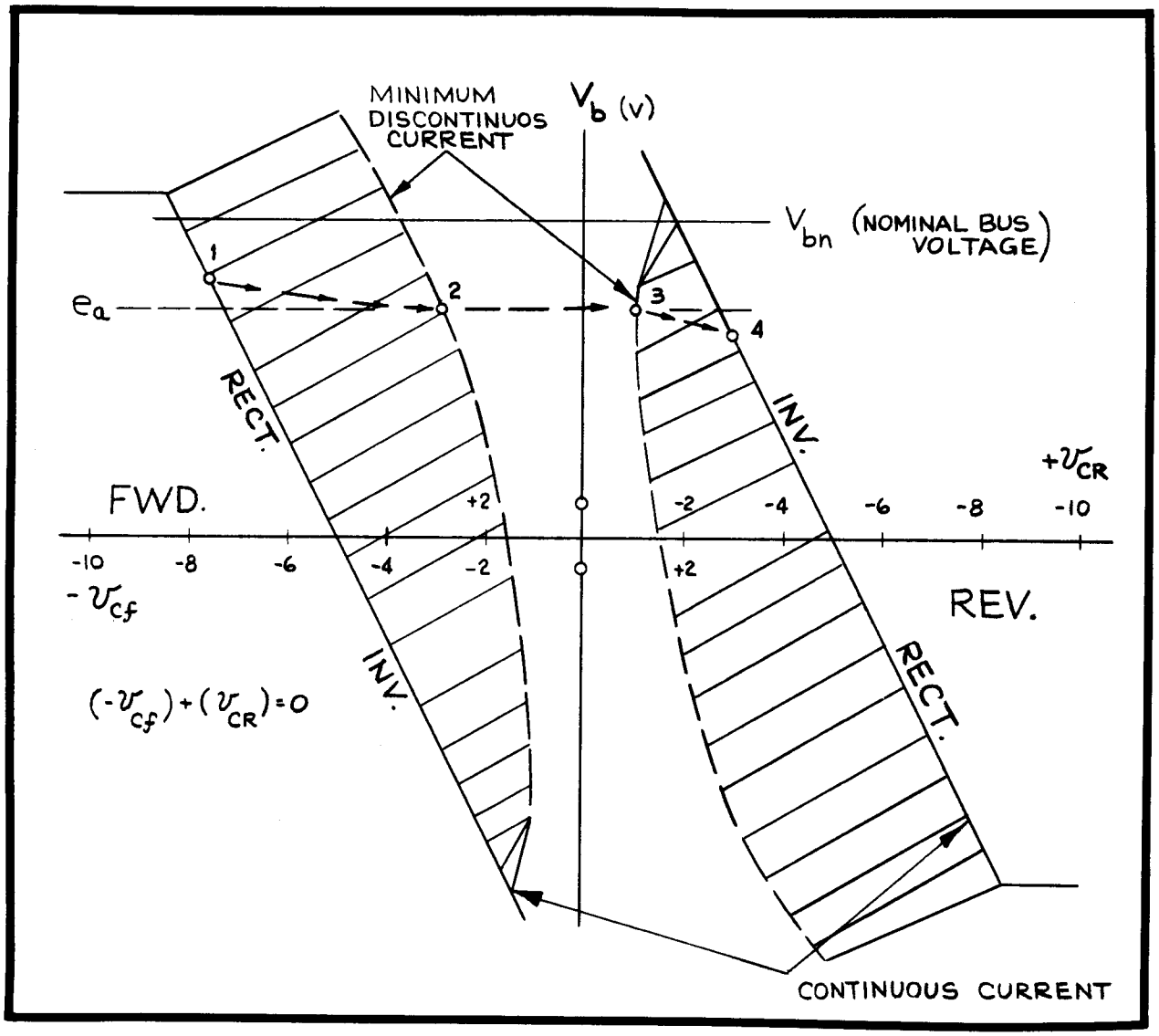

FIG. III - 6 DOUBLE CONVERTER COATED CHARACTERISTICS

With the aid of Figure III-6, a current reversal will be described. The counter emf e_a of the load is assumed to be as shown in Figure III-6 (continuous current is flowing) with the forward converter rectifying at point 1. Suddendly a current reversal is demanded as a result of $+i_a^*$ going from a positive to a negative value. This will cause $-v_{cf}$ to advance toward a positive value and $+v_{CR}$ to advance toward a negative value. At point 2 the forward current will stop altogether and V_b will equal e_a. At point 3, $+v_{CR}$ will have become negative enough to start inverting current in the reverse converter. Finally at point 4, the new quiescent state of reverse current has been reached and $-i_a$ is matching again the reference $+i_a^*$.

The opposite sequence of events take place in case of a change from reverse to forward current.

Figure III-7 shows an oscillogram of a current reversal in the double converter with a step change of current reference.

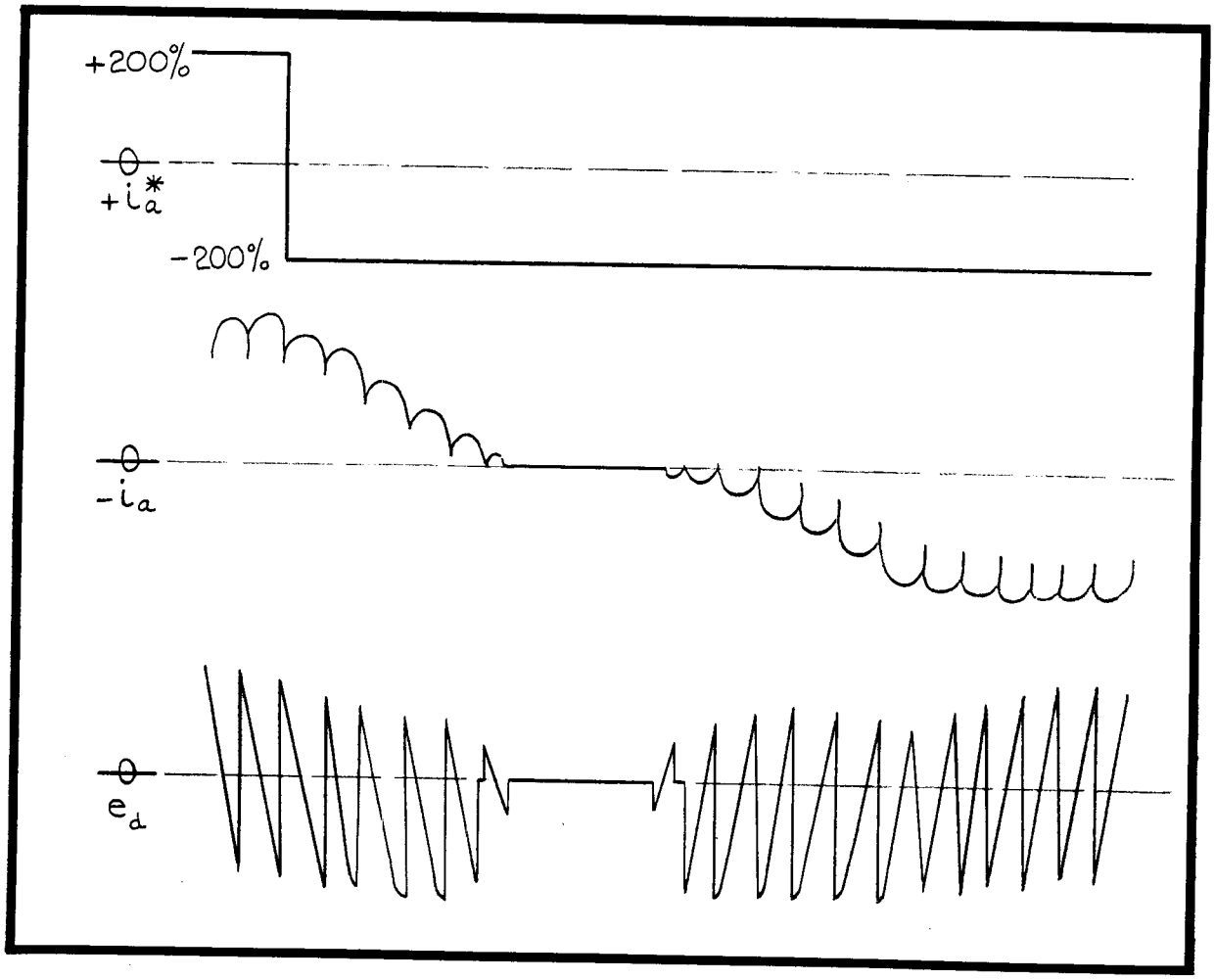

FIGURE III - 7 REVERSAL OF ARMATURE CURRENT

8. Thyristor Power Modulator (TPM)

This modulator assembly includes the thyristors connected in a three-phase, single-way double converter circuit. The schematic diagram is shown on Figure III-8. TPM's employed on drives 5 to 20 HP use power disc thyristors which are clamped between heat sinks allowing single sided cooling. Drives up to 20 HP use natural convection cooling.

The R-C networks connected from the ac lines to the DC output terminal serve to attenuate excessive rates of voltage which otherwise may lead to undesired turn on of thyristors, and to clamp the oscillations that would otherwise be produced by the commutation process. The pulse transformers provide the necessary isolation between thyristors and the proper pulse amplitude.

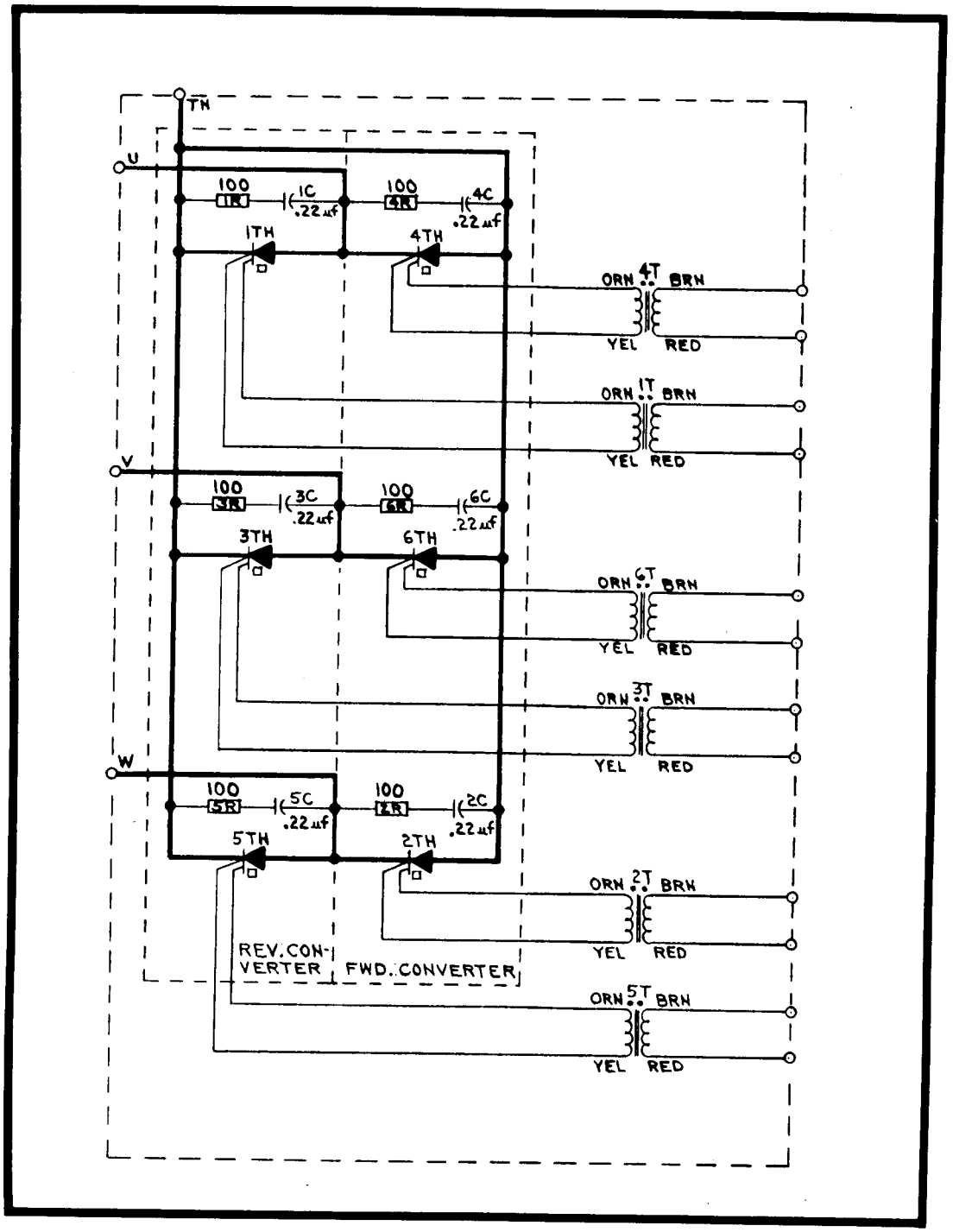

FIGURE III - 8 THYRISTOR POWER MODULATOR

NOTE: The R-C suppressors and gate pulse transformers (GPT) are mounted on printed circuit boards attached to each side of the TPM.

C. Regulator Cage

The regulator Cage contains both preselected and optional components. The sum of the preselected components will be designated as the basic regulator and comes in two types:

1. Voltage Regulator. This includes three single phase transformers connected as a three-phase transformer with a delta primary and star secondary used as both gate control transformer and dc power supply transformer, gate pulse generator board, power supply and phase detector board, static sequencer board, protection board, calibration board, and voltage and current controller (V & CC) board.

2. Speed Regulator. This includes the same equipment as the voltage regulator except a speed and current controller (S&CC) board is substituted for the V&CC board.

In both the V&CC board and S&CC board an external current limit is provided at terminal 43. This provides (with an appropriate external network which may be part of the optional equipment in the cage) a means of current limit recalibration or current control with outer voltage or speed limit.

Space is provided in the regulator cage for one optional plug in board.

Figure III - 9A, 9B, 9C and 9D shows a signal distribution diagram of C600M regulator.

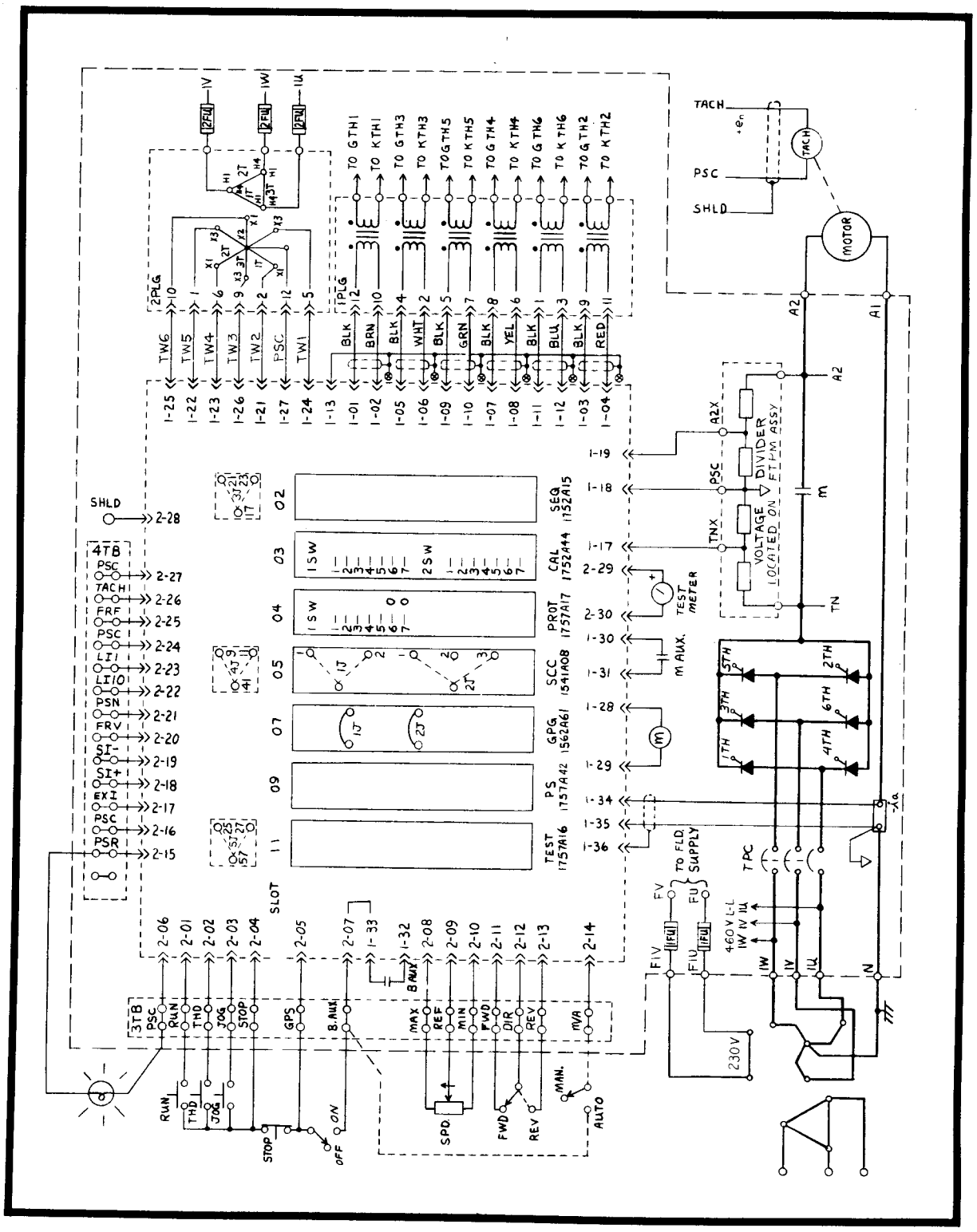

FIGURE III = 9A C600M INTERCONNECTION DIAGRAM

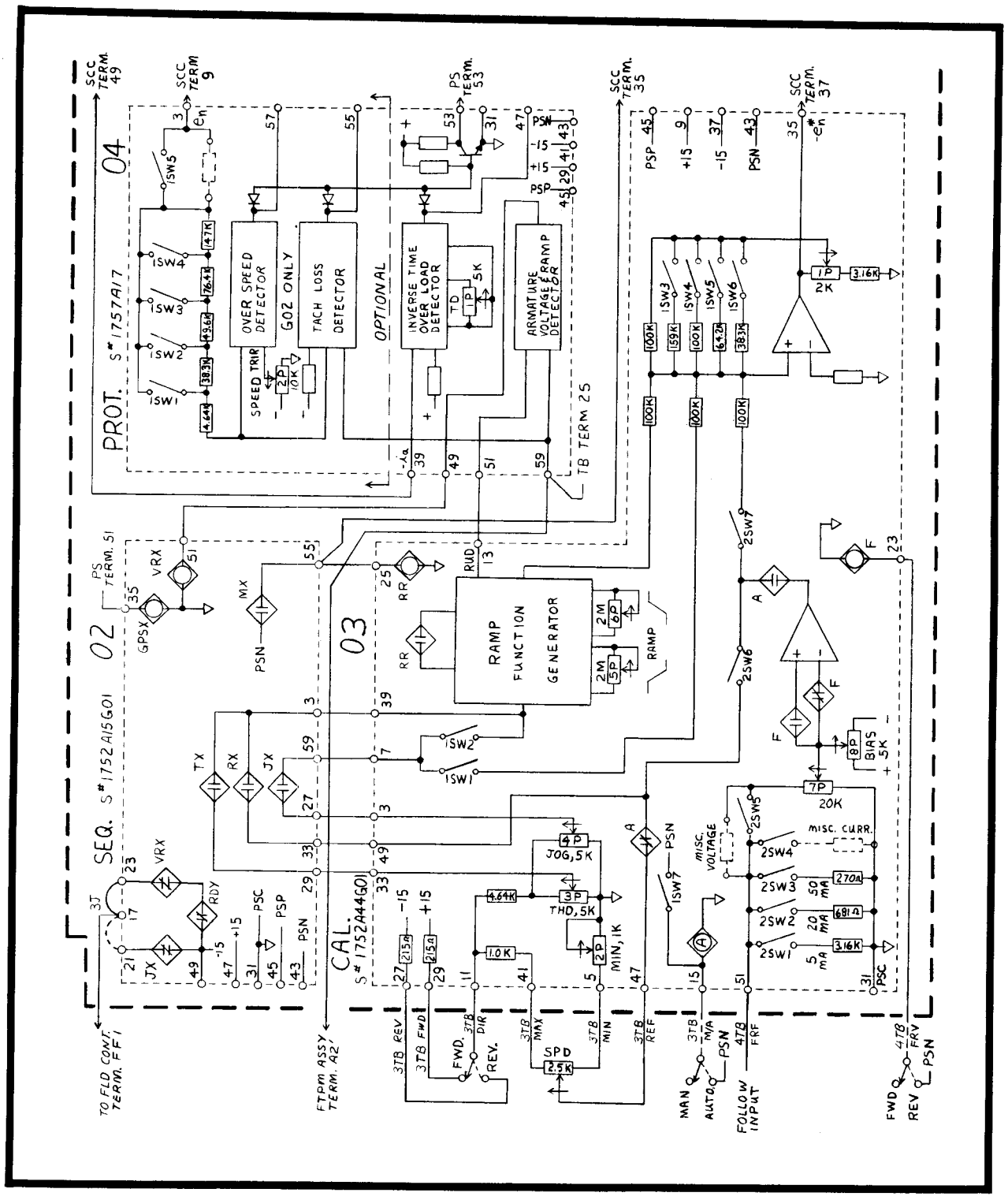

FIGURE III - 9B SPEED OR VOLTAGE REGULATOR SIGNAL DISTRIBUTION PART I

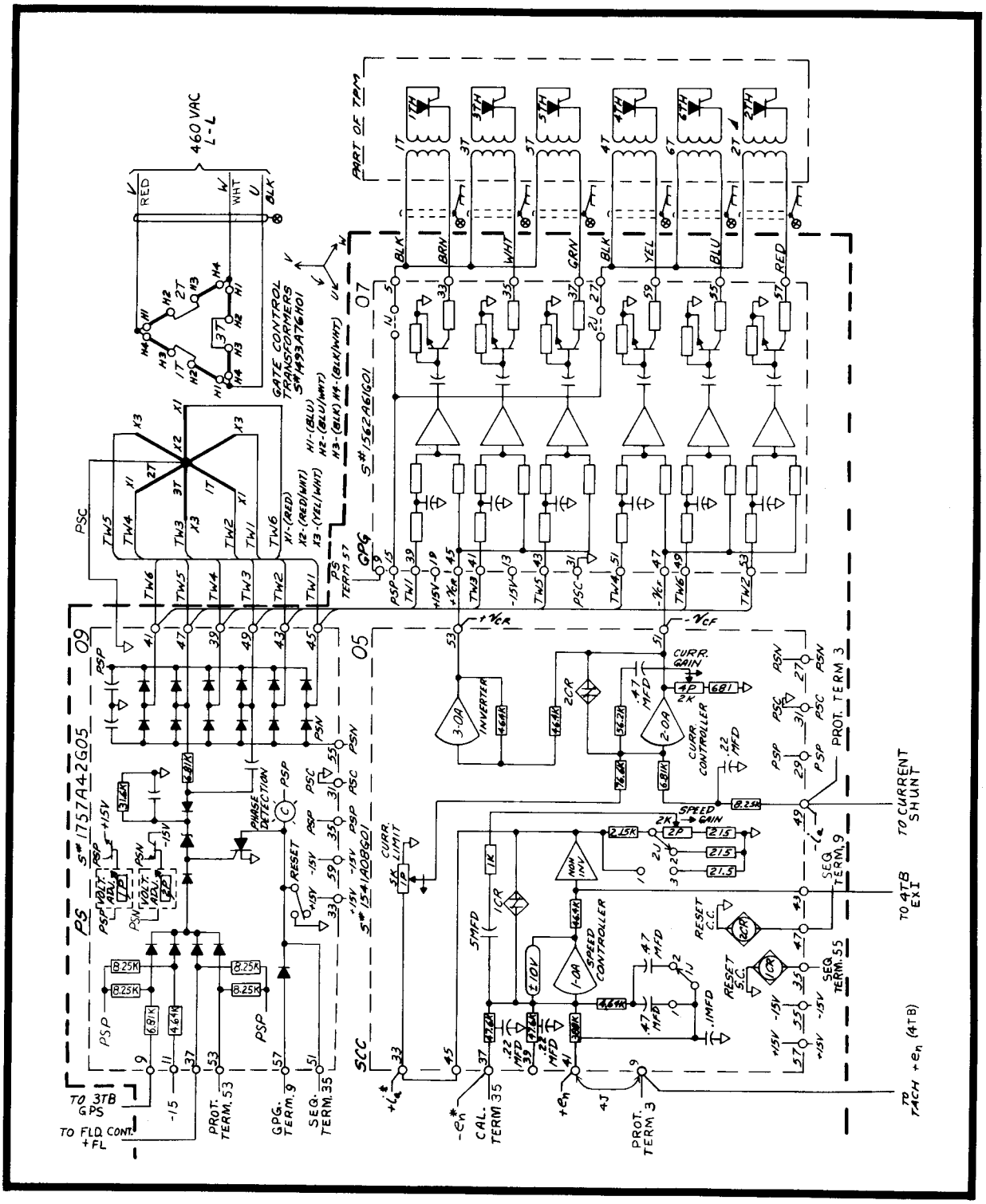

FIGURE III - 9C SPEED REGULATOR SIGNAL DISTRIBUTION PART 2

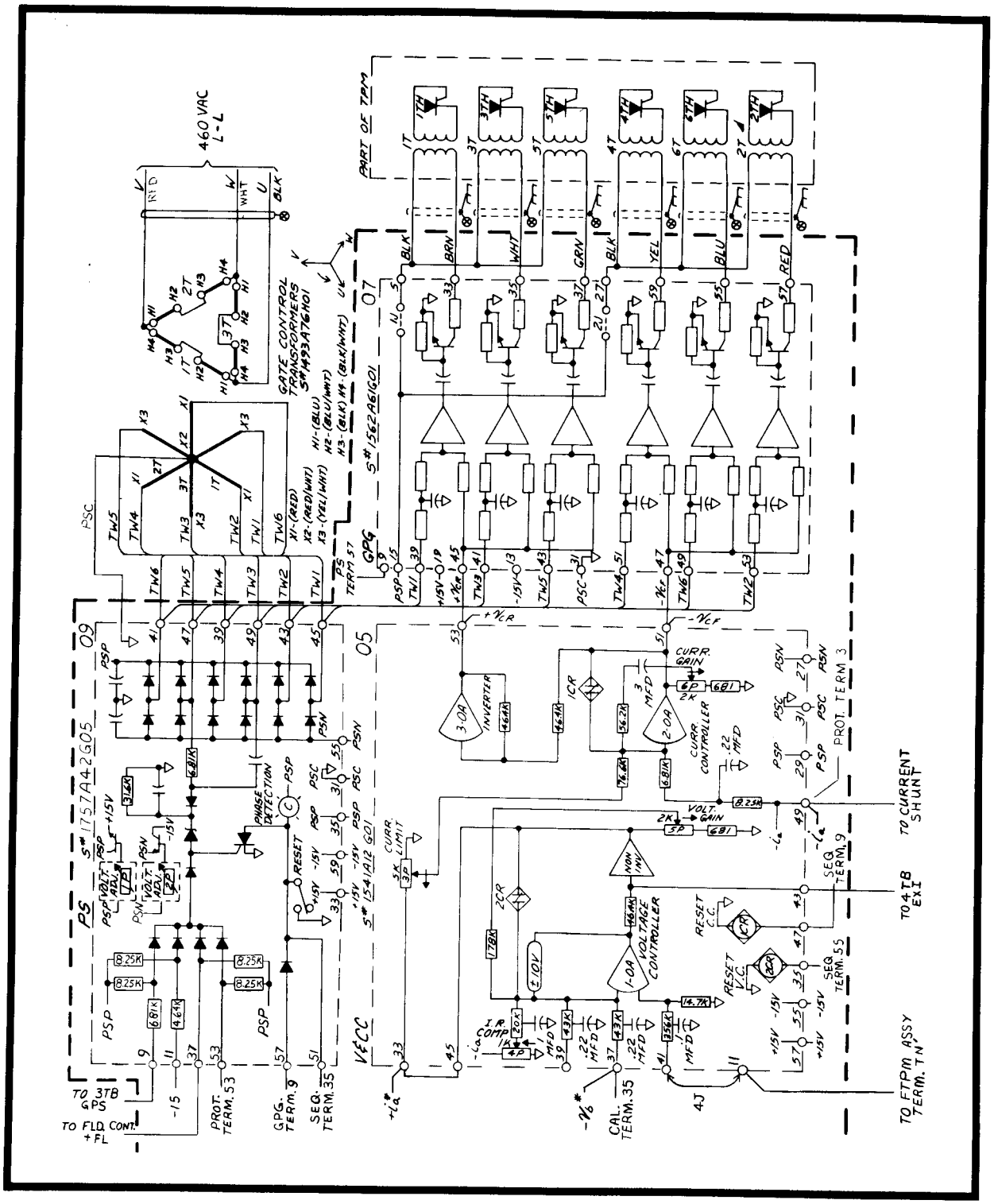

FIGURE III - 9D VOLTAGE REGULATOR SIGNAL DISTRIBUTION PART 2

1. Gate Pulse Generator (GPG)

A schematic diagram of the GPG is shown in Figure III-11. The GPG board contains six identical circuits, of which three form the forward GPG and the other three form the reverse GPG. Inputs common to all circuits are +15V, -15V, PSP, PSC, and GPS which when tied to PSC prohibits any gate pulses from being released. (The initiation of this pulse inhibit function is discussed in a later section covering the power supply and phase detector board.) Inputs to the forward GPG are its control voltage $-v_{cf}$ and three timing waves TW4, TW6, and TW2. Outputs are pulse 4, pulse 6, and pulse 2. Inputs to the reverse GPG are its control voltage $+v_{CR}$ and three timing waves TW1, TW3, TW5, and corresponding output pulses 1, 3, and 5.

A requirement of either GPG is to have three pulses spaced 120^{o} apart. The timing waves generated from the six phase star secondary transformer are six identical sine waves displaced 60^{o} between TW1...TW2, TW2...TW3, etc. The resulting 120^{o} displacement between timing waves to the forward GPG/reverse GPG (TW4...TW6, TW6...TW2/TW1...TW3, TW3...TW5) provides the means to obtain three pulses spaced 120^{o} apart over the entire phase shift range under steady state conditions. It must be remembered that the control voltages ($-v_{cf}$, $+v_{CR}$) are generated such that only one can be negative at a time and therefore only one GPG can be on at a time.

A second requirement of either GPG is to limit the dc control voltage so that the pulse cannot advance ahead of $\alpha = 10^{o}$. This assures that pulses cannot be phased out when demanding a large voltage in the rectification mode which would otherwise result in a sudden loss of voltage. The limit function is provided by the -15V with 17R, 84R, and 8D for the forward GPG and with 14R, 16R and 7D for the reverse GPG. With continuous current flowing this type of limit results in a fixed voltage limit (Figure III-6), and with 10% low line voltage, assures that pulses do not advance ahead of $\alpha = 10^{o}$. For nominal line voltage the advance limit is approximately $\alpha = 30^{o}$.

A linear relationship between the input dc control voltage and the output voltage of the power converter is desired ($E_d/_{-v_{cf}}$ = constant), assuming continuous current is flowing in the power converter. Since the converter voltage varies as the cosine of the gating angle, the phase position of the output pulses must vary as the inverse cosine of the dc control voltage. This is accomplished by pulsing when the control voltage intersects an appropriate cosine wave. The generation of pulse 4 will be explained with reference to Figure III-10.

Pulse 4 is to be controlled during the period when line W is positive with respect to line U. Timing wave 4 leads W-U by 120^{o}. Resistor 45R, 46R and capacitor 10C is a 30^{o} lag filter which with TW 4 generates cosine wave 4 which leads W-U by 90^{o}. A positive bias is added through 47R so that when $-v_{cf}$ is zero pulse 4 is biased to $\alpha = 180^{o}$. Current from the bias, cosine wave, and control voltage is summed at the base of transistor 16TR. When the sum of this current reaches zero, proceeding toward negative values, a pulse is initiated. Transistor 16TR turns off, 18TR turns on, capacitor 11C couples the signal and establishes the pulse width to 19TR, 19TR turns off turning 20TR on for the specified pulse width. Resistor 56R with the pulse transformer establishes the proper power level to gate thyristor 4TH.

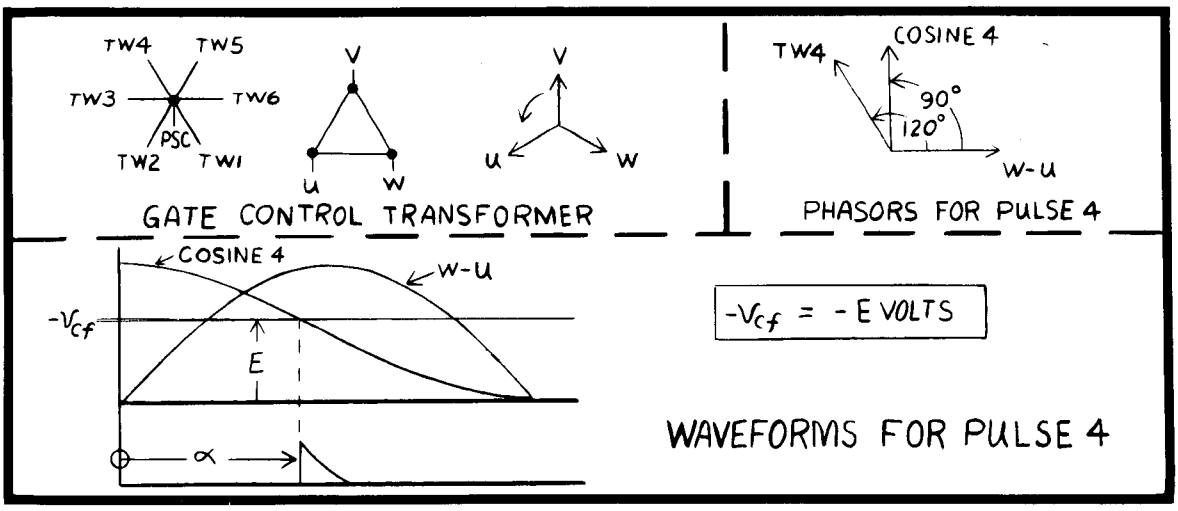

FIGURE III - 10 PHASING FOR PULSE 4

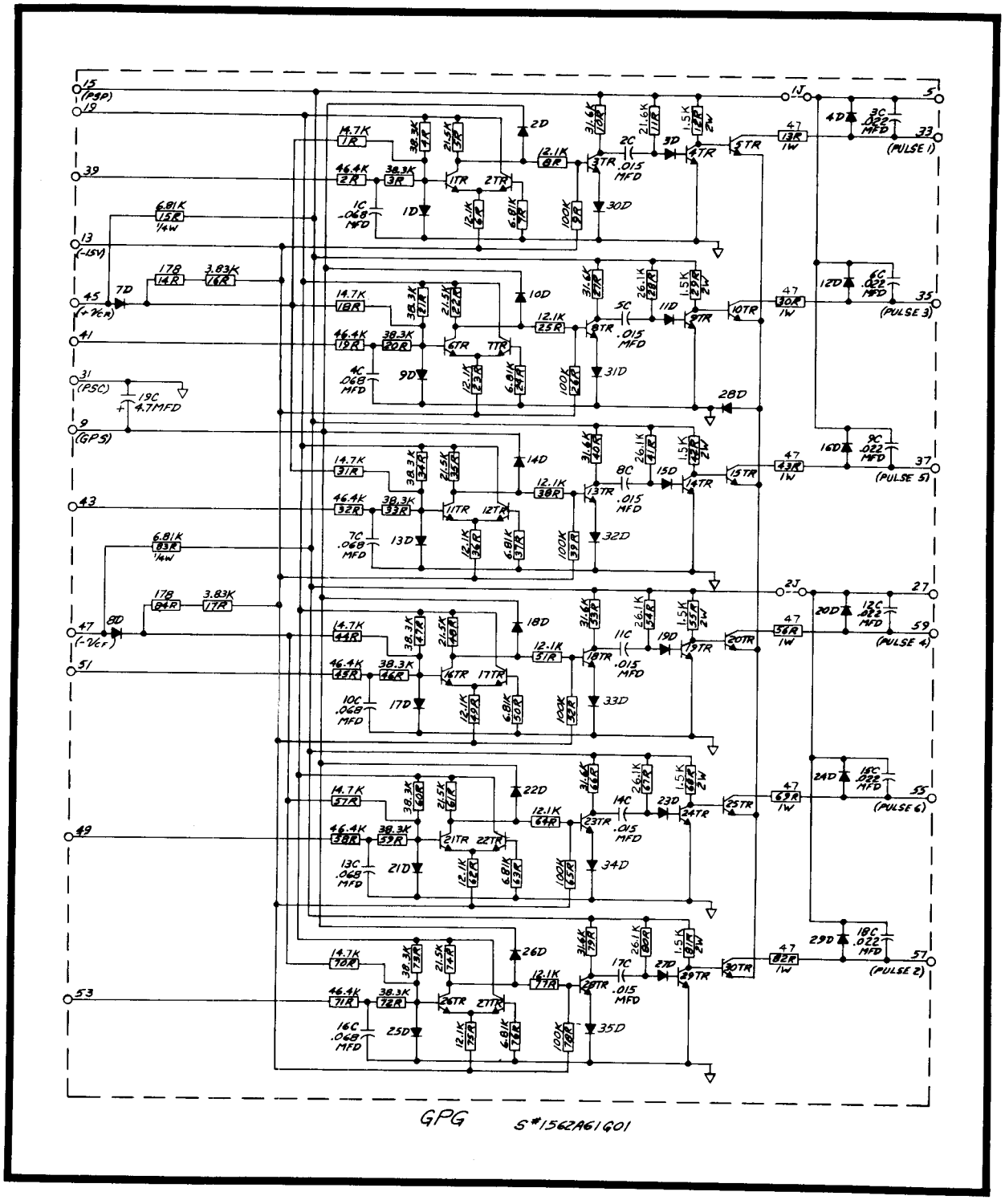

FIGURE III - II GATE PULSE GENERATOR

2. Power Supply and Phase Detector (PS & PD)

This board performs the functions of an unregulated ±24V DC power supply, a regulated ±15V dc power supply, and a phase sequence and missing phase detector. Figure III-12 is a schematic diagram of this board.

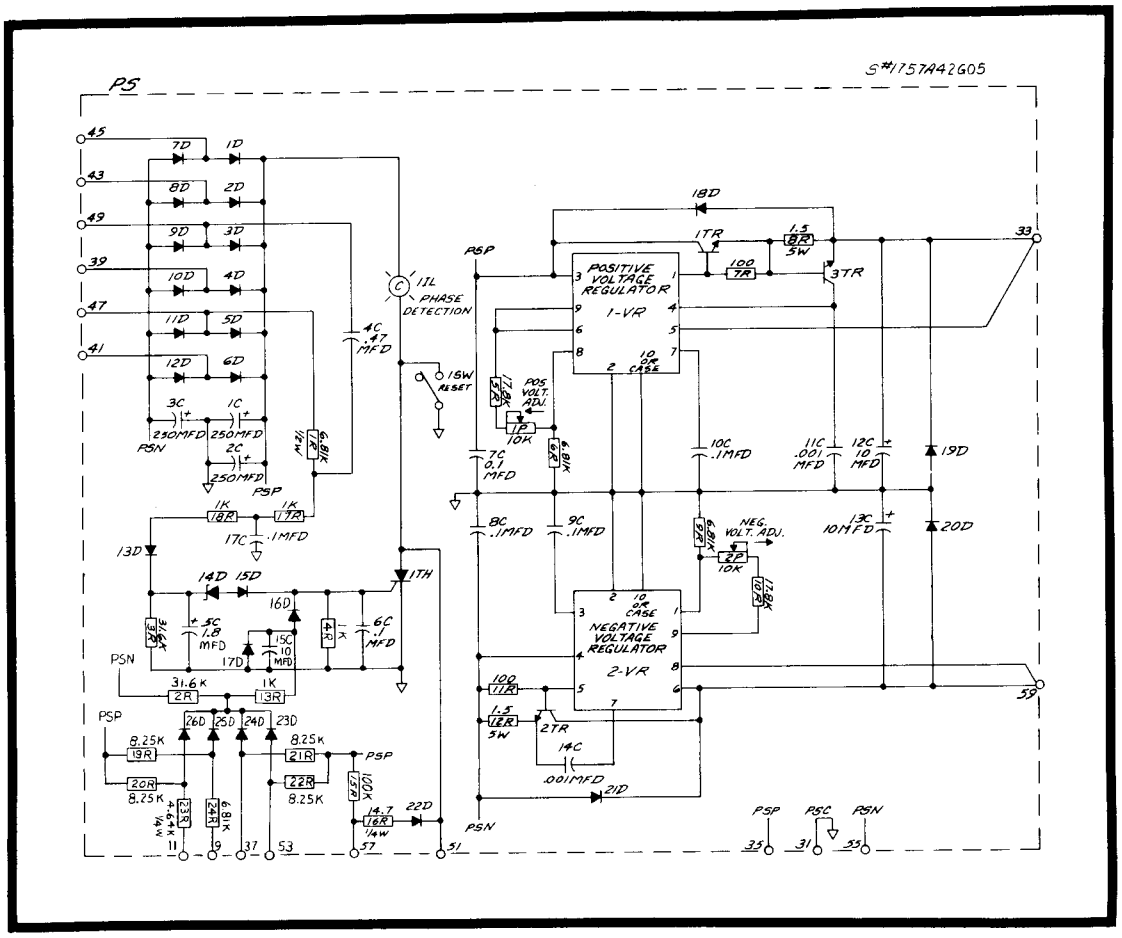

FIGURE III - 12 POWER SUPPLY & PHASE DETECTOR

The unregulated ±24V dc supply is powered by the timing waves TW1, TW2,...TW6. These sine waves are rectified near their peak values by diodes 1D through 12D and charge capacitors 1C, 2C, and 3C. The +24V dc supply is denoted as PSP and the -24V dc supply is denoted as PSN. PSP and PSN supply dc power where voltage regulation and ripple are not critical such as driver stage of the GPG, and input power to the regulated supplies.

The ±15V dc power supplies are controlled by integrated circuit voltage regulators 1-VR and 2VR. Transistors 1TR and 2TR are amplifier stages and are current limited just above 300 ma by associated circuitry. Each supply is short proof for a moderate period of time. potentiometers 1P and 2P are vernier adjustments for the supplies. The ±15V dc regulated supplies are used to supply power for integrated circuit operational amplifiers in the regulator cage and for reference voltages.

Timing waves TW3 and TW5 are applied to the R-C network 1R and 4C. With proper phase sequence (also no phases missing) the amplitude at the output of the R-C network is insufficient to breakover zener diode 14D and trigger thyristor 1TH. With improper phase sequence or missing phases the voltage out of the R-C network increases significantly and will breakovaer 14D triggering 1TH. Thyristor 1TH could also be triggered from external signals brought in at terminals 9, 11, 37 and 53. Firing of 1TH inhibits gate pulses by droping the voltage at terminal 57 to near PSC potential, resets the sequencer to the stop mode, and provides a power not ready signal at terminal PSR located on 4TB.

3. Voltage and Current Controller (V&CC)

This board consists of a voltage controller (1-0A), a current controller (2-0A), and an inverter (3-0A). Figure III-13 is a schematic diagram of this board

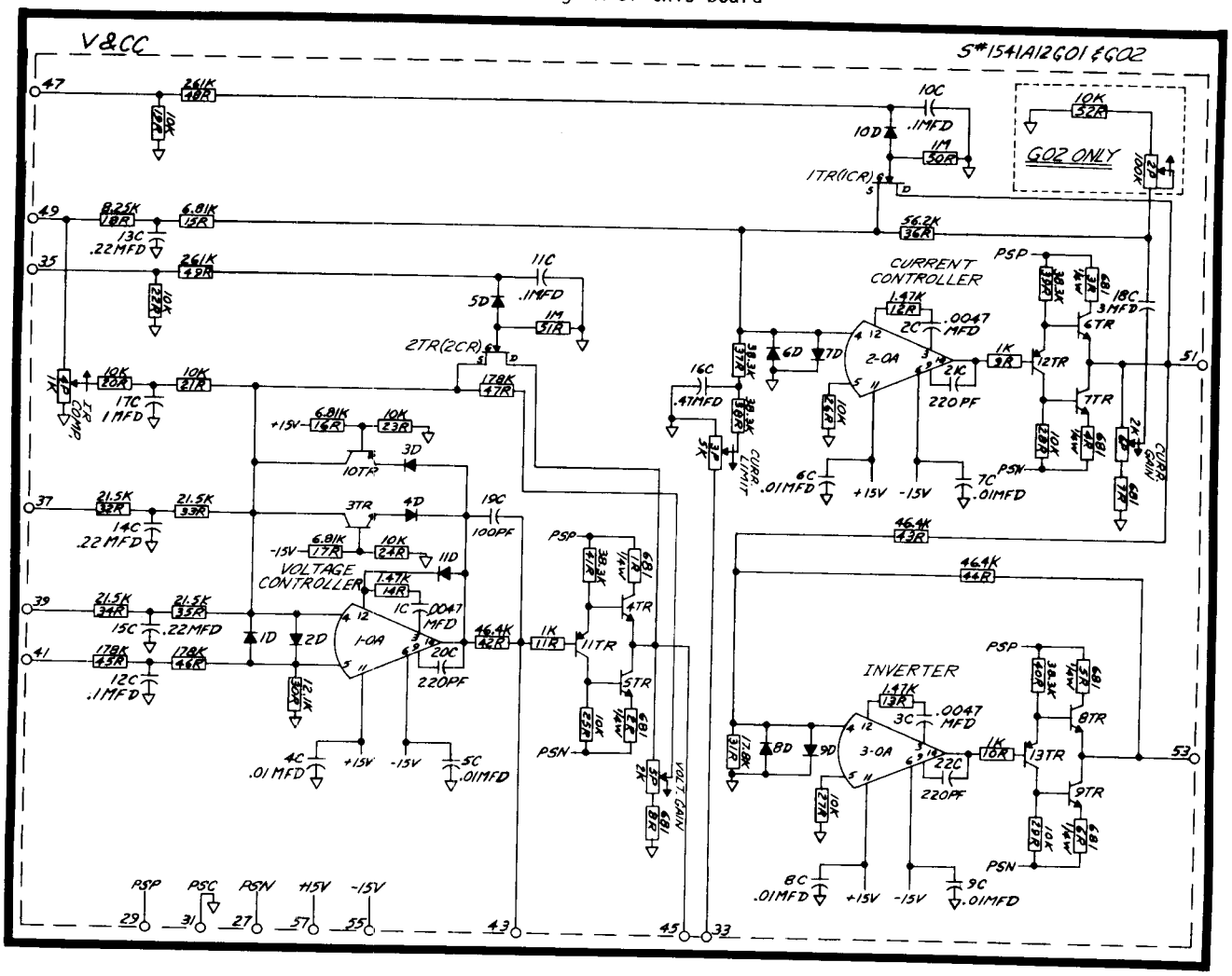

FIG. III - 13 VOLTAGE & CURRENT CONTROLLER

The current controller and inverting amplifier are used as a differential output amplifier to drive both the forward and reverse gating channels of the GPG. The current controller is a PI controller with a fixed lead of 150 ms which maintains steady state accuracy of the current loop. There is a 10 ms filter at the input of the current controller to limit the rate of change of current. Current gain, hence dynamic performance, of the current controller is adjusted by means of pot 6P. A current limit adjustment is provided by pot 3P, and a reset function is provided by FET switch 1TR to prevent amplifier drift during standby conditions (terminal 47 open).

The voltage controller is a proportional amplifier with a 15 ms filter at the voltage feedback to reduce voltage ripple. Voltage controller gain adjustment is provided by potentiometer 5P, which in conjunction with 6P (current controller gain) determines the response of the drive. When a small reference ($-V_b^*$) change is made, the drive would reach the new reference in about .1 sec provided current limit is not reached. IR compensation is provided by 4P. FET switch 2TR provides a reset function for the amplifier. The limiter (approximately ±10V) of the voltage controller provides the current limit reference to the current controller when no external current limit is used.

4. Speed and Current Controller (S&CC)

This board consists of a speed controller (1-0A), a current controller (2-0A), and an inverter (3-0A). Figure III-14 is a schematic diagram of this board.

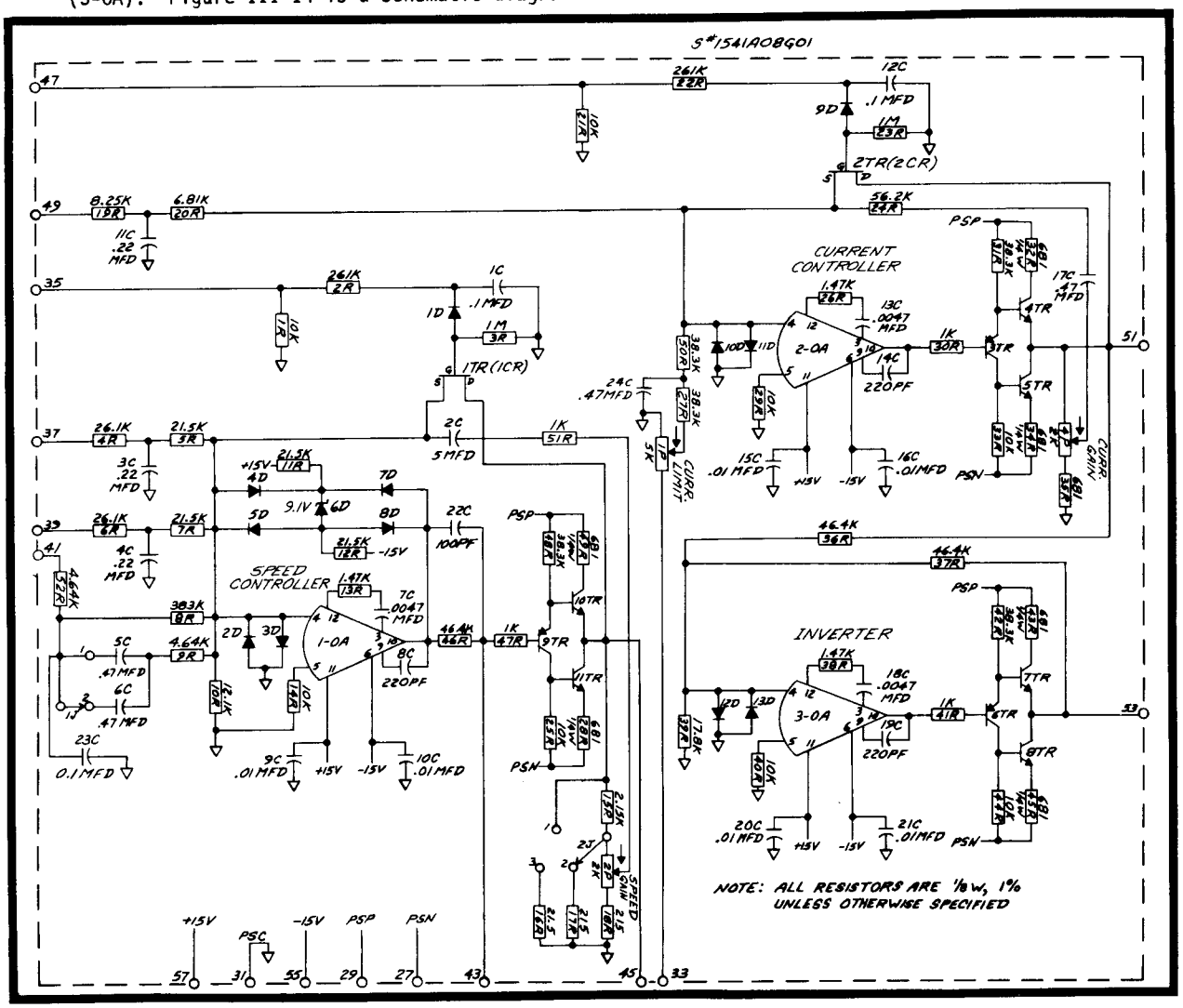

FIG. III - 14 SPEED & CURRENT CONTROLLER

The current controller and inverting amplifier are used as a differential output amplifier to drive both the forward and reverse gating channels of the GPG. The current controller is a PI controller with a fixed lead of 28 ms to compensate for the armature time delay. There is a 10 ms filter at its input to limit the rate of change of current. Current gain, hence dynamic performance, of the current controller is adjusted by potentiometer 4P. A current limit adjustment is provided by pot 1P and a reset function is provided by FET switch 1TR to prevent amplifier drift during standby conditions (terminal 47 open).

The speed controller is a type 1 controller with a small lead in the feedback to approximately cancel the lag at the input of the current controller. A lead of 190 ms or 380 ms, selected by jumper 1J, is provided in the tachometer feedback loop to compensate for the mechanical time constant of the motor. Speed controller gain is adjusted by jumper 2J and pot 2P. Through selection of jumper connection 2J and pot setting 2P, a crossover frequency of 10 rad/sec.... 50 rad/sec can be obtained. A reset function is provided by FET switch 2TR. The speed controller limiter (approximately ±10V) provides the current limit reference to the current controller when no external limit is used.

5. Calibration Board (CAL)

A schematic of the CAL board is shown in Figure III - 15. The board consists of reference potentiometers, a manual/auto mode selector, a scaling amplifier, a ramp function generator, and a follow circuit.

A speed potentiometer (2.5k) when connected to pins 5, 41, and 47 provide full speed range of adjustment, whereas thread (THD-3P) and jog (JOG-4P) adjusts from 0 to 50% speed. Minimum speed pot (2P) adjusts over a 0 to 30% range. Reversing the reference is accomplished by reversing the polarity of the 15 volts supply pin (11) through connection to either pin (29) or pin (27) by using the Forward/Reverse switch.

The "manual" reference (by speed pot) applied at terminal 47 and the "Auto" reference emminating from 5-0A output is switched by transistors 1TR and 2TR to pin 49 where it goes to the Sequencer Card. When manual or normal operation is desired, pin 15 is at zero volts; when "auto" mode is desired, pin 15 is tied to -24 volts. Switches, 2SW6 and 2SW7 allow the follow signal to be routed through or around the ramp function generator respectively. Switches 1SW1 and 1SW2 determines whether the Jog reference is to pass around or through the Ramp Function Generator, respectively.

The "Max" Speed pot 1P adjusts the speed range, in conjunction with calibration op-amp 3-0A and 1SW3 through 1SW6, as follows:

TYPE OF DRIVE	1SW SWITCHES CLOSED	MAX. SPEED ADJUSTMENT RANGE (RPM)
Speed Regulated	3, 4, 5, 6	588 - 960
Speed Regulated	3, 4, 5	956 - 1561
Speed Regulated	3, 4	1521 - 2482
Speed Regulated	3	2456 - 4010
Voltage Regulated	3	

NOTE: 1) Maximum speeds are based on a maximum input reference of 10 volts and a tachometer generator voltage of 20.8V/1000 RPM. Maximum speeds are decreased proportionately for a lower maximum input reference.

2) Where the maximum input reference is considerably less than 10V, switches 3, 4, 5, and 6 may be left open and will yield an adjustable speed range of 2933 to 4785 RPM with a 7.5 volt maximum input reference applied.

Other combinations of the above positions are possible, but they will result in overlapping two adjacent ranges of the above.

The signal follow circuitry is comprised of op-amps 4-0A and 5-0A and associated components. Switches 2SW1 through 2SW5 allows following of current reference (i.e., 1-5ma, 4-20ma, 10-50ma) of either polarity or a voltage reference of 0 to ±10VDC. Pot 8P allows biasing out part of the current source reference such that zero reference may be achieved when minimum input current is applied. With full current reference (i.e., 5ma, 20ma, and 50ma) 12 volts reference can be achieved with 7P fully CW. With 1SW1 through 1SW5 open and 38R specified, a miscellaneous voltage may be brought into pin 51. Reversing of the follow signal may be obtained by use of the polarity switch operable by pin 23. With pin 23 at -24 volts the signal polarity at pin 51 is non-inverted. When pin 23 is held at zero volts, the reference polarity of pin 51 is inverted.

Pot 5P adjusts the rate of ramping in the negative going direction (i.e., forward deceleration/reverse acceleration). Pot 6P adjusts rate of positive going signals at the ramp input (i.e., forward acceleration/reverse deceleration). The ramp time is adjustable from 2 to 40 seconds. Pin 25 is used to reset the Ramp. When at -24V the reset is disabled, when at zero volts the reset is enabled.

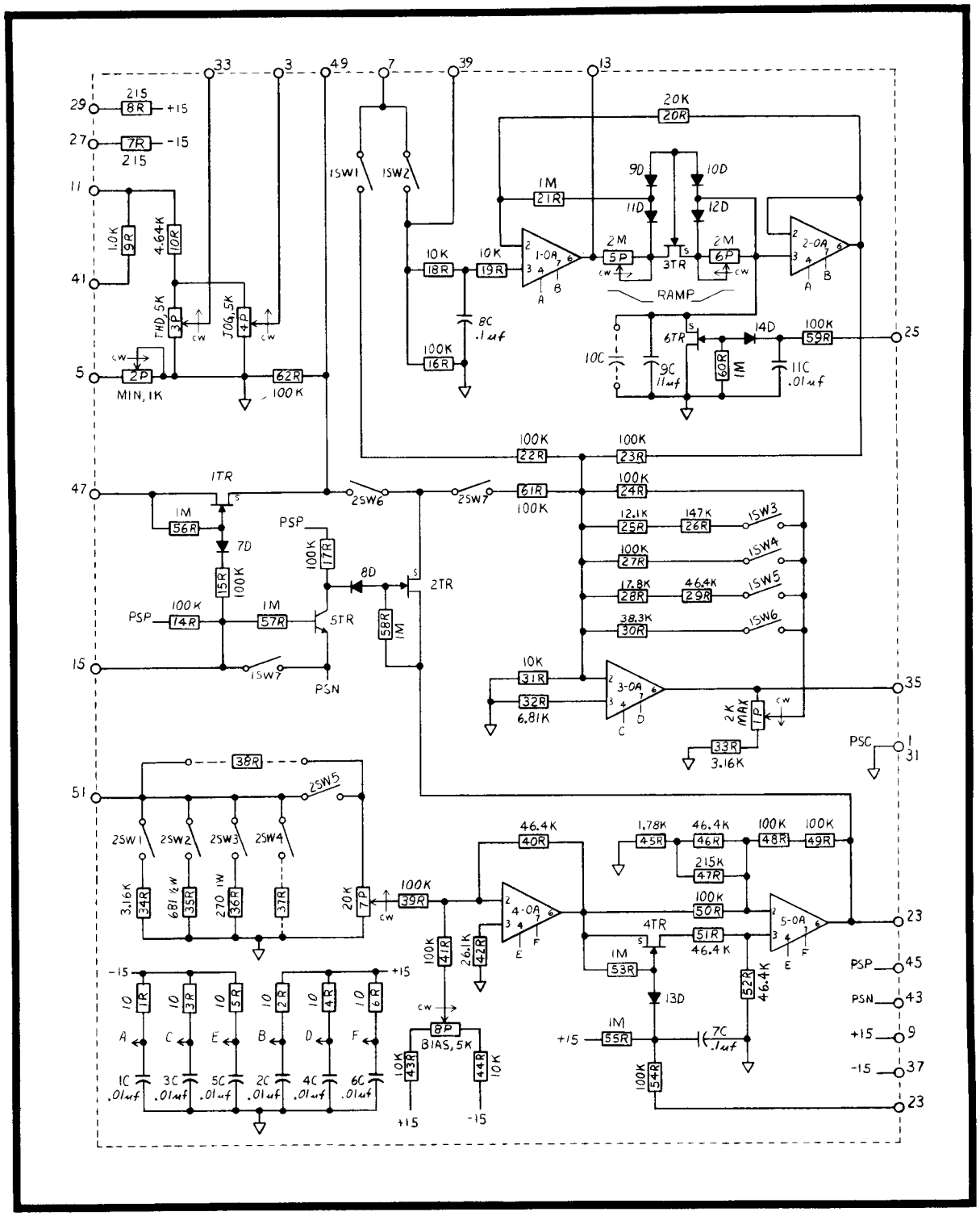

FIGURE III - 15 CALIBRATION BOARD

6. Protection Board (PROT.)

A schematic of the PROT. board is shown in Figure III - 16. G01 of this board consists of a static overload circuit and a voltage sensor used for antiplugging. G02 is an option which includes the G01 circuitry plus a tach loss and overspeed detector.

Overload protection is provided by op-amps 1-OA, 2-OA, 3-OA and associated circuitry. The static overload circuitry is designed to provide protection for both Motor and TPM; an improvement over the usual overload relay. Typical points on the trip curve of the static overload circuit are: 150% at one minute, and 200% at 10 seconds, and 115% continuously. Instant tripping occurs on overloads exceeding 225% rated current. Potentiometer 1P adjusts for tolerance of components associated with the timer amplifier, 2-OA. Current feedback (0.5 volts equal to 100% rated current) is fed to pin 39. When 115% I_{dn} is exceeded (i.e., 115% X 0.5V), the bias current to 2-OA is exceeded and 2-OA integrates positively until the bias current of 3-OA is exceeded at which point the output of 3-OA, which is normally in positive saturation switches to a -0.5 volts. Whenever the outputs of either 3-OA, 4-OA, or 5-OA go negative from positive saturation transistor 1TR turns off, a signal at pin 53 is fed to the Power Supply board where a GATE PULSE SUPPRESSION function is initiated.

The Voltage sensor is an absolute value circuit which integrates the CEMF motor voltage and the first stage of the ramp function generator. Whenever the CEMF Voltage (Pin 59) is approximately 20% or more of the rated voltage feedback (75V) or the first stage of the ramp function generator (pin 51) is greater than 7 volts either positive or negative, the output of 6-OA (pin 49) will be -7.5V or more negative. This signal is sent to the sequence board which performs antiplugging function.

The optional Tach Loss and Overspeed Detector circuitry is comprised of 5-OA and 4-OA and their associated circuitry respectively. Op-amp 5-OA compares the difference between the tach feedback and voltage feedback signals and compares this to a fixed bias representing roughly 30% of rated bus voltage. If 30% bus voltage is exceeded and the tach signal is not present, the output of 5-OA will switch from positive to negative saturation and gate pulse suppression will be initiated as previously explained. Op-amp 4-OA compares the tach feedback voltage with an adjustable bias (2P). If the feedback exceeds the value set by the bias, gate pulse suppression is again initiated.

The tach loss and overspeed detector portion of the circuit is adjusted as follows:

If the tachometer used in the system has a gain of 20.8V/1000 RPM and if the base speed of the drive is either 500, 650, 850, 1150, or 1750 RPM, then the tachometer input may be applied directly to pin 3 and 1SW adjusted per Table 1.

TABLE 1

INPUT SELECTION TABLE

BASE SPEED OF DRIVE		1SW SWITCHES CLOSED
500 RPM	-	1SW1. 1SW5
650 RPM	-	1SW2, 1SW5
850 RPM	-	1SW3, 1SW5
1150 RPM	-	1SW4, 1SW5
1750 RPM	-	1SW5

If the tachometer used has a gain other than 20.8V/1000 RPM or if the base speed of the drive is other than 500, 650, 850, 1150 or 1750 RPM, then the tachometer input signal must be applied to terminal 3 through a miscellaneous series resistor, Rex, switch 1SW1 must be closed and all others open. The value of Rex may be calculated by the following equation:

$$Rex = \frac{|V_t|\ Base}{80} - \frac{1}{8} \times 10^6 \text{ ohm}$$

Where $|V_t|$ Base is the tachometer generator voltage at base speed.

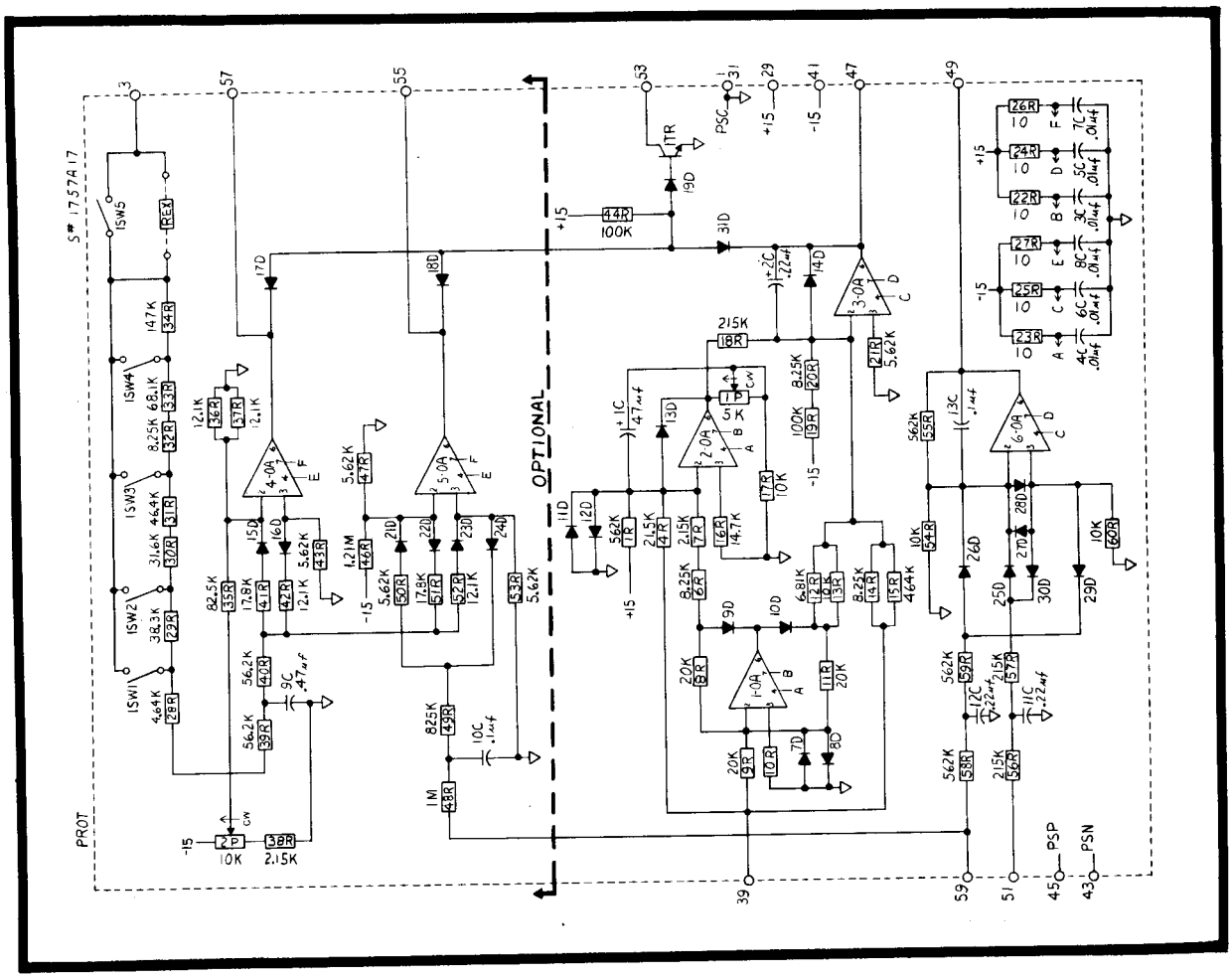

FIGURE III - 16 PROTECTION BOARD

7. Static Sequencer (SEQ.)

Figure III - 17 is a schematic diagram of this board and Figure III - 18 is a relay equivalent of the static sequencer.

The board employs high level logic NAND gates in combination with necessary semiconductors and passive components required for static sequencing. It receives signals from the operators station and permits the drive to perform the required function if the system feedback signals are correct. The sequencer controls the contactor located on the back panel and supplies internal references for the calibration board, the controller board and the field supply.

NOTE: THE DIGITAL INTEGRATED CIRCUITS OPERATE FROM PSC TO THE -15VDC REGULATED SUPPLY. Therefore a logic one is zero volts, & a logic zero is -15VDC with respect to PSC.

The sequencer is capable of supplying the options of jog and thread, as well as the standard run-stop functions. Pin 5 and associated components provide 50mA current sinking capability to energize an optional power supply ready relay. Pins 21 and 23 provide the field economy signals of JOG-only full field and RUN, THD, & JOG full field respectively. Pin 51 monitors the output of the Voltage Sensor located on the Protection board. This in combination with associated components, prevents picking up or dropping out the contactor if there is a large voltage across the motor armature or the ramp function generator is ramping. The static time delay circuit has a fixed drop out time constant of approximately one second after the voltage at pin 51 is more positive than -7.5VDC.

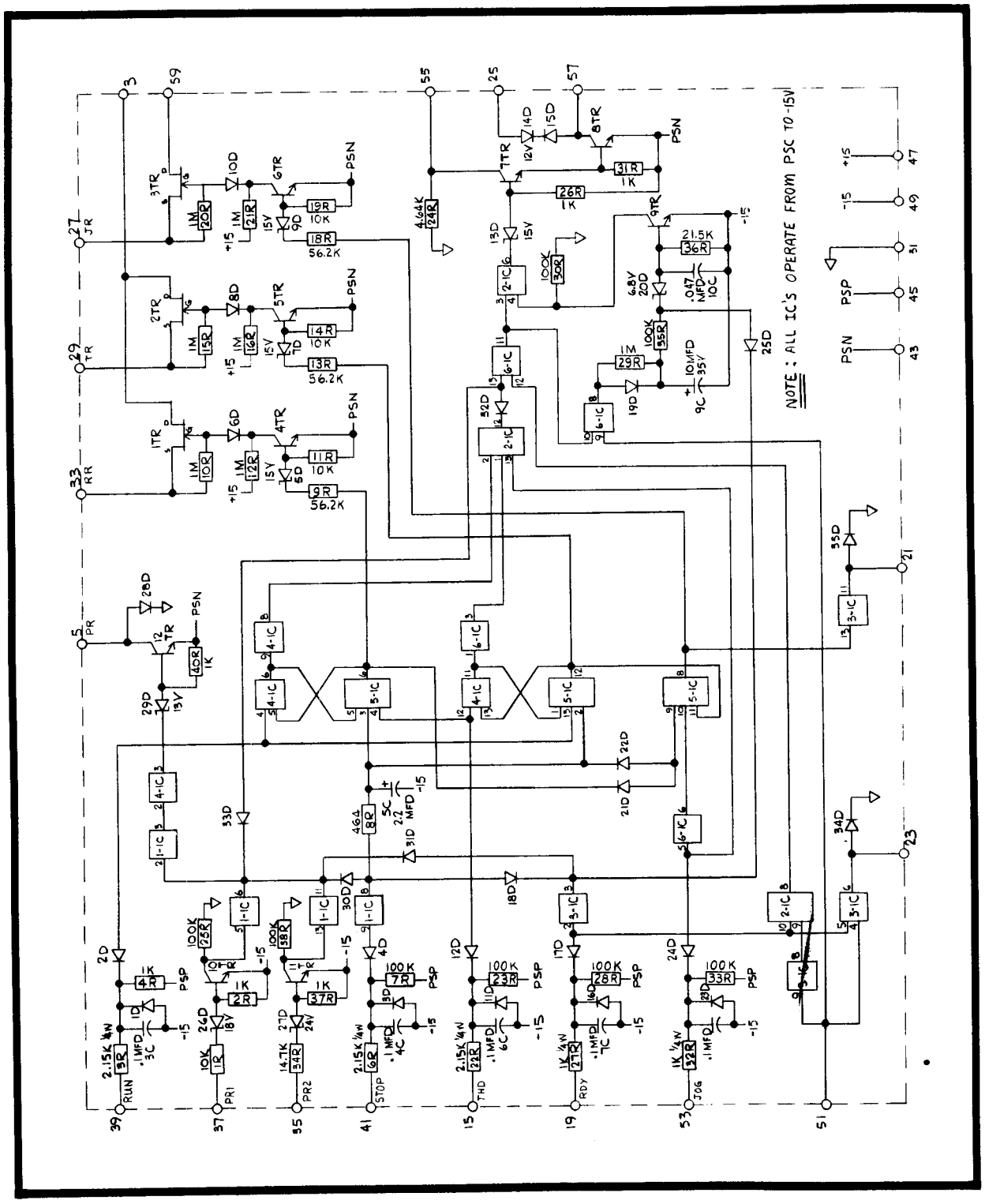

FIGURE III - 17 SEQUENCER

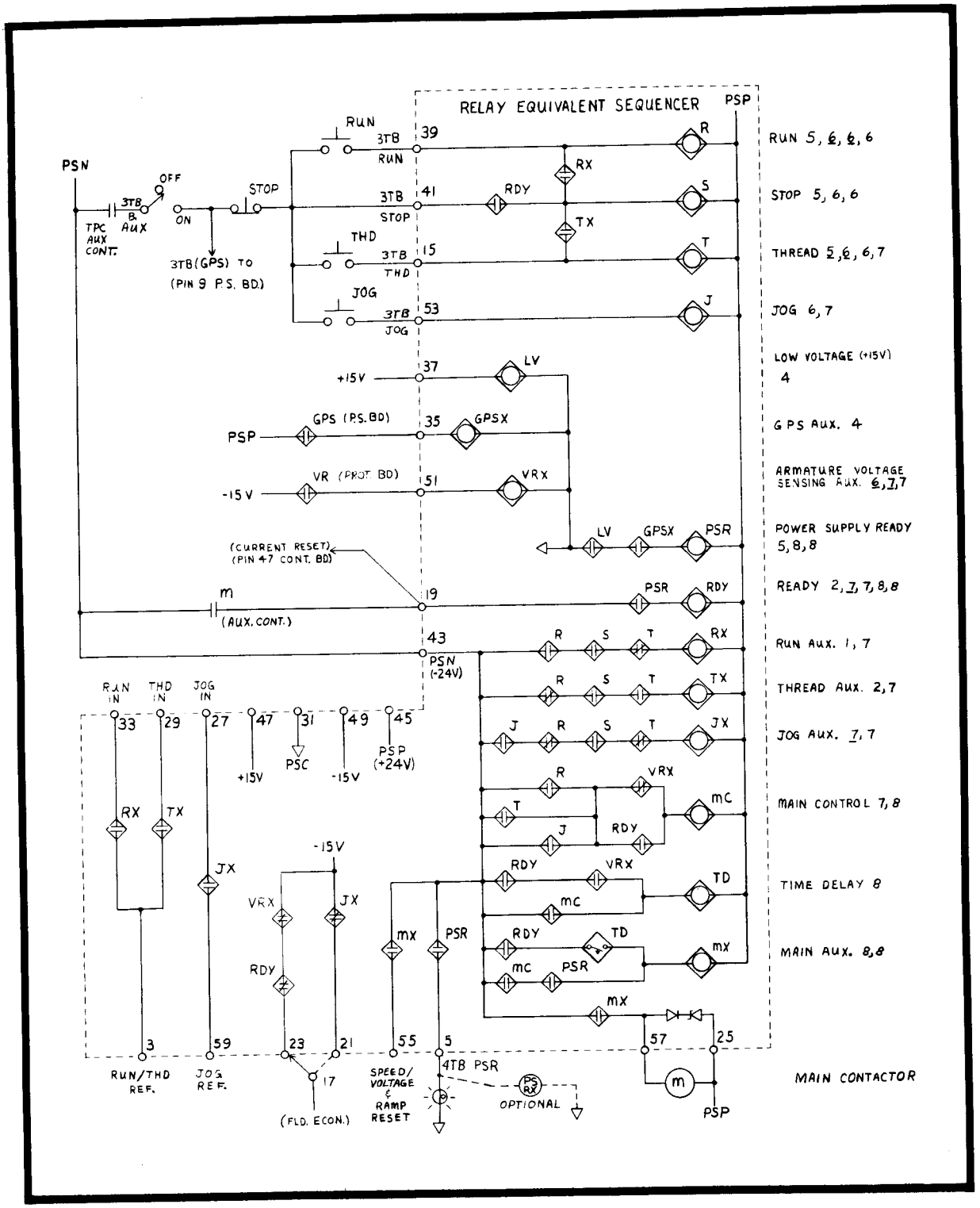

FIGURE III - 18 RELAY EQUIVALENT SEQUENCER

D. Converter Power Circuit Protection

Figure III - 19 shows a single line diagram of the C-600M TPS. The ac voltage is brought from the customer feeder to the thyristor transformer (the customer may use an ac breaker or other disconnect drive in his line). The secondary of the transformer has a single phase tertiary winding used for field excitation. This single phase line has fuses to serve as protective and disconnect functions.

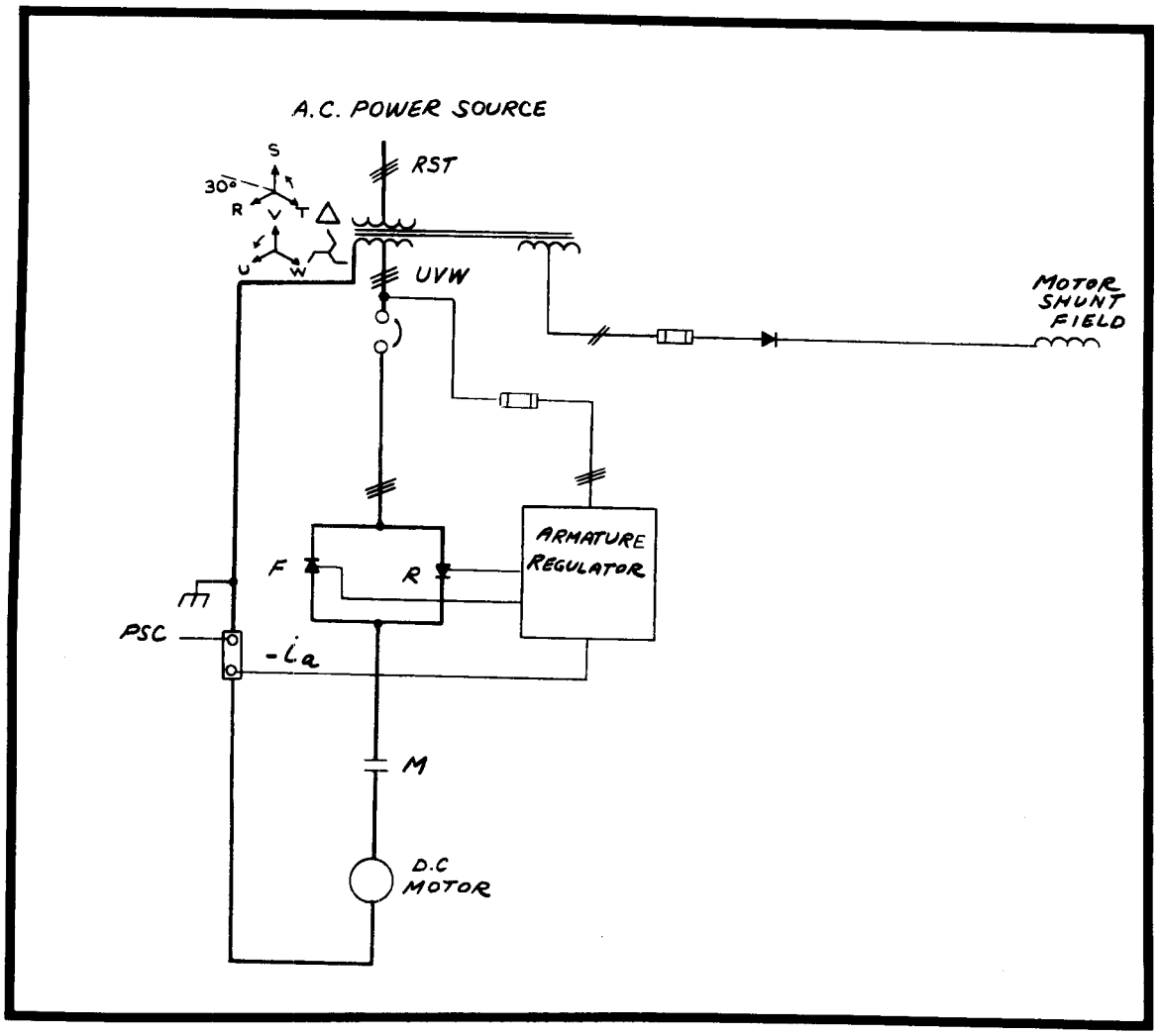

FIGURE III - 19 THYRISTOR POWER SYSTEM

There is a thyristor breaker connected from the secondary of the transformer. This molded-case MCP ac breaker has magnetic trip only, which is set above the current limit rating of the drive. This breaker is coordinated with the impedance of the transformer and serves to protect the thyristors under both ac faults and dc faults (line to line faults and motor to line faults through the neutral of the transformer) should they occur. These faults, by their nature, are of high amplitude but due to rapid magnetic tripping of the breaker are of short duration, and are held below the surge capability of the thyristors.

The shunt provides a current feedback signal to the regulator. The main sequencing device is the dc contactor between the power converter and the dc motor armature. Its main function is to de-energize the motor positively in case of an emergency or if any work is required on the driven machinery.

Normally closed limit switches or other emergency stop interlocks may be inserted in series with the off/on switch and these will drop out the contactor immediately upon initiation, as will operation of the off/on switch, the static overload circuit, the tach loss circuit, the overspeed circuit, or the field loss circuit.

Optional Accessories

The test module (S#1757A16G01) is an option that can be added to the regulator cage to aid in start up and trouble shooting. This module provides an adjustable ±10V test voltage as well as a means of sensing critical voltages. The panel meter used is a zero center meter. A ten position switch, with selected series resistors, allows for monitoring ten differenct voltages with the single meter.

Test module (S#1757A16G02) includes the G01 circuitry plus a load indicator driver and a tachometer signal absolute value generator. The load indicator has outputs of either 0 to 1mA or 0 to 10VDC for an suitable external meter and is adjustable from 100% to 300% load. The tachometer signal generator is provided to drive a zero left volt meter whose full scale deflection is compatible with the maximum tachometer voltage.

F. Rating

1. AC Feeder

Standard power system incoming voltages are 230V and 460V - 60 Hz - 3 phase or 380V - 50 Hz - 3 phase. Tolerance +10%, -5% on voltage, ±5% on frequency.

2. DC Voltages

Standard dc voltages are 240V for 5 HP...20 HP. These thyristor power systems are able to produce the rated dc voltage at 200% current with 95% line voltage.

3. DC Current

The continuous dc current rating of a TPS depends on several factors such as Thyristor transformer, TPM size, ambient temperature, elevation.

Standard ambient temperature range: 0 to 40°C.

Standard elevation limit: 3300 feet above sea level.

TPS continuous current ratings are at rated current for each horsepower at Standard voltage.

Standard transient current rating is 150% for 1 minute.

The thermal overload is set to protect the motor based on 115% of motor full load current.

4. Regulation

For load changes to rated current and line regulation within that specified:

Voltage Regulator	2%
Speed Regulator	0.25% with standard tach

IV. AUXILIARY FIELD EXCITER

Constant potential and variable voltage field exciters can be added to feed the fields of the dc machines which have their armatures powered by the main C-600M power converter.

A. Adjustable Voltage Field Exciter

The auxiliary field exciter consists of a single phase thyristor power module (TPM), a field controller board, and a CEMF sensor board. It is mounted to the armature TPM assembly.

This system is used for field weakening applications in conjunction with a speed regulated armature supply. The field current is held to rated current below base speed and then decreases when the armature voltage tries to exceed its rated (crossover) voltage for speeds greater than base speed.

1. Field TPM

The field TPM is a single phase full-wave semiconverter with freewheeling diode. The semiconductors are protected by a R-C network and a surge suppressor. It is supplied 230V ac power from the single phase tertiary winding of the thyristor transformer. The TPM is rated 180V dc maximum and 6 amperes.

2. Field Controller Board

The C600M field supply is a PI current controller with CEMF crossover. The current feedback signal ($-i_{f1}$) is obtained from a sensing resistor in the field circuit. The sensing resistor is selected such that $-i_{f1}$ is .75V to 2.5V at rated field current. This signal is amplified by operational amplifier 3-OA and associated components. Potentiometer 1P is used to adjust the gain of 3-OA such that its output ($-i_f$) equals 2.0V for rated field current.

The field loss indication is provided by operational amplifier 2-OA and associated components which compare the $-i_f$ signal to an adjustable reference obtained from the wiper arm of 2P. Circuit operation is such that transistor 4TR is turned off when the field current drops below the desired level. This initiates a gate pulse suppression in the armature regulator.

Operational amplifier 1-OA provides the voltage reference for the gate pulse generator. It does this by comparing the current or voltage feedback signals (the output of 3-OA or the output of the CEMF sensor respectively), with the internal command reference originating from either 5TR or the wiper arm of 3P. Potentiometer 3P provides a means of adjusting the field strength during standby operation. For full field operation (FF1 = OVDC) 5TR is turned on. Thus 5TR and the associated voltage divider provide the full field reference.

The gate pulse generator provides gate pulses to the TPM. The phase angle at which the gate pulses occur is determined by the feedback signals. The control power supply for the field exciter is contained on the field controller board in order to maintain proper field control in the event of an armature regulator failure.

ADJUSTMENTS	POTENTIOMETERS	RANGE
Max. Field Current	1P	Adjust for rated current
Field Loss	2P	0 -45% of rated current
Standby Field	3P	0 -50% of rated current

3. Bus Boltage/CEMF Sensor Board

The bus voltage/CEMF sensor is a differential amplifier. Therefore the output of the sensor is a DC signal proportional to the armature voltage. An absolute value circuit is required to provide the same polarity output regardless of the input polarity. The output of the sensor is approximately 2 volts at rated armature voltage.

The sensor board is piggy-back mounted over the field controller board. The control power supplies originate on the field controller, and are connected by means of jumpers at stab terminals PSP, PSC, and PSN. The input (armature voltage) is connected to screw terminals on the voltage sensor, while the input (- CEMF 1) is a stab terminal connected to stab terminal CE on the controller board.

Two types of sensors are available.

a) The standard voltage sensor is merely a bus voltage sensor which has no adjustments. Component values are pre-selected to provide crossover at 220 to 240 volts.

b) The optional CEMF sensor is used for special applications. It provides adjustment of the crossover voltage (1P) and IR Compensation adjustment (2P). The IR Compensation is usually not connected and therefore not used.

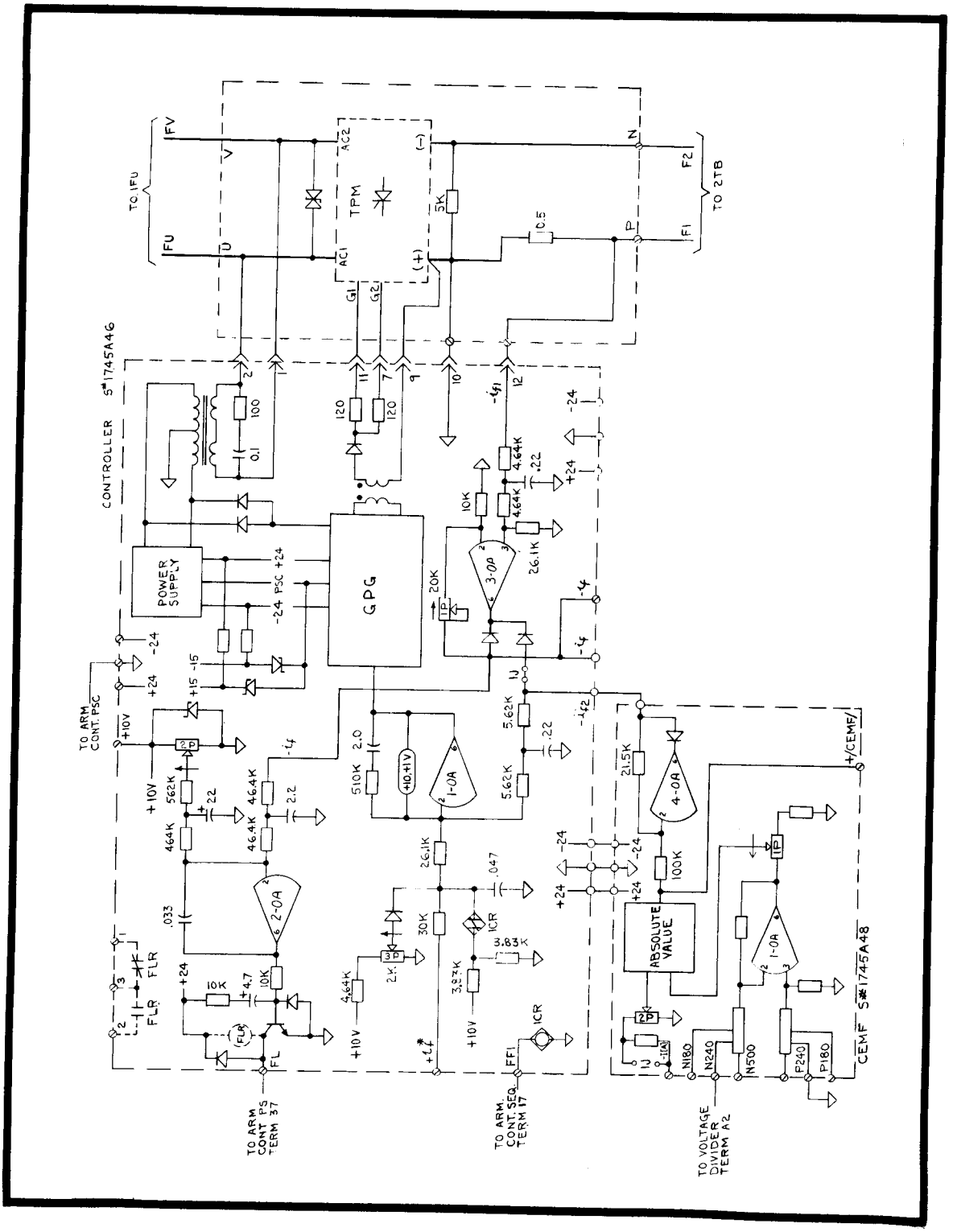

FIGURE III - 20 REGULATED FIELD SUPPLY WITH CEMF CROSSOVER