BASIC SYSTEMS DRIVES

BUFFER AMPLIFIER BOARD S#1781A04

I. INTRODUCTION

This printed circuit card is from the series of cards designed for the BSD MASTER CONTROLLER and BSD DRIVE CONTROLLER functions. Buffering of control signals by inverting and non-inverting amplifiers against overloading is accomplished by this card. Some flexibility in application of this board has been made available and is explained later in this instruction leaflet.

Figure 1 is a picture of the Buffer Amplifier with all its circuits present (G462). However, on a given application only the required circuits are ordered. A front view locating all components by schematic identification is shown on the last page of the instruction leaflet.

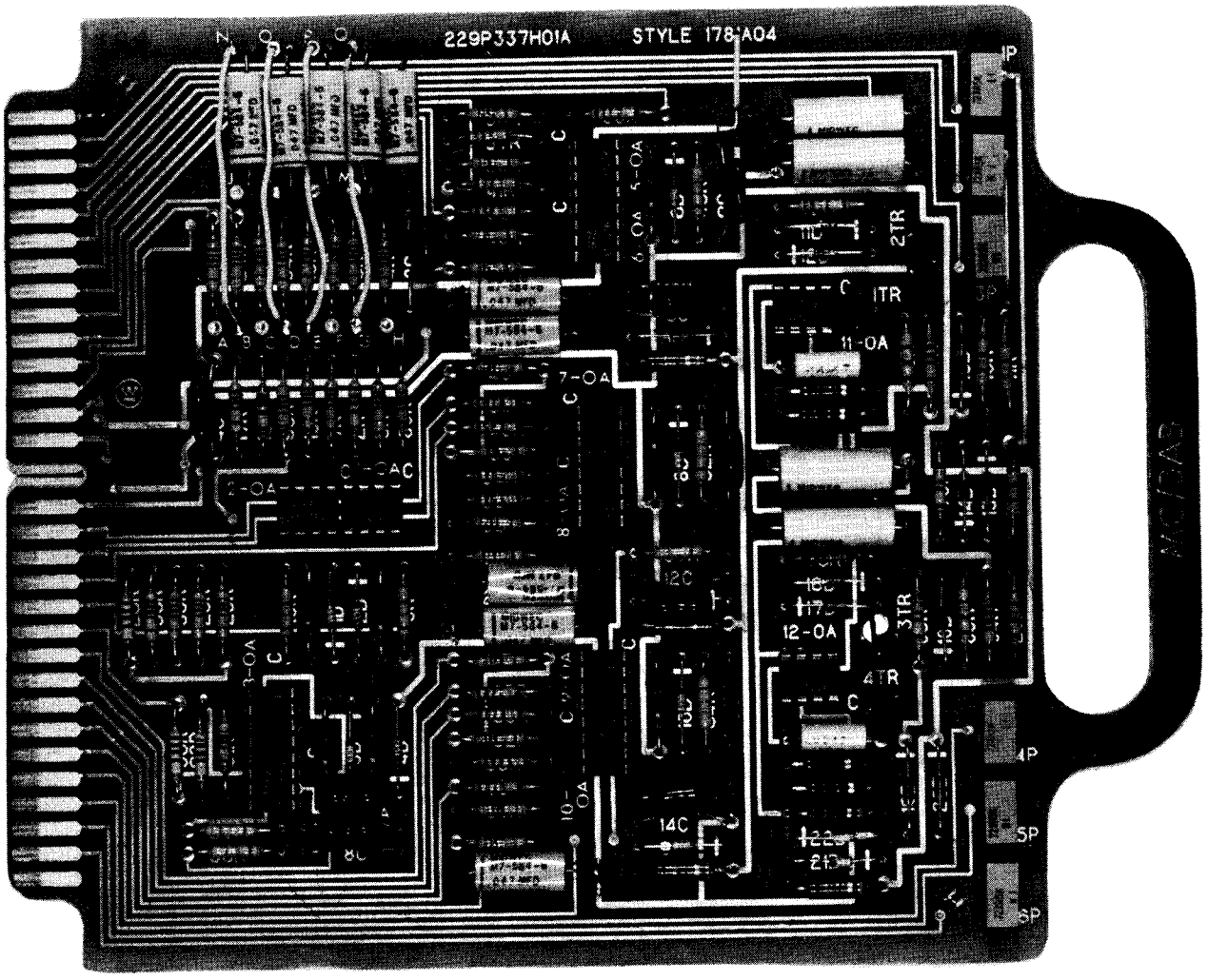


FIGURE 1 PHOTOGRAPH OF THE BAB

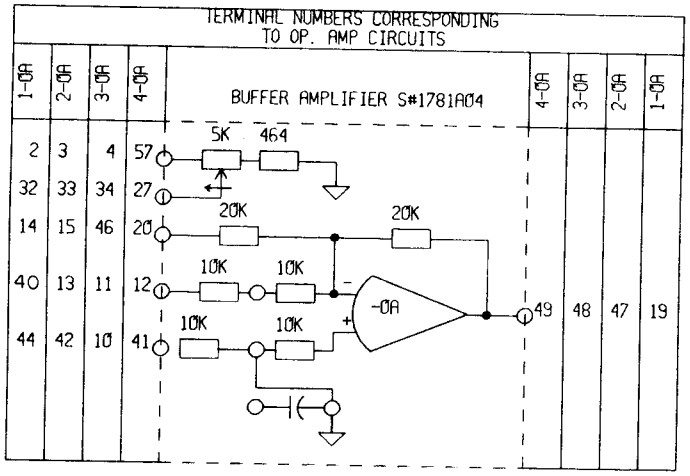


FIGURE 2A. INVERTING SUMMERS - MAX.4

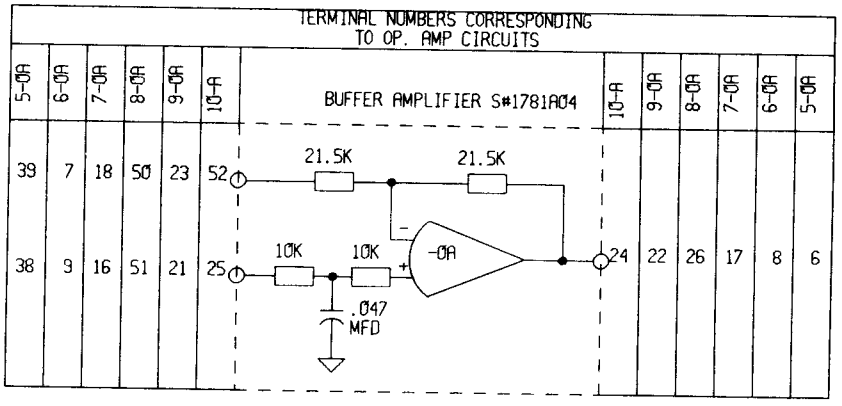


FIGURE 2B. NON-INVERTING BUFFERS-MAX.6

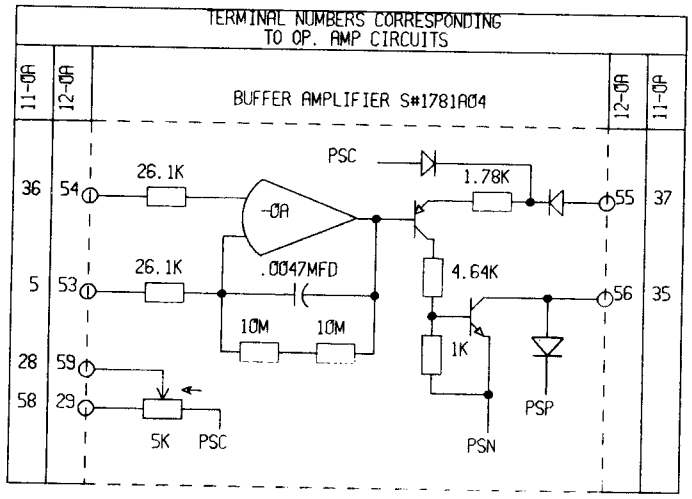


FIGURE 2C. VOLTAGE DETECTORS - MAX.2

SIMPLIFIED SCHEMATIC DIAGRAMS

FIGURE 2

II. DESCRIPTION OF OPERATION

A. Introduction

The Buffer Amplifier Board (BAB) S#1781A04, for a given application, is identified by a three digit group number with each digit indicating the number of duplicate circuits for each of the three functional groups. The hundreths digit represents the number of inverting summers. The tens digit represents the number of non-inverting buffer amplifiers and the units digit represents the number of voltage detectors. For example, S#1781A04G321 refers to a combination of three (3) inverting summers, two (2) non-inverting buffers and one (1) voltage detector. The circuit descriptions are kept general by describing one typical circuit for each of the three functional groups.

B. Circuit Functionalization

Figure 2 consists of simplified schematic diagrams of the three functional blocks available on this board. Each of the figures represents one typical circuit of the maximum identical circuits available. Each of these circuits with application flexibility is described below. The detail circuits for the maximum combination (G462) is given in Figure 3.

B1. Inverting Summers-Maximum 4

There are a maximum of four duplicate inverting summers available as shown in Figure 2a. Each amplifier has an associated set of six terminals, and the appropriate terminal numbers are grouped with the appropriate amplifier numbers. In the group identification 1XX would select amplifier 1-0A; 2XX would select amplifiers 1-0A and 2-0A; etc.

Each circuit consists of an IC741 operational amplifier with ±15V zener type voltage regulated power supply and an output decoupling circuit consisting of a 46.4 ohm resistor and a 100 pf capacitor. As shown in Figure 3, two op amp circuits share one set of zener diodes for power supply regulation. On the standard board, a wire jumper shorts out the non-inverting input to PSC through the 10k resistor. The other two inverting inputs have unity gains. One of these inputs can be attenuated by using the potentiometer resistor circuit as shown in Figure 4a. Other possible applications of this set of circuits are given in Figures 4b through 4f.

B2. Non-inverting Buffers - Maximum 6

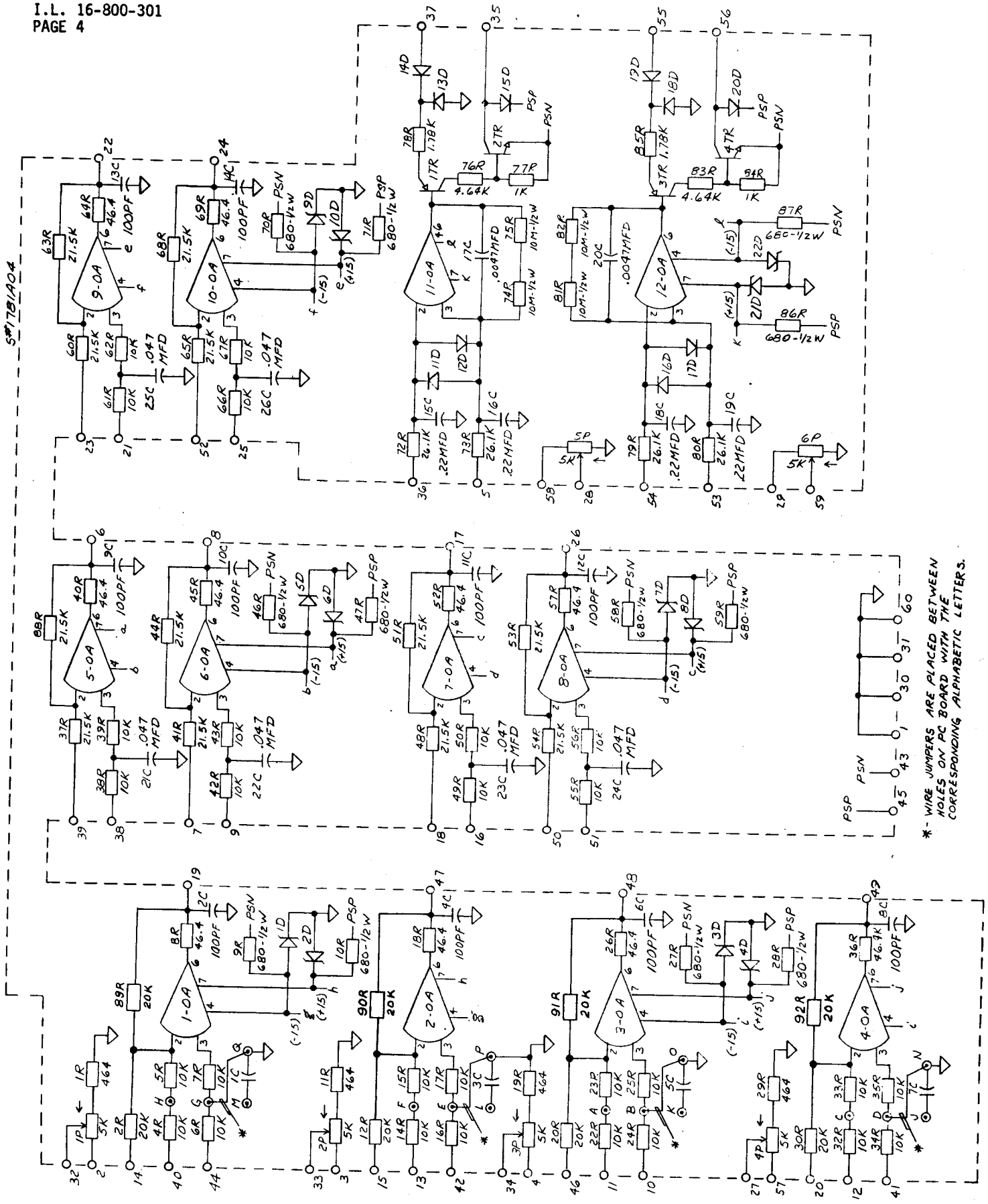
There are a maximum of six duplicate non-inverting buffer amplifiers available as shown in Figure 2b. Each amplifier has a set of three terminals, and the appropriate terminal numbers are grouped with the appropriate amplifier numbers. In the group identification, X1X would select amplifier 5-0A; X2X would select amplifiers 5-0A and 6-0A; etc., up to X6X which would select amplifiers 5-0A through and including 10-0A.

Each circuit consists of an IC741 operational amplifier with ±15V zener type voltage regulated power supply and an output decoupling circuit consisting of a 46.4 ohm resistor and a 100 pf capacitor. As shown in Figure 3, two op amp circuits share one set of zener diodes for power supply regulation. On the standard board, a .047 MFD capacitor provides an input filter of 0.47 ms in the non-inverting input. The inverting input is left open circuit for this application. However, if a gain of 2.0 is required, the 21.5k in the inverting input should be connected to PSC externally as shown in Figure 5a. If the amplifier circuits are to be used in an inverting mode, the .047 MFD capacitor should be replaced with a wire jumper on the board as shown in Figure 5b.

B3. Voltage Detectors - Maximum 2

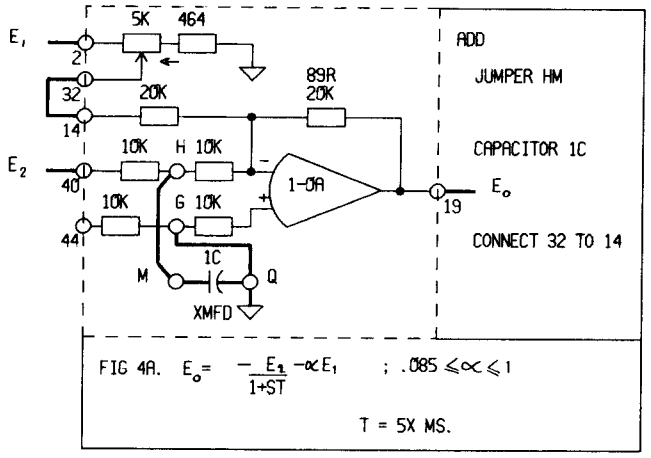
There are a maximum of two duplicate voltage comparator (detector) circuits available as shown in Figure 2c. Each comparator has an associated set of six terminals, and the appropriate terminal numbers are grouped with the appropriate amplifier numbers. In the group identification, XX1 would select amplifier 11-0A; XX2 would select amplifiers 11-0A and 12-0A.

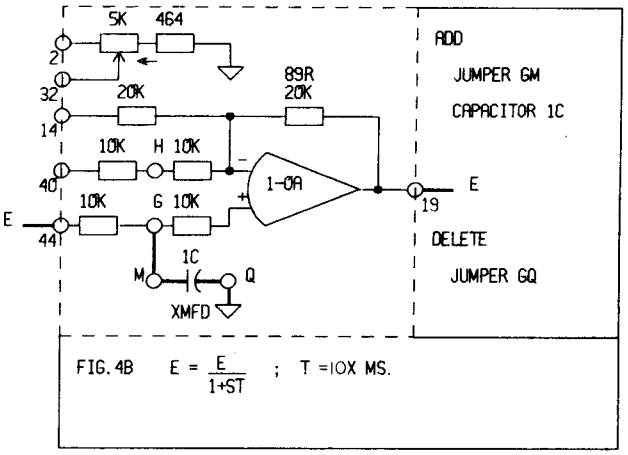
The comparator circuit can be used to determine the relative polarity of two voltages with respect to each other. Refer to Figure 2c. When the voltage at input terminal 36 (54) is negative with respect to terminal 5 (53), the two outputs are non-conducting (transistors off). When the voltage at input terminal 36 (54) is positive with respect to terminal 5 (53), the two outputs are conducting (transistors on). When the output transistor feeding terminal 37 (55) is off, this would correspond to a logic one for either 5V or 15V logic. When this transistor turns on, it represents a logic zero by sinking current from the appropriate logic circuit. When the output transistor feeding terminal 35 (56) is off, this would correspond to a high impedance output. When this output transistor turns on, PSN appears on the output terminal. This transistor driver stage could be used for driving a relay or a FET circuit.

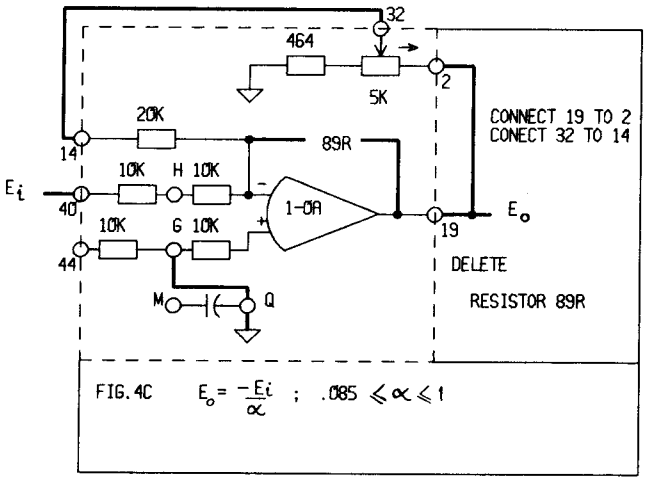


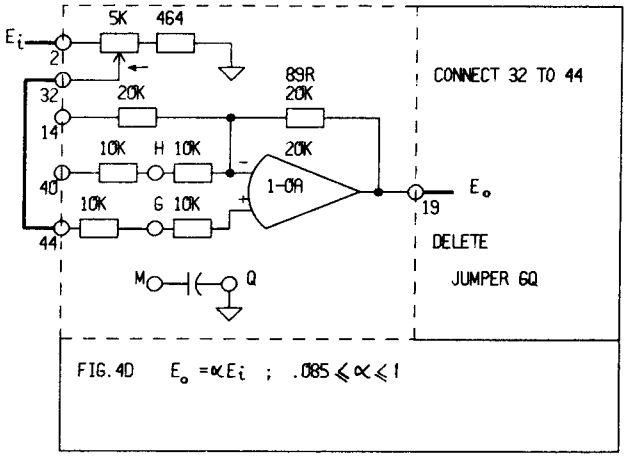
BUFFER AMPLIFIER BOARD

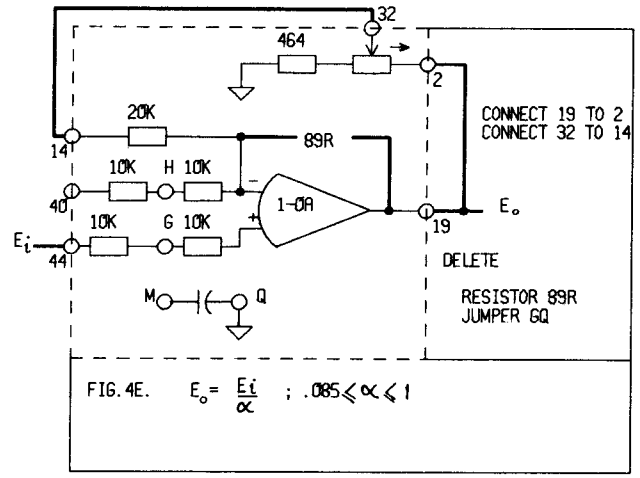
FIGURE 3

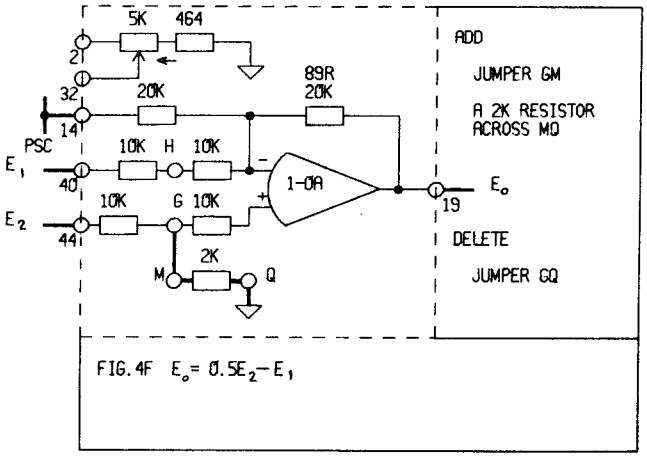






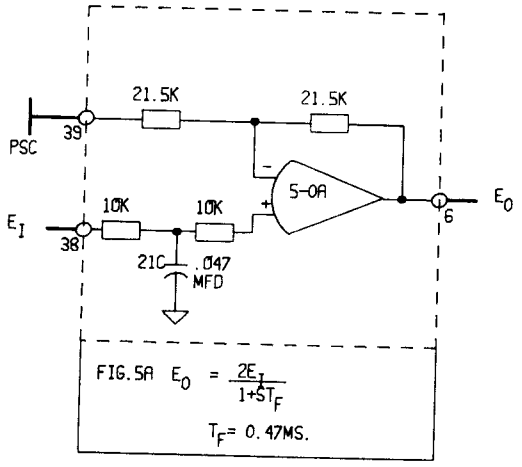


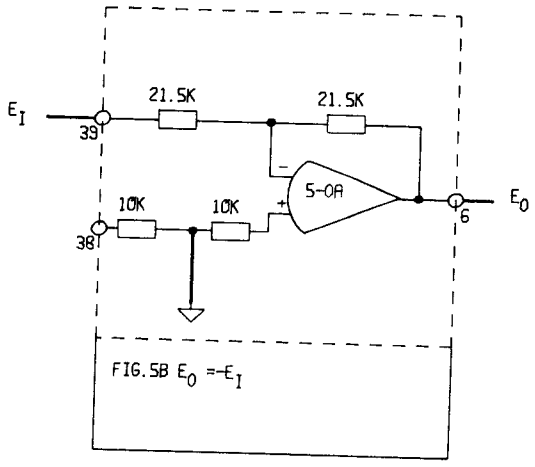




APPLICATION OF OP. AMPS 1-4

FIGURE 4





APPLICATION OF OP-AMPS 5-10
FIGURE 5

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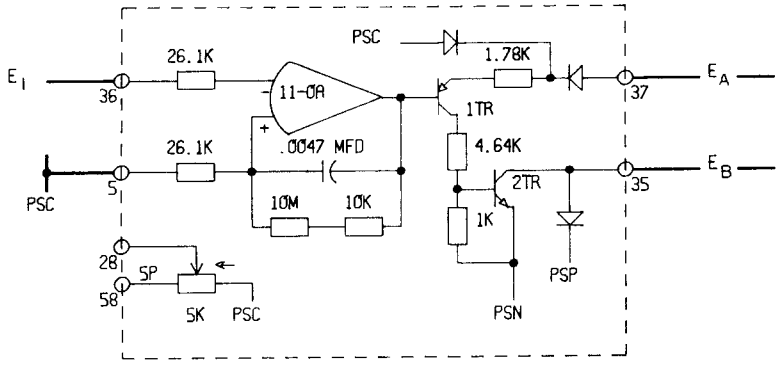


FIGURE 6A - NOT RECOMMENDED

ATTEMPTING TO DETECT ZERO VOLTS

NOTE: FOR ALL THE RECOMMENDED CIRCUITS, INPUTS AT TERMINALS 36 AND 5 SHALL NOT EXCEED 12 VOLTS.

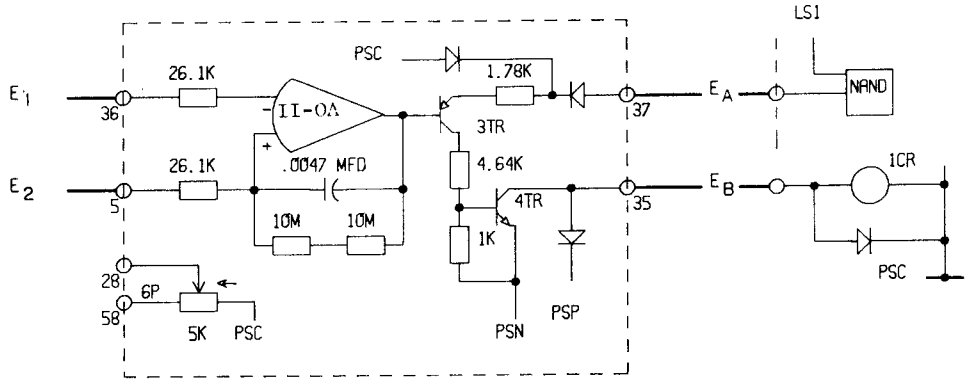


FIGURE 6B - RECOMMENDED

IF $E_1 < E_2$

E_A = 0 TO 0.5V FOR LS1 = "0"
= 6 TO 8V FOR LS1 = "1"

E_B = 0V [1CR DE-ENERGIZED]

IF $E_1 > E_2$

E_A = 0V

E_B = -24V [1CR ENERGIZED]

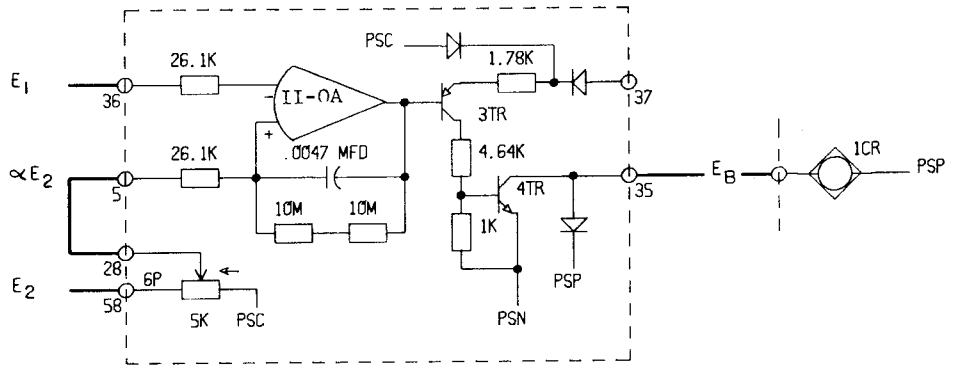


FIGURE 6C - RECOMMENDED

IF $E_1 < \propto E_2$

E_B = +24V

IF $E_1 > \propto E_2$

E_B = -24V

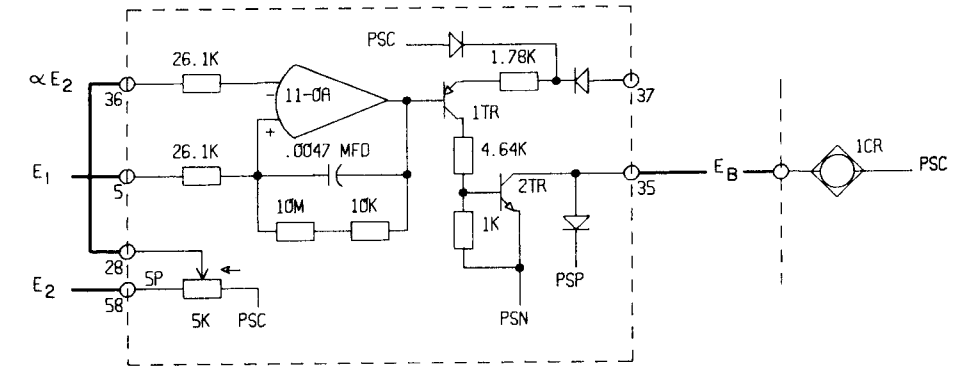


FIGURE 6D - RECOMMENDED

IF $E_1 < \propto E_2$

E_B = -24V

IF $E_1 > \propto E_2$

E_B = 0V

APPLICATION OF DETECTORS
FIGURE 6

The amplifier is used in the differential mode to provide comparison of equal polarity voltages. The input voltage must remain in a voltage band between the IC power supply voltages. The allowable voltage range is ±12V. Hysteresis on the comparator is typically 35mV. Input filters are typically 6ms. Due to hysteresis, detecting zero volts from a unipolarity source is not a recommended mode of operation. Circuit configurations for use of the comparator are shown in Figure 6.

III. CHARACTERISTICS & RATINGS

A. Power Supply Requirements

PSP: +24V ±5% @ 80ma for G462
PSN: -24V ±5% @ 80ma for G462
} plus comparator load current

Current Requirements are 13.3ma/amplifier pair plus load currents on comparator stages.

B. Output Loading for 1-OA through 10-OA : ±12V @ 2.4ma

C. Output Loading for 11-OA & 12-OA

Logic Output

Conducting = 7ma min. at V_{OUT} = 0.5V

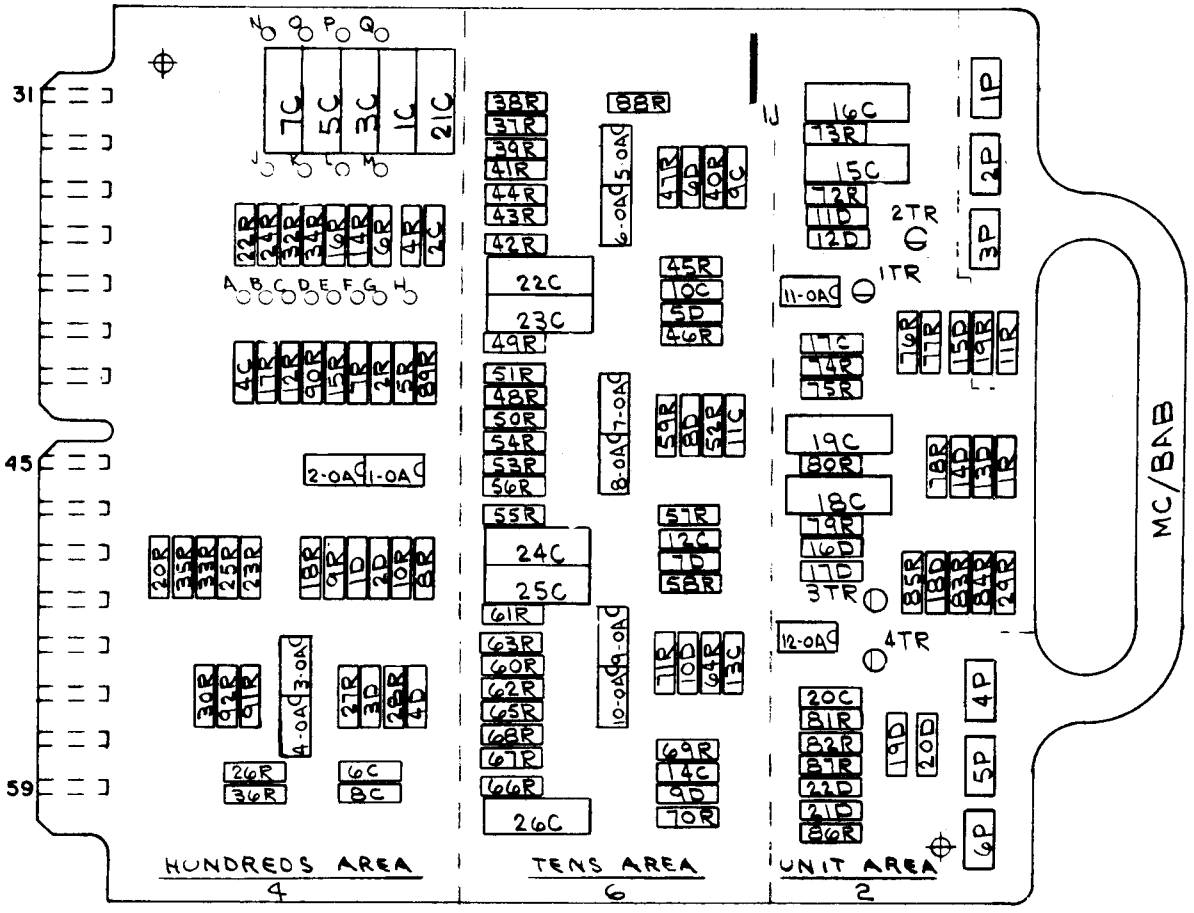
Non-conducting = -0.5ma max. at V_{OUT} = 10V

FET Driver Output

Conducting = 200ma at V_{OUT} = -23V

Non-Conducting = 5μa at V_{OUT} = +24V

D. Allowable Operating Temperature: $0^{o}C$ to $55^{o}C$


31
45
59
HUNDREDS AREA
4
TENS AREA
6
UNIT AREA
2
MC/BAB
2-0A
11-0A
3-0A
4-0A
5-0A
6-0A
7-0A
8-0A
9-0A
10-0A
12-0A
1TR
2TR
3TR
4TR