THYRISTOR GATE DRIVER

I. INTRODUCTION

A general purpose gating system which utilizes a linear ramp for phase control and which can provide phase control ranges of 150^{0}, 180^{0} or 210^{0} is comprised of the Thyristor Gate Driver S#1668A25, the Gate Pulse Generator S#1671A17 and the Gate Synchronizer S#1684A02 (S#1684A05 for 50 hz).

The Thyristor Gate Driver (TGD S#1668A25) amplifies pulses from high level logic elements to a level capable of driving thyristor gates through isolating pulse transformers.

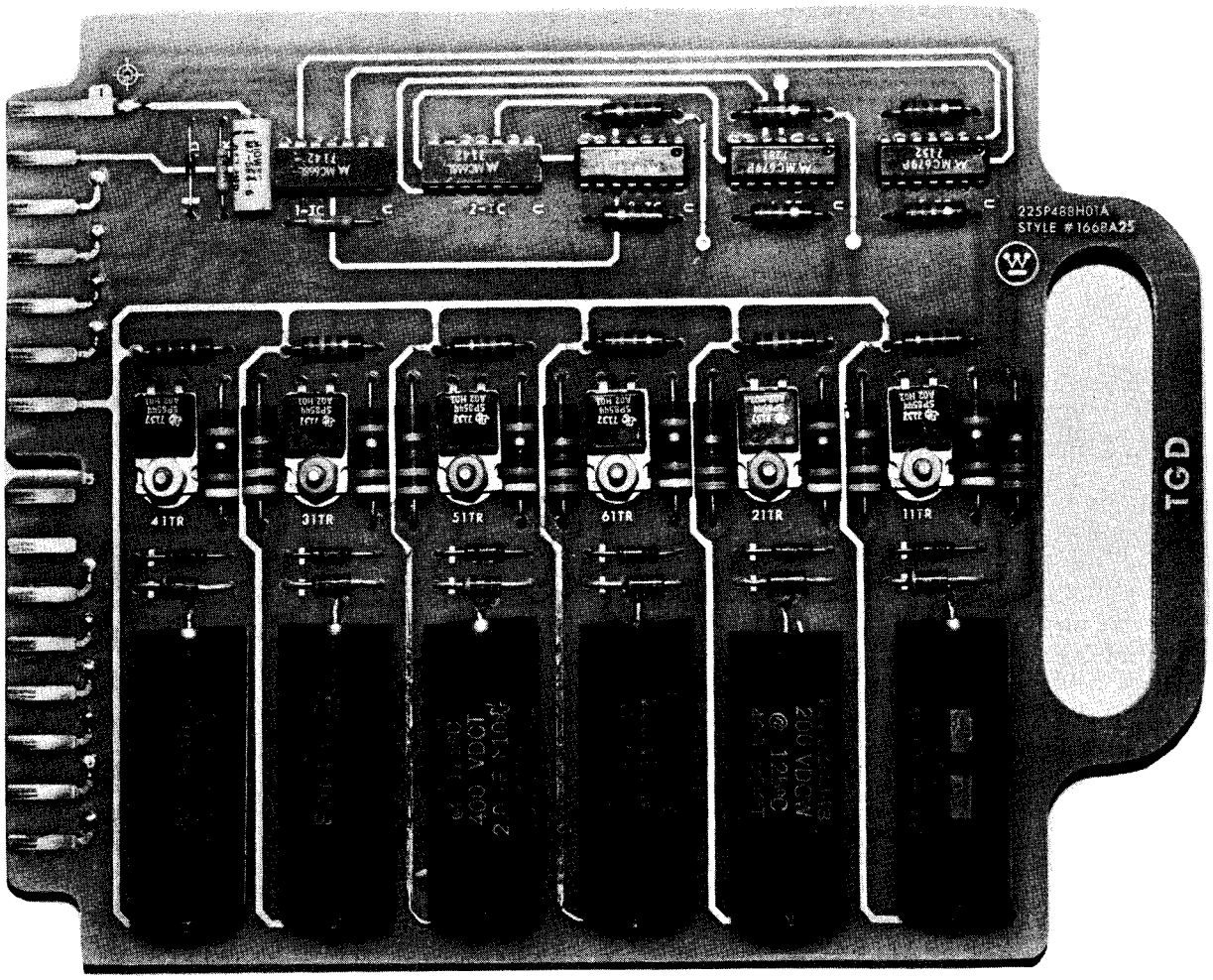


FIGURE 1

Figure 1 is a picture of the TGD. A front view locating all components by schematic identification is shown in the last page of the instruction leaflet. NOTE: Drawing 1668A25 is a multi group assembly and some components will be missing from some style number pc boards.

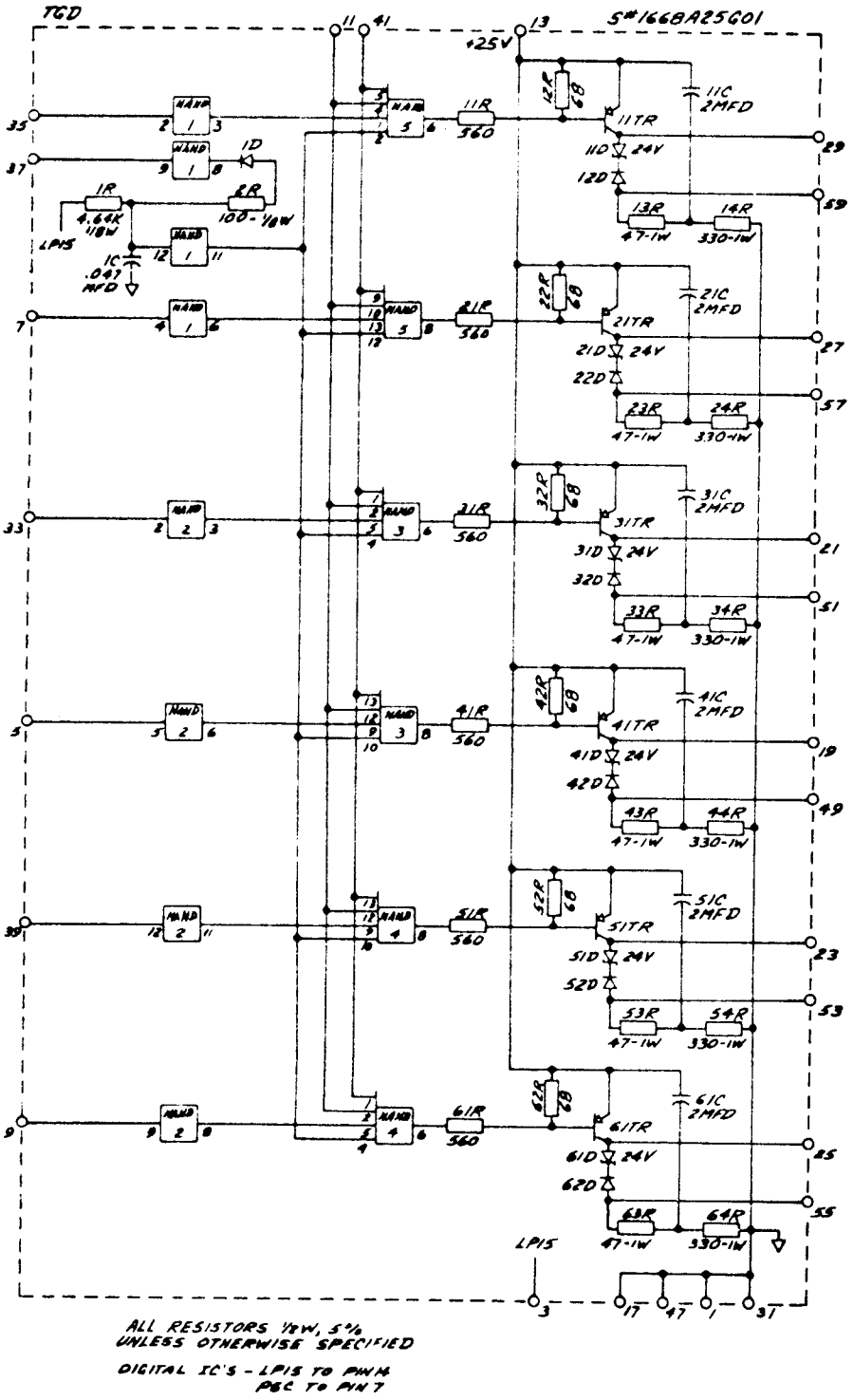


FIGURE 2

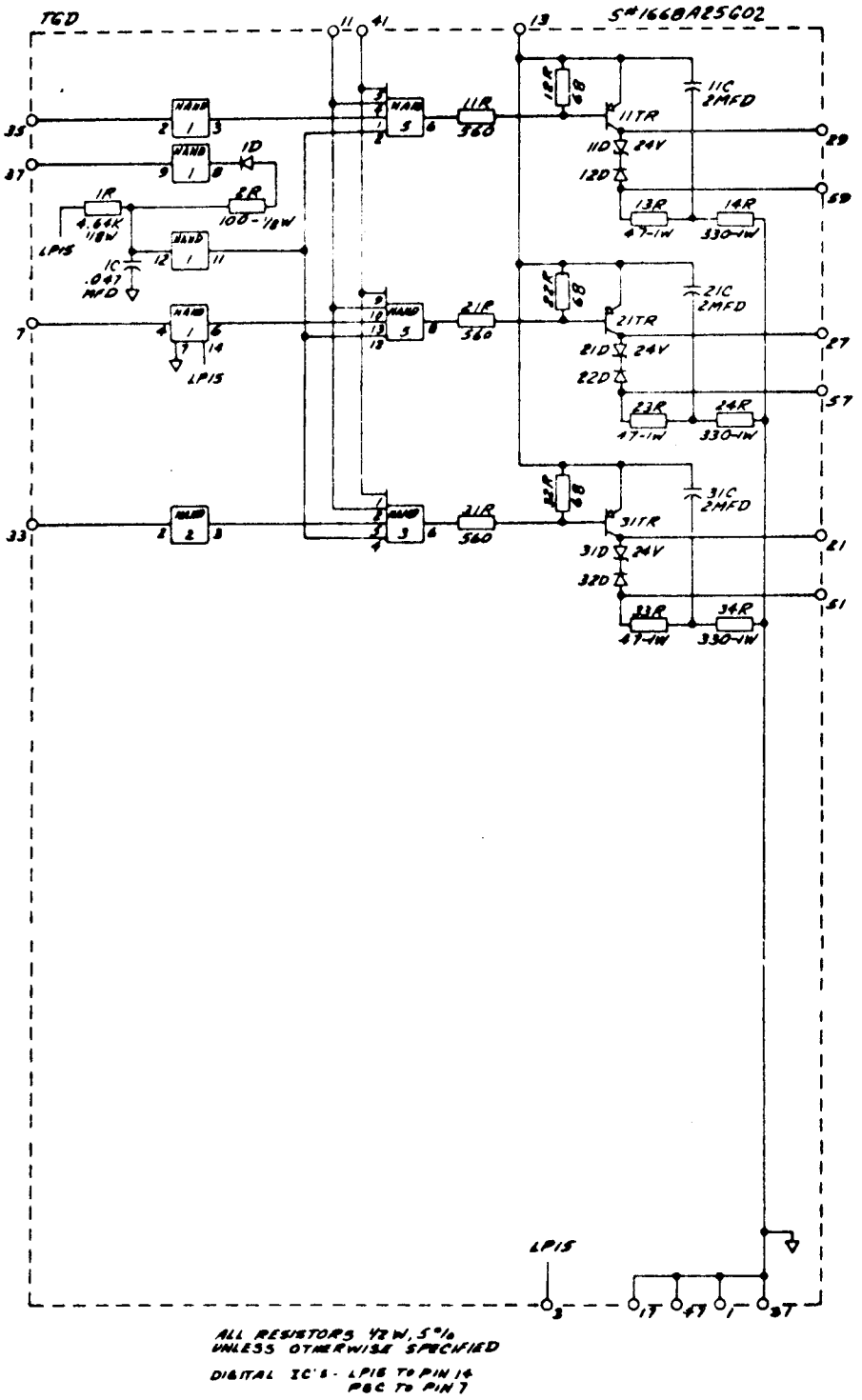

TGD
S#1668A25G02
11
41
13
35
37
7
33
1D
1R
4.64K 1/8W
2R
100-1/8W
LPIS
1C .047 MFD
LPIS
11R 360
21R 360
31R 360
6.8
11TR
11C 2MFD
11D 24V
12D
13R 47-1W
14R 330-1W
21TR
21C 2MFD
21D 24V
22D
23R 47-1W
24R 330-1W
31TR
31C 2MFD
31D 24V
32D
33R 47-1W
34R 330-1W
29
69
27
57
21
51
LPIS
3
17
47
1
37
ALL RESISTORS 1/2W, 5%
UNLESS OTHERWISE SPECIFIED
DIGITAL IC'S - LPIS TO PIN 14
PSC TO PIN 7

FIGURE 3

II. DESCRIPTION OF OPERATION

A. INTRODUCTION

This is a general purpose thyristor gating circuit which amplifies a 0 to 15V input logic signal to the level required to drive one pulse transformer (S#1669A74). The externally mounted pulse transformer isolates the signal and couples it to the gate of the power thyristor. Six or three driver stages are provided on each printed circuit board. All stages are connected to one gate pulse suppression (GPS) line and two inhibit (INH) lines.

B. DRIVER CIRCUIT

1 Gate Signal

The periodicity of the signal applied to the pulse transformer is a function only of the input signal; however, the output amplitude is of the form of an exponential decay. This shaping provides a nigh current, high voltage leading edge on the pulse for hard firing the power thyristor. The remainder of the pulse train decays to a lower level, thus reducing gate dissipation in thyristor while insuring that it is gated ON. The rise times of the output pulses are in the sub-microsecond region.

2 Driver Operation

The TGD was designed primarily for use in picket fence gating systems but can be applied to single pulse systems, provided no power dissipation limits are exceeded. For purposes of illustration a picket fence pulse train will be assumed to be the input signal. One driver stage is shown below in Figure 4; the GPS line and the two inhibit lines are omitted for clarity but they are assumed to be a logic 1. Note that the Driver NAND has an open collector output transistor.

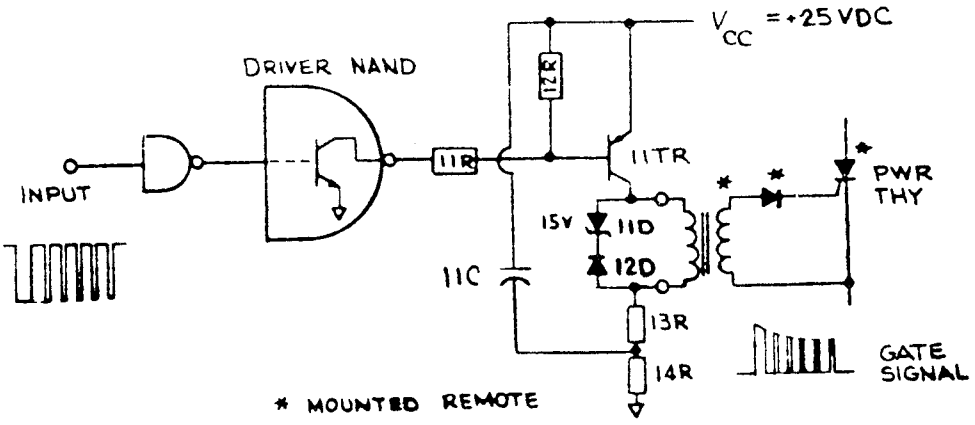


FIGURE 4

A logic 1 at the input, which is the same as the input open circuited, results in a logic 1 at the output of the driver NAND which cuts off transistor 11TR. When a logic 0 is applied at the input, the open collector transistor of the driver NAND pulls resistor 11R low, turning ON transistor 11TR.

Before the long first pulse of the picket fence train, capacitor 11C has been fully charged to the power supply voltage (+25). Thus the initial current through the transformer primary is limited by resistor 13R only, therby applying the high power leading edge of the pulse train to the thyristor gate. As more of the picket fence pulses follow, the capacitor is discharged to the level set by the voltage divider formed by 14R and 13R plus the transformer impedance. This reduces the voltage and current of the gate signal. Hence the exponential envelope of the pulse train.

Diode 12D and zener diode 11D clip the flyback voltage of the pulse transformer thus protecting transistor 11TR from excessive voltage. The 24 volt zener, 11D, allows enough voltage across the pulse transformer secondary for it to reset between pulses.

C. Gate Pulse Suppression

The GPS function has a built in time delay which prevents suppression of the pulses at the driver NAND for approximately 100 μS after a logic 0 appears at the $\overline{GPS}$ input. This is done so that the thyristor will receive any previously initiated hard gate pulse. This in turn assures that the thyristor can be fully turned ON to carry the fault current which started the gate pulse suppression. After the time delay a logic 0 is applied at the input of the driver NAND which turns OFF transistor 11TR and holds it this way as long as gate pulse suppression is activated: i.e., $\overline{GPS}$ = 0.

D. Inhibit

Two inhibit lines ($\overline{INH\text{-}1}$ and $\overline{INH\text{-}2}$) are provided for two purposes.

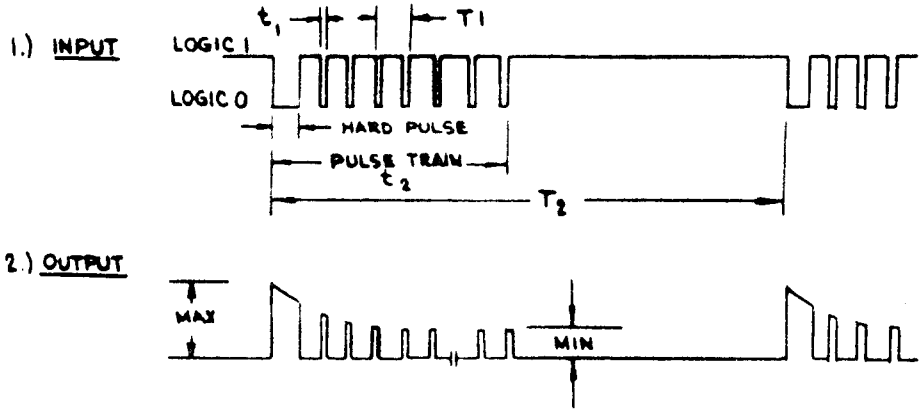
1. At the time power is applied to the system it is desirable to prevent any extraneous gate pulses from reaching the thyristor.

2. To provide the ability to turn OFF all of the gate pulses independent of gate pulse suppression. When $\overline{INH\text{-}1}$ or $\overline{INH\text{-}2}$ are a logic 0 no gate signal will be applied to the power thyristor.

   It is important that any of the unused inhibit lines $\overline{INH\text{-}1}$ or $\overline{INH\text{-}2}$ be tied to LP15 to insure that they will be at logic 1.

III. CHARACTERISTICS AND RATINGS

A. Waveform



B. Definitions

Logic level 1:	+12.5 to 15 volts
Logic level 0:	0 to +1.5 volts
Pulse duty cycle:	t_1/T_1 nominally 25%
Pulse Train duty cycle:	t_2/T_2 nominally 33%
Overall duty cycle:	$t_1 t_2/T_1 T_2$ nominally 8.3%

C. Input Lines

1. Absolute Maximum Ratings

Width of hard pulse	80 µS
Pulse duty cycle	40%
Pulse Train duty cycle	100%
Overall duty cycle	35%

2. All input signals must be compatible with High Threshold Logic IC's, see drawings 1600A68 or 1600A79.

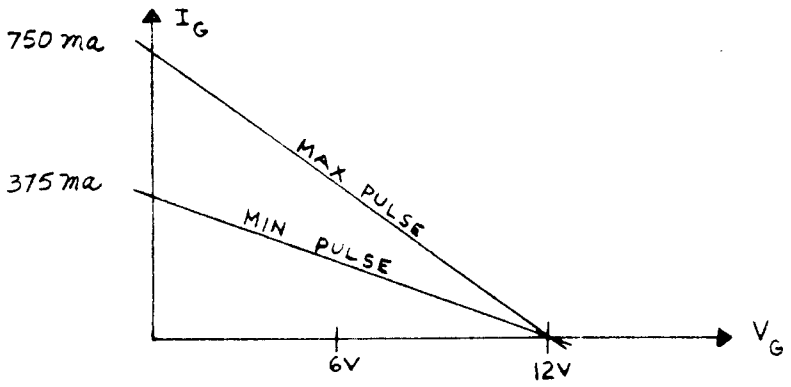
3. Input Load Factors

Pulse 1 through Pulse 6 (Pins 35, 7, 33, 5, 39, 9):	1
$\overline{\text{GPS}}$ (Pin 37)	1
$\overline{\text{INH-1}}$ (Pin 11)	6
$\overline{\text{INH-2}}$ (Pin 41)	6

D. Output

Designed to drive pulse transformer S#1669A74

Output Load Line (Gate Signal)



E. Misc.

Gate Pulse Suppression delay 30 to 120 μS

Gate pulses are suppressed when $\overline{GPS}$ (Pin 37) = Logic 0

or $\overline{INH\text{-}1}$ (Pin 11) = Logic 0

or $\overline{INH\text{-}2}$ (Pin 41) = Logic 0

F. Power Supply

+25	(Pin 13)	24V ± 10% = 125 mA*
+14	(Pin 3)	15V ± 5% = 30 mA*

*These ratings are for 120^{o} long picket fence trains.

G. Operating temperature range: 0 to $+55^{o}$C.

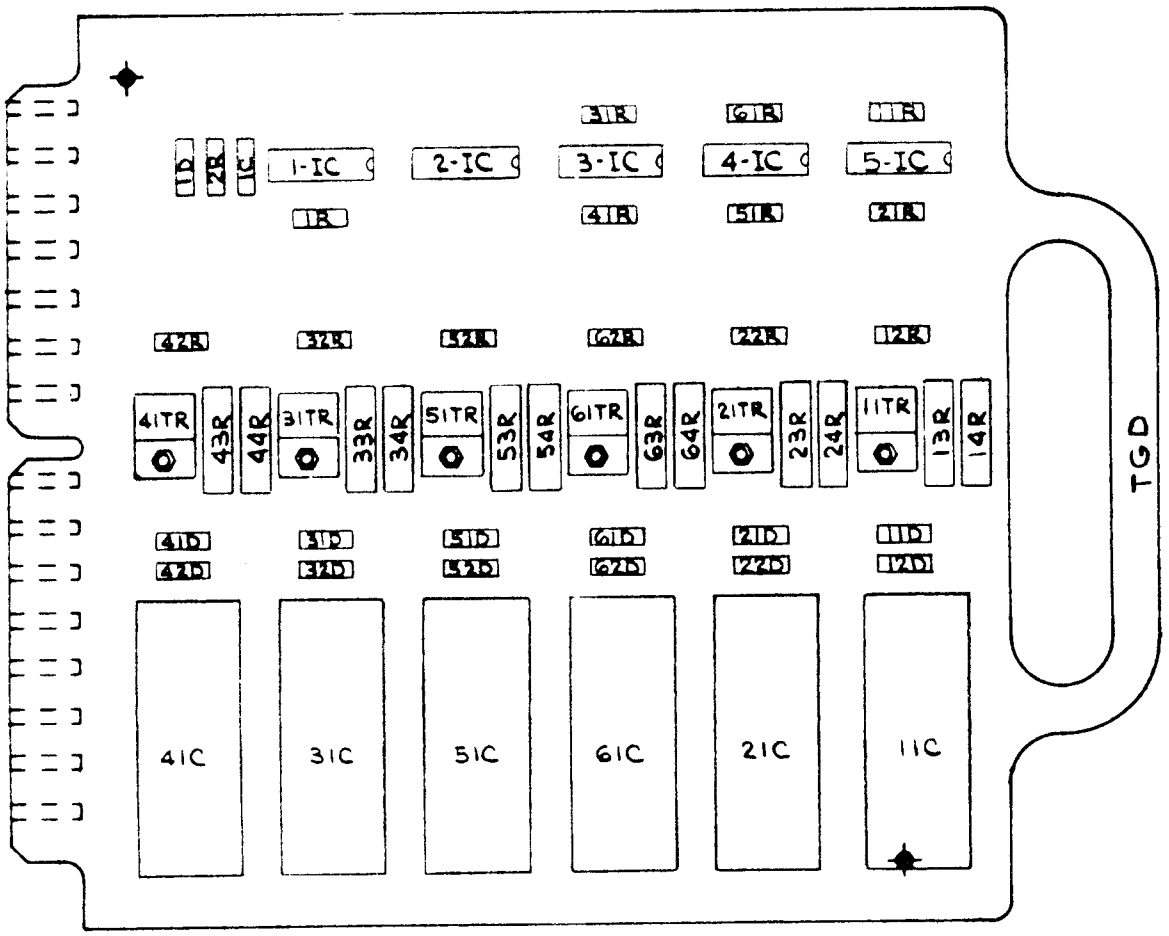


FIGURE 4