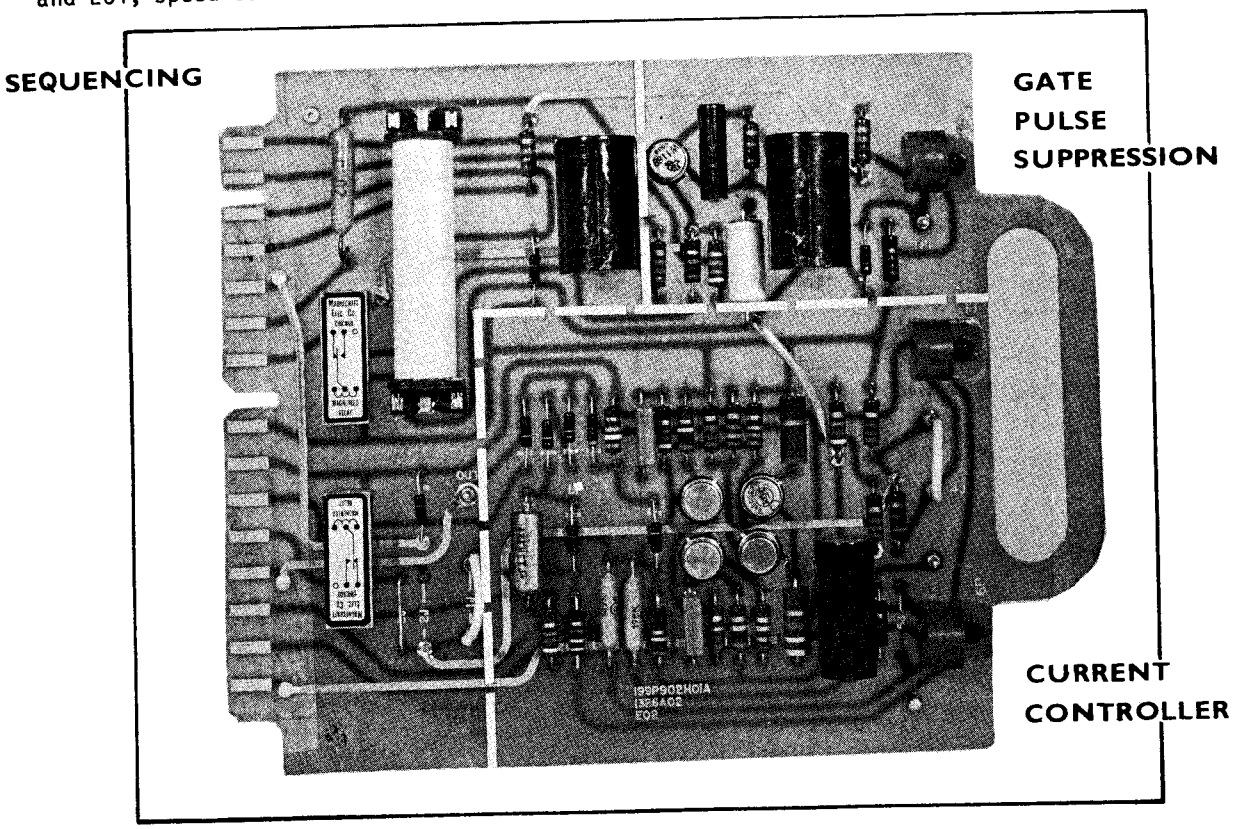
E02 CURRENT CONTROLLER & GATE PULSE SUPPRESSION
For Use in S-56

I. INTRODUCTION

The current controller and gate pulse suppression card (E02) is one of four printed circuit cards comprising basic armature regulators for S-56 systems. Other standard cards, explained in separate instruction leaflets, are: E01, gate pulse generator; E03, voltage controller; and E04, speed controller and ramp-function generator.



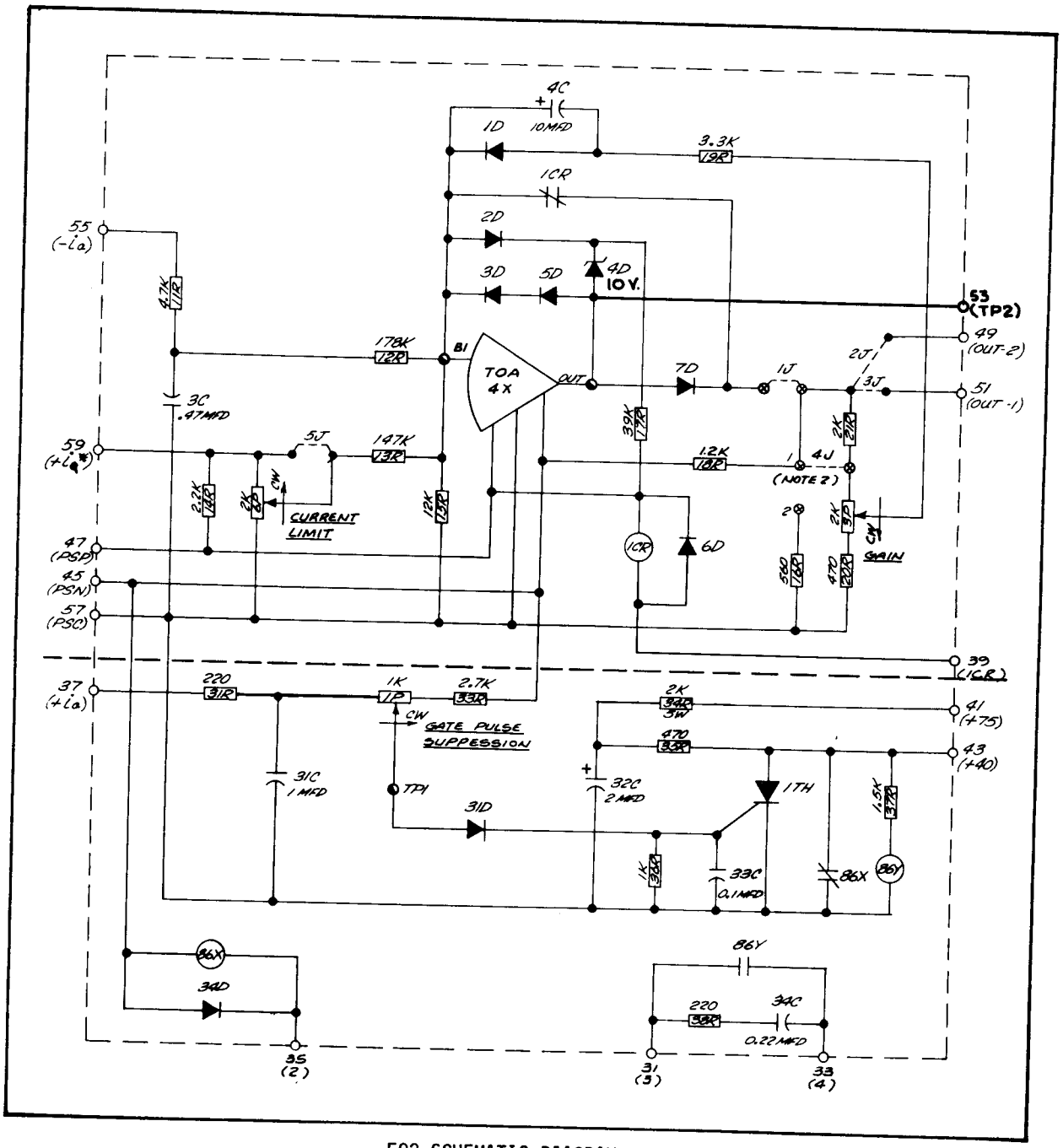
E02 PC CARD
FIGURE 1

Figure 1 is a picture of the E02 pc card as used in speed regulators. By adding or eliminating components, and changing jumper positions, the same board is used in all S-56 basic armature regulators. Dotted lines delineate the three functions provided by the card which will be explained later in the I.L.

Printed circuit cards designed for S-56 systems are plug-in cards for insertion into AMP connector-type number 67131-1 or equivalent. Each card type (designated by "E" number) is uniquely keyed to prevent insertion in improper regulator positions. Over-all board dimensions are 6" X 7.6". A handle is machined in the card which facilitates insertion or removal, and prevents inadvertant component breakage or board contamination. All electrical inputs and outputs are taken through the 15 terminals located at the rear edge of the card. Reading from the top of the pc card to the bottom, terminals will always be identified on schematics by numbers 31, 33, 35, 37,.....59. Potentiometers required for system adjustments are right-angle pots located along the front edge of the pc card.

II. DESCRIPTION

The three functions provided by the E02 card were outlined on Figure 1 and will be explained with reference to the schematic diagram, Figure 2.



E02 SCHEMATIC DIAGRAM
FIGURE 2

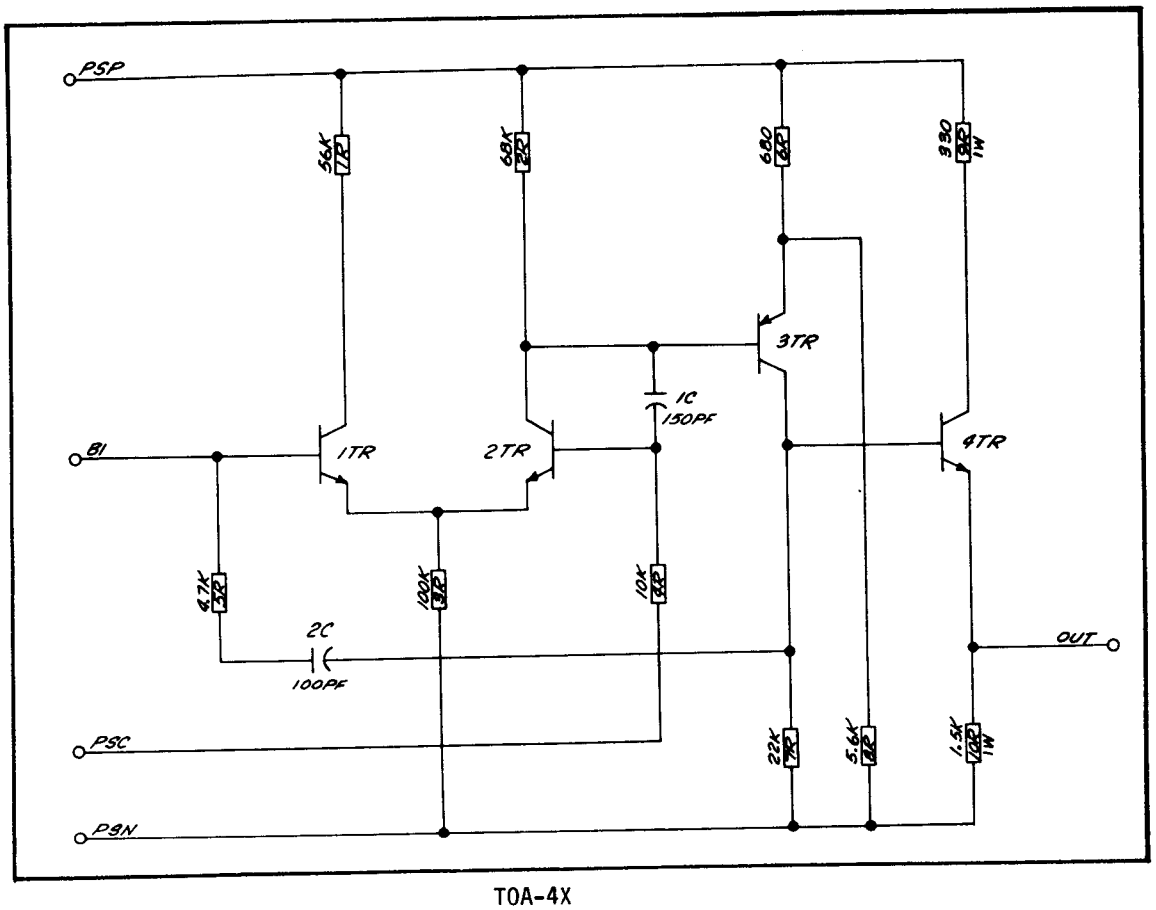
A. Current Controller

DC amplifier (TOA-4X) and associated feedback components comprise the current controller used

in S-56 parallel regulators. A general discussion of operational amplifiers is contained in I.L. 16-800-48.

1. TOA-4X

Figure 3 is the schematic diagram of TOA-4X.



TOA-4X
FIGURE 3

With the base of 2TR connected through 4R to PSC, a signal voltage applied to B1 is amplified by three stages. The first stage is a differential amplifier consisting of 1TR and 2TR, the second stage is the inverting amplifier 3TR, and the final stage 4TR is an emitter follower for the required current gain. Signals are inverted, plus input to B1 will yield a negative output from OUT, and an open-loop dc gain of approximately 2000 is achieved by the three stages.

Capacitors 1C, 2C and their associated resistors serve as shaping networks to optimize the frequency and phase-shift characteristics of the amplifier.

2. Controller Function

Feedback components associated with TOA-4X (see Figure 2) commit its use as a PI controller. The general form of the transfer equation is:

$$\frac{e_{out}}{e_{(-i_a)}} = - \frac{1 + T_{cc}p}{KRiCp} = - \frac{[1 + (19R + \alpha)p]}{(K \cdot 12R \cdot 4C)p}$$

$K \leq 1$

α is dependent on the setting of 3P.

To prevent the amplifier from saturating the output voltage is limited to +1 volt by 3D and 5D, and -10.5 volts by 2D and zener diode 4D. 7D is the switching diode for the current controller, while 18R provides reverse biasing for all switching diodes in the parallel regulator. (Refer to I.L. 16-800-100 for general information on parallel controller operation.) 1D prevents reverse voltage from being developed across electrolytic capacitor 4C.

With the minor changes shown in Figure 4, the E02 board is used in voltage, speed, and current regulators.

Style No.	Use For	Items Eliminated	Jumpers Used
1326A02G01	Voltage Regulator	None	1J, 2J, 4J
1326A02G02	Speed Regulator	None	1J, 3J, 4J
1326A02G03	Current Regulator	14R, 6P	1J, 2J, 4J, 5J

FIGURE 4

When used in voltage or speed regulators, the current controller provides a vertical current limit function adjustable by 6P. In current regulators, 14R and 6P are eliminated, 5J is added and an external current reference signal is brought in to terminal 59. In all regulators, a signal proportional to armature current is brought in to terminal 55 and compared with the reference signal.

1J is a removable board jumper which disconnects the current controller and allows performance of speed or voltage loops to be independently checked. (The E02 board must be reinserted to check performance of speed or voltage controller as reverse bias for all switching diodes is provided through 18R.) 4J is also a removable board jumper and sets the range of gain adjustment by 3P.

2J and 3J are fixed board jumpers which allow the same external wiring harness to be used regardless of the type of regulator.

3. Characteristics and Ratings

a. Allowable operating ambient range: 0 to 55°C.

b. Output: $V_{OUT\ (53-57)}$: -10.5 ±0.7 volts
+1.0 ± 0.4 volts

$I_{OUT\ max.}$ = 5 ma.

c. DC power requirements (including reed relays and gate pulse suppression circuit):

+24V ±1.2V --- 75 ma maximum
-24V ±1.2V --- 75 ma maximum.

d. Gain adjustment by 3P: 4J position 1 --- $5 \geq \frac{1}{K} \geq 1$

4J position 2 --- $25 \geq \frac{1}{K} \geq 5$.

e. Loading effect of gain pot 3P on T_{cc}: $\frac{1}{K} = 1$; T_{cc} = 33 msec.

$\frac{1}{K} = 2.5$; T_{cc} = 39 msec.

$\frac{1}{K} = 12.5$; T_{cc} = 43 msec.

f. Current limit: (when applicable)

Adjustable by 6P from zero to the point of vertical current limit required by the system.

B. Gate Pulse Suppression

Gate pulse suppression is used regardless of the type of basic armature regulator. The schematic diagram consists of all components below the horizontal dotted line on Figure 2.

Positive 75V at terminal 41 originates from a three-phase bridge rectifier physically located on the gate pulse generator (E01) printed circuit card. Normally 1TH is in the forward blocking state and by voltage divider action, +40V is returned from terminal 43 to the E01 board allowing generation of gate pulses for thyristors in the armature semiconverter.

A signal proportional to armature current feeds terminal 37, and 1P adjusts the gating of 1TH to a predetermined fault current level (at least 25% greater than the drive current limit setting). Once gated, the voltage at terminal 43 is the forward drop of 1TH, (0.5V), preventing further production of gate pulses by the E01 pc board.

By inhibiting further production of gate pulses, failure of devices is limited to the thyristor in conduction when the fault occurs, the two bridge diodes it may conduct with, and associated line fuses. In many fault conditions, circuit impedance restricts the rate of current increase such that gate pulse suppression protects all devices.

C. Sequencing

Three dry reed relays are mounted on the E02 card and provide the following functions:

1. 1CR resets the integrating capacitor 4C by providing a quick discharge path when the drive is turned off. As controllers are parallel connected in S-56, reset for all modules with an integral function is provided by the single relay contact.

2. 86Y is provided to sequence the drive off in the event of gate pulse suppression.

3. 86X is provided to reset thyristor 1TH after gate pulse suppression. As 1TH is always forward biased, once gated on it continues to conduct until 86X is de-energized. Closure of 86X contact shunts current from the thyristor, and when it reaches a value less than holding current, it will regain its blocking capability.

III. SERVICE

Personnel familiar with electrical equipment utilizing semiconductors can isolate most problems using an oscilloscope, multimeter, and information contained in relative instruction leaflets.

Semiautomatic equipment is available at the factory to test static and dynamic performance of all edge-connected, printed circuit boards. Generally, repair of modules is facilitated by returning them to: Westinghouse Electric Corporation
Industrial Systems Division
P. O. Box 225
Buffalo, New York 14240.