M4CH THYRISTOR POWER CONVERTER & BASIC REGULATOR
FIELD START-UP PROCEDURE

INDEX — SECTION

Introduction — I

Basic System — II

A. General

B. Start-Up Procedure

Appendix — III

Trouble Shooting — IV

Effective November 1978

I. INTRODUCTION

These instructions provide a step-by-step procedure for the first time start-up of a M4CH Thyristor Power System used as an armature supply for main drive d-c motor application.

Non-standard functions such as special sequencing, director logic, variable regulator, interconnection with other drives, etc. which pertain to a specific application are covered by separate instructions.

The procedures should be followed in the specified sequence, checking each step against the schematic diagram. This will develop familiarity with the system and insure proper operation of the drive system when the sequence is completed. If difficulty is encountered at any step, the source of trouble and/or remedy may be obvious due to LED indicators. If not, refer to the "Trouble Shooting" section of this instruction leaflet for more detailed test procedures.

It should be possible to place the drive system in operation by following the start-up procedure as described, referring only to the applicable schematic diagram. However, a more efficient and confident approach requires a knowledge of fundamental functions and relations which can be obtained by referring to the Instruction Leaflets (I.L.) listed in the Appendix.

II. BASIC SYSTEM

A. General

This section is devoted to a procedure for first time start-up of the basic M4CH Thyristor Power System. The basic system consists of the following:

1. Thyristor Power Converter which contains:

   a) Combination of 1 to 6 thyristor cabinets.
   b) Incoming Cabinet.
   c) Junction Box.

   } Per 6 Ø System

   Refer to I.L. 16-800-346 for a more detailed description of the Thyristor Power Converter.

2. Regulator/Control Cabinet which contains:

   a) Basic Regulator containing:

GCTM	-	gate control module	
DGPG	-	digital gate pulse generator	gating system
TGD	-	thyristor gate driver	
PSM	-	power supply module	
ATR		analog transmitter/receiver	
DTR	-	digital transmitter/receiver	
ORB	-	output relay board	
1IB, 2IB	-	input board	
CC	-	current controller	
VS	-	voltage sensor	
RL	-	reversing logic	

POT	-	pot board
PROT GPS	-	protection gate pulse suppression
PROT BKR	-	protection breaker
DIFFC	-	differential current & ITOL
BAS SEQ	-	basic sequencing
PS	-	power supply
MB	-	meter board

b) Variable Regulator

c) A-C Control relays

3. A-C & D-C Power Circuits with standard protection features

B. Start-Up Procedure

1. Test Equipment

1.1 Dual beam oscilloscope, such as a Tektronix 465, 466 or equivalent.

NOTE: Be sure that the scope is NOT GROUNDED at the line or elsewhere. When the system is energized, the scope case may be at some voltage potential above ground.

1.2 Six (6) channel brush recorder, such are GOULD BRUSH #260 6 CHANNEL RECORDER, MODEL 15-6367-00, 115 VAC, 60 HZ or equivalent.

1.3 Two adjustable battery powered test supplies, 0-12V, with reversing and turn-off switch.

1.4 A digital multimeter such as a FLUKE DIGITAL MULTIMETER, Model 8000A-01, 2000 count digital with rechargeable battery pack or equivalent.

1.5 30 Pin extension board (S#1339A38G02) & 60 pin extension board (S#487A211G01).

1.6 Communications such as sound power phones FM walkie-talkie, or equivalent.

2. Inspection and Preparation

2.1 Check for transportation damage.

2.2 Inspect all cabinets for loose connections, loose hardware, etc.

2.3 Remove all blocking of relays and contactors.

2.4 Check all external wiring which also includes the wiring between the F1, R1 power converter junction box and the regulator/control cabinet.

2.5 Make sure auxiliary a-c disconnect switches and a-c and d-c circuit breakers are open.

2.6 Megger power bus 1U, and F1P, to ground, with 1KV d-c. (Repeat for 2U and F2P in case of a 12 Ø system). Should read a minimum of 1 megohm.

NOTE: PULL GND WIRE FROM GROUND DETECTOR PNL, REMOVE THE CURRENT CONTROLLER BOARDS(S) FROM THE BASIC REGULATOR, AND OPEN THE "M" CONTACTOR ARC SHUTES BEFORE MEGGERING.

2.7 Check each pair of thyristors fuses with an ohmmeter for continuity.

ON ALL SUBSEQUENT STEPS THROUGHOUT THIS START-UP PROCEDURE IT IS ASSUMED THAT THE SERVICE ENGINEER WILL INVESTIGATE PREVENTATIVE INTERLOCKING CIRCUITS TO ENSURE THAT THE TEST FUNCTIONS CAN BE COMPLETED.

NOTE: AFTER MOST STEPS, YOU WILL FIND THE SHEET NUMBER(S) OF THE SCHEME IN PARENTHESIS THAT PERTAIN TO THE COMPONENT OR CIRCUIT UNDER TEST.

3. Auxiliary Power Check

Apply a-c auxiliary power (460V, 60 HZ or 380V 50 HZ) to the incoming terminals. Close the A-C auxiliary Power breaker and check the following:

3.1 AUX. AC POWER ON light is energized. (7)

3.2 AC BREAKER TRIPPED pushlite is energized. (8, 15)

3.3 DC BREAKER(S) TRIPPED pushlite is energized. (10)

3.4 THYRISTOR POWER SUPPLY RESET pushlite is energized. If not, depress it. (13)

3.5 DC CONTACTOR OPEN light is energized. (8)

3.6 All other regulator cabinet door lights should be de-energized except fault finder LED'S. (19 to 22)

3.7 The voltage across CX and CY is 115V $\pm$ 5V. (7)

3.8 Gate Pulse Amplifier Power Supply output (AP-PSC) is +30V $\pm$ 6V. (7)

3.9 Green LED'S energized on the power supply board(s) [PS] in cage position B15 and C15 (12 Ø system only) indicate that P24, N24 and P15 are energized. Use a multimeter and check the following d-c voltages with respect to PSC: (12)

P24 = +24V $\pm$ 0.1V

N24 = -24V $\pm$ 0.1V

P15 = +15V $\pm$ 0.1V

+24 = +24V $\pm$ 4V

3.10 Depress the THYRISTOR FANS ON pushlite located on the regulator cabinet door and note the following: (7)

3.10.1 Red pushlite is energized.

3.10.2 Thyristor cabinet fans start and are exhausting air from the rear top or bottom of the cabinet. If fan rotation is incorrect, interchange any two leads of the appropriate power feeder to the fan(s). (5, 5A)

3.10.3 All series connected air flow switches are closed. Circuit can be checked in the F1 junction box located next to the regulator cabinet. (5, 5A)

ASW1 - ASW2 for a 6 Ø system or

ASW1 - ASW3 for a 12 Ø system

Refer to the Trouble Shooting section of this I.L. for air flow switch calibration instructions if a fan is running and its air flow switch remains open.

4. Calibration & Protective Circuits Check

Before applying main a-c power to the thyristor power system, calibrate and check all protective features of the TPS.

4.1 Calibration of Forward & Reverse Current Calibration Pots. (21)

4.1.1 Disconnect the thyristor gate driver boards [TGD] from cage positions B01 & B03 and C01 & C03. if system is 12 phase. (25, 33)

4.1.2 Disconnect current sensor leads -/I[D]/F1 and -/I[D]/R1 from the F1 and R1 current sensors located in Incoming Cabinet No. 1. (5)

4.1.3 Calculate the necessary test voltage to similate symmetrical drive current (since V/A are equal for F1 and R1 amps) from the following equation:

$$-/I[D]/F1 = \frac{5X\ 0.76}{CT\ PRI\ AMPS} \times I_{DC}$$

where I_{DC} = rated F1 converter d-c amps.

4.1.4 Set pots 2P and 3P to ECW position on the [POT] board located in cage position B09. (21)

4.1.5 Apply the calculated test voltage to pins 39 and 9 of the [POT] board with pin 9 positive with respect to pin 39. (21)

4.1.6 Adjust pot 2P so that pin 43 equals -2V @ rated F1 converter d-c amps. (21)

NOTE: Drive may fault out on GPS or DIFFC. Disregard at this time.

4.1.7 Also check the polarity of the -/I[D]/F1 wire in the incoming cabinet. (Should be negative with respect to PSC) (5)

4.1.8 Repeat steps 4.1.5 thru 4.1.7 to calibrate pot 3P connecting the test voltage between pins 15 (-) and 9 (+) and monitor pin 45 and -/I[D]/R1.

12 Ø SYSTEM

4.1.9 Repeat steps 4.1.1 thru 4.1.8 by disconnecting the current sensor leads in Incoming Cabinet No. 2 and adjusting pots 2P and 3P on [POT] board in cage position C09. (5A,30,33)

4.2 Calibration of 6P on POT board

4.2.1 Calculate -/I[D]/R1 using the equation in step 4.1.3 and apply this test voltage between pins 15 (-) and 9 (+) of the POT board in cage position B09. (20)

NOTE: If the drive system is symmetrical, -/I[D]/R1 will equal the value calculated in step 4.1.3.

4.2.2 Adjust 6P of the above POT board so that pin 27 of the POT board equals -1.0V. (20)

12 Ø SYSTEM

4.2.3 Calculate -/I[D]/R2 using the equation in step 4.1.3 and apply this test voltage between pins 15 (-) and 9 (+) of the POT board in cage position C09. 15 (-) 9 (+). (29)

4.2.4 Adjust 6P of the POT board in position C09 so that pin 27 equals -1.0V. (29)

4.3 Verification of the Inverse Time Overload Circuits.

4.3.1 Remove a-c auxiliary power, remove POT board and set FOC & ROC jumpers (1J and 2J respectively) on the pot board to their maximum setting. Replace pot board and reapply a-c auxiliary power. (21)

4.3.2 Connect the negative test voltage to pin 39 of the POT board. Increase voltage until pin 43 of the POT board equals -6V. This represents 300% rated F1 current. (21)

4.4.4 FOL LED on DIFFC board should come on in 10 seconds ± 2 sec. (20)

4.3.4 Connect the negative test voltage to pin 15 of the POT board. Increase the voltage until pin 27 of the POT board equals -3V. This represents 300% rated R1 current. ROL LED on DIFFC board should come on in 10 seconds ± 2 sec. (21, 20)

12 Ø SYSTEM

4.3.5 Repeat steps 4.3.2 thru 4.3.4 using the POT board in cage position C09 and the DIFFC board in cage position C13. (29, 30)

4.4 Verification of Differential Current Trip Level.

4.4.1 Tie pin 27 to PSC on the PROT BKR board in cage position B12 and also on PROT BKR board in cage position C12 in case of a 12 Ø system. This will disable the a-c and d-c breaker trip circuits so that the breakers will not be cycled unnecessarily on subsequent fault checks. (21, 30)

4.4.2 Make sure all Zone A (ZAP) and Zone B (ZAB) circuits are permissive. (14)

4.4.3 NOTE: Check to make sure that the primary of the gating isolation transformer (normally located in Incoming Cab. No. 1) is connected to the nearest 1U, 1V, 1W voltage per the table shown in the shop order schematic before applying main a-c power. (5B)

4.4.4 Close the A-C Auxiliary breaker, the Main A-C breaker, and the gate control module breaker. Depress the A-C BREAKER TRIP pushlite to make sure the main a-c breaker is trippable from the reg. cab. (7,12,15,8)

4.4.5 Check that the input voltage to the gate control module is 115V ±5V with phase sequence GU, GV, GW and is in phase with power transformer secondary leads 1U, 1V, 1W. (12)

4.4.6 The following LED's should be energized on 1IB and 2IB (cage positions A21 and A22) PSROFF', ZAPR, ZBPR. OCL', ZIR', EXTVRT, LED'S will be energized if respective function is not used. (13, 14)

4.4.7 All LED's on the PROT BKR boards; cage position B12 and C12 (12 Ø system only) and the PROT GPS board in cage position B11 should be deenergized. (21, 22, 30)

4.4.8 Connect the test voltage to pin 39 of the POT board and set for 0 volts. (21)

4.4.9 Depress the THYRISTOR POWER SUPPLY READY pushlite and observe that the amber pushlite is energized, relays 1CR and 2CR on the output relay board (ORB) in cage position A20 are energized, and relays PSR and CMC are energized. (7, 8, 15)

4.4.10 Turn the DC CONTACTOR PERMISSIVE selector switch to its TO CLOSE position. Momentarily close the OPERATOR'S CONTACTOR CONTROL SWITCH. Relays PCM and MC should be energized and the main M contactor/breaker should be energized. The M LED on Input Board 2IB should be energized. (13,15,9,14)

MAKE SURE THE D-C BREAKER(S) REMAIN OPEN.

4.4.11 Increase test voltage in a negative direction until the drive trips out on gate pulse suppression. This should occur when pin 43 of the POT board is -1 V ± 0.2 V. (21,20,22,13,9)

The DIFFC LED on the PROT BKR board, the FDC LED on the DIFFC board and the INH LED on the PROT GPS board should be energized. The POWER SUPPLY READY pushlite and RESET pushlite should be deenergized. The main M contactor/breaker should be deenergized.

4.4.12 Reduce test voltage to 0 volts. (21)

4.4.13 Reset system by depressing the THYRISTOR POWER SUPPLY RESET and READY pushlite and cycle the DC CONTACTOR control switch in that order. (13)

4.4.14 Increase test voltage in positive direction and note the same results as in step 4.4.11 except pin 43 of the board will be +1V ± 0.2 V.

4.4.15 Move test voltage to pin 15 of the POT board. Repeat steps 4.4.11 thru 4.4.14 observing that pin 45 is -1 V + 0.2 V and the RDC LED will be energized for the fault condition.

4.4.16 Repeat steps 4.4.11 thru 4.4.15 using the POT board in cage position C09 and observing PROT BKR board in cage position C12 and DIFFC board in cage position C13. (30,29,22,13,9)

4.4.17 Disable the DIFFC circuit by connecting pin 47 of the DIFFC board in cage position B13 and position C13 (12 Ø system only) to PSC. (20, 29)

4.5 Setting of Forward and Reverse Overcurrent Jumpers

4.5.1 Open A-C Auxiliary Power breaker to prevent a missing board fault. (7)

4.5.2 Remove POT board from cage position B09. (21)

4.5.3 Set FOC & ROC jumpers 1J and 2J respectively per information found on sheet 21 of the schematic.

4.5.4 Plug POT board back into cage. (21)

12 Ø SYSTEM

4.5.5 Remove POT board from cage position C09. (30)

4.5.6 Set FOC & ROC jumpers jJ and 2J respectively per information found on sheet 30 of the schematic. (30)

4.5.7 Plug POT board back into cage. (30)

FOR THE FOLLOWING FAULT CHECKS, ONLY THE "TPS RESET" PUSHLITE NEED BE USED TO RESET SYSTEM. M CONTACTOR/BREAKER CAN REMAIN OPEN. ALSO THE FOLLOWING FAULTS SHOULD ALWAYS LIGHT THE INH LED. TEMPORARY CONNECTIONS PER STEPS 4.4.1 AND 4.4.17 ARE STILL IN ACCECT.

12 Ø SYSTEM

NOTE: IN 12 PHASE SYSTEMS 8 LED ON THE PROT BKR BOARD IN CAGE POSITION C12 WILL BE ENERGIZED IF ANY ONE FAULT OCCURS ON THE PROT BKR BOARD IN CAGE POSITION B12 NAD THE CONVERSE IS ALSO TRUE. THIS MEANS A FAULT IN ONE 6 PHASE SYSTEM WILL TRIP OUT THE OTHER 6 PHASE SYSTEM PROVIDING A 12 PHASE INTERLOCKING FEATURE.

4.6 Verification of Circulating Current Circuit (Double Converters Only).

4.6.1 Apply separate negative test voltages to pins 39 and 15 of the POT board. (21)

4.6.2 Increase test voltage at pin 39 until pin 43 is -1V. Increase test voltage at pin 15 until drive shuts down. Voltage at pin 45 of the POT board should be -1V $\pm$ 0.3V.

4.6.3 Note that the CC LED on the PROT BKR board is energized. (21)

4.6.4 Reduce test voltages to zero and reset drive. (21)

12 Ø SYSTEM

12 Ø SYSTEM

4.6.5 Repeat steps 4.6.1 thru 4.6.4 using POT board in cage position C09 and PROT BKR board in cage position C12. (30)

4.7 Verification of Forward and Reverse Overcurrent Circuit

4.7.1 Increase negative test voltage connected to pin 39 until drive shuts down. This should occur at the proper FWC OC jumper setting voltage ± 10%. The FOC LED on the PROT BKR board should be energized. (21)

4.7.2 Reduce test voltage to zero and reset drive (21)

4.7.3 Increase negative test voltage connected to pin 15 of POT board until drive shuts down. This should occur at the proper REV OC jumper setting voltage ± 10%. The ROC LED on the PROT BKR board should be energized. (21)

4.7.4 Reduce test voltage to zero and reset drive. (21)

12 Ø SYSTEM

4.7.5 Repeat steps 4.7.1 thru 4.7.4 using the POT board in cage position C09 and the PROT BKR board in cage position C12. (30)

4.8 Verification of D-C Breaker Trip Circuit

4.8.1 Apply +24V to pin 9 of PROT BKR board in cage position B12. (21)

4.8.2 The drive should shut down and the DC BKR LED should be energized. (21)

4.8.3 Remove the +24V signal and reset the drive. (21)

12 Ø SYSTEM

4.8.4 Repeat steps 4.8.1 thru 4.8.3 using the PROT BKR board in cage position C12. (30)

4.9 Verification of A-C Breaker Trip Circuit

4.9.1 Trip the a-c breaker by depressing the AC BREAKER TRIP pushlite on the regulator cabinet door. (8, 15)

4.9.2 The drive should shut down and the AC BKR LED on the PROT BKR board should be energized.

4.9.3 For 12 Ø systems, check to see that the AC BKR LED on the PROT BKR board located in cage position C12 is energized.

4.9.4 Reset the drive.

4.10 Verification of ± 24V Power Supply Loss

4.10.1 Remove either the P24 or N24 fuse from the power supply module in cage position A17. (12)

4.10.2 The drive should shut down and the ± 24V LOSS LED on the PROT BKR board should be energized. (12)

4.10.3 Replace the fuse and reset the drive. (12)

4.10.4 Repeat steps 4.10.1 thru 4.10.3 using the PROT BKR board in cage position C12 and the power supply module in cage position D17. (30, 28)

4.11 Verification of Phase Sequence Detection Circuit (22)

4.11.1 Simulate the fault by grounding pin 39 of the PROT GPS board in cage position B11 to PSC.

4.11.2 The drive should shut down and the PH SEQ LED on the PROT GPS board should be energized.

4.11.3 Remove the ground and reset the drive.

4.12 Verification of the Single Phasing Detection Circuit (22)

4.12.1 Simulate the fault by grounding pin 7 of the PROT GPS board to PSC.

4.12.2 The drive should shut down and the 1PH LED should be energized.

4.12.3 Remove the ground the reset the drive.

4.13 Verification of the Undervoltage Detection Circuit (22)

4.13.1 Simulate the fault by grounding pin 5 of the PROT GPS board to PSC.

4.13.2 The drive should shut down and the UV LED should be energized.

4.13.3 Remove the ground and reset the drive.

4.14 Verification of the GPA Power Supply Loss

4.14.1 Remove the fuse from the gate pulse amplifier power supply located on the control panel. (7)

4.14.2 The drive should shut down and the APL LED on the PROT GPS board should be energized.

4.14.3 Replace the fuse and reset the drive (7)

4.15 Verification of the Missing Board Circuit

4.15.1 Disengage any one of the following boards: (19,21,23,30,31)

POT, RL, BAS SEQ

NOTE: In a 12 Ø system both POT boards and both RL boards have the missing board interlock feature.

4.15.2 The drive should shut down and the MB LED on the PROT GPS board should be energized. (21)

4.15.3 Engage the board(s) removed in step 4.15.1 and reset the drive.

4.16 Balancing Current Conditiong Circuit of Reversing Logic Board.

4.16.1 Reconnect the current sensor leads that were disconnected in step 4.1.2 and 4.1.9 if applicable. (5, 5A)

4.16.2 Close main a-c breaker and gate control module breaker and make sure all faults have been cleared and F1, R1 TGD boards in cage position B01 and B03 are engaged. (25)

4.16.3 Adjust 2P on RL board in cage position B08 so that the output on pin 29 (+/I[D]/1) is 0.0m V ± 0.3 mV. (23)

4.16.4 Adjust 1P on RL board so that the output on pin 59 (-I[D]1) is 0.0m V ± 0.3 mV. (23)

12 Ø SYSTEM

4.16.5 Disengage the F1, R1 TGD's and engage the F1, R2 TGD's in cage position C01 and C03 and repeat steps 4.16.3 and 4.16.4 for the RL board in cage position C08. (31)

4.17 Zeroing Current Reference Ramp of Current Controller (24)

4.17.1 Conditions are still the same on step 4.16.2.

4.17.2 Turn pot 1P of POT board in cage position B09 ECCW and POT 5P of the POT board ECCW. Make sure pin 5 of the CC is 0.0V.

4.17.3 Release the current reference ramp of the current controller [CC] in cage position B06 by picking up the M contactor/breaker i.e., logic signal 1CR becomes a logic "1" thereby deenergizing static relay 1CR on the CC board. 1CRDB LED on the current controller will be energized.

4.17.4 Adjust pot 1P of the CC board until -I[D]* (pin 15) is 0.0m V ± 1mV.

4.18 Balancing Current Controller Amplifiers 5-0A and 6-0A (24)

4.18.1 Conditions are still the same as 4.16.2.

4.18.2 Release the current controller by energizing the M contactor/breaker; logic signal 2CR becomes a logic "1". 2CR LED on the current controller should be energized.

4.18.3 Make sure that -I[D]* (pin 23) and +/I[D]/1 (pin 17) are both 0 volts.

4.18.4 Adjust pot 2P on CC in cage position B06 until +V[C]1 (pin 19) has minimum drift without the controller going into its limit condition.

4.18.5 Set the current controller gain pot 4P located on the POT board (cage position B09) and the gain jumper 1J (on the back plane) to their minimum gain position i.e. pot 4P ECCW, red jumper 1J pin 49 to 51.

4.18.6 Set current limit pot 1P on POT board (cage position B09) and red jumpers 2J and 3J associated with the current controller per sheet 24 of the schematic.

12 Ø SYSTEM

4.18.7 Repeat steps 4.18.1 thru 4.18.5 using the current controller in cage position C06 and the POT board in cage position C09. (32)

4.19 Verification of A-C and D-C Breaker Trips

4.19.1 Remove temporary breaker trip inhibit jumpers from pin 27 to PSC from the PROT BKR board in cage position B12 and cage position C12 in case of a 12 Ø system. (21, 30)

4.19.2 Close a-c breaker and d-c breaker(s).

4.19.3 Momentarily remove either the P24 or N24 fuse from the power supply module in cage position A17 and note that the a-c breaker, the d-c breaker(2) and the M contactor/breaker trip out. (12)

4.19.4 Reclose all breakers and M contactor/breaker and reset the drive.

4.19.5 Trip the d-c breaker(s) from the trip module and the pushlite on the regulator cabinet door. Result should be the same as in step 4.19.3. (10, 11)

4.19.6 Repeat step 4.19.4 and trip a-c breaker from the pushlite on the regulator cabinet door and any other device that can trip the a-c breaker. Result should be the same as in step 4.19.3.

4.19.7 Repeat step 4.19.4.

4.20 Verification of CMC Circuit

4.20.1 Verify that the motor overspeed device(s) is operative. (6)

4.20.2 Install a temporary normally closed pushbutton contact (E. STOP) in the CMC circuit between wires 817 and 818. (8)

NOTE: THE PUSHBUTTON SHOULD BE LOCATED SO THAT START-UP PERSONNEL CAN VISUALLY SEE THE MOTOR AND OPERATE THE PUSHBUTTON WHEN CONDUCTING STALLED ARMATURE TESTS.

4.20.3 Operate pushbutton and verify that the M contactor/breaker trips out. (8, 9)

4.20.4 Reset drive and verify that contactor picks up again

5. Procedure for Checking Thyristor, Phasing, Gating and TPS Output Waveform.

OBJECT: To check the power phasing between the F1 converter section and F2 converter section for a 12 ∅ system.

To check the pulse trains phasing with respect to the a-c voltage and with respect to each other and to isolate each power converter section and determine that the gate pulse amplifiers are producting 6 pulse trains of the correct waveform and that the output waveform of the power converter is correct.

5.1 Open the a-c breaker and the d-c loop (d-c breaker(s) and main contactor). Open the auxiliary a-c power breaker.

5.2 A two channel scope with the ability of adding two signals, one of which can be inverted, is required to check thyristor phasing.

5.3 CAUTION: MAKE THE FOLLOWING CONNECTIONS WITH THE A-C BREAKER OPEN. NOTE THAT THE A-C VOLTAGE IS VERY HIGH AND PRECAUTIONS SHOULD BE TAKEN TO PROTECT PERSONNEL AND SCOPE DURING THESE TESTS.

5.3.1 Connect channel 1 to 1U bus located in Incoming Cab. No. 1.

5.3.2 Connect channel 2 to 1W bus located in Incoming Cab. No. 1 and invert it.

5.3.3. Close the main a-c breaker.

5.3.4 Switch to the "ADD" mode and establish line sync and zero crossover point. Mark zero crossover point in some manner. This 1U-1W a-c voltage represents the commutation voltage of thyristor 1 which will be gated by pulse 1.

5.3.5 Open the main a-c breaker.

5.3.6 Repeat steps 5.3.1 thru 5.3.5 looking at 2U and 2W buses located in incoming Cab. No. 2. This will now give the phase relationship between the F1 and F2 converter section(2U-2W logic 1U-1W by 20°).

5.4 Remove the current controller [CC] located in cage position B06 and the analog transmitter/receiver board [ATR] from cage position A18. (24, 18)

5.5 Connect a small negative test voltage (-1V) (-I[D]**) with respect to PSC to pin 29 of edge connector A18. (18)

NOTE: This signal will control the ENF1 and ENR1 logic signals. With -I[D]** negative, ENF1 will be a logic "1", and when it is positive, ENR1 will be a logic "1". (23)

5.6 Connect a positive test voltage with respect to PSC set at zero volts to pin 53 of the digital gate pulse generator [DGPG] located in cage position B05. (25)

5.7 Plug in the F1 TGD in cage position B01, ALL OTHER TGD BOARDS ARE STILL DISENGAGED. (25)

5.8 Connect channel one of the scope to PULSE TRAIN #1 (pins 49 and 47) of the GPA board in cage position 02 located in the F1 thyristor cabinet with pin 47 positive with respect to pin 49. Line sync of scope has been established in step 5, 3, 4.

5.9 Steps 5.5 and 5.6 still apply.

5.10 Close auxiliary a-c breaker and main a-c breaker. THE MAIN D-C LOOP IS TO REMAIN OPEN.

5.11 Energize the thyristor power system.

5.12 Observe that the GPA pulse train is similar to Figure #1 and the phase back angle with respect to the zero voltage crossover point (as marked in step 5.34) should be 145° ± 5°.

Note: The magnitude of the trailing edge is a function of the number of thyristors being gated by the pulse; the fewer thyristors the higher the voltage. The magnitude of the hard (first) pulse should be 28V ± 10% and the magnitude of the tail end of the trailing pulses should be 24V ± 10% for two thyristors to 16V ± 10% for six thyristors.

5.13 Move the scope to PULSE TRAIN #2 (pins 41 and 43) of the GPA board in cage position 06 with pin 43 positive with respect to pin 41. Observe that the GPA pulse train is similar to Figure #2. Note that it occurs 60° after PULSE TRAIN #1.

5.14 Proceed to see that the remaining pulse trains are present and displaced 60° from each other.

PULSE	GPA BOARD CAGE POSITION	POSITIVE PIN WITH RESPECT TO PIN	
#1	02	47	49
#2	06	43	41
#3	04	47	49
#4	02	43	41
#5	06	47	49
#6	04	43	41

5.15 Connect scope to pin 37 (-V[B]1] of the voltage sensor located in position B07. Pin 37 is negative with respect to PSC. (24)

5.16 Increase test voltage on pin 53 of the DGPG in the positive direction until voltage sensor output (-V[B]1) equals -3V. The TPS output should read one half rated voltage and the waveform should show six pulses present and 60° apart from approximately 10% to rated volts. The trace should be stable over the entire voltage range with no random jitter, missing pulse, or great difference in amplitude. (24)

5.17 Further increase the test voltage until full rated output is obtained. The voltage sensor output should be -6V and the test voltage should not exceed +5V. (24)

The waveform should be similar to Figure #4.

5.18 Return the test voltage to zero volts and remove the a-c power.

FOR R1 CONVERTER SECTION

5.19 Repeat steps 5.7 thru 5.18 with the following exceptions:

5.19.1 Remove the F1 TGD in cage position B01 and plug in the R1 TGD in cage position B03. (24)

5.19.2 Change the polarity of test voltage -I[D]** on pin 29 of the edge converter A18 to a small positive value to enable reverse gating. (18)

5.19.3 Polarity of voltage sensor will be reversed. (24)

12 Ø SYSTEM

5.20 Repeat steps 5.4 thru 5.19 using the PC boards pertaining to the F2, R2 converter system, namely the current controller in cage position C06, the digital gate pulse generator in cage positive C05, F2 thyristor gate driver in cage position C01, and the R2 thyristor gate driver in cage position C03. (32, 33)

6. Calibration of D-C Current Sensor

6.1 Prepare motor for stall current test as follows:

6.1.1 Set the mechanical overspeed device to a very LOW TRIP VALUE and verify E. STOP pushbutton installed in step 4.20.2 and follow steps 2 thru 10 (DELETE STEP 1) on STALLED CURRENT TEST ON DC MOTOR I.L. 16-800-286A REFERRING TO THE NOTE ON THE BOTTOM OF PAGE 1 OF THE I.L. (6, 8)

6.2 Install the F1 and R1 TGD boards in cage position B01 and B03 respectively and if a 12 Ø system is being tested remove the F2 and R2 TGD boards from cage positions C01 and C03 respectively. (25, 33)

6.3 Check and make sure that the current sensor leads -/I[D]/F1 and -/I[D]/R1 that were disconnected in step 4.1.2 have been reconnected. (5, 5A)

6.4 With the main a-c breaker open, the d-c loop open and with the auxiliary a-c power on, calibrate the d-c F1 and R1 current sensors (A140) located in Incoming Cabinet No. 1 by adjusting the balance pot 1P of the respective current sensor so there is 0 V ± 0.01V output with 0 V input. (5, 50)

6.5 Set current limit pot 1P located on the POT board to position 1 which represents 30% current limit. (24)

6.6 With ATR located in cage position A18 still disengaged, connect a test voltage -I[D]** set a 0 volts to pin 29 of the edge connector. (18)

6.7 Plug in the current controller (CC) in poistion B06. (24)

6.8 Connect one channel of the scope to pin 43 of the POT board in position B09. Pin 43 is negative with respect to PSC. Connect the other channel to pin 37 of the voltage sensor board in cage position B07 with pin 37 negative with respect to PSC. (21, 24)

6.9 Close the main a-c breaker, aux. a-c breaker and d-c breaker(s). Depress the POWER SUPPLY READY pushbutton and turn the DC CONTACTOR PERMISSIVE selector to the TO CLOSE position and cycle the OPERATOR'S CONTACTOR control switch. (7,13)

6.10 The following LED'S SHOULD NOW BE ENERGIZED.

BOARD	POSITION	LED'S ENERGIZED
1IB	A21	All but ONR, PSRON, RESETR
2IB	A22	All but TACBKR
ORB	A20	All but 52TLX, GPSL
BAS SEQ	B14	All but CF
TGD	B01, Bo3	Indeterminate when -I[D]**=0

6.11 Increase the negative test reference -I[D]** until 25% rated forward current is flowing (-I[D]**= -8.33V ± 10%) (18)

6.12 Calibrate the F1 A240 current sensor gain pot 2P so that -I[DC]F1= -/I[D]F/1 = -0.5V ± 5%. (5,5C,21)

NOTE: Bus drop wires (1-2H) have a mechanical adjustment of ± 2 inches.

6.13 The current feed back waveform should be similar to Figure #3 The trace should be stable with no random jitter, missing pulse, or great difference in amplitude.

6.14 The F1 TGD board LED'S & F1 GPA LED'S should all be energized as well as the FWD LED on the RL board in cage position B08 when "forward" load current in flowing. Also the 1CRDB and 2CB LED'S on the current controller in cage position B06 are energized. (25,23,24)

6.15 Reduce the test voltage to zero. (18)

FOR DOUBLE CONVERTER (R1 SECTION)

6.16 Increase the positive test reference -I[D]** until 25% rated reverse current is flowing. (-I[D]** = -8.33V ± 10%) (18)

6.17 Calibrate the R1 current sensor gain pot 2P so that -I[D]R1 = -/I[D]R/1 = -0.5V ± 5%. (5,5C)

6.18 The current feedback waveform should be the same as in step 6.13 and observe that the R1 TGD board LED'S & R1 GPA LED'S are all energized as well as the REV LED on the RL board when "reverse" load current is flowing. Also the 1CR DB and 2 CR LED'S on the CC are energized.

6.19 Reduce the test voltage to zero.

7. Current Loop Gain Adjustment

7.1 Check to make sure that the gain of the current controller is set at its minimum setting, i.e. 4P on the POT board at ECCW and red jumper 1J connecting pin 49 to 51. (24)

7.2 With motor armature stalled, apply a small negative test reference step (-I[D]** = -1.7 to - 3.4V) to circulate approximately 5% to 10% rated forward current. (18)

NOTE: CURRENT MUST NOT BE DISCONTINUOUS

7.3 Increase the gain pot clockwise until the current loop becomes unstable. If it is necessary to move red jumper 1J to a higher gain position to achieve the unstable condition, set 4P ECCW again before moving the jumper. (24)

7.4 Once instability is achieved, reduce the setting of the gain pot 4P just enough to stabilize the loop. (24)

FOR DOUBLE CONVERTER (R1 SECTION)

7.5 Reverse polarity of test reference and reverse drive rapidly if it is stable in both directions. If drive should shut down due to a fault condition, see Trouble Shooting section and check for current reference ramp deadband of 4 ms.

7.6 Reduce test reference to zero volts, open d-c loop and remove auxiliary a-c power.

8. Verification of Overcurrent Jumper Settings

8.1 Set pot 1P on the POT board in position B09 at its ECW setting. (24)

8.2 Remove fault sensor leads F1FS3 and F1FS4 from the F1 junction box blocks to disable the fault current sensor. (5)

8.3 Remove POT board from cage and set the forward and reverse overcurrent jumper settings as follows or to nearest setting above this: (This should agree with jumper settings on sheet 21 of the schematic) (21)

$$FOC\ (\%) = 1.2 \times FWD\ C.L.\ \%$$

$$ROC\ (\%) = 1.2 \times REV\ C.L.\ \% \times \frac{REV\ RATED\ CURR.}{FWD\ RATED\ CURR.}$$

The available FOC & ROC settings are as follows:

FOC JUMPER (1J) SETTING	ROC JUMPER (2J) SETTING
-	50%
-	80%
-	100%
125%	125%
160%	150%
190%	190%
215%	215%
250%	250%
315%	315%
375%	360%

Note: If the FOC jumper should open for any reason the trip setting will become 100% rated F1 amps and if the ROC jumper should open, its setting will become 50% rated F1 amps.

Example: F1 Amps = 4000; % CL = 200

R1 Amps = 2000; % CL = 150

a) FOC Setting (%) = 1.2 X 2000% = 240%.

Nearest higher setting is 250%

b) ROC Setting (%) = 1.2 X 150% X $\frac{2000}{4000}$ = 90%

Nearest higher setting is 100%

8.4 Plug POT board back into cage.

8.5 Display +/I[D]/1 (pin 29 of RL board) on brush recorder on time scale 125 mm/sec. (23)

CAUTION: REFER TO STEP 6.1.1 & I.L. 16-800-286A BEFORE PROCEEDING.

8.6 Apply small negative pulse width steps for -I[D]** while observing +/I[D]/1 on the brush recorder. (18,23)

NOTE: Insure motor is stopped before applying current pulse.

Increase magnitude of step until forward overcurrent trip occurs. This should occur within ± 5% of the jumper setting. Note +/I[D]/1 = +2V at rated current.

R1 CONVERTER SECTION

8.7 Repeat step 8.6 using small positive width steps for -I[D]** and verify the reverse overcurrent setting by brush recording.

9. Calibration of Converter FAult Current Sensor (50A)

9.1 Check to make sure the converter fault current sensor is of the proper size as determined from table below using the following rule: (5)

Trip amps = 1.25 X current limit amp of the converter section.

TABLE

CURR. LIMIT (AMPS)	MAX RATED CURR. (AMPS)	FAULT CURR. SENSOR SIZE	SENSOR STYLE NO.
2000 - 4000	3750	4	1895A76G01
3000 - 6000	5000	5	1895A76G02
6000 - 12000	8000	6	1895A76G03

9.2 Reconnect the leads removed in step 8.2 (5)

9.3 CAUTION: Before working on the fault current sensor with the bus energized, connect the magnetic reed switch mounting panel temporarily to ground. (5)

9.4 Remove the POT board in cage position B09 and move the FOC and ROC overcurrent jumpers to their next higher setting. (21)

9.5 Apply a-c power, reset drive, and close d-c loop.

9.6 Brush is still monitoring +/I[D]/1 (pin 29 of the RL board in cage position B08) (23)

CAUTION: REFER TO STEP 6.1.1 & I.L. 16-800-286 BEFORE PROCEEDING.

9.7 Apply at pin 29 of edge connector A18 with the ATR still disconnected a small negative pulse width steps for -I[D]** while observing +/I[D]/1 on the brush recorder. Increase the magnitude of step until d-c breaker trips. (18)

NOTE: The d-c breaker will probably trip out before the 125% C.L. amps is obtained because the fault current sensor magnetic reed switch has been set at its most sensitive position at the factroy, i.e. edge of reed switch case where leads exit is the sensitivity reference point and should be set at 3.5 on the scale provided.

9.8 Desensitize the switch by moving it toward 7 on the scale. By using a trial and error procedure and curves 1 thru 3 as a guide, the appropriate setting should be obtained. If the breaker continues to trip out below the 125% C.L. point, the reed switch unit should be moved one position further away from the reactor core (increasing X dimension) and the above procedure repeated.

9.9 When the correct setting has been obtained, check to make sure that the trip module causes a gate pulse suppression. (11)

9.10 Remove lead TDCBKR1 from terminal 2 of the breaker trip module. Trip breaker again by circulating 125% C.L. Amps. (11)

9.11 Reconnect lead TDCBKR1 to trip module and restore the FOC jumper to its proper setting as determined in step 8.3 and remove the temporary ground jumper from the magnetic reed switch mounting panel. (11,21)

R1 CONVERTER SECTION

9.12 Repeat steps 9.1 thru 9.11 using a positive test voltage step for -I[D]** (18)

NOTE: FOR 12 Ø SYSTEMS DELAY STEP 9.13 UNTIL F2, R2 SECTION IS TESTED.

9.13 Shut down drive.

9.14 Reset the current limit pot 1P on POT board in cage position B09 to drive requirements. (24)

12 Ø SYSTEM

10. F2, R2 Power Converter Section

Test the F2, R2 converter section in a similar manner as was done in steps 6 through 9 above with the following exceptions:

10.1 Remove the F1, R1 thyristor gate driver and replace the F2, R2 TGD'S in cage positions C01 and C03.

10.2 The current controllers in position B06 and C06 must both be used.

10.3 The a-c and d-c current sensor are located in Incoming Cabinet No. 2.

10.4 All scope and brush measurements are to be made on equivalent PC boards in the "C" row (F2,R2) of the basic regulator.

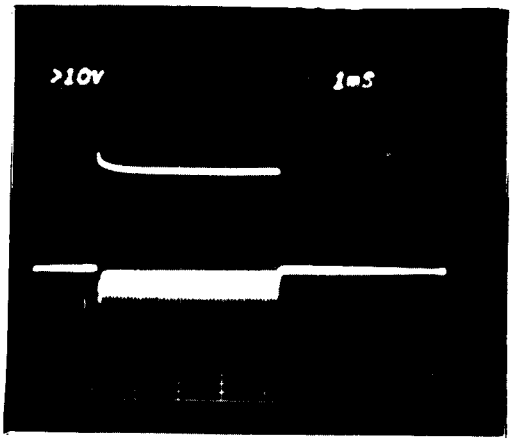
10.5 Make sure that the breaker trip module causes a gate pulse suppression in both the F1, R1 and F2, R2 basic regulator section and that both d-c breakers are tripped.

10.6 Shut down drive.

10.7 Install all TGD's and operate as a 12 Ø system under stall conditions circulating about 25% current. Reverse drive rapidly several times.

10.8 Shut drive down.

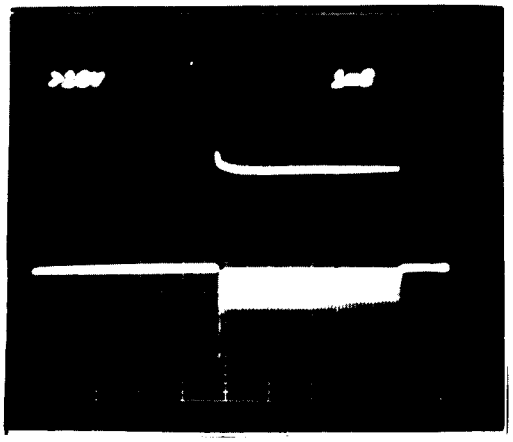
III APPENDIX



10 V/CM

1 MS/CM

GPA PULSE TRAIN #1
FIGURE #1



10 V/CM

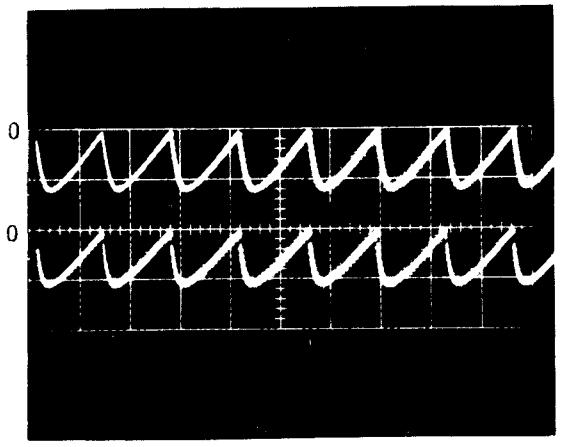
1 MS/CM

GPA PULSE TRAIN #2
FIGURE #2

Ø V [B]

-/I[D]/
(FWD or
REV)

Ø = -V[B] FOR "FWD"
+V[B] FOR "REV"



5 V/CM *

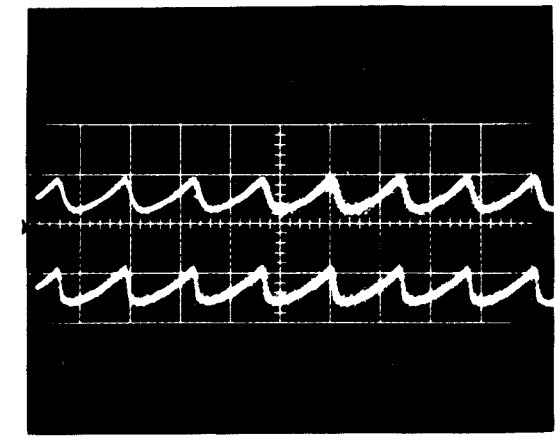
0.2V/CM *
2 MS/CM

VOLTAGE & CURRENT SENSOR OUTPUTS
@ 50% RATE VOLTAGE

FIGURE #3

Ø V[B]

-/I[D]/
(FWD or
REV)



5 V/CM *

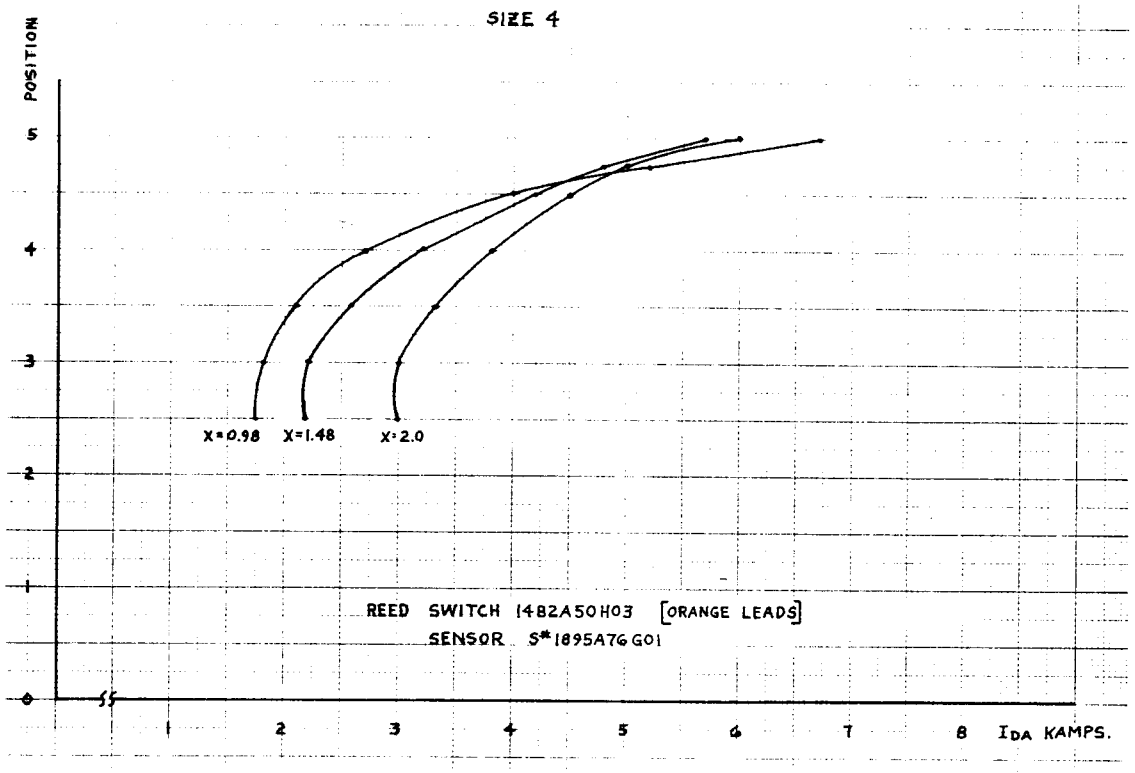
0.2 V/CM*
2 MS/CM

* UNCALIBRATED SCOPE

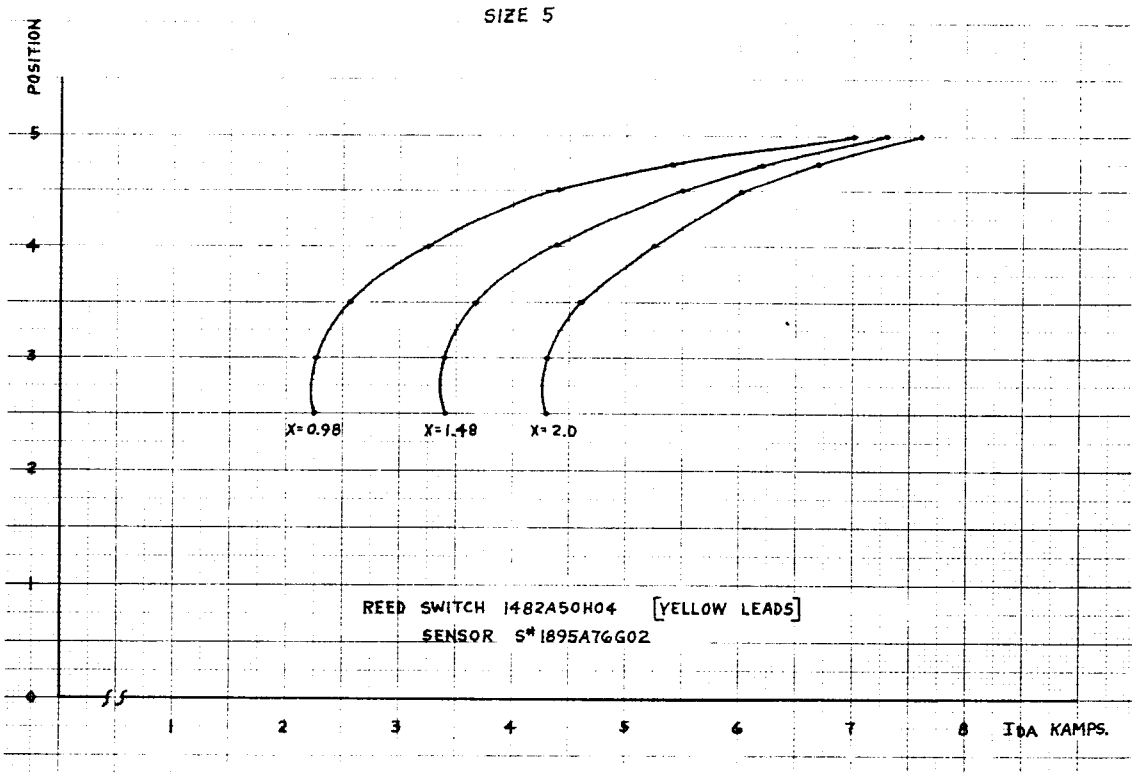
VOLTAGE & CURRENT SENSOR OUTPUTS
RATED VOLTAGE

FIGURE #4

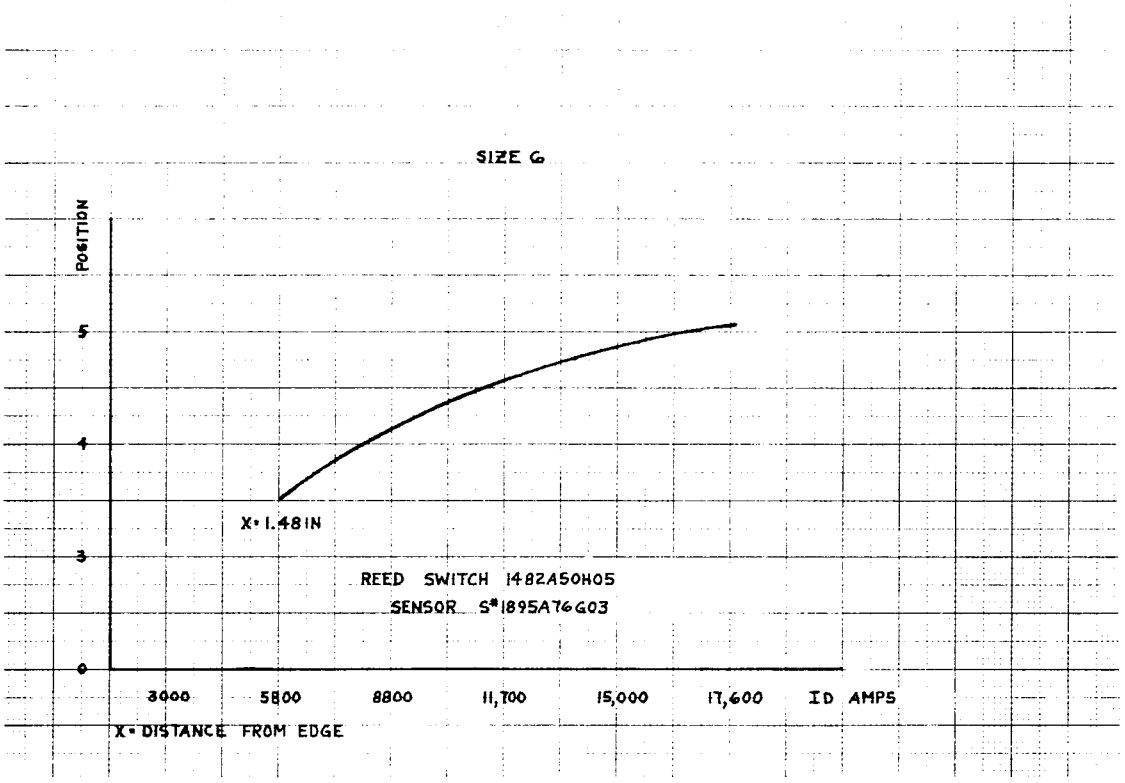
FAULT CURRENT SENSOR TYP. CALIBRATION CURVES



CURVE #1



CURVE #2


SIZE G
POSITION
5
4
3
0
X=1.481N
REED SWITCH 1482A50H05
SENSOR S#1895A76G03
3000
5800
8800
11,700
15,000
17,600
ID AMPS
X=DISTANCE FROM EDGE

CURVE #3

INSTRUCTION LEAFLETS (REFERENCE)

The following instruction leaflets (I.L.) sescribe the M4CH system and its standard components:

M4CH THYRISTOR POWER SYSTEM

I.L. 16-800-346

STANDARD COMPONENT

I.L. 16-800-263 Thyristor Power Module

I.L. 16-800-286A Stalled Current Test on DC Motors.

IV TROUBLE SHOOTING

1. Calibration of thyristor cab air flow switch.

   1.1 Remove pressure switch cover plate.

   1.2 From the knurled knob located adjacent to the microswitch to its extreme CCW position (DECREASING PRESSURE).

   1.3 Now turn the knob one full turn in the clockwise direction.

   1.4 The air flow switch is now correctly set.

2. Checking Current Reference Ramp Deadband.

   2.1 Put the scope on the current ramp output of the current controller, pin 15 of the [CC] in cage position B06 and check to see if the current ramp has a 4 ms ± 1 ms deadband when going from both FWD to REV and REV to FWD. If not, replace the Reversing Logic Board. Refer to figure #5.

   NOTE: If a 12 Ø system is used (F2, R2), interchange the RL board of the F1 section with the RL board of the F2 section and verify the 4 ms deadband for RL (2). Return the RL boards to their original locations.

3. Pulse Train Problems

   3.1 Refer to figure #6 for an expanded scale view of a typical GPA pulse train.

   3.2 To insure that the proper pulsing is being received by the thyristor module, place the scope prober to the gate (G) and cathode (K) terminals of the pulse transformer assembly of the 1 TH thyristor power module. Terminal G is positive with respect to terminal K.

   3.3 Scope trace should be similar to figure #7 to ensure that the hard pulse is firing the thyristor. Disregard magnitude and bottom part of trace.

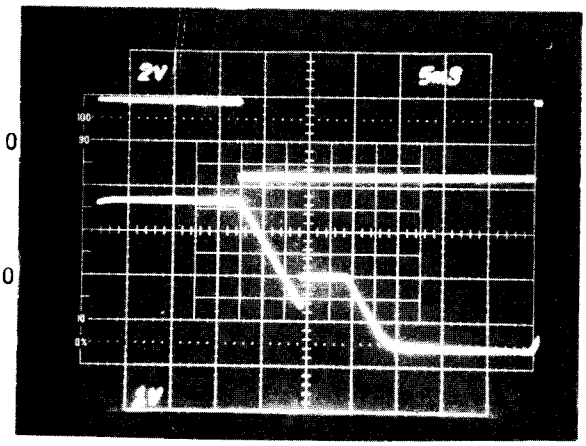
   NOTE: If the gating circuits is incorrect (wiring reversed) than the reset voltage fires the thyristor as shown in figure #8.

   3.4 Proceed to see that the remaining thyristor (2 TH thru 6 TH) of all the "FWD" or "REV" bridges are being fired by the hard pulse.

   This verifies that every thyristor is receiving the "hard" pulse.

INPUT
(-IREF)

OUTPUT
(-I[D]*)



2 V/CM

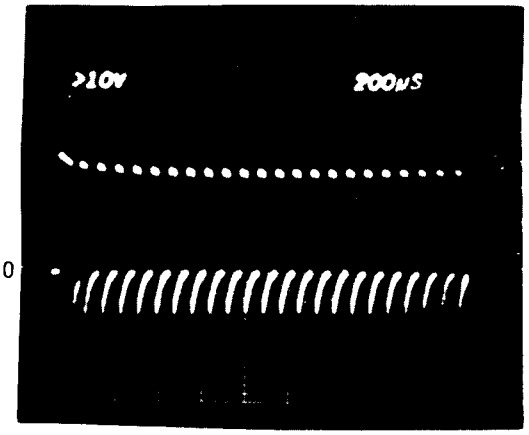
1 V/CM

5 MS/CM

* 4 MS -- DEADBAND

INPUT AND OUTPUT OF CURRENT
REFERENCE RAMP DURING A
CURRENT REVERSAL

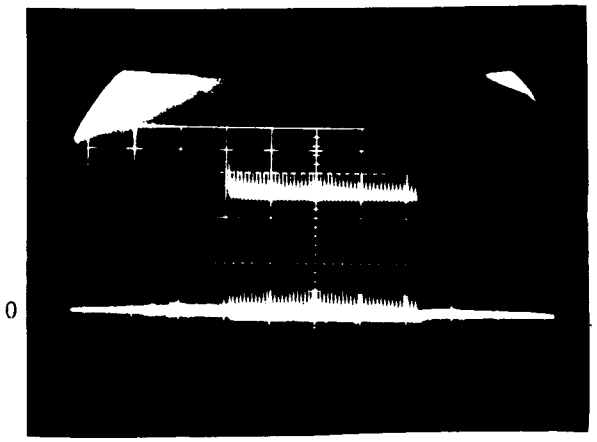
FIGURE #5



10V/CM

200 MS/CM

TYPICAL GPA PULSE TRAIN
FIGURE #6



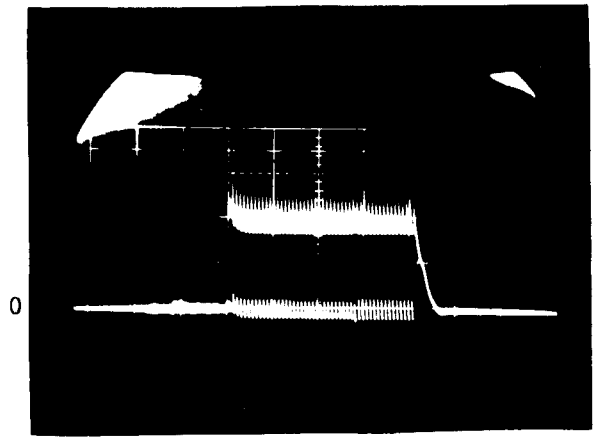
1 V/CM

1 MS/CM

BOTTOM PORTION OF TRACE MAY HAVE NOISE UPERIMPOSED ON IT.

"TYPICAL" CORRECT GPA PULSE TRAIN AT OUTPUT OF PULSE TRANSFORMER ASSY

FIGURE #7



1 V/CM

1 MS/CM

"TYPICAL" INCORRECT GPA PULSE TRAIN AT OUTPUT OF PULSE TRANSFORMER ASSY.

FIGURE #8