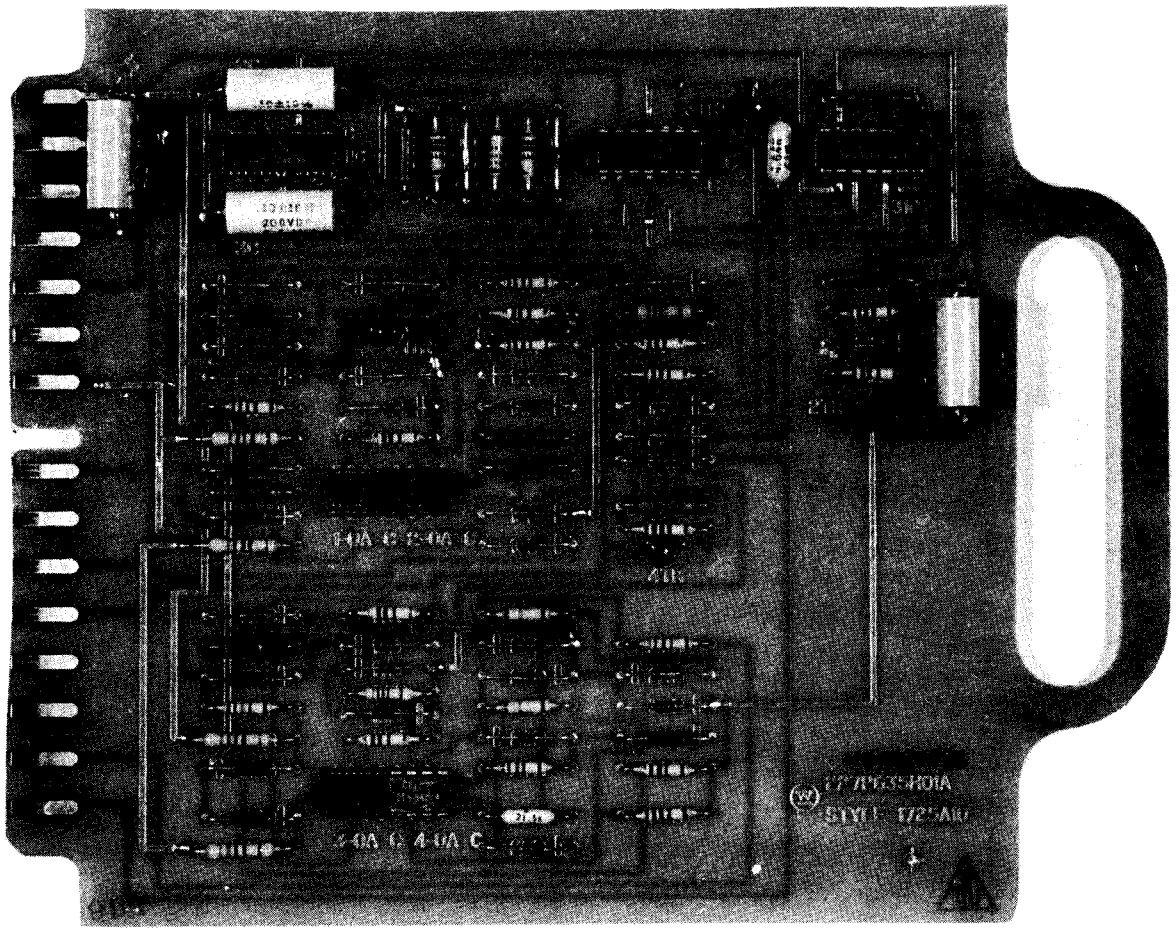
BANK SELECTOR

I. INTRODUCTION

The F80 controller cards are used to provide phase control of a single phase F80 field exciter TPM in either a single converter or a dual converter configuration. The basic F80 cards include the Gate Selector and Driver S#1725A08, the Gate Controller S#1725A09 and the Bank Selector S#1725A10 (used only in the dual converter applications with a field voltage loop).

The Bank Selector, BS, card controls the selection of the forward and reverse thyristors on the TPM assembly by supplying the appropriate enables to the GS&D. In addition, the BS controls the output signal to the gating circuitry by controlling the operation of a signal conditioning amplifier.

Figure 1 is a picture of the BS. A front view locating all components by schematic identification is shown on the last page of the instruction leaflet.



II. DESCRIPTION OF OPERATION

The Bank Selector (BS) card was designed for use with F80 dual converter field exciters and should be used only when regulating a field voltage loop. The BS card controls the selection of forward and reverse gate drivers and allows bank reversal only when a) field current drops below a threshold level and b) the TPM voltage goes discontinuous. A signal conditioning amplifier operates to feed the correct polarity signal to the gating system.

The inputs to this card are as follows:

+V (c) on terminal 51

-V (B) on terminal 21

CP on terminal 33 (from GS&D)

$-|I_f|$ on terminal 57

Circuit operation will be discussed with reference to Figure 2. Amplifier 4-OA and the subsequent circuitry up to transistor 3TR are used to monitor field current. As long as field current is above a threshold value, the output signal from 3TR will be low. This low signal is applied to the clocked RS flip flop terminals S2 and R2 and prevents the flip flop from changing state. When the field current signal drops below a threshold value, 3TR will turn off and the flip flop state will be determined by the output state of the SWITCHING LINE DETECTOR.

The SWITCHING LINE DETECTOR function is performed by 3-OA. This amplifier monitors the voltage controller output +V(c) and the bus voltage signal -V(B). When operating in the inverting mode whether forward or reverse, the output signal from this amplifier maintains a consistent signal level until the TPM voltage (and Field Current) goes discontinuous at which time the output level will either go high or low depending upon the signal polarities. The RS flip flop will change state to agree with changed output from 3-OA. The clocked flip flop follows the state of the output of 3-OA once field current drops below the threshold value.

Figure 3 is the operating curve for 3-OA. Normal operation must occur within the limits of points A, B, C and D. Assume that the system is operating at point ℓ in Figure 3 and that the TPM is generating a positive output voltage at an $\alpha = 100^{\circ}$. The output from 3-OA is low. The output from NAND gate 3B is high. The RS flip flop is set such that $\overline{Q}$ = "1" and Q = "0" causing terminals 39 and 35 to be a "1" and a "0" respectively. A "1" on terminal 39 alerts the forward TPM gate drivers; a "0" on terminal 35 inhibits the reverse TPM gate drivers. If the reference polarity changes sign, the system operating point moves from ℓ to m: At point m field current is being removed. Below the threshold point for field current, 3TR will turn off. When the field voltage goes discontinuous, the output from 3-OA will go high and the output from NAND gate 3B will go low. The next clock pulse "1" to "0" transition will change the state of the flip flop such that Q = "1" and $\overline{Q}$ = "0" subsequently causing terminals 35 and 39 to be a "1" and a "0" respectively. Terminal 35 in the "1" state will enable the reverse gate drivers; terminal 35 in the "0" state inhibits the forward gate drivers. The system will then be operating at point n which is calling for reverse TPM voltage also at $\alpha = 100^{\circ}$. The field current detection circuitry will cause 3TR to turn on and no further changes can take place in the bank selection circuitry.

To prevent a forward, reverse overlap condition, the "1" outputs from the RS flip flop are delayed by 0.8 ms before being applied to the output terminals 35 and 39. The zero outputs from the flip flop are not delayed.

Amplifiers 1-OA and 2-OA form a signal conditioning amplifier. In order for the circuitry to operate properly, terminals 35 and 59 must be wired together on the backplane. The transfer curve for this circuit is shown in Figure 4.

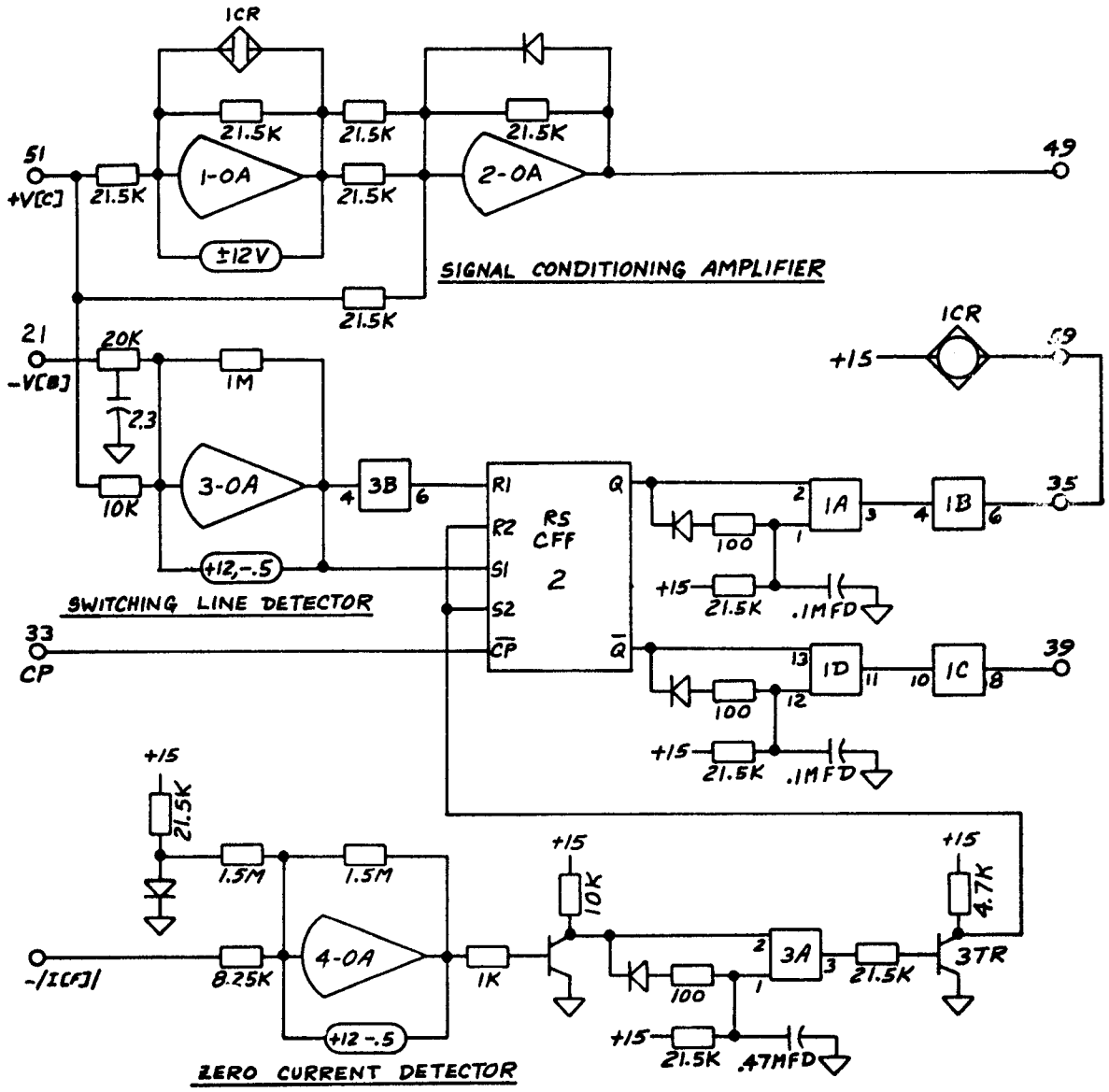
In the forward mode, terminal 35 is low and 1CR is energized. Amplifier 1-OA is reset. In the reverse mode, terminal 35 is high and 1CR is de-energized. Amplifiers 1-OA and 2-OA generate the desired output.

The outputs from this card are as follows:

-V(c) on terminal 51.

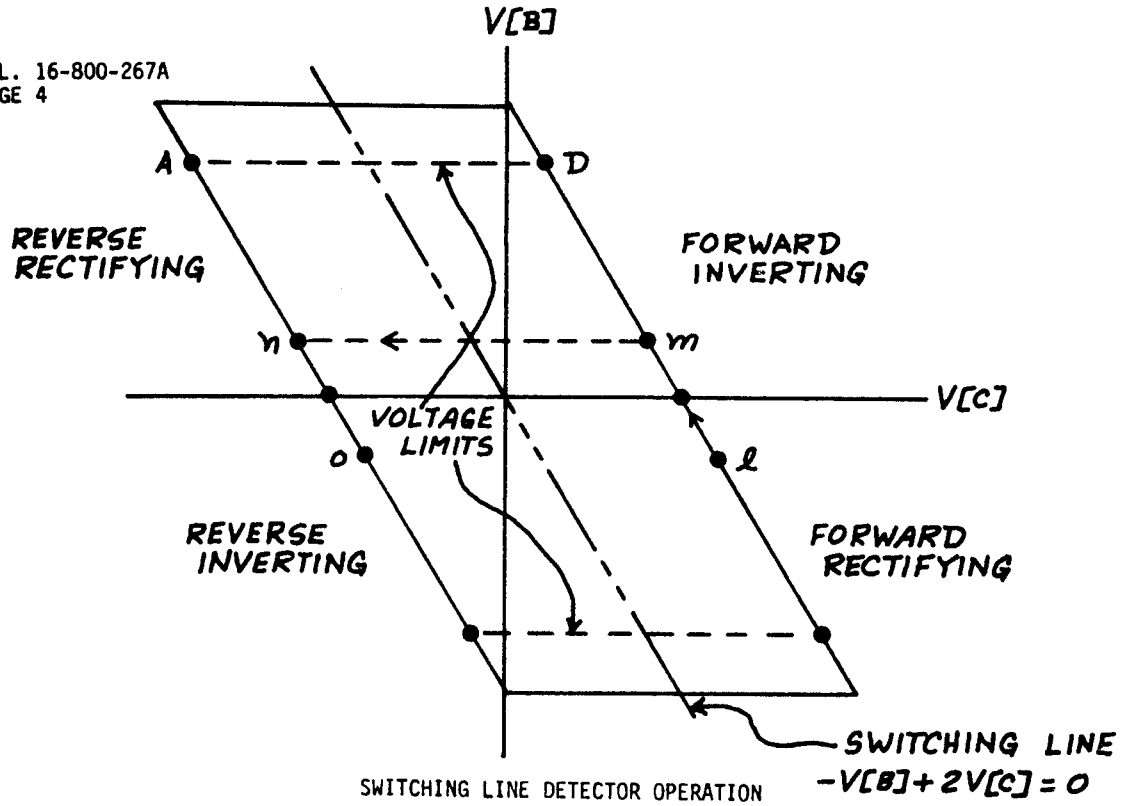
FORWARD ENABLE on terminal 39

REVERSE ENABLE on terminal 35



SIMPLIFIED BANK SELECTION

FIGURE 2



SWITCHING LINE DETECTOR OPERATION

FIGURE 3

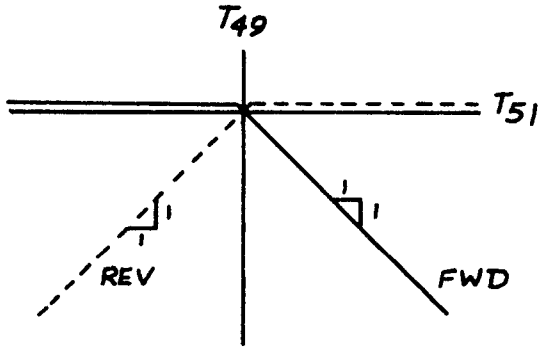


FIGURE 4

III. CHARACTERISTICS AND RATINGS

Zero Current Detector:	Due to non-linearities in the transducer, zero current is detected at around 1 to 2% of 80 Ampere-Turns.
Signal Condition Amplifier:	Gain is unity with normal operation being a negative output voltage.
Power Supplies:	PSP +24V ±1.2V @ 35ma
	PSN -24V ±1.2V @ 35ma
	+15 +15V ±1.5V @ 30ma
Interlock:	RP1 for the GS&D card should be interlocked through terminals 17 and 19 of this card in order to protect the TPM if this card is inadvertently removed with power applied.

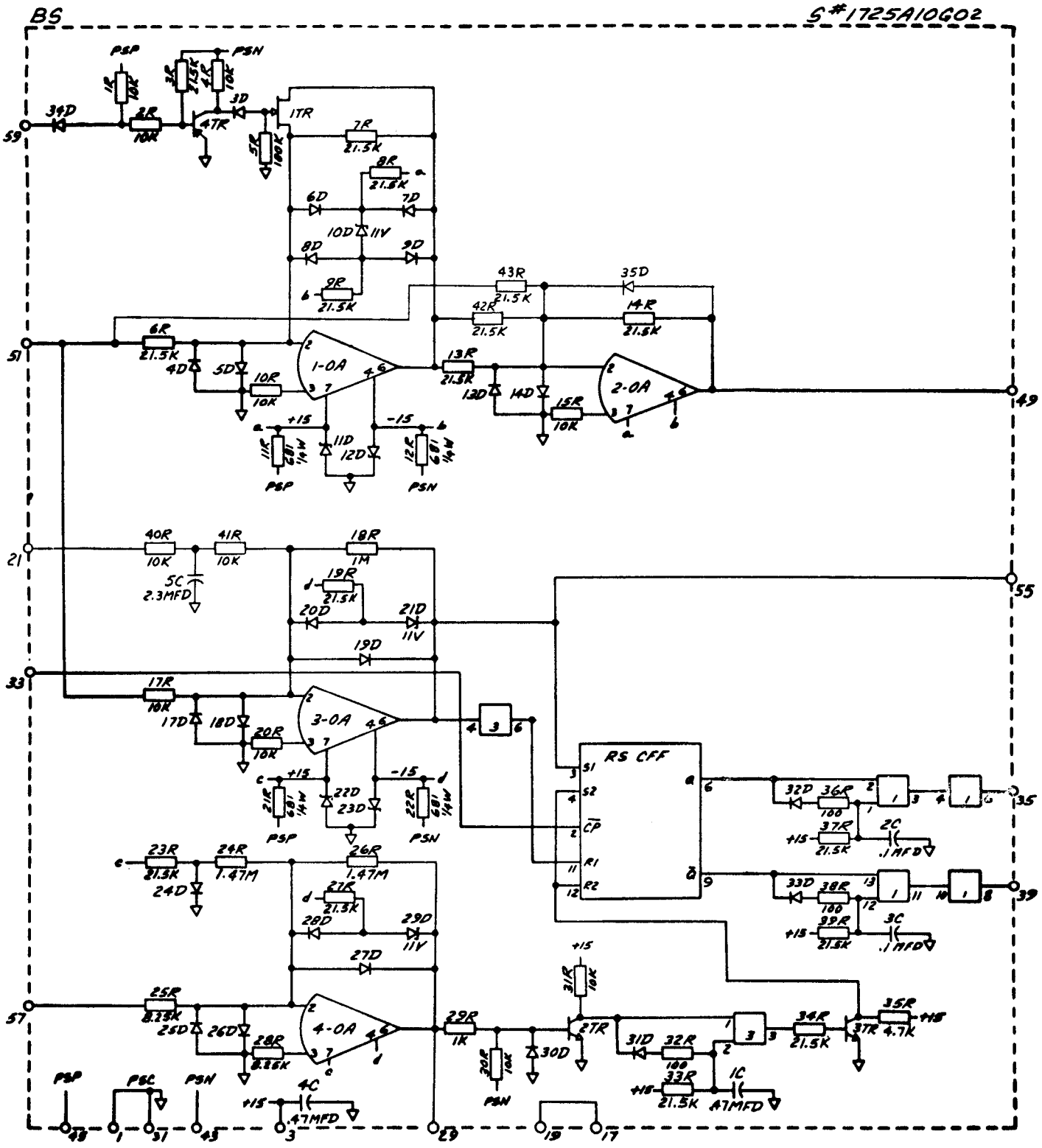

BS
S#1725A10G02
1-0A
2-0A
3-0A
4-0A
RS CFF
+15
-15
PSP
PSN
PSC
ALL RESISTORS ½w, 1% UNLESS OTHERWISE SPECIFIED

FIGURE 5

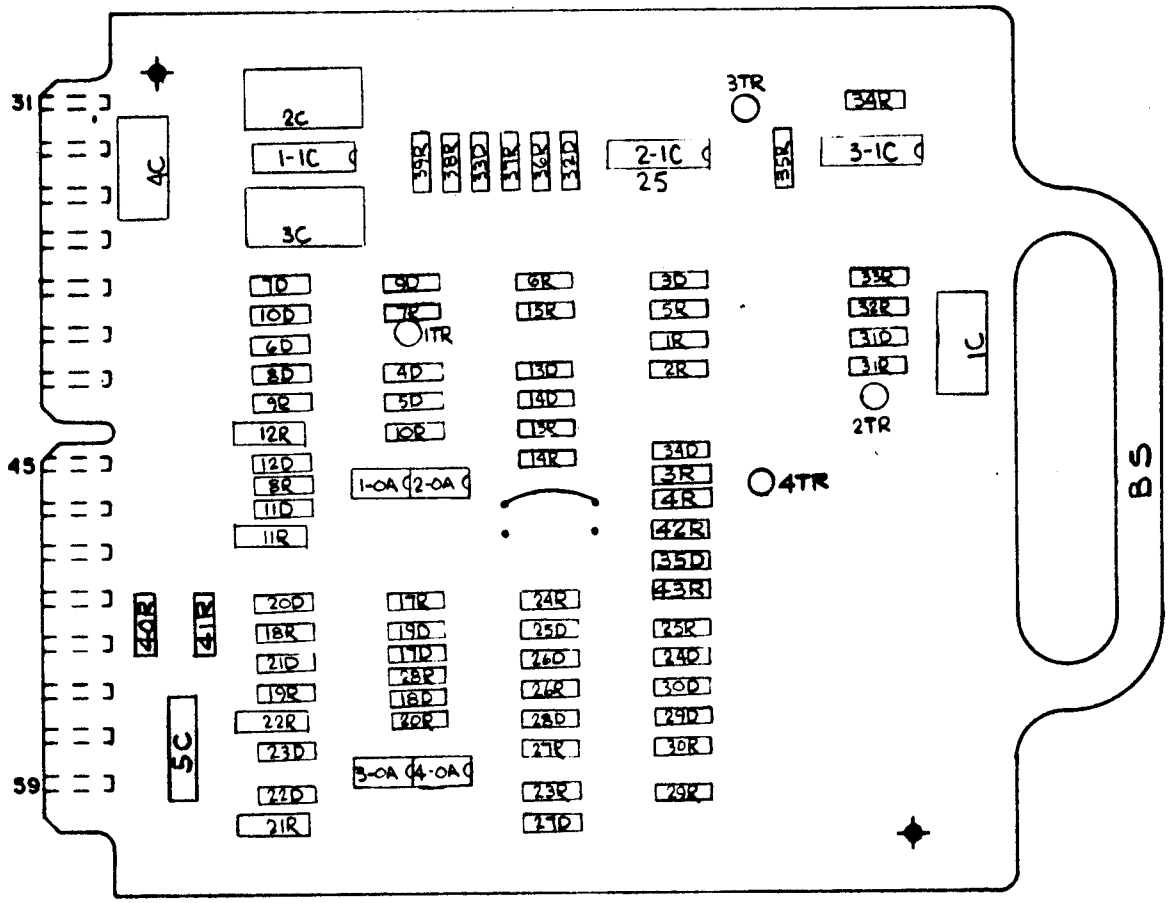


FIGURE 6

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