I.L. 16-800-391

M5C/M4CL
BASIC REGULATOR

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J. INTERFACE AREAS (p. J1)

K. AVAILABLE CAGE OPTIONS (pp. K1-K6)

M5C/M4CL BASIC REGULATOR

A. Introduction

A motor drive system as shown in Figure A1 is designed to provide control of a specific motor parameter such as speed, counter emf, torque, etc. so as to satisfy specific requirements for the job which the system has to perform. In the design of these systems certain parts of the hardware are used repeatedly while other parts have to be specifically tailored to satisfy unique job requirements. The repeating hardware has been categorized as the basic regulator while the tailored hardware is designated the variable regulator.

The basic regulator encompasses an ac to dc power converter, at times an isolating or voltage matching power transformer, electronics to control the power converter by regulating the output current, basic sequencing required for the converter and the motor and basic protection for the converter and the motor.

The variable regulator encompasses the additional electronics required for regulation, interfacing or metering, any additional sequencing or any additional protection required to satisfy the particular job specifications.

This instruction leaflet discusses the electronics associated with controlling, sequencing, interfacing and protecting in the basic regulator. The particular family of hardware is called the M5C/M4CL Basic Regulator. This designation encompasses different power levels in the ac to dc converter.

Figure A2 shows some of the elements in the basic regulator. Input ac to the converter is monitored from a voltage and current standpoint. The converter shown is a single converter and with this type of converter the output voltage can be positive or negative while the output current can be only positive. This is known as two quadrant operation. If each of the thyristors shown is replaced by two thyristors in an anti-parallel configuration, the converter becomes a dual converter in which four quadrant operation is possible. Sequencing is handled by the inputs and outputs. Once the regulator has been sequenced on, the command input is a signal which says regulate for this level of armature current.

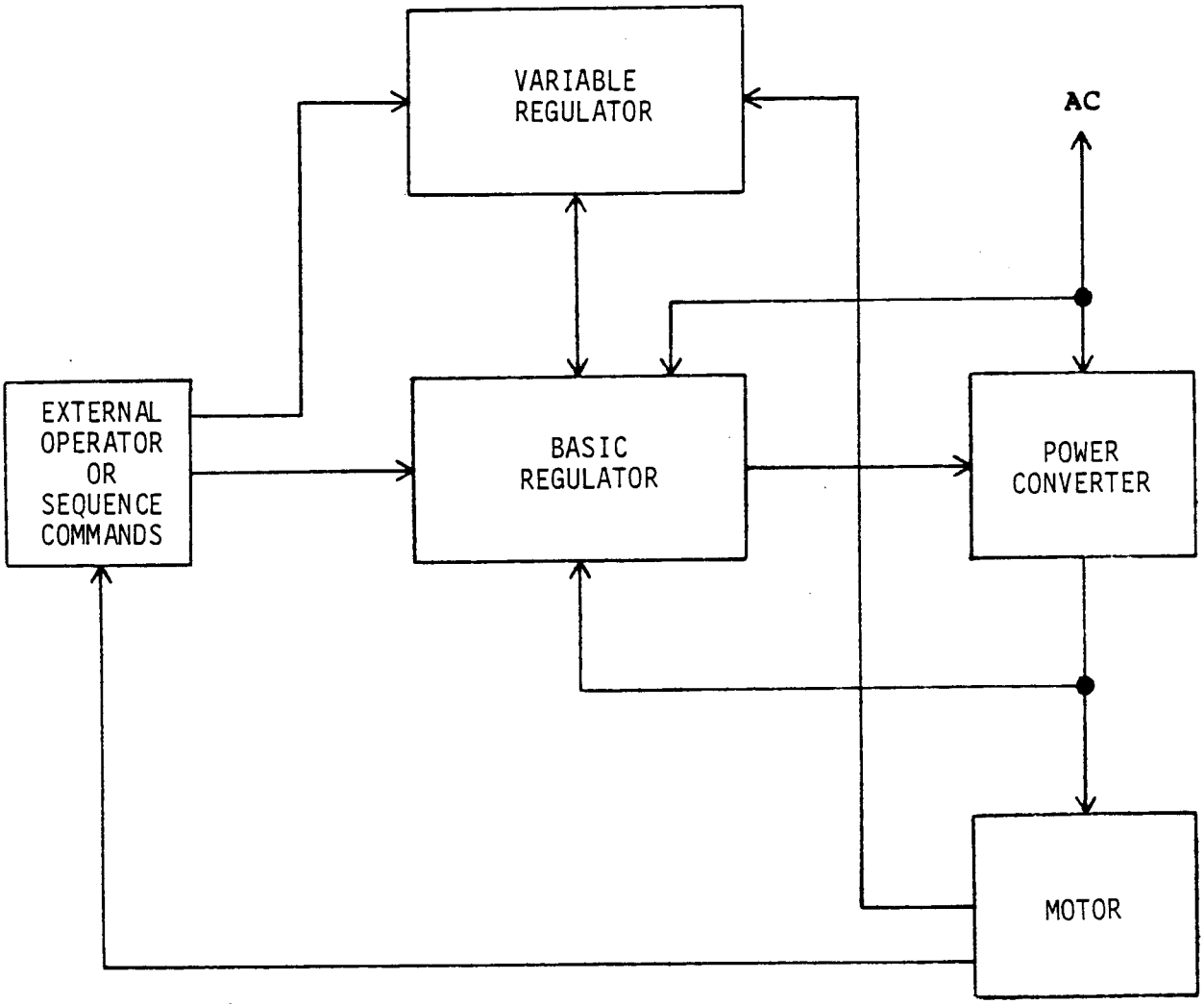
The regulating function provided is a high speed current loop with minimum delay time associated with a bank reversal (a reversal of current in the converter section). The sequencing interfaces with the electrical world outside of the electronics (pushbuttons, relays, limit switches, etc.) and establishes the operating condition of the drive as a function of received command or status or fault information. The protection

function monitors various signals from the motor and from the converter and shuts the system down upon the detection of any abnormalities. Figure A3 is the current regulator block diagram of the basic regulator subsystem.

The regulator electronics, basic and variable, are in two separate mechanical packages. The variable regulator electronics can be in the same cabinet with the basic regulator. It is then designated as a local variable regulator. When the variable regulator is in a different cabinet, it is designated a remote variable regulator. There are hardware differences required with a remote variable regulator so as to minimize any communication noise which might occur due to the physical separation and resultant additional wire lengths.

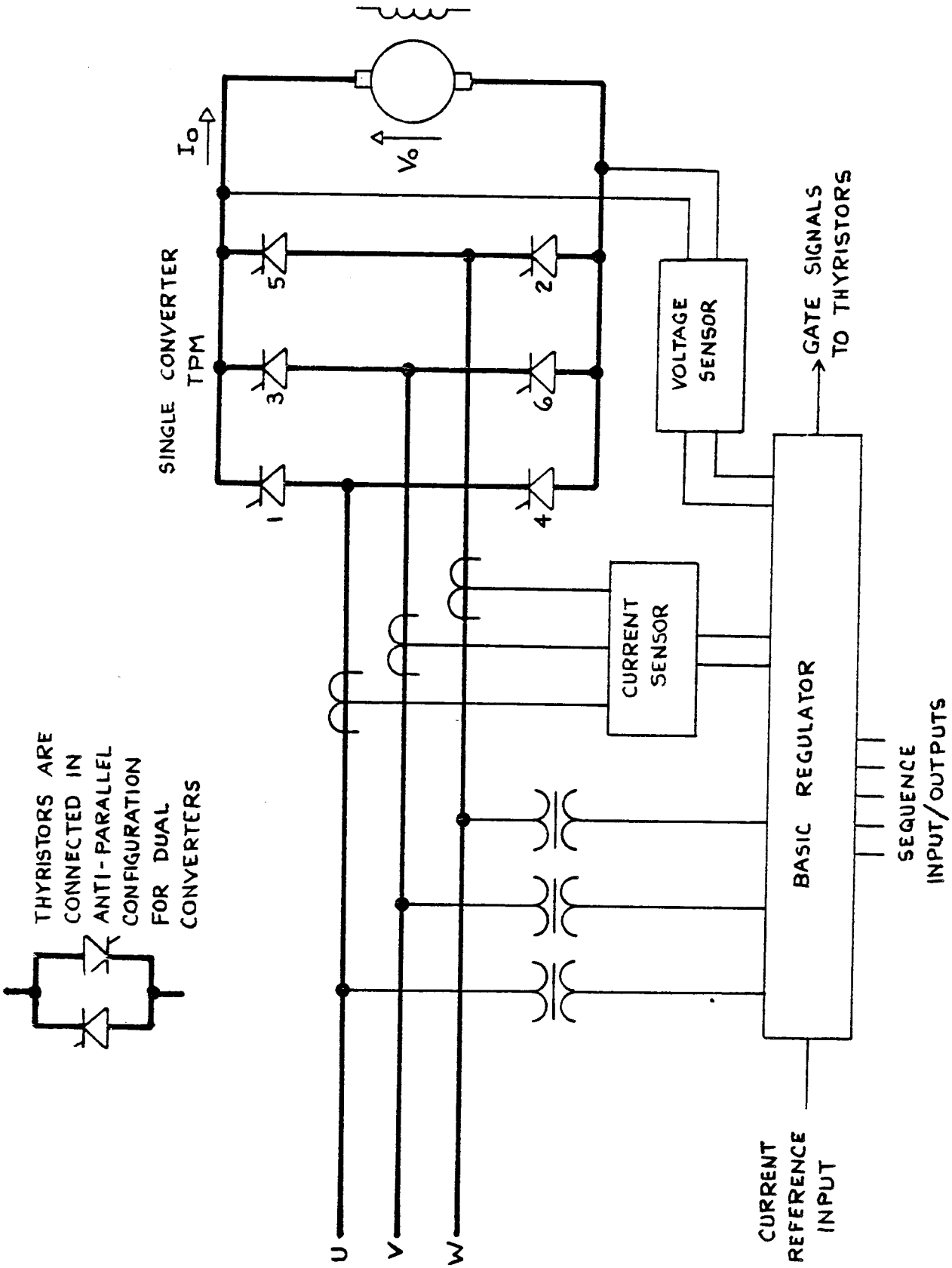
The Basic Regulator electronics as shown in Figure A3 is isolated from the high voltage in the power converter and from the 115V AC that is used for external sequencing. Some of the isolation is located within the regulator electronics while other isolation is externally provided. For example, the 115V AC that is used for sequence control is wired to front edge connected cards in the regulator. Front connection in this case facilitates wiring noise class separation. The AC signals are then optically coupled (isolated) into the regulator cage. In the power converter, ac CT's, step down isolation transformers and thyristor pulse transformers isolate the regulator electronics from the voltage levels within the converter.

The Basic Regulator in conjunction with the power converter generates and regulates motor armature current as determined by the input current reference command +I(D)** of Figure A3. In order to do this, the external circuitry must be properly conditioned so that the correct sequencing status exists and that the correct commands are received to allow the basic regulator to perform its function.



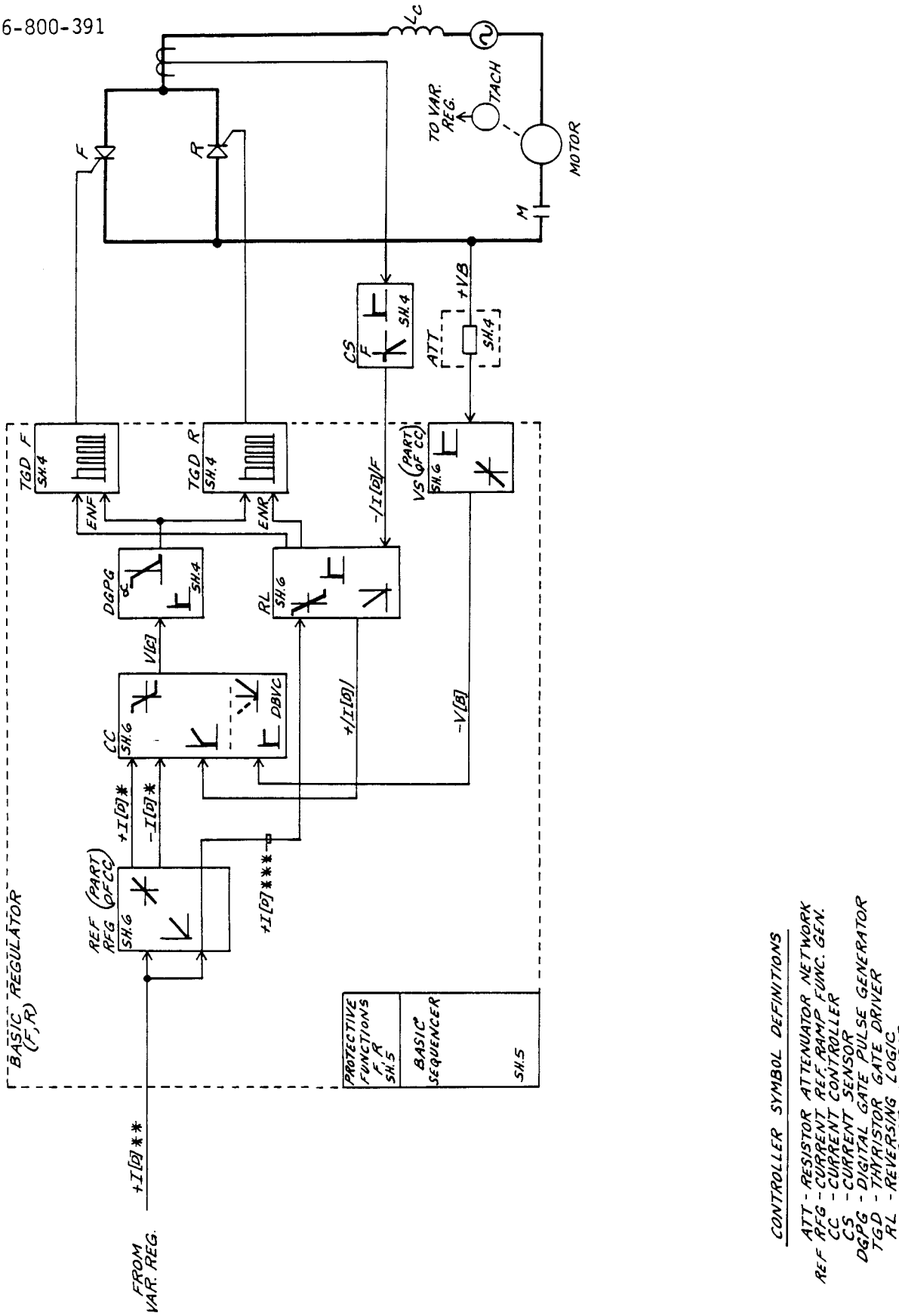
MOTOR DRIVE SYSTEM BLOCK DIAGRAM

FIGURE A1



ELEMENTS OF A BASIC REGULATOR

FIGURE A2



CONTROLLER SYMBOL DEFINITIONS

ATT - RESISTOR ATTENUATOR NETWORK
REF RFG - CURRENT REF. RAMP FUNC. GEN.
CC - CURRENT CONTROLLER
CS - CURRENT SENSOR
DGPG - DIGITAL GATE PULSE GENERATOR
TGD - THYRISTOR GATE DRIVER
RL - REVERSING LOGIC
VS VOLTAGE SENSOR

BASIC CURRENT REGULATOR BLOCK DIAGRAM

FIGURE A3

B. Hardware And LED Identification

The M5C/M4CL regulator electronics are comprised of a basic set of printed circuit cards which are always used in a system and an optional set of printed circuit cards which may or may not be used depending upon the job requirements. The basic card set is always required because it is these cards that perform the basic function of the system. The optional cards provide additional sequencing, more sophisticated fault analysis, additional signal monitoring, isolation from remotely located variable regulators, diagnostic and test capacity, and signal monitoring.

The hardware has been designed such that a particular system can always be expanded to pick up the various options if a customer so desires. The backplane (panel with sockets and associated wiring) always has all edge connectors (sockets into which the printed circuit boards are plugged) and the associated wiring that is required in the most sophisticated system. This allows the hardware package to be manufactured as a standard assembly into which are plugged the standard printed circuit cards and any ordered options.

The standard cards and their location in the cage is as follows:

A22	Input Board
A20	Output Relay Board
A18	Analog Transmitter/Receiver
A01	Power Supply Module
B10	Basic Sequence & Protection
B08	Pot board
B07	Reversing Logic
B06	Current Controller
B05	Digital Gate Pulse Generator
B03	Thyristor Gate Drive (R) - Dual Converter Only
B01	Thyristor Gate Driver (F)

The optional cards and their location in the cage is as follows:

A21	Input Board
A19	Digital Transmitter/Receiver
A15	Meter Board
B22	Interconnect Board
B21	Interconnect Board (w/o test module)
B15	Test Module
B12	Differential Current
B11	Fault Finder

A front view of the regulator is shown in figure B1, the basic regulator, and in figure B2 which shows all options in their respective positions in the cage (except for the B21 option).

On the basic regulator cards, light emitting diodes (LED's) have been designed on the printed circuit boards to provide diagnostic information on the status of the regulator. Three different LED colors have been used with the colors indicating status as follows:

Yellow	Signal Status Condition (On or Off)
Green	On for drive to be fully operational
Red	Off with drive operating
	On only with drive faulted.

The LED status on the basic regulator external interface cards is as follows:

A22 INPUT BOARD

LED NAME	NORMAL STATUS	COMMENTS
ZAPR	ON	ASSOCIATED WITH EXTERNAL SEQUENCING
ZBPR	ON	
ONCR	OFF	ON WHEN CONTACTOR CLOSE PB IS DEPRESSED.
M	ON	OFF WITH CONTACTOR OPEN
PSR RSET	OFF	ON WHEN TPS READY/RESET PB IS DEPRESSED
CCC'	ON	OFF ONLY IF SC & CC RESET OPTION WITH CONTACTOR CLOSED IS USED.

A20 OUTPUT RELAY BOARD

LED NAME	NORMAL STATUS	COMMENTS
PSR1	ON	OFF WITH DRIVE FAULTED (ITOL ERROR, ZONE A NOT PERMISSIVE OR INHIBIT LINE LOW)
PSR2	ON	
PCM	ON	POWER SUPPLY READY (PSR1 ON) AND ZONE B PERMISSIVE
VRLR	OFF	ON WHEN MOTOR VOLTAGE (AND TPM VOLTAGE IF USED) IS LESS THAN 10% RATED.
ONR	ON	OFF WITH CONTACTOR OPEN
GPSR	OFF	ON WITH DRIVE IN GATE PULSE SUPPRESSION

From a sequencing stand point the following priority and procedure is used for drive sequencing as indicated by the the LED's on A22 and A20. LED's are underlined.

1. ZAPR ON

2. DEPRESS TPS READY/RESET
   a. PSRRSET ON WITH PB DEPRESSED.
   b. PSR1 AND PSR2 ON WITH PB DEPRESSED.
   c. PSR1 AND PSR2 ON WITH PB RELEASED.
   ONLY IF NO FAULTS EXIST (INH' & ITOL' ARE ONES)

3. ZBPR ON

4. PCM ON

5. DEPRESS CONTACTOR CLOSE PB.
   a. ONCR ON WITH PB DEPRESSED.
   b. ONR ON ONLY IF VRLR ON (VRL LED ON BS&P MUST BE ON).
   ON LED ON BS&P STAYS ON WITH PB RELEASED TO INDICATE LATCHING OF ON COMMAND.

6. M ON INDICATES THAT CONTACTOR HAS CLOSED.

7. AT THIS POINT THE BASIC REGULATOR IS READY TO GO. IT IS NOW WAITING FOR COMMANDS TO RELEASE THE CURRENT CONTROLLER AND THE CURRENT REFERENCE RAMP TO BE FULLY OPERATIONAL.

The remaining LED's on the basic system provide the following information.

1. PSOK (PS) — Normally ON with power supply operational If LED is out check power supply voltages and fuses in assembly.

2. ON (BS&P) — ON with contactor closed.

3. VRL (BS&P) — ON with motor voltage < 10%. OFF with motor voltage > 10%.

4. GPS (BS&P) — ON when drive has faulted.

5. FWD or REV (RL) — Indicates polarity of current reference signal (this is applicable even for single converters) and converter section being gated (+REF FWD: -REF REV).

6. 1CRDB (CC) — When this LED is out, the current reference ramp output is reset to zero and the regulator

must appropriately respond. When the LED is ON, the current reference is dependent upon the input signal and any delay produced by the ramp circuit.

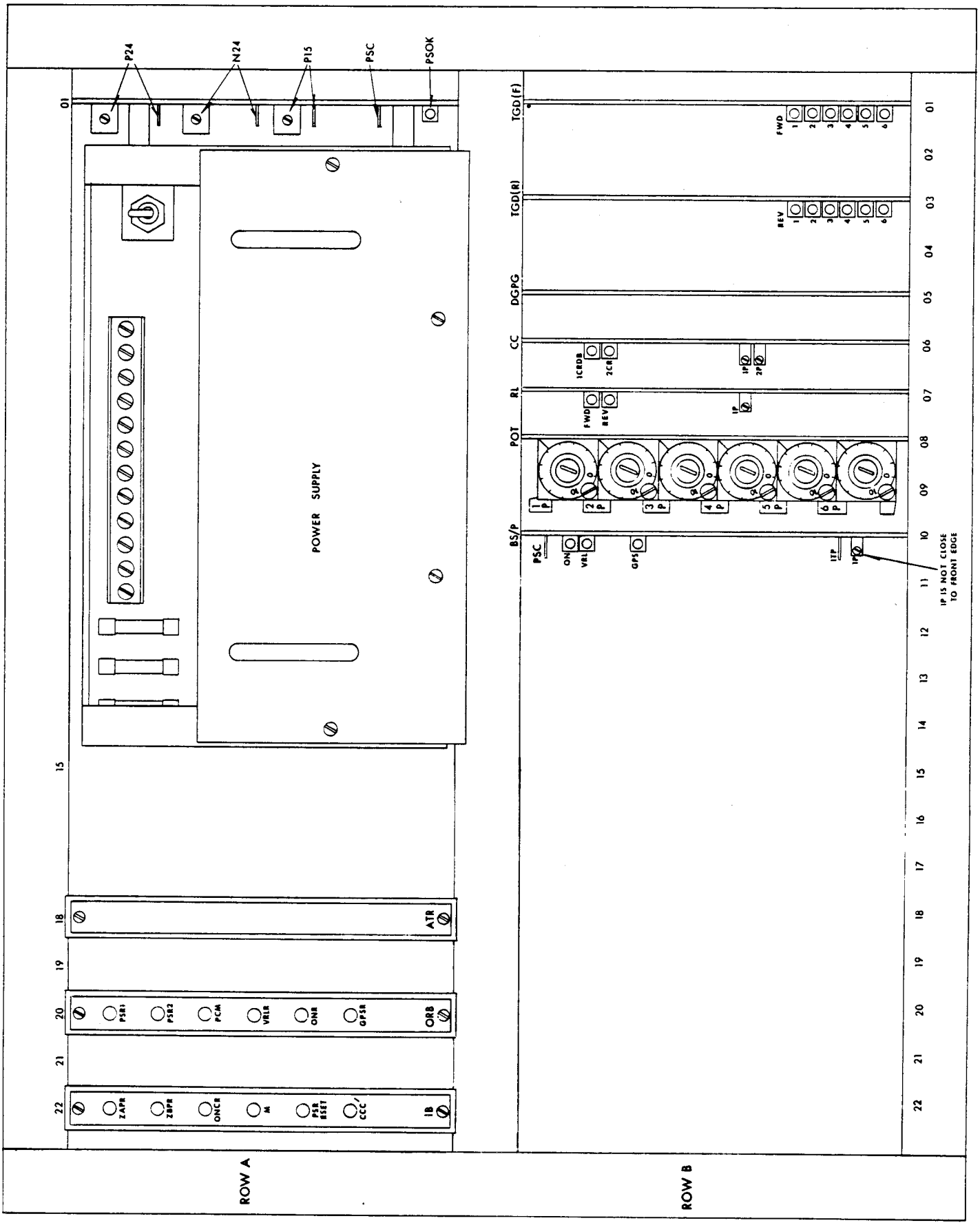
7. 2CR (CC) — When the LED is out, the current controller is reset and the gating angle is approximately 140°. When the LED is ON, the current controller regulates for the input reference.

8. TGD LEDS FWD/REV — The six LED's on the TGD card indicate that gating pulses are being transmitted by the appropriate driver channel. Normally one set of TGD LED's will be on uniformily and the LED's that are ON should agree with the FWD or REV LED's on the RL card.

From a quick check standpoint, the red GPS light indicates that the drive has faulted and it must be appropriately reset before restarting. The two green LED's (1CRDB and 2CR) on the CC card indicate the regulating mode of the regulator. With both LED's ON the system is fully operational. With both LED's OFF the system is completely reset. With 1CRDB OFF and 2CR ON, the CC card holds the current to zero. These are the only valid modes for these two LED's.

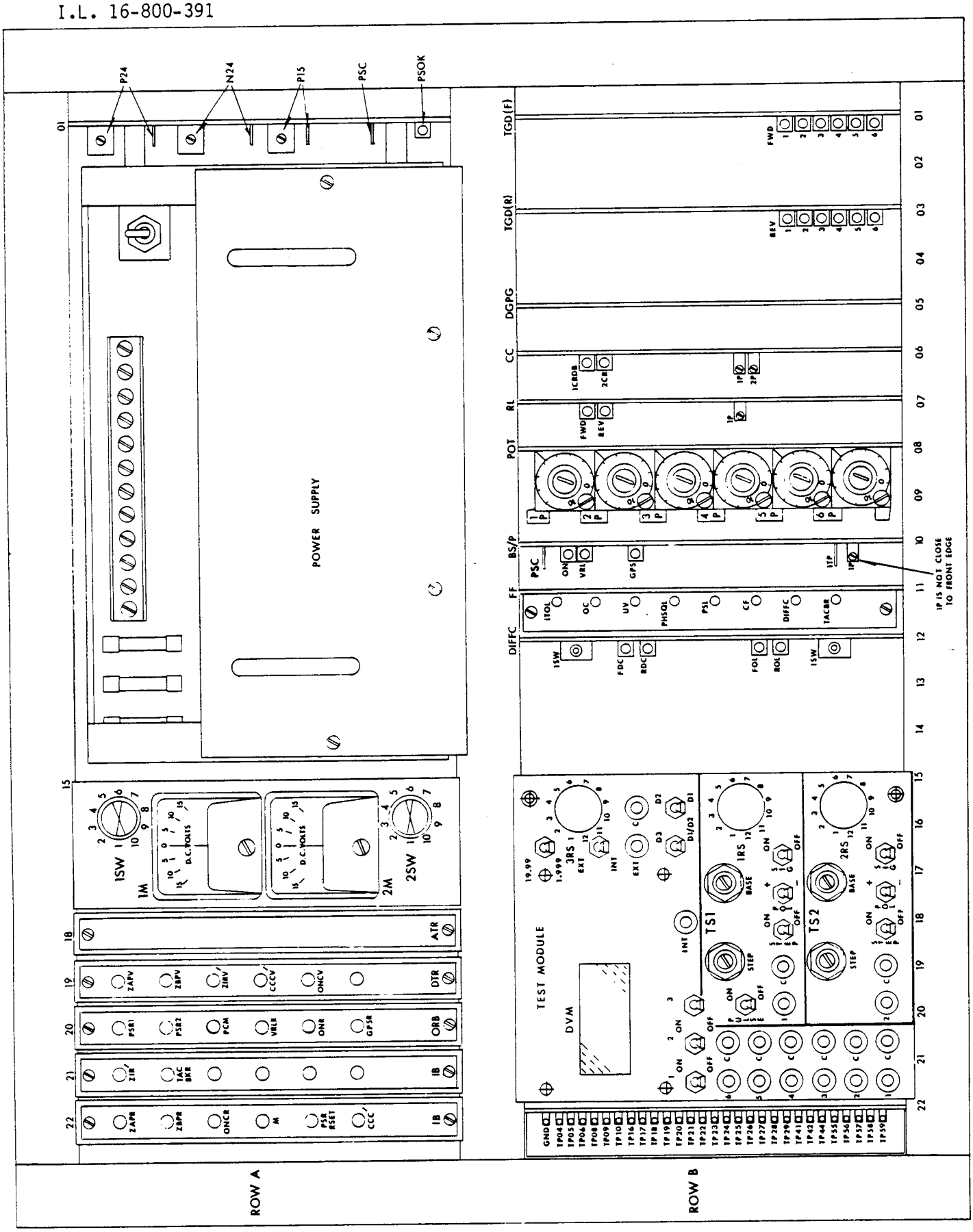
On the basic system, if the ON LED on the BS/P card is ON, the two green LED's on the CC card should be ON unless the CCC' LED (A22) is out. When the system expands with additional input sequence options, there is an additional signal (ZIR) which can be used to control 1CRDB with the contactor closed. On a basic system where the CCC option is not used, closure of the contactor as indicated by the auxiliary signal fed back to the regulator releases the current controller and the current reference ramp.

In the basic regulator, some of the printed circuit cards are interlocked through wiring on the cards to prevent the generation of any gating pulses if the appropriate cards are not plugged into the cage. These cards are the Reversing Logic in B07, the Pot Card in B08 and the Basic Sequencer and Protection Card in B10. Removal of any of these cards will automatically inhibit pulse amplification on the Thyristor Gate Driver Card(s).



FRONT VIEW—BASIC CAGE

FIGURE B1



FRONT VIEW— BASIC CAGE WITH ALL OPTIONS

FIGURE B2

C. Basic Interface Cards

The standard interface cards used with the basic regulator are shown in Figures C1 through C4. The input board (Figure C1) utilizes optical couplers to isolate the regulator electronics from the external 115V ac which is used for the external switches, lights, contacts, etc. The output relay board (Figure C2) utilizes mercury relays to provide this isolation. The ATR board (Figures C3 & C4) provides analog buffer isolation for external communication.

On the input boards, when 115V ac is applied to the input terminals (i.e., F1 and F3 in Figure C1), the associated LED (ZAPR) on the front connector assembly is lit indicating that current is flowing in the input circuitry to the optical coupler. With 115V ac applied to the input terminals, the output terminals 1Z and 1Z' should be a logic one and a logic zero respectively. When 115V ac is removed, the associated LED should extinguish and the corresponding output terminals should change state: 1Z = 0 and 1Z' = 1.

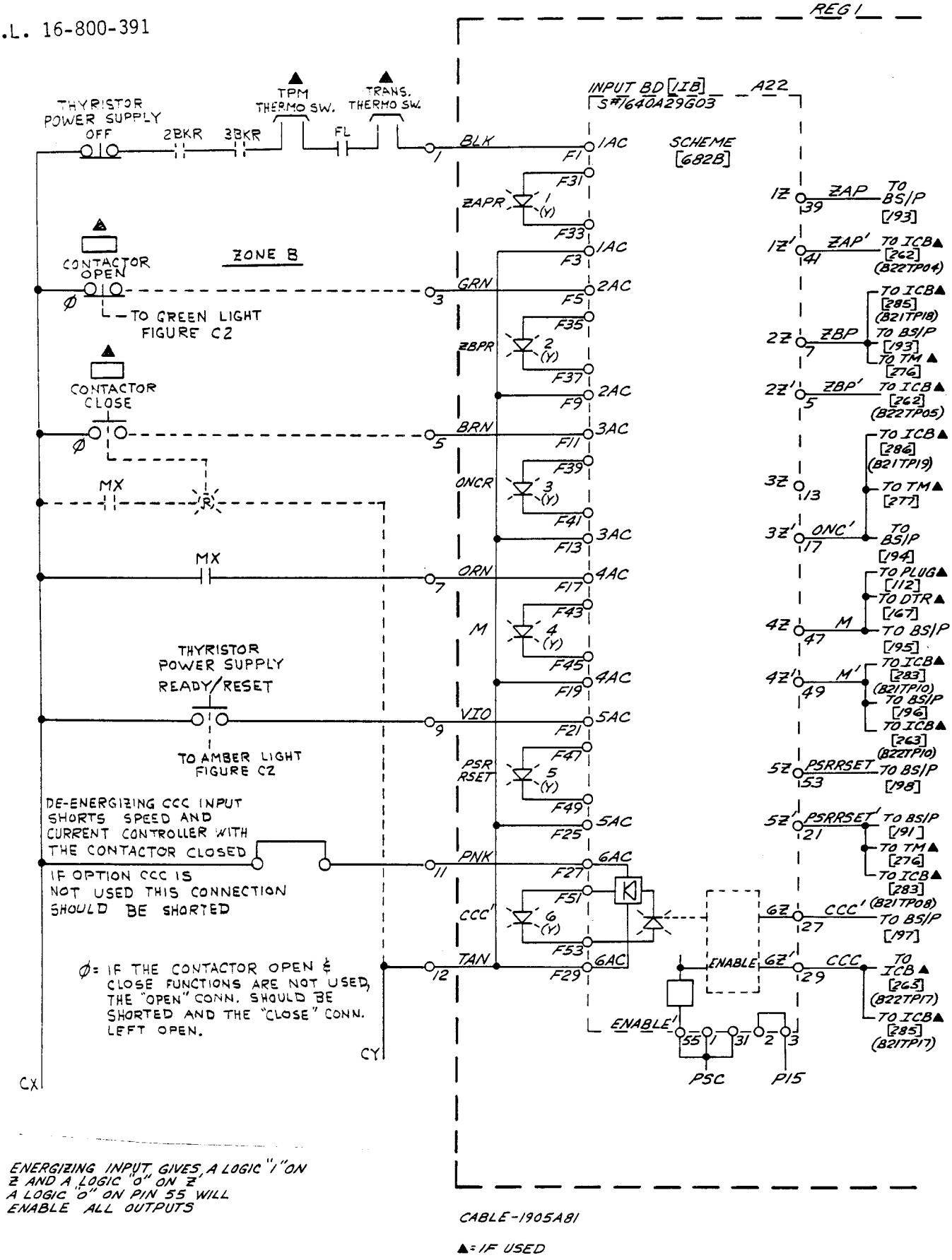
The output relay board (Figure C2) uses a single normally open mercury relay contact per relay. The relay is energized when the appropriate LED on the front connector assembly is lit indicating that energizing voltage has been applied to the relay coil. The output mercury wetted contacts should have some form of noise suppression across the load. This could be a type B suppressor across an AR type relay or an OTTF transformer type indicating light. For resistive loads refer to drawing 1482A88 for the required contact protection.

The output relay board also interfaces with door lights which indicate system status. Once the drive has been reset and this must be done at the drive cabinet (Thyristor Power Supply Ready/Reset Pushbutton) control is available to an operator. If a fault occurs the drive will shut down and cannot be restarted until a reset is generated at the equipment. In order to make the faulted drive more noticeable, the pushlite associated with the TPS Ready/Reset pushbutton will operate in a blinking mode until the drive is reset.

With a local variable regulator there is direct wire communication to and from the basic regulator. The ATR card in Figure C3 provides only an isolating buffer between the analog signal and the external meters.

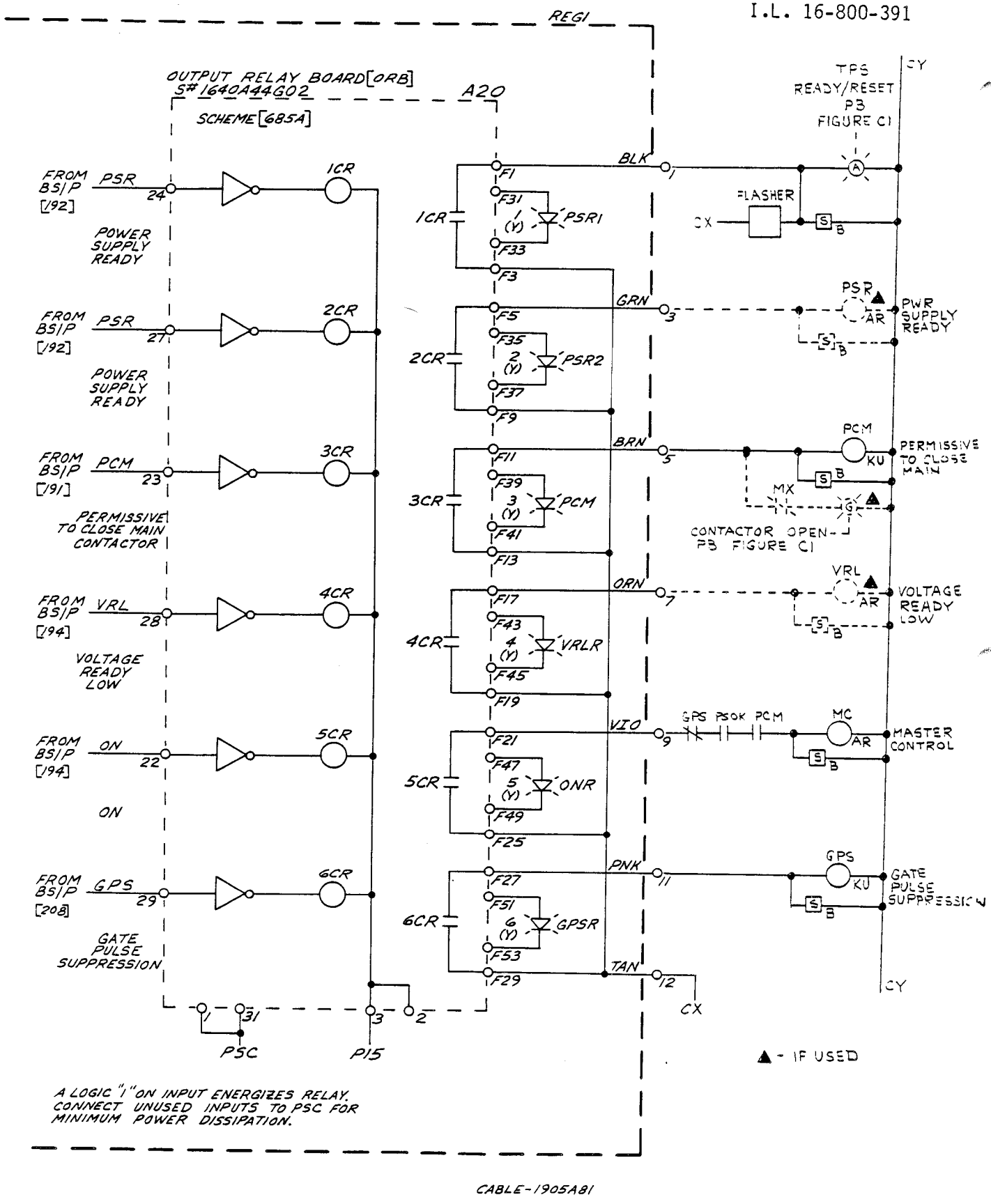
With a remote variable regulator, differential transmission and receiving is used with analog signals as shown in Figure C4. This technique minimizes the effect of any common mode noise pickup that may occur on the wiring. The external meters are again buffered for noise isolation.

The associated figures may not be complete. They are included for explanatory purposes. Refer to the job schematics for the completed wiring in the system.



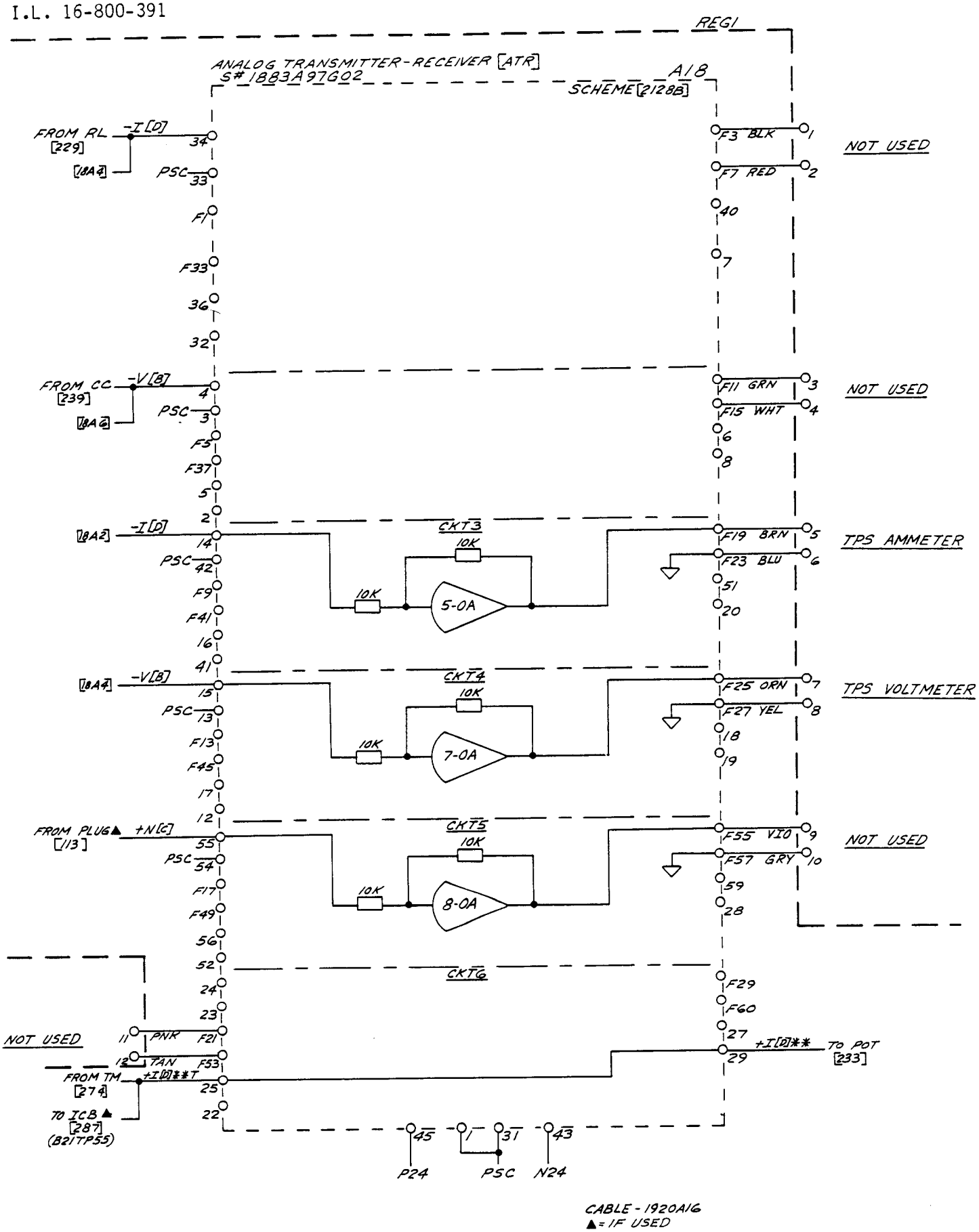
BASIC REGULATOR - INPUT LOGIC

FIGURE C1



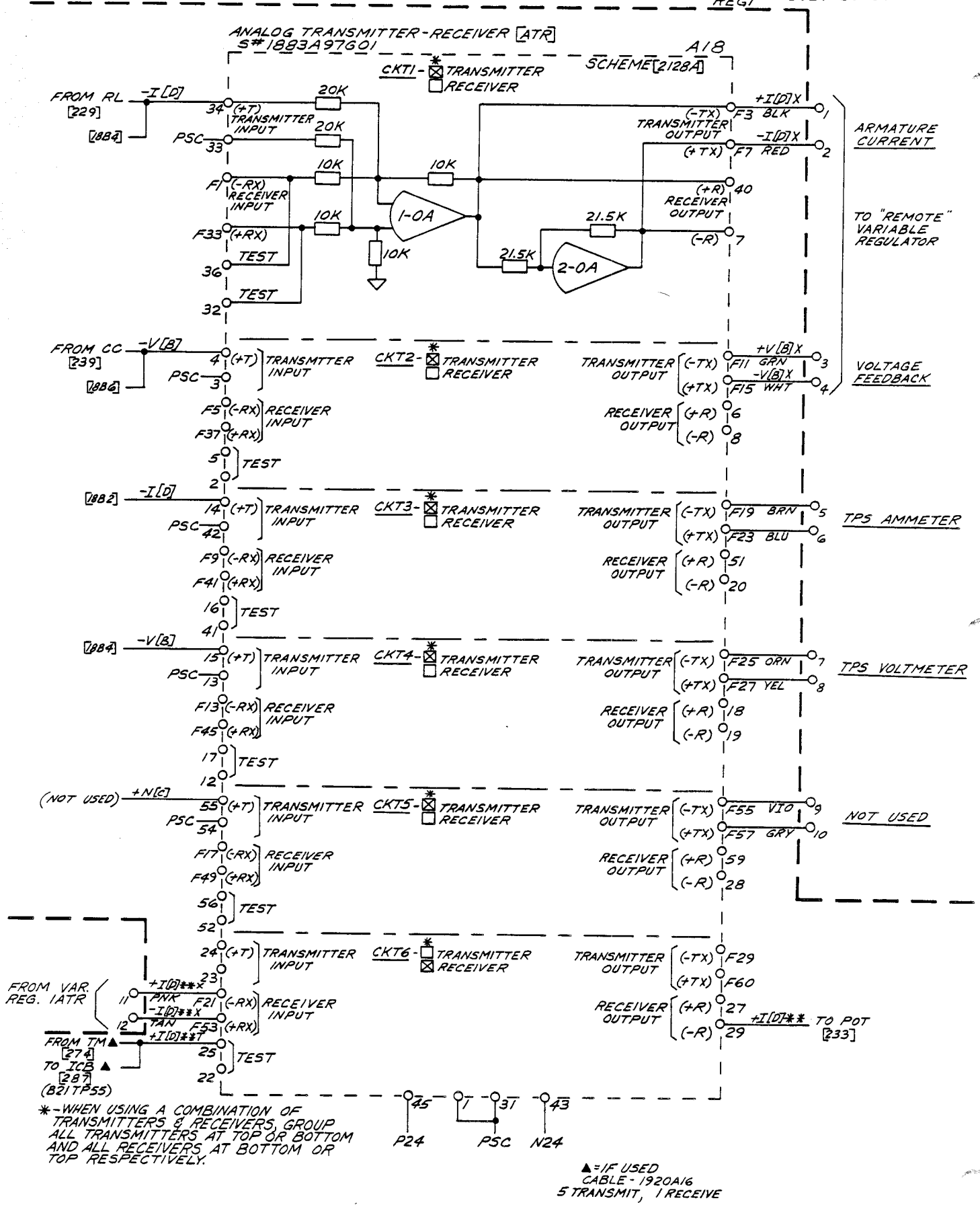
BASIC REGULATOR - OUTPUT RELAY

FIGURE C2



ANALOG INTERFACE
WITH LOCAL VARIABLE REGULATOR

FIGURE C3



ANALOG INTERFACE
WITH REMOTE VARIABLE REGULATOR

FIGURE C4

D. Basic Sequencing & Protection

The Basic Sequencer and Protection scheme is shown in Figures D1 and D2. The simplified scheme is separated into a sequence sheet Figure D1 and a protection sheet Figure D2.

Some of the logic signals shown on the diagram are associated with the use of the DTR option. This discussion assumes that these signals are not present. On a particular system where these signals are used. then the appropriate conditions must be satisfied for the function being exercised.

If the drive has faulted and has not been reset, the pushlight Thyristor Power Supply Ready/Reset will be flashing on and off. Once the drive has been reset the light will remain on.

The drive can be started as follows. Assuming that all external conditions required for the Zone A signal are satisfied (ZAP = 1), depressing the external pushlight Thyristor Power Supply Ready/Reset should clear any faults if they exist and/or set a flip flop which through external circuitry (via PSR signal) causes the associated pushlight to come on.

Subsequently, assuming that all external conditions required for the Zone B signal are satisified (ZBP = 1), an external Permissive to Close Main Signal (PCM = 1) is generated which is used externally to energize relay PCM. Contacts of this relay provide a permissive for energizing relay MC.

With Zone B satisfied, the external Contactor Close pushbutton can be depressed. If the motor voltage (and the TPS voltage when used) is (are) below 10% of rated voltage as indicated by the on VRL LED, the close contactor signal (ONC' = 0) will cause a flip flop to be set and through external sequencing (via ON signal) the drive dc contactor (M) will close.

An auxiliary contact from M is fed back into the regulator to indicate that the contactor close function has taken place. If the contactor does not close within 2 seconds after initiation, a contact failure signal (CF' = 0) is generated which shuts the drive down by gate pulse suppression and changes the Ready light on the door to a flashing mode (prior to the fault, the light was on steady). With the contactor closed and with signal CCC' (T48) in the one state, NAND gate 0 has two inputs 1's and NAND gate P has an output 1 which is applied to the CC card to release the current controller. With logic signal ZIR' a one, NAND gate Q has three input one's and the signal 1CR on T16 should be a one which when applied to the CC card releases the current reference ramp. The 1CRV signal is applied to the variable regulator to initiate release of the speed controller. For basic operation, the contactor close function releases the current controller and the current reference ramp in the basic regulator.

The ZIR option allows independent control of the current reference. With signal ZIR' normally a 1, the signal 1CR will go to a 1 after the main contactor is closed. If ZIR' is a zero, the current reference ramp will remain reset until the signal ZIR' is changed to a 1. This option, when used, allows the current reference to be reset at any time forcing the system to zero current with the contactor closed.

Option CCC allows the current controller and the current reference ramp to be reset with the contactor closed. The only restriction is that the associated voltage ready signal (VRL) and the EXTVRT signal (if used this signal would be applied to terminal 46 of BS/P card) be both 1's which allows the reset function to take place only at low motor voltage. If the drive was running and CCC' was changed from a 1 to a 0 no action would take place until both VRL and EXTVRT are both 1's. Some other action into the variable regulator must take place to slow the drive down. When the VRL signals reach the appropriate state, all controllers are reset through the processing of CCC' = 0.

Notice that the signal (RESET') used to reset any fault indication is not operable unless the contactor is open (ON' = 1). The external Thyristor Power Supply Ready/Reset Pushlight inputs the signal PSRRSET to NAND gate T which if ON' = 1 outputs a low RESET' signal which resets the regulator.

The basic drive protection is shown on Figure D2. The faults monitored are as follows:

Fault	Signal Name	Pertinent Data
Inverse Time Overload	ITOL'	Per Curve on Figure D2
Overcurrent	OC'	Per 1J Setting on Pot Board in position B08
Single Phase or Undervoltage	UV'	85% of Nominal
Phase Sequence	PHSEQOK	
Power Supply	PSOK	Loss of fuse in power supply module

Optional Drive Protection is as follows:

Fault	Signal Name	Pertinent Data
Differential Current	DIFFC'	Fault occurs when AC and DC currents have a difference greater than 50% of rated current.
AC Breaker Trip	TACBKR'	A signal is applied from the breaker preventing drive system operation with the breaker open

The ITOL curve must be selected by adjusting 1P on this card to the checked voltage as shown in Figure D2. This voltage can be observed by monitoring on the BS/P Card 1TP (see Figure B2) with respect to PSC (use a DVM) and adjusting 1P for the appropriate voltage as marked. This will calibrate for the required curve. The job schematics should be referenced for the correct adjustment of the potentiometer. The setting of the forward overcurrent jumper 1J should also be obtained from the job schematics.

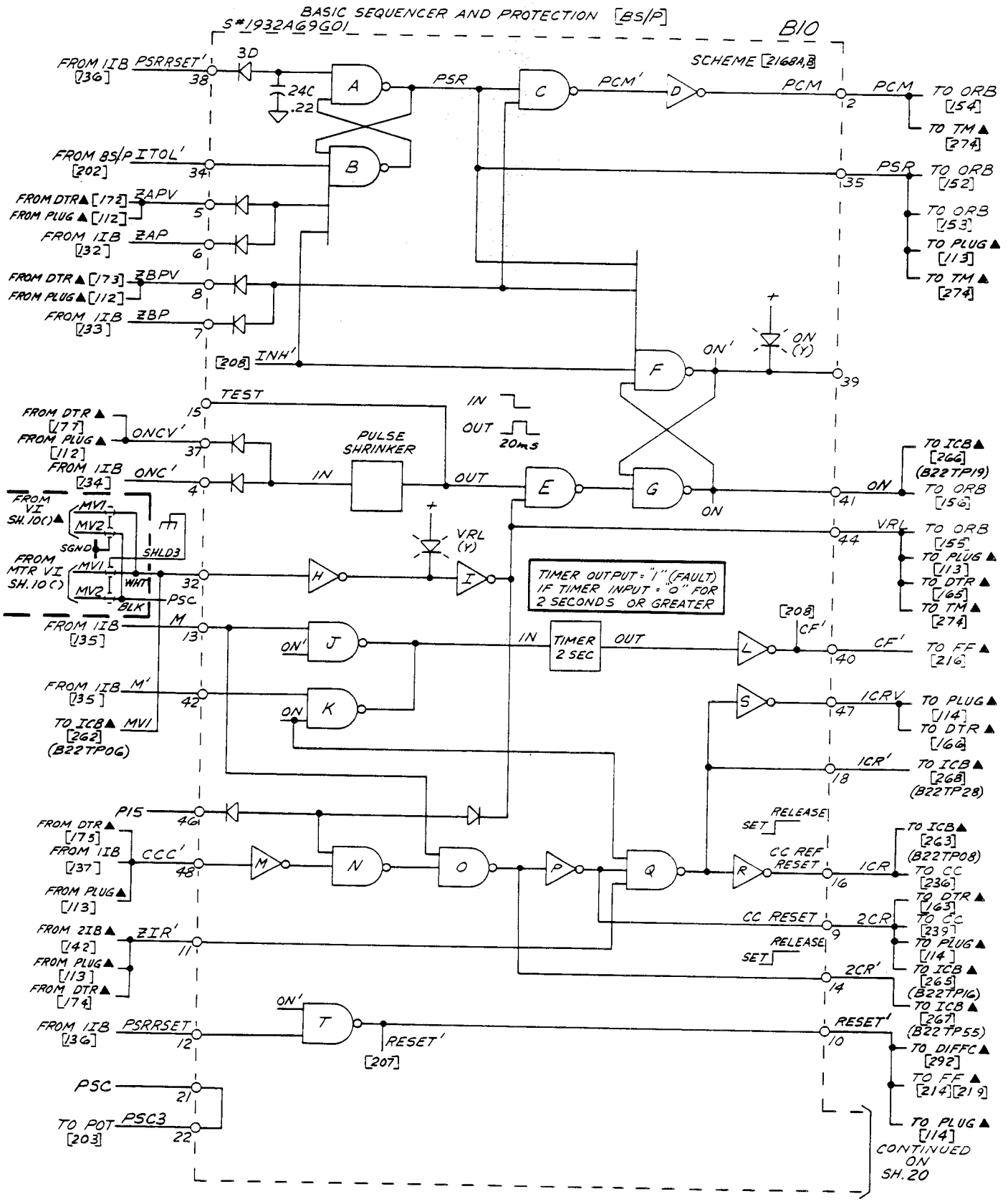
The GPS and INH' logic signals which control the output pulsing are normally in the 0 and 1 state respectively to allow the system to operate. The following conditions will set the fault flip flop which will cause gate pulse suppression and light the GPS LED.

a. OC' = 0
b. UV' = 0
c. PHSEQOK = 0
d. PSOK = 0
e. CF' = 0
f. DIFFC' = 0
g. TACBKR = 0

} if used

The two logic signals GPS and INH' appropriately block the gating pulses and the low INH' signal causes the main contactor to drop out and the power supply ready light to operate in a blinking mode. Depressing the TPS Ready/Reset pushlite should clear the fault circuitry and relight the READY light.

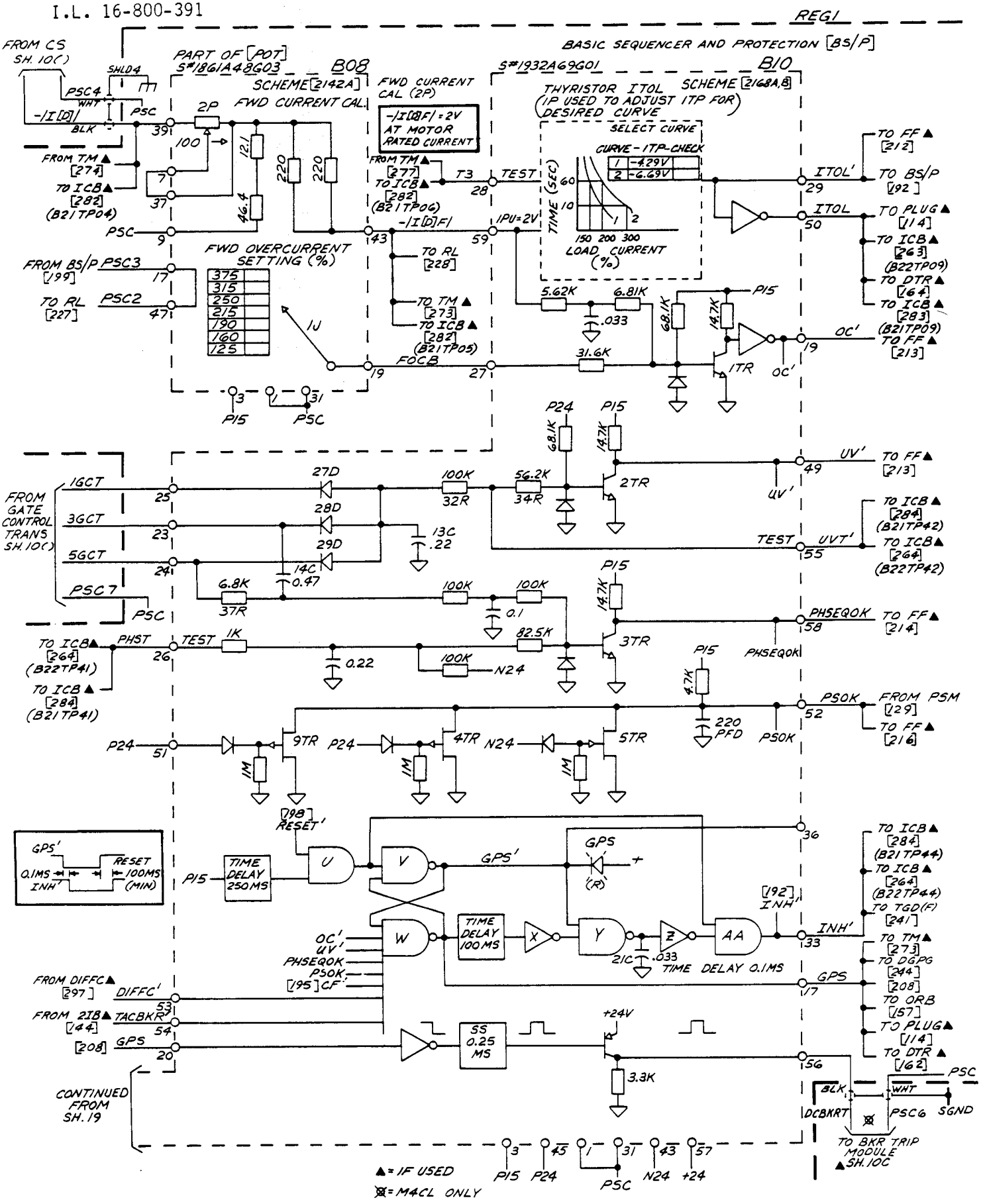
If a Breaker Trip Module is used in the system, the GPS signal going from a zero to a one causes a pulse to be generated which is used to activate the Trip Module and subsequently clear the breaker. This signal is shown at the bottom of Figure D2.



▲ = IF USED

BASIC REGULATOR - BASIC SEQUENCING

FIGURE D1



BASIC REGULATOR - PROTECTION

FIGURE D2

E. Reversing Logic

The Reversing Logic card (See Figure E1) provides control of the reversing process when it is initiated by a reference polarity change. The input reference signal on terminal 55 is checked for polarity and when the output of the polarity comparator (CMP1) and the status of the directional flip flop (via signals FD and R) do not agree, a bank reversal is started. See signal RR in the timing diagram, Figure E2.

The reversing logic card requires two simultaneous conditions to complete a reversal. First the command polarity must be different from the present status of the drive. This difference is indicated when the RR signal goes from a zero to a one. Second, the drive current must be below a low threshold level which is typically less than 0.3% of rated current. This is indicated by the logic signal ZI1 going from a zero to a one. When ZI1 and RR are both ones, a proceed with reversal signal is generated.

NOTE: The RL Card is also designed for use on a twelve phase system which requires RL interlocking for such a system. When used in a six phase system, wiring between terminals 11 and 19 and between 15 and 17 forces the signal IC to be a one and the signal ZI2 to be the same as ZI1. This limits the simultaneous required conditions to two. When used on a twelve phase system, the input signals to terminals 17 and 19 would be ZI2 and CFD(B)2 respectively in the first six phase system. The numeric numbers would change on the second six phase system. On a twelve phase system, both regulators must see the same command, both must request a reversal and both must have zero current before a bank reversal is allowed to take place.

When the PWR' signal goes from a one to a zero, timer TM2 is triggered which subsequently triggers TM1. The timed signal (from the 4ms TM2 timer) EN blocks output gates F and G so that both the forward (ENF) and the reverse (ENR) thyristor gate driver enables are forced to zero inhibiting any pulsing during this 4ms window. When TM1 is triggered the signal PTR (0.3MS in time) allows the information from the reference polarity comparator to be transferred into the directional flip flop. After the 0.3ms the information transfer gates B and C are blocked. After the 4ms period the output driver enables are allowed to go to their natural state. With the drivers enabled, thyristor pulsing is generated and current is allowed to pick up in the opposite direction.

The timed signal EN is also applied to the current controller card. During this 4ms window the current reference ramp is reset and a precharge voltage is applied to the integrating capacitor to minimize slewing time of the current controller operational amplifier when it attempts to generate current after a current reversal. Output signal FWD(B) provides

directional control on the current controller card for maintaining a unipolar reference and for generating the correct precharge voltage.

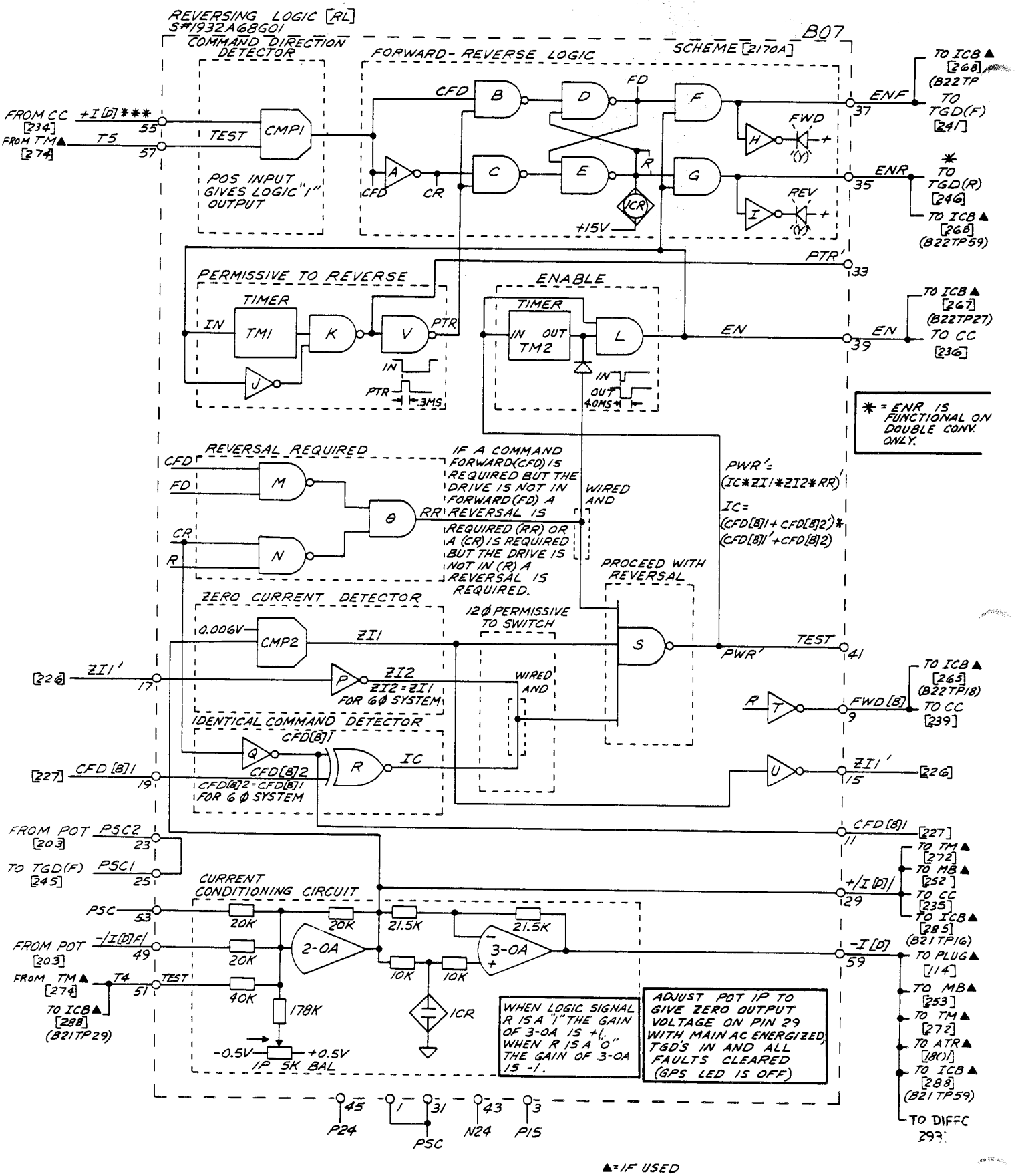
The RL card also contains a current conditioning circuit. Amplifier 2-0A buffers the current signal. This amplifier has a balance adjustment which is used to null the current feedback signal for a zero current condition. Amplifier 3-0A in conjunction with static relay 1CR generates a bidirectional drive current signal.

NOTE: On some systems where there are separate forward and reverse ac current transformers, both current signals -/I(D)F/ and -/I(D)R/, are applied to this buffer (Terminals 49 and 53) respectively. The zero current comparator, CMP2, which prevents bank reversal, is fed by the output of 2-0A.

NOTE: The zeroing of amplifier 2-0A is critical. The zero current comparator CMP2 changes state for current signal levels around 6 millivolts. If the RL Card ever has to be replaced, this balance adjustment should be checked.

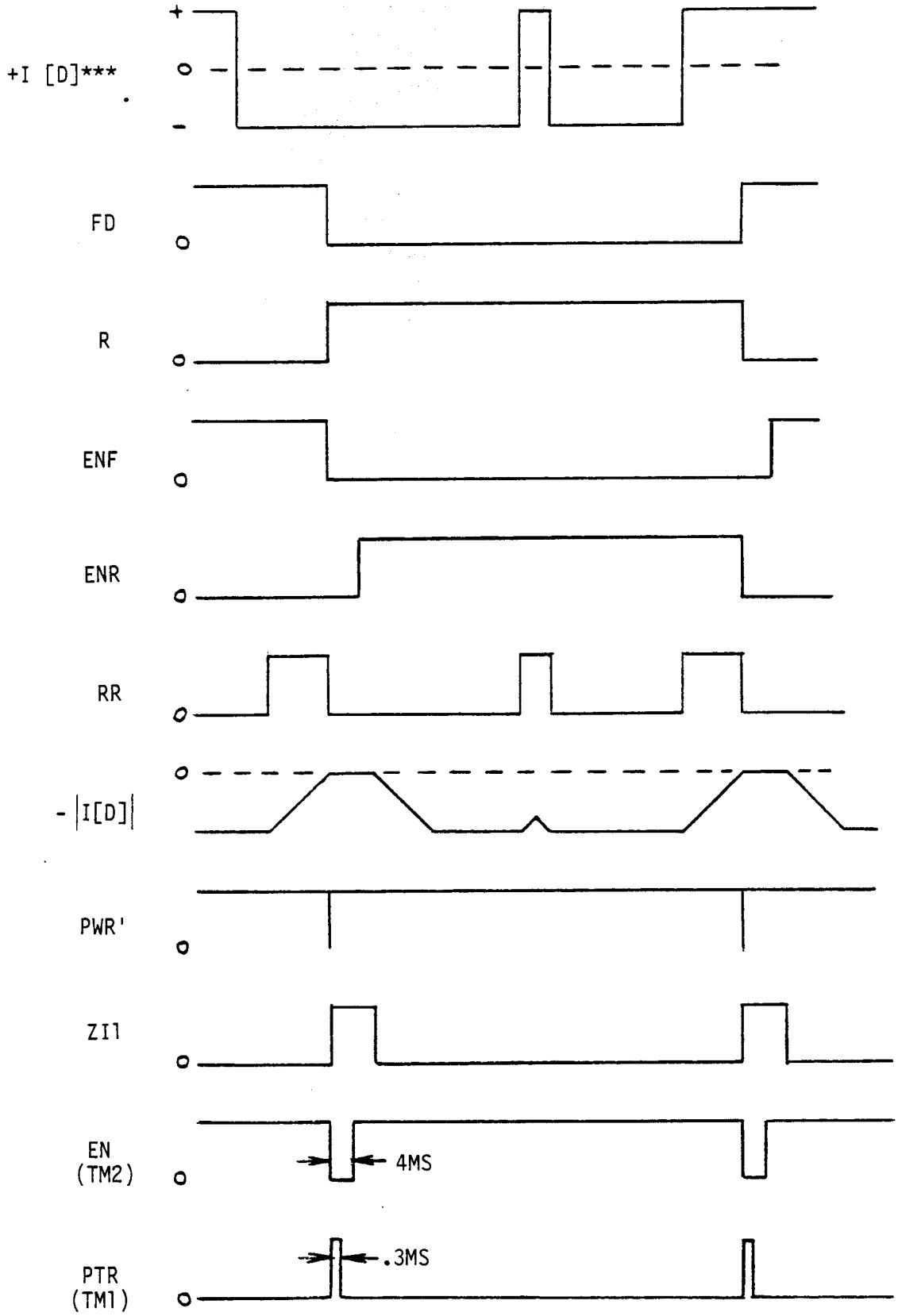
The RL Card is always used in the basic regulator even if only a single converter is used. The design of the Reversing Logic and Current Controller Cards is such that the absence of a reverse converter does not alter the circuit operation.

The reversing logic card establishes forward operation when the reference is positive and establishes reverse operation when the reference is negative. The comparator CMP1 switches very close to zero. In dual converter operation, the input reference normally reverses polarity to satisfy outer loop requirements. In single converter operation, the reference is generally limited so that a negative reference cannot be generated. In general this voltage would be limited close to zero. If the limit is such that the reference goes slightly negative then the basic regulator will proceed in the attempt to generate negative current even though none can be created. There are no windup or dead time problems created by this mode of operation.



BASIC REGULATOR - REVERSING LOGIC

FIGURE E1



BANK REVERSAL TIMING DIAGRAM

FIGURE E2

F. Current Controller

The current controller pc board simplified schematic is shown in Figure F1. The functions provided by this card are current reference rate limit, a PI type current controller and a minimization of dead time in association with a bank reversal in the gating system.

The reference input signal +I(D)** is applied through a current limit potentiometer (1P) to a three stage ramp function generation (RFG). 1P provides a current limit adjustment range from 0% (ECCW) to 300% (ECW): the latter corresponding to +10.0 volts. The three stage RFG generates a linear ramp with the output voltage level being dictated by the input voltage level (unity gain). The rate at which the current reference is applied to the current controller is dictated by the current rate potentiometer (5P). This pot adjusts the ramp rate from a level of 20 p.u./sec (ECCW) to 96 p.u./sec (ECW). 20 p.u./sec means that a current change from zero to rated current can occur in one twentieth of a second. The setting of this pot is dictated by the commutation capacity of the motor.

The current controller (5-0A) is the innermost regulating loop in the system. The controller is a PI type controller and the response of the current loop is adjusted to a maximum level with gain potentiometer 4P and gain jumper 1J. The current feedback signal (2V at rated current) is always positive and the current reference (10/3V at rated current) is appropriately controlled by static relay 3CR to maintain a unipolarity reference to the current controller amplifier.

Both the ramp function generator and the current controller have associated green LED's which indicate the status of the circuits. When LED 1CRDB is out, the RFG is reset; when LED 1CRDB is lit, the RFG is operational. When LED 2CR is out, the current controller is reset; when LED 2CR is lit, the current controller is operational. The RFG has a balance potentiometer which is used to zero one of the associated RFG output terminals for zero input. The current controller has a balance potentiometer which is used to cancel the offset errors associated with the current controller.

The speed of the current loop is determined by the gain potentiometer (4P) and the gain jumper (1J) but of equal importance is the minimization of time required when the converter switches from the Forward Mode to the Reverse Mode and vice versa. Bank reversal is controlled by the Reversing Logic board and certain actions take place on the current controller board during the reversal.

When the current reference signal +I(D)** changes polarity, a bank reversal is initiated. The reference, the ramp output and the current might be as shown in Figure F2. In general, the

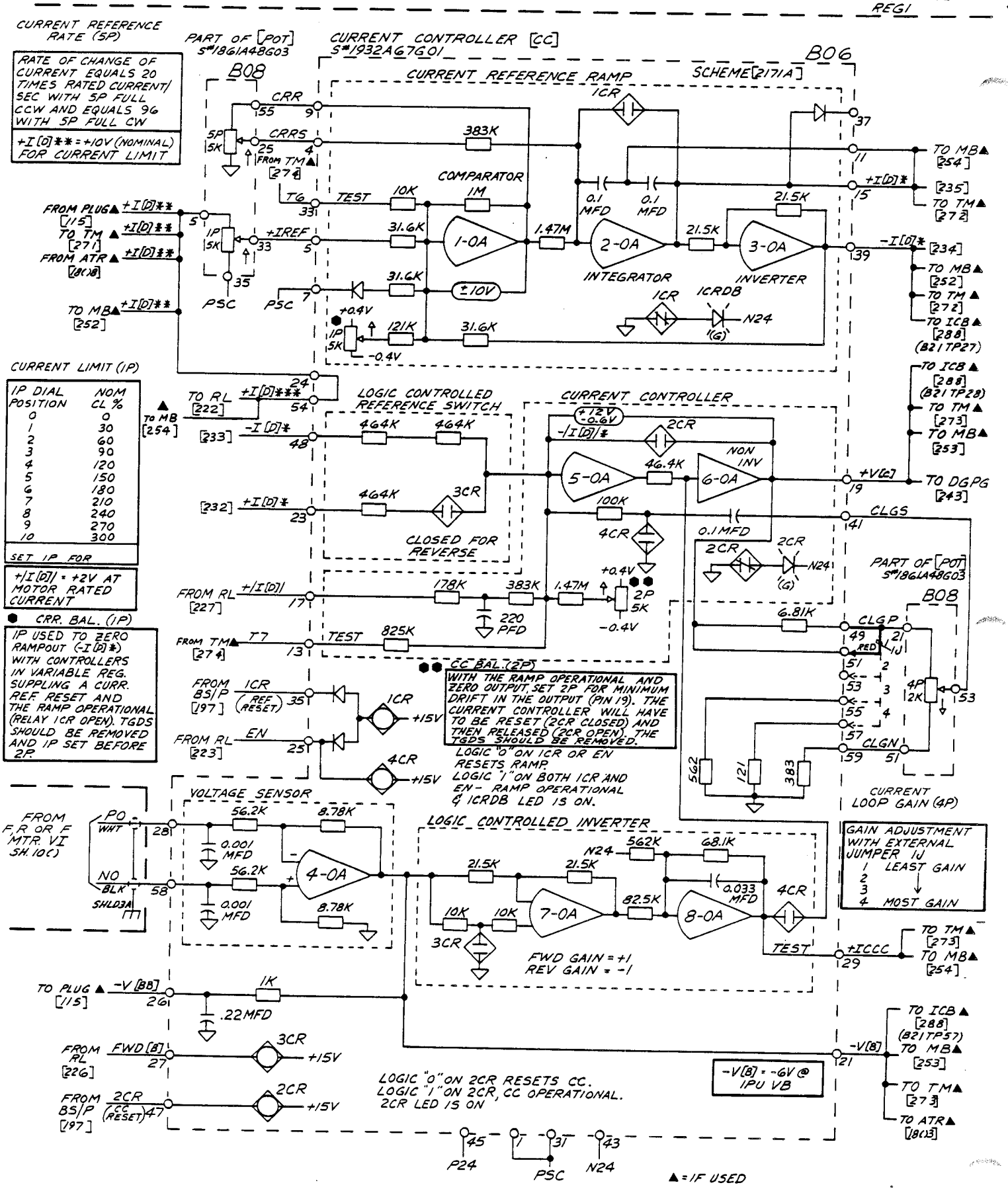
current should follow the reference ramp as the current controller is set for very fast operation. The ramp changes are quite fast as the reference can change from 0 to rated current in 50ms (20 p.u./sec) or as low as 10.4ms (96 p.u./sec). As the reference ramp goes to zero, the current follows. The reference changed polarity to initiate a bank reversal but the reversal is inhibited by the presence of current and no action can take place until the last current pulse goes to zero. Once the current zero is detected, bank reversal is allowed. Bank reversal takes place during a 4ms window during which the RFG is held reset (to prevent wind up) and during which the current controller is precharged to a gating angle which is a function of both direction and motor voltage. The function of the precharge on the current controller integrating capacitor is to minimize the slewing time of the current controller required in order to reach a gating angle where current is generated after a reversal takes place.

The reset of the RFG circuit is controlled by the signals which energize static relay 1CR. In this case the signals are 1CR from BS/P and EN from RL; the latter signal provides the 4ms reset window during the bank reversal.

The precharge of the CC integrating capacitor is initiated by the energization of static relay 4CR (by the EN logic signal). The external bus voltage signal is scaled and isolated by 4-0A. Amplifiers 7-0A and 8-0A precondition this signal which is used to generate the appropriate precharge. A fixed bias voltage is generated by 8-0A which provides an initial firing angle of 100° in the stall mode. The motor CEMF in conjunction with desired direction adds or subtracts from this bias in the generation of the precharge voltage. The directional information is supplied by static relay 3CR.

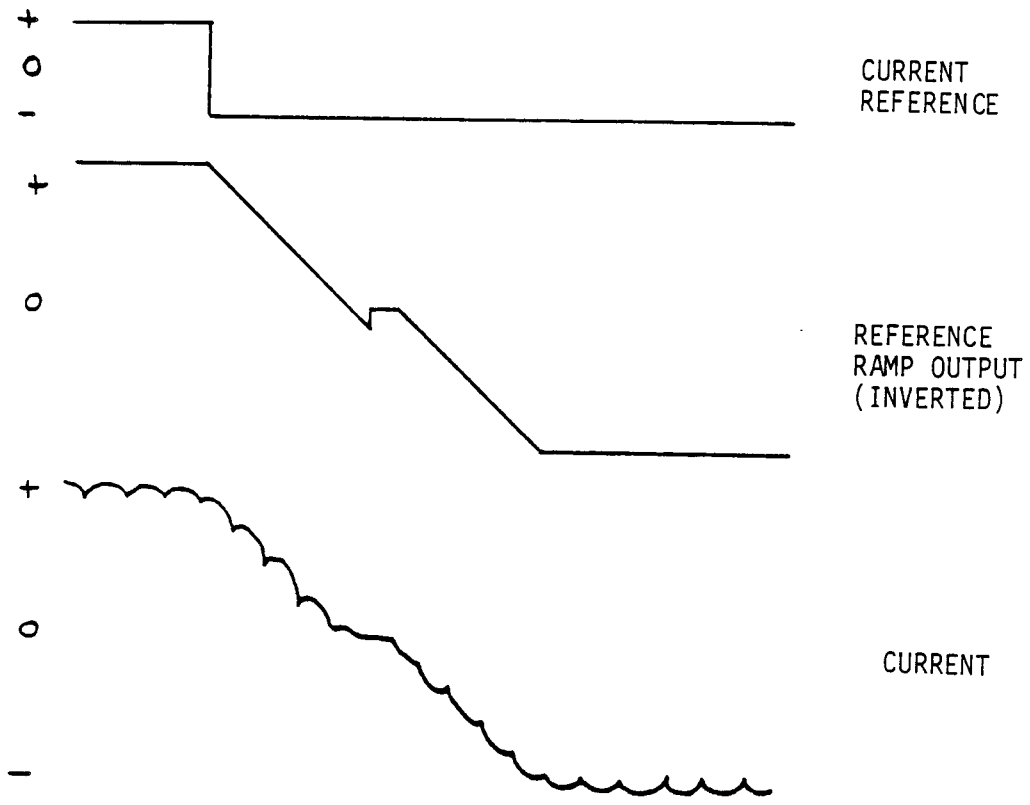
During the 4ms deadtime (EN = 0) static relay 4CR is energized. The output from 8-0A is applied to the non-inverting buffer 6-0A. One side of the integrating capacitor (0.1 MFD) is grounded and the output of 6-0A is applied to precharge the capacitor so that when the gate pulses are released at the end of the 4ms window, the gating angle is such that current (discontinuous) is produced.

The recordings of Figure F3 show current reversals with the RFG set at 20 p.u./sec and 96 p.u./sec. A recording of the current controller output shows the effect of the precharge. These recordings were taken at a stall condition with no motor field. The recording in Figure F4 shows the step response on the regulator after it has been properly adjusted for maximum response. This response time cannot be observed on a brush recorder as the pen response of the recorder is not fast enough. These recordings were taken on a digital oscilloscope the subsequently recorded at a slower speed.



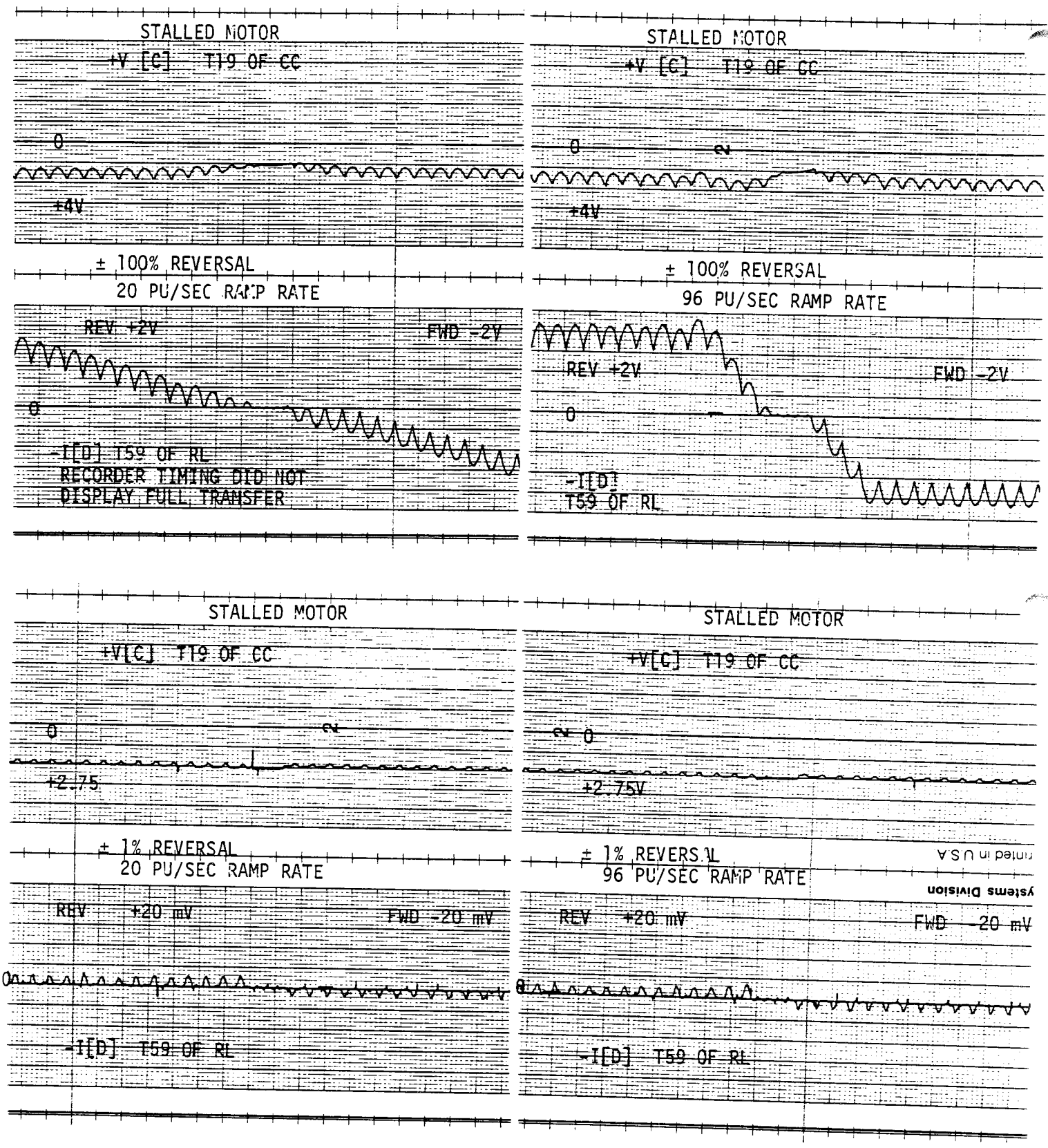
BASIC REGULATOR - CURRENT CONTROLLER

FIGURE F1



CURRENT REVERSAL DIAGRAM

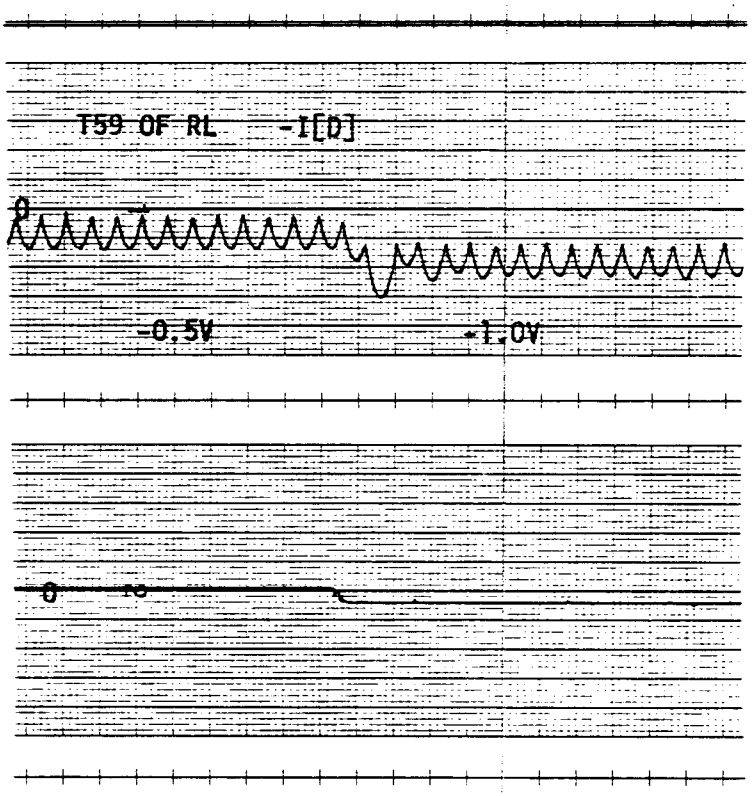
FIGURE F2



CURRENT REVERSAL RECORDINGS ±100%, ±1%
FIGURE F3

M5C
STEP INTO CURRENT LOOP
400A/50 MV SHUNT CHANGED
FROM 8 MV TO 16 MV

CORRESPONDING STEP
(-.74V) INTO T13 OF CC



CURRENT CONTROLLER STEP RESPONSE
FIGURE F4

G. Gating System

The gating system is shown in Figure G1. The basic components are a pulse generator (Digital Gate Pulse Generator) and a pulse amplifier (Thyristor Gate Driver). Two driver cards (TGD) are shown because they are used with a dual converter system to handle either the forward or the reverse operating mode of the converter. If the system contains only a single converter, the reverse driver card would be deleted.

The Thyristor Gate Driver card amplifies the logic signal pulses to power levels capable of driving either an externally mounted pulse transformer assembly, or an externally mounted gate pulse amplifier assembly which is used when the external power structure requires the paralleling of thyristors to develop the required load current. In either case, the pulse transformer provides isolation between the power circuitry of the thyristors and the electronics of the regulator.

A typical simplified thyristor pulsing circuit is shown in Figure G2. Capacitor 11C and resistors 13R and 14R are used to shape the envelope of the output pulse train so that the initial pulses in the pulse train supply more energy to the thyristor in order to insure rapid turn-on of the power device under high current conditions. Each pulse channel of the TGD card has an associated Light Emitting Diode (LED) which lights when pulses are being supplied to the external circuit. These LED's provide diagnostic information on the operation of the regulator. Generally, the LED's will be all on or all off together and when on they will all have the same relative intensity. The LED's provide a quick visual check on the status of the gating pulses. In a dual converter system at very light loads, both the Forward and Reverse TGD LED's may appear to be on at the same time. Due to switching between the forward and reverse converter banks, the LED's are turning on and off at a very rapid rate.

Two logic control lines are used on the TGD cards to inhibit pulse generating at the appropriate time. One line is associated with the operating mode of the regulator: forward or reverse. Notice in Figure G1 that one TGD card has the signal ENF while the other TGD has the signal ENR. The control has been designed such that these are non-overlapping mutually exclusive logic signals. The second control line is the INH' which is normally a logic one and goes to the zero state only when the regulator has detected an abnormal operating condition and shut the system down.

Figure G3 is a block diagram of the DGPG. The Digital Gate Pulse Generator (DGPG) uses a custom large scale integrated circuit (LSI) to produce gate signals for a thyristor power converter. The logic level gating signals (GP1 through GP6) are synchronized to a single phase sinewave input signal, and

their phase displacement is a linear function of an input analog control voltage Vin. The gating signals are composed of a train of picket fense pulses which begin with a 50 usec hard pulse. A Thyristor Gate Driver (TGD) card S# 1861A45G01 is used to amplify the gate signals to a level sufficient to gate a power thyristor.

Gate signals are generated and phase controlled by use of a digital multiplexing technique. The bulk of the digital circuitry is contained in the custom LSI circuit, therefore, the circuit description refers to functions contained inside as well as outside of the LSI chip (GPG 80). A counter (the Delay Counter) is phase locked to the synchronizing voltage by a Phase Locked Loop. From the Delay Counter an analog ramp is developed by which the phase delay information is generated. A second counter (the Gating State Counter) multiplexes the outputs of the Delay Counter to produce the six analog ramps necessary for control of the phase displacement of the individual gating signals. The Gating State Counter is also used to create the gating signal pulse trains and distribute them to the proper output terminals.

The input sine wave synchronizing signal defines the phase delay angle of the GP1 gating signal. For a conventional six-pulse bridge thyristor power circuit, GP1 gates thyristor THY1. Hence, the synchronizing signal is in phase with the commutation voltage for THY1, in this case the U-W voltage. The synchronizing signal is first filtered and phase shifted. Then the zero crossing detector converts it to a logic level square wave. The input filter causes the square wave to be delayed from the input sinewave by 75 degrees, consequently the effects of noise in the synchronizing signal are virtually eliminated.

The Phase Locked Loop (PLL) synchronizes the Delay Counter to the output of the zero crossing detector. As a result any given binary state of the Delay Counter has a fixed phase relationship to the synchronizing signal regardless of its frequency. Since the Delay Counter has 384 states for each cycle of the synchronizing signal, each count is equivalent to 0.9375 electrical degrees. The Delay Counter outputs are connected by a multiplexer to the Digital to Analog Converter (DAC) from which an analog representation of the delay angle is synthesized. The phase relationship between the delay angle information and the synchronizing signal can be shifted by the multiplexer, whose addresses are controlled by the Gating State Counter.

The DAC generates a current ramp output in response to the digital inputs. This signal is compared to the analog control voltage by a comparator whose output triggers a Monostable Multivibrator at the instant a new thyristor gating pulse is desired. The 50 uSec output pulse of the monostable is used as

the leading pulse of the gating pulse train as well as to clock the Gating State Counter. Clocking of the Gating State Counter is controlled by the Endstop circuit which restricts the gating angle of the DGPG to the proper operating range.

The picket fence gate signal is initiated by the 50 uSec "hard" pulse, and continued by the locally generated picket fense oscillator signal. The gate pulse train is terminated by either the initiation of the second subsequent gate signal, 120 degrees later, or by the tail end chop signal which prevents the pulse train from extending beyond a critical phase delay of 225 degrees.

The purpose of the 50uSec first pulse is to assure that the initial signal applied to the power thyristor gate is adequate to gate the device completely ON for any operating conditions. The picket fence oscillator signal which contributes the remainder of the pulse train maintains the ON state of the thyristor. The oscillator is not synchronized with the 50uSec pulse, thus its phase and frequency relationship to the 50uSec pulse is unpredictable. The tail end chop feature prevents gating of the power thyristor for an extended time while it is reversed biased.

The purpose of the Gate Pulse Suppression (GPS) logic signal is to permit the suppression of the output gating pulses in a rapid and orderly manner. This is accomplished by sensing the existance of either a hard pulse or a picket fence pulse and then GPS is permitted to become effective only during the time that no pulses exist. As a result any individual pulse which began prior to the activation of GPS will not be shortened but allowed to continue for its normal time. Any pulses beginning after the occurrence of GPS will be totally suppressed. This feature is especially important at the beginning of the thyristor's conduction interval as it assures that the device will receive a complete 50uSec hard pulse to turn it on under all operating conditions.

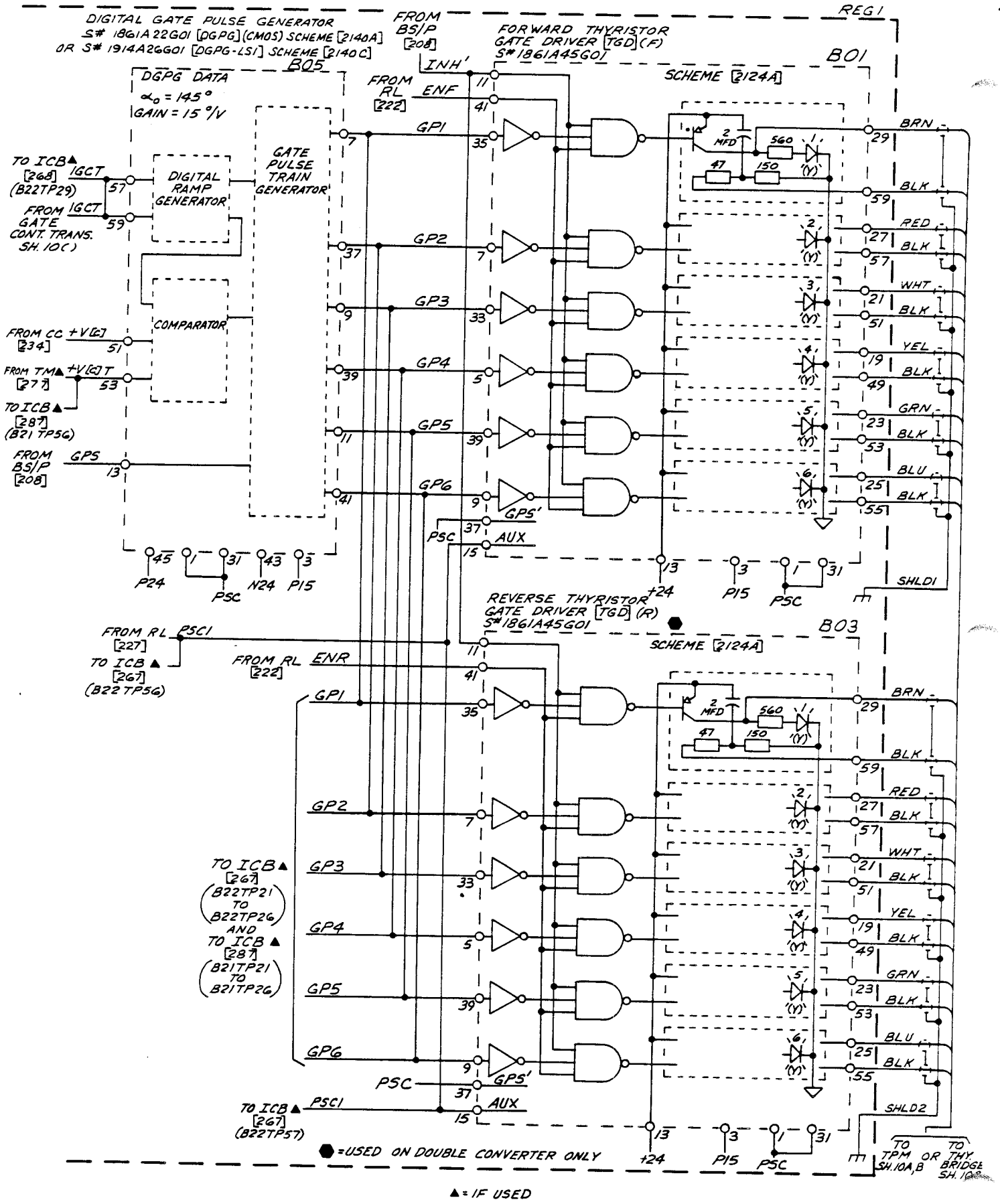
In order to utilize the digital gate pulse generator to properly gate a thyristor converter, an ac reference signal must be supplied which provides the basic system timing. In Figure G4a the synchronizing transformer is used to provide this signal. Note that the primary of the sync. transformer and the secondary of the power transformer have the same phase relationship. The secondary signal 1GCT (in phase with the U-W ac line voltage) is the sync. signal required for the correct phasing of the firing of thyristor THY1.

Figure G4b depicts a 12 pulse converter which is operated by two separate gating systems with a common synchronizing transformer. Note that the two power transformer secondaries have a phase displacement of 30°. This is done so that the commutation of the second six pulse thyristor set occurs half

way between the commutations of the first six pulse set. The bottom set of thyristors is controlled by a DGPG which is time coordinated by the synchronizing signal 1GCT. The firing of thyristor THY1 is coordinated to the 1U-1W waveform. The second six pulse converter has its own DGPG which is time coordinated by the synchronizing signals 1GCT and 2GCT (vectorially added). The net resultant timing signal is delayed 30° from the 1GCT signal and THY1 in the second set is coordinated to the 2U-2W waveform.

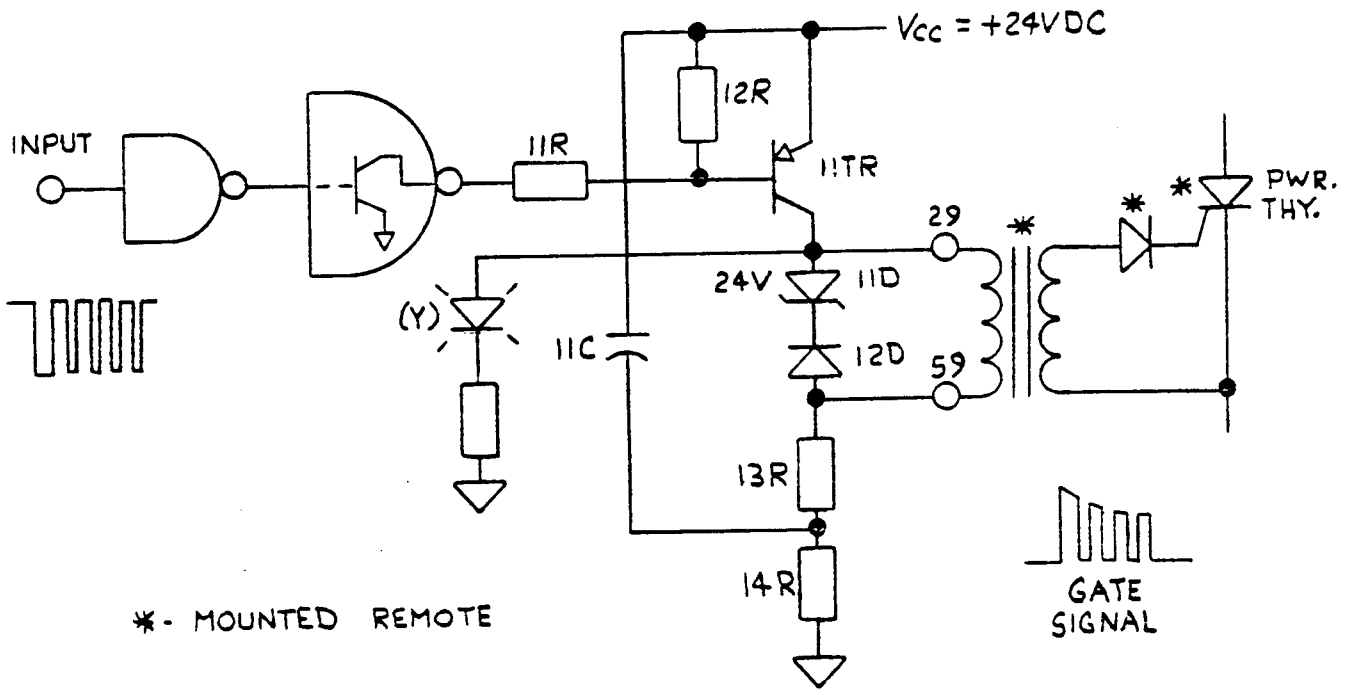
The above synchronization discussion is predicated on the connection of the synchronizing transformer to the secondary winding of the correct power transformer.

The two or in some cases three printed circuit cards which comprise the gating system first generate and then amplify (voltage and current) six sixty degree displaced pulse train signals. The pulse trains are normally 120° in duration unless the gating angle is such that tail end chop (elimination of gating pulses past = 225°) reduces the width of the pulse train.



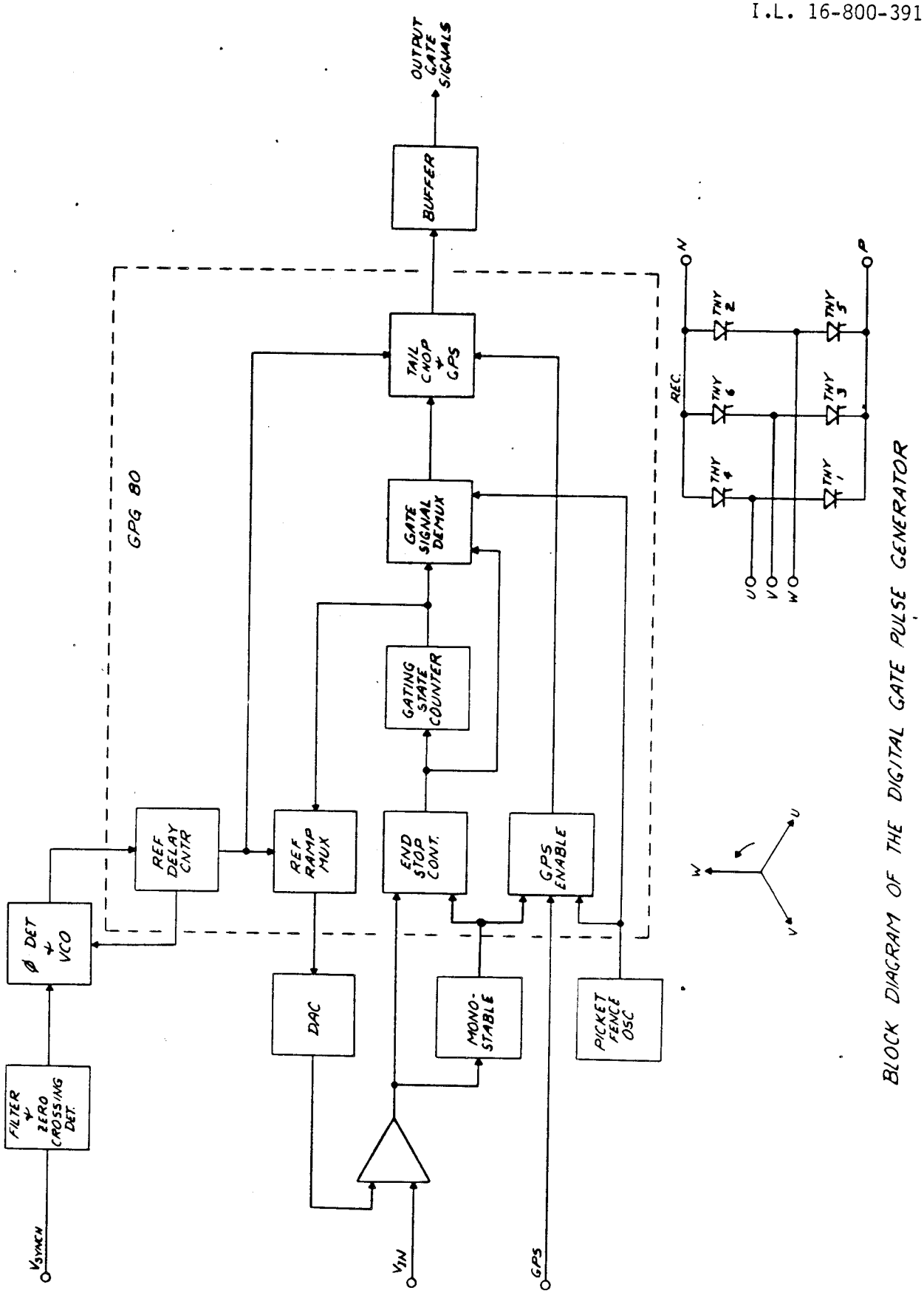
BASIC REGULATOR - GATING SYSTEM

FIGURE C1



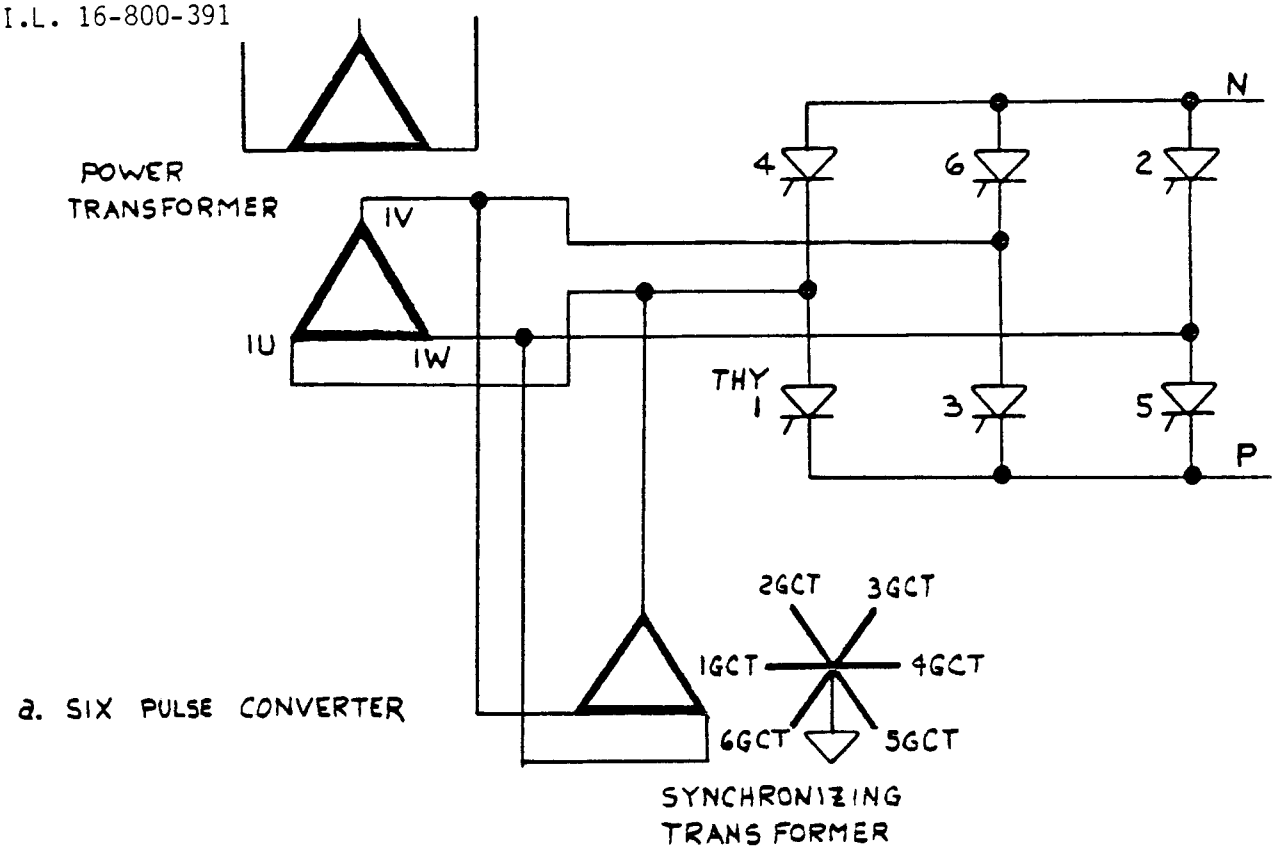
TYPICAL TGD PULSING CIRCUIT

FIGURE G2

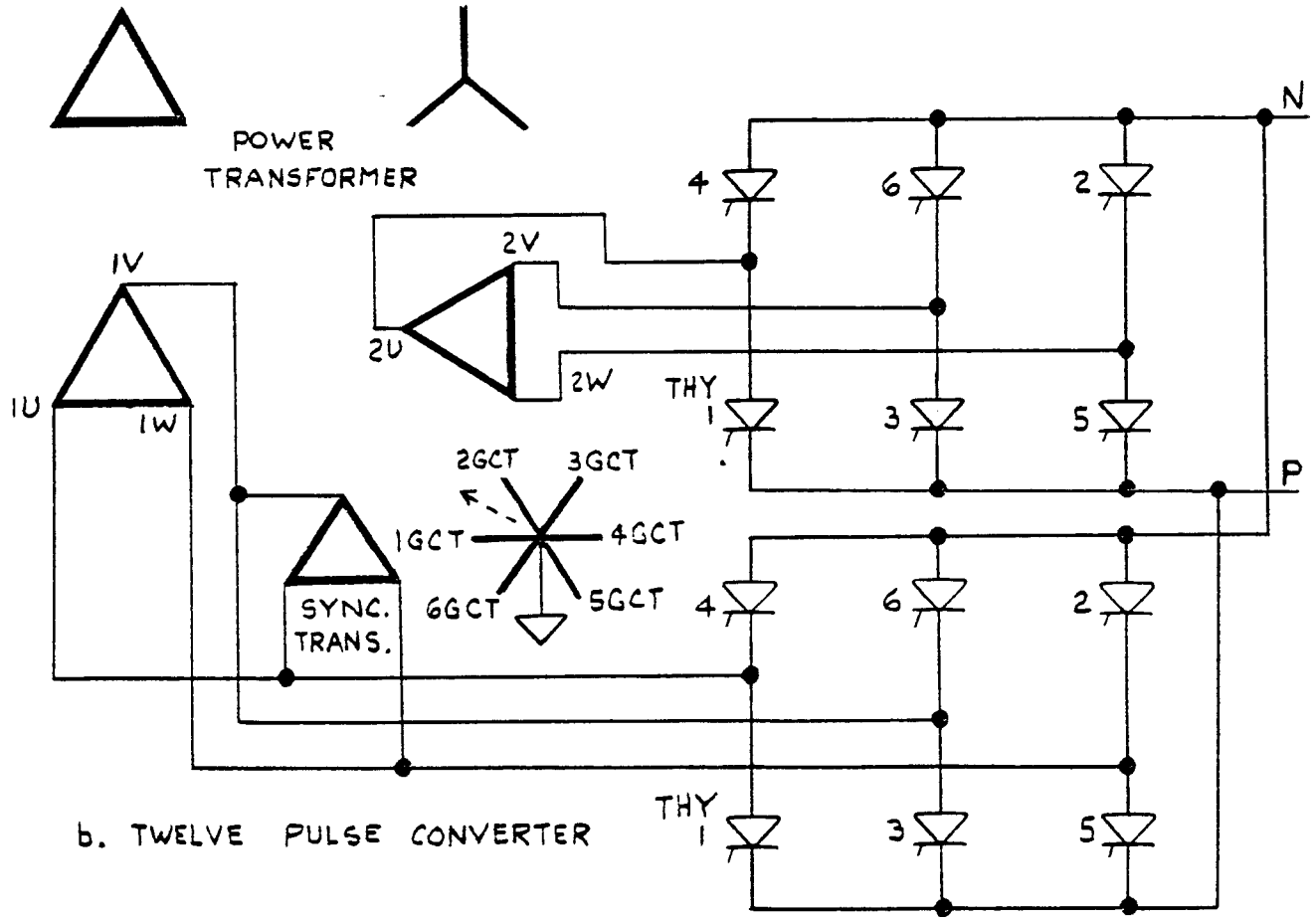


DGPG BLOCK DIAGRAM

FIGURE G3



a. SIX PULSE CONVERTER



b. TWELVE PULSE CONVERTER

GATING SYNCHRONIZATION

FIGURE G4

H. Power Supply

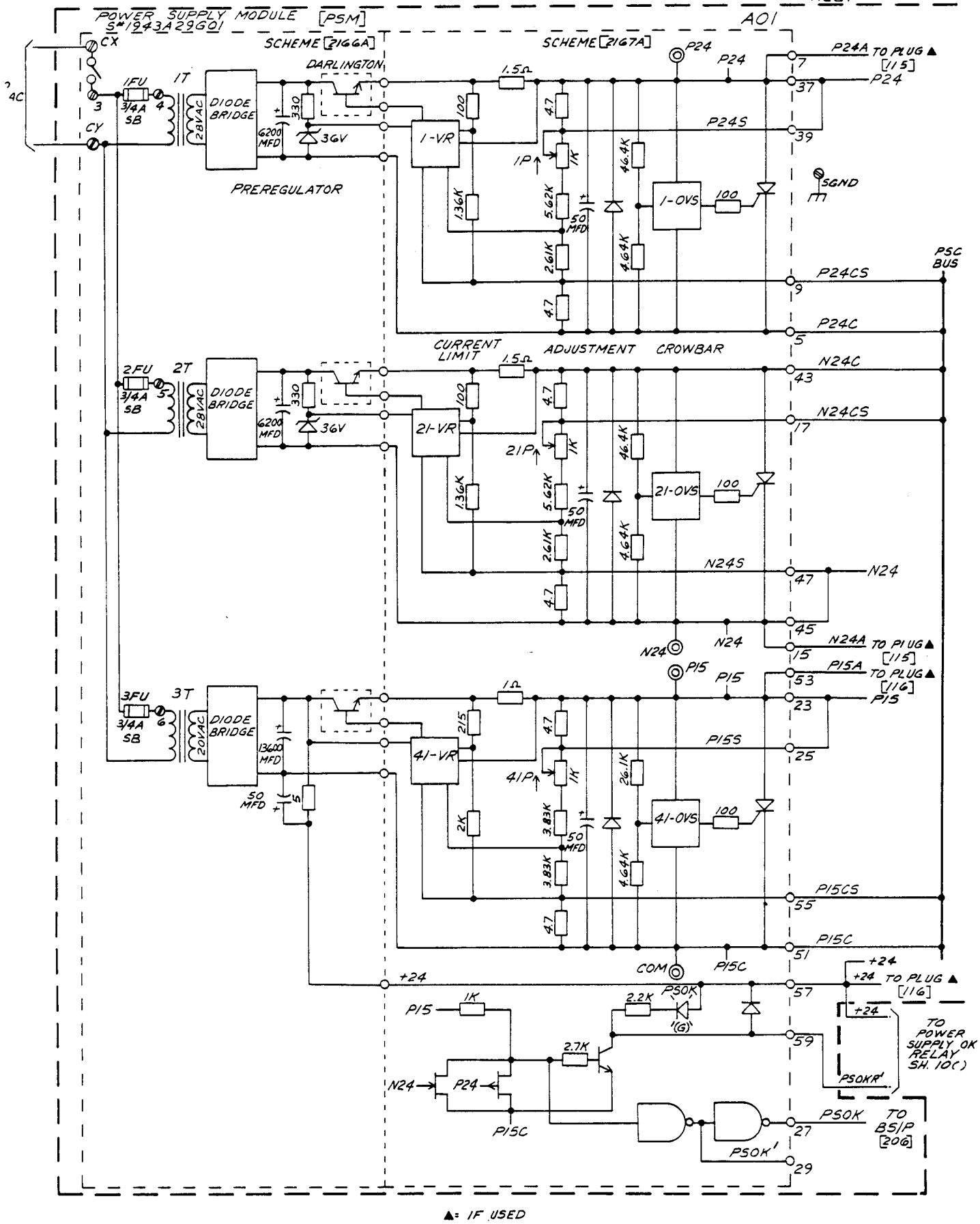
A simplified schematic of the Power Supply Module is shown in Figure H1. Inputs requirements are 115 volts ac ±5% 50/60 HZ 180 VA. The output voltages are as follows:

+24 Volts (P24) regulated at 1.5A (nominal)
-24 Volts (N24) regulated at 1.5A (nominal)
+15 Volts (P15) regulated
+24 Volts (+24) unregulated } at 2A (nominal)

The current on the P15 output plus the current on the +24 output cannot exceed 2A.

The three regulated supplies are almost identical. Each supply has an adjustment potentiometer for setting the output voltage, an overvoltage protection circuit which shorts the output in the event an overvoltage is detected and foldback current protection to prevent thermal overload of the series pass darlington in the event the load is excessive or shorted.

The input transformers are protected by 3/4A slow blow fuses. Loss of any of the input fuses or a shorted output will cause the external relay PSOK to de-energize. Contacts of this relay are used in the drive sequencing. When the power supply outputs are operational, a green LED is on to so indicate. The LED indicates that an input fuse is not blown and that some voltage exists on the output. The LED will be on even if the output voltage is outside of the normal expected tolerance range.



BASIC REGULATOR - POWER SUPPLY

FIGURE H1

I. Printed Circuit Board Power Supply Requirements

The basic boards used in the regulator cage have the following power requirements listed in milliamps.

NAME	P24	N24	P15	+24	S#
TGD (F)	-	-	30	125	1861A45G01
DGPG	35	25	30	-	1914A26G01
CC	55	80	-	-	1932A67G01
RL	30	30	95	-	1932A68G01
POT	-	-	-	-	1861A48G03
BS/P	25	25	100	12	1932A69G01
ATR	120	120			1883A97G01
ORB	-	-	130	-	1640A44G02
IB	-	-	100	-	1640A29G03

The power supply for the basic cards are as follows:

P24	N24	P15	+24	
265	280	485	137	6 Pulse SC
265	280	515	137	6 Pulse DC (2 TDG Cards)

Each optional card used in the regulator has its own power requirements and the total drain on the supply and the remaining capacity will have to be determined for each job.

The following list indicates the power requirements for each optional card that could be used in the system (in ma).

NAME	P24	N24	P15	+24	S#
FF	-	-	20	-	1932A75G01
ICB	-	-	-	-	1640A22G01
IB	-	-	100	-	1640A29G03
TM	100	70	10	-	1943A23G01
DTR	-	-	115	-	1883A98G01
MB	-	-	-	-	1640A28G01
DIFFC	80	80	50	-	1883A96G01

For a particular job, the excess capacity available in the power supply can be used to operate a local variable regulator. The power supply voltages are prewired in the cable harness that interconnects the regulators so that the variable regulator can be powered from the power supply in the basic regulator assuming the supply capacity is not exceeded.

J. Interface Areas

In the use of the basic regulator, external connections must be made to the regulator. The areas of connections involve front connected printed circuit cards, interconnection plugs and 115 VAC for the power supply module.

Front connected cards provide isolation between the regulator and the external world. Isolation from 115 Vac is provided by Input Cards and Output Relay Cards as has already been shown in Figures C1 and C2; and the associated cables must be terminated correctly with appropriate signal sequencing as required in the system. Any additional option boards of a similar nature must be terminated and sequenced correctly.

Optional front connected cards are used for interfacing with a remotely mounted variable regulator. These cards are the Digital and Analog Transmitter/Receiver Cards which are used to optimize the required interface function. 115 vac must be brought into the Power Supply Module at the correct terminal block points (CX and CY) to provide operating power.

The remaining connections are made to plugs on the backplane. The associated cables connect the basic regulator to the TPM assembly, the Variable Regulator assembly (if local), and to the Regulator Cabinet. The signals carried on these cables are shown in Figure J1 through J4. The cables used depend upon the TPM selected. All signals to the TPM and the Regulator Cabinet (except DCBKRT) are required in the basic system and must be properly interfaced. All of the signals transmitted between the Basic and Variable Regulator are not required to operate the basic system. A particular system must use or generate the appropriate signals as required for that system.

Figures J1 through J4 show the signals terminated on the back plane plugs.

	FROM F.R BASIC REG		TO TPM		
	PLUG POSITION		PLUG POSITION		
SIGNAL NAME	HOI	PIN	HOI	PIN	SH. NO.
BRN		01		01	24
BLK		02		02	
RED		03		03	
BLK		04		04	
WHT		05		05	
BLK		06		06	
YEL		07		07	
BLK		08		08	
GRN		09		09	
BLK		10		10	
BLU		11		11	
BLK		12		12	
RED		13		13	
BLK		14		14	
BRN		15		15	
BLK		16		16	
YEL		17		17	
BLK		18		18	
WHT		19		19	
BLK		20		20	
BLU		21		21	
BLK		22		22	
GRN		23		23	
BLK		24		24	↓
MV2		25		25	19
MVI		26		26	↓
SHLD3+3A		27		27	19 23
SHLDI		28		28	24
NO		29		29	23
PO		30		30	↓
SHLD4		31		31	20
SHLD2		32		32	24
-/I [D]/		33		33	20
PSC4		34		34	↓
		35		35	
	↓	36	↓	36	

SINGLE CONVERTER

CABLE S#1752A08G06 - SIZE 2 OR 3

DOUBLE CONVERTER

CABLE S#1752A08G04 - SIZE 2 OR 3

	FROM F.R BASIC REG	TO REG CAB		
	PLUG POSITION	TERM. BLK. POSITION		
SIGNAL NAME	HO7	PIN	HO7TB	01	SH. NO.
-I[DC]F		01		01	NOT USED
PSC5		02		02	
DCBKRT		03		03	
PSC6		04		04	↓
IGCT		05		05	20
3GCT		06		06	
5GCT		07		07	
PSC7		08		08	↓
MV2		09		09	19
MVI		10		10	↓
+24		11		11	12
PSOKR'	↓	12	↓	12	↓

CABLE S#1905A67G10

● = USED ON DOUBLE CONVERTER ONLY.

BASIC REGULATOR - PLUG SIGNAL DISTRIBUTION
M5C - SIZE 2 OR 3 TPM

FIGURE J1

	FROM F.R BASIC REG		TO TPM		
	PLUG POSITION		PLUG POSITION		
SIGNAL NAME	H01	PIN	F	PIN	SH. NO.
BRN		01		06	24
BLK		02		09	
RED		03		14	
BLK		04		13	
WHT		05		01	
BLK		06		04	
YEL		07		12	
BLK		08		15	
GRN		09		02	
BLK		10		03	
BLU		11		07	
BLK		12		10	
RED		13	R	03	
BLK		14		02	
BRN		15		07	
BLK		16		10	
YEL		17		01	
BLK		18		04	
WHT		19		12	
BLK		20		15	
BLU		21		06	
BLK		22		09	
GRN		23		13	
BLK		24		14	
MV2		25	C	12	19
MVI		26		09	
SHLD3+3A		27		08	19 23
SHLDI		28			24
NO		29		11	23
PO		30		10	
SHLD4		31		07	20
SHLD2		32			24
-/I [D]/		33		05	20
PSC4		34		04	
		35			
		36			

SINGLE CONVERTER

CABLE S#1965A62G01 - SIZE 1

DOUBLE CONVERTER

CABLE S#1965A62G02 - SIZE 1

	FROM F.R BASIC REG		TO REG CAB		
	PLUG POSITION		TERM. BLK. POSITION		
SIGNAL NAME	H07	PIN	H07TB	01	SH. NO.
-I[DC]F		01		01	NOT USED
PSC5		02		02	
DCBKRT		03		03	
PSC6		04		04	
IGCT		05		05	20
3GCT		06		06	
5GCT		07		07	
PSC7		08		08	
MV2		09		09	19
MVI		10		10	
+24		11		11	12
PSOKR'		12		12	

CABLE S#1905AG7G10

● = USED ON DOUBLE CONVERTER ONLY.

BASIC REGULATOR - PLUG SIGNAL DISTRIBUTION
M5C - SIZE 1 TPM

FIGURE J2

	FROM F,R BASIC REG		TO THY. BRIDGE (REG CAB)		
	PLUG POSITION		TERM. BLK. POSITION		
SIGNAL NAME	H01	PIN			SH. NO.
BRN		01	FTB	01	24
BLK		02		02	
SHLD1		28		03	
RED		03		04	
BLK		04		05	
SHLD1		28		03	
WHT		05		06	
BLK		06		07	
SHLD1		28		08	
YEL		07		09	
BLK		08		10	
SHLD1		28		08	
GRN		09		11	
BLK		10		12	
SHLD1		28		13	
BLU		11		14	
BLK		12		15	
SHLD1		28	↓	13	
RED		13	RTB	04	
BLK		14		05	
SHLD2		32		03	
BRN		15		01	
BLK		16		02	
SHLD2		32		03	
YEL		17		09	
BLK		18		10	
● SHLD2		32		08	
WHT		19		06	
BLK		20		07	
SHLD2		32		08	
BLU		21		14	
BLK		22		15	
SHLD2		32		13	
GRN		23		11	
BLK		24		12	
SHLD2	↓	32	↓	13	↓

	FROM F,R BASIC REG		TO REG CAB		
	PLUG POSITION		TERM. BLK. POSITION		
SIGNAL NAME	H07	PIN			SH. NO.
-I[DC]F		01	IHGTTB	01	29
PSC5		02		02	↓
DCBKRT		03		03	20
PSC6		04		04	↓
IGCT		05		05	20
3GCT		06		06	
5GCT		07		07	
PSC7		08		08	↓
MV2		09		09	19
MV1		10		10	↓
+24		11		11	12
PSOKR'	↓	12	↓	12	↓

CABLE S#1905A67G10

MV2	H01	25	CTB	01	19
MV1		26		02	↓
SHLD3		27		03	↓
SHLD3A		27		06	23
NO		29		04	
PO		30		05	↓
SHLD4		31		09	20
-|I[D]|		33		07	
PSC4		34	↓	08	↓
		35			
	↓	36			

SINGLE CONVERTER
CABLE S#1946A59G01

DOUBLE CONVERTER
CABLE S#1946A59G02

●=USED ON DOUBLE CONVERTER ONLY.

BASIC REGULATOR - PLUG SIGNAL DISTRIBUTION
M4CL

FIGURE J3

	FROM F.R BASIC REG		TO VAR REG		
	PLUG POSITION		PLUG POSITION		
SIGNAL NAME	H05	PIN	H05	PIN	SH. NO.
M		01		01	13
ZAPV		02		02	19
ZBPV		03		03	
ONCV'		04		04	
+N[C]		05		05	18
CCC'		06		06	19
ZIR'		07		07	
PSR		08		08	
VRL		09		09	
ICRV		10		10	
2CR		11		11	
RESET'		12		12	
GPS		13		13	20
ITOL		14		14	
-I[D]		15		15	22
+I[D]**		16		16	23
-V[BB]		17		17	
P24A		18		18	12
P24A		19		19	
N24A		20		20	
N24A		21		21	
P15A		22		22	
P15A		23		23	
+24		24		24	
		25		25	
		26		26	
		27		27	
		28		28	
		29		29	
		30		30	
		31		31	
		32		32	
		33		33	
		34		34	
		35		35	
		36		36	

CABLE S#1946A08G04

	FROM F.R BASIC REG		TO VAR REG		
	PLUG POSITION		PLUG POSITION		
SIGNAL NAME	H03	PIN	H03	PIN	SH. NO.
VTM1		01		01	27
VTM2		02		02	
VTM3		03		03	
VTM4		04		04	
VTM5		05		05	
VTM6		06		06	
VTM7		07		07	
VTM8		08		08	
VTM9		09		09	
VTM10		10		10	
VTM11		11		11	
VTM12		12		12	
VTM13		13		13	
VTM14		14		14	
VTI1-1		15		15	
VTI1-2		16		16	
VTI1-3		17		17	
VTI1-4		18		18	
VTI2-1		19		19	
VTI2-2		20		20	
VTI2-3		21		21	
VTI2-4		22		22	
		23		23	
		24		24	
		25		25	
		26		26	
		27		27	
		28		28	
		29		29	
		30		30	
		31		31	
		32		32	
		33		33	
		34		34	
		35		35	
		36		36	

CABLE S#1946A08G04

H05 AND H03 PLUGS USED FOR LOCAL VAR. REG. ONLY

BASIC REGULATOR - PLUG SIGNAL DISTRIBUTION
FOR LOCAL VARIABLE REGULATOR

FIGURE J4

K. Available Cage Options

K1. Interfacing Variable to Basic

In a drive system, communication is required between the variable regulator and the basic regulator. Two mechanical arrangements are used which require different interconnection approaches.

When the variable regulator is located in the same cabinet as the basic regulator, communication between the two electronic assemblies is direct by pre-wired cable harness (see Figure J4).

When the variable regulator is physically separated in a different cabinet, additional hardware is required in order to minimize the possibility of noise pickup associated with the added wiring. Also, the potential for ground differences between the two cabinets raises the possibility of generating common mode errors if signal transmission is not correct.

In order to minimize the effects of noise sources, interface buffers are used to communicate between the two regulators. A digital transmitter-receiver (DTR) card as shown in Figures K1-1 and K1-2 is used to provide logic communication between the two cages. An analog transmitter-receiver (ATR) card as shown in Figure K1-3 is used to provide analog communication between the two cages. The DTR and the ATR cards are intended to be located in cage positions A19 and A18 of the basic regulator respectively. In the variable regulator there must be corresponding DTR and ATR cards. The DTR card is pre-wired to interface the following signals.

Basic to Variable

GPS	= 1 Drive in Gate Pulse Suppression
2CR	Current Controller reset when 2CR = 0.
ITOL	= 1 For an Inverse Time Overload - Momentary
VRL	Voltage Ready Low VRL = 1 when motor voltage is < 10%.
1CRV	Current Controller Reference reset when 1CRV = 0
M	M = 1 with main contactor closed.

Variable to Basic

ZAPV = 1 Zone A Permissive from the variable is satisfied.
ZBPV = 1 Zone B Permissive from the variable is satisfied.
ZIR' = 0 Resets current reference ramp.
CCC' = 0 Resets current controller and current reference ramp with the contactor closed if the VRL functions are satisfied.
ONCV' = 0 momentary. Command to close contactor from variable regulator.
(SPARE)

These signals have been allocated for communication between the two regulators for use in a variety of systems. In a particular system certain signals may not be used and it will be necessary that the signal origin be terminated correctly. This is especially the case for the digital signals transmitted by the variable regulator. For example, if the Zone A and B functions from the variable regulator are not used then the appropriate lines in the variable regulator must be tied to the logic power supply voltage so that ZAPV and ZBPV are both ones in the basic regulator. Any of the logic signals in Figure K1-2 not used by the variable regulator must be appropriately tied to either the logic power supply or logic common in the variable regulator. In the variable regulator ZAPV, ZBPV, ZIR' and CCC' should be tied to the logic power supply if not used and ONCV' should be tied to PSC if not used.

Logic communication between the external sequencing and the basic regulator and between the basic and variable regulators involves wire anding logic elements. Wire anding means that two logic chip outputs are tied together and both input conditions must be satisfied in order for the common output to be in the one state.

The transmitted analog signals are shown in Figure K1-3. These include the current reference signal from the variable regulator and the transduced armature voltage and current signals to the variable regulator.

K2. Fault Finder

The basic regulator when operational can be turned off in a gate pulse suppression mode for a variety of reasons. These are as follows:

Overcurrent
Undervoltage or Single Phase
Phase Sequence
Loss of Power Supply Voltage
Contactor Failure
Differential Current Error
AC Breaker Trip

Gate pulse suppression (via INH or an Inverse Time Overload) will cause the contactor and the power supply ready relay to drop out.

Most of these signals are momentary only and if the drive shuts down there is no indication of what caused the shut down. An option that is available for indication purpose is the fault finder shown in Figure K2-1. As shown in this figure, there are eight LED's with the identification as marked. These indicators are electrically connected so that only the first fault which occurs is indicated. When this option is used, information is immediately available on this card as to what caused the fault. This card is intended for position B11 of the Basic Regulator.

K3. Meter Board - Analog

If analog meters are required in the regulator cage, then the Meter Board S# 1640A28G01 as shown in Figure K3-1 can be inserted into position A15 of the Basic Regulator. The signals monitored are as shown and any two can be displayed at any time. The analog meters are $\pm$15 volt meters with 1 volt increment marks. Two rotary deck switches are used for signal selection.

K4. Interconnect Board

The Interconnect Board S# 1640A22G01 is intended to provide front accessibility to various signal lines in the Basic Regulator. The points monitored are as shown on Figure K4-1 and these points have been selected to minimize the necessity of connecting instruments to the backplane. These points could be used in startup or troubleshooting. This card is intended for position B22 in the regulator cage.

A second Interconnect Board can be used in position B21 if the Test Module is not used. The points wired to this position are shown in Figure K4-2.

K5. Input Board

An optional Input Board which is the same style number board as is used in position A22 has been engineered into position A21. This board would be used if the system was designed for forcing zero current with the contactor closed or if an indication of an ac breaker trip signal was required. Refer to Figure K5-1.

K6. Test Module

The Test Module is shown in Figure K6-1 and is intended to be plugged into position B15 of the regulator cage. The module occupies seven cage positions and a front view of the assembly is shown in Figure B2.

The Test Module provides as follows:

1. a 3 1/2 digit LCD (liquid crystal display) digital voltmeter with selectable ranges of 0 to 2V or 0 to 20V. Input resistance is greater than 5M ohm in the 2 volt range and is 1M ohm in the 20 volt range. Any overrange on the meter causes the three least significant digits to blank out. For polarity, only the minus sign is indicated. The range select switch is marked 1.999 - 19.99.

   The DVM monitors any of the regulator signals that are shown connected to rotary deck switch 3RS provided that the rotary deck switch and the three associated toggle switches are correctly positioned. The DVM can monitor external signals if the INT/EXT toggle switch is appropriately set and the input signal is applied to the EXT banana jack.

   Although only capable of reading up to 19.99 volts, the regulator supplies P24, N24 and P15 are monitored by rotary deck switch 3RS - Deck 3. Positions 8 and 10 monitor P24 and N24 respectively with scaled readings of $\pm$12.00 volts. The P15 supply is monitored in position 12 and is directly indicated as 15.00.

2. Six unity gain non-inverting buffers are provided for instrumenting internal regulator signals while the drive is operational. The buffered signals are available at banana jack points one through six on the front of the module. The buffers can be programmed to monitor any of the 28 signals monitored by the input terminals of rotary deck switch 3RS. To change buffer monitoring, the Test Module must be removed from the cage and the associated six jumpers from the piggyback board can be connected to any of the twenty-eight pins which are near the connector

fingers. The appropriate pins are marked with the external terminal number. Use of these buffers prevents instrumentation or lead loading from affecting the signal being monitored. It also prevents the inputting of noise into the regulator which may be occurring because the leads used to monitor signals although primarly used for applying a signal to an instrument can also couple noise from an external noise generator back into the regulator. The buffers will prevent this reverse feed effect.

3. Three toggle switches numbered 1, 2 and 3 are used for logic input signals and are wired to open and close the contactor and reset the drive. The external sequence switches may not be convenient when the drive is initially being checked during startup. The ability to have this control at the regulator will assist startup if this module is used.

4. There are two independent test voltages available from the module. The two test signals are controlled by the hardware within the box designated TS1 and within the box designated TS2. Refer also to Figure B2. The two test signals have the same control and adjustment procedure except that the TS1 test signal can be operated in a pulse mode. Refer to the TS2 section of the schematic of Figure K6-1. The SIG ON/OFF switch grounds or outputs the signal from the BASE pot. The BASE pot with the STEP switch in the OFF position can adjust the output signal for 0 to 24 volts. Polarity of the output depends upon the polarity (POL) switch. With the STEP switch in the ON position, the output signal is reduced as the STEP pot is rotated clockwise. When using this step function which is actually a reduction in output voltage, the signal may have to be precalibrated before use in a particular circuit so that the correct levels are generated. If the actual circuit requires a step increase in voltage then after initial calibration, the STEP switch can be put in the OFF position to generate the required signal increase. With two test signals available, one circuit can generate a level and the other circuit can generate the step. This necessitates having two input terminals free for test purposes on the circuit being tested. The TS1 and TS2 circuits can produce the type of output voltage level just discussed.

   The TS1 circuit is also capable of automatically producing a pulsed output. With the SIG switch OFF and the BASE pot at some voltage then throwing the PULSE switch to the ON position will generate the output voltage pulse which goes from zero to the level of the base pot and then back to zero. The output level and polarity are determined by what is on the base pot wiper. The zero level is not quite zero due to the finite on resistance of static relay

1CR. Only one pulse is produced. To repeat the pulse, the PULSE switch must be put to OFF and then back to ON. Alternating polarity pulses can be generated after the PULSE switch is in the ON position by changing the position of the POL (polarity) switch. Each time this switch is repositioned, an opposite polarity output pulse is generated. In the pulsing mode the use of amplifier 2-0A restricts the output pulse amplitude to approximately ±12 volts.

In the basic regulator the test output voltages are wired to various points for startup assistance. 1RS and 2RS must be appropriately positioned to inject a test signal as required. Positions 1 of both 1RS and 2RS are dead points and the two rotary deck switches should be returned to these points to prevent inadvertent signal injection after testing has been completed.

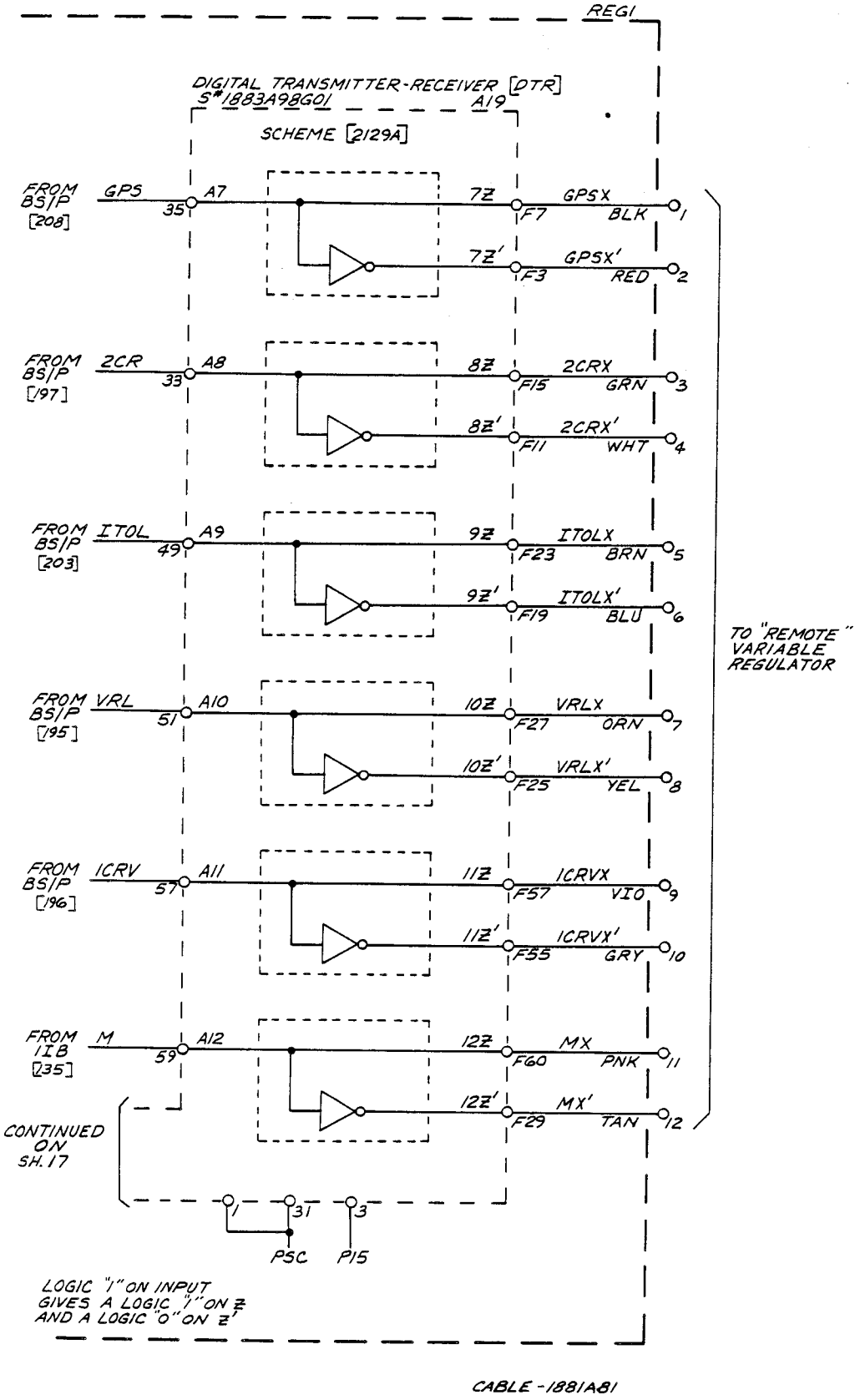
The output signals from TS1 to TS2 can be monitored at the appropriate banana jacks 1 and 2 and the EXT banana jack associated with the DVM makes it quite convenient to check these levels. The amplitude of the pulse output from TS1 can also be checked by monitoring the steady state level of the base pot.

The banana jacks on the Test Module take 0.080 inch test pins. If necessary the DVM reading can be checked by comparing it to the voltage level on the INT banana jack. The output from 1-0A is always scaled for a 0 to 2 volt level so that there might be a decimal point error in making a comparison.

K7. Differential Current

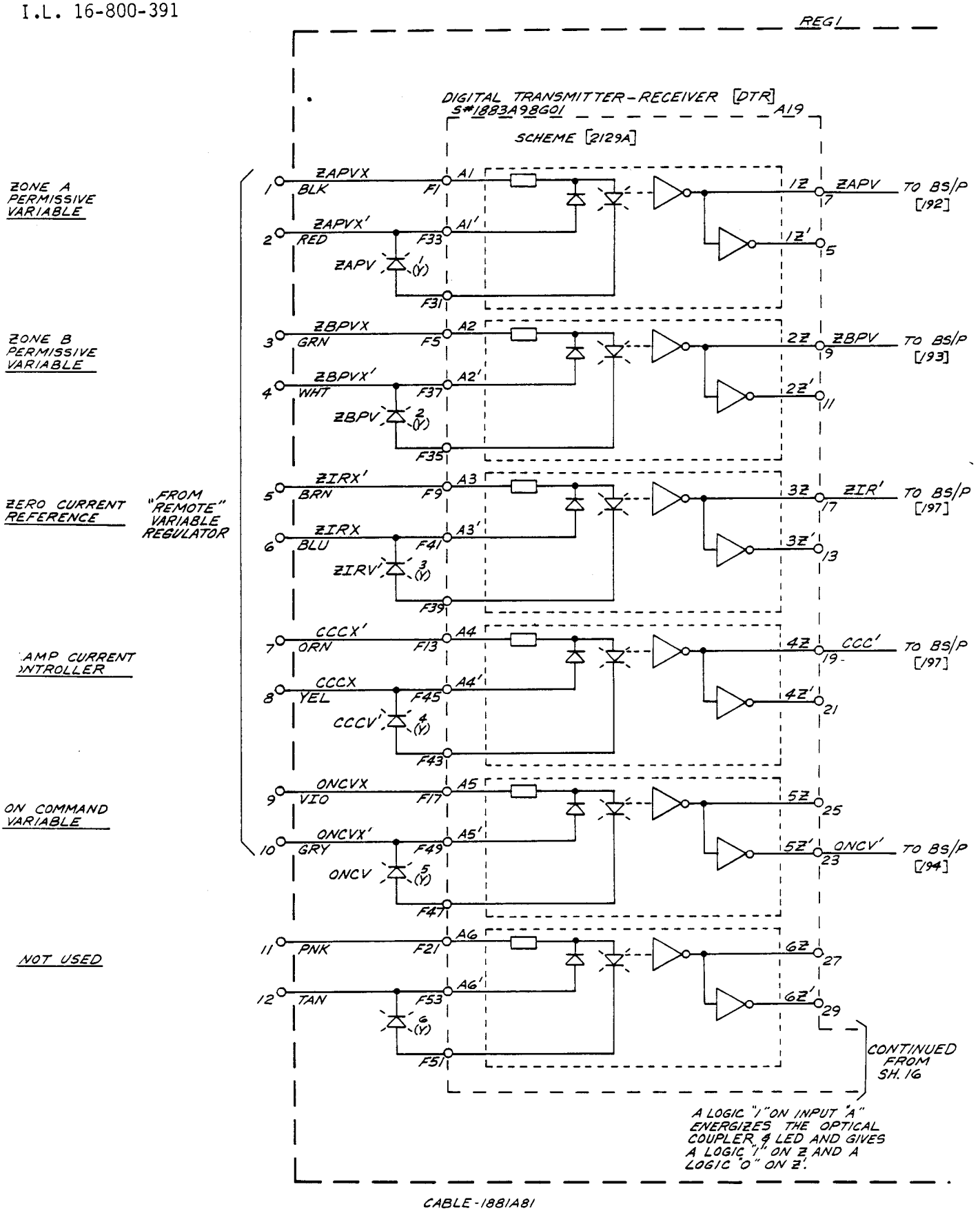
In some systems the requirement exists that both the ac line current and the dc armature current be monitored and the system shut down if an excessive difference exists between the two currents. When required in a system, the DIFFERENTIAL CURRENT AND ITOL card S#1883A96G01 is inserted into cage position B12 to provide this function. See Figure K7-1.

In the basic system, the current feedback is obtained by ac CT's which monitor the input current to the power converter. For a differential current check a dc shunt must be used in the armature circuit and an amplifier/isolator current sensor must be used to generate the required cage signal.



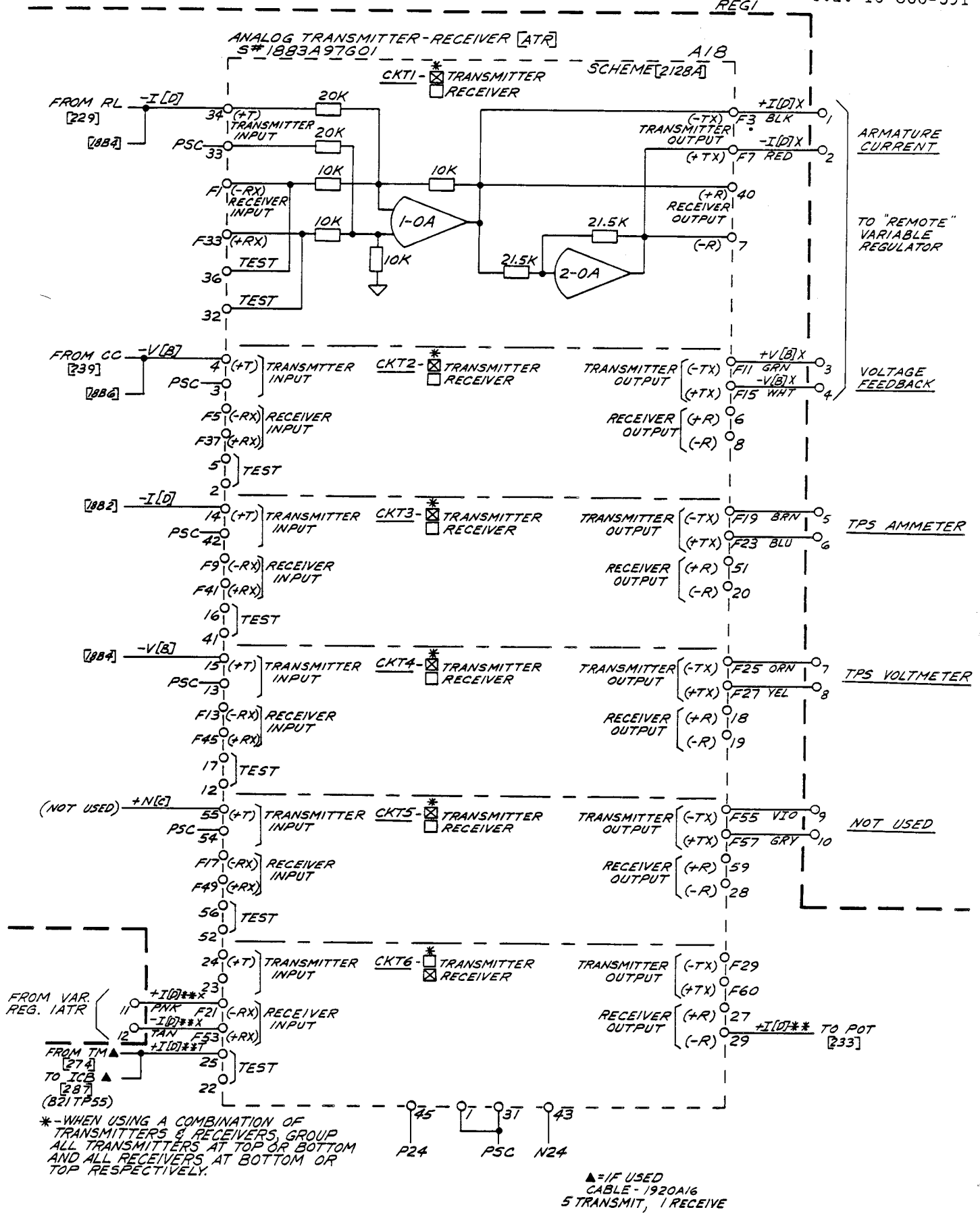
BASIC REGULATOR - DIGITAL TRANSMITTER

FIGURE K1-1



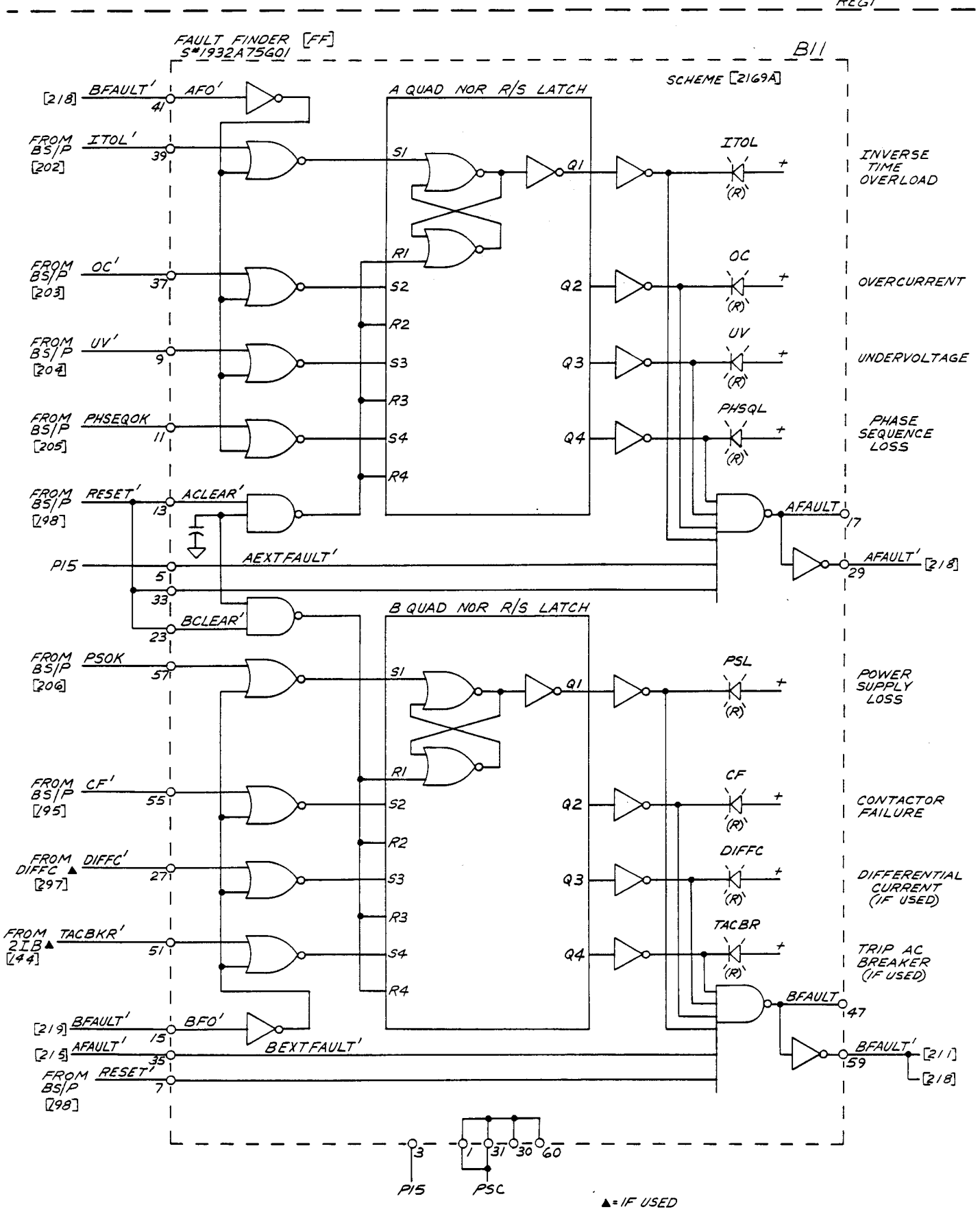
BASIC REGULATOR - DIGITAL RECEIVER

FIGURE K1-2



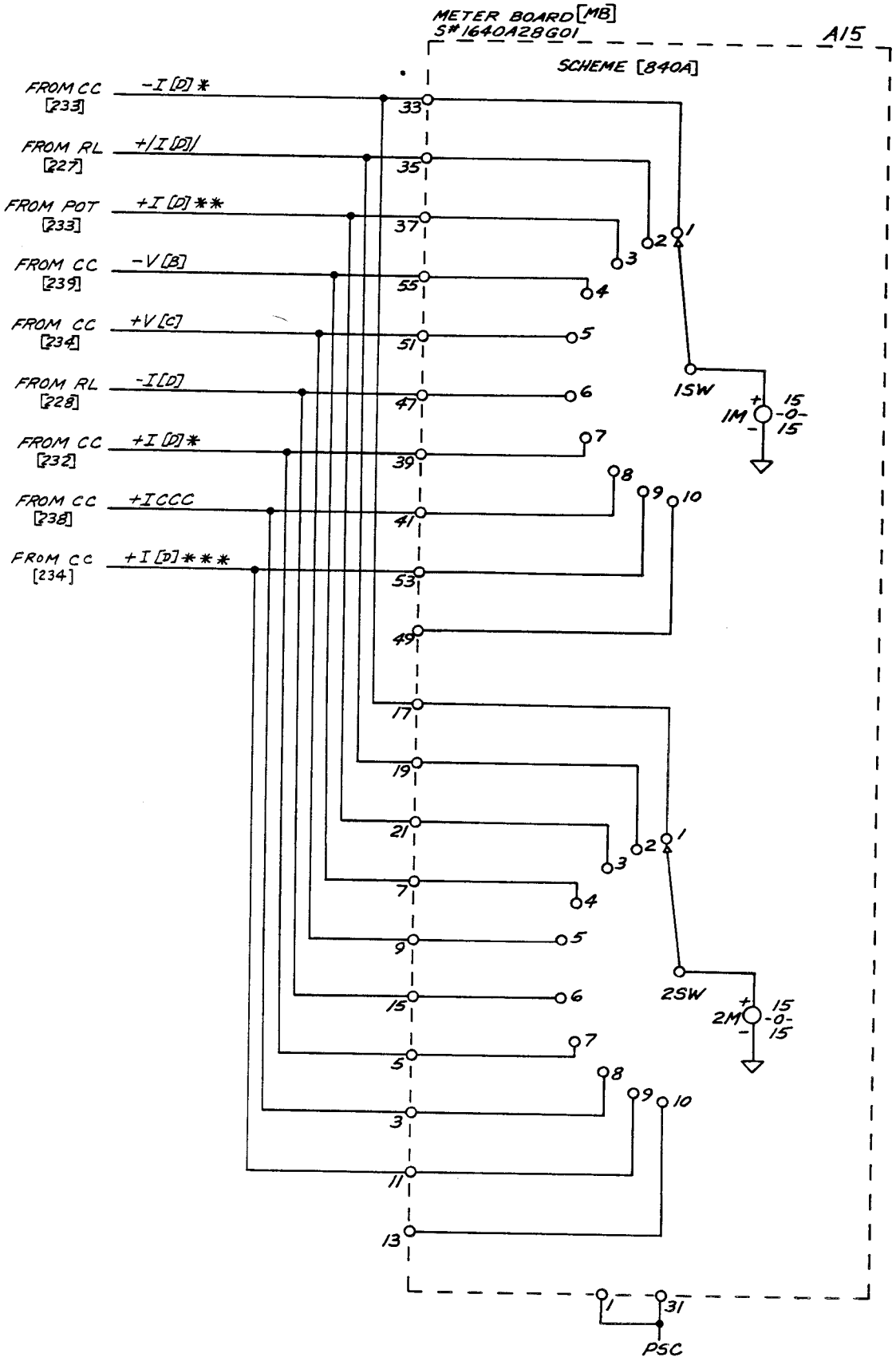
BASIC REGULATOR - ANALOG TRANSMITTER/RECEIVER

FIGURE K1-3



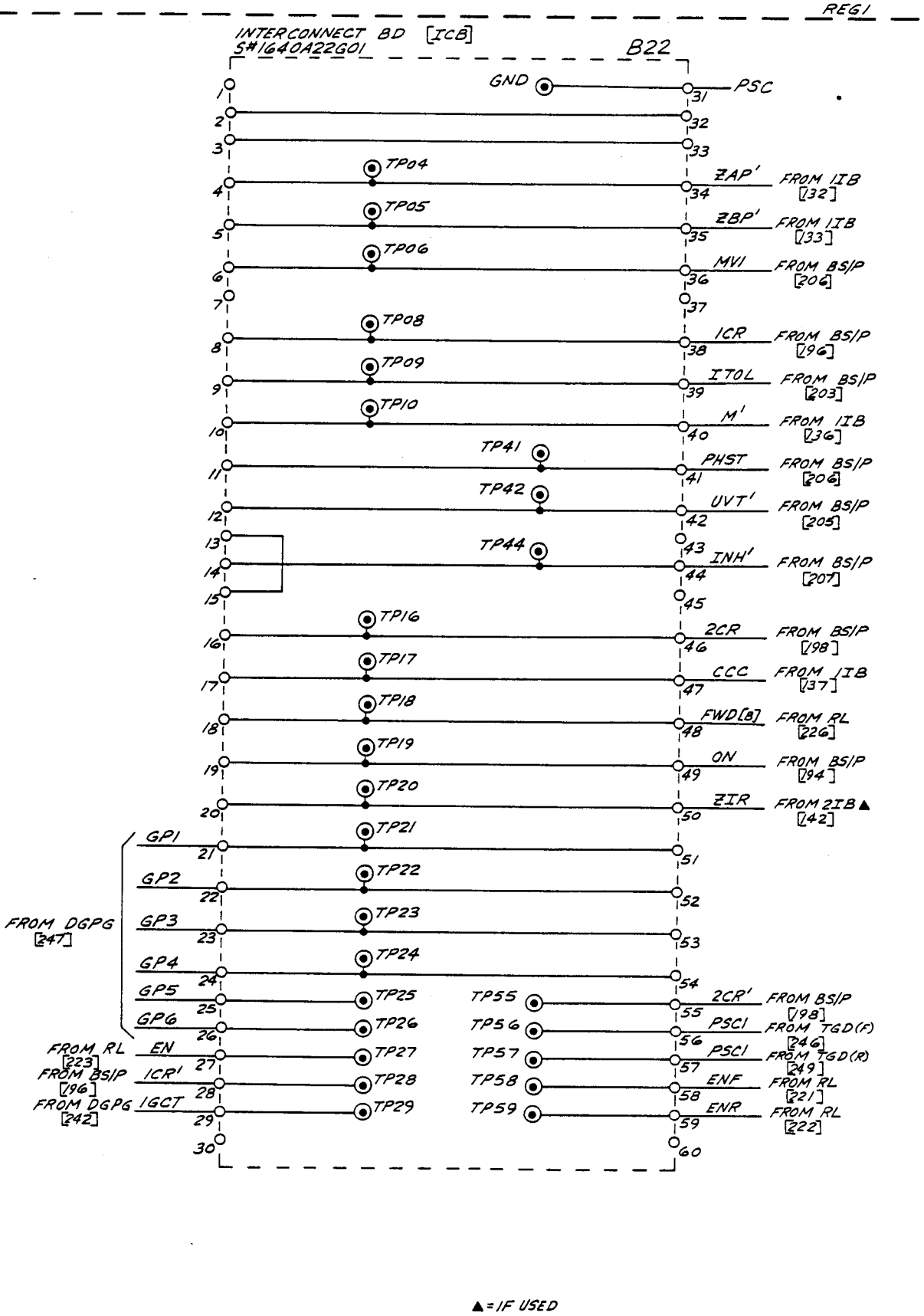
BASIC REGULATOR - FAULT FINDER

FIGURE K2-1



BASIC REGULATOR - METER BOARD

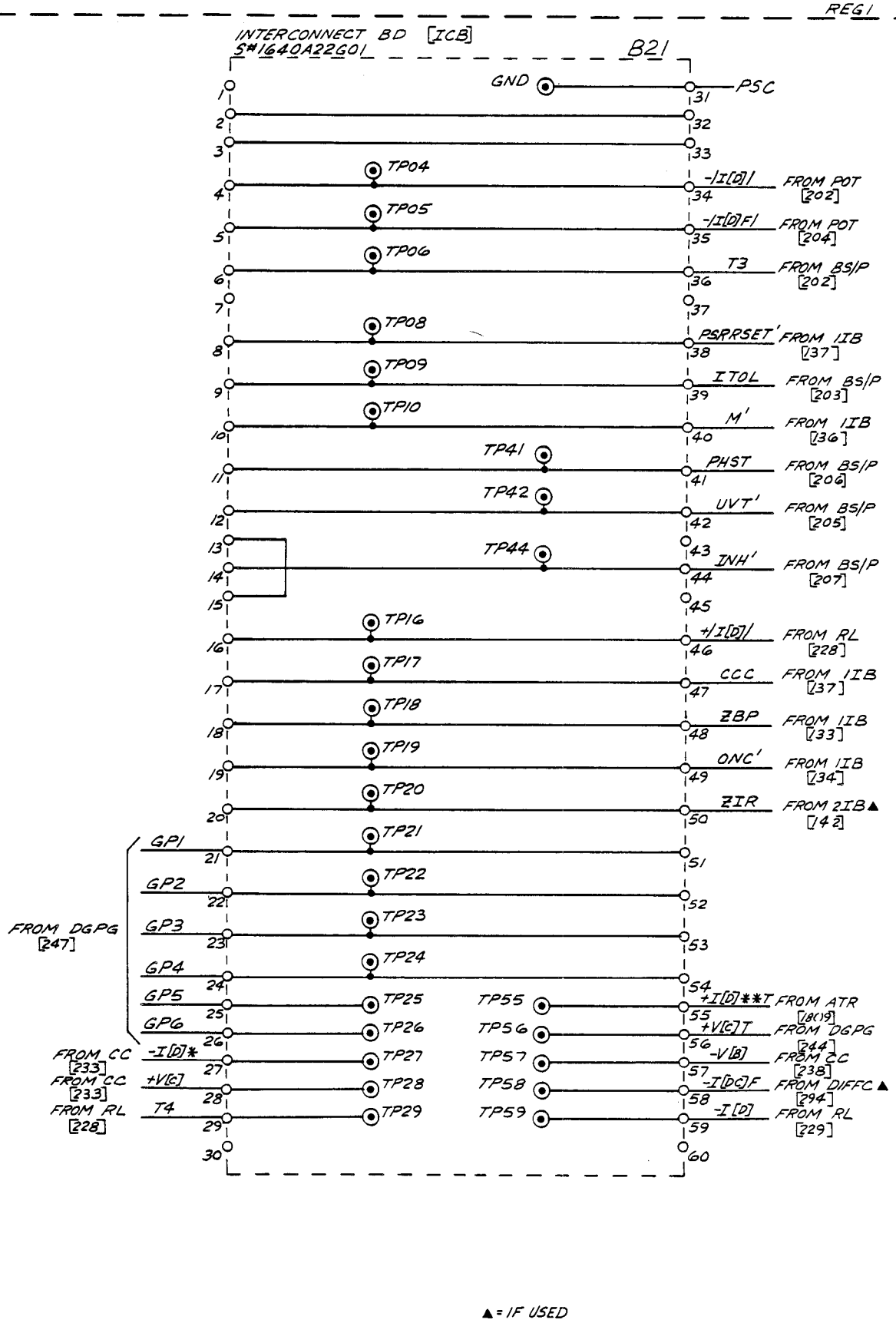
FIGURE K3-1



▲ = IF USED

INTERCONNECT BOARD

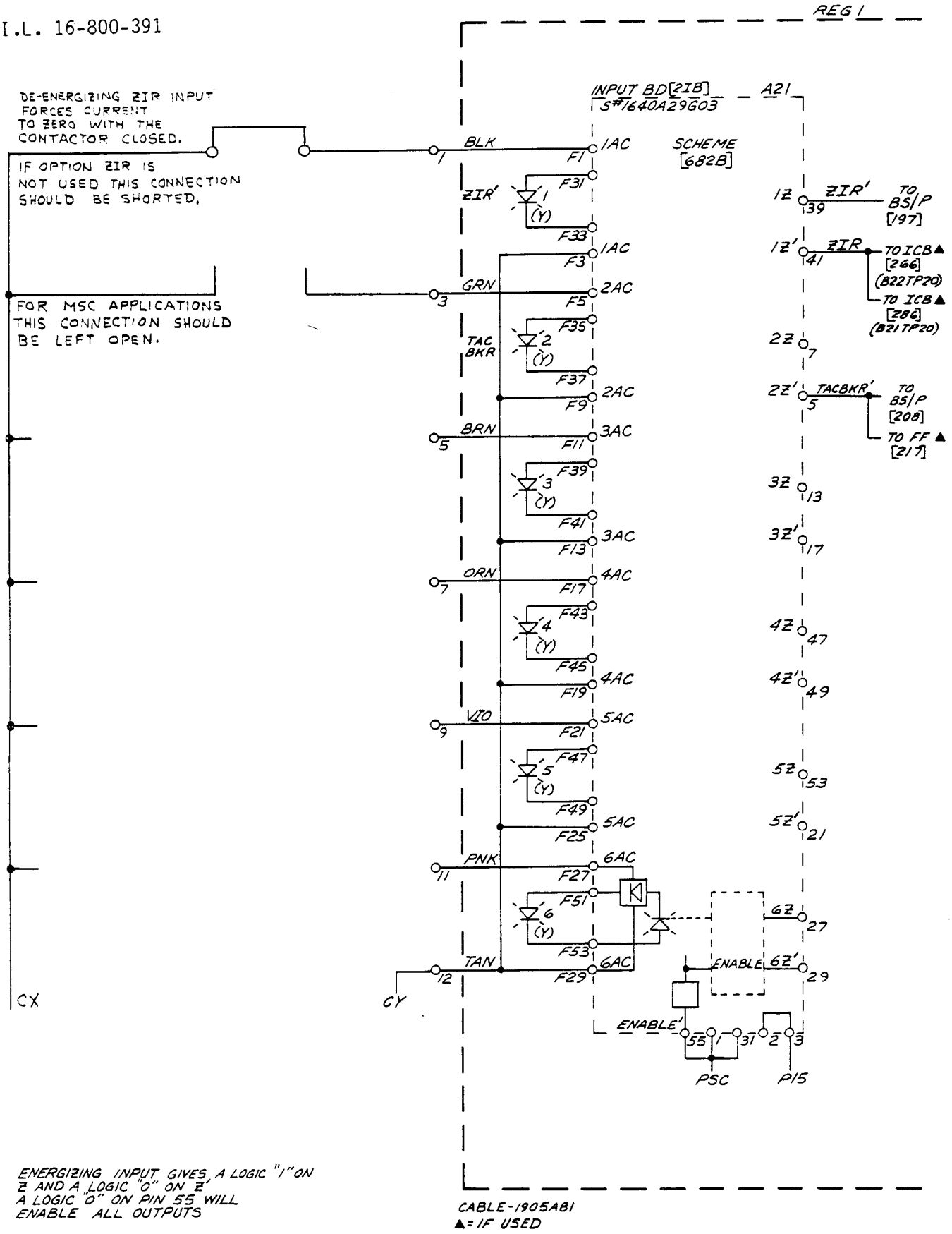
FIGURE K4-1



▲ = IF USED

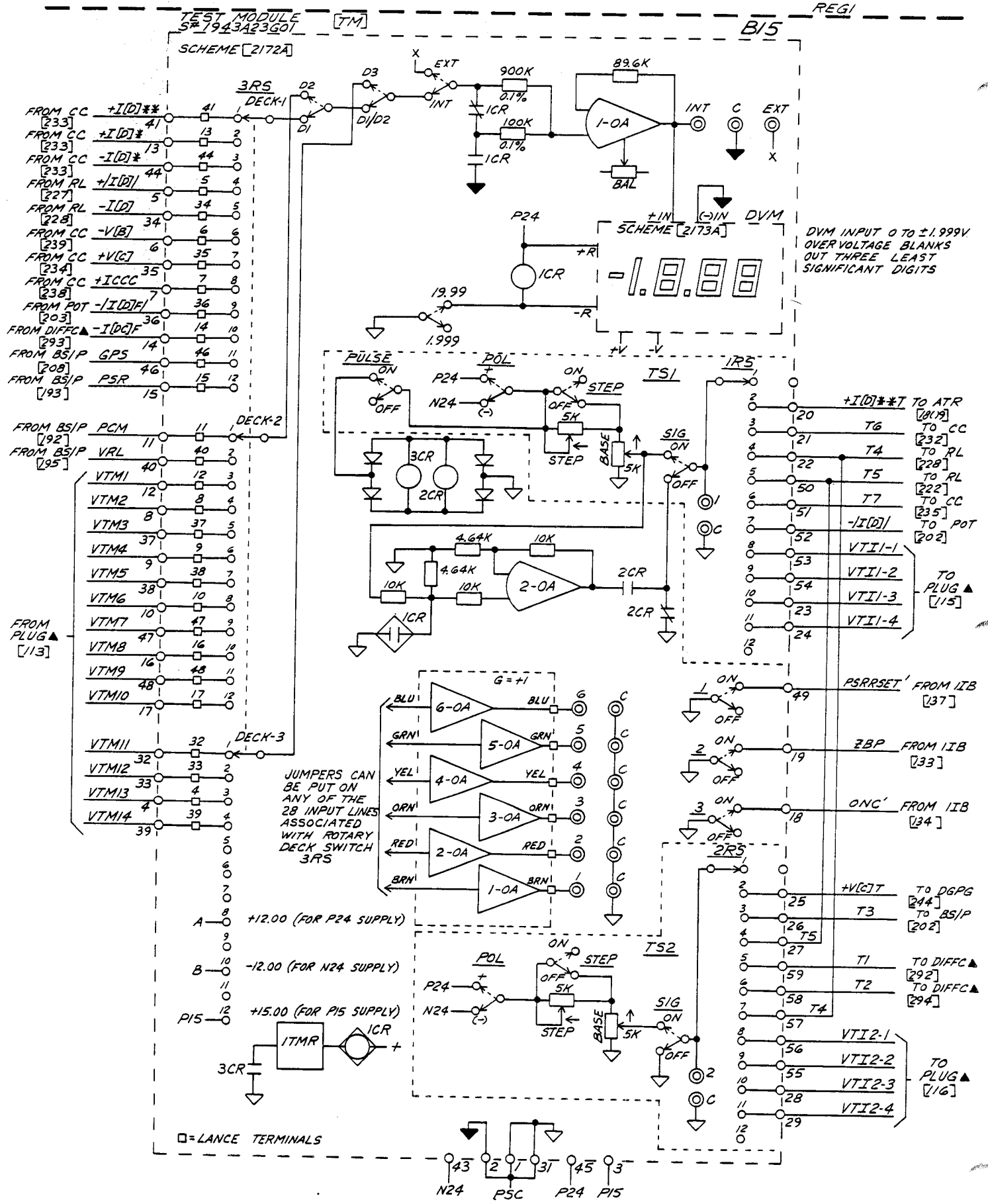
INTERCONNECT BOARD

FIGURE K4-2



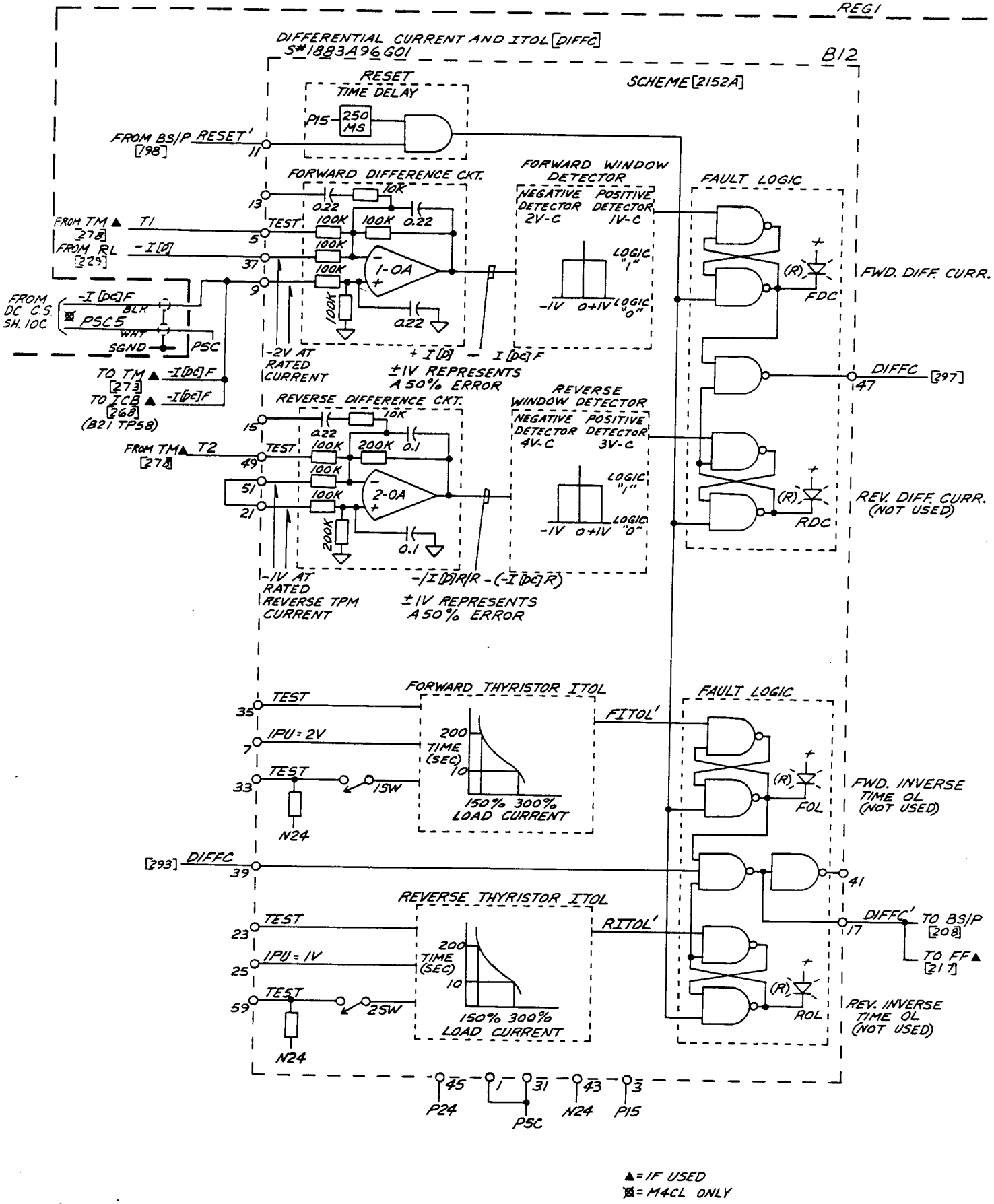
BASIC REGULATOR - INPUT LOGIC

FIGURE K5-1



BASIC REGULATOR - TEST MODULE

FIGURE K6-1



BASIC REGULATOR - DIFFERENTIAL CURRENT & ITOL

FIGURE K7-1