M5B BASIC REGULATOR

INDEX

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A. THEORY OF OPERATION

I. Introduction

All M5B Thyristor Power Systems contain a basic regulator. This basic regulator is housed in one cage complete with cards to gate a Thyristor Power Module (TPM), provide a closed inner voltage loop including reversing control, provide an outer current regulating loop, provide means for opening and closing the dc contactor and to provide fault protection and indication. There are 16 basic styles of basic regulators but all are wired with a common diagram. The various options listed below are accomplished from the basic wiring by a change of cards and/or push-on jumper connections. Full time metering is provided for all critical points and only three calibration potentiometers are required to set up the system. All sequence control is solid state high level logic. The various style numbers are listed in Table I. The remainder of this leaflet describes how these variations are accomplished, how they work, how they are placed in service, and some trouble shooting hints in case of difficulty. Figures I and IA are the basic wiring diagrams for all groups which shows the constant wiring for the backplane and the jumpers required to convert from style to style.

BASIC REGULATOR VARIATIONS

1841A45 GROUP #	AC SUPPLY FREQUENCY		CONVERTER TYPE		60 SECOND OVERLOAD		FAULT INDICATOR CARD	
	60 HZ	50 HZ	SINGLE	DOUBLE	150%	200%	YES	NO
01	X		X		X		X	
02	X		X		X			X
03	X		X			X	X	
04	X		X			X		X
05	X			X	X		X	
06	X			X	X			X
07	X			X		X	X	
08	X			X		X		X
09		X	X		X		X	
10		X	X		X			X
11		X	X			X	X	
12		X	X			X		X
13		X		X	X		X	
14		X		X	X			X
15		X		X		X	X	
16		X				X		X

TABLE I

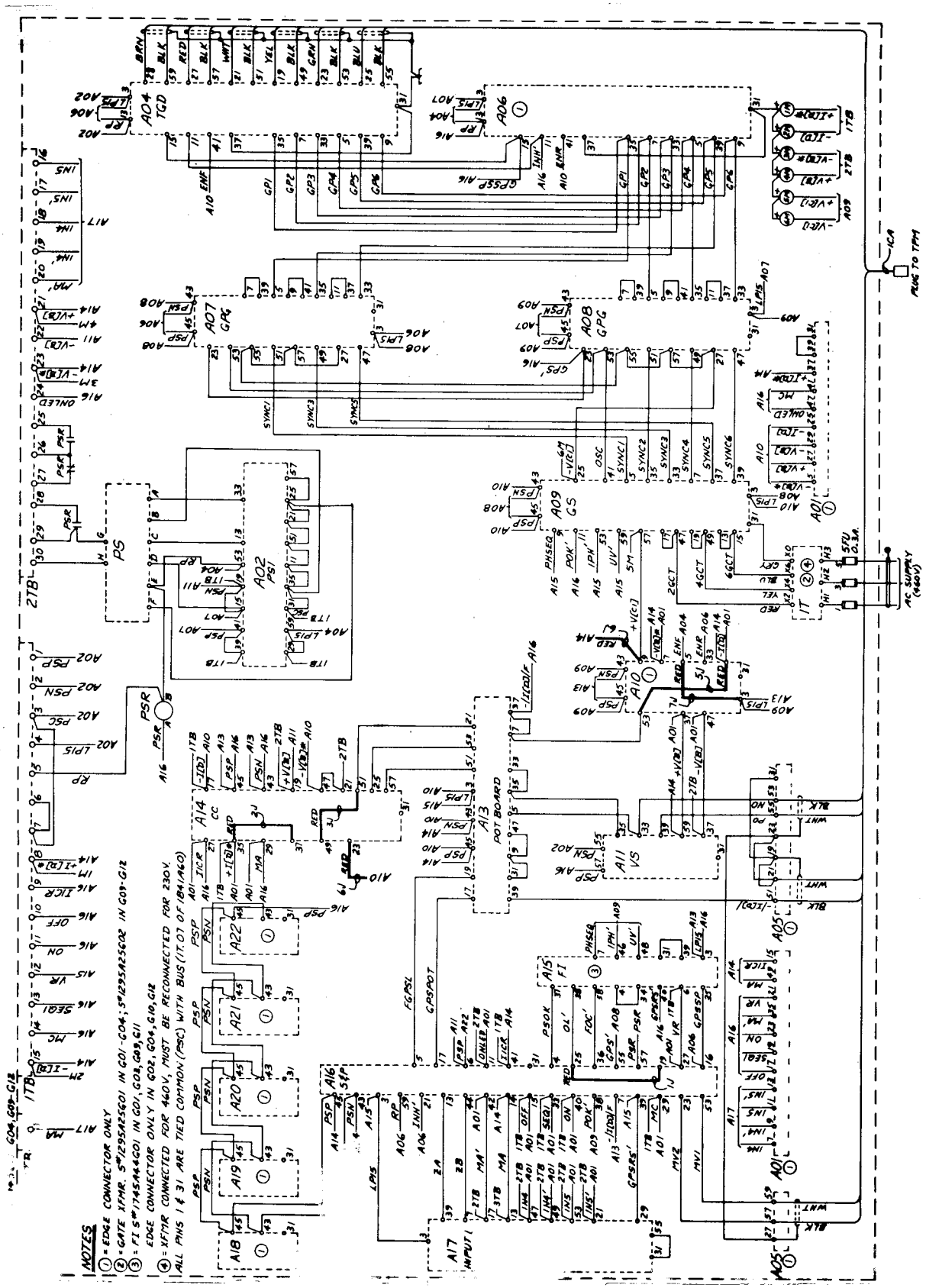

FIGURE 1

BASIC REGULATOR — SINGLE CONVERTER

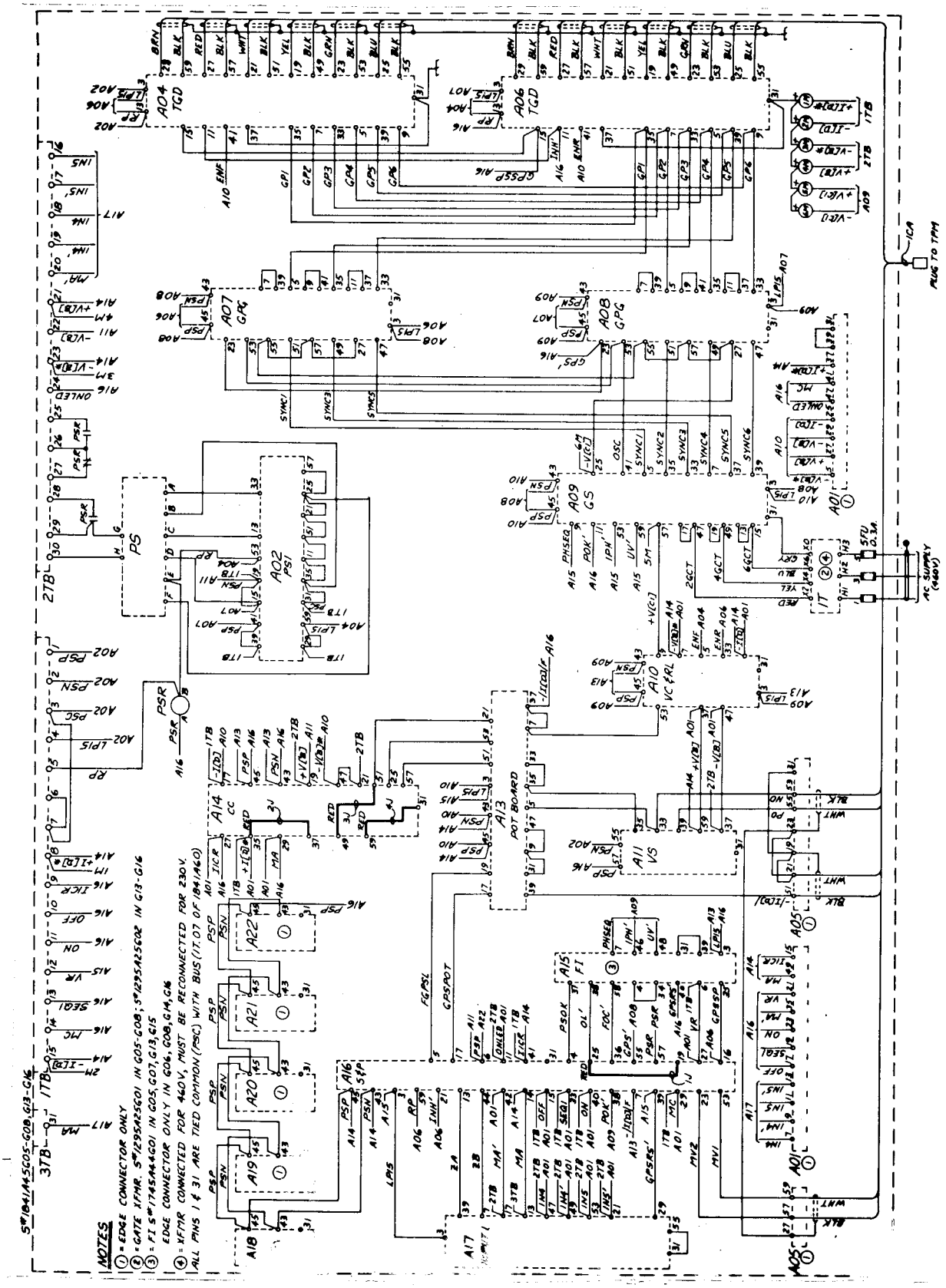

FIGURE IA

BASIC REGULATOR - DOUBLE CONVERTER

II. Thyristor Power Converter

A thyristor power converter is an apparatus which by means of phase controlled gating of thyristors (or other controlled rectifier cells) converts an ac supply line voltage into an adjustable dc voltage; this process is known as rectifying. Inversely, dc voltage can be converted back into the ac line voltage; this mode of operation is called inverting. A converter which only can perform one of these functions is called a rectifier or an inverter, respectively.

Once a thyristor is turned on, it can only be turned off by reducing the anode current to a very small value. In the phase-controlled converters, the ac line voltage performs the function to end the conduction period by commutating the anode voltage.

Many converter configurations have been developed. The six phase, double way circuit (three phase bridge) has evolved as the preferred arrangement for thyristor power supplies. It is simple and offers the best thyristor and transformer utilization. Figure II shows the elementary schematic of such a converter for a six phase system. The transformer is shown delta-wye connected, but the inverse may be used. It is desirable to use the delta connection for at least one winding to eliminate flux ripple of the third harmonic in the core. The main purpose of the transformer is to adjust the line voltage to the proper level, to provide isolation and to introduce inductance into the converter current path. This inductance (or added reactors) is required to control the rates of currents during commutation and faults as will be seen later. The dc output side of the converter is connected to a load circuit consisting of a counter emf e_a, resistance R_d and inductance L_D.

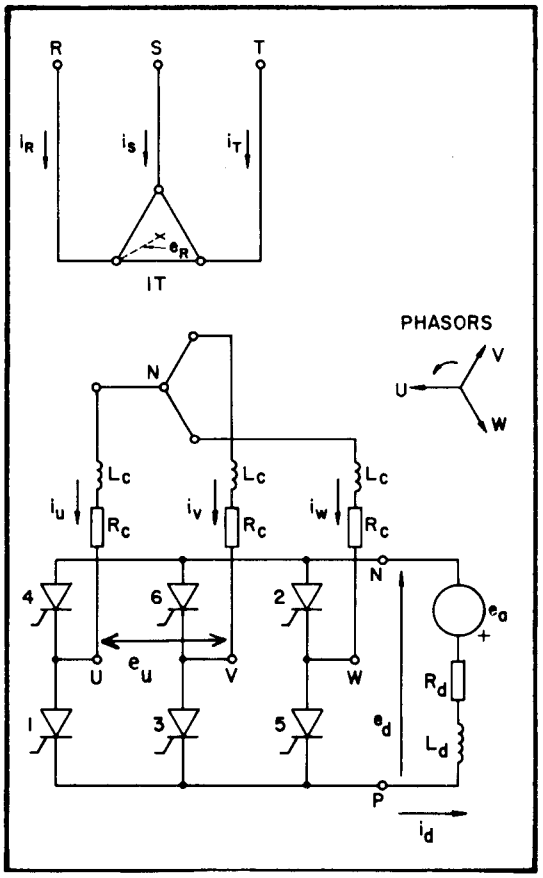

FIGURE II

SIX , DOUBLE WAY CIRCUIT

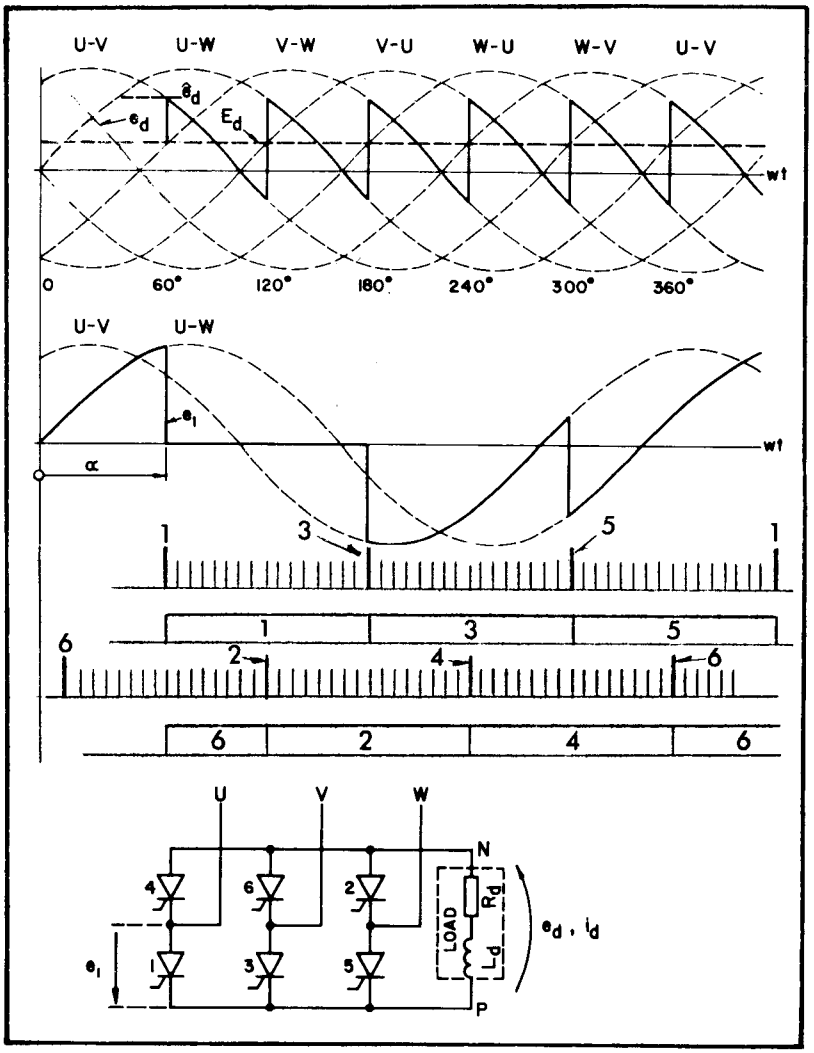

FIGURE III

WAVEFORMS OF THYRISTOR CONVERTER AT ∝= 75°

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The significant current paths and waveforms can now be developed (Figure III). The uppermost traces show the secondary line voltages, measured from the first terminal letter to the second terminal letter. Initially, all thyristors are assumed to be in the blocking state.

At ωT = 15° a pulse train of 120° duration is applied to thyristor No. 6. Since there is no other thyristor gated at this time a current path is not available to carry current. Sixty degrees later at ωT=75°, a pulse train of 120° duration is applied to thyristor No. 1. Now with thyristors No. 6 and No. 1 receiving synchronized pulses a current path is available from U to P through the load to N and then to V. Thus the line voltage e_{uv} is applied to the load. Sixty degrees later at ωT= 135° a pulse train is applied to No. 2; current is flowing in No. 6 and No. 1 at this time, however, the current in No. 6 will commutate to No. 2 because the voltage e_{uw} is greater than e_{uv}. Pulse trains are applied to successive thyristors each 60° and commutations will take place each 60° (on the negative side of the bridge when even numbered pulses are applied and on the positive side of the bridge when odd numbered thyristor gates are applied).

Assuming that the load is highly inductive, the dc current will reach a steady value after a number of cycles, and each thyristor will then conduct a 120° wide current block each cycle. The respective waveforms of the thyristor anode-cathode voltages can now be easily developed. Figure III illustrates this for a gating angle of α = 75°. Note that α is measured from the point where the anode-cathode voltage of the respective cell swings positive. Hence, for α =0, the thyristors do not have to absorb any positive voltage anymore and are then comparable to simple diodes. It is apparent from the waveshapes of the output voltgae that its average value E_d is a function of the gating angle. It reaches a maximum at α = 0°, is zero for α = 90° and assumes negative values back to α = 180°. This transfer curve can be obtained by integrating the waveforms. The result is:

$$E_d = E_{do} \cos \alpha$$

where the saturated output voltage is

$$E_{do} = \frac{3\sqrt{2}}{\pi} E_u$$

where E_u --- line-to-line rms ac voltage.

Since the load current cannot reverse, the average power flow will change its sign with the voltage. Rectifier operation (α<90°) renders motoring in the load circuit whereas inverter operation (α>90°) requires the load to be generative.

Figure IV illustrates the range of operation on a time basis. In the beginning, the converter is operated in its rectifying mode with α = 0. Then α is steadily increased into the inverter mode of operation. The lower trace shows the voltage across one of the thyristor legs.

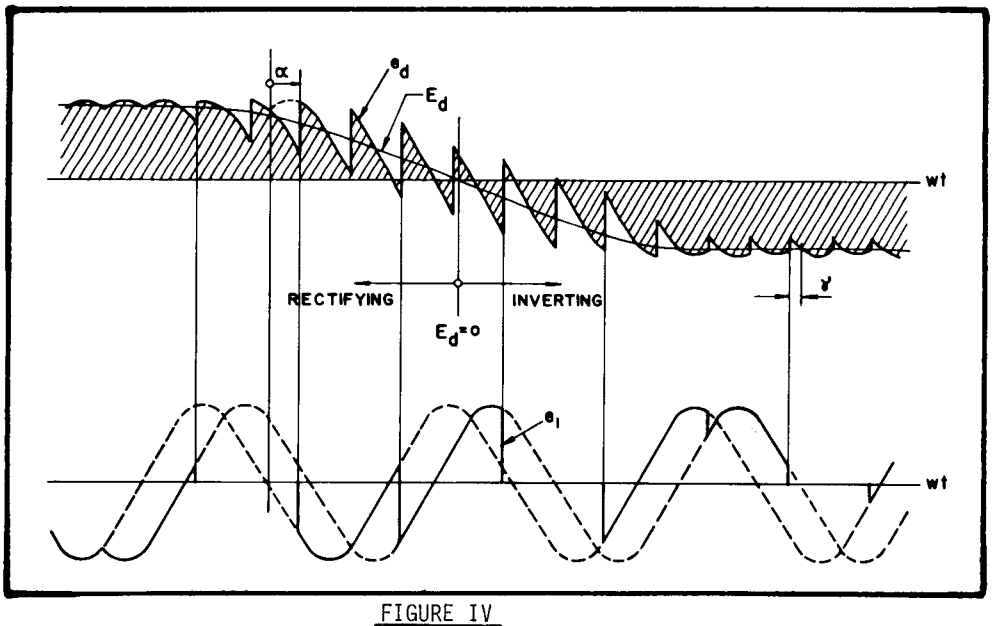


FIGURE IV

RANGE OF OPERATION ILLUSTRATED ON A TIME BASIS
ON THE LEFT, α = 0, RECTIFYING MODE.
α THEN INCREASES TO INVERTER MODE.

Up to this point, the reactances offered by the transformer, reactors in the ac line and the power line have been neglected. This so-called commutating reactance, however, is significant. Instead of instantaneously commutating the load current from one leg to another (upon gating of the latter), the current rate is limited and shaped by it. This means both these legs conduct simultaneously for a period of time, shorting out effectively the ac source. This produces notches in the sine wave measured on points U-V-W, which, in turn, reduce the dc bus voltage.

Taking account of these commutation effects, one can derive a converter equation which includes this reactive drop:

$$E_d = E_{do} \cos \alpha - E_{do} \; 1/2 \, X_c \; I_d/I_{dn}$$

where x_c --- relative reactance of transformer, ac reactors and line (based on I_{dn})
I_d --- actual dc current
I_{dn} --- nominal (rated) dc current.

The assumption made so far was that the dc load current is continuous, and the equation applies for this condition only.

In a practical circuit such as commonly found with dc motor armatures as load, the actual operation always covers the range of discontinuous current at light load levels also. Reducing the load current, one finally reaches a level where the ripple amplitude is high enough to interrupt the current cyclicly. At this transition point, the regulation characteristic takes a sharp break and aims to a point equal to the peak converter voltage e_d at zero load current. This transition point depends on the gating angle α, the inductance and the losses in the load circuit.

Commutation from a first leg to a second must always be completed before the anode voltage of the second leg swings negative. If the latter should happen, the cummutation is incomplete and the full-load current will commutate back into the first leg. This situtaion can only arise if the commutation was initiated at a high angle (in the inverter range) and if the load current is continuous.

The circuit described so far can provide voltage of both polarities. The current, however, can only flow in the conducting direction of the rectifying cells. This circuit is, therefore, classified as unidirectional or single converter.

If current reversal is required, a second converter can be added and connected to the first one in an antiparallel circuit as shown in Figure V. Since such a circuit can produce load current in both directions, this circuit is classified as a bi-directional or double converter.

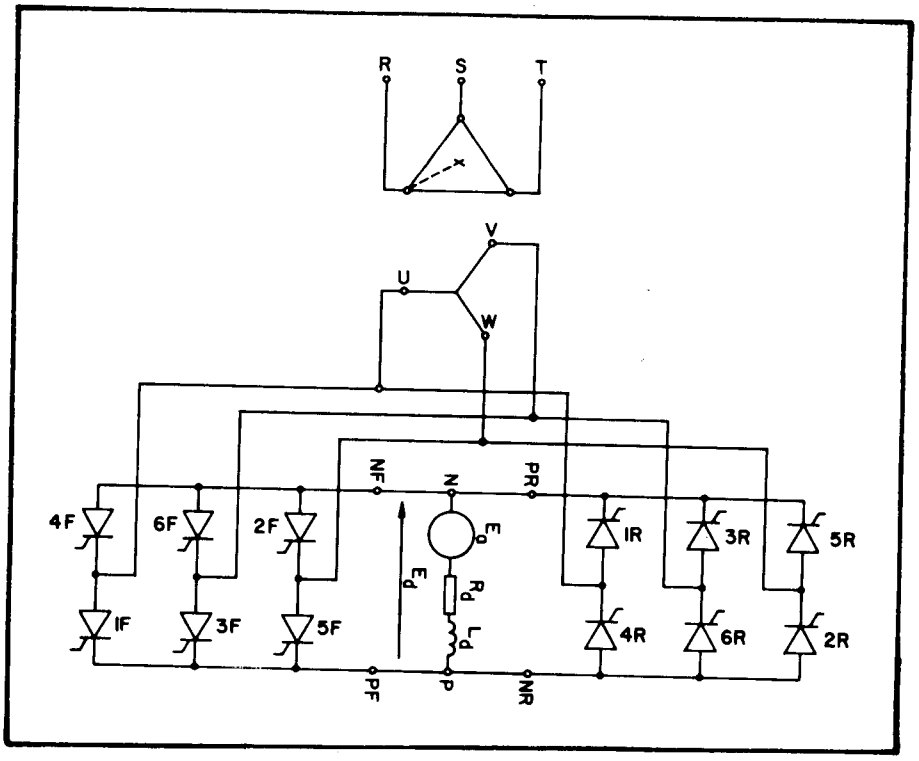


FIGURE V

DOUBLE CONVERTER
ANTIPARALLEL CIRCUIT

There are several ways to control such a double converter. The principle used in M-5B is to use one gate pulse generating system shared by two (forward and reverse) pulse amplifiers (Thyristor Gate Drivers); with a logic system so that only one Thyristor Gate Driver (TGD) can be operative at any time. The logic and control system determines whether the forward or reverse converter should be gated. The operation will now be explained with the help of Figure VI and Figure VII. The systems diagram shows the main control elements of the double converter, with the power circuit in single line diagram form. An inner voltage loop is closed. This regulating loop helps greatly to overcome the nonlinearities of the power converter when going from continuous to discontinuous current. This loop makes it possible to consider the converter system for the outer (variable regulator) loops as a "black box" amplifier with nearly ideal (linear) characteristics.

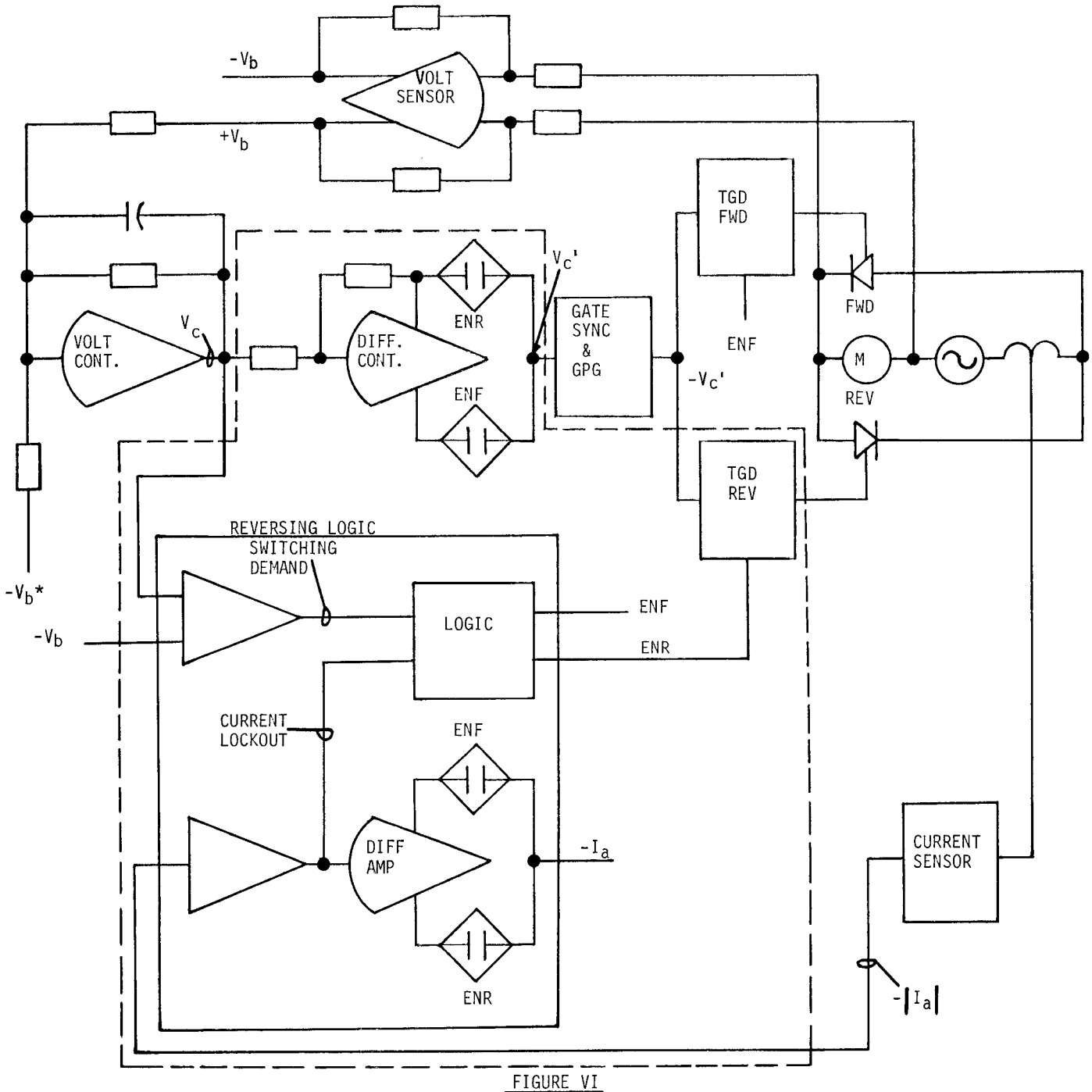


FIGURE VI

DOUBLE CONVERTER CONTROL SYSTEM

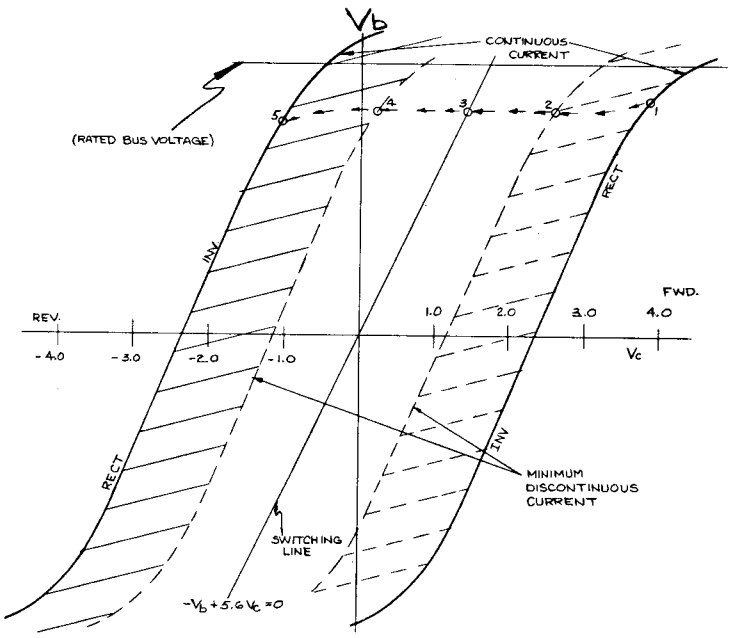


FIGURE VII

DOUBLE CONVERTER
CONTROL CHARACTERISTICS

The bus voltage is picked up by the voltage sensor (VS) and brought to one input of the voltage controller (VC) where it is compared with the reference voltage $-V_b^*$ applied at a second input. When both inputs are zero, V_c will be zero as will V_c' which corresponds to a gating angle of $\alpha = 145°$ due to a bias in the gate synchronizer (GS).

In operation, depending on the polarity of the difference of the two input voltages to the voltage controller, control voltage V_c will swing positive or negative. By comparing this voltage V_c with bus voltage $-V_b$ the polarity of required converter conduction can be determined. For example, if bus voltage V_b is smaller than the reference $-V_b^*$, forward load current is indicated, and therefore the forward channel of the double converter should be pulsed. Under this condition V_c is positive going and compared with $-V_b$ at the input of the reversing logic will result in ENF to be a logic "1" and pulsing from the forward TGD is released. If now the reference $-V_b^*$ is reduced to demand reverse current. the opposite sequence of events will take place.

Figure VII shows the output of the power converter as a function of V_c for the cases of continuous and minimal discontinuous (pulsing) current. The shaded area between represents the field of various possible states of discontinuous current conduction.

It should be noted that the signal V_c' going to the GS is equal to V_c when forward gating is required; and equal but opposite to V_c when reverse gating is required. The gating system requires a negative going (less positive) voltage to phase advance, therefore an absolute value circuit is used (represented in Figure VI by DIFF. CONT. and logic contacts on its outputs) to invert V_c' from V_c when the reverse TPM is being gated. This inversion is also required to establish the proper polarity (always negative feedback) for total loop gain.

The case of minimal discontinuous current is mainly of interest for armature loads. It is representing the case for a gating angle adjustment where the peaks of the converter output voltage (e_d) are just matching the counter emf of the motor (See Figure III). For any higher gating angle no current conduction can set in any more. This then means that no current flow can continue in the area passed the minimum discontinuous current line. Shifting into this area indicates that current of the opposite polarity is required. However, to simplify the sensing of this condition and to add some safety margin, actual switching is initiated when the indicated switching line is crossed.

As shown in Figure VII current will be zero when switching from forward to reverse gating under normal operating conditions. However, some fault conditions can occur (inverter fault for example) which would ask for a gating reversal with current flowing. Also in the reversing logic is a current lockout feature which prevents gating crossover until current drops to a very low value (less than 5% of rated current) so that circulating current faults

will not be initiated due to other faults. Shown in the reversing logic as well as in a polarity selector for current feedback. This is shown as a differential amplifier with reversing contacts on the output. Current feedback is negative for forward current, and positive for reverse current.

With the converter in the forward conduction mode, a reversal shall now be described. The counter emf e_a of the load is assumed to be as shown in Figure VII with the forward converter rectifying at point 1. Enable forward (EN FWD) is a logic "1" and forward gate pulses are released. Suddenly the reference $-V_b^*$ is lowered to a value below e_a demanding a current reversal. This will cause the VC output voltage V_C to advance toward negative values. At point 2, forward current will stop altogether; and at point 3, the reversing logic will be initiated. EN FWD will become a logic "0" stopping forward pulses. About 2ms later EN REV will change from a logic "0" to a logic "1" releasing reverse pulses. At point 4, the reverse converter starts to pick up current in the inverting mode. Finally at point 5, the new quiscent state of reverse conduction has been reached where V_b is again matching the reference $-V_b^*$.

The opposite sequence of events take place in case of a change from reverse to forward current. Figure VIII shows an oscillogram of a current reversal in a double converter with current regulator.

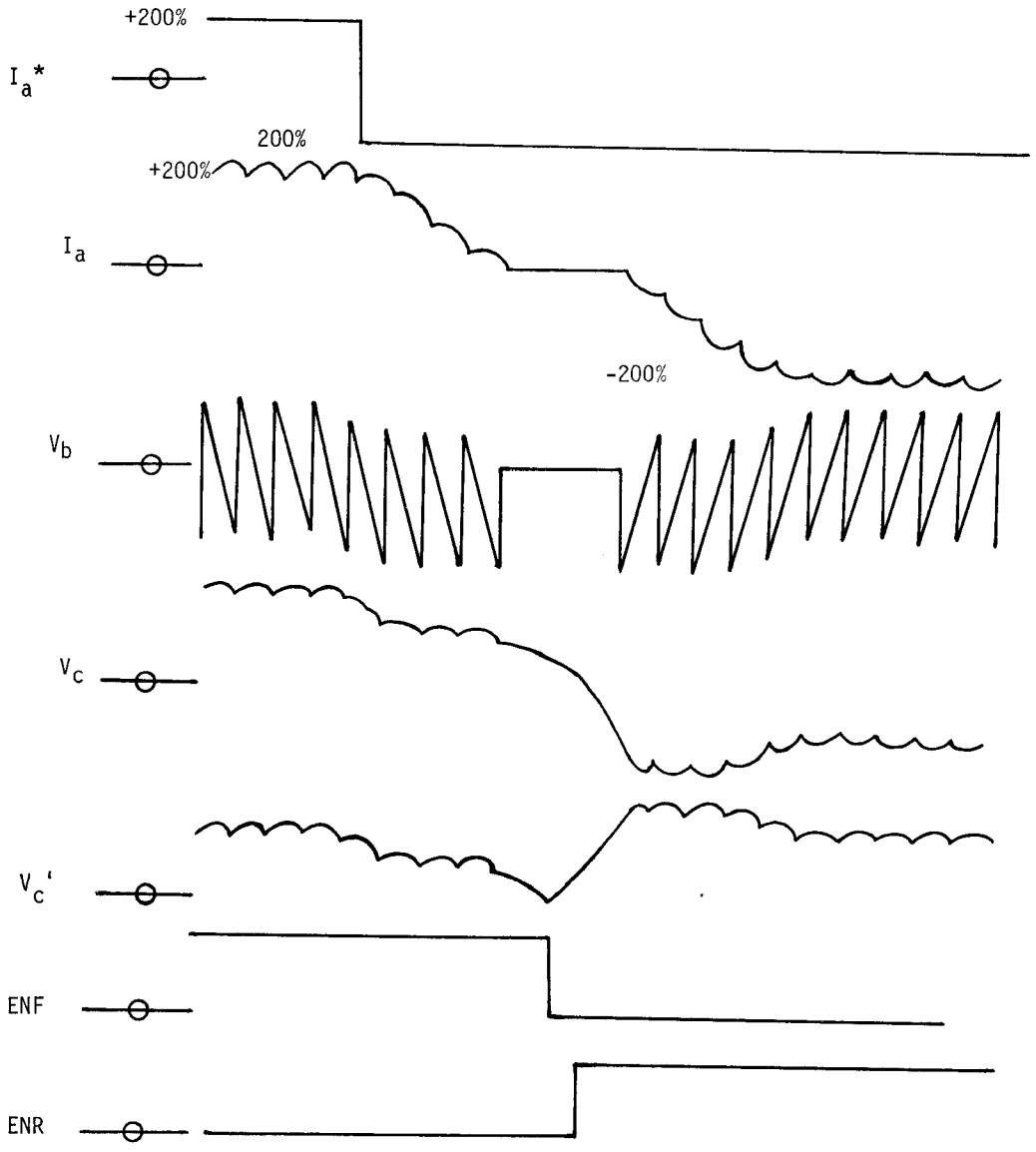
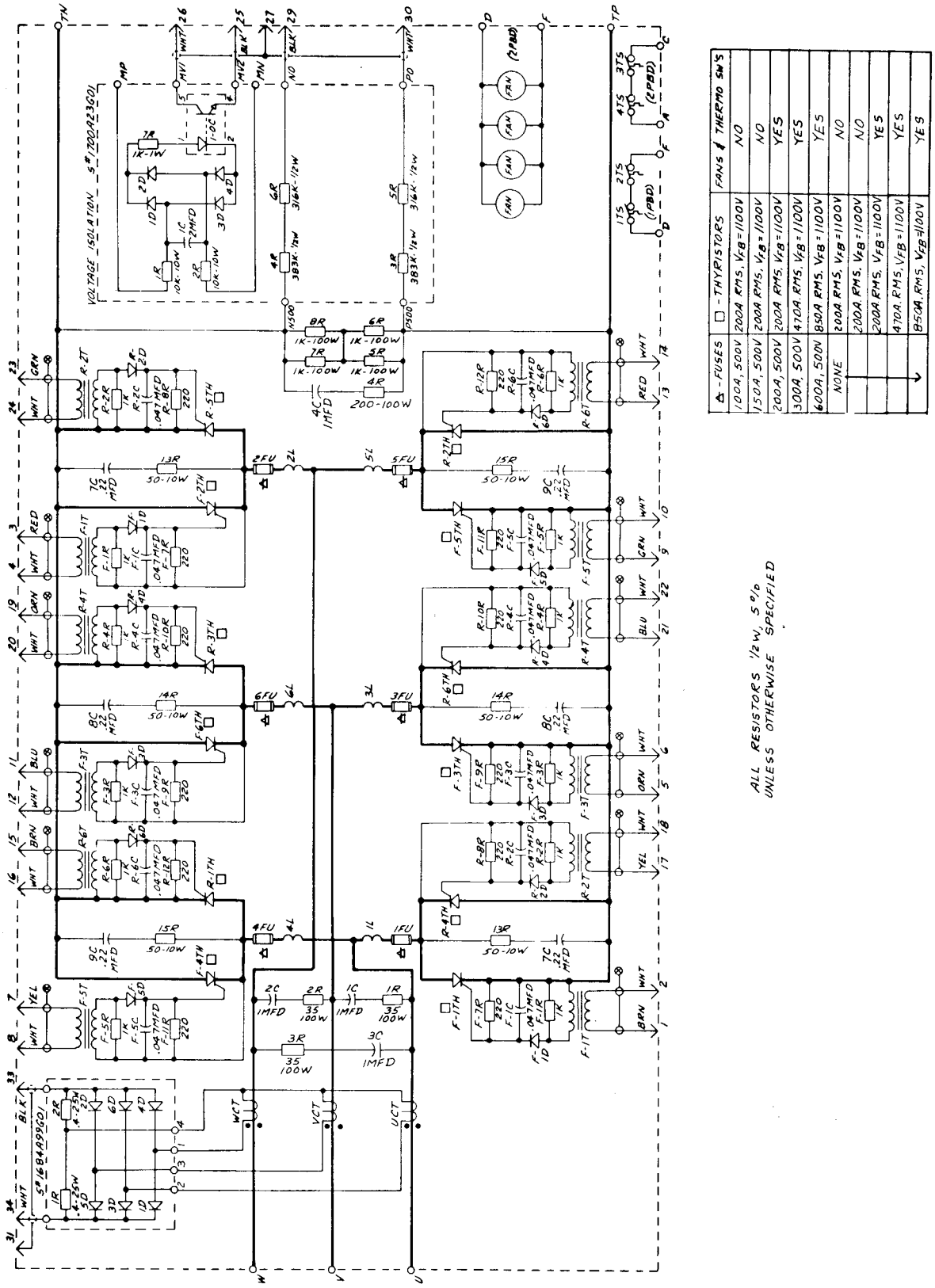


FIGURE VIII

The thyristor power modulator (TPM) assembly includes the thyristors mounted on heat sinks in a six-pulse, bridge circuit. Two thyristors are connected in antiparallel in the case of double converters. This TPM also contains current transformers, current sensor, thyristor R-C networks, thyristor gate pulse networks, preload resistors, AC and DC R-C networks, ferrite core assemblies, an attenuator network for voltage feedback, and a static motor voltage sensor. Fans are used on sizes greater than 150A, with thermo switches added for air loss detection. For class III protection fuses are included. A typical diagram is shown in Figure IX.



Δ - FUSES	□ - THYRISTORS	FANS & THERMO SW'S
100A, 500V	200A RMS, V_{FB} = 1100V	NO
150A, 500V	200A RMS, V_{FB} = 1100V	NO
200A, 500V	200A RMS, V_{FB} = 1100V	YES
300A, 500V	410A RMS, V_{FB} = 1100V	YES
600A, 500V	850A RMS, V_{FB} = 1100V	YES
NONE	200A RMS, V_{FB} = 1100V	NO
	200A RMS, V_{FB} = 1100V	NO
	200A RMS, V_{FB} = 1100V	YES
	410A RMS, V_{FB} = 1100V	YES
↓	850A RMS, V_{FB} = 1100V	YES

FIGURE IX

DOUBLE CONVERTER TPM

The TPM has current ratings of 150A, 250A, 360A, and 660A with voltage ratings of 240V and 500V. For class III protection, fuses protect thyristors from circulating current faults and inverter faults by melting and clearing the fault. For class I protection, an ac thyristor breaker and dc breaker mounted on the contactor panel, with a high impedance transformer is required to protect thyristors, and fuses are not used.

Thyristor R-C networks are used to store hole recovered charge from thyristors at turn off of current. Ferrite core assemblies attenuate excessive rates of voltage, which otherwise may lead to undesired turn on of thyristors. R-C networks across the AC line and DC output damp the oscillations that would otherwise be produced by the commutation process. Gate pulse transformer networks provide isolation and shaping for the gate pulses.

Three current transformers are connected in a wye network across the current sensor bridge and to the center point of the burden resistor. This rectified signal of the ac line currents is a true reflection of the dc load current flowing during operation. The current feedback (termal 33) is always negative. Three sizes of CT's are used; 200 to 5, 400 to 5, 600 to 5. Voltage at terminal 33 with respect to terminal 34 (of the TPM plug) is:

$$I_a = - I_{dc} \times \frac{5 \times .76 \times \text{PRI TURNS}}{\text{CT (200, 400, or 600)}}$$

More than 1 primary turn is only required on the 200 to 5 CT and where the rated dc current is below 120A.

The static motor voltage sensor picks up when motor voltage exceeds about 20V. This signal is used in the regulator sequencing to prevent contactor pickup should the motor have appreciable voltage on at the time of contactor initiation; providing the function previously performed by a VR relay.

The five power connections (3AC and 2DC) are bolted connections to studs. Connections of gate leads from the regulator, and feedback signals to the regulator are made with a single plug connector. Connections to the fans and thermo-switches are screw terminal connections on the pulsing boards.

III. Gate Pulse Generating System

The M5B gate control system consists of a gate control transformer (GCT) S#1295A25; the reversing logic portion of the voltage controller card (VC & RL) S#1757A01 for double converters; portions of the gate sync card (GS) S#1710A08 for 60 hz operation, S#1752A12 for 50 hz operation; two gate pulse generator cards (GPG) S#1671A17; two thyristor gate driver cards (TGD) S#1861A45*for double converters, one for single converters; some components associated with the pulsing circuits of the thyristor bridges; the inhibit ($\overline{\text{INH}}$) and gate pulse suppression ($\overline{\text{GPS}}$) functions of the protection board; and the interconnecting wiring.

Features designed into the M5B Gating System are:

(1) Reversing Logic - Only one converter can be gated at a time.

  (a) Primary Crossover Logic - Comparison of voltage feedback to voltage demand signal, which is generated internally in the VC & RL card, to determine whether forward or reverse converter operation is required.

  (b) Current Crossover Lockout - Crossover cannot be initiated when current is greater than 5% of rated. Current will always be zero when crossover is asked for under normal operating conditions. Under certain fault conditions (inverter faults) crossover could be asked for with high current flowing, by the voltage crossover logic, however, the current lockout feature prevents crossover faults to be generated on top of initial fault.

  (c) Bias - Is preset for the regulating system used. It assures smooth intiation of current and voltage at start of gating and smooth crossover.

(2) Synchronizing Signals - Are spaced precisely 60° apart.

  (a) Gate Control Voltages - From GCT are directly in phase with the TPM supply voltage. In most cases the primary of GCT is taken directly off the TPM transformer secondary. In this case gating is correctely phased with no change in gate control wiring, regardless whether TPM supply transformer is delta-delta, wye-delta, or delta-wye.

NOTE: * - Some earlier model basic regulators may have S#1668A25 thyristor gate driver cards (TGD).

(b) Sync Signal Generation - Zero crossing detection of GCT waves only, and are well filtered. Filtering virtually eliminates distortion due to commutation notches and higher frequency harmonics. Zero crossing detection eliminates any effects of line amplitude fluctuations.

(3) Phase Advance Limit - Fixed at 0°. No additional margin required in TPM transformer as would be the case for a fixed at greater than 0°.

(4) Picket Fence Gating - Pulses are delivered directly from firing transistor in TGD or GPA to thyristor pulse transformer to be fired. No steering diodes required as in double pulsing. Pulsing power supply is a highly filtered dc supply and is immune to large line distortion and fluctuations. Gating power is not sensitive to phasing.

(a) Hard Pulse - Gives large overdrive to thyristors for quick turn on at first pulse; when high di/dt can occur, for discharging R-C networks in conjunction with commutation of high current levels.

(b) Trailing Pulses - Are available and required to refire thyristors when operating under light load, discontinuous current operation. They are of reduced amplitude and duration to reduce loading on the gate.

(c) Tail End Chop - Shortens pulse train (t_0 less than 120°) where gating cannot be required when operating at high delay angles. This reduces reverse leakage dissipation when thyristors have reverse voltage applied.

(d) Ramp Gating - Generates six pulses at 60° intervals with variations of less than 1° at α = 180° which is worst tracking angle. Phase angle is directly proportional to control voltage over the range of $0 \leq \alpha \leq 180°$.

(e) Ring Counter - Turns off preceeding pulse in its half of the converter (3 turns off 1, etc.) as preceeding pulses are no longer required under any operating conditions.

(5) Adjustments - None are required within the gating system.

The VC & RL establishes a phase angle demand signal +Vc. It as well establishes which converter, forward or reverse, is to be gated with signals ENF or ENR.

The GS has three functions associated with gate control. It receives three sinusoidal waves displaced 120° which are in phase with the TPM supply voltage. It uses zero crossing points to generate 6 sync pulses displaced 60° which start, and at a later period reset, timing ramps in the GPG. A 12k hz free running oscillator is also located on this board and is used as clock pulses for all trailing pulses generated. The third circuit on the GS provides the bias and phase advance limit function which conditions the phase demand signal ($+V_C$ to $-V_C$) from the VC & RL before it goes to GPG.

The GPG(s) process the sync signals (1, 3, 5 and 4, 6, 2), phase control signal ($-V_C$), clock pulses, as well as $\overline{GPS}$ permissive signal to generate a pulse train(s) with proper starting phase angle, correct width of pulses, and correct termination of pulses. A sync signal of 240° duration starts a timing ramp at 10 prior to α =0°. Signal $-V_C$ determines at what time ($0° \leq \alpha \leq 180°$) after start of ramp the pulse train is triggered. The width of the hard pulse (first pulse) is timed within the GPG. Clock pulses are mixed with a timing window to provide trailing pulses. The first pulse and trailing pulses are not synchronized; first pulse timing is determined only by $-V_C$, and trailing pulses are determined by clock pulse timing following a first pulse. With $0° \leq \alpha \leq 110°$ pulse train are of 120° duration with each GPS ring counter terminating with pulses (3 turns off 1, 5, turns off 3, etc., for 1 GPG; 4 turns off 2, etc., for 2 GPG). The ramp is reset at α = 230° by the sync signal, and any trailing pulses remaining are terminated; therefore with $110° \leq \alpha \leq 180°$ pulse trains are shorter than 120°. Signal $\overline{GPS}$ must be a "1" to allow any pulses to occur.

The TGD amplifies pulses from the GPG. In systems where parallel thyristors are not employed (up to approximately 500 HP) the TGD shapes as well as amplifies pulses for thyristor gating, with pulses in the first 150usec of greater amplitude than remaining pulses. A logic "1" signal (ENF or ENR) is required for gating to be allowed and only one TGD in double converters can be operative at a time. Signal $\overline{INH}$ must be a "1" to allow pulsing. $\overline{INH}$ is delayed from GPS by 100 usec so that if GPS occurs during a first pulse, the first pulse and only this pulse will be allowed to proceed through the TGD to thyristors.

The M5B Gating System I.L. 16-800-289 includes description of operation for the VC & RL, GS, GPG, and TGD. It also includes functional schematics and illustrative waveforms. Please refer to that I.L. for more details of individual gating boards, as well as I.L. 16-800-241 and I. L. 16-800-242.

IV. Inner Voltage Loop - Double Converter

Each M5B system contains an inner voltage loop which consists of the:

1. Power Transformer (if used)
2. Thyristor Power Modulator (TPM)
3. Gating System
4. Voltage Sensor
5. Voltage Controller
6. Reversing Logic
7. DC Power Supply

The power transformer is used if necessary to convert the user's 3 phase voltage to a level required to produce the desired dc voltage from the TPM. For 500 volt dc systems this is 460 volts, 3 phase.

The TPM, Gating System & Reversing Logic were described previously.

The voltage sensor card is used to sense the dc bus voltage and to transduce it to a regulator signal for use in the basic regulator. A transistorized differential amplifier with excellent common-mode rejection is utilized in an op-amp manner. The output voltages are essentially independent of the bus potential to ground but reflect only the difference of the potentials at P and N. The input attenuator is adjusted to yeild output voltages of $\pm$9.6V for nominal bus voltage. For a detailed description as well as ratings and characteristics, refer to I.L. 16-800-247.

The power supply consists of the followning essential parts:

Rectifier transformer
Bridge rectifiers
Filter capacitors
$\pm$24V, +15V series regulator module

The transformer, diodes, filter capacitors, and fuses with a sub assembly pc board are used as a pre regulator s#1752A02 and is mounted on the magnetic panel. The transformer has a 115V ac primary and three isolated secondary windings. Twelve diodes used as three singal phase bridges are used with transformer secondary windings and filter capacitors to generate unregulated supplies of about 40V, 40V, and 25V. Fuses are used to protect transistors in the series regulators should there be a short circuit at their outputs.

The series regulator pc board has three identical circuits. The two 40V supplies are used with series regulators to generate $\pm$24V; the +25V supply with its series regulator is used to generate +15V. Adjustment pots are used to factory set the voltages at +24V, −24V, +15V and should not require adjustment in the field. Light emitting diodes are used. These LEDs will go out should its fuse blow.

The unregulated +25V supply is also used for gate power. The above power supplies are only sufficient to power boards located in the regulator cage. I.L. 16-800-244 describes the card in greater detail.

The voltage control portion of the card has been alluded to in earlier discussions of reversing of power flow. The actual controller portion of the card is shown in Figure X. With the voltage sensor calibrated to produce 9.6 volts at rated TPM voltage, a voltage of 10.0 volts on terminal 7 will cause the TPM to be 1.00 per unit. The time constant is approximately 3 milliseconds. The transfer function in block diagram form is:

$$\frac{\overline{V}_B}{\overline{V}_B^*} = \frac{}{1 + .003S}$$

The input on terminal 7 ($-V_B^*$) comes from the current controller whose output is limited to about 10.5 volts which indicates that the maximum bus voltage will be 5% greater than rated.

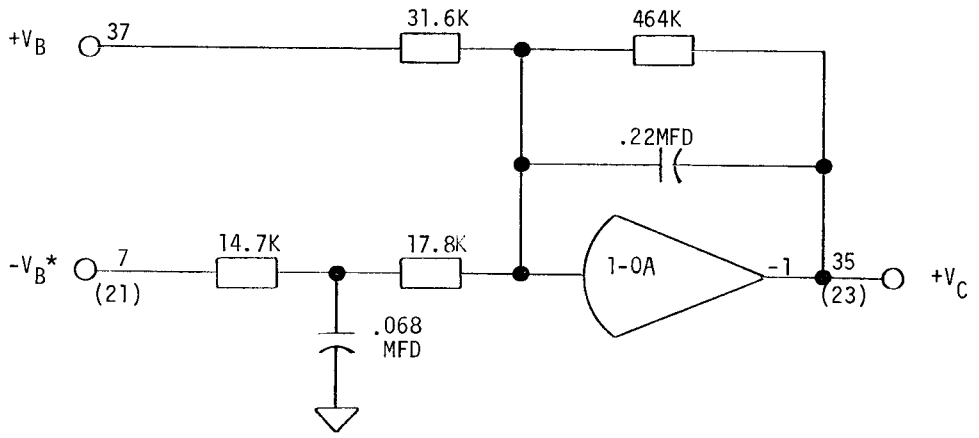


FIGURE X

V. Inner Voltage Loop - Single Converter

As in the dual converter system the single converter also has an inner voltage loop. This loop contains the same components as the dual converter except only 1 TPM and no reversing logic since there is only one converter to fire. Since there is no reversing logic the voltage controller and reversing logic card is omitted. The voltage control loop is physically located on the current controller. Its circuit is identical to that of Figure X which ends with terminal 35 as V_C. The terminal numbers in parentheses are those for the single converter. The voltage loop gain is the same as for the dual converter.

$$\overline{V}_B = \frac{\overline{V}_B^*}{1 + .003S}$$

Since on the single converter the VC & RL card is not used, the voltage controller is physically located on the current controller card and the back plane wiring is fixed, it is necessary to add jumpers 5J, 6J and 7J to provide circuit continuity. These jumpers are shown in Figure I.

VI. Current Loop

The current loop of the M5B system is composed of:

1. Current controller
2. Current sensor
3. Closed voltage loop
4. IR drop of the motor

The current sensor was discussed previously. With a double converter it was shown that the reversing logic reversed the current sensor output as well as the gating signal voltage for the double converter. With single converters the current feedback is the output of the current sensor. In either case the output of the current sensor is attenuated with pot 2P located on the pot card, such that at rated current the current feedback voltage is -2 volts or $-2\overline{I}_D$.

The dc motor with fixed field has the well known equations of:

$$V_T = K_V N + IR_a \quad (1+T_aS)$$

$$N = \frac{K_T I}{JS}$$

Where V_T = Terminal Volts
K_V = CEMF Constant, V/RPM
N = Speed in RPM
I = Armature Amperes
R_a = Armature Loop Resistance
T_a = Armature Loop Time Constant
K_T = Torque Constant, lb-ft/AMP
JS = Inertia, $WK^2/308$

These equations can be operated on to produce the block diagram of Figure XI.

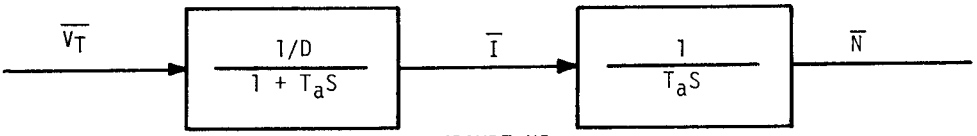


FIGURE XI

Where T_a is the time in seconds to reach rated speed at rated current and D is the per unit IR drop.

The current controller card contains the current controller, rate current limit ramp and means of current limit adjustments in steps by an external edge connector jumper. The current controller standard is style number 1745A21G02 for single converters and G04 for double converters. These provide for fixed current rate. On occasion a variable rate is used in which G01 or G03 are used. On G01 and G02 this board contains the single converter voltage controller for the inner voltage loop and reverse current simulation.

The simplified schematic for the card is shown in Figure XII.

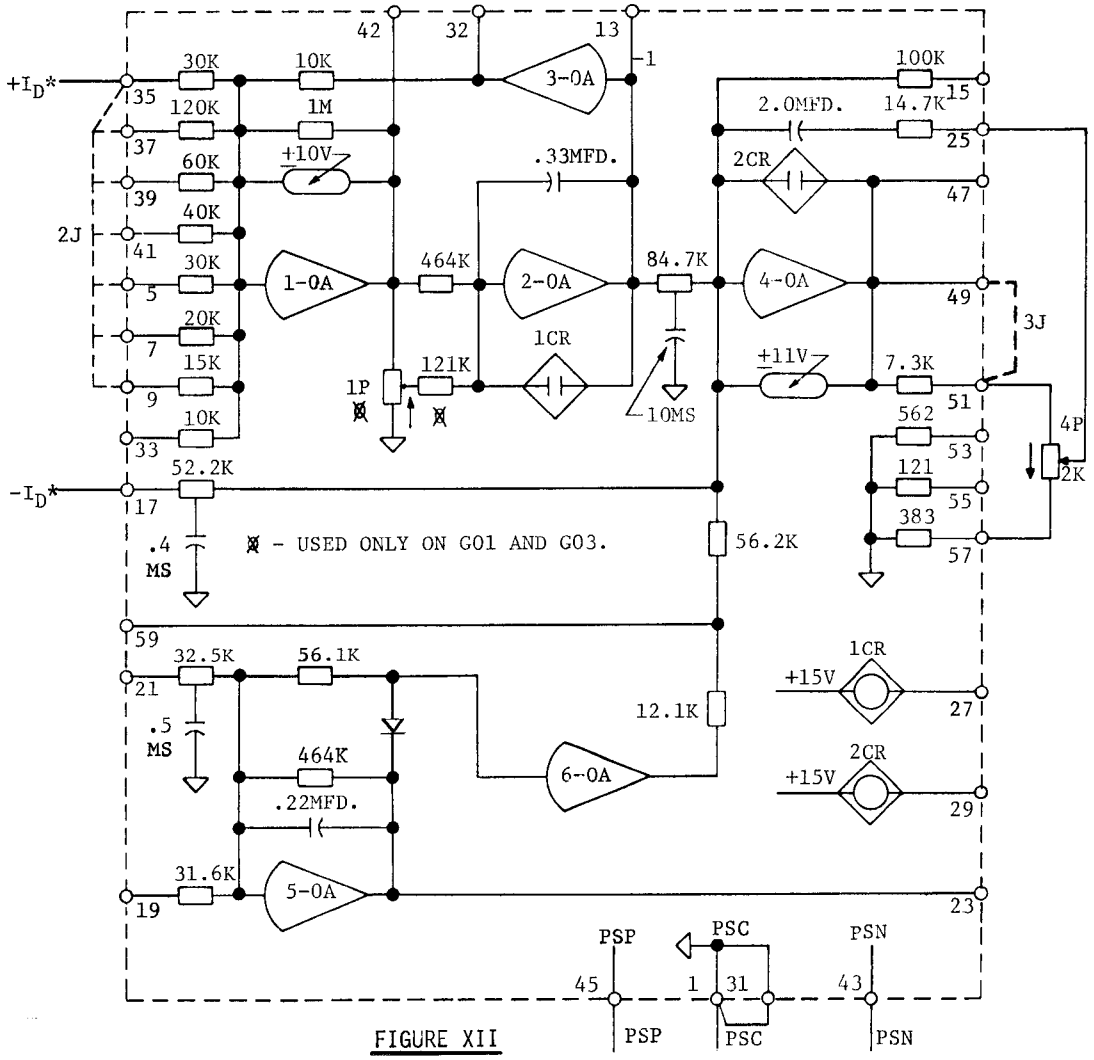


FIGURE XII

The current reference (+I_D*) comes into terminal 35. Current limit is determined with limit voltage from the SC or VRC and current limit jumper position. Unless reduced by external networks this limit voltage is ±10V accurate to within 2%. Reference +I_D* at terminal 35 only, gives a current limit of 100% rated motor (or drive) current. A jumper from terminal 35 to terminal 37, 39, 41, 5, 7, or 9 gives a current limit of 125%, 150%, 175%, 200%, 250% or 300% respectively.

The ramp or rate current limit is made up of op amps 1, 2 and 3 with associated circuitry. With a step reference change 1-0A goes to 10V. The capacitor on 2-0A will start to ramp and as 3.3V output on terminal 13 corresponds to 100% current reference the time required to change 100% current reference for G02 and G04 is:

$$T = \frac{3.3V \times .33 \text{ MFD} \times 464K}{10V} = .05 \text{ seconds}$$

Therefore the rate of change of current is:

$$\frac{100\%}{T} = \frac{100\%}{.05 \text{ sec.}} = 20 \text{ times rated current per second}$$

For G01 and G03 additional current is available into the ramp from 1P and 22R and the rate of change of current can be increased to a maximum of 97 times rated current per second. 3-0A provides feedback to 1-0A to match $+ I_{[D]}^*$.

A ramp for rate current limiting has some advantages over using a lead term in the current feedback, for speed controlled systems. The ramp requires no additional lead term in the SC to force the CC. This provides less high frequency gain for tachometer ripple and makes the ramp system less susceptible to sloppy current limiting caused by tachometer noise, ripple, etc.

4-0A and associated circuitry provides the current controller function. It is a PI controller with a fixed lead of 30ms to approximately cancel the armature time delay. 100% current reversals through the dead zone can be completed in about 40ms with about 7% overshoot. Current feedback $-I_D$ is brought in at terminal 17, and is adjusted to -2V at rated current by the current adjust pot (2P) on the pot board.

The block diagram of the current loop is shown in Figure XIII.

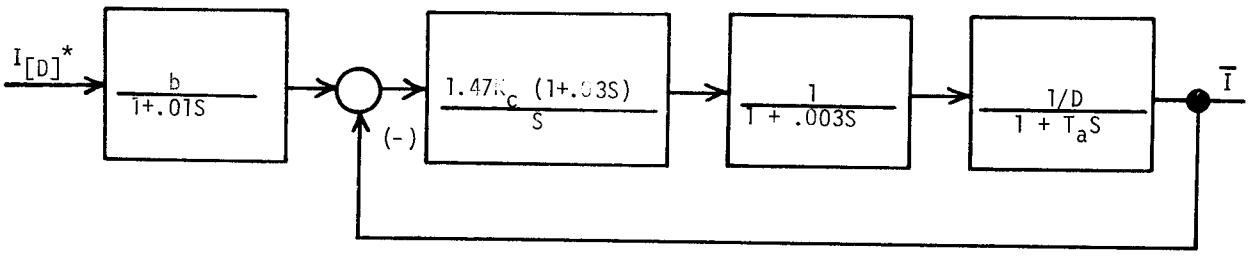


FIGURE XIII

Where b is defined as the per unit current limit setting of the drive and Kc is the current controller gain as set to give proper dynamic response.

Dynamic adjustment of the current loop is provided by 4P on the pot board and a jumper between terminal 51 and terminal 49, open, 53, or 55. Terminal 51 to 49 gives the least gain, next no jumper, next 51 to 53, and greatest gain is 51 to 55. With standard adjustment procedures, a crossover response of about 200 rad/sec is expected. The closed current loop transfer function is simply $\bar{I}/\bar{I}_D^* = \frac{b}{1 + .01S}$ in the steady state with a di/dt limit of 20 (or in the case of G01 or G03 a di/dt limit adjustable from 20 to 100).
A logic zero input at terminal 27 resets the ramp and effectively opens the reference. A logic one (+15V) at terminal 27 allows the ramp to operate. A zero at terminal 29 resets the current controller which is a zero voltage demand. The logic is firther discussed under Protection.

For single converters (G01 or G02 used) the voltage controller and reverse current simulation is provided on this board. Terminal 49 is tied to 21($-V_B^*$). When forward current and voltage is demanded, 5-0A and associated circuitry provide the same gain as the voltage controller in the double converter. Reverse current demand should be only a few percent of rated; just enough to be sure the drive is turned off. This however would make the current controller wind up to saturation without reverse current simulation. 6-0A and associated circuitry with 58R, 27D, 28D, and 60R reduces the gain of the voltage controller and provides a simulated feedback to the current controller when reverse current is demanded.

VII. Converter Sequencing and Protection

Figure XIV shows a single line diagram of a double converter armature supply. The ac voltage is brought from the customer feeder to an ac breaker, which depending on the short circuit capacity may be followed by current limiting ac fuses. This breaker is feeding the

gate control and regulating system as well as the thyristor transformer. It may therefore be located in the customer distribution center. This common supply without interlocking of the TPM and gate control is made possible by a design feature of the sequence and protection board (S&P) which eliminates any spurious pulsing during the ac turn on transient.

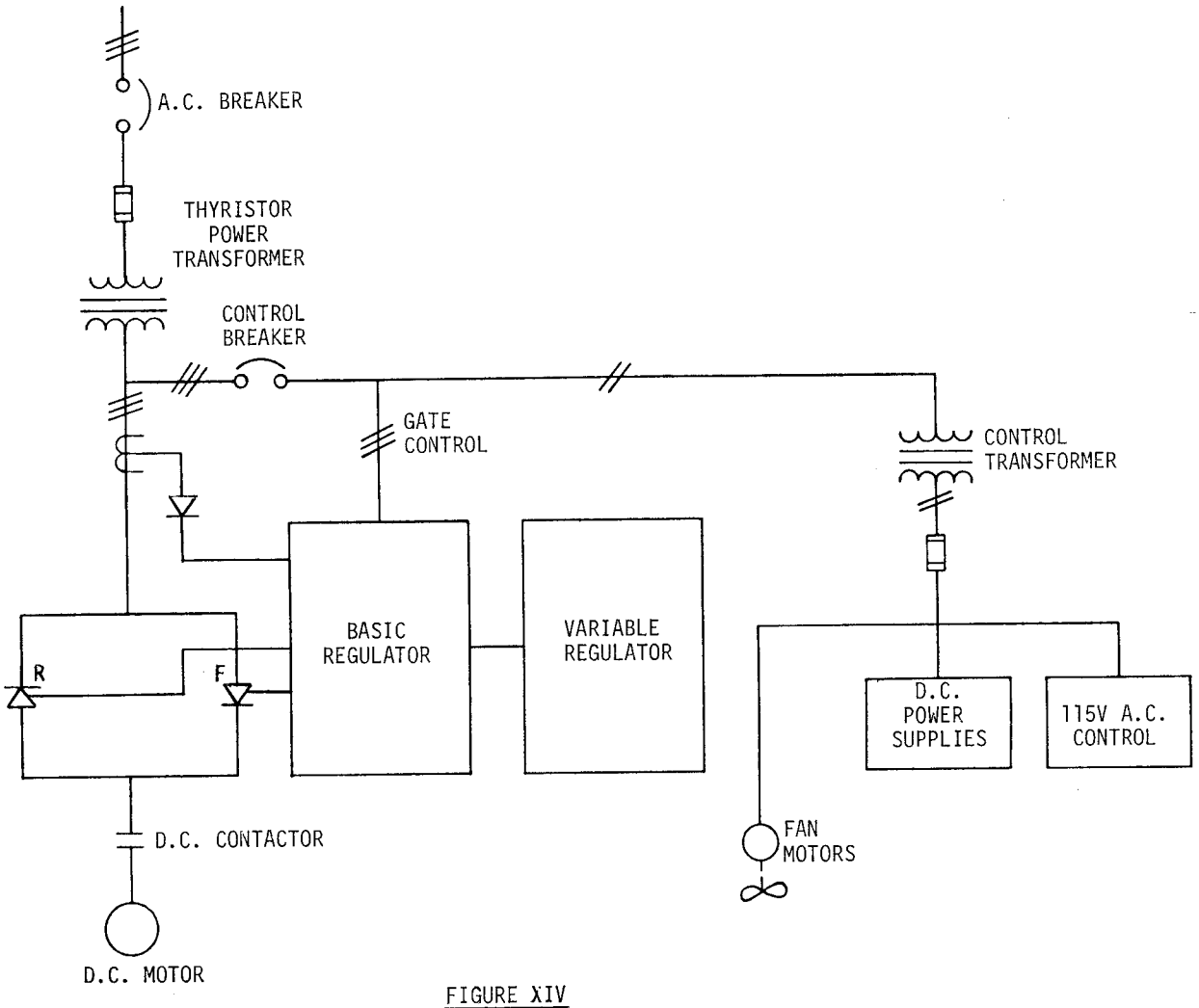


FIGURE XIV

The molded case ac breakers employed in M5B systems have magnetic trip only, set high enough that no tripping occurs due to the transformer inrush current.

The transformer secondary current is monitored with current transformers. These signals are rectified and this ac signal is sent to the regulator for current feedback, instantaneous overcurrent, and inverse time overload functions.

The main sequencing device is the dc contactor between the power converter and the dc motor armature. Its main function is to de-energize the motor positively in case of an emergency or if any work is required on the driven machinery. It is not providing electrical isolation of the armature. This is accomplished by tripping the ac breaker.

Internal regulator sequencing is all done with static logic elements located on the S&P card. External contacts required for sequence and protection such as main contactor auxiliary (Ma), zone A contacts (TPM thermo switch, thyristor circuit breaker auxiliary if class I protection is employed, etc.), contactor close and open pushbutton, etc., are brought through an input isolation board. These contacts have 115V ac for forcing voltage and are then coupled through optical isolators to generate logic "1" (+15V) and "0" (PSC) signals. All logic contacts and switches are designated with a diamond around the represented element. The PSR and MC switch is capable of picking up a relay as employed on M5B. The PSR relay is optional and its contact would likely be required in a line up of several drives to indicate all power supplies are ready for contactors to be closed. MC is the only relay (magnetic) required for basic sequencing and it of course is to pick up the dc contactor.

The Sequence and Protector card (RG/S&P/01) provides protection for the Thyristor Power Supply from various faults such as ac supply problems, regulator power supply problems, instantaneous and thermal overload as well as contactor failure. It also provides for the basic logic to open and close the line contactor under normal operating conditions and to open it under fault conditions. The simplified schematic diagram is shown in Figure XV.

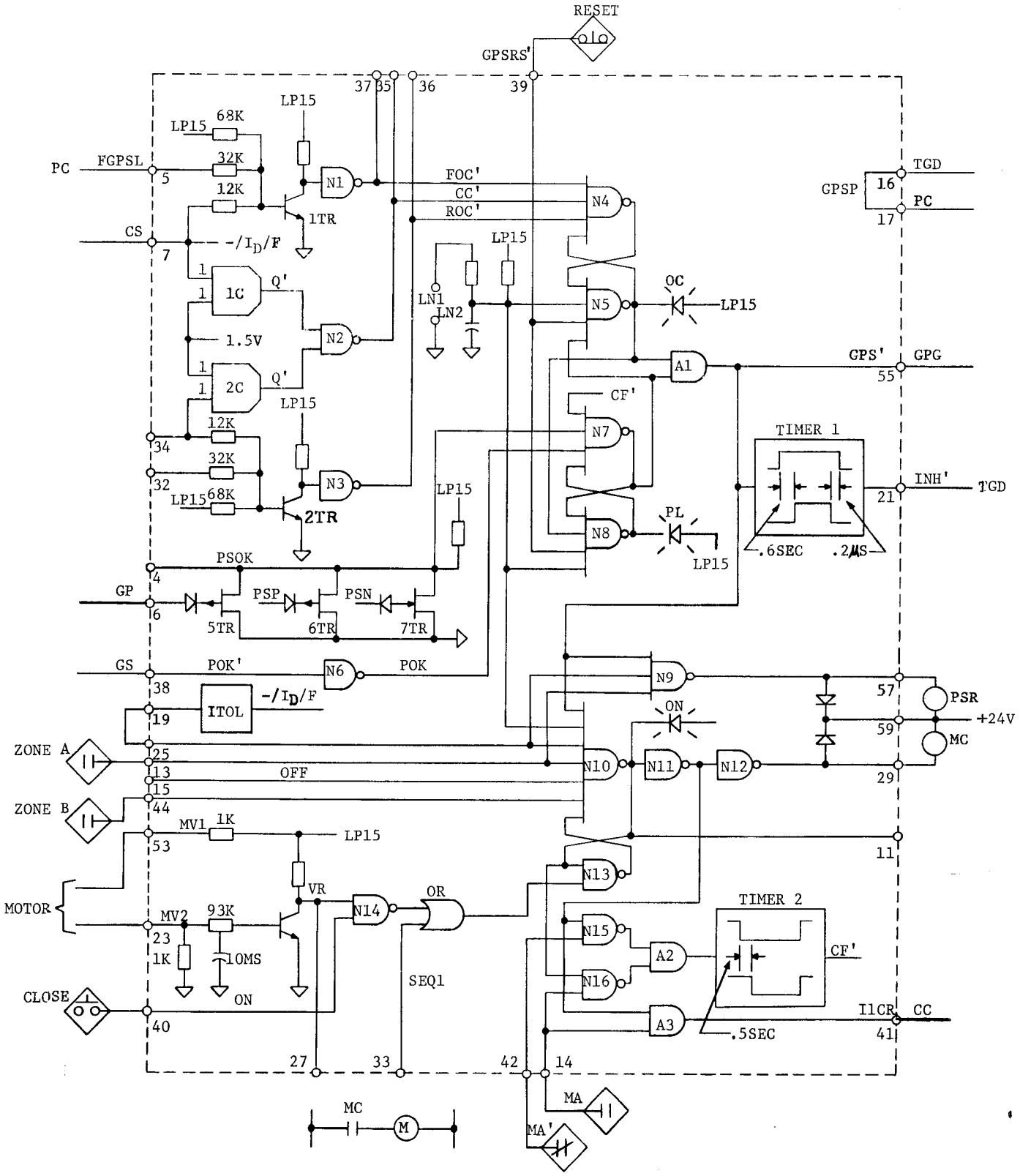


FIGURE XV

Instantaneous overcurrent protection, also defined as Gate Pulse Suppression or GPS, is provided by the circuits in the upper left corner of Figure XV. Consider first the circuitry associated with transistor 1TR and NAND 1. When the base of 1TR is greater than positive 565 millivolts 1TR is conducting so the input to NAND 1 is a logic "0". The output of NAND1 (FOC') is a logic "1" under this condition. Conversely when the base of 1TR is less than positive 565 millivolts 1TR is non-conducting causing its collector voltage to be near +15 volts so that the output of NAND 1 is logic "0". The base voltage of 1TR is determined by the net effect of 3 currents: 1) a positive bias from LP15, 2) an input voltage on terminal 7 from the current sensor which is negative 2 volts at rated current regardless of the direction of TPM current, and 3) a positive input current on terminal 5. The input on terminal 5 is fixed by dropping resistors located on the Pot Card. Located on this card is a series of resistors with one end connected to LP15 as shown in Figure XVI. The value of resistance is selected by jumper 1J on the card to stab type terminals marked in percent.

The value of voltage on terminal 7 for which the base, of 1TR will be less than 565 millivolts and therefore FOC' will be a logic "0" is found from the formula:

$$V_7 = -(246 + 2.07R) / (31.6 + R)$$

There R is the value (in Kohms) of the resistor selected by 1J on the Pot Card. Since V_7 is equal to $-2|\bar{I}|$ where $\bar{I}$ is the per unit TPM current, the values for $\bar{I}$ can be determined for each jumper position. The following table lists the per unit currents at which GPS will occur and, as a reference, the corresponding values of current limit which are set as an integral part of the current loop.

1J POSITION	R	$\lvert\bar{I}\rvert$ GPS	$\lvert\bar{I}\rvert$ CL
open		1.00	
125%	383K	1.25	1.00
150%	147K	1.50	1.25
185%	74.9K	1.85	1.50
215%	46.4K	2.15	1.75
245%	31.6K	2.45	2.00
310%	12.1K	3.10	2.50
370%	2.15K	3.70	3.00

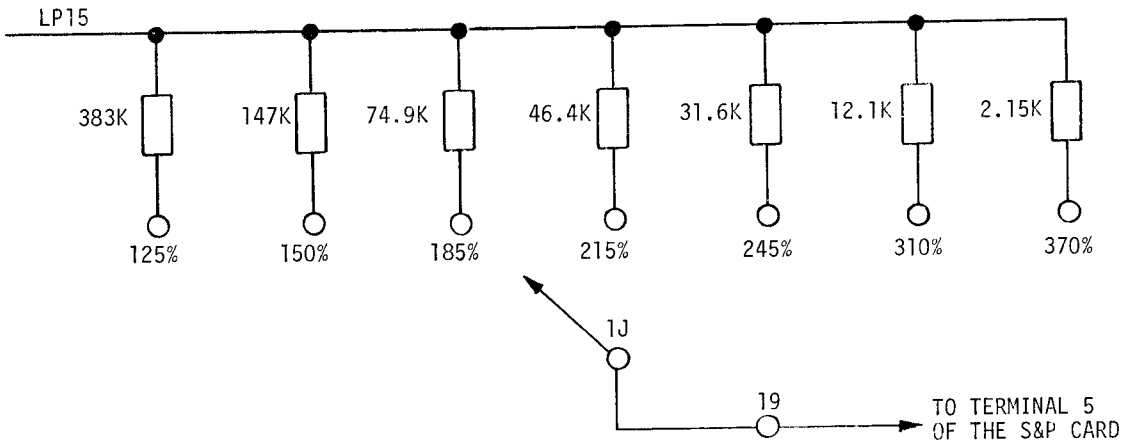


FIGURE XVI

Note that the jumper position marking is actually the percent overcurrent where GPS occurs and that GPS is 125% of the current limit value. In dual converters the GPS value for reverse is the same as forward since the absolute value of current is used. In summary FOC' is a logic "1" when the per unit current is less than the Pot Card jumper setting and a logic "0" as is described later.

As just stated terminal 7 is normally connected to the current sensor and is $-2|\overline{I}|_F$ or really $-2|\overline{I}|$ since no distinction is made between forward and reverse. In some situations where a distinction must be made terminal 7 is connected to a forward only current sensor so its output is $-2\overline{I}_F$ when the forward TPM is conducting and 0 when it is not. A reverse current sensor whose output is $-2\overline{I}_R$ when the reverse TPM is conducting and 0 when it is not is connected to terminal 34 of the S&P card. Terminal 34 is the input to a circuit identical to the forward GPS detection circuit described except its logic output is ROC'. A separate set of resistor selected by 2J is located on the Pot Card and the circuit operates in the same manner as the forward GPS circuit, i.e., ROC' is a logic "0" for any values above this setting. The effect of the logic transition is to be seen later.

In most static power supply systems the gating circuitry prevents turning on the forward and reverse converters at the same time which would produce circulating currents. In some special systems such as cycloconverters or high response servo positioning systems, it is necessary to provide low circulating currents to assure no deadband when switching from one converter to another. As long as the amount of circulating current is low no problem exists but if a gating malfunction should occur it is necessary to detect when the circulating current exceeds a predetermined value. This detection is also accomplished on the S & P card. The forward and reverse currents on terminals 7 and 34 are fed to individual biased comparators (1C and 2C of Figure XV).

The comparator outputs are logic "1" if their input current is greater than 0.43 per unit. The comparator outputs are in the inputs to NAND 2. Only when both comparator outputs are logic "1" (which indicates that both forward and reverse currents are greater than 0.43 per unit) will the output of NAND 2 be a logic "0". The output of NAND 2 is designated CC. As before,the effect of the logic transition is discussed later.

The ROC' and CC logic functions always exist but if there is no reverse current sensor, terminal 34 is open so ROC' and CC' are always logic "1" and can never switch to the "0" state.

As previously stated protection against both ac and dc power supply malfunctions are required and detected by the S & P card. The regulator dc power supply faults are detected by field effect transistors 5, 6 and 7TR. All of these transistors are connected between PSC and the PSOK bus which is terminal 4 of the S&P card. If none of the transistors is conducting the PSOK bus is positive 15 volts or logic "1" due to its bias. If any of these transistors should conduct the PSOK line is connected to PSC or becomes a logic "0". Transistors 6 and 7 TR conduct only if the PSP or PSN regulated 24 volt supplies are abnormal. Transistor 5TR conducts if terminal 6 is not positive 24 volts. If gate power is supplied by a voltage other than PSP this is denoted by GP and connected to terminal 6. In small systems where GP does not exist, terminal 6 is connected to PSP and 5TR functions the same as 6TR. If any of these power supplies should fail PSOK changes from logic "1" to "0". Its effect is described later. Note that no protection for LP15 is provided since LP15 is the logic power and is required for any logic to function. The system is self-protecting however, since without LP15 the gates cannot function.

On the gate synchronizer card are the fault detection circuits which detect ac power supply faults. The faults detected are gating oscillator failure, single phasing of the ac line, incorrect phase sequence of the ac line and undervoltage of the ac line. These faults are summed on the synchronizer card into a single logic element whose output is logic "0" when none of the mentioned faults are present and logic "1" if any one or more faults exist. This logic signal is designated POK' and is connected to terminal 38 of the S&P card where it is applied to NAND 6 whose output is defined as POK. Like previous circuits it is logic "1" on no fault and logic "0" if a fault exists.

Another possible malfunction is contactor failure or failure to close when it should or failure to open when it should. The circuits which detect this failure are described later under contactor operation. For the protection feature assume a signal CF' exists which is logic "1" with no failure and logic "0" if there is a failure.

Several possible faults have thus been detected and all have been converted to digital logic signals which are logic "1" under no-fault conditions and go to logic "0" if a fault occurs. For any of these faults operation of the power supply system should be inhibited or stopped if operating. If a fault occurs and gating is stopped the fault may disappear such as in gate pulse suppression, The system should not lose the information but retain it for the trouble shooting personnel. The next few paragraphs describe how the transition of a fault signal from "1" to "0" inhibits or shuts down the system in an orderly fashion and provides for reset. The shutdown logic is comprised of NANDs 4, 5, 7, 8 and AND 1. When no fault is present FOC', CC', ROC', PSOK, POK and CF' are at the logic "1" state. The RESET button is connected to terminal 39 through an input card and its signal (GPSRS') is logic "1" when the button is not depressed and "0" when it is depressed. NANDs 4 and 5 are connected as a flip-flop as are NANDs 7 and 8. These flip-flops must be initialized upon initial

application of power which is accomplished by a resistor-capacitor combination. When power is first applied the capacitor is not charged so one input to NANDs 5 and 8 is a logic "0." As the capacitor charges its voltage builds up to LP15 or a logic "1". The time constant of this circuit is 250 milliseconds. This initial "0" forces the outputs on NANDs 5 and 8 to be logic "1". The overcurrent (OC) and power loss (PL) light emmiting diodes (LEDs) are turned off. The inputs to NAND 4 are all logic "1" so its output is "0" which holds NAND 5 at "1" when the power on circuit has timed to logic "1". In the same manner NAND 8 is held at logic "1". With NANDs 5 and 8 at "1" so is AND 1 and TIMER 1. The output of AND 1 is defined as GPS which is fed into the Gate Pulse Generator cards which when logic "1" allows generation of gate pulses. The output of TIMER 1 is defined as INH' and is applied to the Thyristor Gate Driver and when logic "1" allows any gating pulses from the gate generators to be applied to the thyristors. Note that GPS' comes on at the logic "1" state instantly but INH' does not become a "1" for 600 milliseconds after GPS. This insures that the gate generators are fully stabilized before allowing any gate pulses to the thyristors. Likewise when GPS' goes to logic "0" the INH' signal does not go to "0" for 200 milliseconds which allows any TGD hard pulses to go through to fully turn on a power thyristor to carry the fault current. The gating system is described in IL 16-800-289, the Gate Pulse Generator in IL 16-800-242 and the Thyristor Gate Driver in IL 16-800-241.

On any type of instantaneous overcurrent one or more of the overcurrent signals (FOC', CC' or ROC') will change from "1" to "0" which forces NAND 4 to logic "1". As long as all the other inputs to NAND 5 are logic "1" its output will go to "0". This "0" turns on the OC light denoting an overcurrent fault and causes 1 to also go to "0" which stops gating. With NAND 5 at "0" NAND 4 will remain at "1" even if the fault disappears (which it will because the thyristors are turned off). This insures that the type of fault is remembered allowing the trouble shooter to recognize what type of fault caused gate pulse suppression.

Likewise, any type of power supply malfunction (PSOK, POK, or CF') will cause at least one input to NAND 7 to be "0" and will force NAND 7 output to logic "1". As long as all other inputs to NAND 8 are also "1" its output will be "0" which will turn on the PL light and cause gate pulse suppression since AND 1 goes to "0". As in the overcurrent fault, the flip-flop retains the fault indication even of the fault disappears.

Note that the two LEDs indicate the general type of fault as power loss on overcurrent but not the specific fault. The optional Fault Indicator does indicate the particular fault saving trouble shooting time. This card is described in another section.

Also note that the cross connection of NANDs 5 and 8 provide annunciation on a first come - first served basis. As soon as one fault occurs it blocks the other light so that if one fault should cause the other only the first fault light is turned on.

Two methods are available to reset the flip-flop aside from removing and reapplying power. The primary method is the RESET button which when depressed causes GPSRS to go to logic "0" which forces both NANDs 5 and 8 to "1" which reset GPS and turns on the LEDs. If the fault still exists NAND 4 or NAND 7 will stay at "1" and will not allow NANDs 5 and 8 to remain at "1" when the button is released. Reset can only be completed when the fault is corrected. The other method is to momentarily connect the two lance terminals on the S&P card marked LN1 and LN2 together. This shorts the power on timing capacitor and resets NANDS 5 and 8 which will stay for the power on time of 250 milliseconds even if the fault persists. As before, reset in this manner cannot be completed until the fault is corrected.

Another fault that should cause a shutdown but not necessarily a gate pulse suppression is a power supply thermal overload. First it is necessary to detect such a condition and convert it into a digital logic signal. The circuitry that accomplishes this is shown in Figure XVIIA. The S&P card has two style numbers which cause the resistances in these circuits to change for different ranges of overload protection. The normal style is 1745A38G01 and the other is 1745A38G03. The resistor values for G03 are shown in paretheses in Figure XVIIA. The input to the circuit is the output of the current sensor which as previously mentioned is -2 volts at rated current either motoring or regenerating or $-2|\overline{I}|$. The circuit consists of 3 main parts, the first being a biased integrator whose output is limited to all positive values and up to 0.5 volts negative. The positive bias assures that the integrator does not begin to integrate or ramp until the input from the current sensor is more negative than -2.3 volts or since this is $-2\ |\overline{I}|$ is greater than $1.15|\overline{I}|$. The second portion of the circuit is a unity gain inverting amplifier with a time delay of 470 milliseconds. The third component is a operational amplifier with no feedback impedance other than a diode which will allow all positive value outputs but limits negative outputs to -0.5 volts.

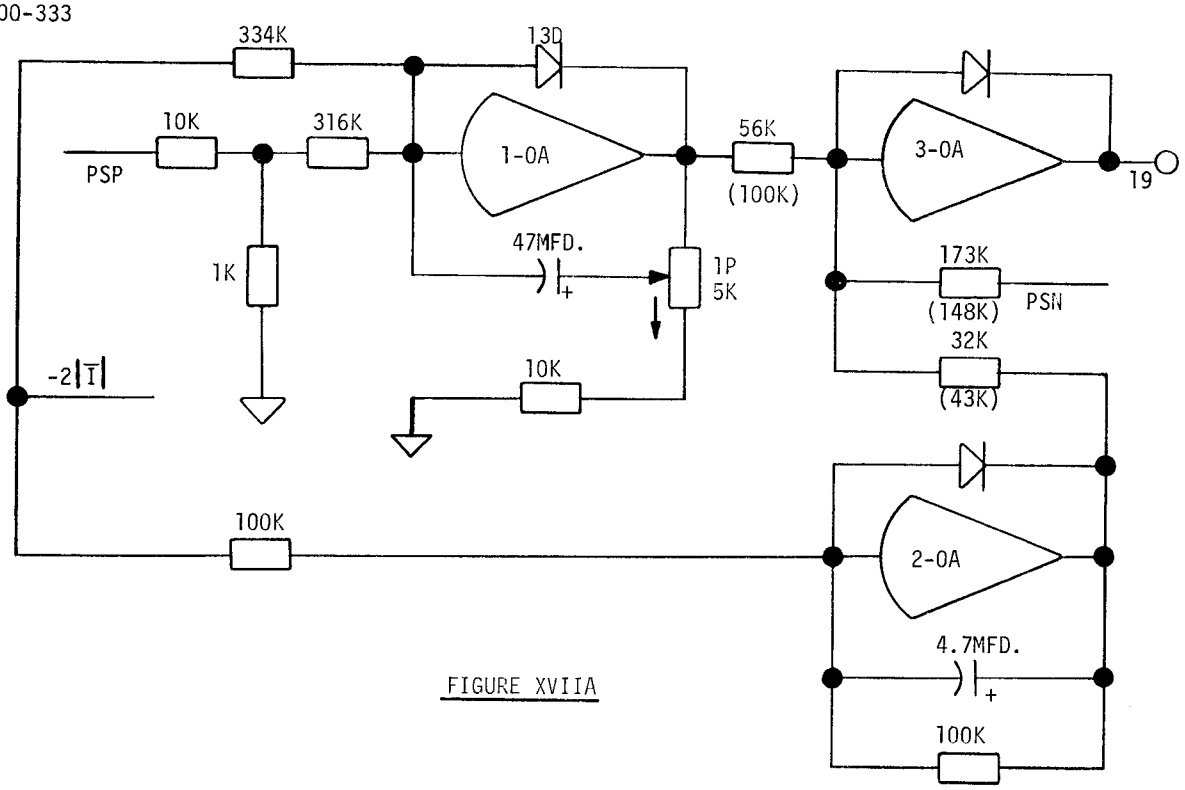


FIGURE XVIIA

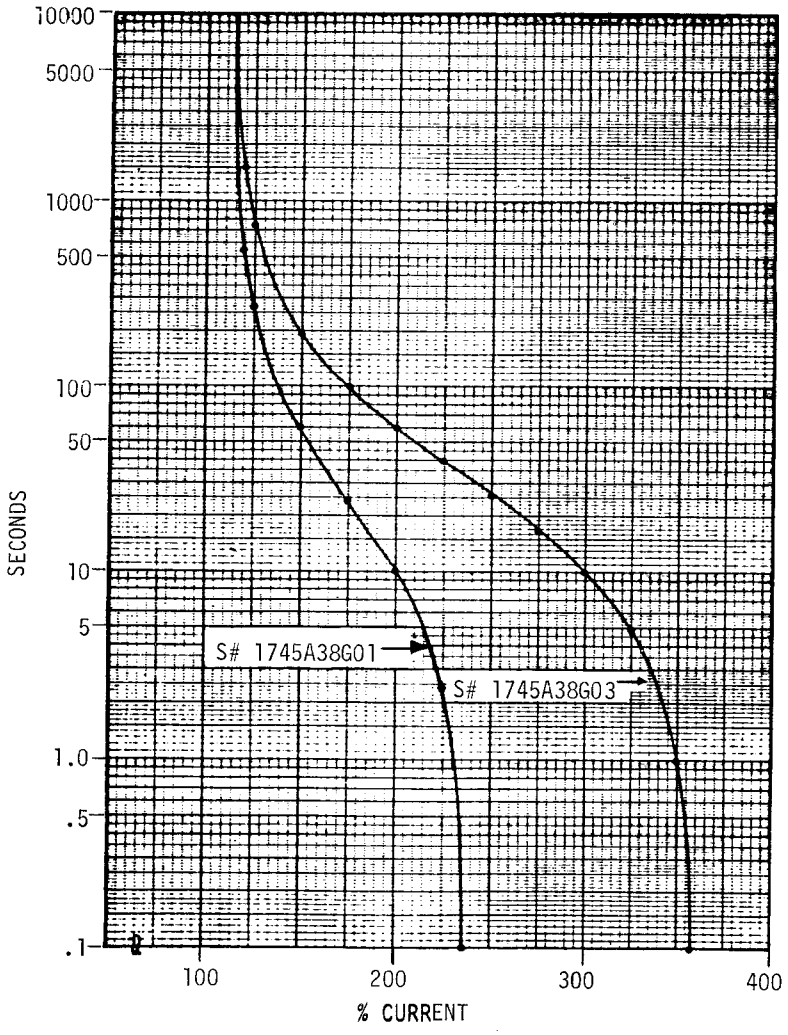


FIGURE XVIIB

When the net input to 3-OA is positive its output is -0.5 volts or logic "0", however, when the net input is negative the output, which is terminal 19 is high positive or a logic "1". The inputs to 3-OA are the integrator and inverter outputs and a negative bias. With currents less than $\pm$1.15 per unit, the net input is negative due to the bias so the output on terminal 19, which is also defined as OL', is a logic "1." For currents greater than $\pm$1.15 per unit the time for OL' to switch from logic "1" to "0" is given by the following equations (pot 1P is factory set and should not be adjusted in the field.)

$$T = 24.05\ (2.36 - \overline{I})\ /\ (\overline{I} - 1.15) \text{ for G01}$$

$$T = 32.16\ (3.58 - \overline{I})\ /\ (\overline{I} - 1.15) \text{ for G03}$$

These curves are plotted in Figure XVIIB which shows that for G01 the trip time at 150% current is 60 seconds or 10 seconds for 200% current. For G03 the times are 200% in 60 seconds and 300% in 10 seconds.

The overload logic signal can be used for indication only by monitoring terminal 19 or for shutdown by connecting it to terminal 25 which is an input to NANDs 9 and 10. If the circuit is left open terminal 25 is by definition a logic "1" which indicates no overload so regardless of what terminal 19 does, not shutdown is initiated.

Two other sets of interlocks are provided which will cause shutdown or prevent starting but do not cause gate suppression. One set is defined as Zone A interlocks which are protective interlocks which are normally under an electrician's control such as circuit breakers, transformer or TPM thermal control switches, motor field loss, auxiliarry motor starters, magnetic overloads, etc. The other set is defined as Zone B interlocks which are generally under operator control such as lubricating pumps, limit switches, proximity switches, remote contactor open-close permissive circuits, etc. All Zone A interlocks are connected in series externally and applied to the S&P card through an Input Card. When all Zone A interlocks are closed the Zone A logic signal is "1". Zone B interlocks are also a lumped signal through another input circuit. The Zone B logic signal is also "1" when all interlocks are closed. The state of Zone A or Zone B can easily be determined by the Zone A or Zone B LED on the Input Card.

NAND 9 has three inputs, Zone A, OL' and GPS' which when all are logic "1" will cause its output to be logic "0" and causes relay PSR (Power Supply Ready) to be energized. PSR is an interface with external devices and also turns on the Power Supply Ready light to inform the electrician that if a problem exists it is not in Zone A interlocking or protective circuits but rather in Zone B. PSR has extra interlocks which are often used to interlock Zone B of various sections of a process line control together.

The remainder of the S & P card is devoted to line contactor opening and closing. Part of this control consists of a static voltage sensing relay which senses motor terminal voltage. It provides a digital output (VR) isolated from the power circuits by an optical coupler which is "1" when the terminal voltage is within $\pm$25 volts of zero and logic "0" for all other values of armature voltage. The actual opening and closing of the contactor is under the control of the flip-flop consisting of NANDs 10 and 13. When NAND 10 is a logic "1", NAND 11 is "0" and NAND 12 is "1" causing relay MC to be denergized. If NAND 10 is "0" relay MC is energized. Contacts of MC close in the contactor coil circuit to pick up the contactor M. An interlock of M is converted into logic signals MA and MA' through one input circuit on an Input Card. MA is logic "1" with the contactor closed. A LED marked ON is located on the S&P card which shows the logic state of NAND 10 and is lit when the contactor is told to close.

The S&P card can be used with a separate sequence card to operate the contactor in which terminals 15 (OFF) and 33 (SEQ 1) are the interconnections. These signals are not necessary to basic operation of the contactor and for the following discussion are assumed to be logic "1" (either true logic "1" or open circuit which by definition is "1"). In order for the contactor to close all inputs to NAND 10 must be logic "1". These inputs are GPS', OL' Zone A, Zone B, OFF, the power on timer, and the output of NAND 13. With no faults and all protective interlocking correct the power on timer forces NAND 10 to "1" which is also one input to NAND 13. The CLOSE button applied through an Input Card is logic "0". This "0" holds NAND 10 in the "1" state when the power on timer goes to "1". The contactor is then open and the ON LED is dark.

To close the contactor NAND 13 must go to "1" or one of its 2 inputs must go to "0", The OR output will go to "0" when NAND 14 goes to "0" which can only occur when both of its inputs are logic "1". This will happen if VR is "1" and the CLOSE pushbutton is depressed. When NAND 10 goes to "0", NAND 13 is locked at "1" regardless of what happens to the CLOSE button, VR or the OR.

The only way to open the contactor is for NAND 10 to become logic "1" which means that at least one of its inputs must go the "0". These inputs are as stated GPS', OL' Zone A, Zone B, OFF, power on timer and NAND 13. NAND 13 is and stays at "1" as does the power on timer. Therefore, if there is gate pulse suppression, opening of an interlock in Zones A or B or if the OFF input goes to "0" the contactor will open.

When the auxilliary card is not used OFF, is logic "1" as previously stated and except for fault or interlocking failures Zone B is used to open the contactor. With the auxiliarry card used, the contactor is closed by causing SEQ 1 to go to "0" which forces OR to "0" and NAND 13 to logic "1". To open the contactor the OFF signal goes to "0".

The contactor failure signal, CF', was mentioned earlier where it was assumed that it was logic "1" unless there was a failure when it went to "0" at which time it causes a shutdown by a power loss gate pulse suppression. The failure detection circuit consists of NANDS 15 and 16, AND 2 and TIMER 2. With NAND 10 at logic "1" the contactor should not be closed so MA should be "0" and MA' should be a "1". NAND 11 will be "0" so NAND 15 should be "1". NAND 16 should also be "1" and AND 2 should be "1". The timer is non-inverting so its output, CF' should be "1". If the contactor is closed under these conditions NAND 16 will be "0" as will AND 2 and TIMER 2 or CF' which is a failure. When NAND 10 goes to "0" which should cause the contactor to close, NAND 15 goes to logic "0" as does AND 2. The timer starts to time and if the contactor does not close within 500 milliseconds CF' goes to logic "0" and causes gate pulse suppression. If M does close within the allowed 1/2 second NAND 15 goes back to "1" due to MA' and the timer is reset and CF' stays at "1".

If the contactor is closed and NAND 10 goes to logic "1" which should cause the contactor to open NAND 16 goes immediately to "0" as does AND 2 and the timer starts to time. If the contactor does not open within 500 milliseconds, CF' goes to "0" and causes GPS. If M does open within the allowed 1/2 second NAND 16 goes back to "1" due to MA and the timer is reset causing CF' to remain at "1".

AND 3 controls the reset of the current controller. When its output on terminal 41 which is defined as I1CR is logic "0" the current loop reference is zero or the TPM is regulated to zero current. When I1CR is logic "1" the current is regulated to its reference value. From Figure XV it is seen that I1CR is logic "1" only when the contactor is supposed to be closed (NAND 11) and when it is actually closed (MA). Before the contactor is closed then it is "0" and when the contactor is told to close (NAND 11 goes to "1") nothing changes but when M has actually closed, as signaled by MA, it goes to "1" and the current is regulated to the desired value. This insures that the contactor does not close while the open circuited TPM is trying to regulate current which would be maximum TPM voltage. When the contactor is closed and current is being regulated normally, if the contactor is told to open (NAND 11) goes to "0" and I1CR goes immediately to "0" and the TPM is regulated to zero current before the contactor drops out. This insures that the contactor never opens under load unless its coil fails. The actual current controller is discussed elsewhere.

Terminals 16 and 17 of the S & P card are connected internally on the card. External to the card is a connection which runs from PSC through a similar circuit on the Pot Card to the TGD Cards. When all cards are plugged in the PSC or logic "0" appears at the TGD which enables gating. If either card is unplugged the circuit is open or a logic "1" which inhibits gating (see IL 16-800-241). This prevents running with no fault protection.

Figure XVIII is a very simplified relay equivalent schematic to aid in following the static logic previously described.

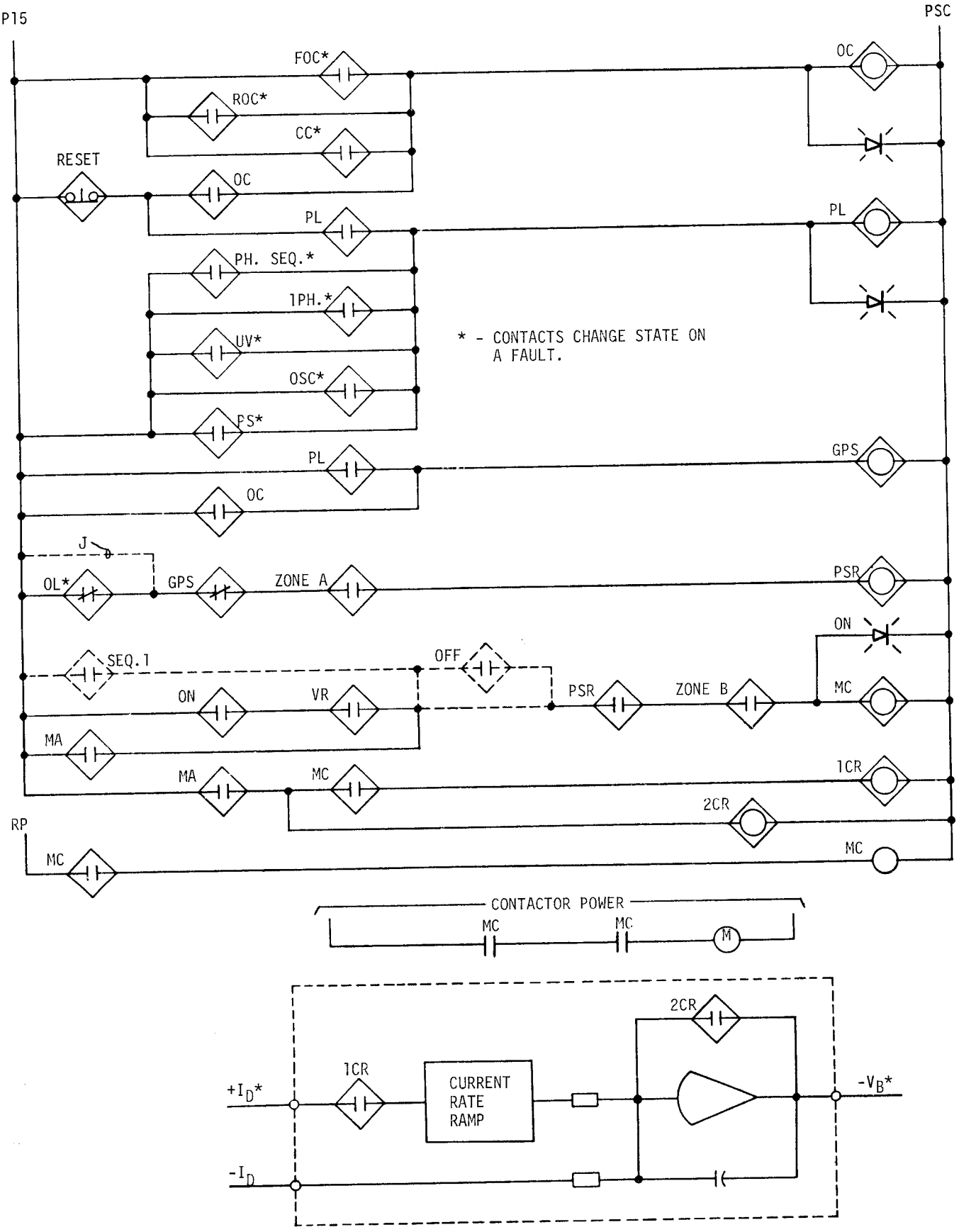


FIGURE XVIII

VIII. Fault Indicator

The Fault Indicator card, S#1745A44G01, is an optional card which can be used to pin point several different points in the logic system. The NANDs are numbered in Figure XIX for ease in description. They are not so numbered on the card itself. The specific faults are annunciated by light emitting diodes (LEDs) on the front of the card. The Fault Indicator amplifies the standard available fault indication available elsewhere. For example, on the Sequence and Protector card previously discussed the power loss LED indicates a fault of:

a. Power supply.
b. Single phasing of ac input line.
c. Incorrect phase sequence of ac input line.
d. Undervoltage of the ac input line.

This is done with one LED and although it can be determined that one of these faults occurred and shut down the system, it does not indicate which of the four faults occurred. The Fault Indicator does identify the specific fault and if more than one fault occurred, which came first.

The indicating LEDs 1 through 10 are driven by multiple input NANDs (3, 6, 10, 14, 18, 22, 26, 30, 34, 38) and will be turned on when the NAND output is a logic "0". For the NAND output to be a logic "0" all of its inputs must be logic "1". All of these driver NANDs have two common inputs (as well as at least one other input). These inputs are marked RESET 1 and RESET 2. RESET 1 is tied to LP15 through a 15K ohm resistor which would normally cause RESET 1 to be a logic "1" to enable all the driver NANDs, however the line can be forced to logic "0" in two ways: 1) by operating the small toggle switch on the front edge of the card, or 2) by pushing the gate pulse suppression reset pushbutton which through an Input Card forces signal GPSRS' to logic "0" from its normal logic "1" state. With RESET 1 at logic "0" all driver NANDs have a logic "1" output and all LEDs are turned off.

RESET 2 is provided to initially insure that all LEDs are turned off. RESET 2 is tied to LP15 through a 47K ohm resistor and to PSC through a 2.2 MFD capacitor. When power is first turned on and the NAND power is applied, the LEDs might turn on which would (as will be shown later) lock them on but RESET 2 builds up exponentially to logic "1" from its initial logic "0" state due to the time constant of the 2.2 MFD capacitor. Therefore, all driver NANDs have an initial logic "0" ramping to logic "1" which holds all NANDs at "1" until initialized. With both RESET lines at logic "1" the driver NANDs will be enabled and can be controlled by their other inputs.

LED 1 indicates operation of the voltage ready signal VR which is a logic "1" when the TPM is less than 25 volts and logic "0" above this point. With terminal 39 connected to PSC, NAND 1 is held at 1. NAND 2 is a logic "0" with low TPM voltage which keeps at least one input to NAND 3 at logic "0" and LED 1 is off.

When the TPM voltage is greater than 25 volts, VR is logic "0", NAND 2 is logic "1" making all inputs to NAND 3 logic "1" so NAND 3 is logic "0" and LED 1 is turned on. NAND 39 and NAND 40 are logic "1" and "0" respectively. LED 1 then follows the TPM voltage being off with low voltage and turned on with high voltage.

LED 2 indicates when the pot card and protection cards are plugged in. It is necessary that the pot card be plugged in since without it there is no current feedback, gate pulse suppression level is zero, and other protective features are inoperable. Terminal 9 is open which by definition is logic "1" therefore NAND 5 is logic "0" and keeps NAND 4 at logic "1". The signal on terminal 35 is zero volts if both the pot card and the sequence and protector card are plugged in by virtue of the fact that GPSSP (terminal 35) is connected through terminals 16 and 17 of the S & P card and terminals 17 and 47 of the pot card to PSC. As long as both cards are plugged in this connection is not broken and GPSSP is logic "0" so driver NAND 6 is logic "1" and LED 2 is turned off. If either card is not inserted correctly the PSC connection is broken which by definition is logic "1" and now with all inputs to NAND 6 at logic "1" LED 2 is turned on. NANDs 39 and 40 are logic "1" and "0" respectively. Termianl 32 is then logic "0" if either LED 1 or LED 2 is on and can be used for other purposes if desired.

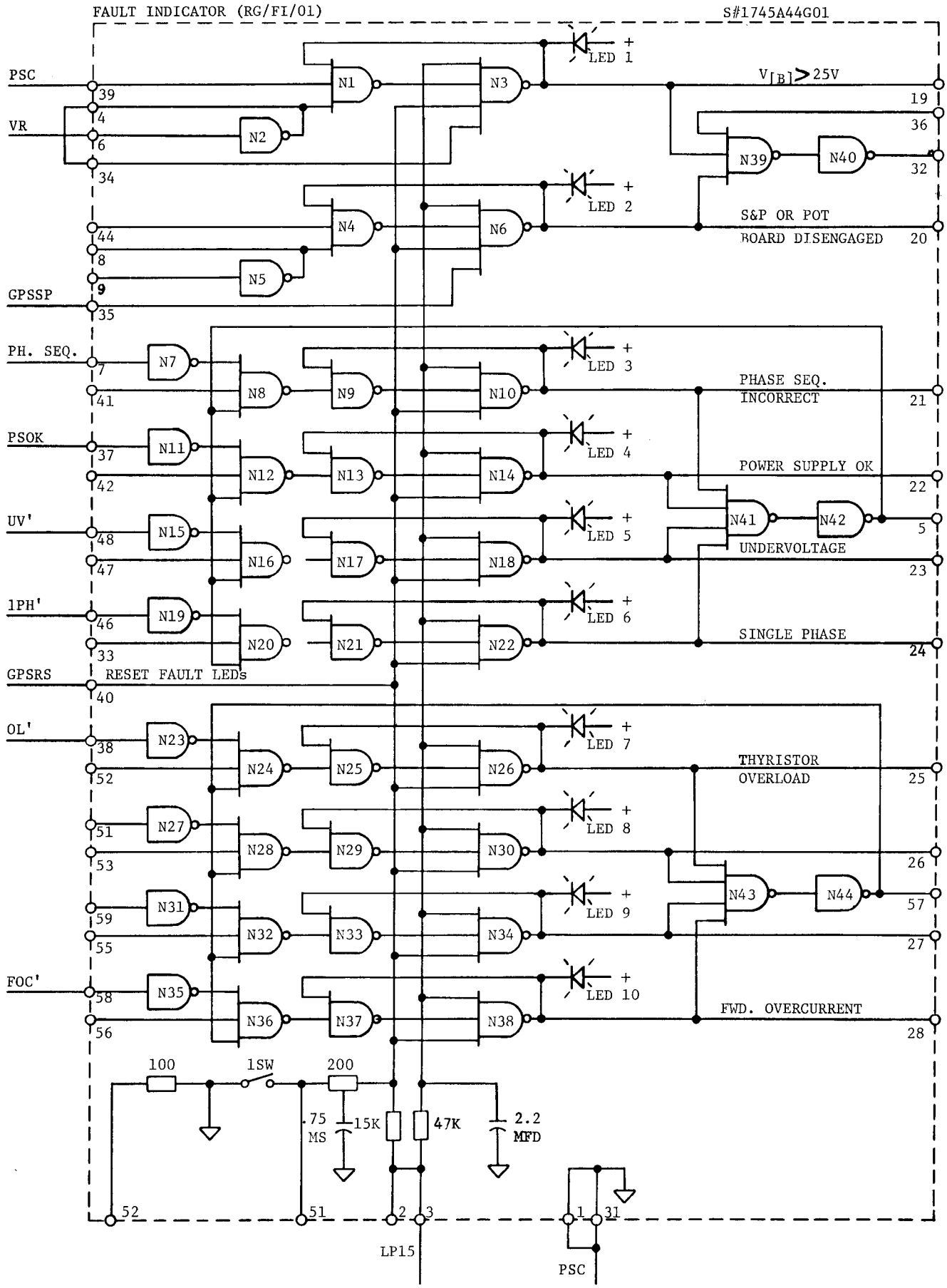


FIGURE XIX

LEDs 3, 4, 5 and 6 operate as a group to indicate loss of phase sequence of the input line, regulator power supply, undervoltage and single phasing of the input line respectively. Initially RESET 2 made all inputs to NAND 41 a logic "1" so NAND 42 and at least one input to NANDs 8, 12, 16 and 20 are also at logic "1". With none of the previously listed faults occurring all their inputs are at logic "1" so the outputs on NANDs 7, 11, 15 and 19 are logic "0" keeping NANDs 8, 12, 16 and 20 at logic "1". Note that each of NANDs 8, 12, 16 and 20 have another input terminal which is open circuited and thus always logic "1". Since all LEDs are off both inputs to NANDs 9, 13, 17 and 21 are logic "1" keeping NANDs 10, 14, 18 and 22 at logic "1" or LEDs off. Assume one of the 4 possible faults occurs and its signal goes to logic "0". Its input NAND (7 or 11 or 15 or 19) will go to logic "1" and cause the corresponding NAND (8, or 12 or 16 or 20) to be a logic "0". Likewise, a memory NAND (9 or 13 or 17 or 21) will now go to logic "1" and a driver NAND (10, or 14 or 18 or 22) will go to logic "0" turning on the correct LED (3, or 4 or 5 or 6). When the LED turns on, its respective memory NAND (9, 13, 17 or 21) will have one of its inputs at logic "0" regardless of whether the fault has disappeared or not so the lit LED will stay lit until either RESET 1 or RESET 2 goes to logic "0". Also, when a LED turned on NAND 41 goes to logic "1" and NAND 42 goes to logic "0". This logic "0" is fed back to disable NANDs 8, 12, 16 and 20 so that no matter how many more of the 4 faults occur they cannot turn on their respective LED. The circuit then has a memory and also annunciates the first fault or the system is a "first come - first served" one. When RESET 1 or 2 goes to logic "0", NANDs 10, 14, 18 and 22 are switched to logic "1" which turns off any lit LEDs and resets all memories even if the fault still persists. If the fault persists the correct LED will relight when RESET 1 and 2 are both logic "1". If two faults do occur simultaneously only one LED will light but only the speed of the logic gates will determine which one.

LEDs 7, 8, 9 and 10 operate in another "first come - first served" basis as do LEDs 3, 4, 5 and 6 just described. LED 7 annuncuates an overload and LED 10 a forward overcurrent. LEDs 8 and 9 are uncommitted and can be used to annunciate any other faults which can be digital signals such as reverse overcurrent. If the fault signal is normally logic "1" and goes to "0" on a fault it is connected to terminal 51 or 59. If the signal is normally logic "0" and goes to logic "1" on a fault it should be connected to terminal 53 or 55. These LEDs operate in exactly the same manner with RESET just as LEDs 3, 4, 5, and 6 do. Note that a fault in either group will be displayed.

The Fault Indicator is not necessary to operation but certainly does help to locate a particular fault in the minimum time. Note that it cannot locate a faulty LP 15 supply voltage since LP 15 powers the card.

B. START-UP PROCEDURE

I. Introduction

These instructions provide a step by step procedure for first time start-up of the basic regulator of a M5B thyristor power system used as the armature supply for a dc motor drive.

Nonstandard functions such as special sequencing, direction logic, interconnection with other drives, etc. which pertain to a specific application must be covered by separate instructions.

The procedures should be followed in the specified sequence, checking each step against the schematic diagram. This will develop familiarity with the system and insure proper operation of the drive system when the sequence is completed. If difficulty is encountered at any step, the source of trouble and/or remedy may be obvious. If not, refer to the "Trouble Shooting" section of this instruction leaflet for more detailed instructions.

It should be possible to place the basic regulator in operation by following the start-up procedures as described, referring only to the applicable schematic diagrams. However, a more efficient and confident approach requires a knowledge of fundamental functions and relations which can be obtained by referring to the previous sections of this instruction leaflet.

II. System

A. General

This section is devoted to a procedure for first time start-up of the basic regulator of a M5B system as applied to armature power supplies and includes:

TPM - Thyristor Power Modulator case assembly, either single or double converter.

Basic regulator assembly containing:

1 - PS1 - ±24 volt, +15 volt regulated power supply.

2 - RG/GPG/01 - Gate pulse generators.

1 - TGD - Thyristor gate driver (2 cards if dual converter).

1 - RG/GS/02 - Gate synchronizer.

1 - Pot board.

1 - RG/S&P/01 - Sequence and protector.

1 - RG/VC & RL/01 - Voltage controller and reversing logic card. (Dual converters only)

1 - VS - Voltage sensor.

1 - RG/CC/01 - Current controller.

1 - Input card.

1 - RG/FI/01 - Fault indicator - optional

AC and dc power circuits with standard protection and sequencing.

B. Start-Up Procedure

1.0 Recommended Test Equipment

1.1 A multimeter with a internal impedance of 20,000 ohms/volt.

1.2 Adjustable battery powered test supply, 0-22V, with reversing and turn-off switch.

1.3 Dual beam oscilloscope such as Tektronix 502, 545 or equivalent.

NOTE: Be sure that the scope is NOT GROUNDED at the line plug or elsewhere. When the drive is energized, the scope case may be at some voltage potential above ground.

1.4 30 Pin extension board (S#1339A38G02).

2.0 Before Applying AC Power

2.1 Make a visual check of the equipment for loose wires and connections, remove blocking from relays and contactors, all function boards are present and plugged in to the basic regulator and all external connections are made as well as function jumpers per Figure I.

2.2 Disconnect one side of motor armature from the drive.

2.3 Remove incoming I[D]* wire at terminal block.

2.4 Remove the current controller board (RG/CC/01) and replace with a 30 pin extension board (S#1339A38G02).

2.5 Plug the current controller board into the extension board and open up the jumper connection on the extension board to pin 47.

2.6 Jumper out any ZONE A and ZONE B contacts of Input Board 1 that do not originate in the M5B structure.

2.7 Check TPM current transformers for proper primary turns as read from the schematic diagram. This is normally 1 except on the lower power ratings.

2.8 Remove any incoming -V[B]* wiresfrom the terminal blocks of the regulator assembly. Connect a ±15V VDC adjustable test voltage between -V[B]* and PSC. Set a 0 volts.

2.9 Connect an oscilloscope across TP-TN at resistor board terminals. Use ac line trigger, 2MS per CM sweep rate and appropriate vertical sensitivity.

2.10 Make sure that the DC LOOP selector switch normally mounted on the M5B cabinet door is in the PERMISSIVE CLOSE position.

3.0 Apply Rated 3 Phase AC Power With Phase Sequence R-S-T And Observe:

3.1 Transformer primary circuit breaker (is supplied) remains closed on transformer inrush. If the breaker trips out, increase the trip setting # in increments of "2" until the breaker remains closed.

3.2 Red indicating light mounted on the door indicates AC POWER ON.

3.3 Cabinet and TPM ventilating fans (if supplied) are operating and the air flow is from the bottom to the top of the structure.

3.4 Green indicating light mounted on the door indicates POWER SUPPLY READY. (Relay PSR is energized).

3.5 Voltage across CX and CY is 115V ±5V.

3.6 Light emitting diodes (LED'S) on the PS1 board indicate that PSP, PSN, and LP15 are energized.

3.7 The regulator power supply voltages should be as follows:

PSP	= +24V + 1V
PSN	= -24V ∓ 1V
LP15	= +15V ∓ 0.5V
RP	= +24V ∓ 4V, -2V

3.7 ZONE A and ZONE B LED's on Input Board 1 are energized.

3.8 The PH. SEQ (1 LED) and the OSC (2 LED) LED'S on the RG/GS/01 board are energized.

3.9 The OC (overcurrent) LED, the PL (power loss) LED, and the ON LED on the RG/S&P/01 board are deenergized.

3.10 If the conditions in step 3.9 are not observed, the following voltages or logic signals should be checked at the following pins of the RG/S&P/01 board. (a logic "1" = +12.5V to +16V and a logic "0" = 0V to + 1.5V).

pin	4	=	logic "1"	pin	27	=	logic "1"
pin	6	=	+24V	pin	29	=	+24V
pin	7	=	0V	pin	33	=	logic "1"
pin	8	=	logic "1"	pin	36	=	logic "1"
pin	11	=	logic "1"	pin	38	=	logic "0"
pin	13	=	logic "1"	pin	39	=	logic "1"
pin	14	=	logic "0"	pin	40	=	logic "0"
pin	15	=	logic "1"	pin	41	=	logic "0"
pin	16 & 17	=	PSC	pin	44	=	logic "1"
pin	19	=	logic "1"	pin	55	=	logic "1"
pin	21	=	logic "1"	pin	57	=	0V
pin	25	=	logic "1"				

ON ALL SUBSEQUENT STEPS THROUGHOUT THIS START-UP PROCEDURE IT IS ASSUMED THAT THE SERVICE ENGINEER WILL INVESTIGATE PREVENTATIVE INTERLOCKING CIRCUITS TO ENSURE THAT THE TEST FUNCTIONS CAN BE COMPLETED.

3.11 Remove wires marked SEQ. 1 and OFF from regulator terminal blocks and connect terminal block points to PSC through switches or jumpers. Open both of these switches which by definition is Logic "1". The following sequence will be used to open and close the dc contactor when required.

3.11.1 Close the dc contactor by pulsing SEQ. 1 jumper to PSC and then open.

3.11.2 Cause the dc contactor to open by pulsing OFF jumper to PSC and then open.

4.0 Inner Voltage Loop Test

4.1 Close the dc contactor.

4.2 Observe that the M LED on Input Board 1 is energized and the ON LED on the RG/S&P/01 board is energized. (This indicates that the dc contactor is closed and that the current controller and the outer loop controller have been released.)

4.3 Slowly adjust the test voltage applied to terminal -V[B]* of the terminal block from 0 to -10 volts and observe:

4.3.1 TPM output voltage waveshape should be smoothly controllable with six pulses per cycle. The pulses should be stable and of equal magnitude over the voltage range with no random jitter. Figures 1 and 2 show typical waveform at 50% and at rated voltage. Refer to the trouble shooting section if the waveshapes are not obtained.

4.3.2 The TPS output voltmeter varies smoothly from 0 to approximately positive rated volts.

4.3.3 Miniature meter +V[B] varies smoothly from 0 to +9.6V.

4.3.4 Miniature meter -V[C1] varies smoothly from +5V $\pm$1V to 0.4V $\pm$ 0.2V from 0 output to rated output respectively.

4.3.5 On double converters only, the FWD (1 LED) on the RG/VC&RL/01 board is energized.

4.4 For double converters, reverse the polarity of the test voltage applied in step 4.3 and observe:

4.4.1 Performance should duplicate that previously observed in steps 4.3.1 thru 4.3.4 except with all polarities reversed except -V[C1].

4.4.2 The REV (2 LED) on the RG/VC&RL/01 board is energized.

4.5 Remove ac power.

5.0 Voltage Limit Adjustment

5.1 Disconnect the test voltage from terminal -V[B]* of the terminal block, and reconnect the original wiring to this point.

5.2 Close the pin 47 circuit on the extender board in which the current controller RG/CC/01 is plugged.

5.3 Apply ac power and close the dc loop contactor.

5.4 The bus voltage is now to be set at 110% of rated value. For this purpose the board production -V[B]* (the current controller) is driven into saturation by applying the test voltage (+) to +I[D]* on the terminal blocks.

5.5 Trim the BUS VOLTAGE ADJUST pot (1P) on pot board (S#1841A46G01) to obtain 110% of rated bus voltage.

5.6 For double converters reverse the polarity of the test supply and note that the magnitude of the "reverse" output voltage is within $\pm$2% of the "forward" output voltage in step 5.5.

5.7 Remove ac power.

CAUTION: BEFORE CONDUCTING STALLED CURRENT TESTS ON A DC MOTOR, PLEASE REFER TO I.L. 16-800-286.

6.0 Current Loop Test

6.1 Verify that the current feedback polarity is correct per the schematic information.

6.2 Set-up the following temporary conditions:

6.2.1 Remove the motor field excitation.

6.2.2 Reconnect the motor armature circuit.

6.2.3 Turn pot 2P on the pot board (S#1841A46G01) fully CW.

6.2.4 Open the red jumper (2J) with Berg terminals to pin 35 of the current controller [RG/CC.01] so that +I[D]* can only produce rated current.

6.2.5 Check that 1J on the pot board is in the 125% position.

6.2.6 Place a scope between pin 7 of the pot board and PSC to monitor -/I[D]/F.

6.2.7 Apply the adjustable test reference +I[D]* of the terminal block. Set at 0 volts.

6.2.8 Make sure that the current controller gain jumper (3J), red jumper with Berg terminals, is connected between pins 51 and 49 of the current controller RG/CC/01.

6.3 Apply ac power and close the dc contactor. The current reference ramp and the current controller should be released by logic generated by Input Board 1 and RG/S&P/01. (pin 27 and 29 of the current controller should be +15VDC.
Note that the output voltage remains at zero and the motor remains at stand still.

6.4 Slowly increase the test reference to +10 VDC.

6.5 With pot 2P of the pot board, adjust the armature current for defined rated current. The voltage at pin 17 of the current controller should be -2V ±5% at rated current. Refer to the Trouble Shooting section of this instruction leaflet if -2V is not obtained.

6.6 Observe that the current feedback signal is similar to the one observed in the Inner Voltage Loop Test (six pulses per cycle of nearly equal amplitude). Reduce current reference to zero.

6.6.1 SLOWLY advance test voltage applied to +I[D]* terminal positively and observe armature current on oscilloscope and ammeter.
At first the current trace will appear as symmetrical "bumps" which have considerable 0 value time (discontinuous current). As the test voltage is raised, the zero current time will decrease and peaks get higher. When the current is continuous (oscilloscope trace does not reach zero volts), increase current about 10% further, but do not exceed 40% of rated.

6.7 Turn the current controller gain pot 4P on the pot board clockwise and move the CC gain jumper 3J (red jumper between pins 49 and 51 of the RG/CC/01) towards a higher gain position until the current feedback pulses become suddenly radically unequal (every second or third pulse is larger than others which indicates an instability of two or three times basic frequency).

The following tabulation indicates the gain changes achieved by connecting the gain jumper 3J attached to pin 51 to various other pins on the current controller RG/CC/01.

JUMPER PINS	GAIN
51 - 49	Minimum gain
No jumper *	Next highest gain
51 - 53	Next highest gain
51 - 53	Highest gain

*Leave one end of the jumper on pin 51 and open the other end.

6.8 Put the gain jumper (3J) to its next lower gain position. The current loop stability is now set. Check by applying the test voltage in step fashion and observing that response is smooth with zero or little overshoot.

6.9 If a double converter is used reverse polarity of test voltage to insure smooth transition between positive and negative current.

6.10 If the current controller is S#1745A21G01 or G03 it has a current rate adjustment controlled by 1P on the current controller. The range of adjustment is from 20 to 100 per unit per second and is linear with rotation. 1P should be set according to drive requirements usually the minimum of 20 is sufficient on all but very high speed of response systems. If the current controller style number ends in G02 or G04, there is no di/dt adjustment but fixed at 20 per unit per second.

6.11 Return the test reference to zero and remove ac power.

7.0 Adjustment Of Gate Pulse Suppression

CAUTION: BEFORE CONDUCTING STALLED CURRENT TESTS ON A DC MOTOR, PLEASE REFER TO I.L. 16-800-286.

7.1 Set the Forward Gate Pulse Suppression jumper 1J on pot board S#1841A46G01 at the next highest increment setting above the desired current limit setting. Gate pulse suppression is normally set between 120% and 125% of the current limit setting. The following is a table showing the standard fixed current limit settings that are available and their corresponding GPS setting. (values based on % of rated current).

C.L. SETTING	JUMPER CONNECTIONS	G.P.S. SETTING
100%	No Jumper	125%
125%	35 - 37	150%
150%	35 - 39	185%
175%	35 - 41	215%
200%	35 - 5	245%
250%	35 - 7	310%
300%	35 - 9	370%
400% (Test only)	35 - 33	

7.2 Place the current limit setting jumper (red jumper 2J) of the current controller edge connector to its "test" position (jumper between pins 35 and 33).

7.3 Apply ac power and close the dc loop.

7.4 Slowly increase the test reference +I[D]* until gate pulse suppression occurs. The value should be within ±5% of the selected setting.

7.5 Return test reference to zero and depress the GATE PULSE SUPPRESSION RESET pushbutton. GPS can also be reset by shorting the two lance terminals (LN1 and LN2) provided at the front edge of the RG/S&P/01 board.

7.6 The drive should return to its "ready" state (relay PSR should be energized).

7.7 For double converters reverse the polarity of the test reference +I[D]*.

7.8 Slowly increase the test reference until gate pulse suppression occurs. This value should be within ±2% of step 7.4.

7.9 Repeat step 7.5.

7.10 Remove ac power.

8.0 Current Limit Adjustment

8.1 Place the current limit setting jumper (red jumper 2J found on the current controller edge connector) to the desired current limit value. Refer to table in step 7.1.

8.2 Rapidly increase test voltage on I[D]* to 10 volts and verify that current is within 5% of the desired value.

9.0 Check Current Controller Sequence

9.1 While circulating around 20 to 30% current open contactor and observe that :

9.2 Armature current goes to zero before contactor opens (no arc).

9.3 Then TPM voltage goes to zero.

9.4 Remove ac power.

10.0 Check Motor Rotation and Compounding

10.1 With ac power off remove block on armature so motor is free to rotate.

CAUTION: MOTOR WILL BE FREE TO ROTATE BUT SINCE MOTOR WILL BE CURRENT REGULATED IT WILL ACCELERATE. CONSTANTLY OBSERVE MOTOR SPEED AND INITIATE STOP IF MOTOR ROTATES OVER HALF SPEED.

10.2 Reconnect shunt field of motor.

10.3 Apply ac power and set test voltage at zero.

10.4 Close contactor, armature current should be zero.

10.5 Slowly increase test voltage until motor rotates slowly and note direction and polarity of tachometer feedback voltage TG + to PSC (if supplied).

10.5.1 If rotation was correct for forward direction and TG+ positive with respect to PSC proceed with step 10.5.4. If not go to steps 10.5.2 and 10.5.3.

10.5.2 If rotation was correct and tachometer polarity wrong, reverse tachometer wires and recheck step 10.5 and 10.5.1.

10.5.3 If rotation was incorrect determine whether armature or field leads should be reversed and do so. Repeat steps 10.5 and 10.5.1.

10.5.4 Stop and remove ac power.

10.6 Check compounding if series field is supplied.

10.6.1 With power off reconnect series field and disconnect shunt field.

10.6.2 Set test voltage to zero and apply ac power.

10.6.3 Start drive, current should remain at zero.

10.6.4 Increase test voltage until motor just begins to rotate.

10.6.5 If rotation is correct proceed to step 10.6.7. If not go to step 10.6.6.

10.6.6 Stop and remove ac power and reverse series field and repeat steps 10.6 and 10.6.5.

10.6.7 Stop and remove ac power and make motor connections permanent. Reconnect shunt field.

11.0 Remove any test jumpers and voltages. Restore all removed connections.

12.0 The basic regulator is now set up. The remainder of any start-up and sequence control should be completed by referring to the appropriate instructions.

III. Trouble Shooting

A. General

This discussion is restricted to the standard M5B basic regulator system as used for dc motor armature. Since the equipment was tested at the factory, it is assumed that any trouble is due to component failure rather than incorrect wiring. In case of trouble in the basic TPS system the start-up procedure described in Section B.II provides an organized approach to trouble shooting. Those steps involving voltage measurements and sequence checks are considered to be self explanatory. However, if trouble is encountered in checking the basic regulator, the following trouble shooting procedure may be used.

B. Basic Regulator

1.0 Incorrect TPM Output Waveshape

1.1 If the waveshape is not similar to Figure 1 or Figure 2, a missing pulse is immediately apparent and indicates the corresponding thyristor is not firing. Check for open fuses or an open gate circuit. A typical pulse train is seen in Figure 3. This trace is obtained when a scope is connected across the gate of a thyristor at the pulse transformer and RC board (located on the TPM) with "G" (gate) positive with respect to "K" (cathode).

NOTE: The thyristor firing sequence is identified by color code as follows:

1TH	=	Brown	4TH	=	Yellow
2TH	=	Red	5TH	=	Green
3TH	=	Orange (or White)	6TH	=	Blue

IF THE PROBLEM IS NOT THE THYRISTOR OR A BLOWN FUSE, WE THEN WILL ASSUME IT'S IN THE TGD OR GPG'S.

WITH THE ASSUMPTION THAT THE GATE SYNC. BOARD IS OPERATING CORRECTLY, CHECK THE FOLLOWING BOARD OUTPUTS:

1.2 Check the output of the gate pulse generators (S#1671A17G01) as follows:

1.2.1 Remove the PC board producing the +V[C1] signal, i.e. the RG/VC&RL/01 board for a double converter or the RG/CC/01 board for a single converter.

1.2.2 Tie pin 57 of the gate synchronizing board (RG/GS/01) to PSC.

1.2.3 If a double converter, remove the "REV" TGD board.

1.2.4 Keep the dc loop open.

1.2.5 Make sure when the system is energized that all permissive signals to the "FWD" TGD board are as follows:

pin 41 = logic "1"
pin 11 = logic "1"
pin 15 = PSC

1.2.6 CALIBRATE SCOPE PROBES. Set scope on line sync. and chopped mode.

1.2.7 Put scope probe 1 on X1 (brown lead) of the gate control transformer with respect to PSC. Un calibrate scope so that 6 cm=1 cycle (360°). Magnitude of the ac wave is 70 volts $\pm$ 7V peak to PSC.

1.2.8 Put scope probe 2 on pin 5 (GP1) of the RG/GPG/01 board (pulse 1,3,5) with respect to PSC. Uncalibrate scope so that 6 cm=1 cycle (360°). Magnitude of pulse is +15V $\pm$2V (PULSE #1).

1.2.9 Apply ac power.

1.2.10 Superimpose the two wave forms and compare to Figure 5. Note that the delay angle is approximately 145° and the pulse train is approximately 85° long.

1.2.11 The remaining pulse trains can be checked in a similar manner.

PULSE #2 (GP2) - Move probe 1 to X2 (red lead) of the gate control transformer. Move probe 2 to pin 5 of the pulse 2,4,6, GPG.
The trace should be the same as Figure 5.

PULSE #3 thru #6-Move probe 1 per color code sequence with respect to GP3 thru GP6 for the two GPG boards. Compare to Figure 5.

1.2.12 If all GPG outputs check out OK, proceed to step 1.3.

1.3 Check the output of the thyristor gate driver (S#1668A25G01) as follows:

1.3.1 Set-up conditions the same as steps 1.2.1 thru 1.2.6.

1.3.2 Probe 1 of scope is to be used the same as in step 1.2.7.

1.3.3 Put scope probe 2 on pin 29 (brown) of the FWD TGD with respect to PSC. Uncalibrate scope so that 6 cm=1 cycle (360°). Magnitude of pulse is +22V $\pm$3V (PULSE #1).

1.3.4 Apply ac power.

1.3.5 Superimpose the two waveforms and compare to Figure 4. Note that the delay angle is approximately 145° and the pulse train is approximately 85° long (start of first pulse to the end of the last pulse of the pulse train and does not include the exponential decay).

1.3.6 The remaining pulse trains can be checked in a similar manner.

PULSE #2 - Move probe 1 to X2 (red lead) of the gate control transformer.
Move probe 2 to pin 27 (red) of the FWD TGD.
The trace should be the same as Figure 4.

PULSE #3 thru #6 - Move probes per color code firing sequence as specified in step 1.1.
Compare to Figure 4.

1.3.7 For double converter remove the "FWD" TGD and replace the "REV" TGD in its proper edge connector.
Repeat steps 1.3.1 thru 1.3.6 making sure that the permissive signals to the "REV" TGD are the same as in step 1.2.5.

1.4 If all the waveforms have checked out up to this point and the source of trouble has not been located, please refer to I.L. 16-800-289 for further information.

2.0 Incorrect Current Feedback Signal

2.1 If the current sensor output is not -2V at rated armature current several things could be wrong:

2.1.1 Primary turns (used only for small HP drives) may be incorrect.

2.1.2 PC board could have a cold solder joint.

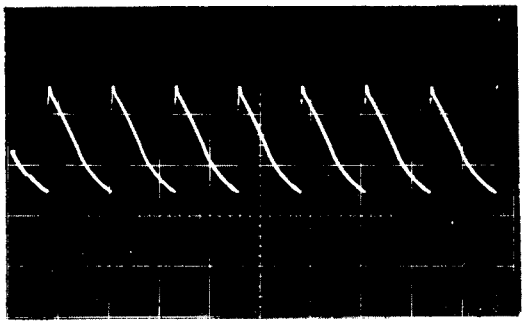
2.1.3 CT ratio could be incorrect.

$$\text{C.S. Output (-/I[D]/) (volts)} = \frac{I_{DC} \times 0.76 \times 5X \text{ PRI. TURNS}}{CT}$$

where:

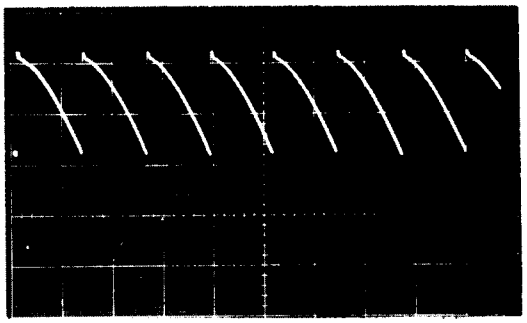
I_{DC} = dc armature current
PRI TURNS = # of cable loops thru CT +1
(this will normally be = 1 except for small HP drives)
CT = current transformer primary ampere rating
(200, 400, or 600) as marked on the CT.

IV. Appendix



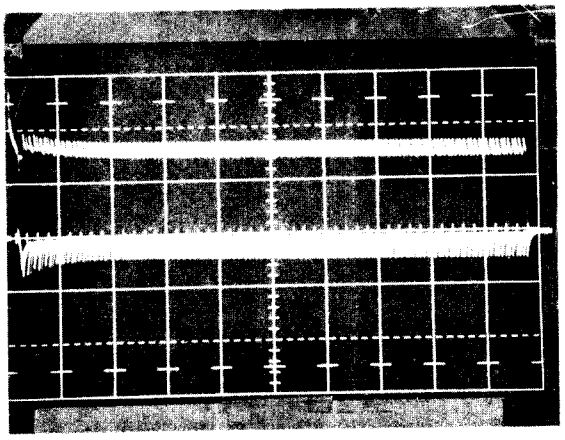
50% VOLTAGE 2ms/cm

FIGURE 1



RATED VOLTAGE 2ms/cm

FIGURE 2



1V/cm
0.2 ms/cm (uncalibrated)

FIGURE 3

THYRISTOR GATE PULSE TRAIN

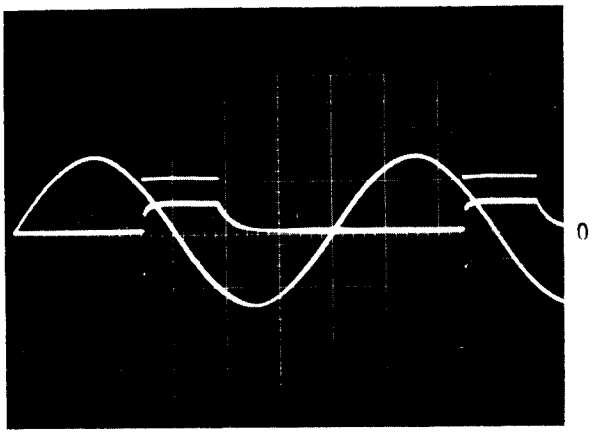


FIGURE 4

THYRISTOR GATE DRIVER OUTPUT PULSE TRAIN

50V/cm - GCT Output
20V/cm - TGD Output
1ms/cm - (uncalibrated)

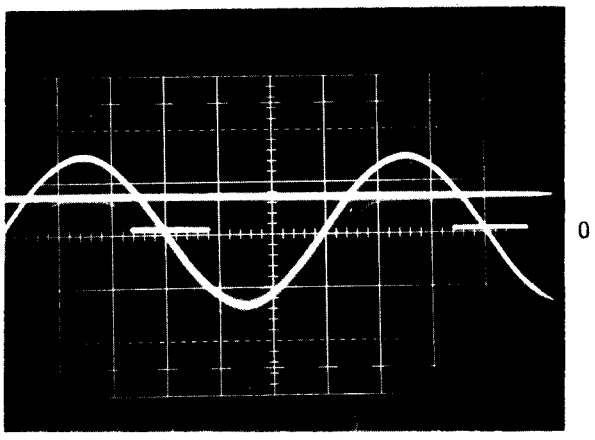


FIGURE 5

GATE PULSE GENERATOR OUTPUT PULSE TRAIN

50V/cm - GCT Output
20V/cm - GPG Output
1ms/cm - (uncalibrated)

Instruction Leaflets (Reference)

The following instruction leaflets (I.L.'s) describe the M5B system and its standard components.

Systems And Basic Regulator

I.L. 16-800-241 - M5B Thyristor Gate Driver
I.L. 16-800-242 - M5B Gate Pulse Generator
I.L. 16-800-244 - M5B Regulated Power Supply
I.L. 16-800-247 - Voltage Sensor
I.L. 16-800-288 - M5B Thyristor Power System
I.L. 16-800-289 - M5B Gating System
I.L. 16-800-298 - M5B Thyristor Replacement
I.L. 16-800-321 - Input Isolation Board

V. Service

Personnel familiar with electrical equipment utilizing semiconductors can isolate most problems using an oscilloscope, multimeter, and information contained in the instruction leaflet.

Semi-automatic equipment is available at the factory to test static and dynamic performance of all edge-connected printed circuit boards. Generally, repair of boards is facilitated by returning them to:

Westinghouse Electric Corporation
Industry Systems Division
P.O. Box 225
Buffalo, New York 14240