INSTALLATION • OPERATION • MAINTENANCE

INSTRUCTIONS

Model 67 NB REC

NARROWBAND RECEIVER

SPECIFICATIONS

Trip-Time Delay: 50 milliseconds for 340-Hz channel spacing, 35 milliseconds for 680-Hz channel spacing. In either case this delay is introduced only in the event that a trip has not been detected earlier through the wideband-receiver system.

Bandwidth: 20 Hz for 340-Hz channel spacing, 40 Hz when the channel spacing is 680 Hz.

Sensitivity: Adjustable from −40 to 0 dBm.

Ambient Temperature Range: -20° to $+55^{\circ}$C.

Power Requirements: Both plus and minus 12 Vdc, each 50 mA.

Size: Each Receiver (two required) is on a 4.71-inch high, by 8-inch deep circuit card no wider than one inch. Each Receiver can be mounted in two one-half-inch module spaces in the DIT-1 Chassis.

DESCRIPTION

General: The Model 67 NB REC Narrowband Receiver is available as an option useful for improving the dependability of DIT-1 equipment when operating through a communication medium with a high level of noise. Even a normally "quiet" circuit can be loaded with noise just at the time when transfer-trip relaying is most needed; the 10 dB improvement of signal-to-noise ratio of this receiver will enhance the dependability of the system under such conditions. The price paid for such additional dependability is an increase in response time to a trip signal. The narrowband receiving system, however, is so designed that it does not replace, but simply augments, the standard Wideband Receiver of the DIT-1 . Thus, the Narrowband Receiver will deliver a trip signal only when a trip has not previously been detected by the wideband receiver, presumably when it has gone into a block condition owing to excessive noise.

With transmitter and receiver connected back-to-back (no intervening communication system) the response time

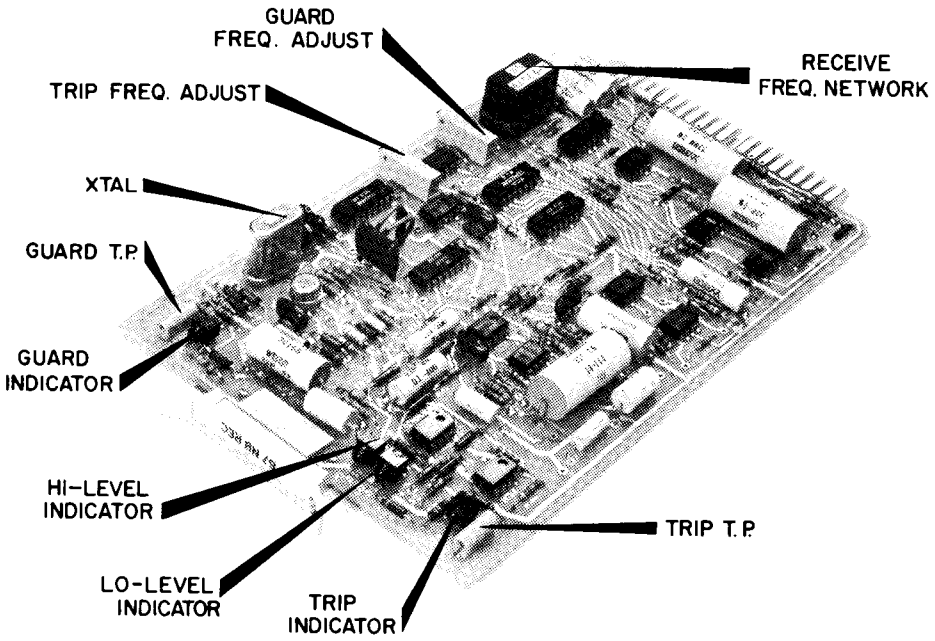

Figure 1. Narrowband Receiver card. Two Receivers are required for each channel; one per sub-channel.

NEW INFORMATION

EFFECTIVE APRIL 1977

of a narrowband receiving system to a transmitted trip will be approximately 50 milliseconds for a channel spacing of 340 Hz. If the noise, however, is below the level at which the Wideband Receiver blocks, then there will be no degradation of speed, (12 mS for 170-Hz bandwidth) for the Narrowband Receivers take over only when a high ratio of noise to signal prevails.

Two Narrowband Receivers are required per system, one for each sub-channel. They are interconnected so that a trip signal must be delivered by each receiver and combined with that from the other receiver in order to deliver a valid signal to succeeding elements of the System. In this way, failure of a component resulting in a false trip signal from a receiver is prevented from being propagated through the System.

Operating Principles: The philosophy of the design of the Model 67 NB REC Narrowband Receiver is contained in the block diagram of Figure 2. A balanced demodulator beats the incoming signal against a crystal-controlled local oscillator. Oscillator frequencies are selected so that, for 340-Hz channel spacing, and irrespective of carrier frequency,a demodulated trip signal gives an output of 340 Hz from the demodulator, while a demodulated guard signal gives an output of 190 Hz. With 680-Hz channel spacing, the principle is the same, though the frequencies differ.

A narrowband, active filter selects the guard and trip signals from the products of demodulation, and these each are rectified with a sensitive operational rectifier, then filtered with an active low-pass filter. The resulting dc signal, whose amplitude is a function of input level, is fed to two signal paths.

In one path, the signal is tested for acceptability as to amplitude and, if too high or too low, the output from the out-of-limit amplitude detectors established a "block" condition rendering the receiver inoperative. In the second path, the ratio of the levels of trip to guard signals, or vice-versa, is tested and, when that ratio is 10 dB or better the signal is accepted. Otherwise, a block is established.

These ratio detectors also determine whether the incoming signal is guard or trip. Using the voltage divider shown on the block diagram, it is clear that it is necessary, for a trip-output command to occur, that the trip signal applied to the inverting input of the signal-ratio detector for trip be 10 dB greater than the signal taken from the guard sub-channel and applied to the non-inverting input of the ratio detector. The same kind of arrangement is used for guard signal, to insure that what is received is truly a guard signal.

At the onset of operation, the system will be in a block condition. If, as in most cases, a guard signal is first received, the guard timer will ensure that the block is not released until guard signal has been received for at least 13 mS. This action improves security by preventing either noise or a transient signal from being mistakenly interpreted as a guard signal.

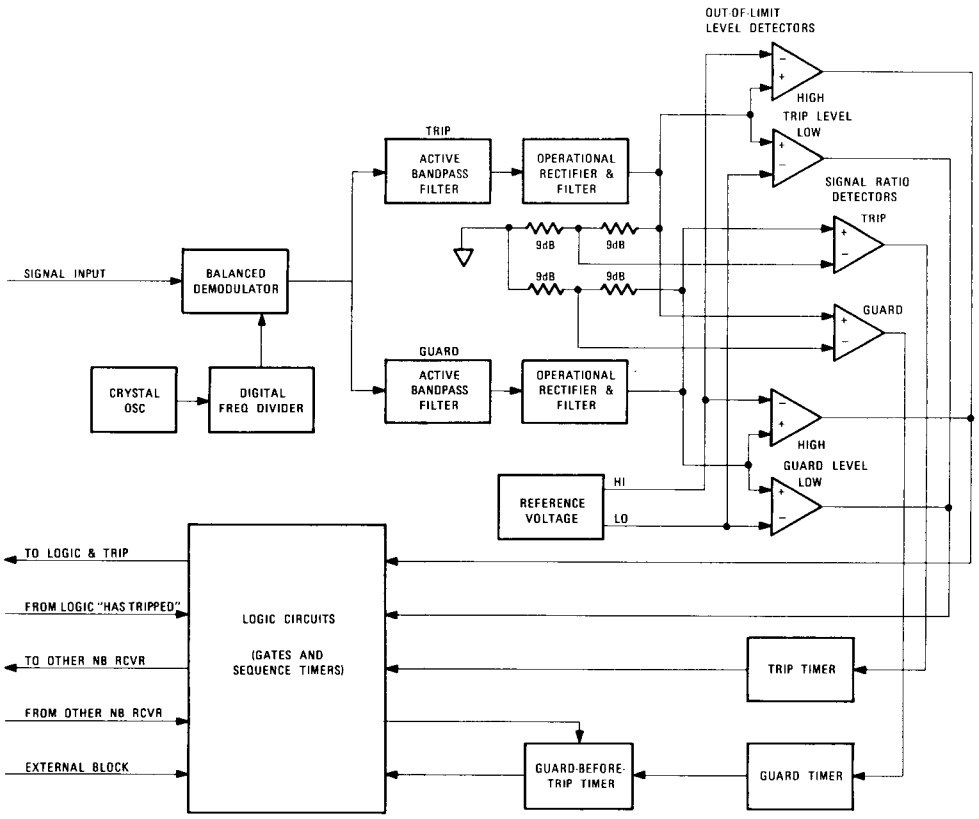

Figure 2. Block diagram, one of two required Narrowband Receivers per channel.

After the signal has been accepted as a valid guard, the guard-before-trip timer requires it to persist for about 300 mS longer, before enabling any trip signal received to be accepted.

Finally, the trip timer, like the guard timer, requires that a trip signal persist for at least 13 mS as a prerequisite to its acceptance through the balance of the circuit as a valid trip command.

The logic circuits of the narrowband receiver provide not only that the timing functions mentioned foregoing be met, but include also:

a. Provision for release of valid trip information to the Model 67 Logic card, for introduction into the regular information channels of the DIT-1 System.

b. Deletion of trip signal from the slower responding Narrowband Receiver when the trip already has been detected by the faster, Wideband Receiver.

c. Test for simultaneous receipt of trip from both Narrowband Receivers before that command is permitted to be released to the remainder of the System.

d. Provision to accept a block signal from an external source, to facilitate diagnostic work on the receiver.

THEORY OF OPERATION

Signal Processing: Before arriving at the Narrowband Receiver, signals from the communication line already have passed through the input circuits of the Model 67 REC Wideband Receiver. There they have been filtered, amplified, and leveled with the AGC circuits of that Receiver to the extent possible. Input signal for the Narrowband Receiver is taken from Terminal 7 of the Wideband Receiver. From there, it appears at Terminal 10 of the Narrowband Receiver, shown in Figure 3 on which the following discussion is based.

The input signal is delivered to IC1 and demodulated against a local-oscillator signal derived from Y1 through binary divider IC2. Frequency of the local-oscillator signal is chosen so that, with 340-Hz channel spacing, the frequency of the demodulated trip signal is always 340 Hz, that of the guard signal always 190 Hz. Table 1 tabulates all standard frequency assignments and components to be selected for each assignment.

Output signal from the demodulator, at Pins 6 and 9, is balanced and fed as a balanced input to IC3B, which functions as a differential amplifier with single-ended output. The output from IC3 is fed, in parallel, to the inputs of two active bandpass filters. The choice of the bandpass network through which it passes is determined by whether the signal is at trip frequency or at guard frequency. IC3A, IC8A, and IC8B are the active elements of the filter tuned to trip frequency. IC9A, IC9B, and IC16B form the guard-frequency filter. Resonant frequency of these narrowband filters is dictated by the choice made for channel spacing, and the frequencies are set by the network plugged into position RZ1. Potentiometers R19 and R36 are adjusted at the factory to peak the filters. The very narrow, 20-Hz, passband of these filters significantly contributes to the ability of the Narrowband Receiver to select signals in the presence of high levels of noise.

Following each filter is an operational rectifier, IC15A and IC15B for the case of trip signal. The output of each operational rectifier is smoothed with an active, low-pass filter, IC14B, for the case of trip signal. Either trip or guard signal, whichever is present, appears in the circuit after this point simply as a change in dc level.

DETECTION

The rectified and filtered input signal, either trip or guard, is next tested with two sets of detectors, namely: (a) window detectors which determine whether the signal level is acceptable, too high, or too low, and (b) signal-ratio detectors which require that the signal detected (either trip or guard) be greater by a predetermined amount (usually 10 dB) than its complement (guard or trip).

Level Detectors: The voltage divider R47, R50, and R51 sets high (4.5 Vdc) and low (0.15 Vdc) reference levels for signal-level detectors, IC13 for trip, IC12 for guard, beyond which the signal is unacceptable. For the case of a trip signal, if the signal is unacceptably high, the output of IC13B will be high. If the signal is unacceptably low, the output of IC13A will be low. Operation of the guard circuits is identical.

Ratio Detectors: IC10B and IC14A are signal-ratio detectors, for trip and guard signals respectively. For analysis, consider IC10B, the trip-signal detector. Guard signal, at the full level delivered from the output of the low-pass filter for the guard channel, is applied to its non-inverting input. Trip signal, when received, is first attenuated by 10 dB through R53 and R54, and then applied to the inverting input of IC10B. During guard conditions the output of IC10B, the trip detector, is high. When a trip is received the circuit demands that the signal at the inverting input be at least 10 dB greater than that at its non-inverting input for the output to go low and thus signal the arrival of a trip command. The same kind of action takes place at IC14A for acceptance of a guard signal.

The ratio detectors have three functions, namely: (a) they determine whether a received signal is a guard or a trip signal, (b) they test the level of the received signal against the level of signal or noise in the channel for the alternate command and demand a favorable condition, and (c) they deliver a command at their output only when these tests have been met, irrespective of the action of the out-of-limit level detectors.

LOGIC CIRCUITS

Function: The logic circuits used in the Narrowband Receiver are shown on the lower portion of Figure 3 and perform the following functions:

a. accept normal guard so that a spurious trip is prevented.

b. accept normal trip and deliver a trip output signal to the Logic Card of the Series 6745 unless otherwise prohibited.

c. withold trip output until a valid trip is confirmed from the companion Narrowband Receiver which monitors the other sub-channel of the System.

d. block trip output when the received signal is excessively low, relative levels of guard and trip signals are unfavorable, when a block signal is received from an external source, and when trip has previously been signaled by the faster responding Wideband Receivers in the System.

e. provide that the signal received, either guard or trip, persists for at least 13 mS to ensure its validity and to minimize the likelihood of response to spurious transient signals and noise.

f. Provide, in addition, that valid guard has been previously received for at least 300 mS before responding to a trip signal.

Guard Operation: The logic circuits function as follows: Consider, first, the most normal condition, which is receipt of guard signal of proper amplitude and frequency, so that a voltage between 0.15 and 4.5 Vdc appears at the non-inverting inputs of IC12A, IC12B, IC10B, and at R55. Under these conditions, output of IC14A is low, of IC12A is low, and of IC12B is high. Tracing through NOR gates IC7B and IC6A, it will be clear that a valid guard produces a high at the output of IC6A, thereby exciting the guard-signal monitor, DS1.

During normal conditions, the output of IC7A will be high. This signal, along with valid guard (also high) at the input of AND gate IC5A, causes a low at IC5, Pin 3 to charge C20 to a low 13 mS later, through operation of the Guard Timer comprised of C20 and R70. The resulting low at inverting-input-Pin 6 of IC17B places a logic high at one input of NOR gate IC7D and, thus, a low at its output. C21 of the Guard-before-trip Timer thus charges through R76 and, approximately 300 mS later, places a logic low at the input of NOR gate IC6C. This low allows passage of a logic-low trip signal at Pin 12 of that NOR gate, provided no block signal (a logic high) is present at Pin 11.

It may be noted that when guard ceases and a trip signal appears as a logic high, at Terminal 5 of the Receiver card, this high is introduced at Pin 13 of IC7D to keep the Guard-before-trip Timer charged, thus preventing a block at the input of IC6C because of loss of guard signal.

Trip Operation: The second normal condition of the circuit is receipt of a trip signal. Assume, again, that all other conditions are normal and, thus, permissive to execution of trip command. Then, the following events occur:

Trip signal from the output of IC10B is a logic low which, at Pin 1 of IC6B, causes a high at the output of that NOR gate and thus excites the trip indicator, DS4. This same signal, at Input-pin 8 of NAND gate IC5C, combines with the normal high at Pin 9 to cause a low at the output. This starts charging the Trip-timer capacitor, C19, through R67. After a delay of 13 mS, interposed by the Trip Timer to validate the trip signal further, the signal is released through IC16A to Input-pin 12 of IC6, where it appears as a logic low. Providing no block is present, the trip signal is released, via Card-terminal 7, to the companion receiver for combination with its trip signal (if present) as a further test of validity.

The trip signal is also combined, at the input of NAND gate IC5D, with the trip signal (if any) from the output of the companion Narrowband Receiver. Thus, the presence of two trip signals at the input of this gate, one from each Receiver, constitutes a further test of validity. If the test is satisfied, a trip command is released to the Logic Card of the Series 6745 through Terminal 5.

Protective Features: Supplementing the tests for validity discussed in the foregoing, the Receiver also contains several other protective features, as follows:

(a) Out-of-limit Signals Too Low

Signals of normal level appear at the inputs of IC7B as logic highs. Signals falling below the low limit of 0.15 Vdc, either trip (IC13A) or guard (IC12B), will cause a logic low at these inputs. When either or both signals are low, the resulting high at Pin 8, IC6B, will cause a low at its output, thereby blocking propagation of a trip signal through the circuit.

(b) Out-of-limit Signals Too High

When input signals exceed the high limit of 4.5 Vdc, the output of the level detectors for trip (IC13B) or guard (IC12A) will go high. These are combined at Pin 2 of IC6B, where a logic high blocks a trip as described in (a), foregoing.

(c) Trip and Guard Timers

The operation of both Timers is identical. Consider the Trip Timer at the output of IC5B. With no trip-signal input, Pin 9 is normally high, Pin 8 normally low, and the output is thus high. C19, therefore, with one side tied to V+, has no charge. Arrival of a trip signal will drop the output of IC5 low, and C19 will charge through R67. About one time constant later (about 13 mS), C19 will charge sufficiently to reduce Pin 3 of IC16A below the reference level held at Pin 2, thereby delaying propagation of the trip signal for the desired period. The period selected was chosen, on the basis of statistical studies, to provide good protection against the possibility of response to false transient signals or noise.

(d) Guard-before-trip Timer

This Timer, which is comprised of C20, which charges through R70 when the output of IC5A goes low, operates

exactly as the timers discussed in (c) foregoing. Its function is to assure a history of stable operation for the system for at least 300 mS before a trip signal is considered acceptable. The philosophy is to improve security. Note, however, that it is the guard signal, not the trip signal, that must be present for the specified 300 mS. Thus, under ordinary conditions, response to a trip signal is delayed only by the 13 mS delay of the Trip Timer. It is only under extraordinary conditions, as by failure of the signaling circuit that a 300 mS delay is introduced; and in this situation the delay is considered advisable for the sake of dependability as well as security.

(e) Trip from other Receiver

As described earlier in the general discussion of the logic section, the requirement for coincident trip from both Receivers is another feature enhancing the security of the System. Coincidence of two trip signals, one from the Channel-A Receiver, the other from the Receiver monitoring Channel B, is required at the two inputs of IC5D to generate a trip-output signal to the Model 67 Logic Card.

(f) "Has tripped" signal

Card Terminals 15 and 16 of the Narrowband Receiver provide for disablement of its trip output when a logic high appears at Terminal 15 or at Terminal 15 and 16. Such a logic high is delivered by the Logic Card when a trip signal has been detected earlier by the faster responding Model 67 Wideband Receivers. A logic high at Terminal 15, or at both, results in a high at Pin 11 of IC6C, and this constitutes a block against trip output at both Terminal 5 and Terminal 7.

At the input of IC5B, R90 holds Pin 5 low to protect the input circuits of the CMOS logic unit, used there, when open-circuited as during storage or transportation. R91 is returned to V+ to keep Pin 6 high when the System does not include a second Logic Card for redundancy, thereby preventing the block that would otherwise occur. If a second Card is used, however, its low output impedance will swamp the bias created by R91 so that the Logic Card will have control over the level at Pin 6. This approach has been used so that the intercard wiring patterns may be the same irrespective of whether one or two Logic Cards are used.

(g) Block-hold Timer

Consider the case in which a trip signal of short duration, say 100 mS, is transmitted over a quiet circuit to a receiving system equipped with a Narrowband Receiver. Owing to the faster response of the Wideband Receiver with which all Systems are equipped, a block will appear at Pin 11 of IC6C before a trip appears on Pin 12 through the slower action of the Narrowband Receiver. If the block from the Wideband Receiver were, then, instantly removed at the end of the short trip period, it is possible that the energy stored in the filters of the Narrowband Receiver will once again introduce a trip command into the System.

To countenance this possibility of an unwanted, second, trip command, the Block-Hold Timer is provided. When the start of a block from the Wideband Receiver originates a logic low at Pin 3 of IC7A, C25 charges rapidly through R97 and CR20, thereby introducing a block at Pin 9 of IC5 before the 13-mS delay of the Trip Timer has expired. When, however, the block from the Wideband Receiver is removed, C25 must discharge slowly through R98. For this case, the time constant is 46 mS, for which period C25 sustains the block condition at the input to IC5C. This method provides the time needed to dissipate the energy stored in the Narrowband Receiver by the original trip signal, and so a false trip is prevented.

(h) External Block

A logic high applied to Terminal 1 will block trip output from the Receiver. It enters the same logic path used for "has tripped" information. The facility is provided for diagnostic purposes and routine testing.

TABLE 1. COMPONENTS FOR DETERMINING FREQUENCY

GROUP	CENTER-FREQ. OF SUB-CHANNEL Hz	CHANNEL SPACING Hz	MODE AND FREQ. Hz	TRANSMITTER: CRYSTAL: SUFFIX FOR XTAL P/N HA-41034-	TRANSMITTER: CRYSTAL: FREQ. MHz	TRANSMITTER: CRYSTAL: CIRCUIT POSITION	TRANSMITTER: CRYSTAL: JUMPER POSITION	TRANSMITTER: BANDPASS-FILTER FREQ. DETER. NETWORK: P/N FOR POSITION RZ1	TRANSMITTER: BANDPASS-FILTER FREQ. DETER. NETWORK: P/N FOR POSITION RZ2	WIDEBAND RECEIVER: INPUT FILTER P/N	WIDEBAND RECEIVER: DISCRIMINATOR NETWORK P/N	WIDEBAND RECEIVER: POSITION IN CARD CAGE (NOTE 1)	NARROWBAND RECEIVER: BEAT FREQ. Hz	NARROWBAND RECEIVER: SUFFIX FOR XTAL P/N HA-41034-	NARROWBAND RECEIVER: CRYSTAL FREQ. MHz	NARROWBAND RECEIVER: JUMPER POSITION	NARROWBAND RECEIVER: RZ1 NETWORK PART NUMBER
1	A 935	340	T 860	−7	3.522560	Y1	A	HB-41065-1		HB-74200-1	HB-74300-1	A	1200	−5	2.45760	F	HB-41064-1
			G 1010	−8	4.136960	Y3											
	B 1275	340	G 1200	−5	2.457600	Y4	F		HB-41065-2	HB-74200-2	HB-74300-2	B	1010	−8	4.13690	A	HB-41064-1
			T 1350	−6	2.764800	Y2											
2	A 1275	340	T 1200	−5	2.457600	Y1	B	HB-41065-2		HB-74200-2	HB-74300-2	A	1540	−9	3.15392	F	HB-41064-1
			G 1350	−6	2.764800	Y3											
	B 1615	340	G 1540	−9	3.153920	Y4	F		HB-41065-3	HB-74200-3	HB-74300-3	B	1350	−6	2.76480	F	HB-41064-1
			T 1690	−10	3.461120	Y2											
3	A 1615	340	T 1540	−9	3.153920	Y1	B	HB-41065-3		HB-74200-3	HB-74300-3	A	1880	−11	3.85024	F	HB-41064-1
			G 1690	−10	3.461120	Y3											
	B 1955	340	G 1880	−11	3.850240	Y4	F		HB-41065-4	HB-74200-4	HB-74300-4	B	1690	−10	3.46112	F	HB-41064-1
			T 2030	−12	4.157440	Y2											
4	A 1955	340	T 1880	−11	3.850240	Y1	B	HB-41065		HB-74200-4	HB-74300-4	A	2220	−13	4.54656	F	HB-41064-1
			G 2030	−12	4.157440	Y3											
	B 2295	340	G 2220	−13	4.546560	Y4	F		HB-41065-5	HB-74200-5	HB-74300-5	B	2030	−12	4.15744	F	HB-41064-1
			T 2370	−14	4.853760	Y2											
5	A 2295	340	T 2220	−13	4.546560	Y1	B	HB-41065-5		HB-74200-5	HB-74300-5	A	2560	−3	2.62144	E	HB-41064-1
			G 2370	−14	4.853760	Y3											
	B 2635	340	G 2560	−3	2.621440	Y4	G		HB-41065-6	HB-74200-6	HB-74300-6	B	2370	−14	4.85367	F	HB-41064-1
			T 2710	−4	2.775040	Y2											
6	A 2635	340	T 2560	−3	2.621440	Y1	C	HB-41065-6		HB-74200-6	HB-74300-6	A	2900	−1	2.96960	E	HB-41064-1
			G 2710	−4	2.775040	Y3											
	B 2975	340	G 2900	−1	2.969600	Y4	G		HB-41065-7	HB-74200-7	HB-74300-7	B	2710	−4	2.77504	E	HB-41064-1
			T 3050	−2	3.123200	Y2											
7	A 2975	340	T 2900	−1	2.969600	Y1	C	HB-41065-7		HB-74200-7	HB-74300-7	A	3240	−15	3.31776	E	HB-41064-1
			G 3050	−2	3.123200	Y3											
	B 3315	340	G 3240	−15	3.317760	Y4	G		HB-41065-8	HB-74200-8	HB-74300-8	B	3050	−2	3.12320	E	HB-41064-1
			T 3390	−16	3.573760	Y2											
8	A 935	680	T 785	−17	3.215360	Y1	A	HB-41065-9		HB-74200-9	HB-74300-9	A	1465	−19	3.00032	F	HB-41064-2
			G 1085	−18	4.444160	Y3											
	B 1615	680	G 1465	−19	3.000320	Y4	F		HB-41065-10	HB-74200-10	HB-74300-10	B	1085	−18	4.44416	A	HB-41064-2
			T 1765	−20	3.614720	Y2											
9	A 1615	680	T 1465	−19	3.000320	Y1	B	HB-41065-10		HB-74200-10	HB-74300-10	A	2145	−21	4.39296	F	HB-41064-2
			G 1765	−20	3.614720	Y3											
	B 2295	680	G 2145	−21	4.392960	Y4	F		HB-41065-11	HB-74300-11	HB-74300-11	B	1765	−20	3.61472	F	HB-41064-2
			T 2445	−22	5.007360	Y2											
10	A 2295	680	T 2145	−21	4.392960	Y1	B	HB-41065-11		HB-74200-11	HB-74300-11	A	2825	−23	2.89280	E	HB-41064-2
			G 2445	−22	5.007360	Y3											
	B 2975	680	G 2825	−23	2.892800	Y4	G		HB-41065-12	HB-74200-12	HB-74300-12	B	2445	−22	5.00736	F	HB-41064-2
			T 3125	−24	3.200000	Y2											

(1) There are two receiver cards per group, one for subchannel A and one for subchannel B. Positions shown are for both wideband and narrowband receiver at their respective locations. Do NOT place narrowband receiver cards in wideband locations, and vice versa.

Table of Replaceable Parts

DIAGRAM SYMBOL	NAME OF PART AND DESCRIPTION	PART NO.
C1, 2	Capacitor, silvered mica, 56 pF, 5%, 500 V, Electro Motive DM-15, or eq.	HA-16517
C3	Capacitor, tantalum, 15 μF, 20%, 20 V, Kemet 1314D227M010AS, or eq.	H-1007-716
C4, 5, 23, 24	Capacitor, tantalum, 1 μF, 20%, 35 V, Kemet T324A473N035AS, or eq.	H-1007-496
C6, 11, 12	Capacitor, silvered mica, 33 pF, 5%, 500 V, Electro Motive DM-15, or eq.	HA-16511
C7, 8, 9, 10	Capacitor, poly., 0.022 μF, 2%, 100 V, Wesco 32P, or eq.	H-5115-51
C13, 14	Capacitor, MPC, 0.56 μF, 2%, 100 V, Wesco 32MPC, or eq.	H-1007-1330
C15, 16	Capacitor, poly., 0.01 μF, 2%, 100 V, Wesco 32P, or eq.	H-5115-135
C17, 18	Capacitor, MPC, 0.033 μF, 2%, 100 V, Wesco 32 MPC, or eq.	H-1007-1328
C19, 20	Capacitor, poly., 0.18 μF, 2%, 100 V, Wesco 32P, or eq.	H-5115-97
C21	Capacitor, metallized mylar, 1 μF, 2%, 100 V, Wesco 32 MM, or eq.	H-1007-795
C22	Capacitor, silvered mica, 47 pF, 5%, 500 V, Electro Motive DM-15, or eq.	HA-16515
C25	Capacitor, mylar, 0.1 μF, 10%, 50 V, TRW 601PE Slim-Line, or eq.	H-1080-304
C26, 27	Capacitor, 0.22 μF, 2%, 50 V, Wesco 32 MPC, or eq.	H-1007-1329
CR1 thru 20	Diode, silicon, 1N914B	HA-26482
IC1	Integrated circuit, balanced modulator, Motorola MC1496G, or eq.	H-0620-110
IC2	Integrated circuit, 12-stage, ripple-carry binary counter/divider RCA CD4040AE, or eq.	H-0620-21
IC3, 8 thru 17	Linear opamp, dual National LM-1458N, or eq.	H-0620-51
IC4	Integrated circuit, hex buffer inverter, RCA CD4049AE, or eq.	H-0615-7
IC5	Quad, 2-input NAND gate, RCA CD4011AE, or eq.	H-0615-5
IC6	Triple, 3-input NOR gate, RCA CD4021AE, or eq.	H-0615-20
IC7	Quad, 2-input NOR gate, RCA CD4001AE, or eq.	H-0615-3
R1 thru 18, R20 thru 35, R37 thru 88, R90 thru 100	Resistor, metal-film, precision 1%, 1/8 W, 100 PPM/DEG C, Type RN55D per RFL spec HA-38301	H-1510-(XXX)
R19, 36	Resistor, variable, 10 K, 10%, ¾ W, Helipot 79PR10K, or eq.	HA-39539
R89	Not used	
RZ1	Resistor, network assembly, exact specification dependent upon channel spacing	HB-41064-(X)
Y1	Crystal, piezoelectric, frequency per channel assignment	HA-41034-(X)

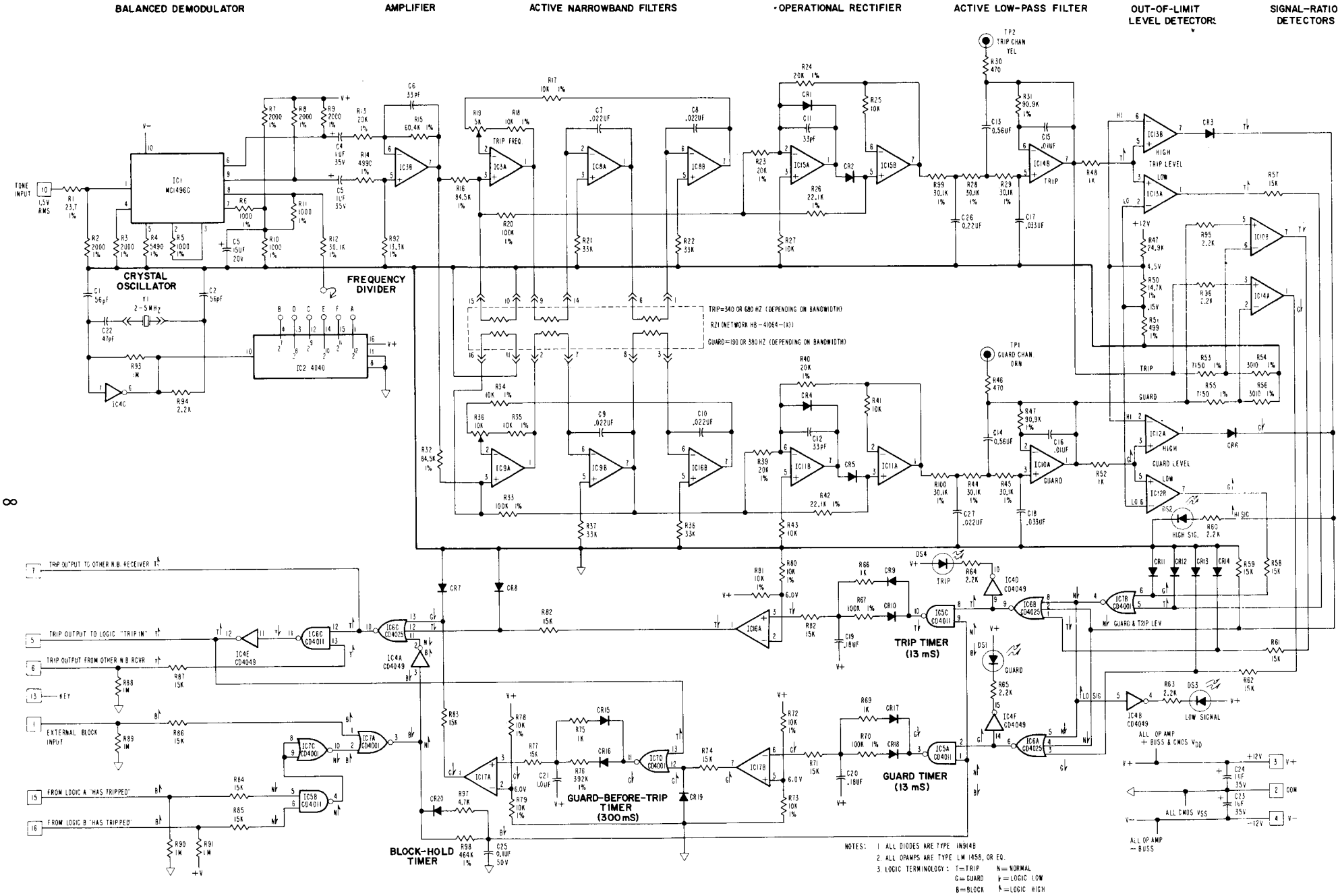

Figure 3. Schematic of Narrowband Receiver for one sub-channel

INSTALLATION • OPERATION • MAINTENANCE

INSTRUCTIONS

DIT-1 AND DIT-1T FREQUENCY-SHIFT AUDIO-TONE FOR PROTECTIVE RELAYING

The attached sheet should be substituted for page 5-6 of the section dealing with the *Series 6000 DC-DC Converter Power Supplies.* (This material is ten pages from the end of the booklet).

Table of Replaceable Parts

DIAGRAM SYMBOL	MODEL	NAME OF PART AND DESCRIPTION	PART NO.
		MISCELLANEOUS COMPONENTS	
S1	All	Switch, toggle SPDT: Right angle mtg. C & K Components 7101-A	HA-39562
TP1 & 3	All	Test jack, red: Cinch 119437-B	HA-38116-2
TP2 & 4	All	Test jack, black: Cinch 119437-C	HA-38116-3
		RESISTORS	
R1	All 129 V	Resistor, fixed comp.: 15 K, 5%, 2 W, Allen Bradley HB	H-1009-251
	All 48 V and All 24 V & 12 V	Same as above, 2.7 K	H-1009-1062
R2	All 129 V	Resistor, fixed.: 33 ohm, 5%, 2 W, Allen Bradley HB	H-1009-1064
	All 48 V and All 24 V and 12 V	Same as above, 22 ohm	H-1009-1063
R3	All 129 V	Resistor, fixed comp.: 12 ohm, 5%, 1W, Allen Bradley GB	H1009-1065
	All 48 V and All 24 V and 12 V	Same as above, 10-ohm	H-1009-4
R4, 5, 6, & 7	All with O-V Protection	Resistor, fixed comp.: 47 ohm, 5%, ¼W, Allen Bradley CB	H-1009-832
R8	All	Resistor, fixed comp.: 3K, 5%, 1 W, Allen Bradley GB	H-1009-466
R9	All	Resistor, fixed comp.: 5.1 ohm, 5%, ½W, Allen BradleyGB	H-1009-712
		SEMICONDUCTORS	
CR1, 2, 12, 13	All	Diode silicon, Type 1N914B	HA-26482
CR3 & 4	All	Rectifier bridge assy., Varo VS-148X	HA-39509
CR5 & 7	All with O-V Protection	Diode, zener: 14 V, 5%, 500 mW, Type 1N5244B	HA-41075
CR6, 8, 10, 11	All 0.375-A units	Diode, rectifier: 1 A, Type 1N4003, Solitron S4003TA20	HA-30769
DS1	All	Light-emitting diode, Dialight Cp. 550-0102	HA-39568
IC1 & 2	All	Three-terminal voltage reg., Fairchild UGH 7812393 National LM340-12T	H-0620-69
Q1 & 2	All 129V	Transistors, matched pair	HA-46756
	All 24V & 12 V	Transistors, matched pair	HA-46757
SCR1 & 2	All with O-V Protection	Silicon controlled rectifier, Motorola 2N4441 or GE C122F	HA-41072
	All	Schematic	HD-41502
		PARTS LIST FOR 1-AMP EXTERNAL REGULATOR, P/N HB-41520	
C1 & 2	All 1-Amp.	Same as C8 in basic unit	
C3 & 4	All 1-Amp.	Same as C9 in basic unit	
CR1, 2, 3, & 4	All 1-Amp.	Diode, rectifier, 1 A, Type 1N4003	HA-30769
IC1 & 2	All 1-Amp.	Same as in basic unit	

INSTALLATION • OPERATION • MAINTENANCE

INSTRUCTIONS

Model 67 NB REC

NARROWBAND RECEIVER

SPECIFICATIONS

Trip-Time Delay: 50 milliseconds for 340-Hz channel spacing, 35 milliseconds for 680-Hz channel spacing. In either case this delay is introduced only in the event that a trip has not been detected earlier through the wideband-receiver system.

Bandwidth: 20 Hz for 340-Hz channel spacing, 40 Hz when the channel spacing is 680 Hz.

Sensitivity: Adjustable from −40 to 0 dBm.

Ambient Temperature Range: -20° to $+55^{\circ}$C.

Power Requirements: Both plus and minus 12 Vdc, each 50 mA.

Size: Each Receiver (two required) is on a 4.71-inch high, by 8-inch deep circuit card no wider than one inch. Each Receiver can be mounted in two one-half-inch module spaces in the DIT-1 Chassis.

DESCRIPTION

General: The Model 67 NB REC Narrowband Receiver is available as an option useful for improving the dependability of DIT-1 equipment when operating through a communication medium with a high level of noise. Even a normally "quiet" circuit can be loaded with noise just at the time when transfer-trip relaying is most needed; the 10 dB improvement of signal-to-noise ratio of this receiver will enhance the dependability of the system under such conditions. The price paid for such additional dependability is an increase in response time to a trip signal. The narrowband receiving system, however, is so designed that it does not replace, but simply augments, the standard Wideband Receiver of the DIT-1 . Thus, the Narrowband Receiver will deliver a trip signal only when a trip has not previously been detected by the wideband receiver, presumably when it has gone into a block condition owing to excessive noise.

With transmitter and receiver connected back-to-back (no intervening communication system) the response time

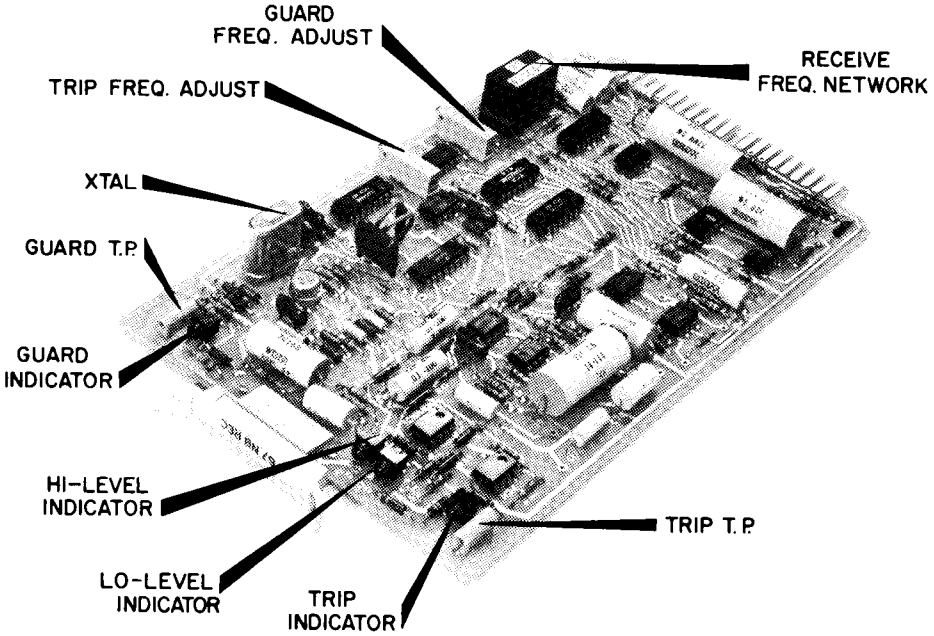

Figure 1. Narrowband Receiver card. Two Receivers are required for each channel; one per sub-channel.

NEW INFORMATION

EFFECTIVE APRIL 1977

of a narrowband receiving system to a transmitted trip will be approximately 50 milliseconds for a channel spacing of 340 Hz. If the noise, however, is below the level at which the Wideband Receiver blocks, then there will be no degradation of speed, (12 mS for 170-Hz bandwidth) for the Narrowband Receivers take over only when a high ratio of noise to signal prevails.

Two Narrowband Receivers are required per system, one for each sub-channel. They are interconnected so that a trip signal must be delivered by each receiver and combined with that from the other receiver in order to deliver a valid signal to succeeding elements of the System. In this way, failure of a component resulting in a false trip signal from a receiver is prevented from being propagated through the System.

Operating Principles: The philosophy of the design of the Model 67 NB REC Narrowband Receiver is contained in the block diagram of Figure 2. A balanced demodulator beats the incoming signal against a crystal-controlled local oscillator. Oscillator frequencies are selected so that, for 340-Hz channel spacing, and irrespective of carrier frequency, a demodulated trip signal gives an output of 340 Hz from the demodulator, while a demodulated guard signal gives an output of 190 Hz. With 680-Hz channel spacing, the principle is the same, though the frequencies differ.

A narrowband, active filter selects the guard and trip signals from the products of demodulation, and these each are rectified with a sensitive operational rectifier, then filtered with an active low-pass filter. The resulting dc signal, whose amplitude is a function of input level, is fed to two signal paths.

In one path, the signal is tested for acceptability as to amplitude and, if too high or too low, the output from the out-of-limit amplitude detectors established a "block" condition rendering the receiver inoperative. In the second path, the ratio of the levels of trip to guard signals, or vice-versa, is tested and, when that ratio is 10 dB or better the signal is accepted. Otherwise, a block is established.

These ratio detectors also determine whether the incoming signal is guard or trip. Using the voltage divider shown on the block diagram, it is clear that it is necessary, for a trip-output command to occur, that the trip signal applied to the inverting input of the signal-ratio detector for trip be 10 dB greater than the signal taken from the guard sub-channel and applied to the non-inverting input of the ratio detector. The same kind of arrangement is used for guard signal, to insure that what is received is truly a guard signal.

At the onset of operation, the system will be in a block condition. If, as in most cases, a guard signal is first received, the guard timer will ensure that the block is not released until guard signal has been received for at least 13 mS. This action improves security by preventing either noise or a transient signal from being mistakenly interpreted as a guard signal.

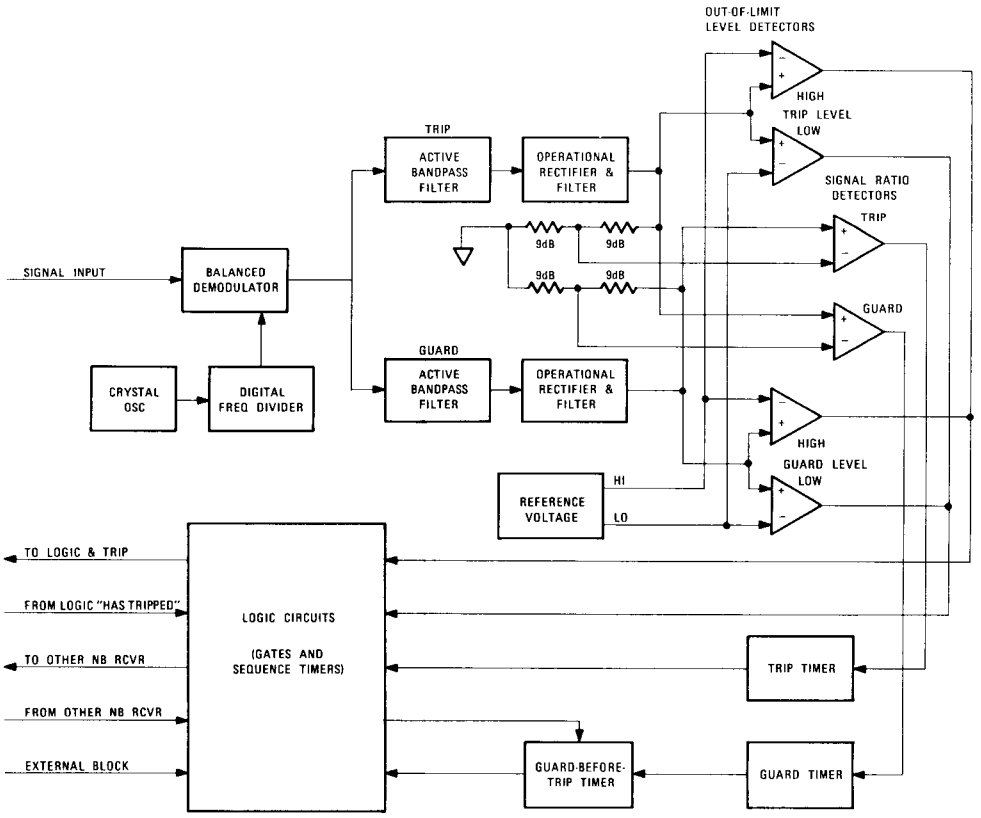

Figure 2. Block diagram, one of two required Narrowband Receivers per channel.

After the signal has been accepted as a valid guard, the guard-before-trip timer requires it to persist for about 300 mS longer, before enabling any trip signal received to be accepted.

Finally, the trip timer, like the guard timer, requires that a trip signal persist for at least 13 mS as a prerequisite to its acceptance through the balance of the circuit as a valid trip command.

The logic circuits of the narrowband receiver provide not only that the timing functions mentioned foregoing be met, but include also:

a. Provision for release of valid trip information to the Model 67 Logic card, for introduction into the regular information channels of the DIT-1 System.

b. Deletion of trip signal from the slower responding Narrowband Receiver when the trip already has been detected by the faster, Wideband Receiver.

c. Test for simultaneous receipt of trip from both Narrowband Receivers before that command is permitted to be released to the remainder of the System.

d. Provision to accept a block signal from an external source, to facilitate diagnostic work on the receiver.

THEORY OF OPERATION

Signal Processing: Before arriving at the Narrowband Receiver, signals from the communication line already have passed through the input circuits of the Model 67 REC Wideband Receiver. There they have been filtered, amplified, and leveled with the AGC circuits of that Receiver to the extent possible. Input signal for the Narrowband Receiver is taken from Terminal 7 of the Wideband Receiver. From there, it appears at Terminal 10 of the Narrowband Receiver, shown in Figure 3 on which the following discussion is based.

The input signal is delivered to IC1 and demodulated against a local-oscillator signal derived from Y1 through binary divider IC2. Frequency of the local-oscillator signal is chosen so that, with 340-Hz channel spacing, the frequency of the demodulated trip signal is always 340 Hz, that of the guard signal always 190 Hz. Table 1 tabulates all standard frequency assignments and components to be selected for each assignment.

Output signal from the demodulator, at Pins 6 and 9, is balanced and fed as a balanced input to IC3B, which functions as a differential amplifier with single-ended output. The output from IC3 is fed, in parallel, to the inputs of two active bandpass filters. The choice of the bandpass network through which it passes is determined by whether the signal is at trip frequency or at guard frequency. IC3A, IC8A, and IC8B are the active elements of the filter tuned to trip frequency. IC9A, IC9B, and IC16B form the guard-frequency filter. Resonant frequency of these narrowband filters is dictated by the choice made for channel spacing, and the frequencies are set by the network plugged into position RZ1. Potentiometers R19 and R36 are adjusted at the factory to peak the filters. The very narrow, 20-Hz, passband of these filters significantly contributes to the ability of the Narrowband Receiver to select signals in the presence of high levels of noise.

Following each filter is an operational rectifier, IC15A and IC15B for the case of trip signal. The output of each operational rectifier is smoothed with an active, low-pass filter, IC14B, for the case of trip signal. Either trip or guard signal, whichever is present, appears in the circuit after this point simply as a change in dc level.

DETECTION

The rectified and filtered input signal, either trip or guard, is next tested with two sets of detectors, namely: (a) window detectors which determine whether the signal level is acceptable, too high, or too low, and (b) signal-ratio detectors which require that the signal detected (either trip or guard) be greater by a predetermined amount (usually 10 dB) than its complement (guard or trip).

Level Detectors: The voltage divider R47, R50, and R51 sets high (4.5 Vdc) and low (0.15 Vdc) reference levels for signal-level detectors, IC13 for trip, IC12 for guard, beyond which the signal is unacceptable. For the case of a trip signal, if the signal is unacceptably high, the output of IC13B will be high. If the signal is unacceptably low, the output of IC13A will be low. Operation of the guard circuits is identical.

Ratio Detectors: IC10B and IC14A are signal-ratio detectors, for trip and guard signals respectively. For analysis, consider IC10B, the trip-signal detector. Guard signal, at the full level delivered from the output of the low-pass filter for the guard channel, is applied to its non-inverting input. Trip signal, when received, is first attenuated by 10 dB through R53 and R54, and then applied to the inverting input of IC10B. During guard conditions the output of IC10B, the trip detector, is high. When a trip is received the circuit demands that the signal at the inverting input be at least 10 dB greater than that at its non-inverting input for the output to go low and thus signal the arrival of a trip command. The same kind of action takes place at IC14A for acceptance of a guard signal.

The ratio detectors have three functions, namely: (a) they determine whether a received signal is a guard or a trip signal, (b) they test the level of the received signal against the level of signal or noise in the channel for the alternate command and demand a favorable condition, and (c) they deliver a command at their output only when these tests have been met, irrespective of the action of the out-of-limit level detectors.

LOGIC CIRCUITS

Function: The logic circuits used in the Narrowband Receiver are shown on the lower portion of Figure 3 and perform the following functions:

a. accept normal guard so that a spurious trip is prevented.

b. accept normal trip and deliver a trip output signal to the Logic Card of the Series 6745 unless otherwise prohibited.

c. withold trip output until a valid trip is confirmed from the companion Narrowband Receiver which monitors the other sub-channel of the System.

d. block trip output when the received signal is excessively low, relative levels of guard and trip signals are unfavorable, when a block signal is received from an external source, and when trip has previously been signaled by the faster responding Wideband Receivers in the System.

e. provide that the signal received, either guard or trip, persists for at least 13 mS to ensure its validity and to minimize the likelihood of response to spurious transient signals and noise.

f. Provide, in addition, that valid guard has been previously received for at least 300 mS before responding to a trip signal.

Guard Operation: The logic circuits function as follows: Consider, first, the most normal condition, which is receipt of guard signal of proper amplitude and frequency, so that a voltage between 0.15 and 4.5 Vdc appears at the non-inverting inputs of IC12A, IC12B, IC10B, and at R55. Under these conditions, output of IC14A is low, of IC12A is low, and of IC12B is high. Tracing through NOR gates IC7B and IC6A, it will be clear that a valid guard produces a high at the output of IC6A, thereby exciting the guard-signal monitor, DS1.

During normal conditions, the output of IC7A will be high. This signal, along with valid guard (also high) at the input of AND gate IC5A, causes a low at IC5, Pin 3 to charge C20 to a low 13 mS later, through operation of the Guard Timer comprised of C20 and R70. The resulting low at inverting-input-Pin 6 of IC17B places a logic high at one input of NOR gate IC7D and, thus, a low at its output. C21 of the Guard-before-trip Timer thus charges through R76 and, approximately 300 mS later, places a logic low at the input of NOR gate IC6C. This low allows passage of a logic-low trip signal at Pin 12 of that NOR gate, provided no block signal (a logic high) is present at Pin 11.

It may be noted that when guard ceases and a trip signal appears as a logic high, at Terminal 5 of the Receiver card, this high is introduced at Pin 13 of IC7D to keep the Guard-before-trip Timer charged, thus preventing a block at the input of IC6C because of loss of guard signal.

Trip Operation: The second normal condition of the circuit is receipt of a trip signal. Assume, again, that all other conditions are normal and, thus, permissive to execution of trip command. Then, the following events occur:

Trip signal from the output of IC10B is a logic low which, at Pin 1 of IC6B, causes a high at the output of that NOR gate and thus excites the trip indicator, DS4. This same signal, at Input-pin 8 of NAND gate IC5C, combines with the normal high at Pin 9 to cause a low at the output. This starts charging the Trip-timer capacitor, C19, through R67. After a delay of 13 mS, interposed by the Trip Timer to validate the trip signal further, the signal is released through IC16A to Input-pin 12 of IC6, where it appears as a logic low. Providing no block is present, the trip signal is released, via Card-terminal 7, to the companion receiver for combination with its trip signal (if present) as a further test of validity.

The trip signal is also combined, at the input of NAND gate IC5D, with the trip signal (if any) from the output of the companion Narrowband Receiver. Thus, the presence of two trip signals at the input of this gate, one from each Receiver, constitutes a further test of validity. If the test is satisfied, a trip command is released to the Logic Card of the Series 6745 through Terminal 5.

Protective Features: Supplementing the tests for validity discussed in the foregoing, the Receiver also contains several other protective features, as follows:

(a) Out-of-limit Signals Too Low

Signals of normal level appear at the inputs of IC7B as logic highs. Signals falling below the low limit of 0.15 Vdc, either trip (IC13A) or guard (IC12B), will cause a logic low at these inputs. When either or both signals are low, the resulting high at Pin 8, IC6B, will cause a low at its output, thereby blocking propagation of a trip signal through the circuit.

(b) Out-of-limit Signals Too High

When input signals exceed the high limit of 4.5 Vdc, the output of the level detectors for trip (IC13B) or guard (IC12A) will go high. These are combined at Pin 2 of IC6B, where a logic high blocks a trip as described in (a), foregoing.

(c) Trip and Guard Timers

The operation of both Timers is identical. Consider the Trip Timer at the output of IC5B. With no trip-signal input, Pin 9 is normally high, Pin 8 normally low, and the output is thus high. C19, therefore, with one side tied to V+, has no charge. Arrival of a trip signal will drop the output of IC5 low, and C19 will charge through R67. About one time constant later (about 13 mS), C19 will charge sufficiently to reduce Pin 3 of IC16A below the reference level held at Pin 2, thereby delaying propagation of the trip signal for the desired period. The period selected was chosen, on the basis of statistical studies, to provide good protection against the possibility of response to false transient signals or noise.

(d) Guard-before-trip Timer

This Timer, which is comprised of C20, which charges through R70 when the output of IC5A goes low, operates

exactly as the timers discussed in (c) foregoing. Its function is to assure a history of stable operation for the system for at least 300 mS before a trip signal is considered acceptable. The philosophy is to improve security. Note, however, that it is the guard signal, not the trip signal, that must be present for the specified 300 mS. Thus, under ordinary conditions, response to a trip signal is delayed only by the 13 mS delay of the Trip Timer. It is only under extraordinary conditions, as by failure of the signaling circuit that a 300 mS delay is introduced; and in this situation the delay is considered advisable for the sake of dependability as well as security.

(e) Trip from other Receiver

As described earlier in the general discussion of the logic section, the requirement for coincident trip from both Receivers is another feature enhancing the security of the System. Coincidence of two trip signals, one from the Channel-A Receiver, the other from the Receiver monitoring Channel B, is required at the two inputs of IC5D to generate a trip-output signal to the Model 67 Logic Card.

(f) "Has tripped" signal

Card Terminals 15 and 16 of the Narrowband Receiver provide for disablement of its trip output when a logic high appears at Terminal 15 or at Terminal 15 and 16. Such a logic high is delivered by the Logic Card when a trip signal has been detected earlier by the faster responding Model 67 Wideband Receivers. A logic high at Terminal 15, or at both, results in a high at Pin 11 of IC6C, and this constitutes a block against trip output at both Terminal 5 and Terminal 7.

At the input of IC5B, R90 holds Pin 5 low to protect the input circuits of the CMOS logic unit, used there, when open-circuited as during storage or transportation. R91 is returned to V+ to keep Pin 6 high when the System does not include a second Logic Card for redundancy, thereby preventing the block that would otherwise occur. If a second Card is used, however, its low output impedance will swamp the bias created by R91 so that the Logic Card will have control over the level at Pin 6. This approach has been used so that the intercard wiring patterns may be the same irrespective of whether one or two Logic Cards are used.

(g) Block-hold Timer

Consider the case in which a trip signal of short duration, say 100 mS, is transmitted over a quiet circuit to a receiving system equipped with a Narrowband Receiver. Owing to the faster response of the Wideband Receiver with which all Systems are equipped, a block will appear at Pin 11 of IC6C before a trip appears on Pin 12 through the slower action of the Narrowband Receiver. If the block from the Wideband Receiver were, then, instantly removed at the end of the short trip period, it is possible that the energy stored in the filters of the Narrowband Receiver will once again introduce a trip command into the System.

To countenance this possibility of an unwanted, second, trip command, the Block-Hold Timer is provided. When the start of a block from the Wideband Receiver originates a logic low at Pin 3 of IC7A, C25 charges rapidly through R97 and CR20, thereby introducing a block at Pin 9 of IC5 before the 13-mS delay of the Trip Timer has expired. When, however, the block from the Wideband Receiver is removed, C25 must discharge slowly through R98. For this case, the time constant is 46 mS, for which period C25 sustains the block condition at the input to IC5C. This method provides the time needed to dissipate the energy stored in the Narrowband Receiver by the original trip signal, and so a false trip is prevented.

(h) External Block

A logic high applied to Terminal 1 will block trip output from the Receiver. It enters the same logic path used for "has tripped" information. The facility is provided for diagnostic purposes and routine testing.

TABLE 1. COMPONENTS FOR DETERMINING FREQUENCY

GROUP	CENTER-FREQ. OF SUB-CHANNEL Hz	CHANNEL SPACING Hz	MODE AND FREQ. Hz	TRANSMITTER: CRYSTAL: SUFFIX FOR XTAL P/N HA-41034-	TRANSMITTER: CRYSTAL: FREQ. MHz	TRANSMITTER: CRYSTAL: CIRCUIT POSITION	TRANSMITTER: CRYSTAL: JUMPER POSITION	TRANSMITTER: BANDPASS-FILTER FREQ. DETER. NETWORK: P/N FOR POSITION RZ1	TRANSMITTER: BANDPASS-FILTER FREQ. DETER. NETWORK: P/N FOR POSITION RZ2	WIDEBAND RECEIVER: INPUT FILTER P/N	WIDEBAND RECEIVER: DISCRIMINATOR NETWORK P/N	WIDEBAND RECEIVER: POSITION IN CARD CAGE (NOTE 1)	NARROWBAND RECEIVER: BEAT FREQ. Hz	NARROWBAND RECEIVER: SUFFIX FOR XTAL P/N HA-41034-	NARROWBAND RECEIVER: CRYSTAL FREQ. MHz	NARROWBAND RECEIVER: JUMPER POSITION	NARROWBAND RECEIVER: RZ1 NETWORK PART NUMBER
1	A 935	340	T 860 G 1010	–7 –8	3.522560 4.136960	Y1 Y3	A	HB-41065-1		HB-74200-1	HB-74300-1	A	1200	–5	2.45760	F	HB-41064-1
	B 1275	340	G 1200 T 1350	–5 –6	2.457600 2.764800	Y4 Y2	F		HB-41065-2	HB-74200-2	HB-74300-2	B	1010	–8	4.13690	A	HB-41064-1
2	A 1275	340	T 1200 G 1350	–5 –6	2.457600 2.764800	Y1 Y3	B	HB-41065-2		HB-74200-2	HB-74300-2	A	1540	–9	3.15392	F	HB-41064-1
	B 1615	340	G 1540 T 1690	–9 –10	3.153920 3.461120	Y4 Y2	F		HB-41065-3	HB-74200-3	HB-74300-3	B	1350	–6	2.76480	F	HB-41064-1
3	A 1615	340	T 1540 G 1690	–9 –10	3.153920 3.461120	Y1 Y3	B	HB-41065-3		HB-74200-3	HB-74300-3	A	1880	–11	3.85024	F	HB-41064-1
	B 1955	340	G 1880 T 2030	–11 –12	3.850240 4.157440	Y4 Y2	F		HB-41065-4	HB-74200-4	HB-74300-4	B	1690	–10	3.46112	F	HB-41064-1
4	A 1955	340	T 1880 G 2030	–11 –12	3.850240 4.157440	Y1 Y3	B	HB-41065		HB-74200-4	HB-74300-4	A	2220	–13	4.54656	F	HB-41064-1
	B 2295	340	G 2220 T 2370	–13 –14	4.546560 4.853760	Y4 Y2	F		HB-41065-5	HB-74200-5	HB-74300-5	B	2030	–12	4.15744	F	HB-41064-1
5	A 2295	340	T 2220 G 2370	–13 –14	4.546560 4.853760	Y1 Y3	B	HB-41065-5		HB-74200-5	HB-74300-5	A	2560	–3	2.62144	E	HB-41064-1
	B 2635	340	G 2560 T 2710	–3 –4	2.621440 2.775040	Y4 Y2	G		HB-41065-6	HB-74200-6	HB-74300-6	B	2370	–14	4.85367	F	HB-41064-1
6	A 2635	340	T 2560 G 2710	–3 –4	2.621440 2.775040	Y1 Y3	C	HB-41065-6		HB-74200-6	HB-74300-6	A	2900	–1	2.96960	E	HB-41064-1
	B 2975	340	G 2900 T 3050	–1 –2	2.969600 3.123200	Y4 Y2	G		HB-41065-7	HB-74200-7	HB-74300-7	B	2710	–4	2.77504	E	HB-41064-1
7	A 2975	340	T 2900 G 3050	–1 –2	2.969600 3.123200	Y1 Y3	C	HB-41065-7		HB-74200-7	HB-74300-7	A	3240	–15	3.31776	E	HB-41064-1
	B 3315	340	G 3240 T 3390	–15 –16	3.317760 3.573760	Y4 Y2	G		HB-41065-8	HB-74200-8	HB-74300-8	B	3050	–2	3.12320	E	HB-41064-1
8	A 935	680	T 785 G 1085	–17 –18	3.215360 4.444160	Y1 Y3	A	HB-41065-9		HB-74200-9	HB-74300-9	A	1465	–19	3.00032	F	HB-41064-2
	B 1615	680	G 1465 T 1765	–19 –20	3.000320 3.614720	Y4 Y2	F		HB-41065-10	HB-74200-10	HB-74300-10	B	1085	–18	4.44416	A	HB-41064-2
9	A 1615	680	T 1465 G 1765	–19 –20	3.000320 3.614720	Y1 Y3	B	HB-41065-10		HB-74200-10	HB-74300-10	A	2145	–21	4.39296	F	HB-41064-2
	B 2295	680	G 2145 T 2445	–21 –22	4.392960 5.007360	Y4 Y2	F		HB-41065-11	HB-74300-11	HB-74300-11	B	1765	–20	3.61472	F	HB-41064-2
10	A 2295	680	T 2145 G 2445	–21 –22	4.392960 5.007360	Y1 Y3	B	HB-41065-11		HB-74200-11	HB-74300-11	A	2825	–23	2.89280	E	HB-41064-2
	B 2975	680	G 2825 T 3125	–23 –24	2.892800 3.200000	Y4 Y2	G		HB-41065-12	HB-74200-12	HB-74300-12	B	2445	–22	5.00736	F	HB-41064-2

(1) There are two receiver cards per group, one for subchannel A and one for subchannel B. Positions shown are for both wideband and narrowband receiver at their respective locations. Do NOT place narrowband receiver cards in wideband locations, and vice versa.

Table of Replaceable Parts

DIAGRAM SYMBOL	NAME OF PART AND DESCRIPTION	PART NO.
C1, 2	Capacitor, silvered mica, 56 pF, 5%, 500 V, Electro Motive DM-15, or eq.	HA-16517
C3	Capacitor, tantalum, 15 μF, 20%, 20 V, Kemet 1314D227M010AS, or eq.	H-1007-716
C4, 5, 23, 24	Capacitor, tantalum, 1 μF, 20%, 35 V, Kemet T324A473N035AS, or eq.	H-1007-496
C6, 11, 12	Capacitor, silvered mica, 33 pF, 5%, 500 V, Electro Motive DM-15, or eq.	HA-16511
C7, 8, 9, 10	Capacitor, poly., 0.022 μF, 2%, 100 V, Wesco 32P, or eq.	H-5115-51
C13, 14	Capacitor, MPC, 0.56 μF, 2%, 100 V, Wesco 32MPC, or eq.	H-1007-1330
C15, 16	Capacitor, poly., 0.01 μF, 2%, 100 V, Wesco 32P, or eq.	H-5115-135
C17, 18	Capacitor, MPC, 0.033 μF, 2%, 100 V, Wesco 32 MPC, or eq.	H-1007-1328
C19, 20	Capacitor, poly., 0.18 μF, 2%, 100 V, Wesco 32P, or eq.	H-5115-97
C21	Capacitor, metallized mylar, 1 μF, 2%, 100 V, Wesco 32 MM, or eq.	H-1007-795
C22	Capacitor, silvered mica, 47 pF, 5%, 500 V, Electro Motive DM-15, or eq.	HA-16515
C25	Capacitor, mylar, 0.1 μF, 10%, 50 V, TRW 601PE Slim-Line, or eq.	H-1080-304
C26, 27	Capacitor, 0.22 μF, 2%, 50 V, Wesco 32 MPC, or eq.	H-1007-1329
CR1 thru 20	Diode, silicon, 1N914B	HA-26482
IC1	Integrated circuit, balanced modulator, Motorola MC1496G, or eq.	H-0620-110
IC2	Integrated circuit, 12-stage, ripple-carry binary counter/divider RCA CD4040AE, or eq.	H-0620-21
IC3, 8 thru 17	Linear opamp, dual National LM-1458N, or eq.	H-0620-51
IC4	Integrated circuit, hex buffer inverter, RCA CD4049AE, or eq.	H-0615-7
IC5	Quad, 2-input NAND gate, RCA CD4011AE, or eq.	H-0615-5
IC6	Triple, 3-input NOR gate, RCA CD4021AE, or eq.	H-0615-20
IC7	Quad, 2-input NOR gate, RCA CD4001AE, or eq.	H-0615-3
R1 thru 18, R20 thru 35, R37 thru 88, R90 thru 100	Resistor, metal-film, precision 1%, 1/8 W, 100 PPM/DEG C, Type RN55D per RFL spec HA-38301	H-1510-(XXX)
R19, 36	Resistor, variable, 10 K, 10%, ¾ W, Helipot 79PR10K, or eq.	HA-39539
R89	Not used	
RZ1	Resistor, network assembly, exact specification dependent upon channel spacing	HB-41064-(X)
Y1	Crystal, piezoelectric, frequency per channel assignment	HA-41034-(X)

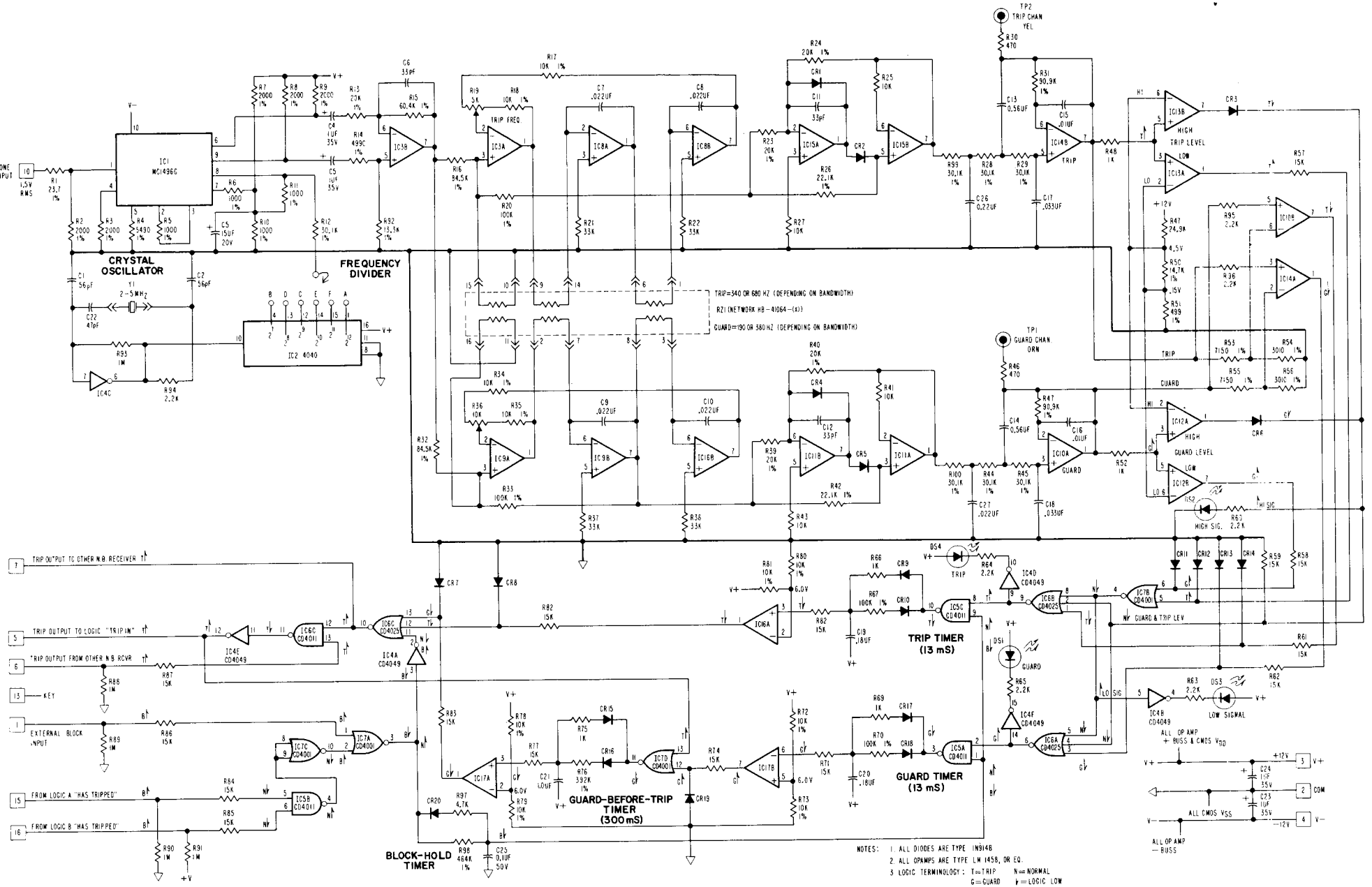

Figure 3. Schematic of Narrowband Receiver for one sub-channel