

LOGIC POWER SUPPLY

Printed Circuit Board Schematic	Drawing 3465D95
Overall Power Supply Schematic	Drawing 3465D87
Power Board and Pegboard Wiring Diagram	3466D35G01
PCB Main Wiring Diagram	3466D30G01
PCB Slave Assembly Wiring Diagram	3466D30G02
Functional Block Diagram	491B512

FUNCTION

The logic power supply is designed to operate from an input voltage ranging between 175 and 320 volts, and to hold regulated logic output voltages above 200v. This eliminates the need for awkward logic battery and charger circuitry, by assuring logic power for any possible survival condition of the inverter.

The power supply is completely self-contained in a frame within the logic drawer. A single input fuse protects the entire logic supply. A single plug makes all external connections, including the logic voltages +20, -20, +40, and SWA-SWB for all logic boards.

OPERATION

The operation of the logic power supply may be best understood by considering separately the following functional component groups.

I. +20 Volt Regulated Power Supply

A. General Description of Operation

1. The 175 to 320 VDC supply is applied first between +P1 and -P5 to limit inrush current for charging of capacitor 10C1 then to +P3 and -P5 after the main breaker is closed.
2. At XA1, the commutating capacitor 11C1 will now charge to the positive input DC voltage.
3. XA2 voltage is sensed by the undervoltage circuit and if it is larger than 175 VDC, it applies a + voltage to the input of the voltage regulator XA9 to turn it on. If the voltage at XA2 is less than 175 VDC or drops below 175 VDC, the undervoltage circuit will prevent the pulse generator from operating, thereby preventing a power supply output voltage. The zener 4Z clamps the voltage to provide a constant reference to the voltage regulator.
4. The input to the pulse generator becomes an exponential ramp at XA4, determined by the 16R1, 15VR1, and 13C1 time constant and the voltage regulator output charging voltage at XA3.
5. The unijunction firing circuitry in the pulse generator provides a continuous row of pulses at XA5 at a frequency determined by the input time constant, adjusted in the factory by potentiometer 15VR1. (Approximately 1-2 KHZ)
6. The thyristor 13TH1 is gated on and draws current through the primary of 17T1 and allows it to flow through to P5 and around 11C1 - 14L1 resonant circuit. 11C1 is charged to an opposite polarity (+ on XA6 - XA1). The thyristor 13TH1, will turn off (commutation occurs) when the reverse resonant circuit current is greater than the load current.
7. The pulse of current through the primary of 17T1 induces a change of flux which develops secondary voltage of +20 on XA7 and -20 on XA8 with the center tap to common.
8. The +20 volts is fed back to the voltage regulator by way of the blocking oscillator in order to close the loop to the voltage regulator as well as supply isolation between the control and power circuits.

9. The input of the voltage regulator XA9 now compares the supply voltage with the feedback voltage. If we look at one increment of time and suppose that the +20 output voltage tries to drop for some reason, e.g. because more load was applied to P11, (the +20 output) the error voltage at XA9 would begin to increase because +20 tries to droop and begins to decrease voltage feedback, but the reference voltage from across 4Z is constant, so the turn-on voltage at XA9 increases. The voltage output of the voltage regulator thereby increases at XA3 and the charging rate to 13C1 increases the pulse generator frequency which increases the voltage at XA7 back to the original 20 volts.

In other words, any change in the output voltage is detected and compensated for as soon as there is a differential voltage at the base of the voltage regulator transistor 19Q.

The output is therefore maintained at a constant regulated +20 voltage setting, independent of changes in loads, as long as the power supply's output capacity is not exceeded.

B. Specific Circuits

a. DC/DC Converter:

The converter is a DC chopper comprising the following main parts: load transformer 17T1, thyristor switch 13TH1, and commutating circuitry 14L1-11C1 for thyristor turnoff.

The gating of the thyristors is provided by the pulse transformer 5T1, pulse-transistor 10Q, and unijunction transistor 14Q1. The control of the gating signal directly affects the operating frequency of the chopper. Additional components 8R1-12C1, and 7D2-9R1 perform surge suppression or clamping functions. The DC chopper operation may be seen as follows. Before the thyristor is turned ON, 11C1 charges to +300. When the thyristor is turned ON, the input +300 appears across the winding H1-H2 of the load transformer 17T1, initiating a flux change. At the same time, the resonant circuit 11C1-14L1 begins its discharge through the thyristors. This voltage which began at +300 will swing toward -300 (with respect to the anode of 13TH1) because of the L-C resonant effect. When the voltage swings negative, the thyristor turnoff takes place. When the thyristors are OFF, transformer 17T1 flux is reset, and the circuit returns to the original condition ready for the next cycle of operation. Repeated switching of 13TH1 therefore causes a relatively high frequency AC voltage to be produced, with the magnitude and

frequency established by the values of 14L1-11C1 and the gating circuit to be discussed. The higher the operating frequency, the greater will be the output voltage.

Two separate 20 volt supplies are derived from the secondary windings of transformer 17T1. The +20 supply is taken from winding X1-X2, rectified half wave by diodes 20D1-20D2, and filtered by 22L1-25C1. Surge suppression for the diodes is provided by 18C1-4R2. The extra winding section X2-X3 with diode 21D1 is part of a clamping circuit used during the flux resetting of transformer 17T1.

b. Voltage Regulation Section:

The +20 supply must be further regulated to hold the desired limits. A portion of the +20 is fed back to a voltage regulator, compared to a reference voltage, and the converter frequency adjusted to bring these voltages into balance. The voltage feedback must be isolated to provide proper regulator performance.

The reference signal is taken from zener diodes 4Z1-2-3-4, (For better drift stability, low-voltage units in series are utilized.)

Reference and feedback signals are compared at the base of transistor 19Q1. The reference voltage forward biases 19Q1, while the feedback voltage reverse biases 19Q1. As a result, the conduction of 19Q1 is determined by the difference, or error voltage.

The collector current of 19Q1 is used to charge capacitor 13C1 through 16R1 and 15VR1. When the voltage across 13C1 rises sufficiently, the unijunction transistor turns on, switching 10Q1 full ON. This then produces a gate pulse for firing thyristor 13TH1 of the DC/DC converter. By controlling the charging rate of 13C1, the repetition rate of the DC/DC converter is controlled, which in turn controls the +20 output voltage as desired.

c. DC Undervoltage Detector:

This circuitry is provided to assure proper starting and stopping of the DC/DC converter. When the input bus voltage is below 175 volts DC, the DC/DC converter is not permitted to start because there would be inadequate voltage for switching properly. Likewise, if the bus voltage falls below 175 volts during operation, the converter shuts down to avoid misfiring and fuse blowing. (An overlap of pickup and dropout voltage is actually used to avoid border-line operation.)

Voltage sensing is done by transistor 27Q1. Whenever the voltage at the emitter of the transistor 27Q1 is positive with respect to the base, the transistor turns ON to allow a current through 24R2 which sets up a blocking voltage to shut OFF or reverse bias the input transistor 19Q1 of the voltage regulator. Values of 29R1 and 28R1 of the voltage divider network are picked so that for 175 volts on terminal FS10, approximately 20 volts will be seen across 28R1 to back bias transistor 27Q1. For any voltage above 175 volts on FS10, the voltage across 28R1 increases to keep 27Q1 back biased or turned OFF, so that no blocking voltage will be developed across 24R2, thereby allowing the power supply to function.

d. Blocking Oscillator:

The blocking oscillator is utilized to provide the desired isolation. A portion of the +20 output is fed back by the divider network 35R1, 36R1, 22D7, 12R3. The blocking oscillator is comprised of transistor 37Q1, transformer 33T1, and timing capacitor 34C1.

When the circuit is energized, the forward bias on 37Q1 turns it ON. Voltage appears across 33T1 winding 1-2, which produces in winding 3-4 a charging current for 34C1 in a direction to reinforce the base drive of 37Q1.

When transformer 33T1 saturates, the winding voltages disappear. Capacitor 34C1 now begin to discharge in the reverse direction, removing the base drive from 37Q1, turning it OFF. 37Q1 will remain OFF until 34C1 discharges to a value below the 37Q1 forward bias, at which time the cycle repeats.

The output of the blocking oscillator is taken from winding 5-6, rectified by diode 22D5 and stored on 30C1. A dividing network of 31VR1 and 32R1 permits adjustment of the amount of feedback to be used. 31VR1 thereby can be used to adjust the level of the +20 supply.

II. -20 Volt Supply

The -20 volt supply is of much lower capacity, and is taken from 17T1 winding X2-X4, rectified full wave by diodes 19D1-2-3, and filtered by 23L1-26C1. The output of this circuit is further regulated by 28R1 and the zener diode 27Z1.

III. a. Square-Wave Supply

The square-wave voltages SWA-SWB are derived from the +20 power supply, by means of a modified Royer inverter. This inverter consists of transformer 34T1, transistors 33Q1 and 33Q2, plus their associated components. The +20 is applied to the center tap of 34T1.

With 33Q1 turned ON (See "Start Sequence Circuit" sheet 7), current flows in 34T1 from 3 to 2, through 33Q1 to COMMON. The voltages induced in winding 3-8 reverse biases 33Q2, keeping 33Q2 turned OFF. Winding 2-1, however, has a voltage in such a direction as to reverse bias the base of 33Q1. After transformer 34T1 saturates, voltages on windings 2-1, 8-3, and 12-8 drop to 0 and 33Q1 turns off. The collapse of this current produces transformer voltages which turn ON transistor 33Q2. Then the current from +20 goes through 3-8, 33Q2, to COMMON, until a similar action ensues on this side of the circuit. The voltages taken from terminals 2 and 8 are the desired square-wave voltages SWA and SWB. Note that both of these are tied to +20 by terminal 3 on 34T1. In this way, the +20 lead acts as a neutral for the square-wave supply. The use of transistor 49Q1 avoids the need for a high-power resistor in the starting circuitry.

b. The +40 Supply

The +40 supply is derived simply from the square-wave rectifier configuration. Diodes 53D1 and 53D2 produce the 20 volt DC output, which is filtered by 32L1 and 26C2. Because of the center-tap connection to the +20 source, the output voltage of this supply is 20 volts above +20, hence serves as the +40 supply.

IV. Start Sequence (Hold-Off Circuitry)

The DC supply power is applied to the logic power supply before it is applied to the inverter stages. Input capacitors must be charged and input breaker ICB closed in before DC power can be applied to the stages. During the interim, after the logic power supply starts and before the DC power is applied to the stages, it is extremely important that the ring counter be set to fire the proper stage thyristor while the rest of the stages are in a hold-off condition. It is best to allow the ring counter to cycle at least once to gate the thyristors without having supply voltage on them.

The precondition cycling action removes any residual flux on the gate modulator pulse transformers and resets them so that false firing wouldn't occur when power is first applied.

It is the purpose of the Start Sequence circuitry to provide the necessary control to cycle all thyristors and reset to the proper starting thyristor. This is done during the first 3 seconds after power is applied to the logic power supply. The start sequence circuitry is so designed that there is about a 3 second delay before there is a holdoff signal of +20 V. applied on terminal FS9. The +20 holdoff voltage is fed to terminals U8 and U15 of the counter board and to U6 and U15 of the counter driver boards. The +20 V holdoff voltage U15 and U6 will prevent the operation of that counter-driver board but the +20 holdoff voltage on U8 will set up that counter-driver board to receive the first pulse from the frequency oscillator and thereby provide the first signal to gate ON the first thyristor as soon as the +20 V holdoff is removed. The holdoff is removed magnetically by the ST time delay relay which breaks contact between the logic power supply and the counter-driver board when the rest of the system is ready to operate.

The details of the circuit operation are as follows. After the power supply starts, +20 volts is applied to terminal FS1. 27QZ is immediately biased on which turns on 49Q1 which starts the square wave generator by turning on 33Q2. After approximately 3 seconds, capacitor 39C1 charges up and zener diode 41Z1 breaks over to turn ON 43Q1 which gates thyristor 46TH1. The output of 46TH1 reverse biases 27Q2 to remove the square wave start reference and provides +20 volts to FS9.

V. Dual Logic Power Supply

The dual logic power supply uses essentially two (2) single power supplies in parallel. See Drawing 3465D87 for interconnection wiring. The only difference is in the fact that all printed circuit board components are not necessary in the paralleled or slave power supply. The slave printed circuitry can follow the master printed circuitry. Therefore, the slave power supply printed circuit board (3465D95) has considerably less components.

The two (2) power supplies are connected in such a way (drawing 3465D87) to stop both supplies and ultimately the inverter, should either one of them have a failure. The fuse 16F1 supplies the individual thyristors (13TH1) but the input voltage to the master supply at FS10 is supplied after the slave's fuse 16F1. As a result, if the slave's main fuse 16F1 blows, the master supply loses its power to terminal FS10 and shuts down by undervoltage shutdown. Note that the gating signal for the slave supply comes from FS11 of the master supply, such that if the master supply's fuse 16F1 blows, the main reference is lost to terminal FS13 which shuts down the master pulse generator which in turn shuts down the slave pulse generator.

VI. Testing

Correct operation of the logic power supply may be verified by measuring the several output voltages for their proper values.

<u>Source</u>	<u>Nominal</u>	<u>Acceptable</u>	<u>Single PS Capacity</u>	<u>Dual P.S.</u>
Input	300 V	175-320 V	1.0 A	2.0 A
+20	20 V	19-21 V	2.0 A	4.0
-20	20 V	18-21 V	250 MA	500 MA
SWA-SWB	80 V P-P	70-80 V P-P	150 Watts	300 W
+40	40 V	36-40 V	0.8 A	1.6 A

All sources have been set on the test floor to their proper value, and should normally not require field adjustment.

VII Trouble-Shooting

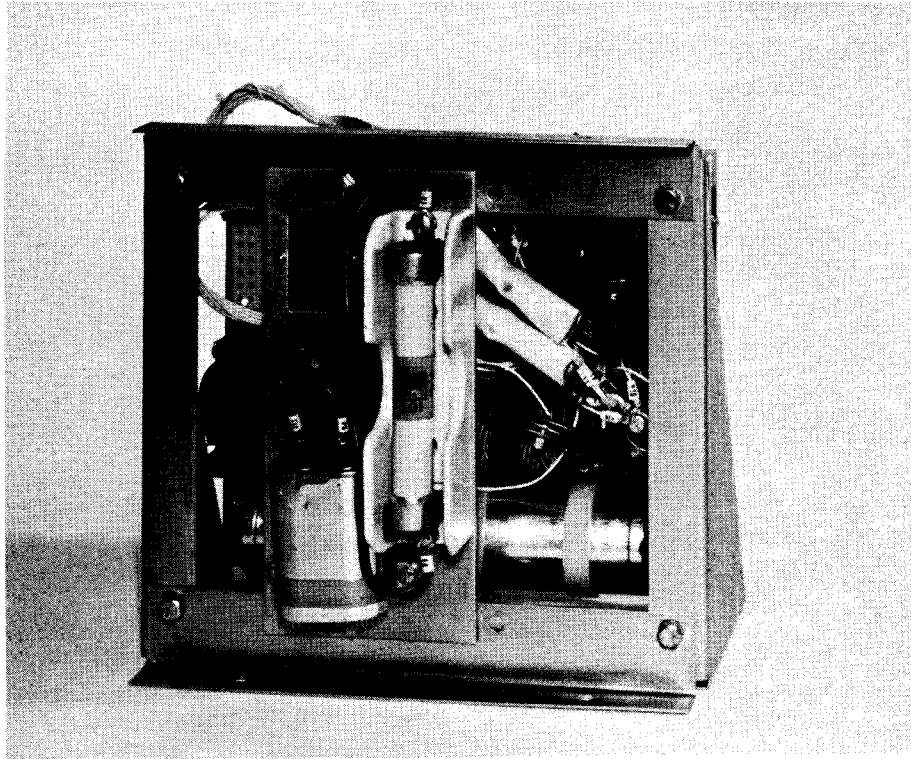
The logic power supply is designed for easy replacement, in the event of trouble. Removal of a single plug connection and four screws will permit substitution of a spare supply. Before making replacement, however, one should determine definitely that the trouble lies internal to the supply, and not external.

Certain clues may help in isolating trouble within the supply.

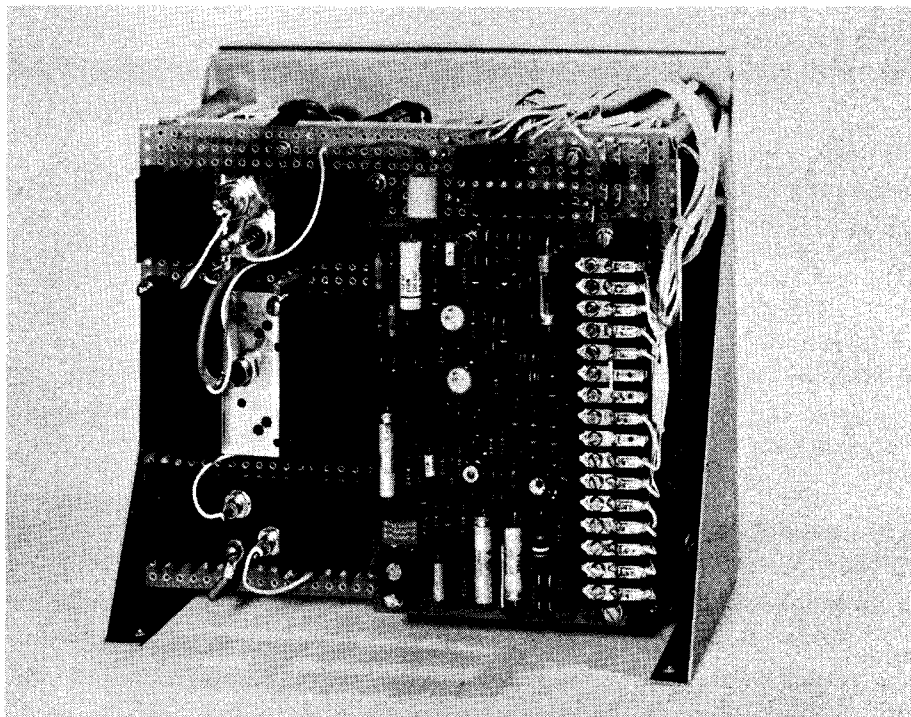
- a. The absence of -20 only, points to the components 19D2, 19D3, 27Z1, 23L1, 26C1, etc., associated with this supply.
- b. The absence of +40 only, likewise points to components in that section only, since +40 is derived from the square-wave supply.
- c. The absence of both +40 and SWA-SWB suggests that the square-wave supply is the source of trouble.
- d. If the absence of all voltages suggests trouble in the +20 supply if the converter is functioning, or in the converter circuitry otherwise. (The converter makes an audible sound when working.)
- e. If the converter is not functioning at all, check for:
 1. Presence of 300 volts DC input
 2. Presence of input fuse 16F1

Otherwise, replace the supply and make a thorough bench check to find out the internal trouble.

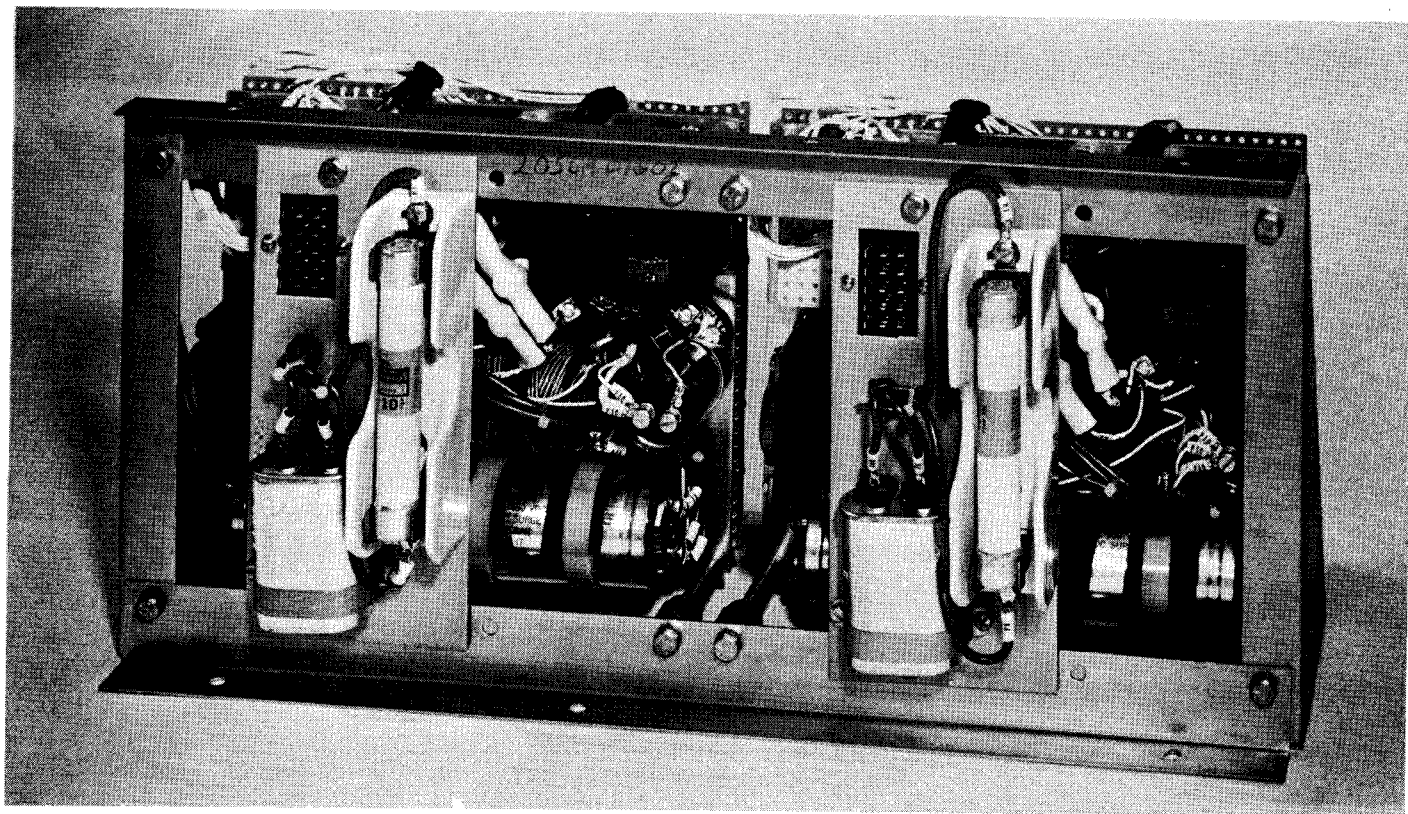
CAUTION: Input fuse is Chase Shawmut A60X10, and must not be replaced by any other fuse without specific authorization in writing from Westinghouse. Use of improper fuse may result in serious damage to the logic power supply.



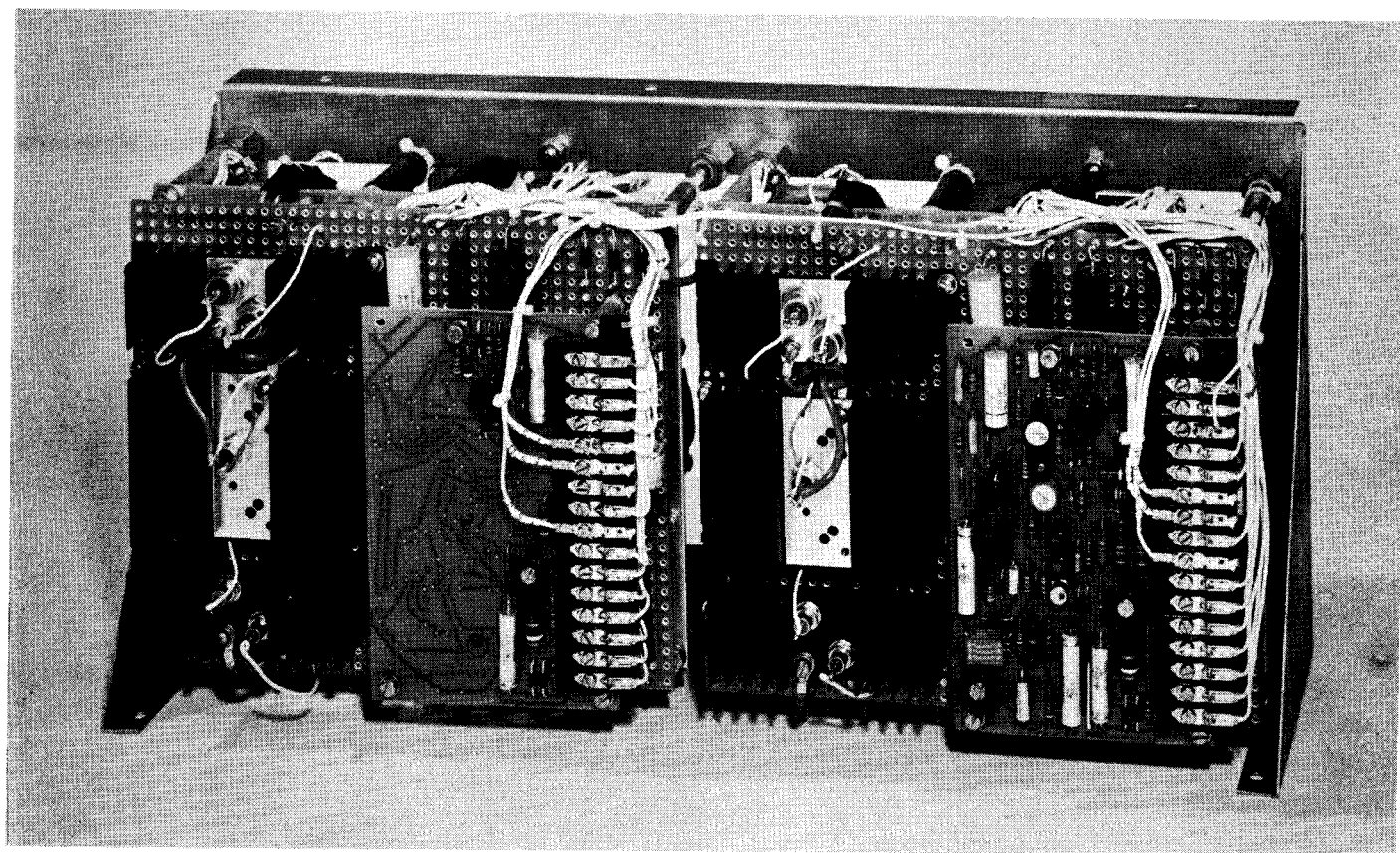
(Front View)



(Rear View)



(Front View)

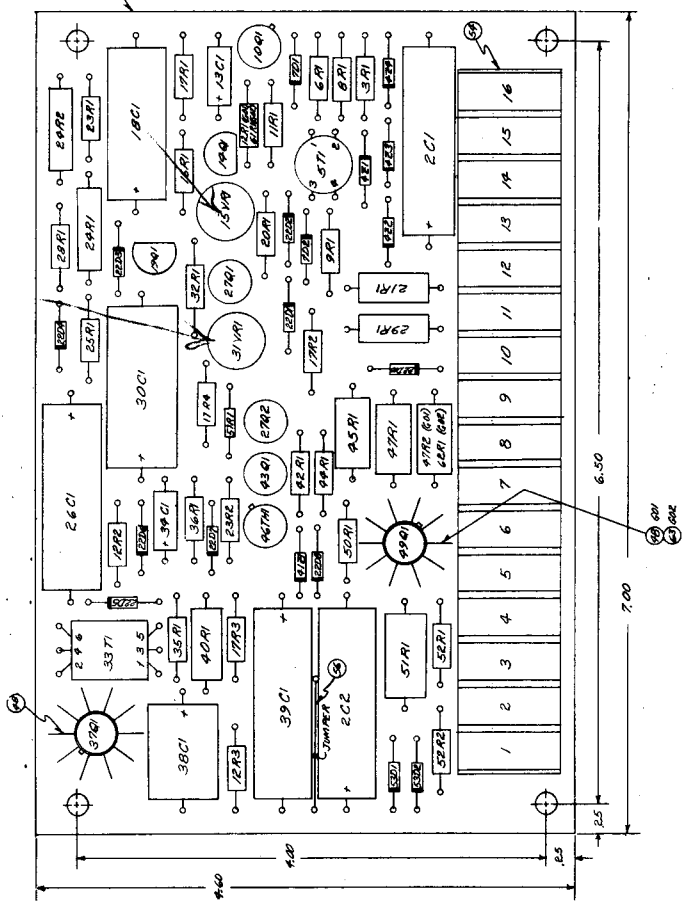


(Rear View)

REF. DWG'S
SCHEMATIC & PAGES
P.C. BOARD DIM. & PARTS
COMPLETE DIM. SUPPLY
MASTER & M. BOARD

20

MAX. FREQ



- NOTES
- 1) BOARD TO BE RUN SOLDERED AFTER ASSEMBLY.
 - 2) BOARD TO BE COVERED WITH PROTECTIVE WAXEN 36012B AFTER TEST.
 - 3) STYLE NUMBER / GAMP TO BE STAMPED ON BOARD.

TITLE: LOGIC POWER SUPPLY CONTROL			
PRINTED CIRCUIT BOARD ASSEMBLY DIMENSIONS			
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WESTINGHOUSE ELECTRIC CORPORATION
TITLE: LOGIC POWER SUPPLY CONTROL
PRINTED CIRCUIT BOARD ASSEMBLY DIMENSIONS
REVISIONS IN INCHES - SCALE
DATE: 10/1/68
BY: WES
CHECKED: J. B. GIBSON
APPROVED: J. B. GIBSON
DESIGN: J. B. GIBSON
DRAWN: J. B. GIBSON
MATERIALS: J. B. GIBSON
TESTING: J. B. GIBSON
PACKAGING: J. B. GIBSON
SHIPPING: J. B. GIBSON
STORAGE: J. B. GIBSON
DISPOSAL: J. B. GIBSON
REWORK: J. B. GIBSON
REPAIR: J. B. GIBSON
REUSE: J. B. GIBSON
RECYCLE: J. B. GIBSON
RECLAIM: J. B. GIBSON
REMANUFACTURE: J. B. GIBSON
RECONSTRUCT: J. B. GIBSON
REBUILD: J. B. GIBSON
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93	REVISION	10/1/68	WES
94	REVISION	10/1/68	WES
95	REVISION	10/1/68	WES
96	REVISION	10/1/68	WES
97	REVISION	10/1/68	WES
98	REVISION	10/1/68	WES
99	REVISION	10/1/68	WES
100	REVISION	10/1/68	WES

