COUNTER/DRIVER BOARD

Schematic Diagram 3450D31
Printed Circuit Assembly 668C407

FUNCTION

The counter/dirver board is a printed-circuit logic board, located in the logic drawer, and plug removable from it. Each such board is associated with one dual-stage drawer. Its function is to receive properly shaped signals from the AFO (adjustable frequency oscillator) board, and to produce the necessary gate control signals to be sent to the inverter stage.

Mechanically, the board consists of two halves which are virtually identical, each half controlling one inverter stage. The discussion will be confined to the operation of one of these halves. Schematic diagram 3450D31 shows the circuitry for this board.

A. Two separate and distinct functions are provided by the counter/driver board. First, the circuitry associated with transistors Q21 through Q24 forms a section of a ring counter. The function of the ring counter is to receive synchronizing signals from the AFO or PG, and to distribute these signals to the proper inverter stages, in the proper sequence, and with the proper timing. It will be recalled from "Basic Theory" that all stages receive identical signals, except that each is delayed a fixed number of degrees from its neighbor. (The delay is set by 360 degrees divided by 2N, where N is the number of stages used.) In the case of a six-stage inverter, the gate control signals must be delayed 30 degrees from each other. It is the function of the ring-counter to assure this phase displacement between stages.

B. The second part of this logic board is the Driver section. There are two Driver sections for each Counter section; one Driver produces a pair of gate control signals for the left-hand pair of thyristors in the inverter stage, while the other Driver produces a pair of gate control signals for the right-hand pair of thyristors. In either case, the "pair" of gate control signals must be complementary to avoid misfiring the inverter; i.e. when GC1 is ON, then GC2 is OFF, and vice-versa. The duration of the gate control signals must be controllable by a pulse-width control signal, PWC. This is necessary in order to control the voltage output of each inverter stage, as required by the voltage regulator. (Refer to "Basic Theory" for description of voltage control by pulse-width control.)

OPERATION

A. Ring Counter Section

Each counter/driver board contains two identical sections. Each section contains a transistor flip-flop, controlled by certain logic signals. The flip-flop sections are interconnected in a ring, so as to successively pass a logic signal around the ring. Synchronization of this shifting of the logic signal is achieved by a COUNT (U10) signal derived from the AFO or PG. The result is that a logic signal is passed around the ring in synchronization with the master oscillator. The output signals taken from each section of the ring are then used to control the inverter stage via the driver sections.

Transistors Q22 and Q23 form a bi-stable flip-flop, whose ON or OFF state may be reversed by logic signals applied to their bases. Assume that in the normal or quiescent state, Q22 is in the full ON state. For this condition, transistor Q23 is reverse biased, and therefore is in the full OFF state. If the base of Q22 receives a negative signal input via diode D47, this will reverse bias Q22 causing it to turn OFF, which action will also cause transistor Q23 to turn ON. The result of the negative signal at the input of Q22 has been to reverse the state of the flip-flop. Further negative signals at this point will have no effect, since the unit is already switched OFF. Switching control now passes to the input of transistor Q23 via diode D49, since a negative input signal here will produce a change of state.

Two logic signals are connected to the bases of the flip-flop; first, a COUNT signal (U10) derived from the AFO; and secondly, a logic signal (SHIFT INPUT) received from the preceding ring-counter section. The COUNT signals are fed continuously to the flip-flop at a rate set by the AFO or PG. A change of state, however, will only occur when the SHIFT INPUT signal is absent. As long as the SHIFT INPUT signal is present, then diode D47 or diode D49 will be blocked, preventing a change of state from occurring as a result of the smaller negative COUNT signals. The state of the flip-flop is detected by resistors R77 and R82 at the collectors of Q22-Q23. These detected signals are utilized to control the gating of the succeeding ring-counter section.

Transistors Q21 and Q24 act as emitter followers to produce output signals to the driver sections. In this way, isolation from the ring counter directly is maintained. Note that Q21 will always have the same state as Q22, and likewise Q24 will have the same state as Q23. Note further that a HOLDOFF control signal at the emitter of Q21, via D45, can prevent passing the output of Q21 on to the driver section. This may be used as an external HOLDOFF control for interlocking purposes.

B. Driver Section

Recall that the function of the Driver section is to produce output pulses in synchronism with the Counter section, and with a controllable pulse-width determined by the external signal PWC. This function may best be considered in three steps: input switching, bias control by PWC, and output switching.

The input switching function is provided by transistors Q3 and Q4. With no input signal from the Counter section, Q3 is forward biased ON from +20 through R1-R2-D2-R7. With Q3 ON, the base drive to Q4 turns Q4 OFF. Consider this the normal condition.

The input signal from the Count section is a negative going pulse (positive pulses are blocked by D1) applied to the base of Q3 through C17-R5-D1-D2. This action will cause Q3 to switch OFF and Q4 to switch ON. In this manner, the switching of Q3-Q4 is initiated in synchronism with the counter section. The duration of this state is determined by the bias control of PWC, before Q3 and Q4 revert to the original state ready for the next input pulse.

The bias control of PWC is governed by capacitor C2 and certain voltage-clamping devices. With no input signal, Q3 is in the ON condition, and capacitor C2 begins to charge toward +40 volts through R3-C2-D2-Q3 to common. As soon as the upper end of C2 rises above the voltage of PWC, however, diode D4 clamps and prevents any further voltage rise. The lower end of C2 is connected to Common via D2-Q3.

Now when an input pulse from the Count section causes Q3 to switch OFF and Q4 to switch ON, capacitor C2 no longer is clamped to Common. The upper end of C2 is now clamped to common by D3-Q4, so its lower end shifts negative by the amount of C2 voltage originally set by PWC. The negative voltage of C2 keeps Q3 reverse biased even after the input pulse disappears. It will continue to hold Q3 OFF until the negative voltage of C2 discharges. At that time, the reverse bias of Q3 disappears, and it returns to the original ON state. Likewise, Q4 returns to the original OFF state. The output of this section is sensed from the collector of Q4, and test point TP1 is connected to this point.

The output switching is provided by transistors Q1, Q2, and Q5. The object is to produce two complementary output pulses at GC1 and GC2, electrically isolated from the previous section.

The output at GC1 is produced by transistor Q1, which connects GC1 to the (+20) bus when Q1 switches ON. When Q1 is OFF, then GC1 is at +40. Switching of Q1 is determined by its base drive, which is normally forward biased from (+40) through R9 to (+20). However, when Q4 turns ON, its collector drops to common pulling Q1 out of conduction. The overall result is that Q1 switches complementary to Q4.

The output of GC2 is produced by transistor Q2, which acts as an ON/OFF switch connecting GC2 to (+20)/(+40) respectively. This transistor cannot be driven directly from Q14 as before, because GC2 must be complementary to GC1. For this reason, a phase-inversion transistor Q5 is interposed.

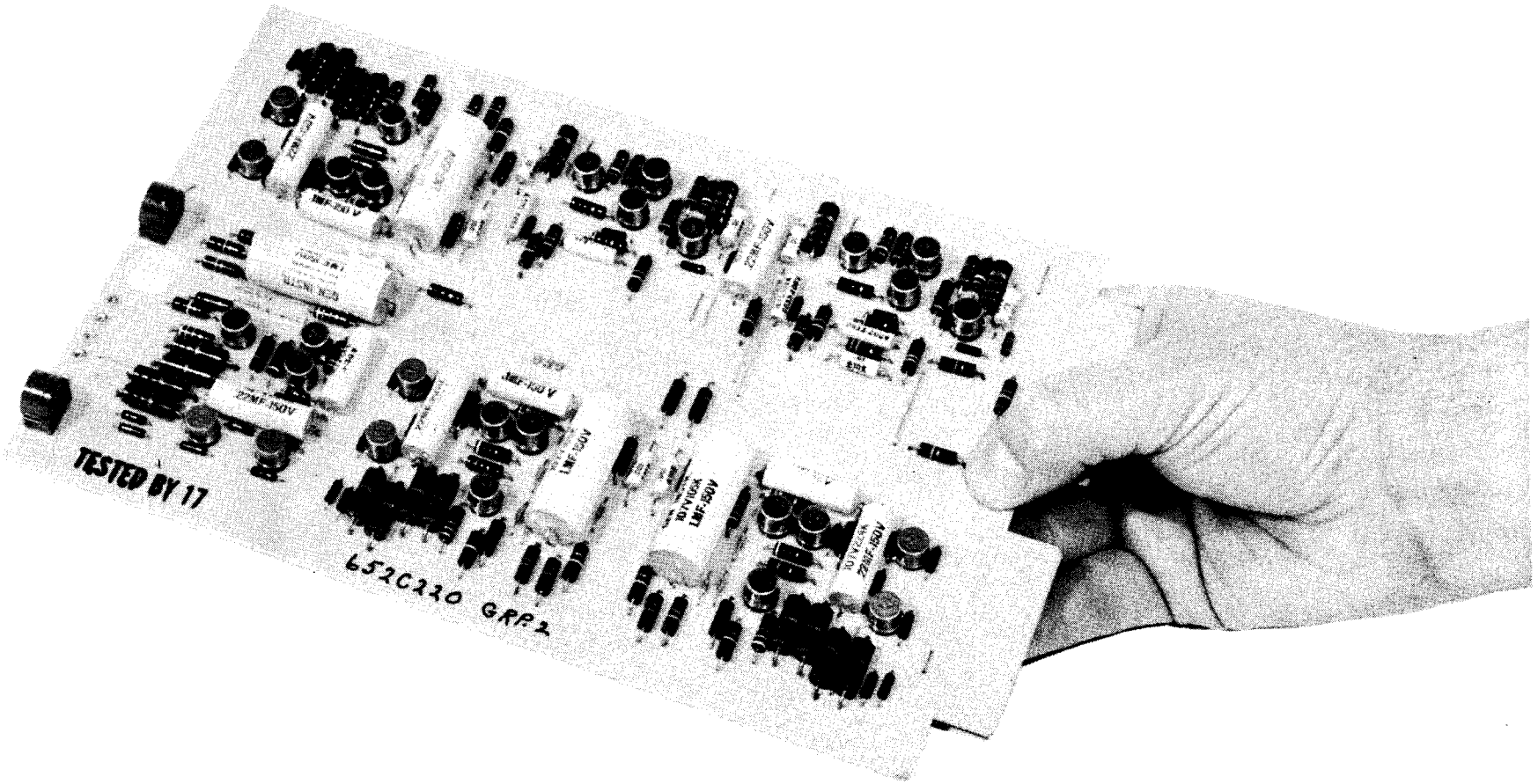
Transistor Q5 is driven by the output of Q4, and will switch ON when Q4 is OFF, and vice versa. The output of Q5 goes to the base of Q2. When Q5 is ON, the base of Q2 is reverse biased and OFF. When Q5 turns OFF, the reverse bias is removed from Q2 and Q2 turns ON. The overall result is that Q2 switches in phase with Q4.

This completes the desired objective of producing complementary output pulses in synchronism with the Counter section, and with pulse-width controlled by an external signal PWC. The second driver section on this board does exactly the same thing, except displaced 180 degrees. Since this second section gets its counter signal from the opposite side of the counter's flip-flop, the 180 degree displacement is assured. Figure 1 shows the waveform outputs of each counter section, used to control one complete inverter stage.

TESTING

Test points are brought to the front of each Counter driver board for convenience in connecting an oscilloscope probe. Each test point is isolated by a 100 K resistor. The four test points are referenced to COMMON, and display a gate-control signal for each half of the two inverter stages contained in one drawer.

Only one adjustment is required for each inverter stage controlled by a counter/driver board. This is a BALANCE (1P) adjustment that assures equal positive and negative half-cycles of the inverter stage output. If this adjustment is not made within certain limits, the half-cycles may be unbalanced resulting in a DC component to the stage output. If this DC component is excessive, it will cause transformer saturation and stage misfiring. The unbalance in any complete cycle should not exceed 0.3 volts DC.



COUNTER/DRIVER BOARD

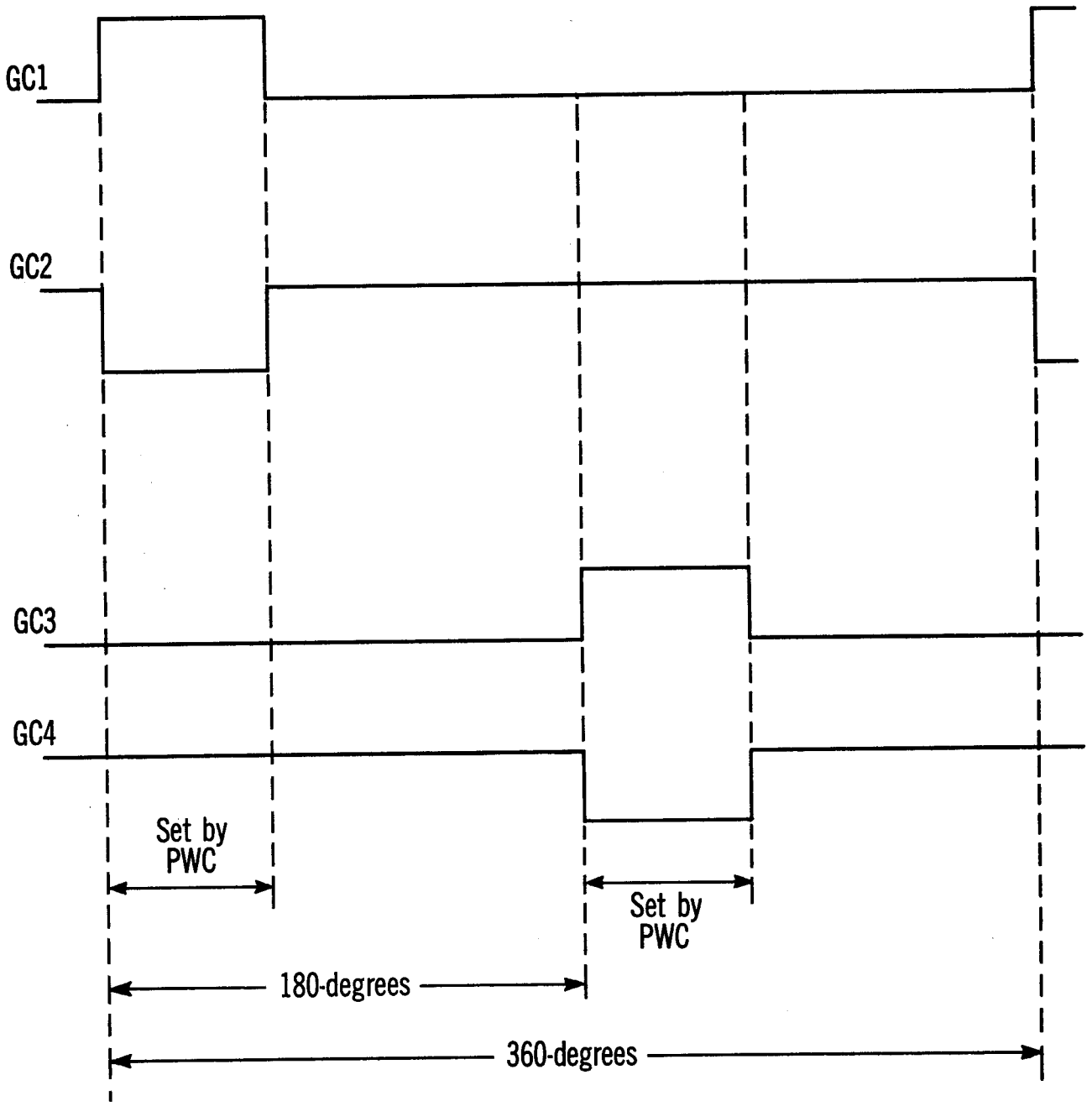
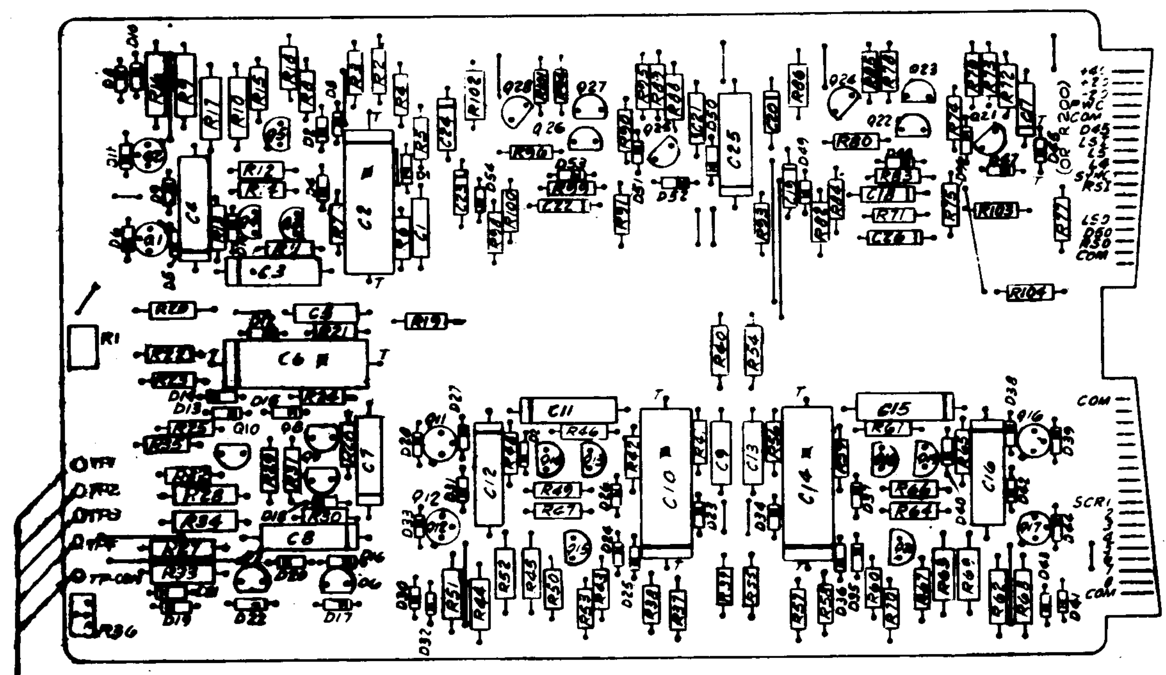


FIGURE 1 - TYPICAL WAVESHAPES OF GATE CONTROL OUTPUT SIGNALS FROM COUNTER/DRIVER BOARD

DWG 668C407 SUB 2



NOTE: BOARD TO BE FLOW SOLDERED AFTER ASSEMBLY
BOARD TO BE COATED WITH PROTECTIVE VARNISH 32101JB AFTER TESTING TO SPECIFICATION 480A783
GROUP * TO BE STAMPED ON BOARD AFTER FINAL ELECTRICAL TEST

Δ-CONSTRUCTION PER BOARD DIMENSION OF DWG. 648C600

APPLICATION NOTE 486A800

TEST POINTS
TURRET LUGS

B/M 2044A61

SUPERSEDES 652C220

S.O.	IT.	CHANGE
66222M	1	FUTURE TUR. LUGS FOR Δ D45 OR R200 WERE NOT SHOWN. SPEC S.L. 5-14-69 ADDED W.R. Wellham 5.15.69

WESTINGHOUSE ELECTRIC CORPORATION

TITLE: ... COUNTER DRIVER BOARD ASSY

DIMENSIONS IN INCHES – SCALE

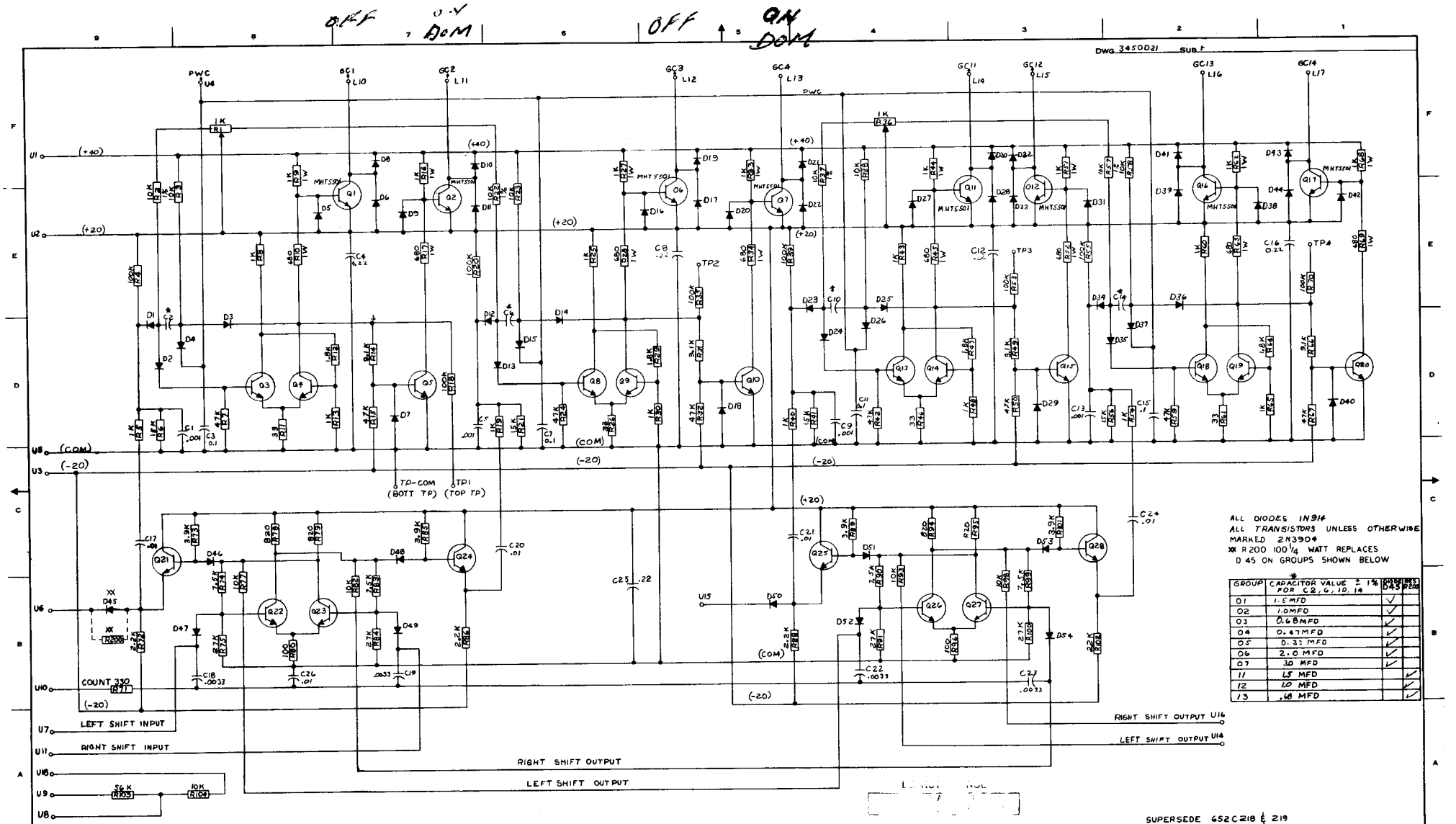
DFTG. DA BRITTIN 1/13/69
APPD. W.R. Wellham
APPD.
APPD.

ENG REF DWG: SCHEM. 345D031

DWG 668C407

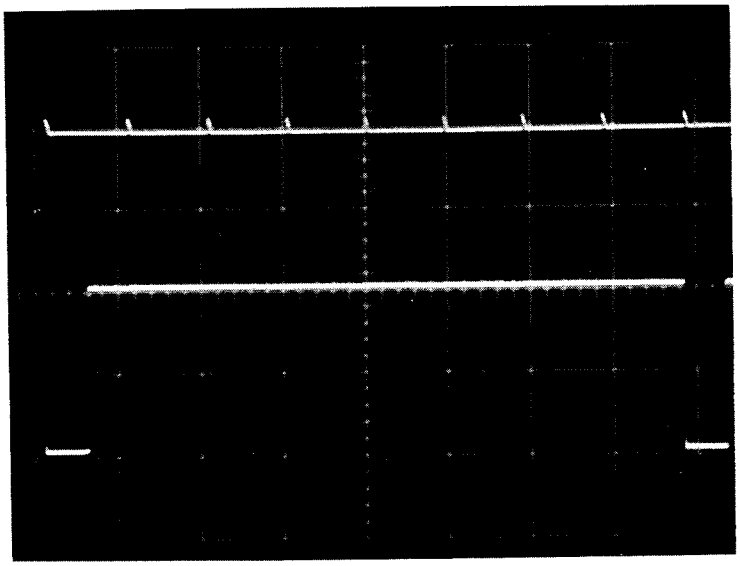
DIV & PLANT LOCATION: GEN. CONT.

BUFFALO DIVISIONS, BUFFALO, N.Y. U.S.A.

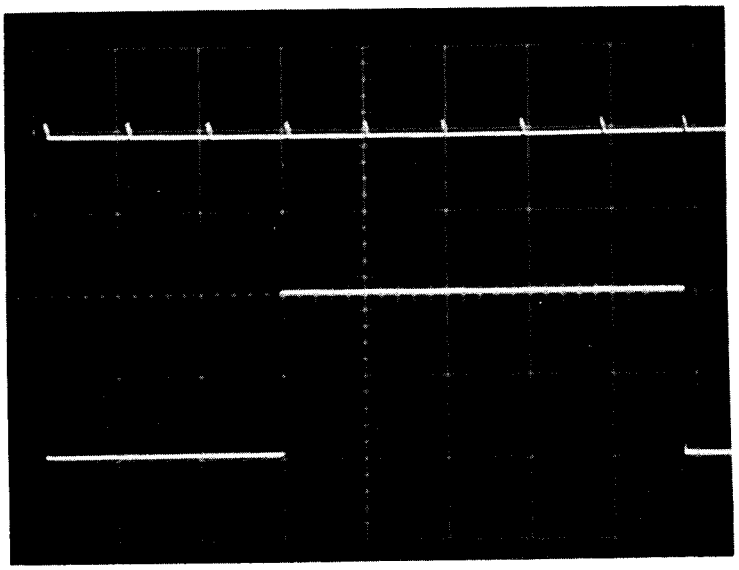


SUPERSEDE 652C218 & 219

WESTINGHOUSE ELECTRIC CORPORATION
TITLE COUNTER DRIVER BOARD SCHEMATIC
DIV. & PLANT LOCATION GEN. CONT. BUFFALO DIVISIONS, BUFFALO, N.Y., U.S.A.
ASSY. DIAG. 652C407
3450D31
02 L

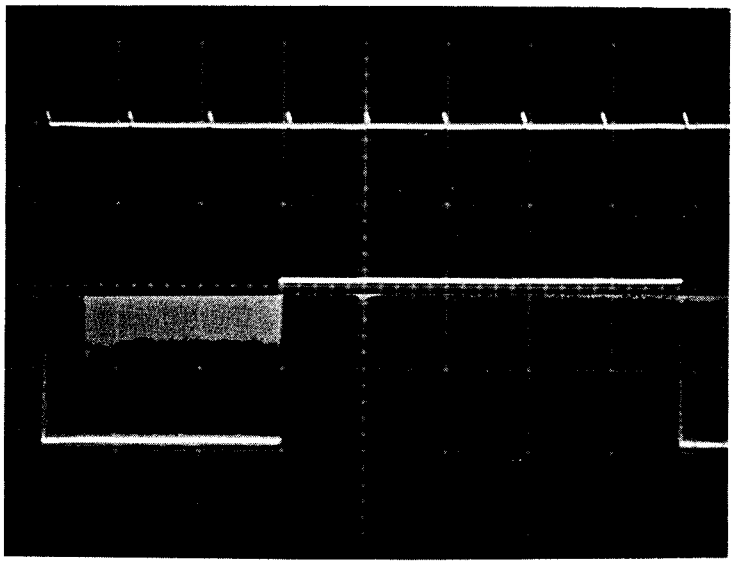


Upper Trace: Reference COUNT signal
Lower Trace: TP to COM (minimum P.W.)



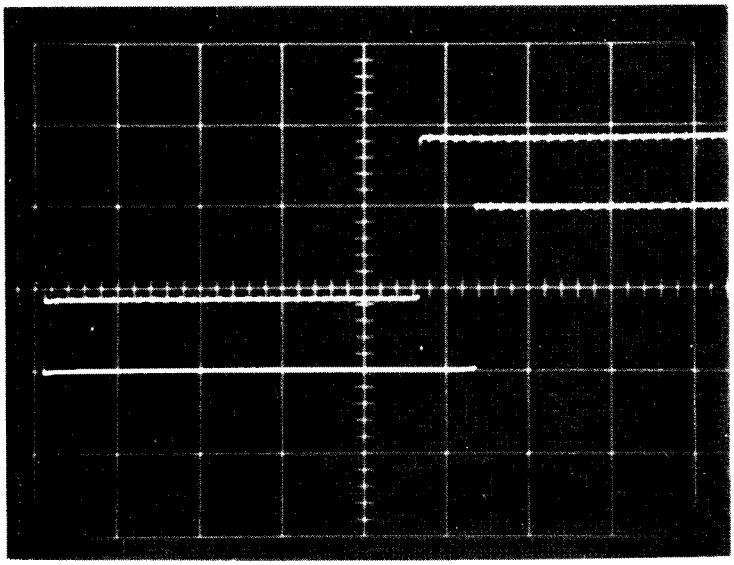
Upper Trace: Reference COUNT signal
Lower Trace: TP to COM (normal P.W.)

TYPICAL WAVEFORMS OF COUNTER/DRIVER BOARD
(Four-Stage Inverter Operation)

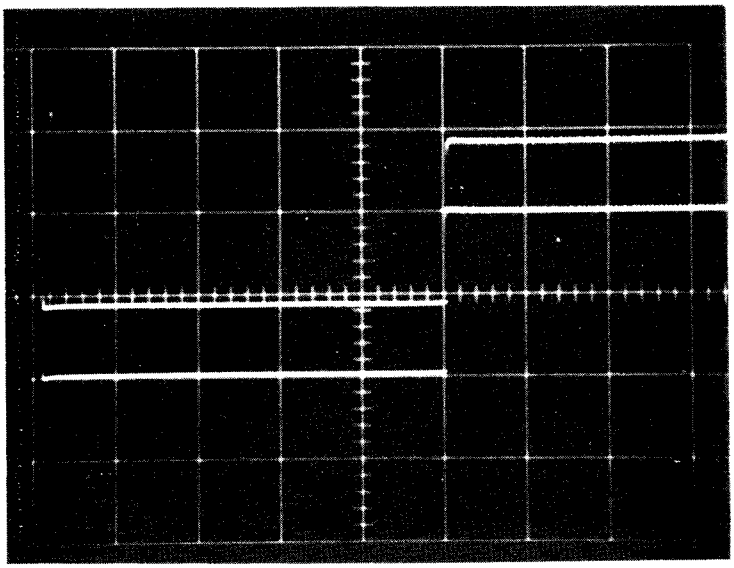


Upper Trace: Reference COUNT signal
Lower Trace: TP to COM

MEMOSCOPE WAVEFORM OF COUNTER/DRIVER BOARD
GOING FROM MINIMUM TO NORMAL PULSE WIDTH



INCORRECT BALANCE



CORRECT BALANCE

COUNTER/DRIVER BOARD BALANCE
ADJUSTMENT BY TRIMPOT SETTING