MICRO-PRODAC
POWER SUPPLY PANEL

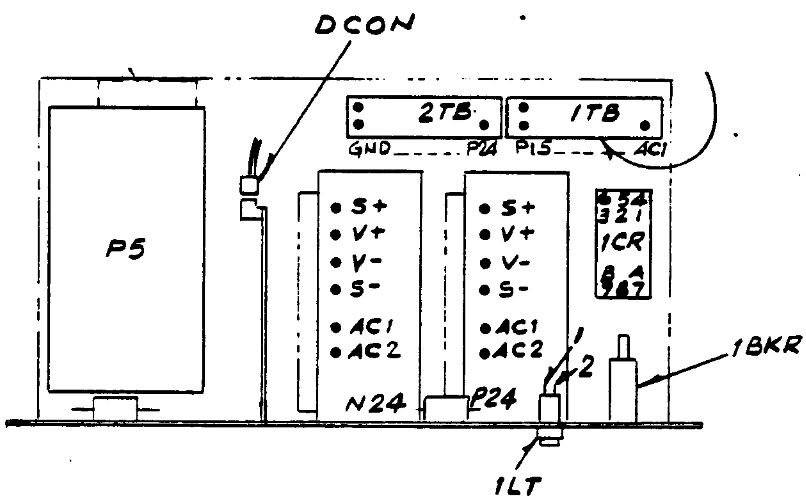
I. INTRODUCTION

The MICRO-PRODAC Power Supply Panel is designed to provide the MICRO-PRODAC Cage with regulated +5V, +24V and -24V as well as provide the M-6 cage with regulated +15V. The MICRO-PRODAC Bus Power Specifications are given in Appendix 3. The Recommended Power Supply Specifications for the +5V, +24V and the -24V supplies are given in Appendix 4. A 3-pin 15V regulator powered by the +24V supply provides the +15V for the M-6 cage.

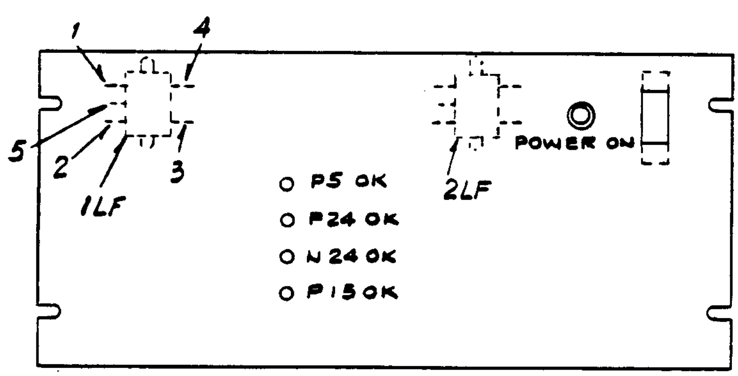
AC transients are prevented from affecting the DC supply outputs by the implementation of two line (AC) filters as shown on the block diagram in Figure 1. The AC line is protected by a 25A circuit breaker. An AC Power On light is also provided.

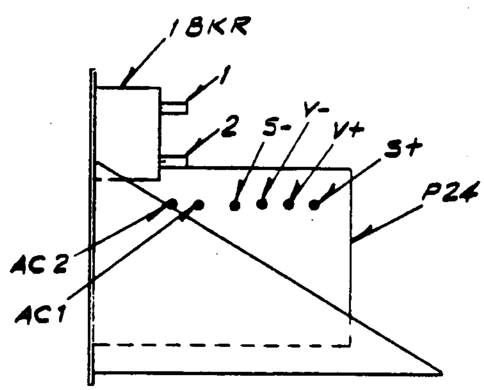
AC line loss and DC power supply failure indication/detection are provided by the Power Supply Detection (PSD) Board. Four green "Supply OK" LEDs give quick visual failure status for the +5V, +24V, -24V and +15V supplies.

The 1K pull-up resistor for the Power Fail Interrupt ($\overline{PFIN}$) signal is located on the PSD Board. If either an AC loss or a +5V failure is detected, $\overline{PFIN}$ is driven low (0V) for a minimum of 3ms. If any failure is detected (i.e. AC loss, +5V, +24V, -24V or +15V failure), the relay 1CR will be de-energized.



TERM. NO. ARE THE SAME FOR 1LF, 2LF





EFFECTIVE DATE: AUGUST, 1981

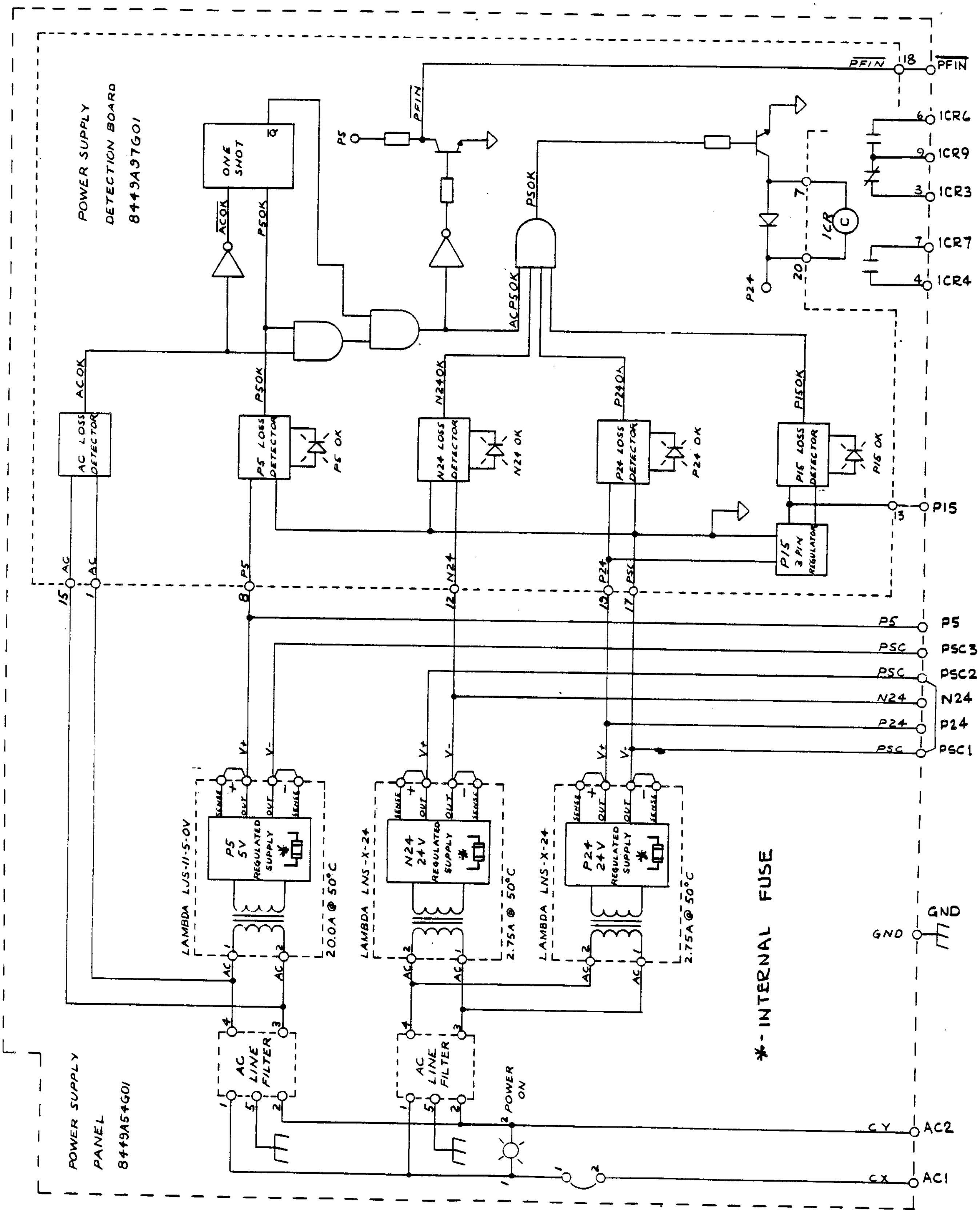

POWER SUPPLY
DETECTION BOARD
8449A97G01
ONE SHOT
ACOK
PSOK
PFIN
P5
ACPSOK
N24OK
P24OK
P15OK
AC LOSS DETECTOR
P5 LOSS DETECTOR
N24 LOSS DETECTOR
P24 LOSS DETECTOR
P15 LOSS DETECTOR
P5 OK
N24 OK
P24 OK
P15 OK
P15 3 PIN REGULATOR
1CR
P24
PFIN
1CR6
1CR9
1CR3
1CR7
1CR4
P15
P5
PSC3
PSC2
N24
P24
PSC1
PSC
P5 5V REGULATED SUPPLY
N24 24V REGULATED SUPPLY
P24 24V REGULATED SUPPLY
LAMBDA LJS-11-5-OV
LAMBDA LNS-X-24
20.0A @ 50°C
2.75A @ 50°C
*- INTERNAL FUSE
GND
AC LINE FILTER
POWER ON
POWER SUPPLY
PANEL
8449A54G01
AC2
AC1

FIGURE 1

II. DESCRIPTION OF OPERATION

AC Loss Detector

The AC loss detection circuitry was designed to be a total power loss detector and not a level detector. The detector has a built in time delay via a 555 timer to prevent nuisance trips due to line droops and transients. An optical coupler provides isolation between the 115VAC line and the logic circuitry.

An input drive of approximately 5ma which amounts to 52VRMS input voltage is required for 1TR to start turning on. As a result of 1TR conducting current 2TR and thus 1-OC start to conduct. As 2TR turns on, it supplies more base drive to 1TR causing it to turn on quicker (i.e. "snap on") and eventually saturate. 1-OC shorts out 8R and 1C forcing the output of the 555 to remain high (ACOK=1).

As the AC voltage drops below the 52VRMS level, 1TR starts turning off along with 2TR and 1-OC. For a 60HZ sinusoidal input voltage, 1-OC will remain off for approximately 2.5ms and 3ms for a 50HZ input. This allows capacitor 1C to charge for 2.5ms (3ms for 50HZ) under no-fault conditions. 1C requires 7-8ms to charge to the 2/3 supply level (3.3V) in order to drive the output of the 555 low (ACOK=0). Under normal operating conditions 1C will never have enough time to charge up to the required 2/3 level before 1-OC turns on discharging 1C thru 8R. A time delay of 4.5 to 8ms for 60HZ input (or 4 to 8ms for 50HZ) will elapse before ACOK goes to a 0. The actual time delay will depend on what point of the sinusoid the power loss occurs.

The signal ACOK is inverted and fed into a one-shot (4IC) configured as a pulse stretcher. 47R and 5C are set to obtain a pulse width of approximately 9ms which will guarantee that $\overline{PFIN}$ (Power Fail Interrupt) will remain 0 long enough for the processor to service the power failure routine. Since the one-shot only puts out a single pulse, ACOK and P5OK are nanded with the Q output forming signal $\overline{ACP5OK}$ to ensure that $\overline{PFIN}$ remains 0 for as long as an AC loss condition exists. The $\overline{ACP5OK}$ signal is inverted and is fed into a DTL AND gate which drives relay 1CR. An AC loss (ACOK=0) will de-energize relay 1CR.

Under normal operating conditions (ACOK=1) the base of 8TR is biased slightly negative to prevent noise from affecting the $\overline{PFIN}$ line which has been found to be noise sensitive.

+5V Failure Detector

The +5V detector is a precision level detector that utilizes a quad-comparator (5IC) with an open-collector output. The level settings for all the detectors are found in Table 1. The detector is designed to keep the "P5 OK" LED on and the comparator output P5OK=1 in the event the V+ supply (i.e. +24V supply) should fail. All subsequent detectors have this feature.

The +24V is divided down to obtain a 4.5V reference voltage which is applied to the (-) input of the comparator. Under the no-fault condition, the output transistor of the comparator is off. Therefore, +5V is seen at the (+) input as well as the output of the comparator (P5OK=1). With 3D reversed biased, 3TR turns on allowing current thru the "P5 OK" LED.

Should the +5V supply fall below the reference voltage (i.e. 4.5V), the open collector transistor will turn on dropping the output to 0.2V (P5OK=0). Transistor 3TR no longer has the required base voltage and turns off causing the "P5 OK" LED to extinguish. The P5OK=0 signal has the identical effect as the ACOK=0 signal. The $\overline{PFIN}$ is driven low and relay 1CR is de-energized. The hysteresis resistors 12R and 13R require that the failed +5V supply comes back up to 4.75V before P5OK=1 again.

The V+ input (+24V) to the quad-comparator is auctioneered with the +5V supply in order to keep the V+ the required 1.5V above the common-mode voltage in the event the +24V supply should fail. Capacitor 3C is used to prevent noise that can be generated when the +24V supply fails from affecting the P5OK output signal which would in turn affect $\overline{PFIN}$.

+15V Failure Detector

The +15V detector works in an identical manner as the +5V detector. Note that since the +24V supply drives the +15V regulator, a failure of the +24V supply may result in a failure of the +15V supply.

On the +15V detector, it is not a concern if the common-mode voltage should come within 1.5V of the V+ source due to a +24V supply failure causing P15OK=0. This is true since a +24V failure would have already de-energized 1CR and the P15OK signal does not affect $\overline{\text{PFIN}}$.

-24V Failure Detector

The -24V detector utilizes the comparator in a zero crossing configuration in order to detect a negative voltage with a positive reference voltage. Hysteresis is obtained by turning off 5TR which will allow 27R to enter into the reference voltage divider network. Under the no-fault condition 5TR is turned on shorting out 27R.

A reference voltage of 21.6V is applied to the (-) input of the comparator thru a 100K resistor. Likewise the -24V supply voltage is applied to the (-) input thru a 100K resistor. The (-) input will therefore be biased slightly negative holding the output open collector transistor off (N24OK=1). Although a small current flows thru the 2-OC diode to drive the base of 5TR, it is not nearly enough to turn off the "N24 OK" LED.

Should a fault condition occur (i.e. -24V supply drops below -21.6V), the (-) input to the comparator will swing slightly positive causing the output to go low (N24OK=0). 2-OC will now have sufficient drive to reverse bias 6TR shutting off the "N24 OK" LED. 5TR turns off allowing 27R to raise the reference voltage to 23V. This requires the -24V supply to come back up to -23V before N24OK=1 again. As in the previous detectors, should the V+ supply fail, the "N24OK" LED will remain on.

+24V Failure Detector

The +24V detector utilizes a different quad-comparator (6IC) where the V+ and the reference voltage are both supplied by the +5V supply. In order to keep the V+ the required 1.5V above the common-mode voltage under no-fault conditions, it is necessary to divide down the +24V and the +5V.

A reference voltage of 2.16V is applied to the (-) input and the +24V is applied to the (+) input via a divide by 10 network (i.e. 2.4V will be seen at the (+) input). 7D is placed in series with the hysteresis resistors since the + input is at a 2.4V potential instead of the full 24V. With the above exceptions, the +24V detector is the same as the +5V and the +15V detectors. The hysteresis resistors are set such that if a failure occurred, the +24V supply would have to come back up to +23V before P24OK=1 again.

Power Up Delay

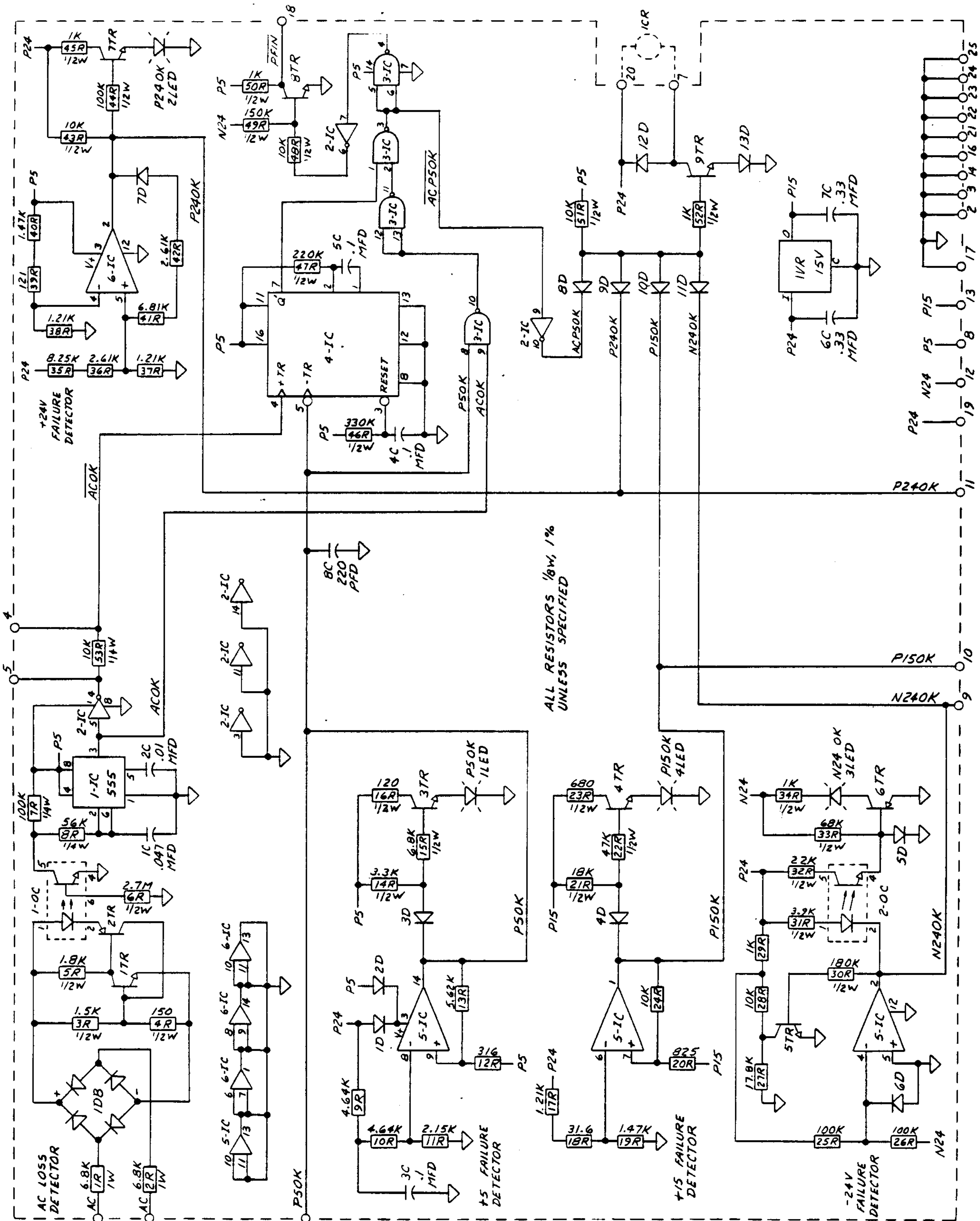
The one-shot pulse stretcher has a power up delay network consisting of 4C and 46R connected to its RESET input. This delay network will insure that PFIN remains high for approximately 20ms after power is initially applied.

SUPPLY	DROP OUT	PICK UP
+ 5V	4.50V	4.75V
+15V	13.0 V	14.0 V
+24V	21.6 V	23.0 V
-24V	-21.6 V	-23.0 V

TABLE 1

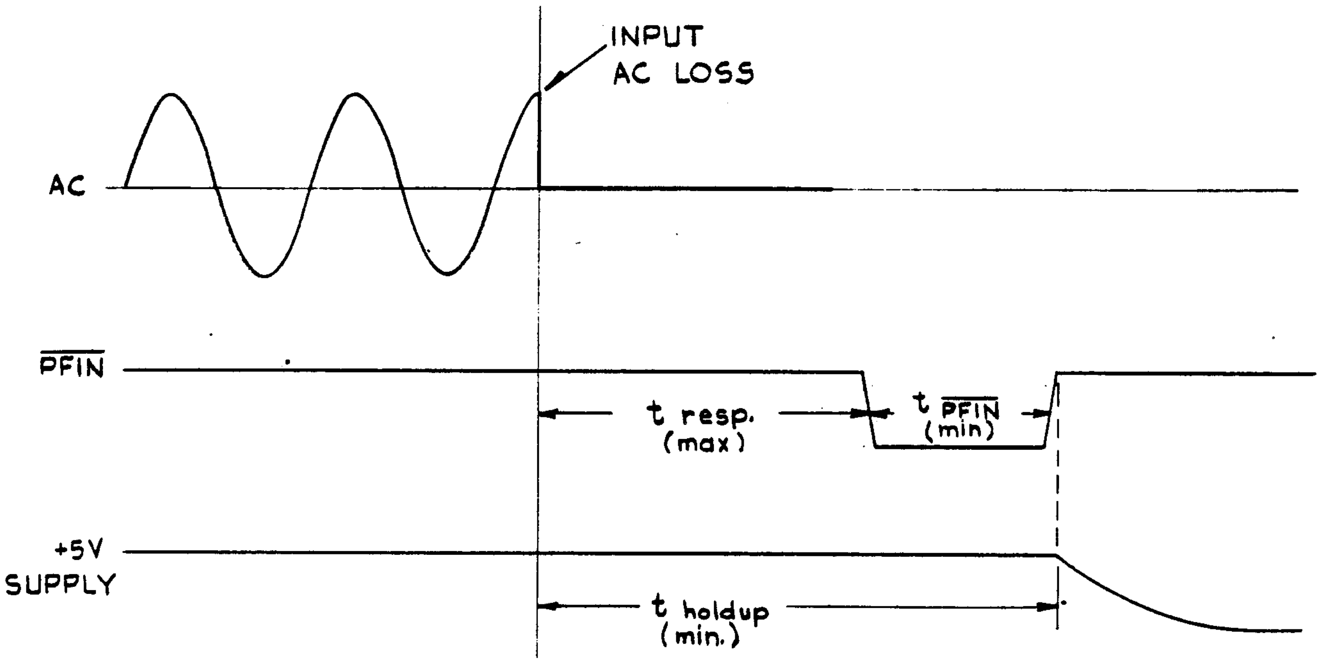
POWER SUPPLY DETECTION LEVELS

MICRO-PRODAC POWER SUPPLY DETECTOR
SCHEMATIC DIAGRAM



APPENDIX 2

TIMING SPEC FOR AC LOSS DETECTION



The AC loss detection circuit along with the +5V power supply must meet the following timing specifications.

	MIN	MAX
t_{RESP}	2ms	10ms
$t_{\overline{PFIN}}$	2.5ms	-
t_{HOLDUP}	13ms	-

APPENDIX 3

BUS POWER SPECIFICATIONS

Standard (P1)

Mnemonic	Ground GND	+5 +5V	+12 * +12V	-12 * -12V
Nominal Output	Ref.	+5.0V	+12.0V	-12.0V
1Tolerance from Nominal	Ref.	±5%	±5%	±5%
2Ripple (Pk-Pk)	Ref.	50mV	50mV	50mV
3Transient Response Time		500uS	500uS	500uS
4Transient Deviation		±10%	±10%	±10%

* NOT USED IN MICRO-PRODAC SYSTEMS

APPENDIX 3 (Continued)

BUS POWER SPECIFICATIONS

Analog Power Optional (P2)

Mnemonic	Ground PSC †	+15 +15V	-15 -15V	+24 † P24	-24 † N24
Nominal Output	Ref.	+15.0V	-15.0V	+24.0V	-24.0V
1Tolerance from Nominal	Ref.	±5%	±5%	±5%	±5%
2Ripple (Pk-Pk)	Ref.	10mV	10mV	50mV	50mV
3Transient Response Time		100uS	100uS	-	-
4Transient Deviation		±10%	±10%	-	-

† ADDED TO MULTIBUS STANDARD FOR USE IN MICRO-PRODAC SYSTEMS

NOTES:

1. TOLERANCE IS WORST CASE, INCLUDING INITIAL VOLTAGE SETTING LINE AND LOAD EFFECTS OF POWER SOURCE, TEMPERATURE DRIFT, AND ANY ADDITIONAL STEADY STATE INFLUENCES.
2. AS MEASURED OVER ANY BANDWIDTH NOT TO EXCEED 0 TO 500KHZ.
3. AS MEASURED FROM THE START OF A LOAD CHANGE TO THE TIME AN OUTPUT RECOVERS WITHIN ±0.1% OF FINAL VOLTAGE.
4. MEASURED AS THE PEAK DEVIATION FROM THE INITIAL VOLTAGE.

APPENDIX 4

RECOMMENDED POWER SUPPLY SPECIFICATIONS FOR MICRO-PRODAC SYSTEMS

MNEMONIC	+5V	+24V	-24V
Input Voltage	105 - 130VAC	105 - 125VAC	105 - 125VAC
Input Frequency	50 - 60HZ	50 - 60HZ	50 - 60HZ
Power Efficiency	70% (min)	40% (min)	40% (min)
Output Current Rating 0 - 50°C	20A (min)	2.5A (min)	2.5A (min)
Output Line Regulation for line variation over the Input Range	±1.0%	±1.0%	±1.0%
Output Load Regulation for load variations from 0 to full load	±1.0%	±1.0%	±1.0%
Ripple and Noise	50mV p-p (max)	50mV p-p (max)	50mV p-p (max)
Adjustable Range	±5%	±5%	±5%
Overvoltage Protection	Required	Required	Required
Overload Protection (Short Circuit & Current Limit)	Required	Required	Required
Holdup Time after AC loss (Within Regulation)	15ms min	15ms min	15ms min
Turn On/Turn Off Overshoot (0 to full load)	None	None	None