M5B GATING SYSTEM

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I. INTRODUCTION

The M5B gate control system consists of a gate control transformer (GCT) S#1295A25; the reversing logic portion of the voltage controller card (VC & RL) S#1757A01 for double converters; portions of the gate sync card (GS) S#1710A08 for 60 hz operation, S#1752A12 for 50 hz operation; two gate pulse generator cards (GPG) S#1671A17; two thyristor gate driver cards (TGD) S#1668A25 for double converters, one for single converters; some components associated with the pulsing circuits of the thyristor bridges; the inhibit ($\overline{INH}$) and gate pulse suppression ($\overline{GPS}$) function of the protection board; and in the case where the TPM consists of parallel bridges, one or more gate pulse amplifiers (GPA); and the interconnecting wiring.

Features designed into the M5B Gating System are:

1. Reversing Logic - Only one converter can be gated at a time.

   a. Primary Crossover Logic - Comparison of voltage feedback to voltage demand signal, which is generated internally in the VC&RL, to determine whether forward or reverse converter operation is required.

   b. Current Crossover Lockout - Crossover cannot be initiated when current is greater than 5% of rated. Current will always be zero when crossover is asked for under normal operating conditions. Under certain fault conditions (inverter faults) crossover could be asked for with high current flowing, by the voltage crossover logic, however, the current lockout feature prevents crossover faults to be generated on top of initial fault.

   c. Bias - Is preset for the regulating system used. It assures smooth initiation of current and voltage at start of gating and smooth crossover.

2. Synchronizing Signals - Are spaced precisely 60^0 apart.

   a. Gate Control Voltages - From GCT are directly in phase with the TPM supply voltage. In most cases the primary of GCT is taken directly off the TPM transformer secondary. In this case gating is correctly phased with no change in gate control wiring, regardless whether TPM supply transformer is delta-delta, wye-delta, or delta-wye.

   b. Sync Signal Generation - Zero crossing detection of GCT waves only, and are well filtered. Filtering virtually eliminates distortion due to commutation notches and higher frequency harmonics. Zero crossing detection eliminates any effects of line amplitude fluctuations.

3. Phase Advance Limit - Fixed at 0^0. No additional margin required in TPM transformer as would be the case for α fixed at greater than 0^0.

4. Picket Fence Gating - Pulses are delivered directly from firing transistor in TGD or GPA to thyristor pulse transformer to be fired. No steering diodes required as in double pulsing. Pulsing power supply is a highly filtered dc supply and is immune to large line distortion and fluctuations. Gating power is not sensitive to phasing.

   a. Hard Pulse - Gives large overdrive to thyristors for quick turn at first pulse; when high di/dt can occur, for discharging r-c networks in conjunction with commutation of high current levels.

   b. Trailing Pulses - Are available and required to refire thyristors when operating under light load, discontinuous current operation. They are of reduced amplitude and duration to reduce loading on the gate.

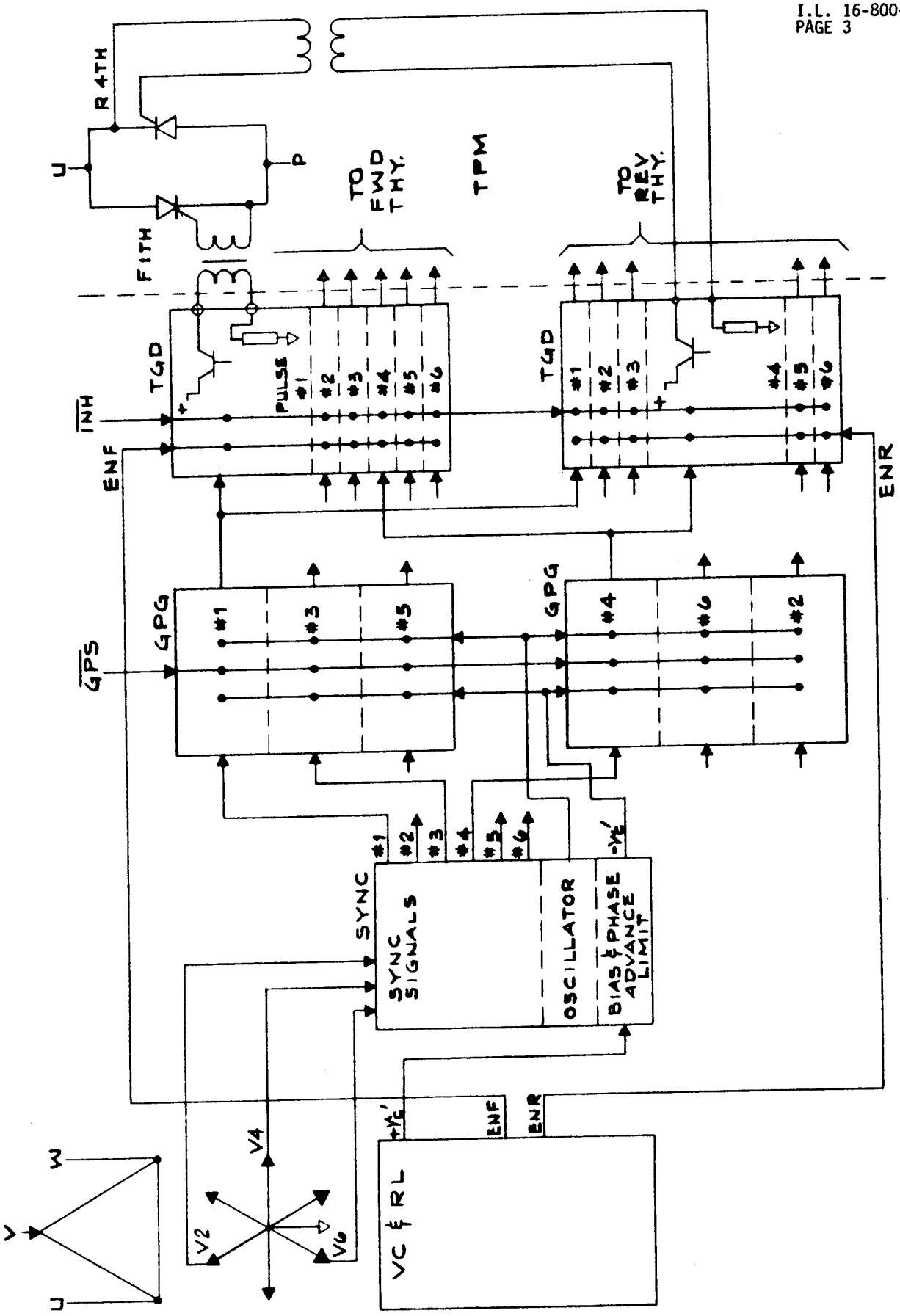
   c. Tail End Chop - Shortens pulse train (to less than 120^0) where gating cannot be required when operating at high delay angles. This reduces reverse leakage dissipation when thyristors have reverse voltage applied.

   d. Ramp Gating - Generates six pulses at 60^0 intervals with variations of less than 1^0 at $\alpha = 180^0$ which is worst tracking angle. Phase angle is directly proportional to control voltage over the range of $0^0 \leq \alpha \leq 180^0$.

   e. Ring Counter - Turns off preceeding pulse in its half of the converter (3 turns off 1, etc.) as preceeding pulses are no longer required under any operating conditions.

5. Adjustments - None are required within the gating system.

The material in this leaflet describes the operation and function of the various circuits. It must be recognized that the circuitry described here is contained on several boards in the regulator cage and in other parts of the system and is not a distinct module. It should also be noted that the diagrams in this material are for instructional purposes; they will be simplified from the complete schematics and may not be current.



GATE PULSE GENERATION
FIGURE II-1

II. DESCRIPTION OF OPERATION

A. Signal Flow

1. Generation of Pulses

Figure 1 is a simplified diagram of the gating system showing important signal points required to generate pulses.

The VC & RL establishes a phase angle demand signal $+v_c'$. It as well establishes which converter, forward or reverse, is to be gated with signals ENF or ENR.

The GS has three functions associated with gate control. It receives three sinusoidal waves displaced 120° which are in phase with the TPM supply voltage. It uses zero crossing points to generate 6 sync pulses displaced 60° which start, and at a later period reset, timing ramps in the GPG. A 12K hz free running oscillator is also located on this board and is used as clock pulses for all trailing pulses generated. The third circuit on the GS provides the bias and phase advance limit function which conditions the phase demand signal ($+v_c'$ to $-v_c'$) from the VC & RL before it goes to the GPG.

The GPG(s) process the sync signals (1, 3, 5 and 4, 6, 2), phase control signal ($-v_c'$), clock pulses, as well as $\overline{GPS}$ permissive signal to generate a pulse train(s) with proper starting phase angle, correct width of pulses, and correct termination of pulses. A sync signal of 240° duration starts a timing ramp at 10° prior to $\alpha = 0°$. Signal $-v_c'$ determines at what time ($0° \leq \alpha \leq 180°$) after start of ramp the pulse train is triggered. The width of the hard pulse (first pulse) is timed within the GPG. Clock pulses are mixed with a timing window to provide trailing pulses. The first pulse and trailing pulses are not synchronized; first pulse timing is determined only by $-v_c'$, and trailing pulses are determined by clock pulse timing following a first pulse. With $0° \leq \alpha \leq 110°$ pulse train are of 120° duration with each GPG ring counter terminating the pulses (3 turns off 1, 5 turns off 3, etc., for 1 GPG; 4 turns off 2, etc. for 2 GPG). The ramp is reset at $\alpha = 230°$ by the sync signal, and any trailing pulses remaining are terminated; therefore with $110 \leq \alpha \leq 180°$ pulse trains are shorter than 120°. Signal $\overline{GPS}$ must be a "1" to allow any pulses to occur.

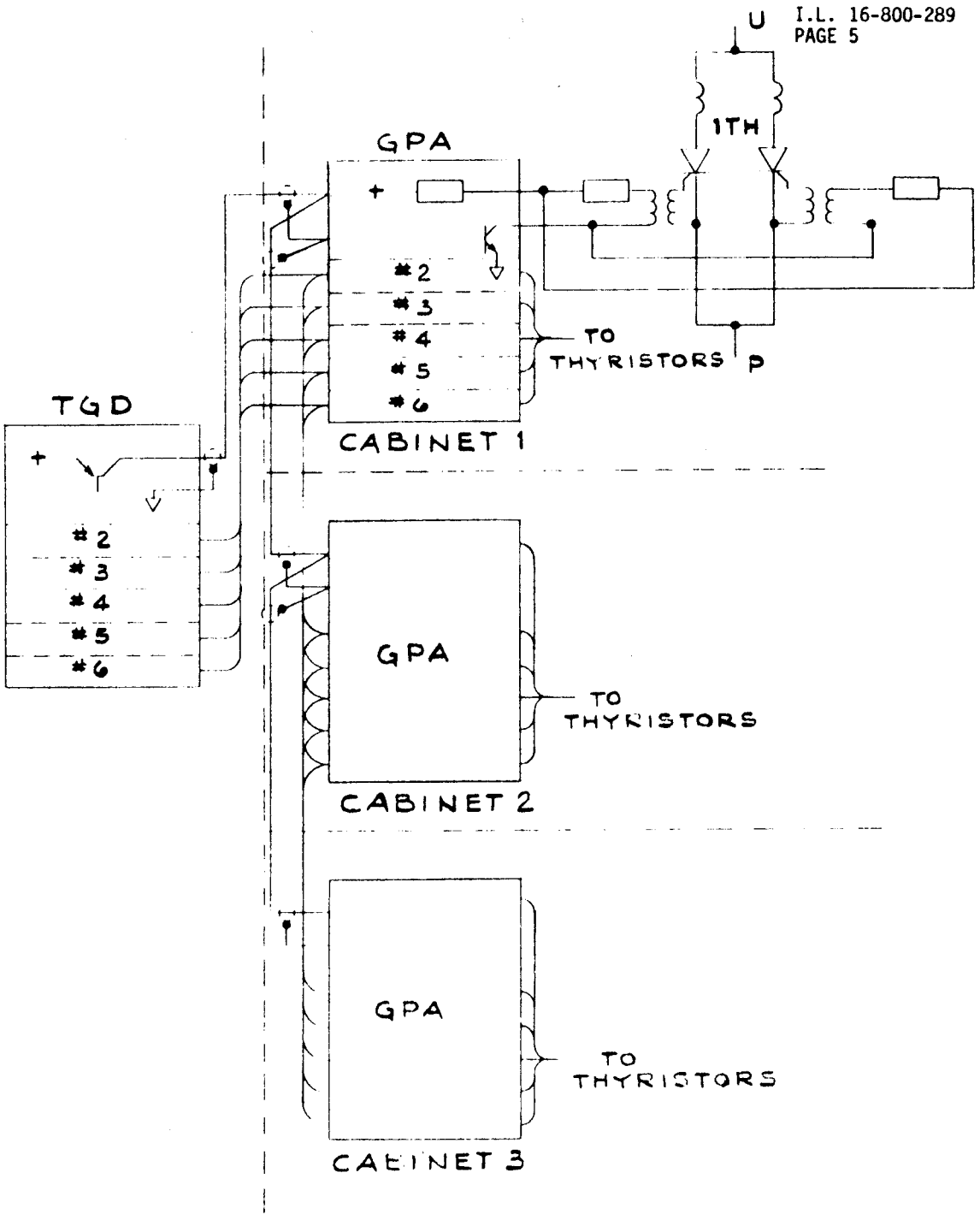
The TGD amplifies pulses from the GPG. In systems where parallel thyristors are not employed (up to approximately 500 HP) the TGD shapes as well as amplifies pulses for thyristor gating, with pulses in the first 150usec of greater amplitude than remaining pulses. A logic "1" signal (ENF or ENR) is required for gating to be allowed and only one TGD in double converters can be operative at a time. Signal $\overline{INH}$ must be a "1" to allow pulsing. $\overline{INH}$ is delayed from $\overline{GPS}$ by 100 usec so that if GPS occurs during a first pulse, this first pulse and only this pulse will be allowed to proceed through the TGD to thyristors.

Generation of functions and signal flow is now established in its simplest form for systems which do not employ parallel thyristors. The preceeding description states functions generated on particular boards, while Figure 1 shows direction of signal flow.

2. Pulse Distribution For Parallel Bridges

Figure II - 2 shows pulse distribution for parallel bridges. Normally two bridges are housed in each cabinet with a GPA associated also with each thyristor cabinet. Figure II - 2 shows only the forward pulse distribution, however reverse gate distribution is identical in principle to forward pulse distribution. Forward and reverse thyristors are not mixed within the same cabinet for parallel bridge operation.

The TGD used for parallel bridge operation is similar to that discussed in section II-A-1, however, capacitors and resistors previously used for pulse shaping are removed and where required jumpers are added. The TGD then serves as straight amplification of power (voltage and current) for gate pulses, and is capable of driving three or more GPAs.



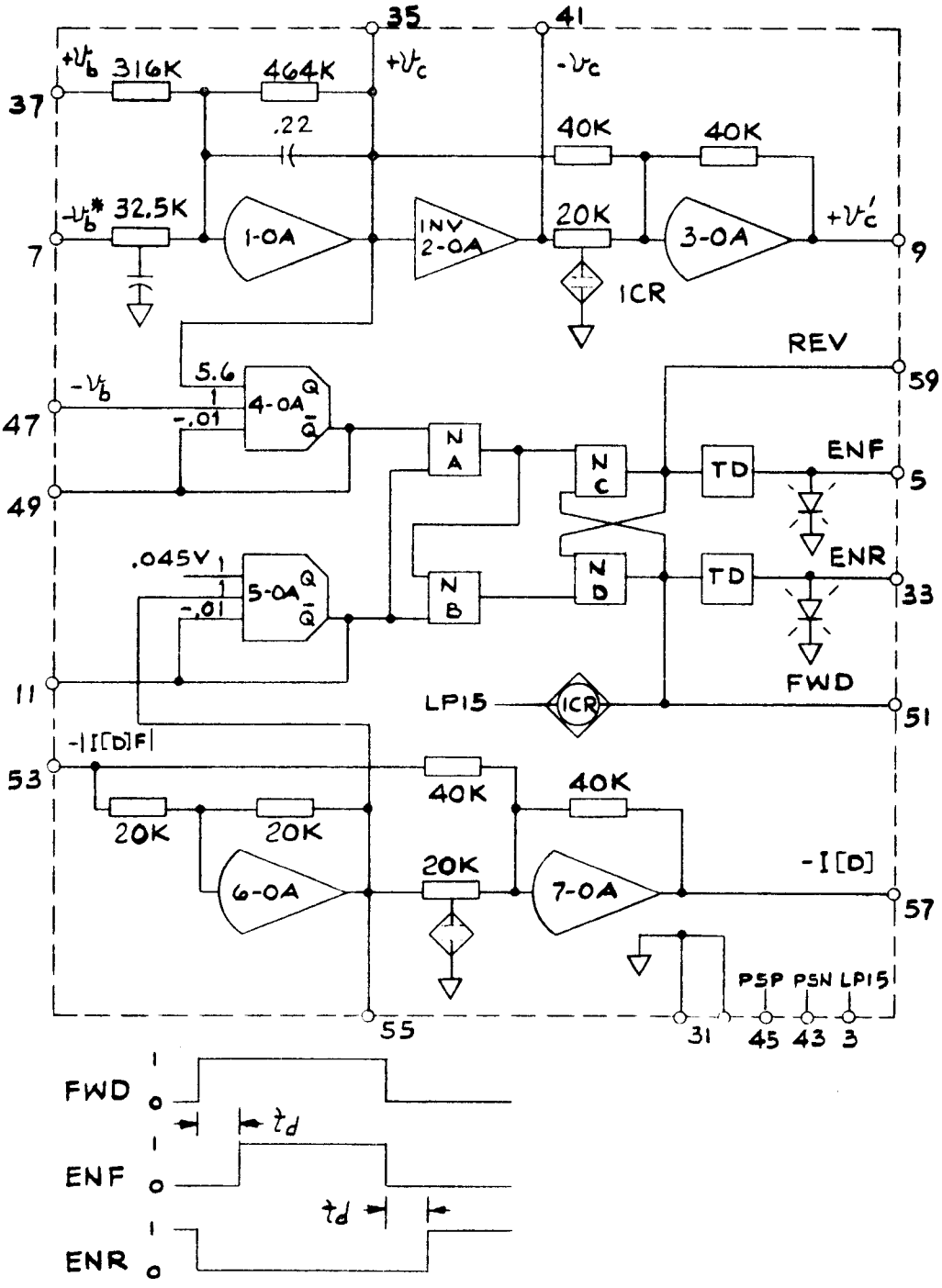
PULSE DISTRIBUTION

FIGURE II-2

GPAs amplify pulses and waveshape them similar to the function a TGD performed when single thyristors were to be fired. Each pulsing circuit in a GPA is capable of gating two or more thyristors in parallel. All pulsing circuits are identical. Figure II - 2 is a simplified diagram and pulse 1 is shown in somewhat more detail than remaining pulses.

B. Voltage Controller and Reversing Logic (VC & RL)

Figure II - 3 is a functional diagram which will be used to describe the principles of operation of the VC & RL.



VC & RL

FIGURE II-3

Operational Amplifier (1-OA) and its circuitry amplify the difference between the reference signal, $-v_b$* and the voltage feedback, $+v_b$ to form the control voltage V_c for the gating system. Time delay T_1 forces the closed voltage loop response to roll off before the effects of the transport delay of the gating system becomes significant.

Since the gating system control voltage is a unipolarity signal, an absolute value circuit is required to invert V_c when the reverse TPM is being gated. The unity gain absolute value circuit composed of Op Amp's 2-OA and 3-OA is controlled by a FET static switch which in turn is controlled by the reversing logic.

Comparator 4-OA generates the forward/reverse logic signal by comparing the output of the voltage controller v_c to the bus voltage signal, $-v_b$. As bias is added to the control voltage (in the limiting circuit on the GS board) there is a delay when going from forward to reverse current operation. For example when going from forward to reverse current, V_c starts toward negative values forcing forward current to zero, as V_c goes slightly more negative 4-OA switches to reverse gating, V_c keeps going negative until reverse current is picked up and established at the demanded level. As the closed voltage loop is fast, transition of current during current reversals is fast however it is smooth with gate switching operating while zero current is following. A logic "0" on pin 49 indicates that the forward bank is to be gated. The output of comparator 4-OA is coupled to the cross-tied NAND (C&D) flipflop by NAND's A & B. As long as the output of comparator 5-OA is a logic 1 the output of the flip-flop follows the output of comparator 4-OA.

Comparator 5-OA changes from a logic 1 to logic 0 when the feedback current becomes greater than .05p.u. (The 1p.u. current level is set at 2.0V by a current calibration circuit located elsewhere in the system). While 5-OA output is a logic 0 the flip-flop is prevented from changing banks. Then no reversing is allowed during high load currents. Under normal conditions the load current is zero at the time of reversing. However some fault conditions exist when drive current is not zero and a reversal could occur, causing additional faults, if this circuit was not used.

Time delays TD ensure that a TPM is allowed to be gated only TD seconds (approximately 3ms) after the other TPM has been turned off. Gate pulses are removed from a TPM immediately upon the switching of comparator 4-OA, which forces either ENF or ENR to a logic 0. Logic signals ENF and ENR go to their respective forward and reverse Thyristor Gate Driver Cards to control which TPM, (the forward or reverse) receives gating pulses. Light Emitting diodes FWD and REV indicate which bank is enabled.

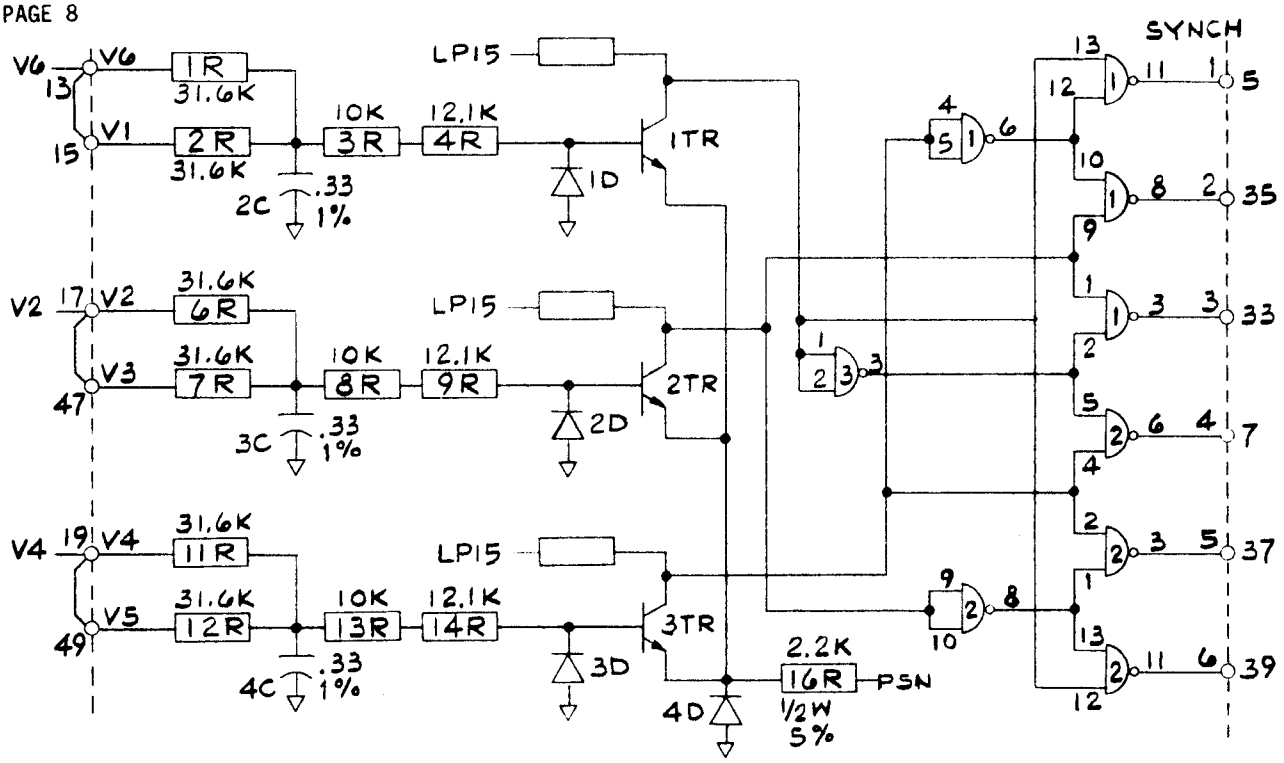
The reversing logic (4-OA, 5-OA and associated NANDs) operate on the current feedback as well. Usually a single set of CTs (3) sensing ac drive current is rectified and brought to terminal 53. When the forward converter is gated the signal at terminal 57 is only zero or negative, however when the reverse converter is gated RL assures the signal at terminal 57 is only zero or positive establishing correct polarity of current feedback for both directions of operation.

C. Gate Synchronizer (GS)

The Gate Synchronizer (GS) generates the digital information used by the Gate Pulse Generator (GPG) to determine the gating angle of the power thyristor. The Synch voltage is obtained from a three phase transformer which has a fixed phase relationship to the commutation voltage of the power thyristors.

The synch signals are generated by transistors 1TR, 2TR and 3TR and their associated input networks. The subsequent NAND gates create the digital SYNCH 1 through SYNCH 6 waveforms required by the Gate Pulse Generator. The input "T" filters add a phase shift of 50 degrees as well as filter out noise existing on the Gate Control Transformer (GCT) output voltage.

The gating angle (α) is established as zero at the time thyristor commutation voltage goes positive. When continuous current is flowing thyristor voltage is well defined, and it can be seen with 5TH conducting, voltage across 1TH (commutation voltage) is U-W with $\alpha = 0^0$ when U-W initially goes positive. Each succeeding commutation voltage, sync signal, and gate pulse is of course sequentially displaced 60^0.



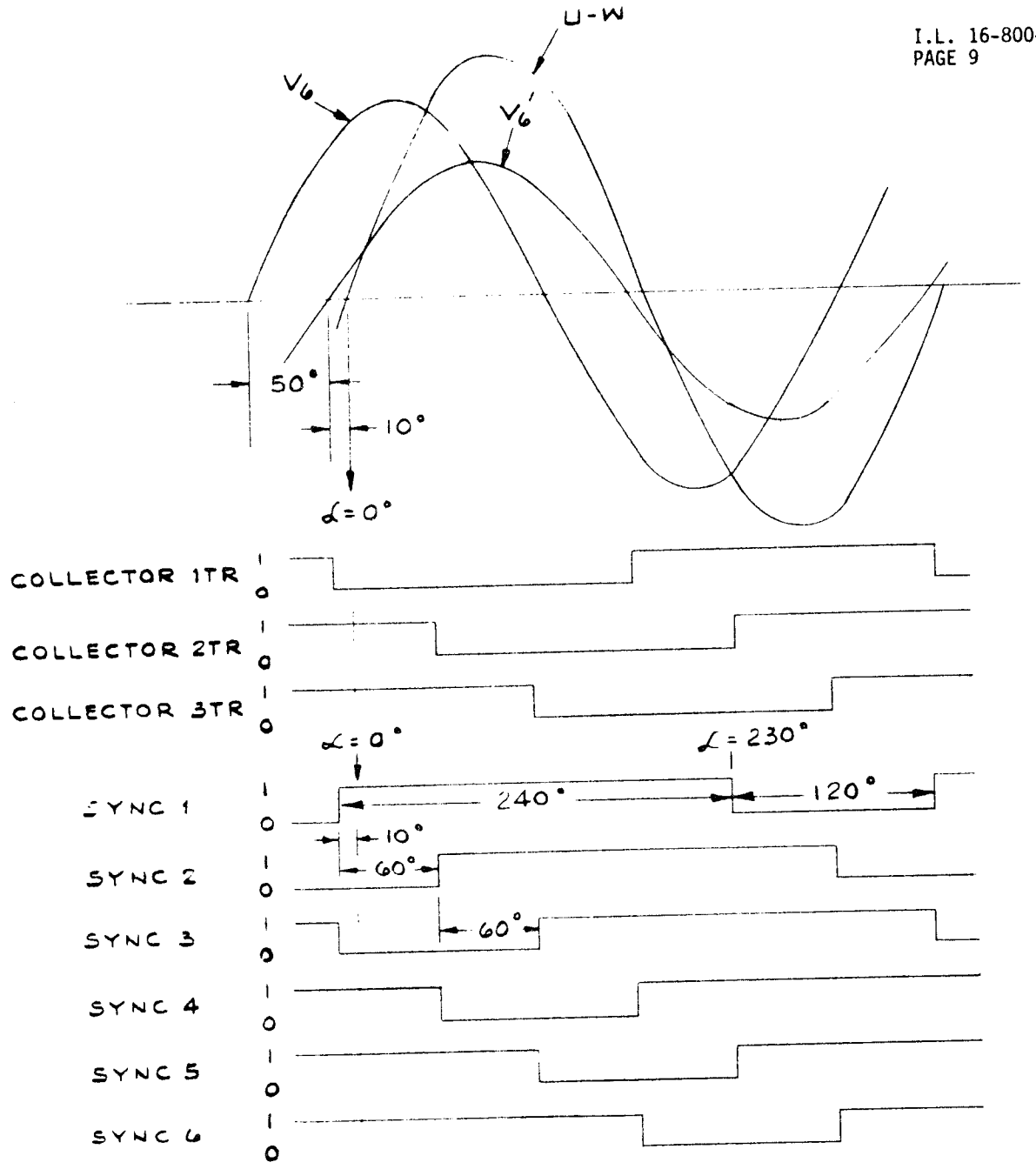
GATE SYNCHRONIZER
FIGURE II-4

Figure II - 5 shows relative waveform position of commutation voltage (U-W), sync timing waveforms (V_6), filtered timing waveform (V_6'), collector 1TR voltage, and sync 1 pulse all associated with 1TH. Collector 2TR, 3TR and remaining sync pulse relative positions are also shown.

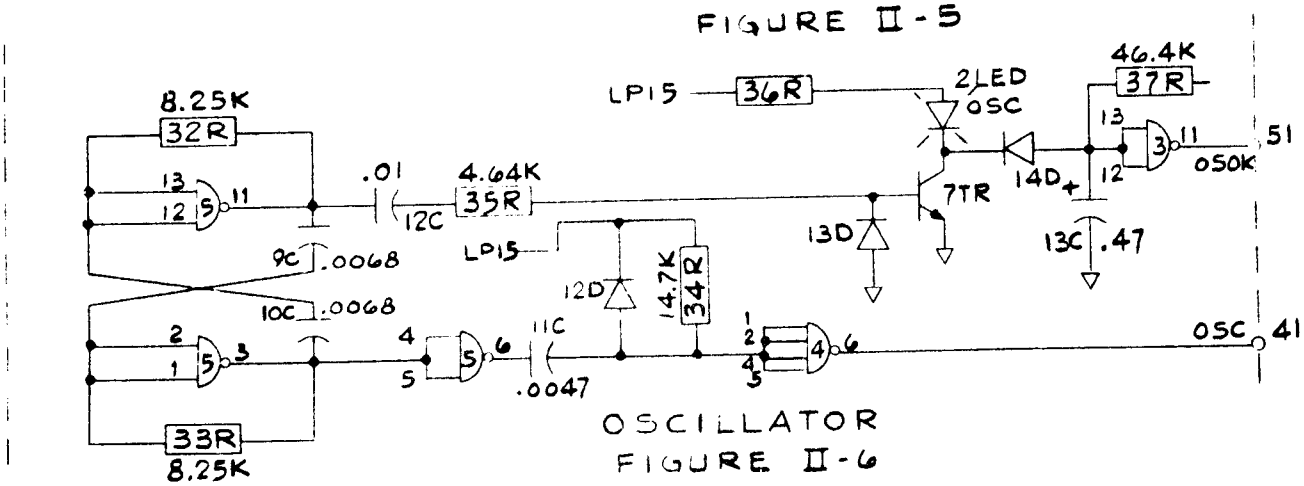
Also located on the GS card are the oscillator (clock) function and the limit and bias amplifier required by the gating system.

Digital NAND gates are used to form an astable multivibrator followed by a pulse shrinker out of which is generated the clock pulse for a picket fence gating system. Resistors 32R and 33R, capacitors 9C and 10C and their associated NAND gates comprise the astable multivibrator. The pulse shrinker composed of resistor 34R, capacitor 11C, diode 12D and their associated NAND gates shorten the 50% duty cycle of the astable multivibrator signal to that required by the gating system (approximately 25% duty cycle).

The Light Emitting diode 2 LED is ON while the oscillator is operating. Coupling capacitor 12C allows transistor 7TR to turn the LED OFF independent of which state the astable multivibrator fails.



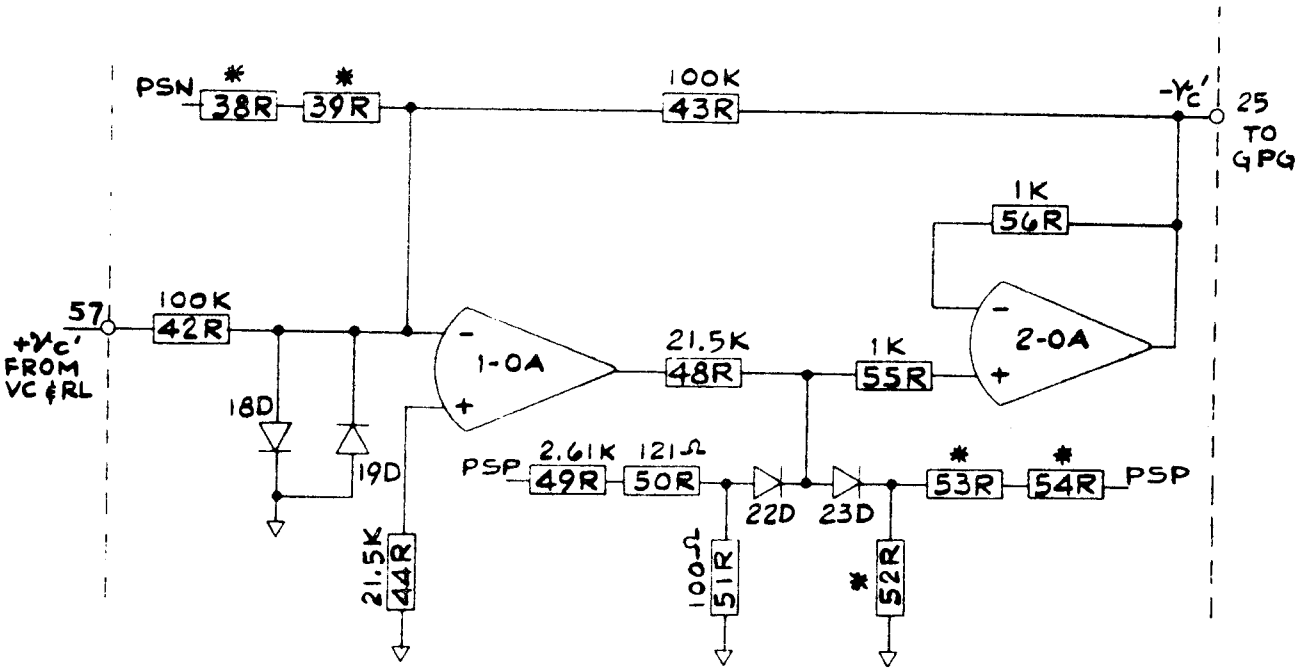
SYNCHRONIZER WAVEFORMS
FIGURE II-5



OSCILLATOR
FIGURE II-6

Operational Amplifiers 1-OA and 2-OA and associated circuitry form a series limit and bias function.

The limiter is required to confine the gate control voltage within the operating range of the gate pulse generator. In addition advance, retard and bias angles for the gating system can easily be set with voltage levels. Selecting the advance, retard and bias angles depends on the system in which the gating system is to be used. The most common system employed is motor drives with α min = 0^0, α max = 180^0, and bias (with input $+v_c'$ = 0 volts) α = 145^0. Corresponding voltage to GPG for these angles is .34V, 6.4V, and 5.3V respectively.

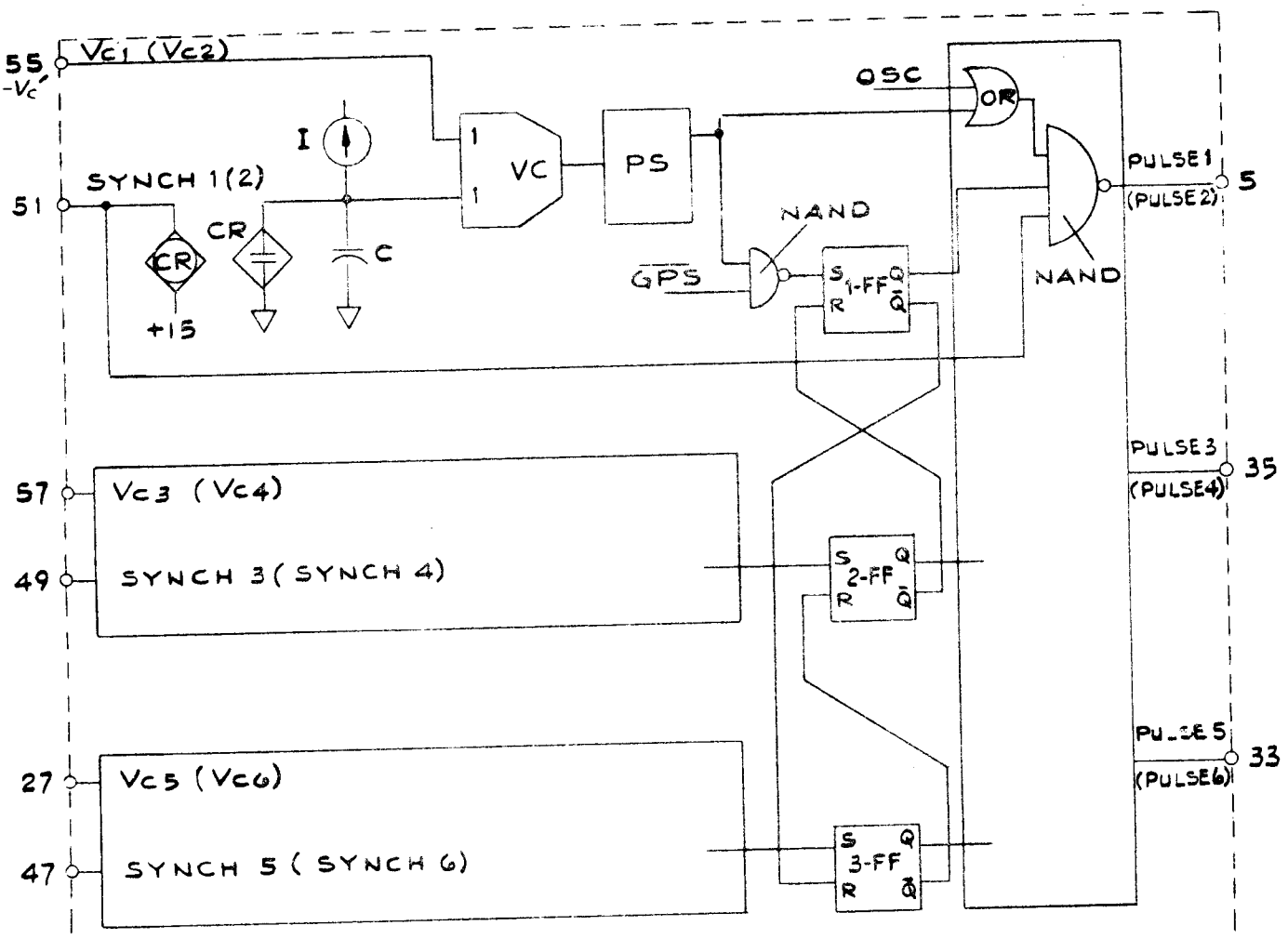


SERIES AMPLIFIER
FIGURE II-7

D. Gate Pulse Generator (GPG)

Each GPG board has three identical circuits providing for picket fence pulse trains spaced at 120^0 intervals. As six pulses are required, two GPG boards are used. Figure II - 8 is a functional diagram of a GPG.

Each sync signal (transition to logic "1") starts each ramp at 10^0 prior to α = 0^0, and resets each ramp at α = 230^0 (transition on sync to logic "0"). The constant current charging the capacitor results in a highly linear ramp from which the gating angle can be determined. The negative going ramp is fed into voltage comparator. VC along with a positive control voltage-V_c'. The point on the ramp at which the comparator switches from a logic 0 is a logic 1 is controlled by $-V_c'$. α = 0^0 at $-v_c'$ = .34V which is the least positive incoming control voltage. As $-V_c'$ goes more positive the phase angle is delayed at a rate of approximately 30^0 per volt for 60 hz. toward α = 180^0 which is in a direction to reduce voltage in the converter. It should be noted the control voltage is $-v_c'$ even though it is always positive, as a less positive voltage gives a phase advance thus causing a more positive voltage in the converter.



GPG
FIGURE II-8

The logic 1 of the comparator is "shrunk" by the pulse shrinker, PS, to a pulse 50uSec long. This pulse serves as the hard first pulse of the picket fence pulse train as well as to set flip-flop 1-FF. The hard pulse is OR'ed with an externally supplied oscillator signal and then this signal is NAND'ed with the Q output of flip-flop 1-FF to form the picket fence pulse train.

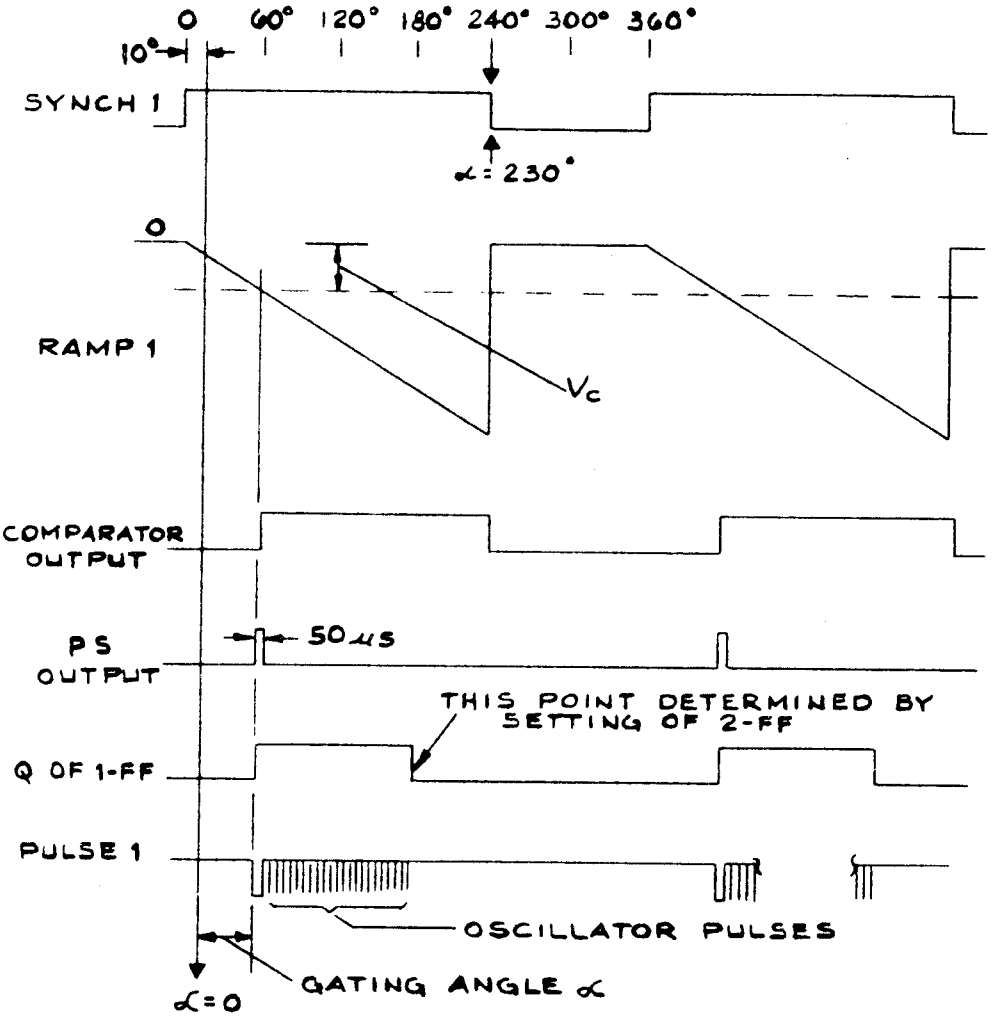
The purpose of the 50uSec hard first pulse is to assure that the initial pulse applied to the power thyristor gate is adequate to gate the device completely ON for any load conditions. The oscillator signal which contributes the remainder of the pulse train, is not synchronized with gating angle or any other signal. Therefore its phase and frequency relationship to the hard pulse is impossible to predict.

Flip-flop's 1-FF, 2-FF and 3-FF are tied together in a ring counter. A flip-flop is turned ON (Q = 1) by its respective set signal (the 50 uSec pulse) and is turned OFF by the turning ON of the succeeding flip-flop. Consequently the only one of the three channels that may generate a picket fence pulse train at any one time, is the one in which the most recent 50 uSec pulse has occurred.

A third input is provided on the output NAND to prevent the picket fence pulse train from continuing past a critical gating angle regardless whether or not the flip flop has been reset. The action is performed by the negative transition of the SYNCH signals i.e., when SYNCH = 0 at $\alpha = 230^{0}$ the picket fence pulse train is chopped OFF, hence tailend chop. This feature prevents the power thyristor from being gated for an extended time while it is reverse biased.

Gate pulse suppression is implemented first by stopping the oscillator pulses then by preventing the advance of the ringe counter. In this manner any hard pulse which began prior to $\overline{GPS}$ going go logic 0 will not be shortened by gate pulse suppression but allowed to continue for the full 50 uSec. This prevents the power thyristor from receiving any weak pulses. As long as $\overline{GPS}$ is a logic 1 the gate pulses are generated in a normal manner.

Important waveforms pertaining to pulse 1 are shown in Figure II - 9.

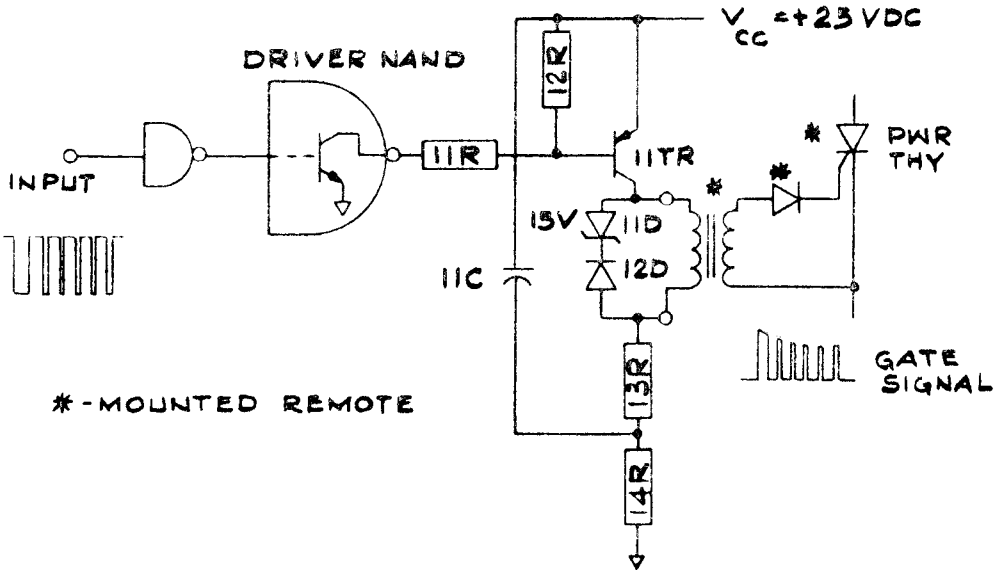


GATING WAVEFORMS
FIGURE II-9

E. Thyristor Gate Driver (TGD)

Six driver stages are located on each printed circuit board. All are identical and Figure II - 10 shows functionally the operation of a single stage.

The periodicity of the signal applied to the pulse transformer is a function only of the input signal, however, the output amplitude is of the form of an exponential decay. This shaping provides a high current, high voltage leading edge on the pulse for hard firing the power thyristor. The remainder of the pulse train decays to a lower level, thus reducing gate dissipation in thyristor while insuring that it is gated ON. The rise times of the output pulses are in the sub-microsecond region.



TGD
FIGURE II-10

A logic 1 at the input, which is the same as the input open circuited, results in a logic 1 at the output of the driver NAND which cuts off transistor 11TR. When a logic 0 is applied at the input the open collector transistor of the driver NAND pulls resistor 11R low turning ON transistor 11TR.

Before the long first pulse of the picket fence train, capacitor 11C has been fully charged to the power supply voltage (+25). Thus the initial current through the transformer primary is limited by resistor 13R only, thereby applying the high power leading edge of the pulse train to the thyristor gate. As more of the picket fence pulses follow, the capacitor is discharged to the level set by the voltage divider formed by 14R and 13R plus the transformer impedance. This reduces the voltage and current of the gate signal. Hence the exponential envelope of the pulse train.

Diode 12D and zener diode 11D clip the flyback voltage of the pulse transformer thus protecting transistor 11TR from excessive voltage. The 15 volt zener, 11D allows enough voltage across the pulse transformer secondary for it to reset between pulses.

There are four inputs which will prevent pulsing even while inputs are receiving gate pulses. Terminal 37 has to be a "0" (PSC) for pulsing to be allowed; it is used to interlock with the current feedback (pot board) and GPS protection (sequence and protection board) so that if either board is pulled and overcurrents are not protected for, pulsing is not allowed. Terminal 15 ($\overline{GPS}$) has to be a "1" except for the first 100 usec for pulsing to be allowed; this GPS function has a built in time delay on the TGD board which prevents suppression of pulses for 100 usec after a logic "0" appears so that thyristors will receive any previously initiated hard gate pulse. This in turn assures that thyristors be fully turned on to carry fault

current which started gate pulse suppression. Terminal 41 has to be a "1" and is used for the ENF or ENR function. Terminal 11 has to be a "1" and is used for the $\overline{INH}$ function which goes to a "0" 100 usec or so after GPS.

When this board is used for parallel bridges (TGD output fans out to GPAs) 11C, 11D, and 12D are eliminated; 13R and 14R are replaced with a jumper (short). Then the output is straight amplification with no waveshaping. This wave shaping function is picked up and performed in a similar manner on the GPAs. As GPAs have no functions employed except for amplification and waveshaping for parallel bridges further discussion in a separate section is not required.

III. TROUBLESHOOTING

Most boards employed in the gating system are complex which makes it difficult to troubleshoot on a component basis. Also many boards require special test equipment to be assured they are operating within specification, not just operational, should components be replaced in the field.

Troubleshooting can be employed on a functional basis, checking that waveforms are correct or incorrect at critical points by using waveforms and functions described in this IL, with the drive interconnecting diagram. Also replacing a suspected bad board with a known good board is useful. It is best to trace a problem to a functional area prior to changing of boards, as wholesale changing is likely to cause more confusion then enlightenment. It is expected that defective boards will be returned to Westinghouse for repair.