CURRENT SENSOR (DUAL CONVERTER)

I. DESCRIPTION

This module is used to sense the dc output current in C-56 Thyristor Power Systems as described in IL 16-800-126. It also contains a gate pulse suppression circuit and a phase sequence and single phase detector circuit.

The six phase double-way rectifier 5D to 10D obtains ac signals from a set of two open delta connected current transformers (CT), mounted on the thyristor power converter (TPM), which monitor the ac current flowing into terminals U and V of the TPM. This rectifier is loaded by two burden resistors, 1R and 2R, across which appear signals of the same waveform as the dc output current of the TPM and of a magnitude proportional to the TPM dc output current. Both polarities of the signal are available at terminals $+i_a$ and $-i_a$; the correct polarity is selected with relays 1CR and 2CR by the reversing logic module.

The voltage across burden resistor 2R is applied through resistor 4R to the gate of thyristor 1TH. If this current overcomes the adjustable bias from potentiometer 4P, the thyristor will turn on, which in turn will short out the +35V supply voltage for the GPG (gate pulse generator). Removal of this voltage effectively suppresses the GPG from releasing any further gate pulses. After such gate pulse suppression has occurred, the thyristor can be reset to its blocking state by temporarily energizing relay 86X.

The level at which suppression occurs is adjustable by potentiometer 4P. This level can be lowered for reverse current by the recalibration potentiometer 5P. Figure 1 gives sensitivity values for these adjustments.

The phase sequence and single phase detector circuit consists of the phase shifting network 10R - 5C supplied by two 120° displaced phase to PSC voltages obtained from the gate control transformer. Depending on the phase sequence, the voltage applied to diode 16D is either large enough (improper sequence) or not large enough (proper sequence) to overcome the breakdown voltage of the zener diode 17D. Whenever the breakdown voltage of the zener diode 17D is overcome, gate pulse suppression occurs. If any primary phase (R, S, T) is absent (single phasing), the voltage applied to diode 16D is large enough to initiate gate pulse suppression. Capacitor 1C serves to delay actuation for approximately 50 ms.

Input 33 is reserved for external suppression if desired.

II. SPECIFICATIONS AND RATINGS

Gain: $i_a = I_a \frac{Np}{Ns}$ (20 OHM)

where: i_a = output signal in volts

I_a = output current of TPM in amperes

Np = primary CT turns

N_S = secondary CT turns

Ambient Temperature: 0 to 55°C

Power Requirements: PSP: +24V ±0.5V 20mA

PSN: -24V ± 0.5V ... 30mA

Primary Turns: Selected so that the output voltage signal (i_a) for maximum TPM current will be between 8V to 16V.

Secondary Turns: S#1295A03G01 - 1000T
S#1295A03G02 - 2000T

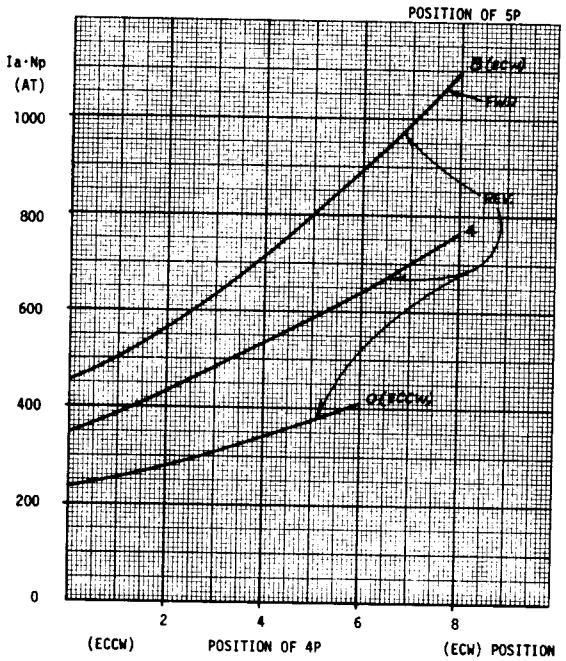
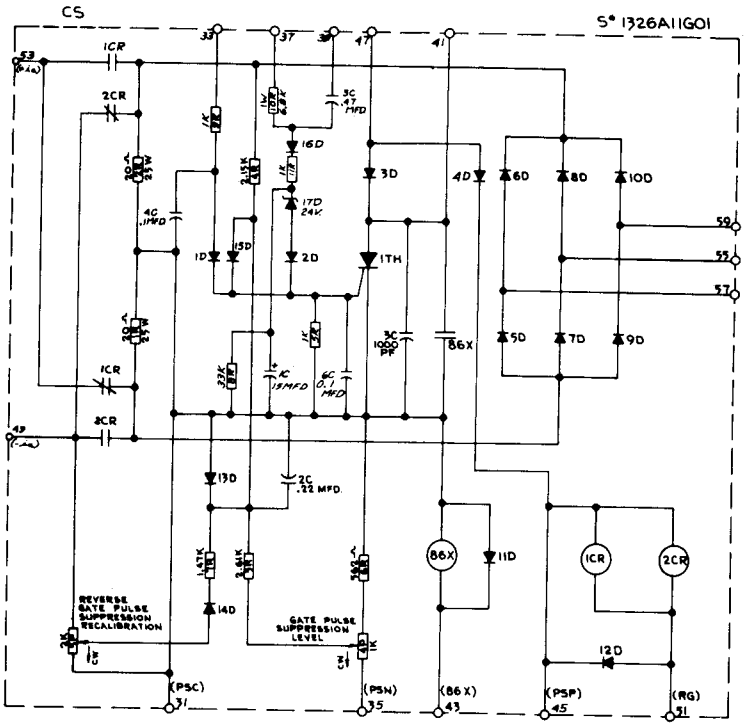


FIGURE 1 GATE PULSE SUPPRESSION ADJUSTMENT



NOTE - ICR AND 2CR PICKED UP FOR FORWARD OPERATION
ALL RESISTORS 0.5 W UNLESS SPECIFIED

CURRENT SENSOR (DUAL CONVERTER) SCHEMATIC DIAGRAM

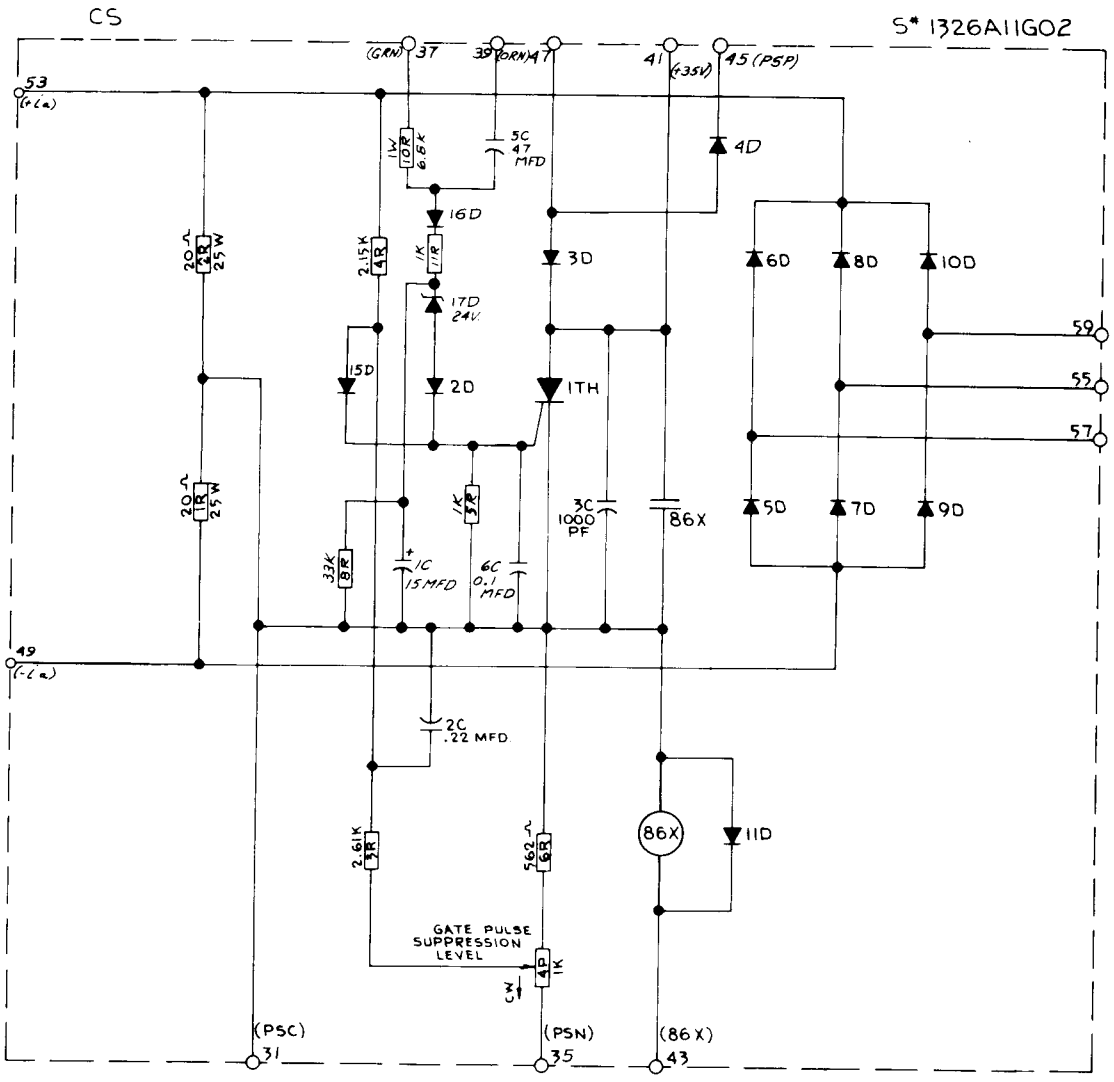
CURRENT SENSOR
(SINGLE CONVERTER)

I. DESCRIPTION

This module is used to sense the dc output current in C-56 Thyristor Power Systems as described in I.L. 16-800-126. It also contains a gate pulse suppression circuit and a phase sequence and single phase detector circuit. The description for the current sensor for dual converters applies with the following exceptions:

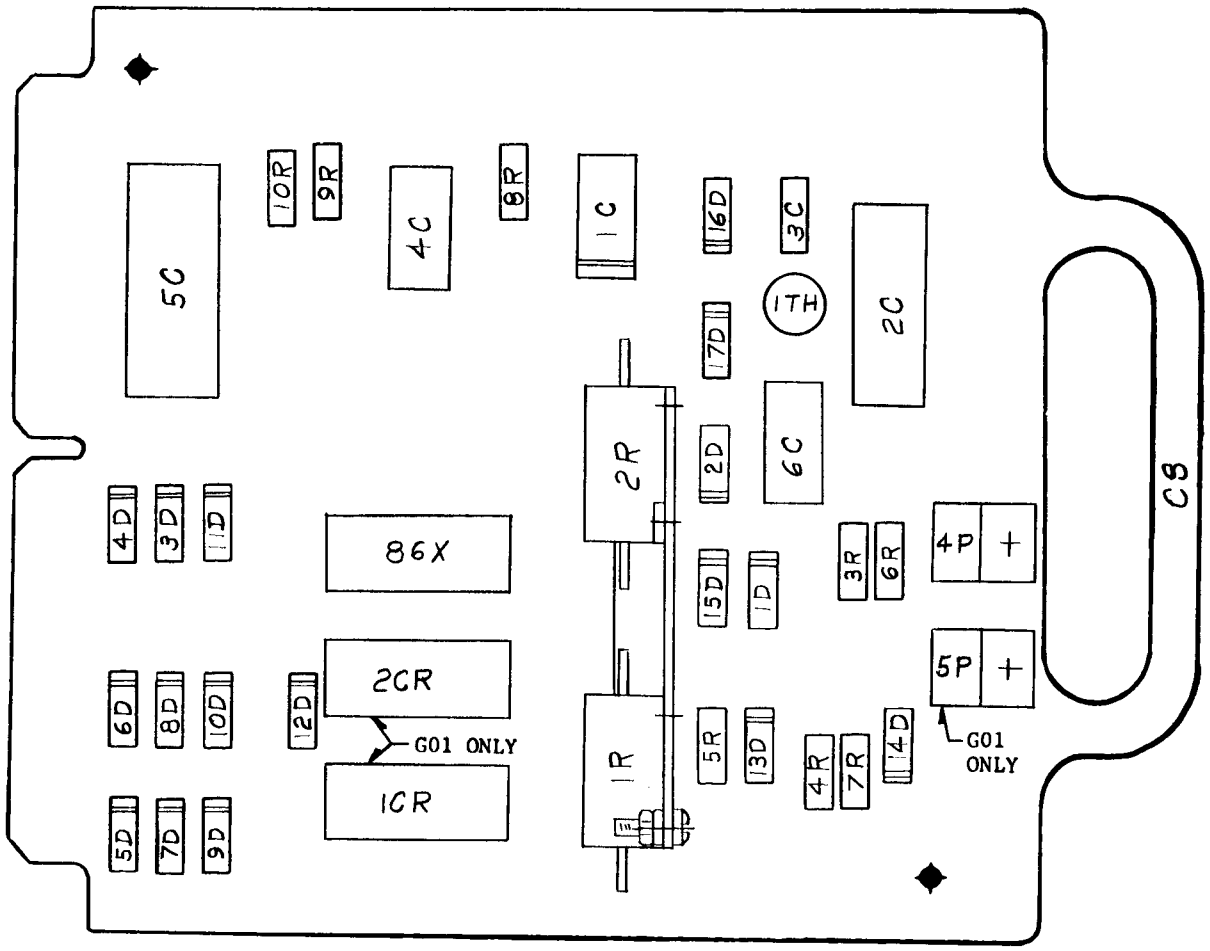
a) There are no reversing relays 1CR and 2CR.

b) There is no recalibration potentiometer 5P.



NOTE - ALL RESISTORS 0.5 W UNLESS SPECIFIED

CURRENT SENSOR (SINGLE CONVERTER) SCHEMATIC DIAGRAM



PC CARD (Front View)