C105 DIFFERENTIAL AMPLIFIER

I. INTRODUCTION

The C105 differential amplifier is a high gain DC amplifier with differential input - differential output capabilities. It is designed to be used as an operational amplifier, where common-mode rejection to provide effective isolation for input circuits, or the availability of two outputs of opposite polarity is required.

There are three designs of the C105 differential amplifier, C105-A C105-B and C105-C. Differences among the three are in selection of the resistors of the collector and emitter circuits of the output stages which determine output current and voltage capabilities. Other than output capabilities, all designs operate identically.

Figure 1 is a picture of the S-56F voltage sensor with the C105-C differential amplifier portion outlined with dotted lines.

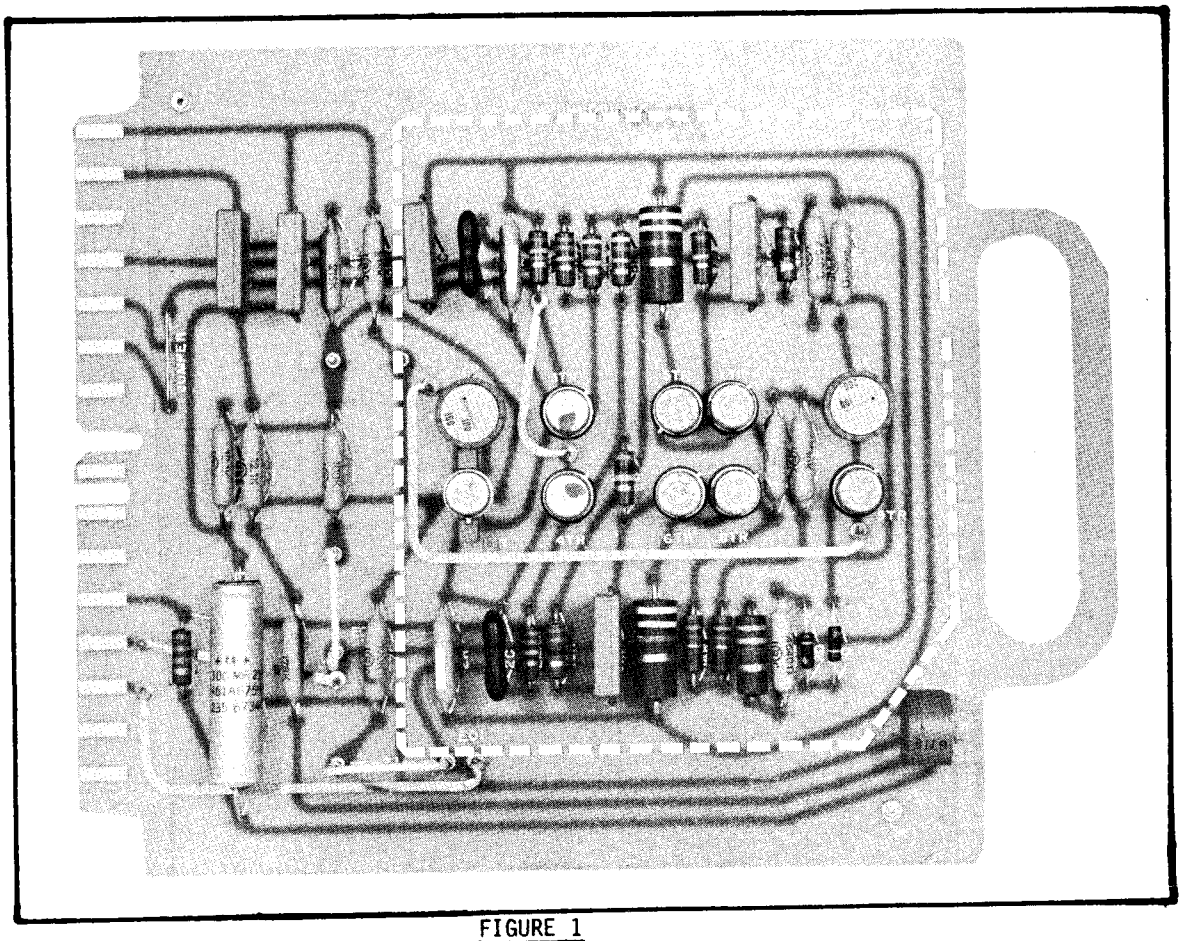

FIGURE 1

The effect of resistor selection (13R,14R,15R,16R,20R) on output current and voltage capabilities and power supply requirements is listed in the characteristics and ratings section. Electrical description of operation which follows applys equally to all amplifier types.

II. DESCRIPTION

The differential amplifier will be described with reference to its schematic diagram, figure 2. It has two inputs (B1, B2) and two outputs (E01, E02). The circuit provides complete symmetry, when comparing the two halves of the differential amplifier, from input to output to minimize common-mode disturbances due to variations in temperature, power supply voltage, etc.

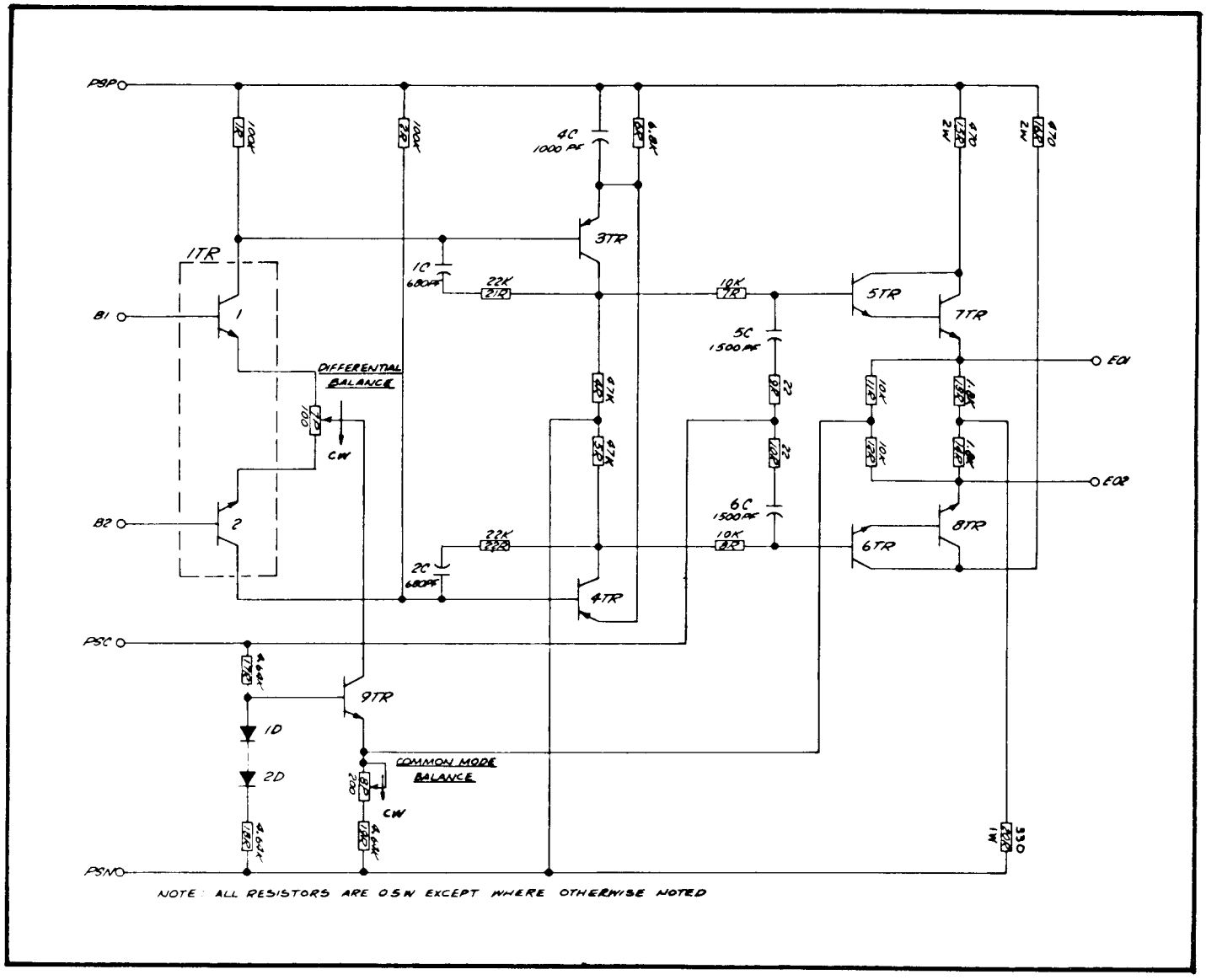

FIGURE 2

A small difference voltage applied between B1 and B2 is amplified through two differential stages. The first differential stage includes transistor 1TR which has a matched pair of high gain silicon transistors mounted in a single TO-5 can, and the second stage includes transistors 3TR and 4TR. A d-c differential voltage gain of about 4000 is achieved in these two stages. A darlington connection of 5TR, 7TR and 6TR, 8TR for the last stage provides current gain for low output impedence and high output power as well as high impedence loading to the second differential stage. Potentiometer 7P is provided so that, with zero differential voltage between B1 and B2, outputs E01 and E02 can be adjusted to be equal; that is the outputs will have zero differential voltage. This differential circuit has a controlled attenuation versus frequency rate of 20-db per decade starting at approximately 100 hertz and extending through approximately 1 megahertz at 0-db. This frequency response is achieved through the use of R-C shaping circuits of resistors 21R, 22R and capacitors 1C, 2C together with resistors 7R 8R, 9R and 10R and capacitors 5C and 6C.

Transistor 9TR is used to provide a high gain common-mode feedback loop by taking the average of the two output voltages and feeding this back through 9TR to the common (emitter) connection of the first stage. Therefore, if equal signals are applied to B1 and B2, there will be practically no change in output voltages since common-mode signals are attenuated strongly by the common-mode feedback loop. Potentiometer 8P is provided so that the average of E01 and E02 can be adjusted to zero with respect to PSC; that is the common-mode voltage can be adjusted to zero. This common-mode loop is stabilized by the R-C circuit consisting of resistor 6R and capacitor 4C.

It should be noted that a positive voltage input to B1 with respect to B2 gives a positive voltage at E01 and a negative voltage at E02. To provide negative feedback, for operation as an operational amplifier, E02 is connected through a feedback impedence to B1 and E01 is connected through a feedback impedence to B2. In operation the voltage at E01 will be of equal magnitude to E02 but of opposite polarity.

III. APPLICATION INFORMATION

Calculation of the gain of a differential input-differential output operational amplifier can be somewhat different than the conventional single feedback operational amplifier since two feedback paths may be available. For a review of operational amplifier theory, refer to I.L. 16-800-48A.

The following assumptions will be made to obtain the transfer function of the C105 operational amplifier. These assumptions introduce negligible error because of high differential gain and high common-mode loop gain.

(1) Input current to B_1, B_2 = 0
(2) Amplifier Drift and Offset = 0
(3) $V_{B1} = V_{B2}$
(4) E02 = -E01

By writing the equations for the voltage at B_1 and B_2 and the currents I_1 and I_2 as shown in figure 3, there is:

(1) $V_{B1} = e_d - I_1 Z_1$
(2) $V_{B2} = -I_2 Z_2$
(3) $I_1 = \dfrac{e_d - E02}{Z_1 + Z_3}$
(4) $I_2 = \dfrac{-E01}{Z_2 + Z_4}$

With VB1 = VB2 and substituting for I_1 and I_2:

(5) $e_d - \dfrac{e_d - E02}{Z_1 + Z_3} Z_1 = \dfrac{E01}{Z_2 + Z_4} Z_2$

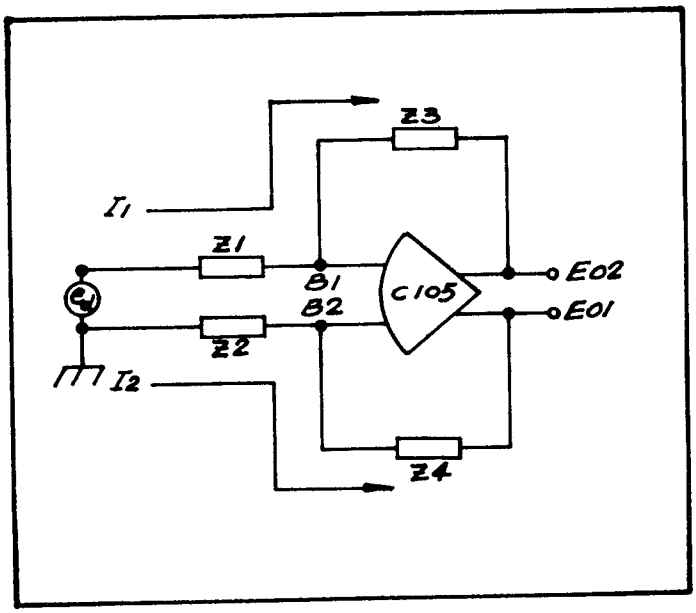

Figure 3

Since E02 = -E01:

$$(6) \qquad E02 = \frac{-e_d \dfrac{Z_3}{Z_1 + Z_3}}{\dfrac{Z_1}{Z_1 + Z_3} + \dfrac{Z_2}{Z_2 + Z_4}}$$

For the case where $Z_1 = Z_2$ and $Z_3 = Z_4$, which is often the case to obtain good common-mode rejection, equation 6 reduced to:

$$(7) \qquad E02 = \frac{-e_d \, Z_3}{2 \, Z_1}$$

If only a single feedback impedance is used (Z_3), then Z_4 is set to a value of infinity and equation 6 reduces to:

$$(8) \qquad E02 = \frac{-e_d \, Z_3}{Z_1}$$

Equation 8 is the same as is obtained for a single output operational amplifier and is twice the value of equation 7 when two equal feedback impedances are used.

The impedances looking out of B1 and B2 must be matched if low voltage and current drift is to be obtained over a wide range of temperature variations. This matching can be accomplished when unequal feedback impedances are used, but the use of symmetrical input and feedback impedances accomplish this matching easily.

Symmetrical input and feedback impedances are necessary if good common-mode rejection is desired. The common-mode rejection ratio of the C105 amplifier is sufficiently high so that common-mode rejection of the operational amplifier is essentially determined by the matching of the input and feedback impedances. The common-mode rejection ratio is defined as:

$$(9) \qquad CMRR = \frac{\text{GAIN (DIFFERENTIAL)}}{\text{GAIN (COMMON-MODE)}} = \frac{Ad}{Ac}.$$

Due to the length of the derivation, the common-mode gain will not be derived. The effect on the output voltage due to a common-mode voltage and to mismatch of input and feedback impedance will be explained with reference to Figure 4.

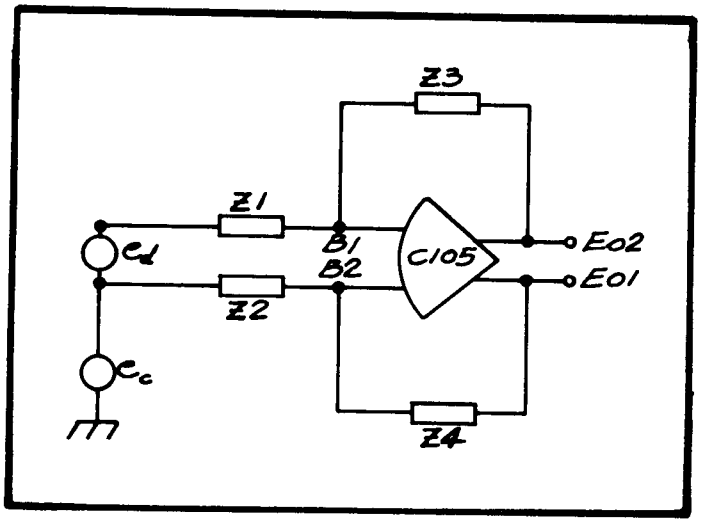

Figure 4

The differential voltage is e_d and the common-mode voltage is e_c. While the operational amplifier design calls for $Z_1 = Z_2$ and $Z_3 = Z_4$, there will be a slight mismatch of impedances due to component tolerances.

Let $Z_2 = \alpha Z_1$ and $Z_4 = \beta Z_3$ and the common-mode gain can be expressed as follows:

$$(10) \qquad Ac = - \frac{Z_1 Z_3 (\alpha - \beta)}{2 \, Z_1 \left(\alpha Z_1 + \frac{\alpha + \beta}{2} Z_3\right)}$$

From equation 7:

$$(11) \qquad Ad = \frac{-Z_3}{2Z_1}$$

Therefore, equation 9 becomes:

$$(12)\quad CMRR = \frac{-\frac{Z_3}{2Z_1}}{-\frac{Z_1Z_3(\alpha-\beta)}{2Z_1\left(\alpha Z_1 + \frac{\alpha+\beta}{2}Z_3\right)}} = \frac{\alpha Z_1 + \frac{\alpha+\beta}{2}Z_3}{Z_1(\alpha-\beta)}$$

For an example; if Z_1 = 100K and Z_3 = 10K and 1% resistors are used, for worst case condition (α = 1.02, β = .98) the CMRR would be:

$$(13)\quad CMRR = \frac{1.02 \times 100K + 10K}{100K\ (.04)} = \frac{11.02}{.4} = 27.5$$

That is the differential voltage is amplified 27.5 times as much as the common-mode voltage. When α and β equals 1, (that is the impedances match exactly) the common-mode gain goes to zero and the CMRR is determined by the C105 amplifier which has a CMRR of greater than 1000. As seen from equation 12, the matching of input and feedback impedances is necessary if rejection of common-mode voltages is to be achieved.

IV. CHARACTERISTICS AND RATINGS

A. Allowable operating ambient temperature: 0 to 55°C

B. Differential gain: 4000 typical

C. Common-Mode Rejection Ratio: 1000 minimum.

D. Maximum common-mode level at B1, B2: ±10V.

E. Differential Drift (B1-B2): Typical voltage drift = 5μv/°C; Typical current drift = .5 mμa/°C.

F. Power Supply Requirements:

	C105-A	C105-B	C105-C
PSP:	+24; 30 ma	+24V; 45 ma	+24V; 30 ma
PSN:	-24; 30 ma	-24V; 45 ma	-24V; 30 ma

G. Output Swing at E01 and E02:

C105-A	C105-B	C105-C
±12V; 4 ma	±14V· 7 ma	±11V; 3.5 ma