I.L. 16-800-324

ACCURCON II STATIC ADJUSTABLE-FREQUENCY INVERTERS

SERVICE MANUAL

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POWER MODULE - DUAL STAGE DRAWER

TYPES 35 AND 70

Schematic Diagram 2935D40
Wiring Diagram 2935D41

FUNCTION

The power module is a drawer containing two complete inverter stages. (Refer to photograph.) The Types 35 and 70 differ only in rating, having identical schematic and mechanical arrangements. These power modules are used to make up complete inverters of the desired power level and number of stages required for a particular application. The following description will apply to only one complete inverter stage.

The function of the inverter stage is to produce single-phase, square-wave AC output power when operated from a fixed DC bus volt. (Refer to "Basic Theory".) This is achieved by a single-phase bridge arrangement of four switching thyristors, which are caused to switch in sequence and timing determined by logic signals from the counter/driver board. The output of the single-phase inverter stage is applied to a single-phase transformer which is then connected to the load.

The AC single-phase power frequency thus produced will be in synchronism with the master oscillator. The average voltage output of the stage is controlled by the duration of the ON time of positive and negative half cycles, as determined by the logic signals.

OPERATION

Operation of the inverter stage is most easily seen by referring to the schematic and examining the following separate sections:

1. The power switching thyristors, SCR11-SCR12-SCR21-SCR22;
2. The turn-off or commutating circuitry, consisting of reactors 11L and 21L, capacitors 11C-12C and 21C-22C;
3. Free-wheeling circuitry to handle the flow of reactive load current, consisting of diodes 13D-14D-23D-24D and damping resistance connected externally by RRP and RRN;
4. Special circuitry for recovery of excess commutation energy, which comprises reactors 13L-15L-23L-25L and diodes 11D-12D-21D-22D; and
5. Protective circuitry which includes current-limiting fuses, surge suppressors, and thyristor delay reactors 12L-22L-24L.

Each of these sections will be described separately for clarity.

A. Power Switching Operation

Referring to schematic diagram PAGE 8 , it is seen that the switching thyristors are arranged in a single-phase bridge circuit, with the DC power bus connected at one pair of terminals (marked +300 DC and 0 V DC), and the load connected at the other pair of terminals (marked AC1 and AC2) of the bridge. It will be noted that each half of the bridge is symmetrical (left and right). Furthermore, the upper and lower thyristors are always switched at the same time in a complementary manner; THAT IS, WHEN SCR 11 is ON then SCR12 is OFF, and when SCR12 is ON then SCR11 is OFF. This must always be the case since simultaneous ON conditions for both SCR11-SCR12 would result in a short-circuit directly across the DC bus, blowing the protective fuse 1FU. With these points kept in mind, the operation of a complete cycle of power flow will be discussed.

Figure 1 shows typical single-phase voltage waveforms seen at the output of any one power stage. The waveshape at maximum frequency or rated frequency will show almost complete conduction during positive and negative half cycles. The waveshape at minimum frequency in adjustable frequency inverter will show a conduction of perhaps only 30 degrees out of the possible 180 degrees. Full 180-degree conduction will only occur at maximum design frequency under conditions of low input line voltage. This is, in effect, a safety margin which permits maximum output even with low DC bus voltage input. Of course, if the voltage falls below the designed limits as specified, then malfunction may be expected to occur, depending on factors of loading, frequency, etc.

Figure 2 shows a typical mid-frequency range, nominal DC voltage, voltage waveshape, with load current superimposed. (Because of the output transformer interconnections, this current is very nearly sinusoidal.) This particular case shows unity power factor loading (resistive load), since current is shown in phase with the voltage. The current flow may be divided into six parts, shown shaded, and the path of current flow examined for each part of the cycle.

1. During interval A (SCR11-22 ON), current and voltage are both positive, producing positive power output to the load. Current flow is: from +300 DC, through SCR11 to the load AC1-AC2, then through SCR22 to the negative bus OVDC.

2. During interval B (SCR 12-22 ON), voltage is zero while the current is still positive. This represents no power output to the load from this stage, but merely a free-wheeling of current. Current flow is: from the load at AC2, through SCR22 to 0 VDC, through an external damping resistor at plugs 2-3 to RRN, through 14D and back to the load at AC1.

3. During interval C (SCR 12-22 ON), the voltage is still zero but the current has reversed direction. The new free-wheeling path for current flow is: from the load at AC1, through SCR12 to 0 VDC, through external damping resistor at plugs 2-3 to RRN, through 34D and back to the load at AC2.

4. During interval D (SCR12-21 ON), the voltage and current are both negative, again producing positive power output to the load. Current flow is: from +300 DC, through SCR21 to the load AC2-AC1, then through SCR12 to the negative bus OVDC.

5. During interval E (SCR 11-21 ON), free wheeling again takes place. Current flow is: from the load at AC1, through diode to RRP, through the external damping resistor at plugs 6-7 to +300 DC, through SCR21 and back to the load at AC2.

6. During interval F (SCR11-21 ON), free wheeling continues but with current flow reversed. The current flow is: from the load at AC2, through diode 23D to RRP, through an external damping resistor at plugs 6-7 to +300 DC, through SCR11 and back to the load at AC1.

NOTE: Observe from the above, that during every interval either SCR11 or SCR21 is switched ON. It is for this reason that these thyristors are referred to as "ON-dominant." Conversely, thyristors SCR12 and SCR22 are termed "OFF-dominant." This is convenient to remember when considering waveforms.

The preceding case described a resistive or unity power-factor load. This is not typical, however, of most loads which are normally inductive in nature. For this case,refer to Figure 3 which shows current lagging the voltage by a full 90 degrees. Again, the cycle is divided into six intervals.

1. During interval A (SCR11-22 ON), current and voltage are both positive, producing positive power output to the load. Current flow is: from +300 DC, through SCR11 to the load AC1-AC2, then through SCR22 to the negative bus OVDC.

2. During interval B (SCR 12-22 ON), voltage is zero while the current is still positive. This represents no power output to the load from this stage, but merely a free-wheeling of current. Current flow is: from the load at AC2, through SCR22 to 0 VDC, through an external damping resistor at plugs 2-3 to RRN, through 14D and back to the load at AC1.

3. During interval C (SCR12-21 ON), the voltage has reversed while the current continues in the positive direction. This represents negative, or regenerative power from the load, which must be pumped back to the DC power supply. This power obviously does not go backward through the rectifier supply, but does help supply power to the other stages of the inverter. In addition, a large input capacitor stores excess energy during part of the cycle. Current flow is: from the load at AC2, through diode 23D to RRP, then through the external damping resistor at plugs 6-7 to +300 DC, next through the DC supply bus to 0 VDC (regeneration), then through the external damping resistor at plugs 2-3 to RRN, through diode 14D and back to the load at AC1.

4. During interval D (SCR12-21 ON), the current finally reverses and flows in the same direction as the negative voltage. This is now positive power flow again to the load. The current path is: from +300 DC, through SCR21 to the load at AC2-AC1, then through SCR12 to the negative bus 0 VDC.

5. During interval E (SCR 11-21 ON), free wheeling again takes place. Current flow is: from the load at AC1, through diode to RRP, through the external damping resistor at plugs 6-7 to +300 DC, through SCR21 and back to the load at AC2.

6. During interval F (SCR11-22 ON), regeneration again takes place because the load current opposes the stage applied voltage. Negative power is taken from the load and pumped back to the DC supply. Current flow is: from the load at AC1, through diode 13D to RRP, then through the external damping resistor at plugs 6-7 to +300 DC, next through the external damping resistor at plugs 2-3 to RRN, through diode 24D and back to the load at AC2.

B. Turn-off, or Commutating Operation

The turn-off mechanism for thyristor switches has been discussed in the section on "Basic Theory". On schematic diagram PAGE 8 , the commutating capacitors which store the switching energy are 11C-12C and 21C-22C. The commutating reactors are 11L and 21L, center tapped.

C. Free-wheeling Operation

Free-wheeling operation has been discussed under Section A, "Power Switching Operation." The elements utilized for the free-wheeling circuit include diodes 13D-23D, and the external damping resistor across plugs 6-7. During regeneration, the free-wheeling takes place with diodes 14D-24D, and the external resistor across plugs 2-3.

D. Recovery Circuit Operation

Since fixed values of commutating capacitors are used, each switching discharges the same amount of energy regardless of varying load requirements. These capacitors are designed to produce reliable turnoff when peak load is being switched, when minimum line voltage is being switched, when minimum line voltage is present, and when the load power factor is worst. Under normal conditions, the amount of switching energy required to turn off the thyristors is much less than the design amount. Unless some form of recovery circuit is used, this energy must be dissipated, and usually it would be through the thyristors. For these reasons, special circuitry has been added to the AccurCon Inverter stages to recover the bulk of this energy, resulting in much greater efficiency, and placing less strain on the semiconductor elements.

Each thyristor is shunted with a combination of reactance and a diode. These are 11D-13L, 12D-15L, 21D-23L, and 22D-25L. During actual commutation, the turn-off current switches through this circuit after the thyristor blocks. The current is then passed to the DC bus and recovered, instead of being dissipated in the devices. The greatest value of this circuitry is for light load operation, where the low requirements of turn-off would otherwise cause a great amount of energy to be wasted.

E. Protective Circuitry

Protection of the semiconductor elements falls into two main categories: overcurrent and surge suppression, both of which can cause failure in extremely short times. The thyristors across the DC bus form a path for short circuit if both should remain ON for even a few milliseconds. For this reason, fast-acting current-limiting fuses are provided to protect against thyristor damage during a mis-fire. These fuses have been very carefully selected and coordination with the specific thyristors used, and they must never be replaced with any other type of fuse without specific approval of the inverter manufacturer. Each fuse is arranged with a trigger fuse in parallel, which actuates a plunger upon blowing. The plunger then actuates the stage indicating light, and any alarm relay circuitry which may be used.

Surge suppression is provided by an RC suppressor around each semiconductor which is exposed to transients. This prevents rapidly changing voltages from imposing stress on the thyristor itself. The recovery diode 11D is likewise protected. The stage filter capacitors also afford protection from certain transient conditions.

Another form of protection for the thyristors is the delay reactor in series with each thyristor. These are delay reactors 12L-14L-22L-24L. Their purpose is to delay slightly the build-up of anode current after the instant of firing, in order to permit the thyristor crystal to become fully conducting before carrying full current. This is important in avoiding thyristor degradation which can be caused by excessive di/dt rates over a period of time.

TESTING

The output waveform of the stage is a good indication of the proper operation of that stage. When the output wave is clean and square, the stage is operating correctly. Loss of a fuse will usually produce a half wave only, or at best, a rounded full wave. In such cases, individual elements should be checked. An oscilloscope across the diodes or thyristors will indicate whether these are operating properly.

For convenience in testing, the schematic diagram is marked with lettered points, which are molded into the half stage. In addition, the drawer wiring diagram indicates clearly the location of all parts of the drawer.

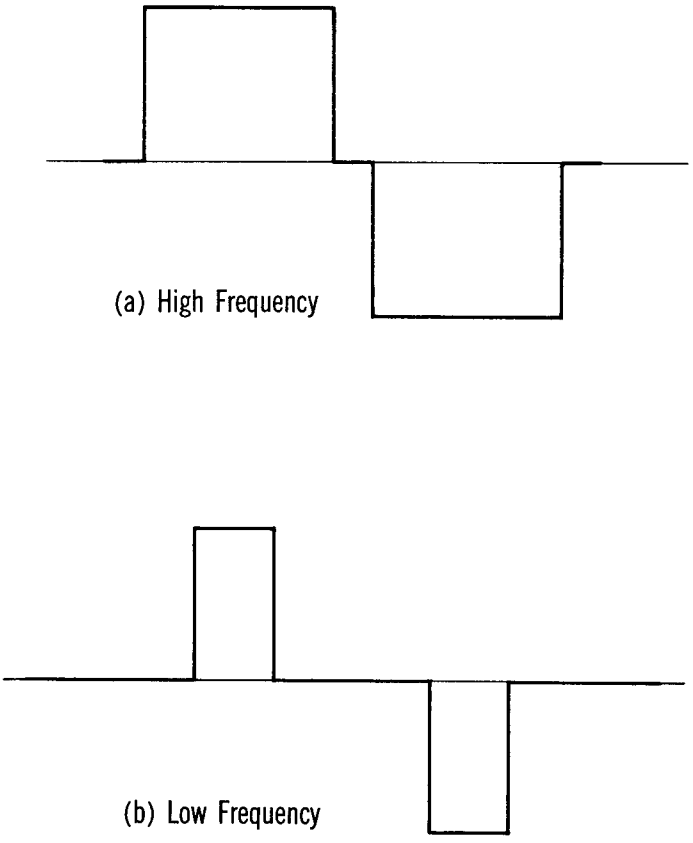


FIGURE 1 - TYPICAL STAGE OUTPUT WAVEFORMS

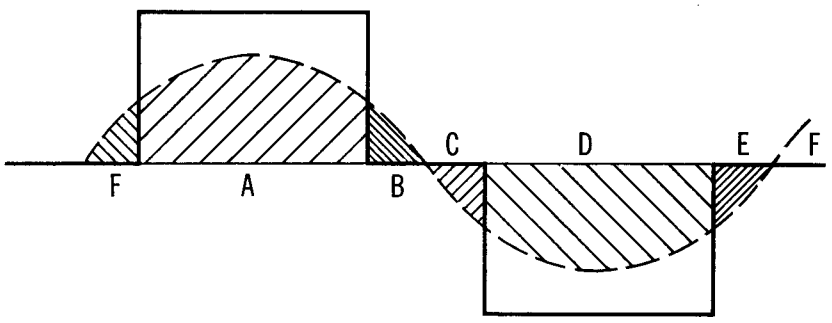


FIGURE 2 - STAGE OUTPUT, RESISTIVE LOAD

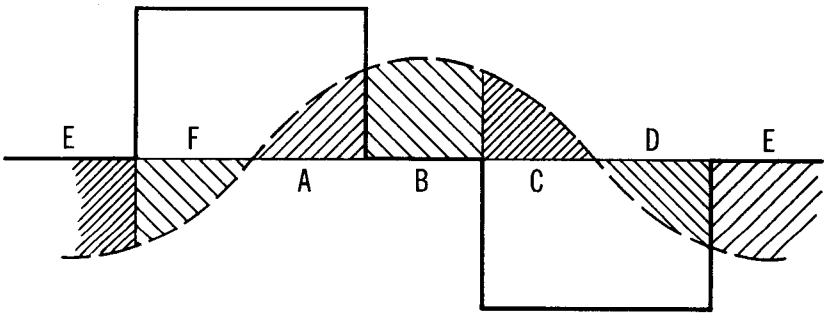
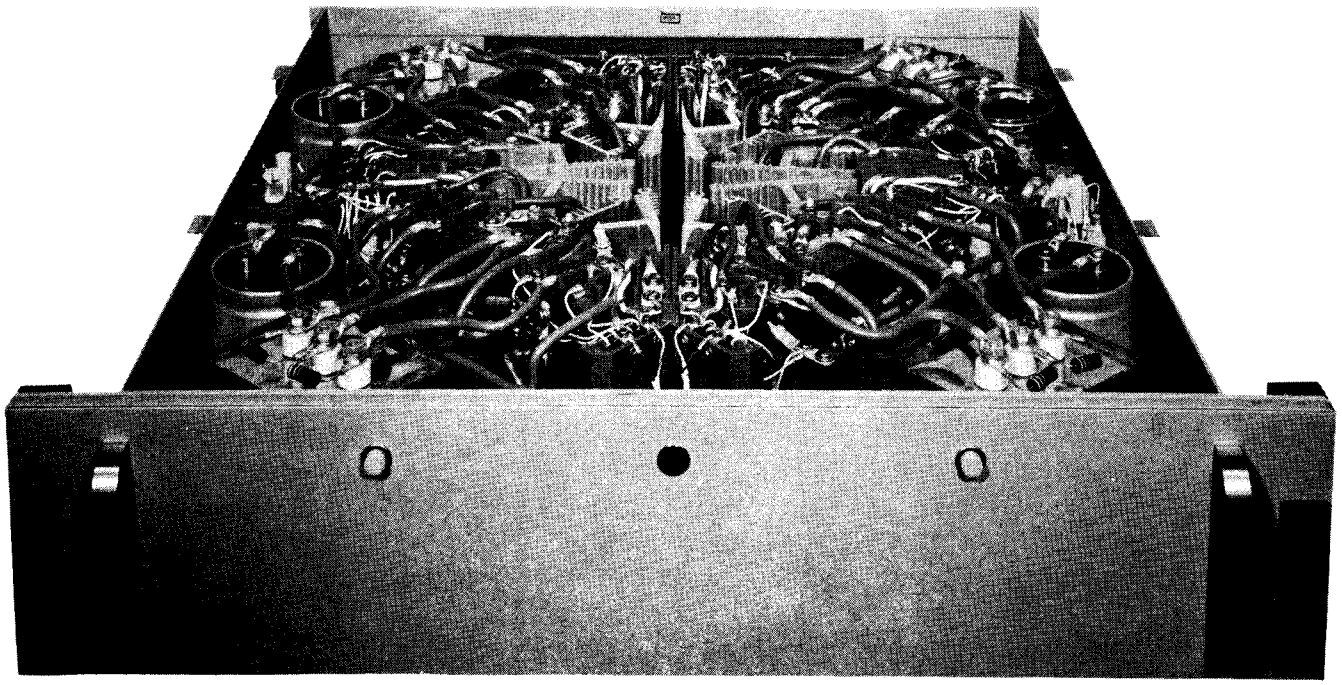
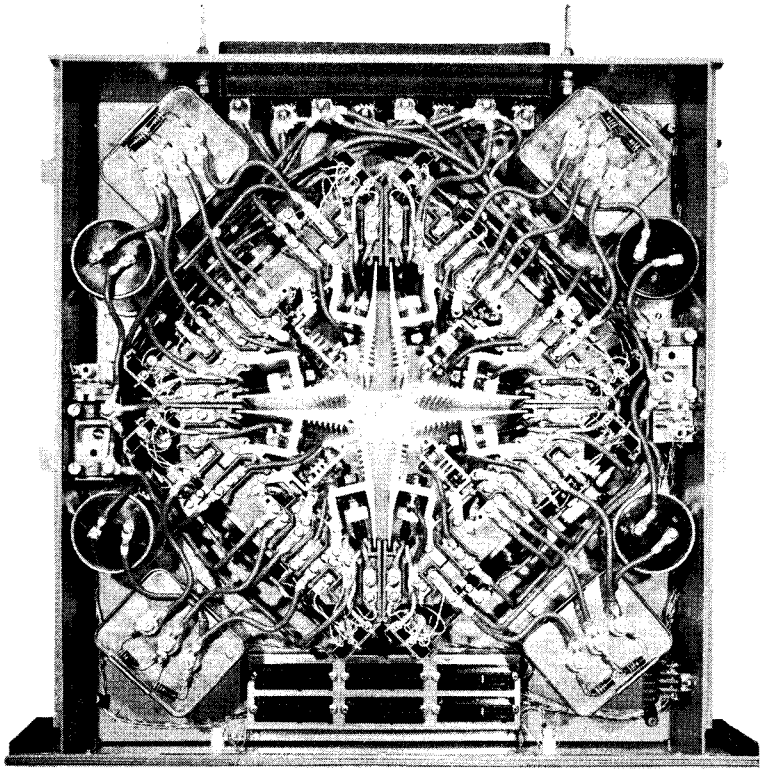


FIGURE 3 - STAGE OUTPUT, INDUCTIVE LOAD



TYPE 35 DUAL-STAGE DRAWER



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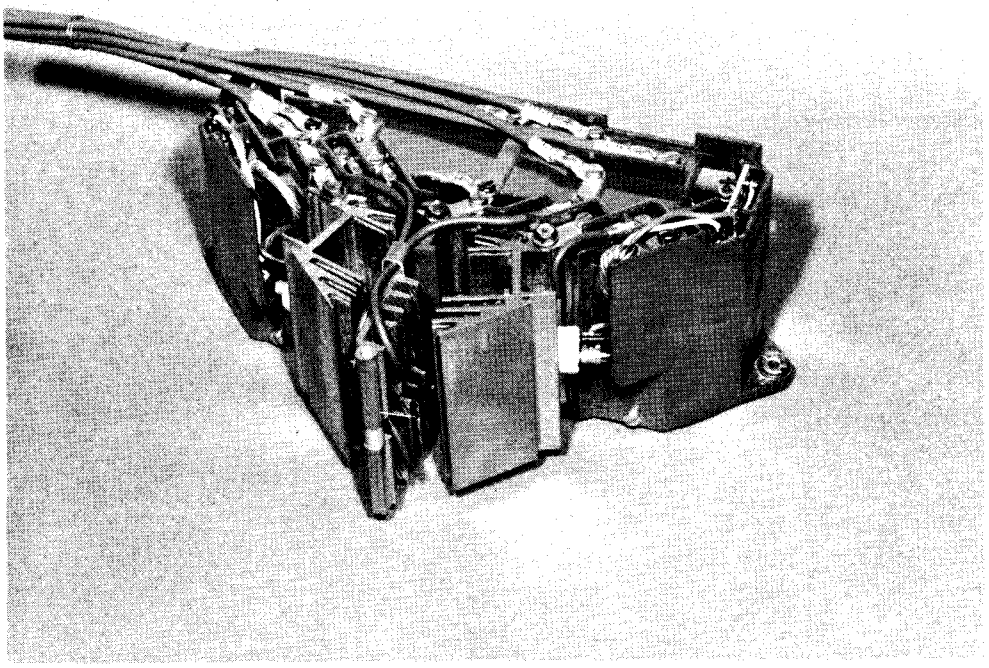

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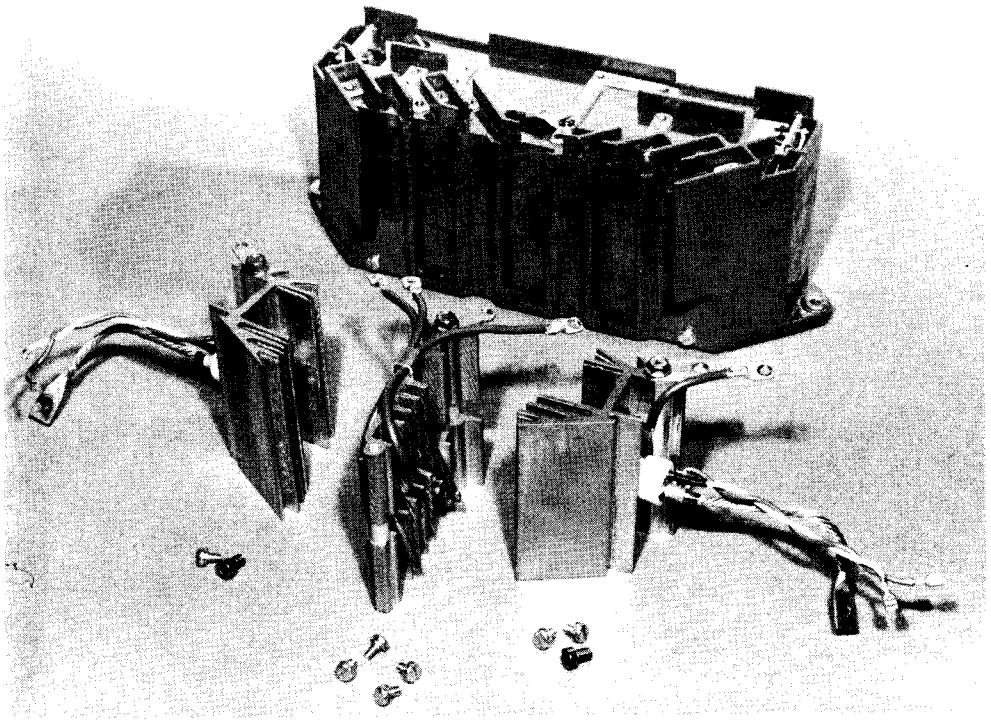

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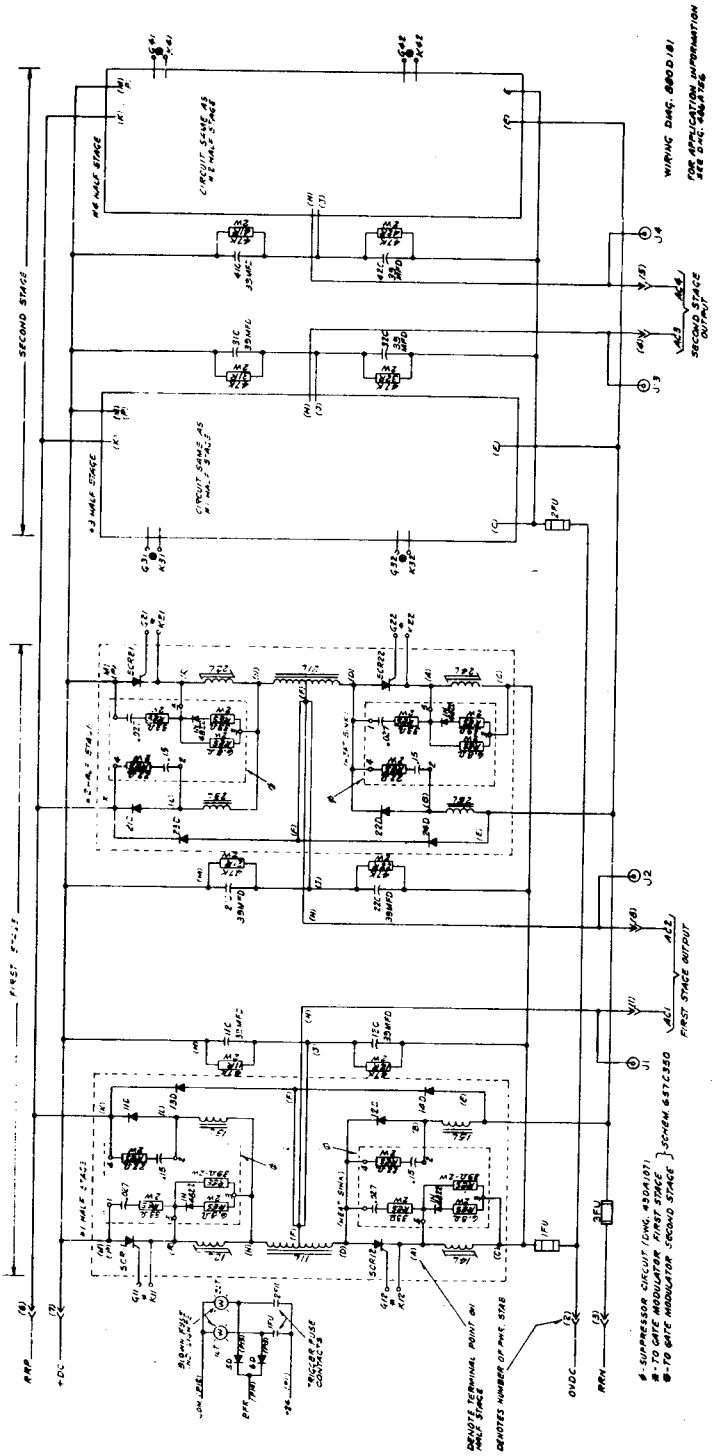

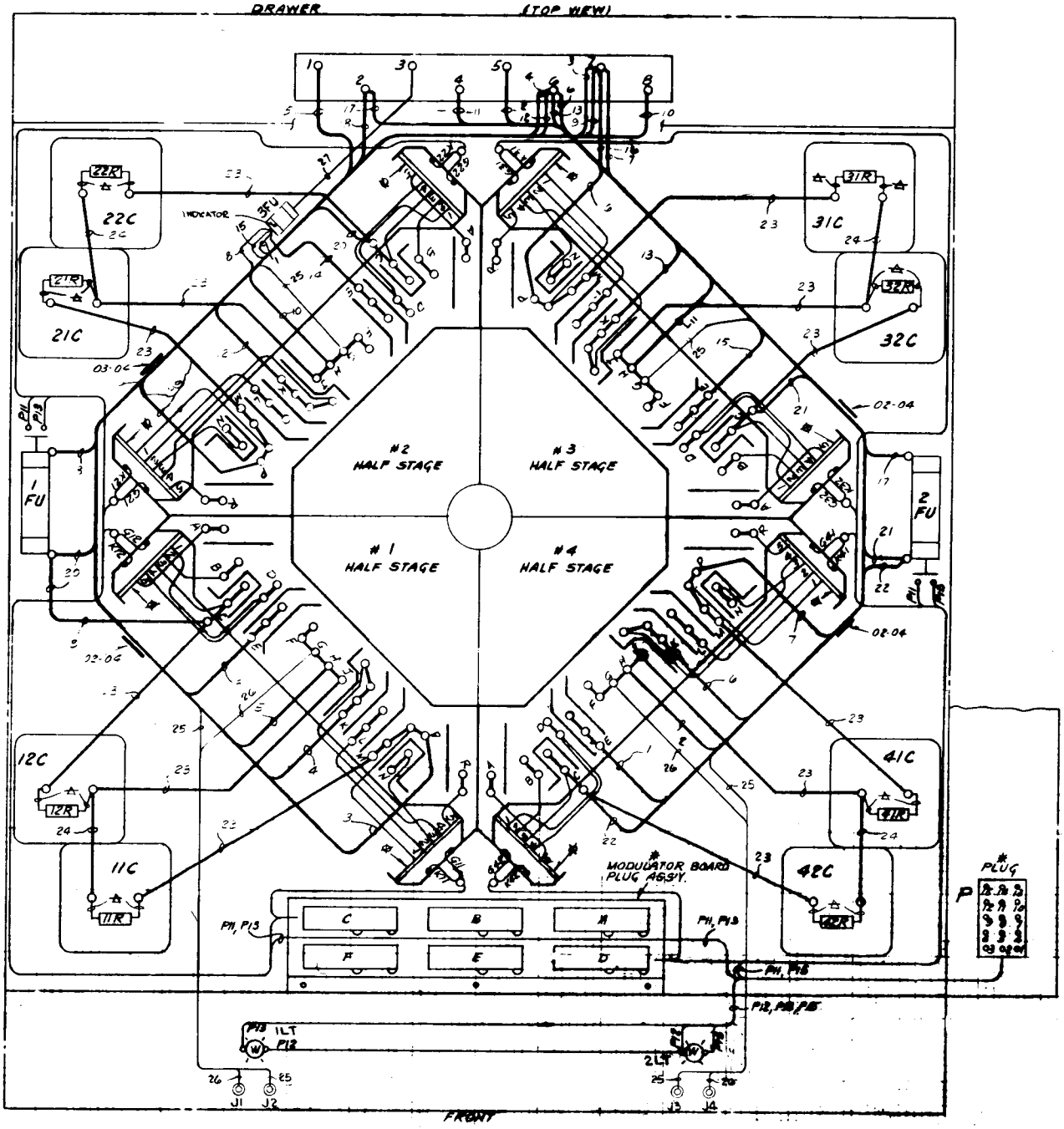
DRAWER
(TOP VIEW)
#2 HALF STAGE
#3 HALF STAGE
#1 HALF STAGE
#4 HALF STAGE
22C
21C
31C
32C
12C
11C
41C
42C
1 FU
2 FU
3FU
INDICATOR
MODULATOR BOARD PLUG ASS'Y.
PLUG
FRONT
J1
J2
J3
J4

ACCURCON A1101 LOGIC

I. FUNCTION

The A1101 control logic provides the basic control necessary for operation of three phase adjustable frequency AccurCon inverters from four thru fourteen stages.

The control consists of two parts:

1. A logic cage containing the printed circuit cards.
2. An input output (I-O) panel

These two subassemblies are mounted in the logic drawer which slides into the control cabinet. A picture of a logic drawer is shown in Figure 1.

Figure 2 shows a functional diagram of a four stage A1101 control. This functional diagram shows a breakdown of circuit functions by printed circuit card. Each board is enclosed by dotted lines. Each circuit function block is shown with signals entering and/or leaving. Signal flow direction is indicated by arrows. In each PC board block the name of the board, the general style number, and the edge connector position (position in the PC card enclosure) are indicated. Also shown on each signal is the terminal number at the edge connection of that board, therefore the complete wiring for a four stage controller is shown on this diagram. For further circuit details of the PC boards, refer to the schematics supplied with the drive. The control is expanded for additional stages by adding Phase Shifter Boards and the appropriate wiring.

The basic control contains five boards:

1. Power Supply
2. Oscillator
3. Voltage Regulator
4. Ring Counter
5. Phase Shifter

A sixth board, the A1101 Gate Modulator board, must be used in conjunction with the A1101 control. This board is located in the power drawers.

Any one of three optional boards can also be used in the control.

1. Cycling control
2. P-jump control
3. Buffer

Operation of these optional boards is described in separate IL's.

The main inputs to the logic drawer are:

a. Frequency reference signals
b. 230 VAC 1Ø control power
c. Voltage feedback signals from the inverter output
d. Sequencing controls

The main outputs from the logic drawer are:

a. Gate control cables for connecting signals and control power to the Gate Modulator boards in the power drawers.
b. Certain interlock and alarm signals.
c. Frequency meter signals.

II. OPERATION

For purposes of description the operation of the A1101 control is broken down into five sections:

1. Power supplies
2. Frequency control
3. Voltage control
4. Sequencing control
5. Gating control

A. Power Supplies

The input for the control power supplies for the A1101 logic is 230 V AC 1Ø. This input power is connected to 1TB of the I-O panel and stepped down in transformer 5T. The Rectifier module on the I-O panel provides full wave rectification and filtering of the two isolated secondaries on 5T. This provides +24V non-regulated voltage for the control logic. Capacitors 1C and 2C provide energy storage for logic power carryover in the event of a short utility line failure. This carryover time is a minimum of 0.5 sec. The +24V supplies are fed to the Power Supply Bd where they are regulated down to +13V. These supplies (P13 for positive 13V, N13 for negative 13V) are precision supplies (.1%) used for referencing and general electronic control. Adjustment of the +13 volt supplies is provided for by 1P on this board. The N13 supply tracks the P13 supply so only one adjustment is required.

Power supply common (PSC) is the quiet common used with the P13 and N13 supplies. Relay common (RC) is a non-sensitive common used for relay circuits and other non critical circuits. These two commons are tied together only at the Rectifier Module to prevent ground coupling noise problems.

The +24Vnon-regulated supply is also used for gating power. For this function the +24V is connected through two normally open contacts of the Gate Power (GP) relay to the gate control plugs.

The +24V supplies are fused on the Rectifier Module in the I-O panel. The +13V regulated supplies are fused on the Power Supply Board. Two LED's on this board indicate operation of the P13 and N13 supplies.

For redundant control power input a second 230VAC 1Ø input can be connected to 4T on the I-O panel. The two supplies are diode coupled at the output of the diode bridges on the Rectifier Module.

B. Frequency Control

For all applications, except when the Buffer Board is used, the frequency command is set externally be a 2.0K ohm potentiometer. For applications which have a Buffer Board, the input signal is either a zero to 10 vdc or 4 to 20 ma dc signal. Operation of the Buffer Board is described in I.L. 16-800-328.

Bias circuits on the Oscillator Board (A17) are used to provide adjustment of the maximum (MAX) and minimum (MIN) output frequencies of the inverter. The output frequency is linear with respect to potentiometer position between these two end stops.

The compelled low frequency (CLF) bias is connected in parallel with the frequency adjustment pot on the FREQ signal. This circuit provides a minimum output frequency of the inverter (normally 6 Hz) when the speed reference (FREQ) is switched off with an ON-OFF switch. The purpose of this circuit is to provide an inverter output frequency lower than the nominal minimum frequency to reduce transients during motor starting.

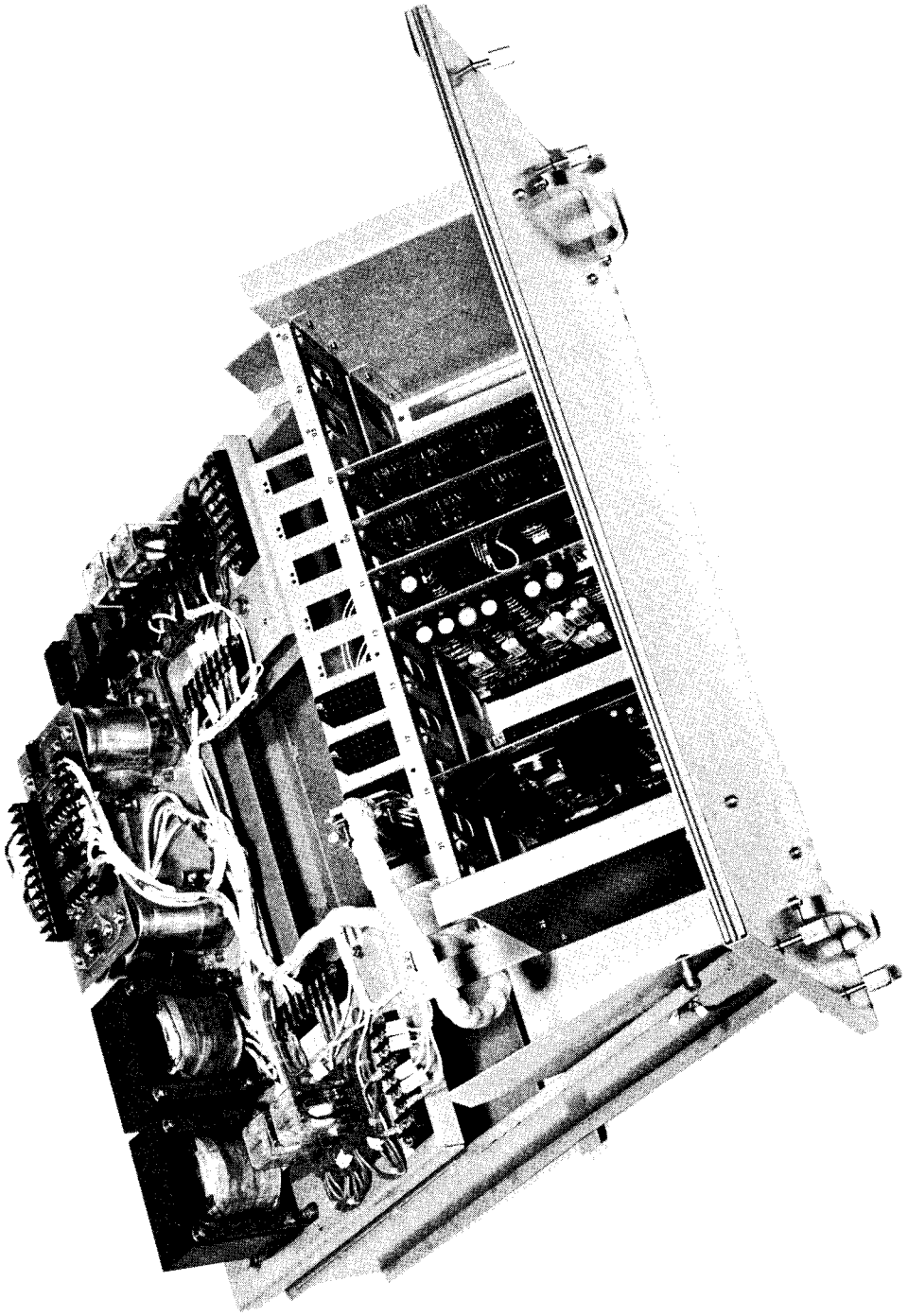

FIGURE 1

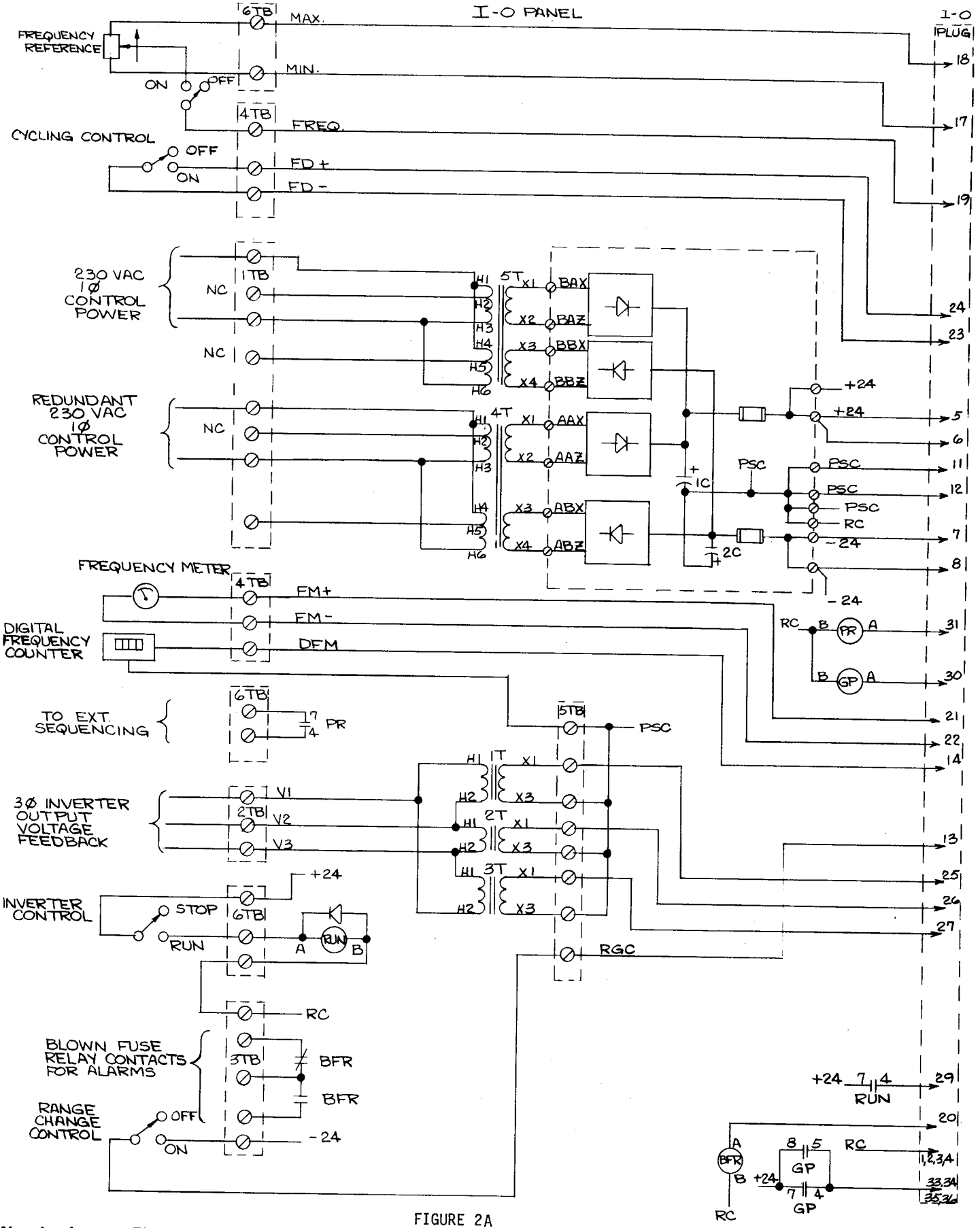

FIGURE 2A

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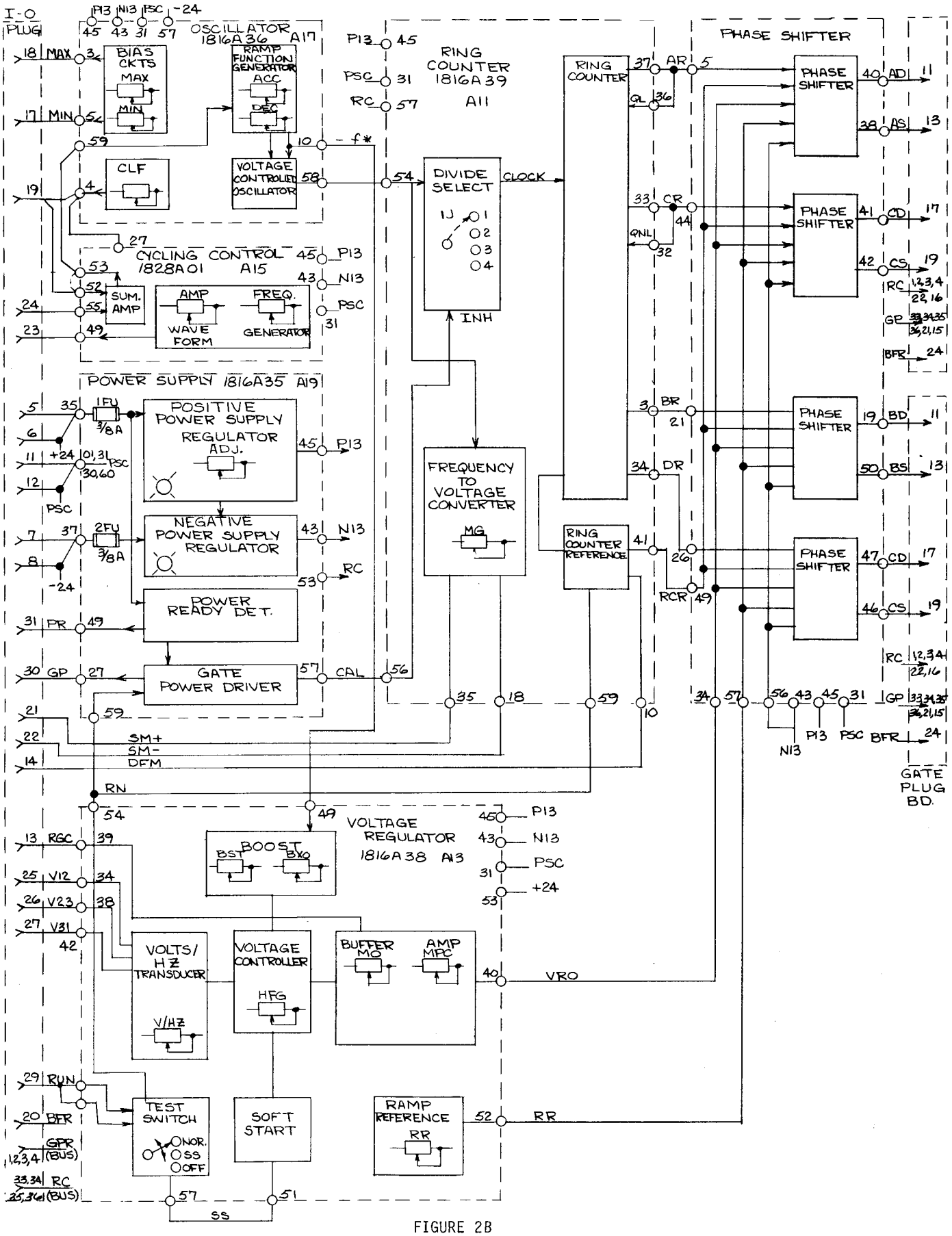

I-O PLUG
OSCILLATOR 1816A36 A17
BIAS CKTS
MAX
MIN
RAMP FUNCTION GENERATOR
ACC
DEC
CLF
VOLTAGE CONTROLLED OSCILLATOR
CYCLING CONTROL 1828A01 A15
SUM. AMP
AMP
FREQ.
WAVE FORM
GENERATOR
POWER SUPPLY 1816A35 A19
POSITIVE POWER SUPPLY REGULATOR ADJ.
NEGATIVE POWER SUPPLY REGULATOR
POWER READY DET.
GATE POWER DRIVER
RING COUNTER 1816A39 A11
DIVIDE SELECT
INH
FREQUENCY TO VOLTAGE CONVERTER
RING COUNTER
RING COUNTER REFERENCE
PHASE SHIFTER
VOLTAGE REGULATOR 1816A38 A13
BOOST
VOLTS/HZ TRANSDUCER
VOLTAGE CONTROLLER
BUFFER MO
AMP MPC
TEST SWITCH
SOFT START
RAMP REFERENCE
GATE PLUG BD.

FIGURE 2B

When a Cycling Control or P-Jump board is provided as an option, the FREQ signal is modulated by this board. A complete description of these boards and their functions is given in I.L. 16-800-329 and I.L. 16-800-330 respectively.

Before being converted to an actual frequency the FREQ signal is processed in a Ramp Function Generator (RFG). The acceleration and deceleration times vary depending which group of the Oscillator board is used. Table 2 gives the ramp times from zero to 10v dc out. Note that the MIN, MAX adjustment will limit the ramp range and therefore limit the ramp time.

TABLE 2

Oscillator Group	Ramp Time (Full Frequency Range)
G01	22 ±10% sec fixed
G02	44 ±10% sec fixed
G03	5.3 to 53 sec adjustable

The output of the RFG feeds into the Voltage Controlled Oscillator.

The VCO is a linear voltage to frequency converter with an output (OSC) which can vary from zero to approximately 5300 Hz.

The OSC signal feeds into a Divide Select Circuit on the Ring Counter Bd. This circuit provides the appropriate sealing from the VCO output to the Ring Counter Input depending on maximum inverter output frequency and the number of inverter stages. This enables the VCO to operate over the maximum range thus insuring the best drift and linearity characteristics. Table 3 gives the division factor from input to output of this circuit.

TABLE 3

Divide Select Position	Division Factor
1	1
2	.5
3	2
4	4

Note that Position 2 is actually a frequency doubling connection.

The OSC signal also feeds into a Frequency to Voltage Converter. This circuit is designed to provide an output signal to drive an analog frequency meter. The HG pot provides a means for gain adjustment.

The Ring Counter section provides the fixed electrical phase shift between stages required for the Harmonic Neutralization approach. The Ring Counter is a nine bit serial input shift register which can be shortened to the number of bits required for the number of inverter stages. The Ring Counter is a "twisted" type so it can accommodate a maximum of 18 stages. The programming for the number of required bits is done on the backplane wiring. The Ring Counter outputs feed into the respective Phase Shifter blocks.

There are five inputs and two outputs on each of the Phase Shifter blocks. The two outputs are the two signals which control the switching of the two poles in their respective inverter power stage. One of the output signals is a "direct" signal which is directly related in phase to the Ring Counter signal. The other output is a "shifted" signal which is shifted in phase from the "direct" signal by an amount controlled by the voltage regulator signal (VRO).

The Ramp Reference (RR) signal controls the gain of the timing (shifting) circuits.

The N13 input provides a bias which establishes a minimum shift and therefore establishes a minimum inverter output voltage.

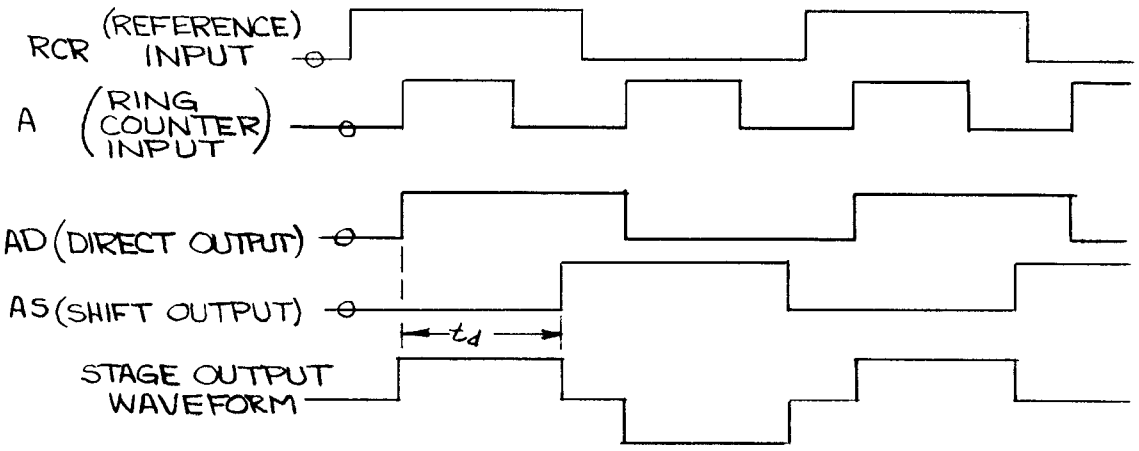
The Ring Counter Reference (RCR) provides a switching direction reference for the two output signals.

Fig. 3 shows typical waveforms for the Ring Counter and RCR input signals, and the direct and shifted output signals.

FIGURE 3

PHASE SHIFTER SIGNALS

(All control signals are referenced to PSC)



As can be seen in Figure 3 the AD signal is clocked by the leading edge of the A signal. The RCR signal sets the level to which the AD signal switches. The AS signal follows the AD signal by a time delay (t_d) which is controlled by the VRO signal. Since equivalent switching occurs in the other phase shifter blocks referenced to the RCR signal, the correct switching pattern is generated for all stages.

C. Voltage Control

In order to provide output voltage regulation a feedback voltage is necessary. This function is provided on the I-O panel with three single phase transformers (1T, 2T, 3T). The 3Ø inverter output voltage is stepped down in the delta-wye transformer arrangement and fed to the Volts/Hz transducer on the Voltage Regulator Bd.

In the Volts/Hz transducer the 3Ø signals are integrated and rectified. This produces a dc output signal which is proportional to the volt-sec area of the sinusoidal inverter output waveforms. The Volts/Hz signal is fed to the Voltage Controller.

Here the feedback signal is compared against an internal reference signal. The error signal is amplified and processed in the Buffer Amp and eventually sent to the Phase Shifter. The inverter output voltage is adjusted with the gain pot (V/Hz) in the Volts/Hz transducer. A high frequency dynamic response of the voltage controller loop. This adjustment can be used to improve the loop stability in certain cases.

Also feeding into the Voltage controller is a boost function. This circuit provides for boosting of the voltage/frequency characteristic at low frequencies to overcome the effect of motor stator resistance. Two adjustments are provided. The Boost (BST) pot sets the amplitude of the boost at minimum frequency. The Boost Crossover (BXO) sets the frequency at which the boost effect tapers to zero. The -f* signal feeding into the Boost circuit is the signal which causes a reduction of the boost as frequency increases. See Fig. 4 for a graphic representation of these functions.

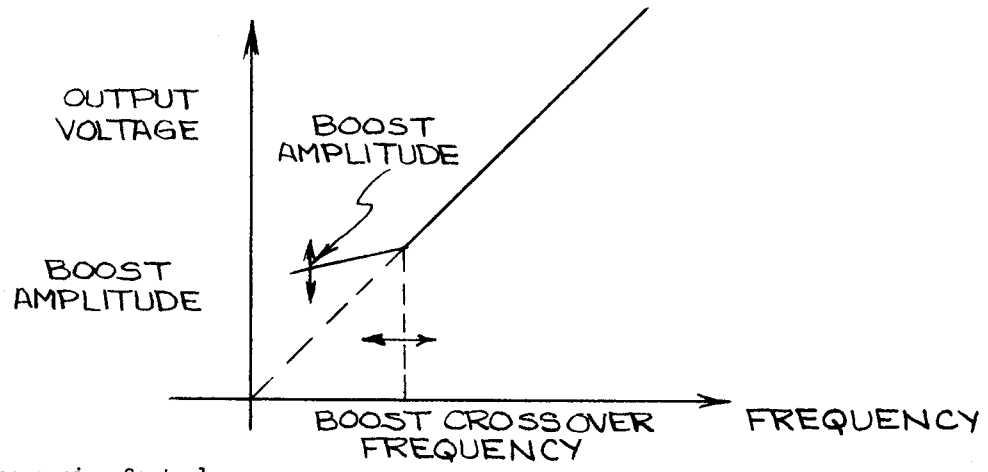
The Buffer Amplifier is a power amplifier which provides capability for driving into all the Phase Shifter Blocks. It also provides two adjustments: Manual Override (MO) and Maximum Pulse Width Clamp (MPC). The MPC adjustment is adjusted to prevent the Phase Shifter pulse width from exceeding 180 degrees. It is actually set (during startup) for somewhat less than 180 degrees to take into account circuit tolerances. The MO pot is used as a manual override of the voltage controller loop. This pot is used during startup and testing procedures only.

The Range Change RGC signal feeding into the Buffer Amp adjusts the Maximum Pulse Width Clamp level when a Range Change control is used on the inverter.

The output signal of the Buffer Amplifier (VRO) is a 0 to -8V dc signal used to control the time delay in the Phase Shifter blocks.

FIGURE 4

BOOST CHARACTERISTIC



D. Sequencing Control

Sequencing for the A1101 control is required in order to insure proper operation of the logic during power-up and power-down conditions.

During a power-up condition the first thing that happens is that the control power +24V builds up. This build up is sensed by the Power Ready Detector on the Power Supply Bd. When the +24V voltage exceeds 18V the PR relay is picked up. Contacts from this relay are used to interlock the inverter dc bus contactor (or breaker). The PR circuit also feeds the clock allow (CAL) signal through an "OR" circuit in the Gate Power Driver block.

This permits the clock signal to feed into Ring Counter, which then begins to cycle. During the first cycle of the Ring Counter the error detecting circuits (in the Ring Counter Block) set the Ring Counter to the correct state.

A short time after the PR relay picks up, the Gate Power (GP) relay is picked up by the Gate Power Driver. This relay closes in the +24V control power to the Gate Power (GP) bus which supplies gating power to the Gate Modulator Boards. Gating of the thyristors in the inverter stages then begins. No cycling of the inverter poles begin however until the RCR signal is enabled.

After the inverter dc link has charged to full potential, the RUN relay is picked up by an external contact. Once this happens a RUN signal is sent to the Test Switch. With the Test Switch in the "Norm" position the Run signal is connected to the soft start circuit, the Gate Power Driver circuit, and the ring counter reference circuit. This signal working thru the Gate Power Driver circuit locks in the GP relay and the CAL signals.

The Run signal feeding into the Ring Counter Reference enables cycling on the inverter output by enabling the RCR signal.

The Soft Start circuit acts on the reference to the Voltage controller. Prior to the application of the RUN signal the reference in the Voltage Regulator is held to zero. When the Run command is applied the voltage reference gradually builds up which causes a gradual buildup of the inverter output voltage. This action is required to limit the magnetizing inrush current of the stage transformers during the first output cycle.

The Test Switch can be used to override the normal starting procedure. When this switch is in the Soft Start (SS) position the inverter output will cycle, but the output voltage will be held at the minimum value (as set by the bias on the Phase Shifter Bd). With the

Test Switch in the OFF position, no cycling (i.e. RCR is not enabled) or voltage buildup occurs.

A shut-down sequence begins when the RUN relay drops out. This occurs when the inverter dc bus disconnect is opened.

An automatic interrupt of this dc bus disconnect is initiated either by an undervoltage sensor on the dc bus or by the power ready detector in the control logic (thru the PR relay).

Once the RUN relay drops out, the RCR signal is immediately inhibited and the Soft Start circuit calls for zero output voltage. This causes the Phase Shifter Blocks to cycle for a maximum of one output cycle before stopping. If the control power is dropping off (as sensed by the Power Ready Detector) then the CAL signal inhibits any clocking of the Ring Counter. This allows the Phase Shifter blocks to time out any pulses which have been initiated. Therefore, the stopping time is one-half cycle of maximum operating frequency (this is the maximum pulse width which can be allowed). The Gate Power Driver contains a time delay which permits the Phase Shifter's to time out. After this time delay the GP relay is dropped out. This disconnects gating power to the Gate Modulator Bds thus preventing any false gating of thyristors as the control power and/or dc bus voltage drops off.

E. Gating Control

The gating control for the inverter is performed on the Gate Modulator Bds. This board is located in the power module drawer, where it serves the purpose of converting incoming gate control signals from the Phase Shifter Bd, into properly shaped and isolated gate drive signals for the thyristors in one complete inverter stage. Two such boards, each of plug in construction, are located inthe power module drawer; one for the control of each stage.

The functional schematic diagram for the connection between the logic drawer gate plug and the thyristors in the power drawer is shown on Figure 6.

The AD signal controls the gating to SCR11 and SCR12. When AD is "high" SCR 11 is being gated. When AD is "Low" SCR12 is being gated. The gate signal applied to the Thyristors is a "picket fence" type with a carrier frequency of about 23 KHZ. The initial pulse on each half cycle is about 50 sec. wide. See Figure 5.

Note that some of the control wiring in the power drawers is not used with the A1101 control.

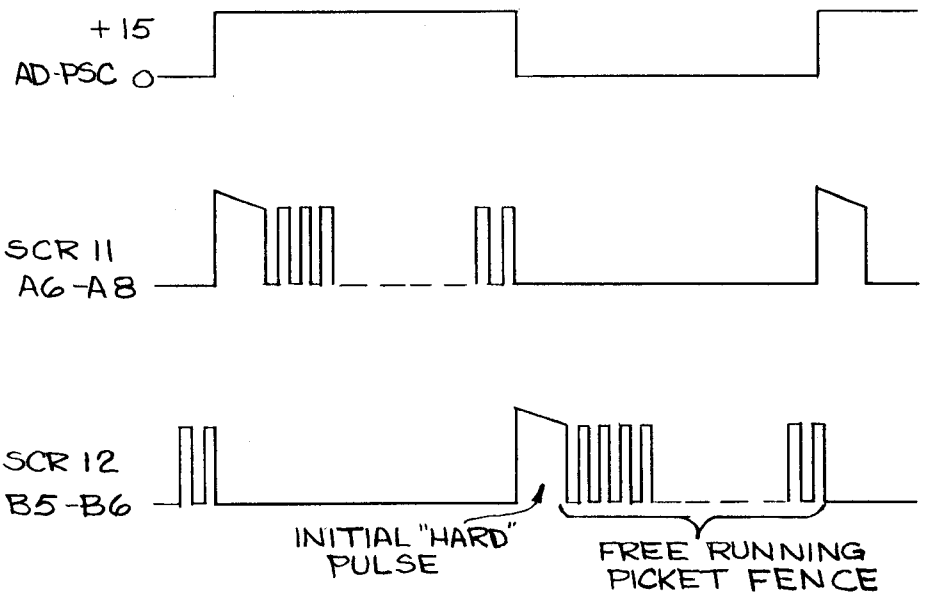


FIGURE 5

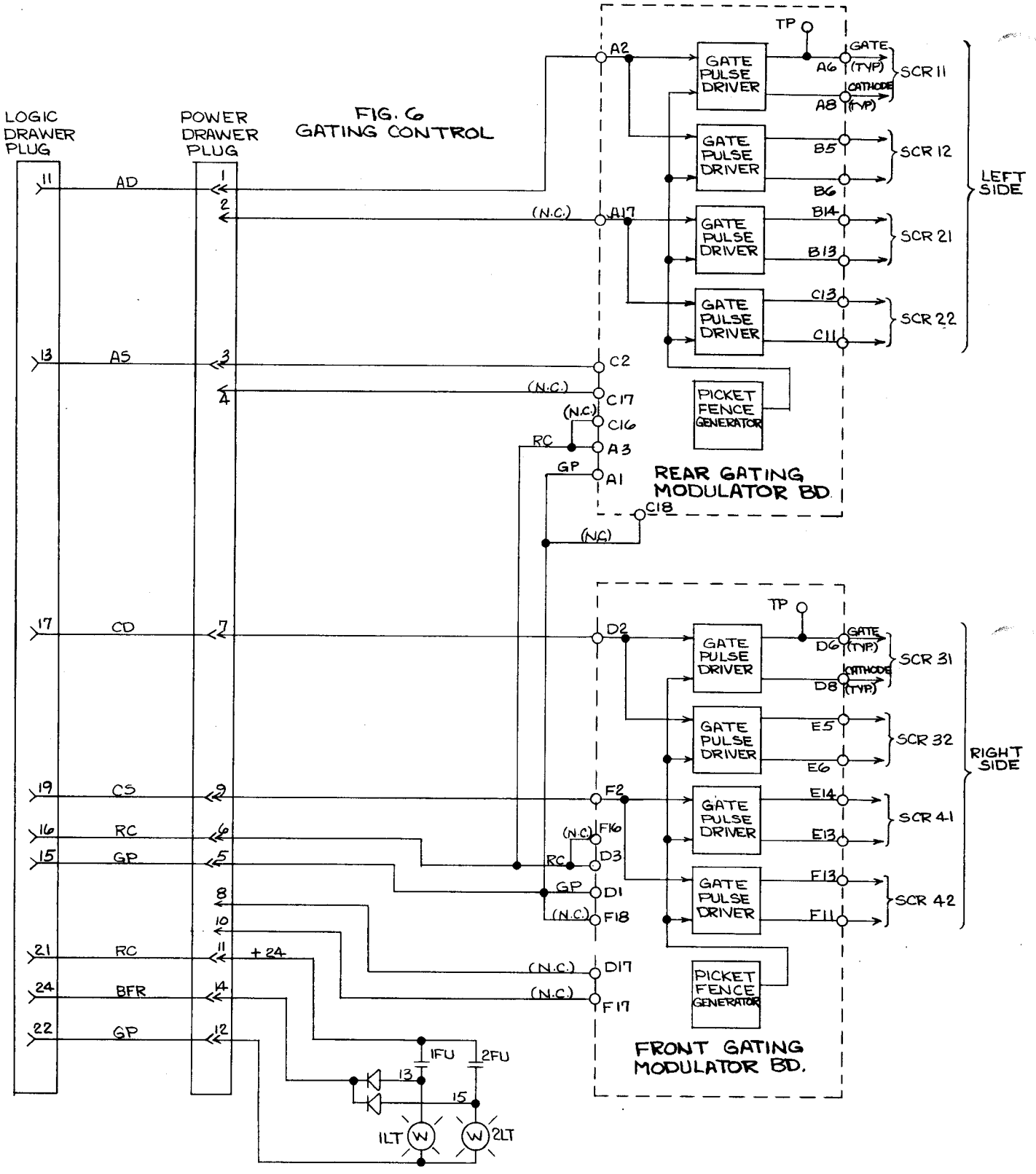


FIG. 6
GATING CONTROL

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TRANSFORMER SECTION

FUNCTION

As described in Basic Theory, the output of each power stage is fed into the primary of a stage output transformer. The secondaries of the several stage output transformers are connected in a harmonic neutralization interconnection to attain a stepped wave output (refer to Figure 1).

TRANSFORMER INTERCONNECTION

The inverter is fully tested at the factory before shipment to insure proper stage output transformer interconnection, therefore, there is normally no need to be concerned about this aspect when the inverter reaches the installation site. Infrequently, however, if an inverter is rather large and/or if access to the installation site is very limited, it is necessary to break the inverter down into smaller shipping sections after it has been factory tested. This introduces the risk of reconnecting the stage output transformers in an improper sequence. This section will be helpful in determining if the transformers are connected properly, and if not, where trouble lies.

Right after the transformer interconnection in Figure 1, is an artist's conception of what the half-cycle waveform would look like on an oscilloscope if the oscilloscope were connected from one of the phases (T1, T2, or T3) to "neutral" (n) with the manual override potentiometer (see Logic Drawer section) turned fully counter-clockwise to obtain narrow pulse-width. Please note that the point designated N in Figures 1 to 6 is not actually neutral of a 4-wire wye connected system because it is not equidistant (in potential) from the three phases.

Use Figures 1 through 6 (depending on the number of stages in the inverter) to determine if the inverter output transformers are connected properly or to determine, at a glance, which transformers are incorrectly connected. First observe the minimum pulse-width waveform phase-to-phase to see if all steps are of the proper size. If one or more steps do not fit the pattern, then it will be necessary to observe the phase to "neutral" waveforms to determine which transformers are incorrectly connected.

After you have determined which stages seem to be out of order, check to be sure that the cause is not actually due to improper firing sequence of the stage due to the logic plugs in the cage assembly of the logic drawer or in the power drawers being plugged in to the wrong receptacles. Before re-wiring any transformer connections, be sure to check with the Inverter Systems system engineer (Product Line Administrator) to assure that such a step is essential.

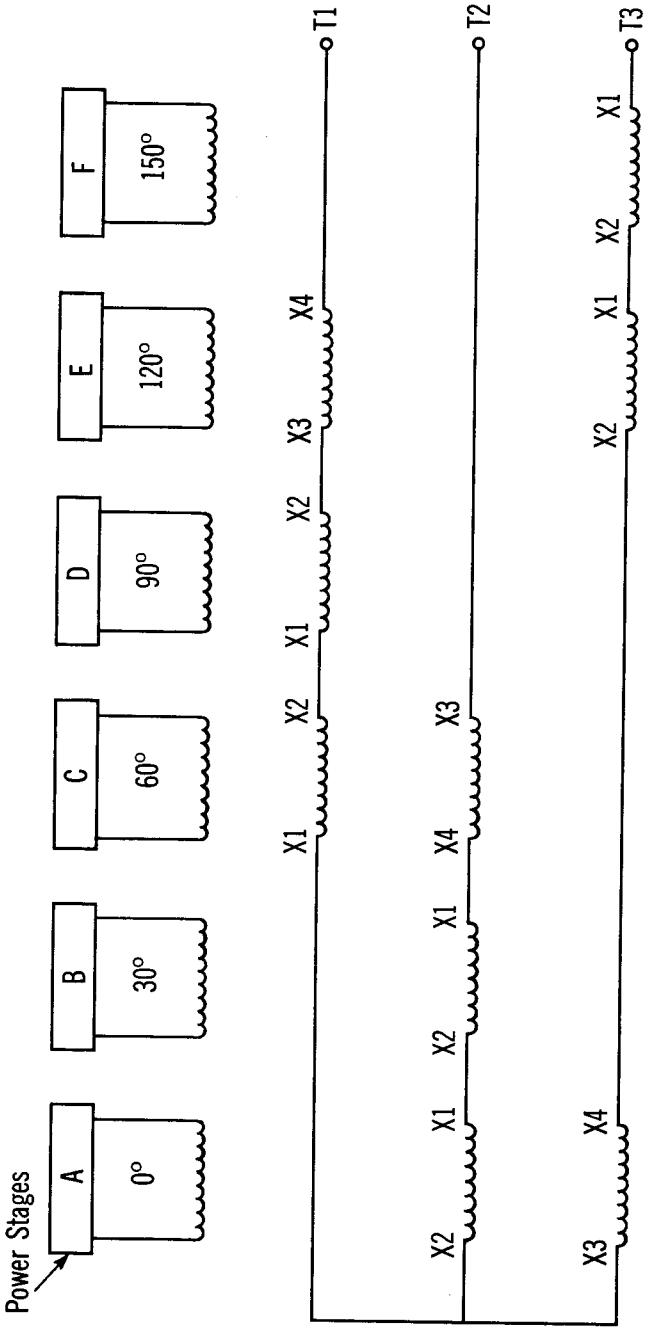
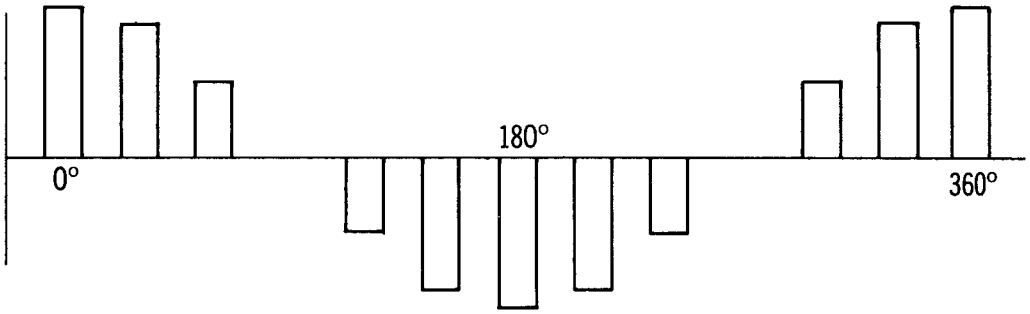
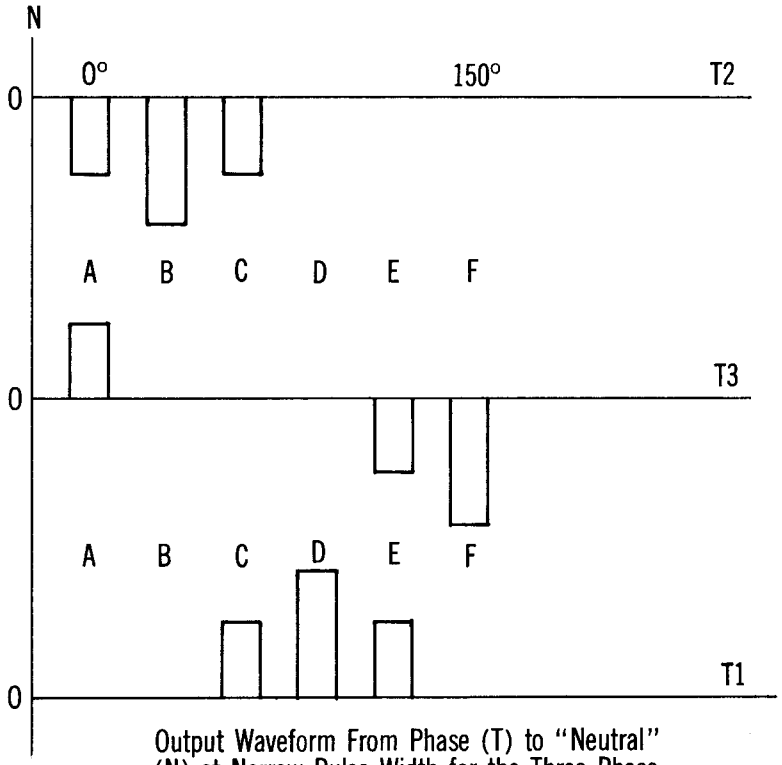


FIGURE 1A - STAGE OUTPUT TRANSFORMER INTERCONNECTION



Output Waveform Phase to Phase (T3-T2)
at Narrow Pulse Width



Output Waveform From Phase (T) to "Neutral"
(N) at Narrow Pulse Width for the Three Phase

FIGURE 1B - SIX-STAGE INVERTER OUTPUT WAVEFORMS

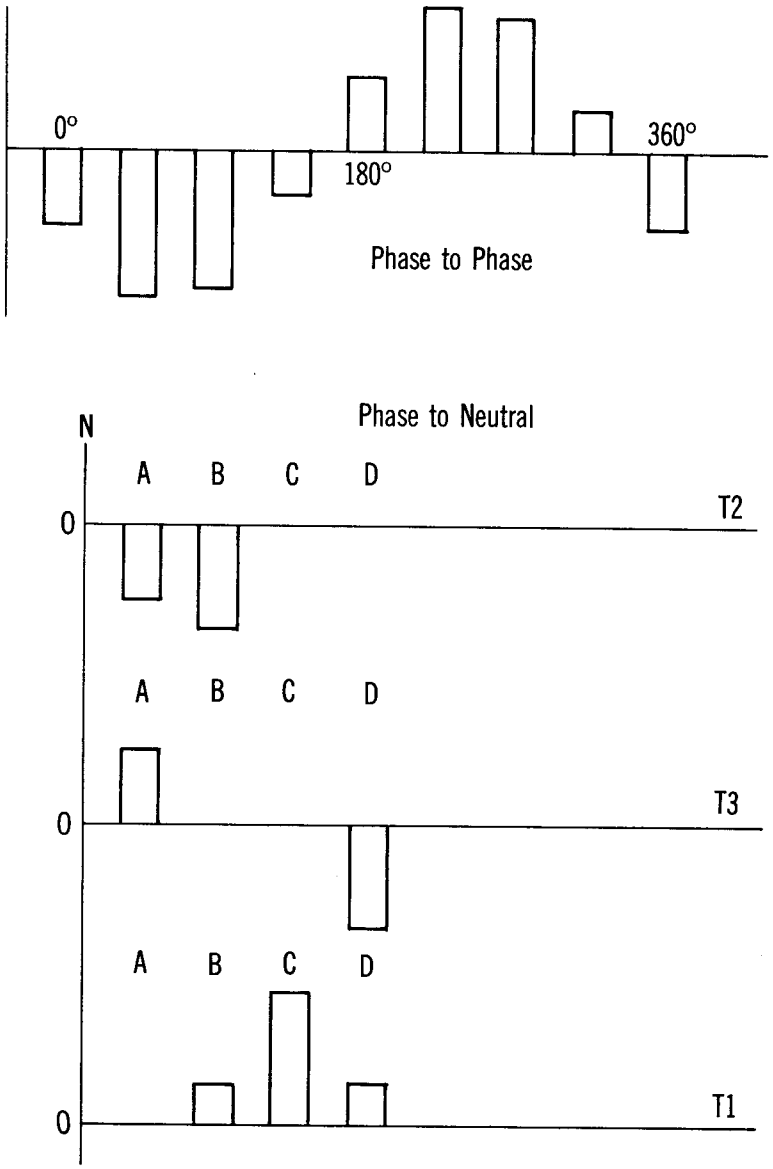
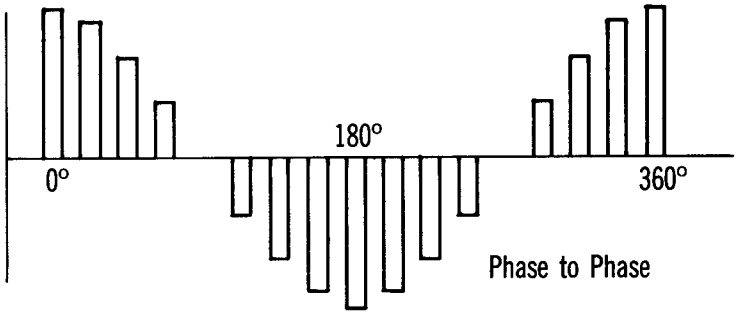


FIGURE 2 - FOUR STAGE INVERTER OUTPUT WAVEFORMS



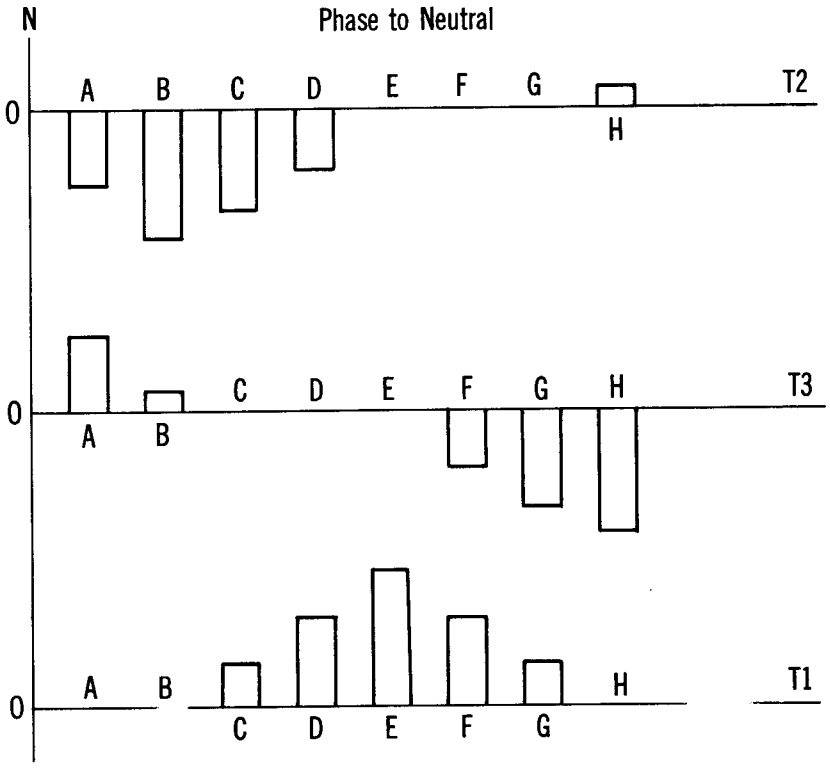


FIGURE 3 - EIGHT STAGE INVERTER OUTPUT WAVEFORMS

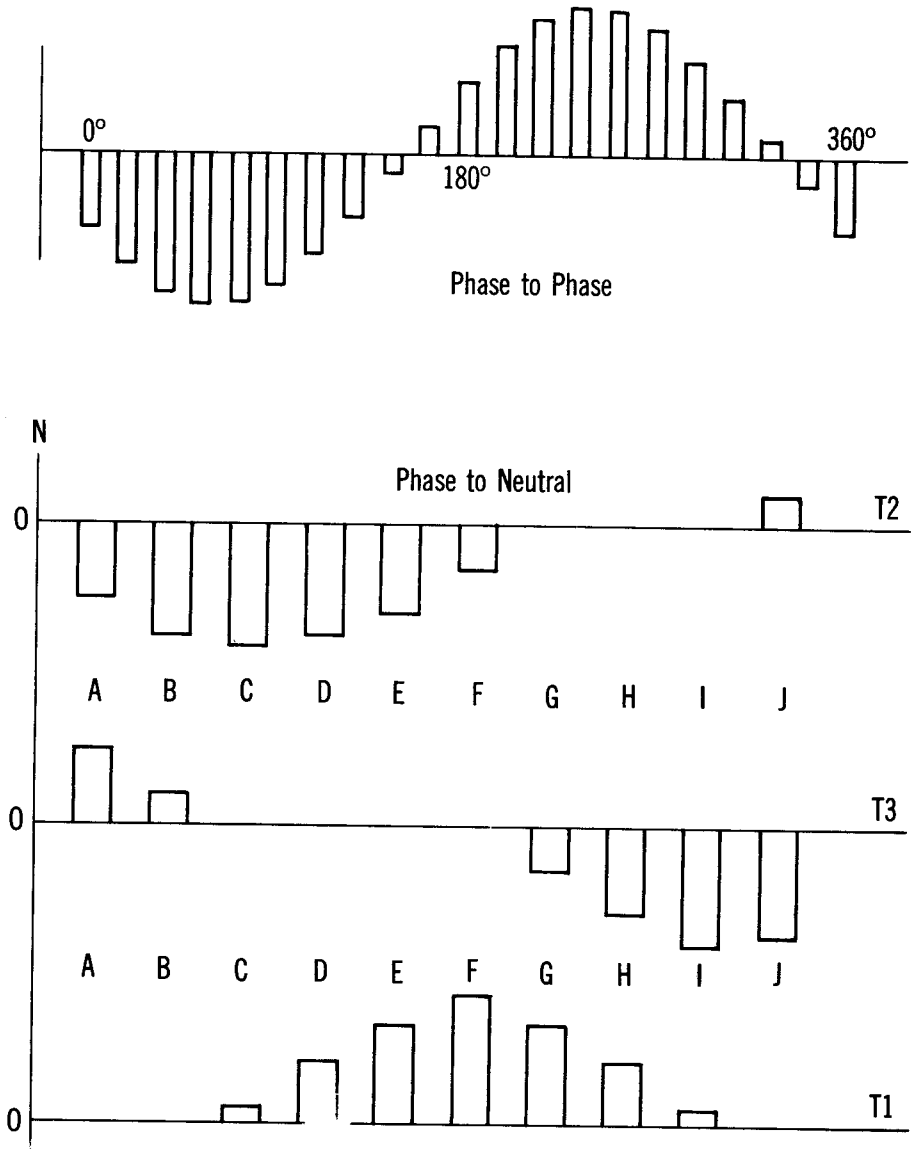


FIGURE 4 TEN STAGE INVERTER OUTPUT WAVEFORMS

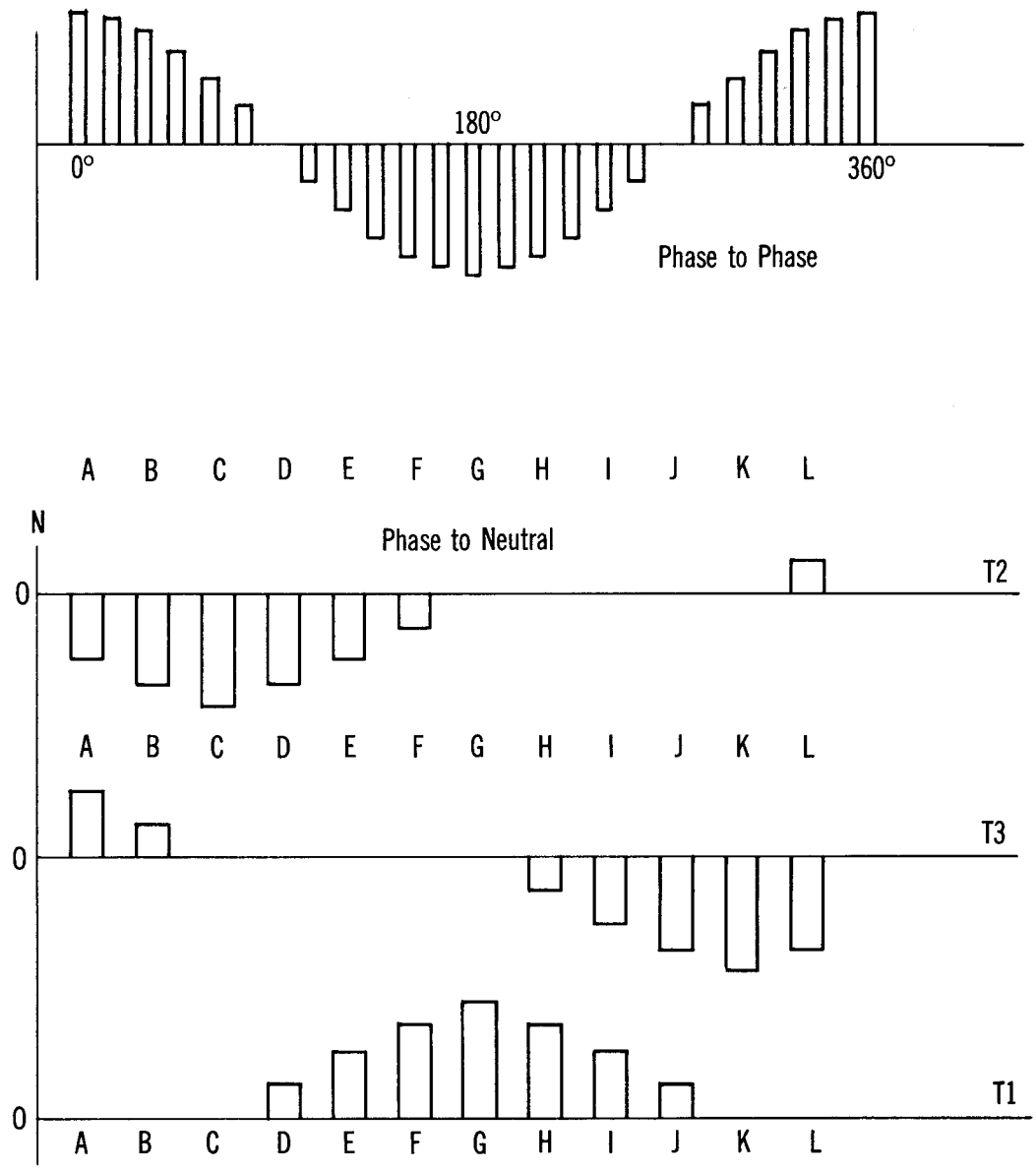
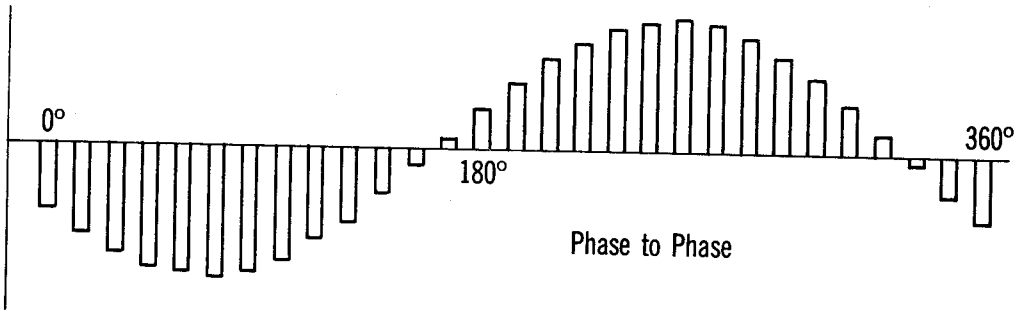


FIGURE 5 - TWELVE STAGE INVERTER OUTPUT WAVEFORMS



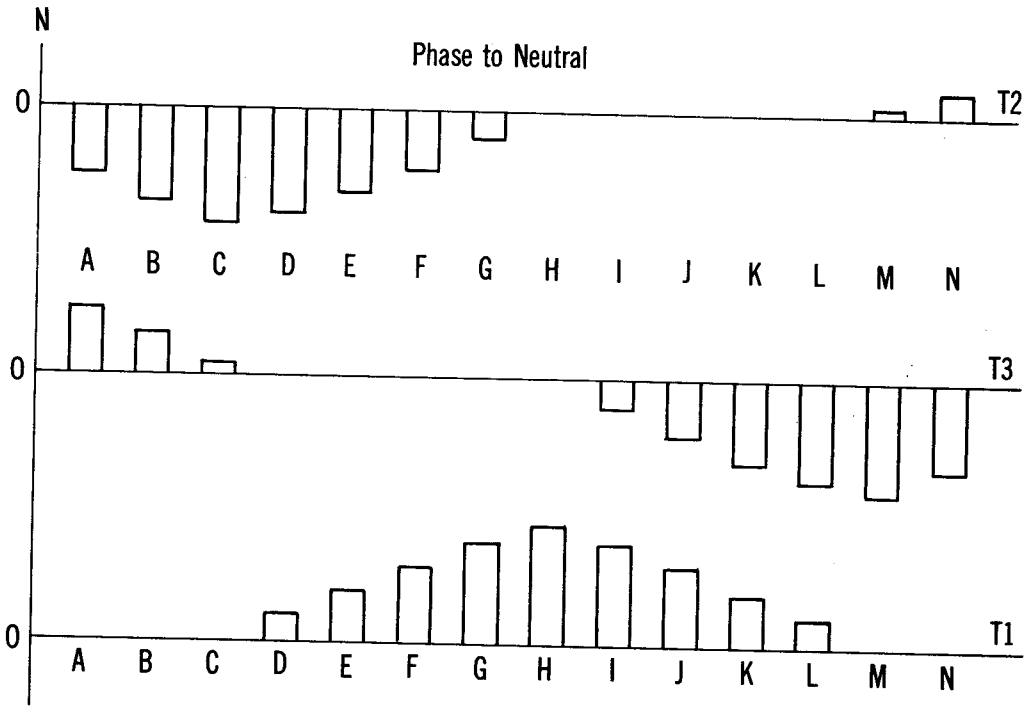


FIGURE 6 - FOURTEEN STAGE INVERTER OUTPUT WAVEFORMS