Instruction Book

I.L. 19-605

AccurCon II Static
Fixed Frequency Inverters

Inverter Paralleling

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Inverter Systems
Industrial Systems Division
Buffalo, N.Y.

INVERTER PARALLELING

GENERAL

This instruction book describes the circuitry and concepts involved with the paralleling of two or more inverters. This book is not intended to be used by itself; it is supplemental to the instruction material on the specific inverters involved.

Operation

When A.C. power systems are paralleled, the three basic parameters, Voltage, Frequency and Phase relationship have to be closely matched. With rotary generators, the problem is complicated by the inertia of the generator, throttle response and mechanical linkages. These introduce lengthy time constants into the control loops which, consequently, also react quite slowly. In an inverter, the time constants are measured in cycles instead of seconds and inertia in the system can be regarded as non-existent. The throttle is replaced by a voltage controlled oscillator which responds sub-cyclically; an inverter can thus be synchronized and held within $\pm 2°$ phase deviation without undue distress or complications arising. Voltage output from an inverter can similarily be held in tight control with response times in the region 2 or 3 cycles.

For extension of power rating or the addition of redundant capability, the theoretrical similarity can be extended further for parallel operation. The practical circumstances for the two systems are not, however, similar and the paralleling of Accurcon inverters can be, as a result, a much simpler process than paralleling rotary generators.

The following comments should clarify this point. With reference to 3424D34, it can be seen that the inverter packages are all synchronized to a Master Oscillator, and that there can be any number of such similar packages. Going back now to our generator simile, this means that we have a number of similar generators mounted on one Drive Shaft. By this means, frequency deviations between generators are prevented and a multitude of control problems removed. However, the inverters have one more advantage in their favor; due to the method of synchronization, the relative phase position can be adjusted precisely (within 1°) when the "generator" is under load and is then held automatically by the synchronizing circuits. In practice, when the inverter packages have been lined up at the logic signal level and then connected in parallel, a KW balance of better than $\pm 5\%$ has been obtained. Minor adjustment of phase at a particular load can improve this further but is not necessary. This balance holds over the full system load range and once set, requires no further adjustment. If an optimum setting is required, it should be carried out at Full Load and after the equipment has been running for say an hour to enable thermal conditions to stabilize. The use of fast synchronizing circuits and a common Master Oscillator have thus removed any "Time" variations between the inverters.

Voltage output is a function of the conduction angle of the stages and this is controlled by a d.c. signal from the voltage regulator. The "Error Restrictor" circuit (referred to on 3424D34 as auctioneering diode scheme 488B948) acts as a clamp between the output circuits of the voltage regulators and assures that the conduction angles and hence output voltages of the individual packages are within very close limits.

In a three package system, for example, with an output of 1000 amperes, a circulating current of only 50 amperes was obtained; this was measured at 150% load on a nominal 700 Amps output equipment.

Error Restrictor Circuit

This is a ring of diodes whcih connect the output (L8) of the Voltage Regulator Board in each Inverter Package to the logic control voltages (L6) of the Voltage Regulator Boards of all the other inverter packages. A specimen arrangement for three inverter packages is shown in Fig. 2. Relay PR is normally part of the inverter package and is arranged to close contacts for the same time that the Paralleling Breaker or Contactor is closed. For convenience, it can be operated by the same switch or push button that operates the paralleling switchgear. It should also be dropped out at the same time. When relay PR contacts are open, the corresponding inverter package is independent of the other regulators and can be treated individually for servicing and test purpose. Operation of the manual control potentiometer in its logic circuits then has no effect upon the other inverters.

Master Frequency Source

The master frequency source consists of three pulse generators arranged so that a failure in any one of them will not cause a failure to the signal used for synchronizing the inverters. A simplified block diagram is shown in Fig. 1. The actual complete diagram is shown on 3424D33 and 663C807, but this is more complex than is required for a basic description.

The simplified block diagram of figure 1 shows three functional sections of the circuit. a) Pulse Generator, b) Gate, c) Bi-Stable Flip-Flop.

a) Pulse Generator:

The basic frequency sources are pulse generators which run at a repetition rate equivalent (for this example) to twice the output frequency of the inverter. The three pulse generators are timed for approximately the same period ($\pm$1%).

b) Gate Circuit:

The gate circuit is arranged so that two pulses have to be coincident to allow a pulse through the gate to the Bi-stable Flip-Flop. If any one of the three pulse generators is not working, the other two still

provide an output pulse. The first pulse which occurs is fed back thru the diodes shown as an input to the pulse generators to reset their timing period. Output from Gate 1 is a combination of pulse generators 1& 2, Gate 2 is 2&3, and Gate 3 is 3&1.

c) Bi-Stable Flip-Flop:

A pulse from the gate circuit switches this circuit and provides a square wave type of output which can be distributed around the inverters for synchronizing purposes.

The output transformer is supplied from a high impedance circuit.

If the Bi-stable ceases to operate, transformer saturation causes loss of the signal voltage from this circuit and no effect is seen on the master signal.

The three Bi-stables are synchronized together and feed out is in parallel.

Operating Sequence

Except when the inverter is being serviced, it is recommended that the Master synchronizing signal be connected to the logic at all times. The service switch is only used for service purposes and plays no part in the normal operating sequences.

The inverter should start up in the normal manner and automatically synchronize and lock in at the correct phase relationship. For supervisory purposes, a lamp should be connected across the inverter output breaker. In the event of malfunction of the synchronizing circuit, the lamp will light. Under correct operation, the lamp does not have sufficient voltage to indicate.

To go into parallel operation, all that is required is for the output (or paralleling) breaker to be closed. When this last power link is closed, the PR relay operates and interconnects the regulators.

It is assumed that the inverter output voltage at no load is equal (within +0.5%) to the No-Load bus voltage. Except where this has been deliberately changed, there is no reason for readjustment under normal operating circumstances, due to the precision and low drift that are inherent in the regulator design.

Suppression

All relay and breaker contacts should be adequately suppressed to quench noise transients from interfering with the control circuits. Every attempt has been made to minimize the effect of such transients but where high voltages and currents are involved, it is not possible to completely eliminate all their effects.

Control wires between inverters and control cubicles should be adequately screened from source to final destination.

Load Transfer to a Bypass Line

Refer to the discussion on make-before-break transfer, and paralleling control panel in the Section of this Instruction Book devoted to Typical Inverter Assembly. The procedures and circuit description is the same.

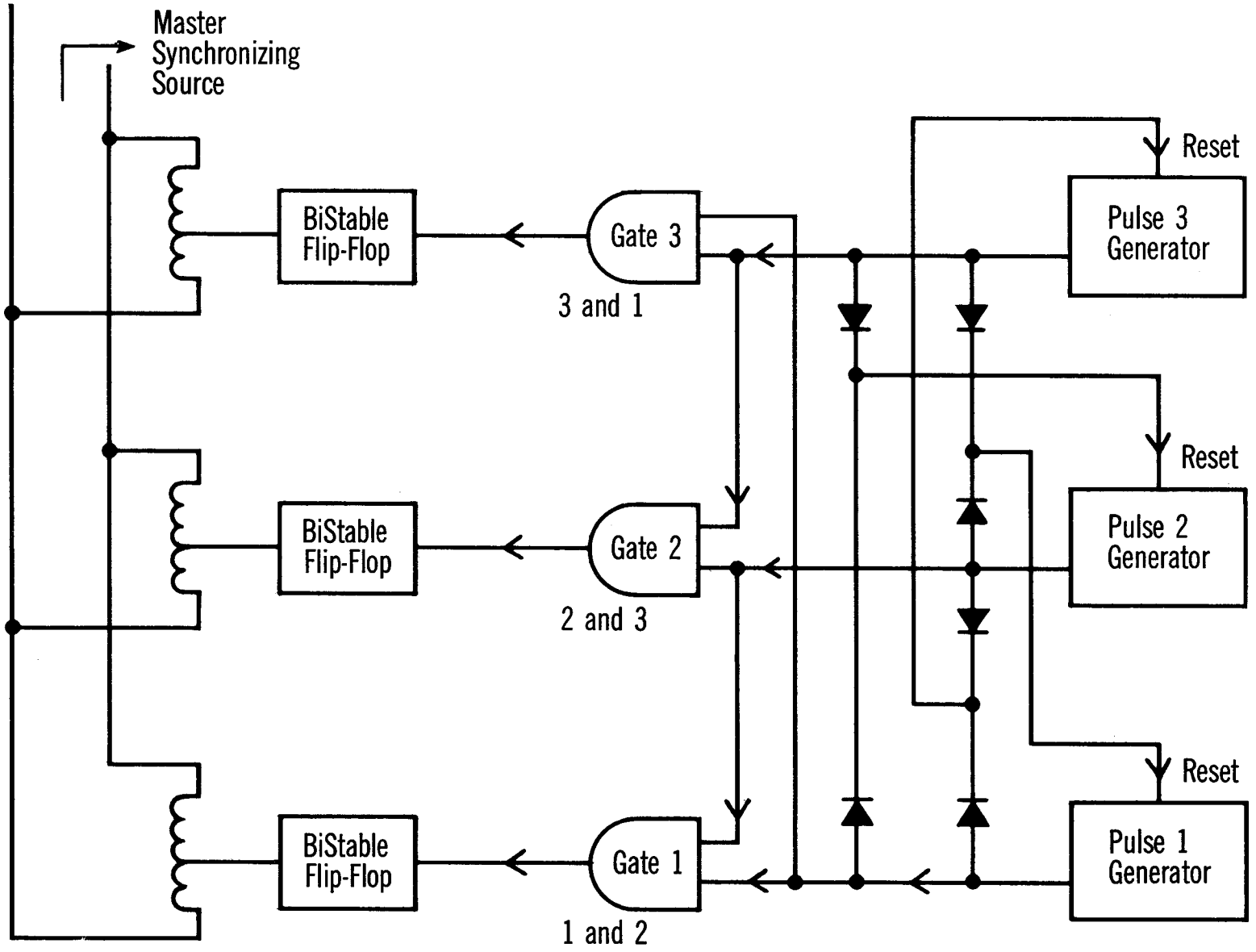


FIGURE 1 - MASTER PULSE GENERATOR SIMPLIFIED BLOCK SCHEME

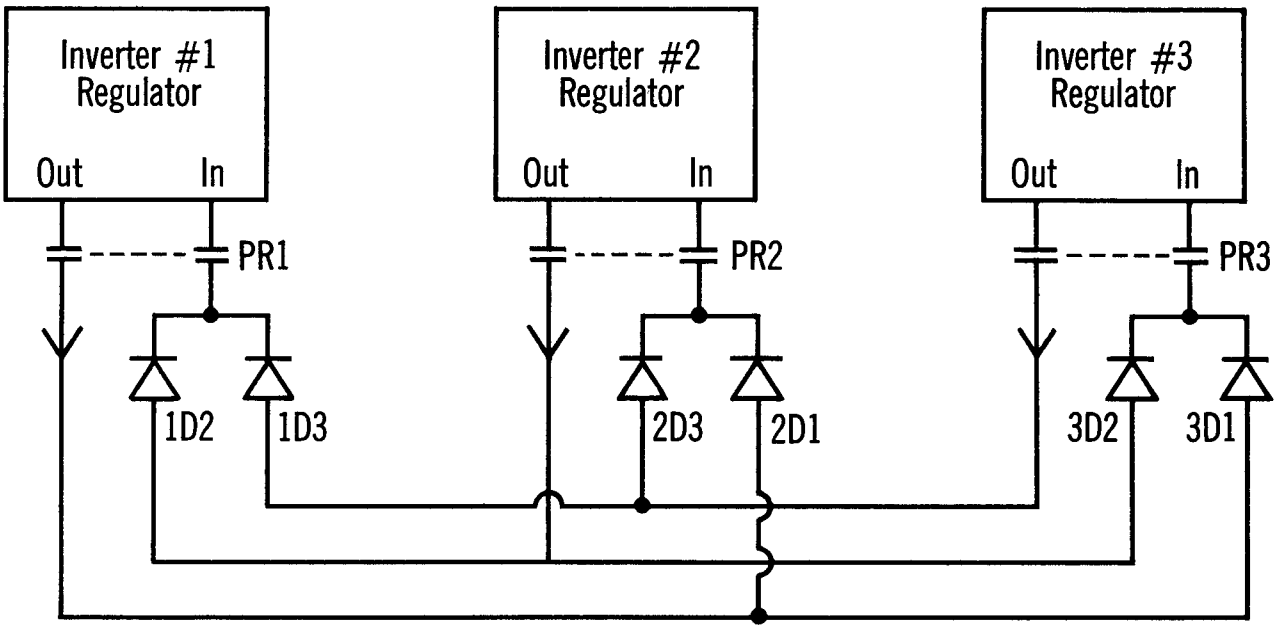
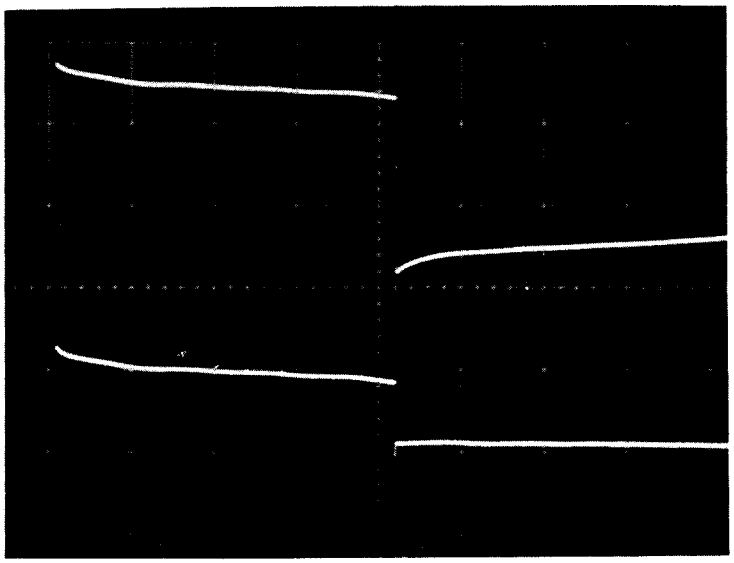
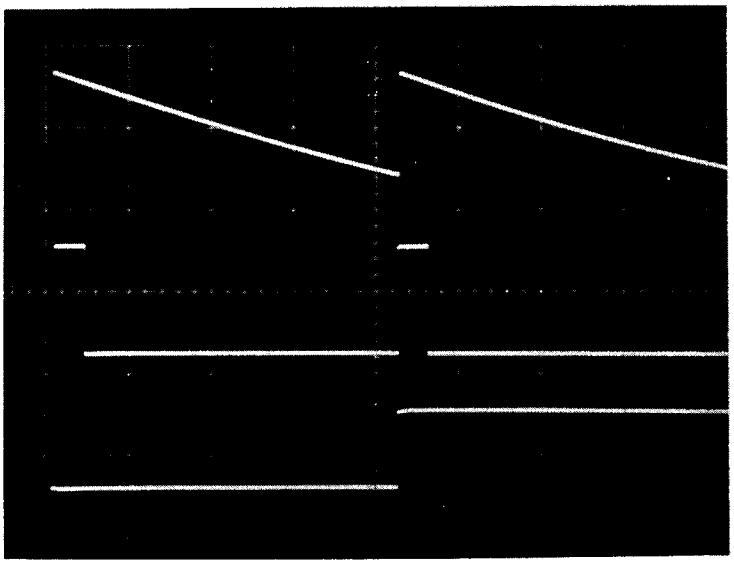


FIGURE 2 - VOLTAGE ERROR RESTRICTOR SCHEME

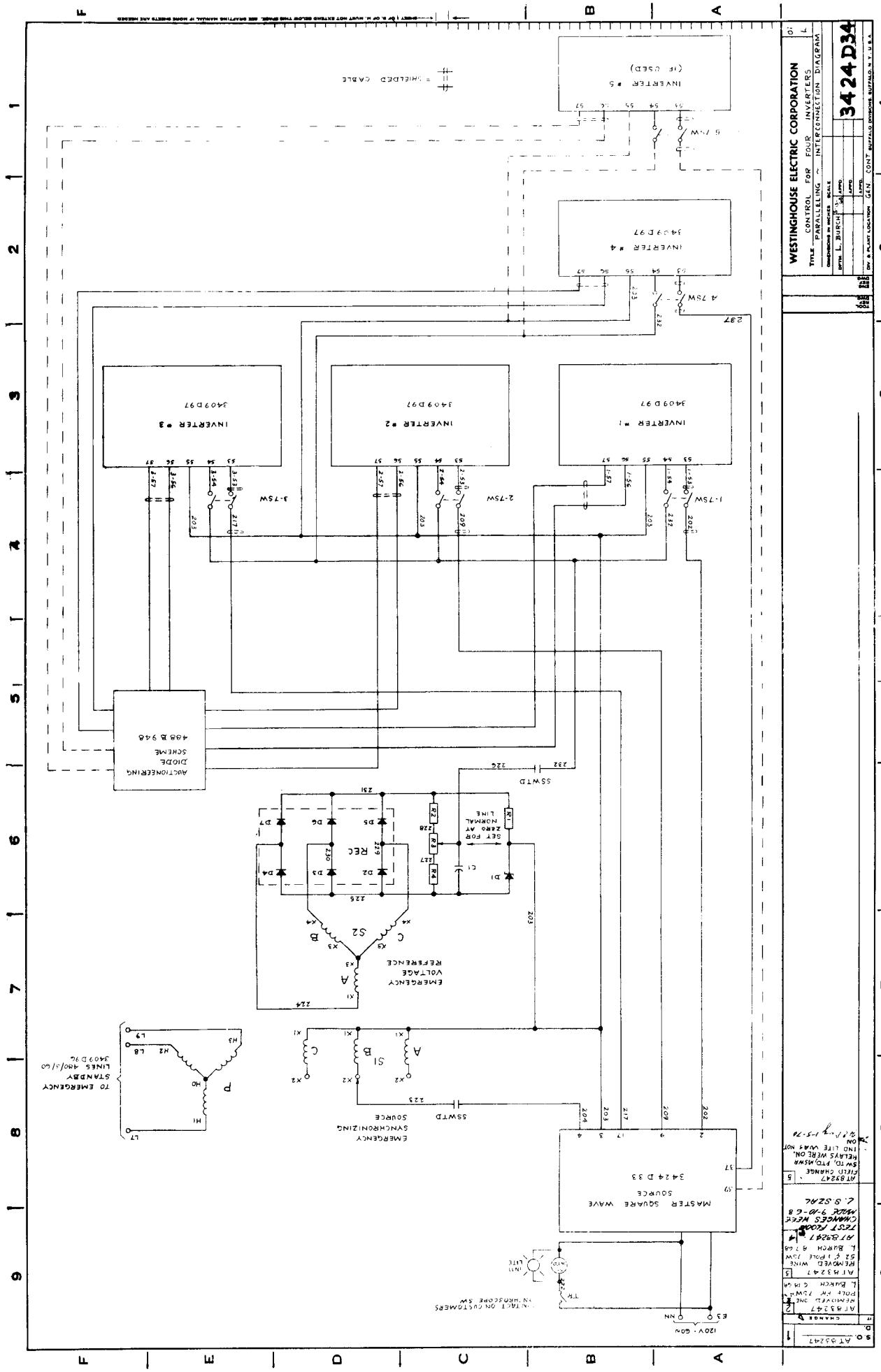


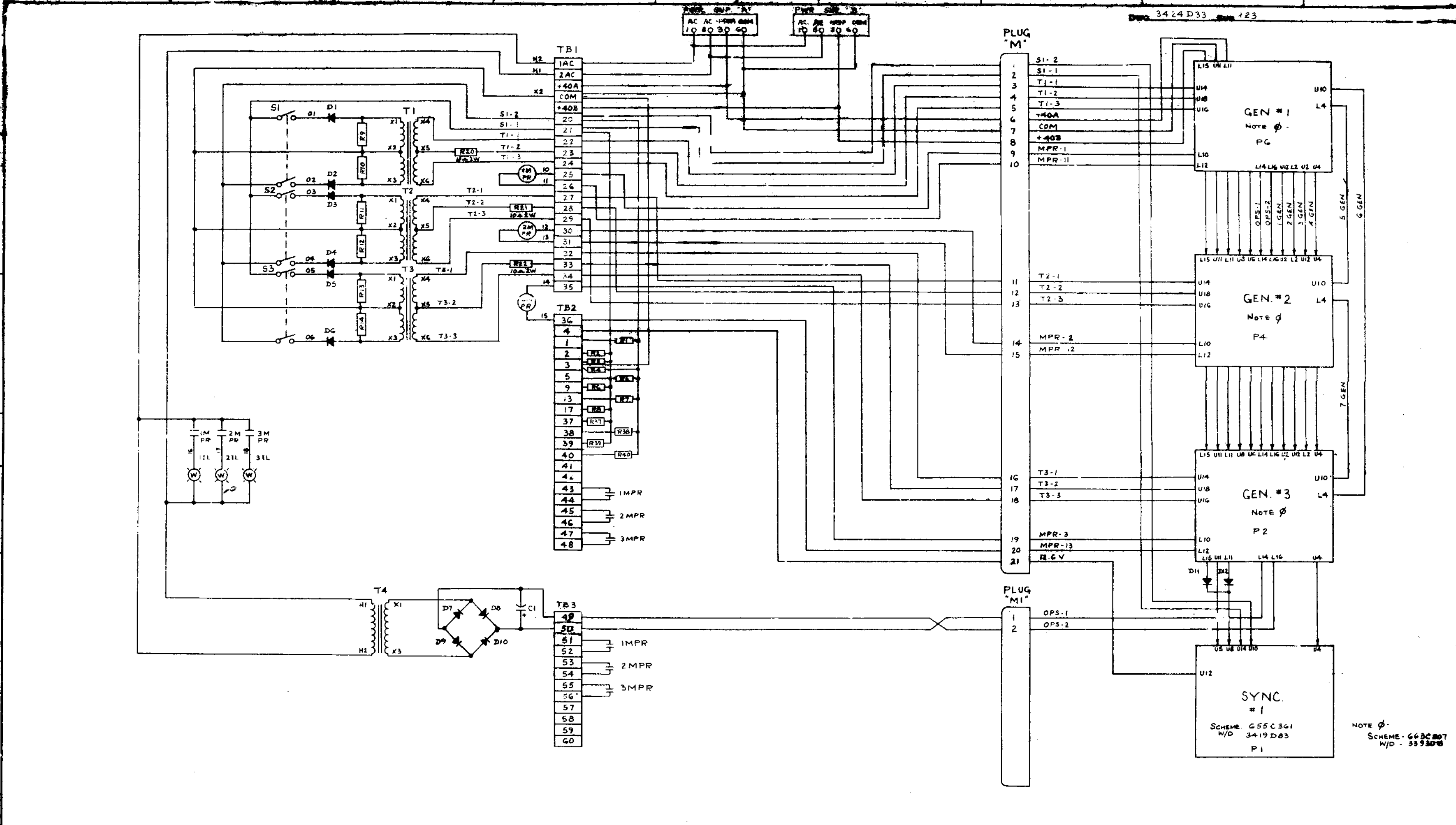
Upper Trace: Primary of T1, T2, or T3
Lower Trace: Output to inverter logics



Upper Trace: Testpoint #1
Center Trace: Testpoint #2
Lower Trace: Testpoint #3

TYPICAL WAVEFORMS OF MASTER
PULSE GENERATOR BOARD


WESTINGHOUSE ELECTRIC CORPORATION
CONTROL FOR FOUR INVERTERS
TITLE - PARALLELING ~ INTERCONNECTION DIAGRAM
3424D34
INVERTER #1
INVERTER #2
INVERTER #3
INVERTER #4
INVERTER #5
MASTER SQUARE WAVE SOURCE
3424D33
1-7SW
2-7SW
3-7SW
4-7SW
5-7SW
SSWTD
EMERGENCY SYNCHRONIZING SOURCE
EMERGENCY VOLTAGE REFERENCE
AUCTIONEERING DIODE SCHEME
TO EMERGENCY STANDBY LINES 480/3/60
120V - 60N
REC
SET FOR ZERO AT NORMAL LINE
CONTACT ON CUSTOMERS OSCILLOSCOPE SW



1	AT 83247-1
2	AT 83247 INTERCHANGED S1 & S3 L. BURCH 8-7-68
3	AT 83247-1 CHG'D WIRING TO SYNC BRD. ON U8 & U6 L. BURCH 4-10-69

WESTINGHOUSE ELECTRIC CORPORATION

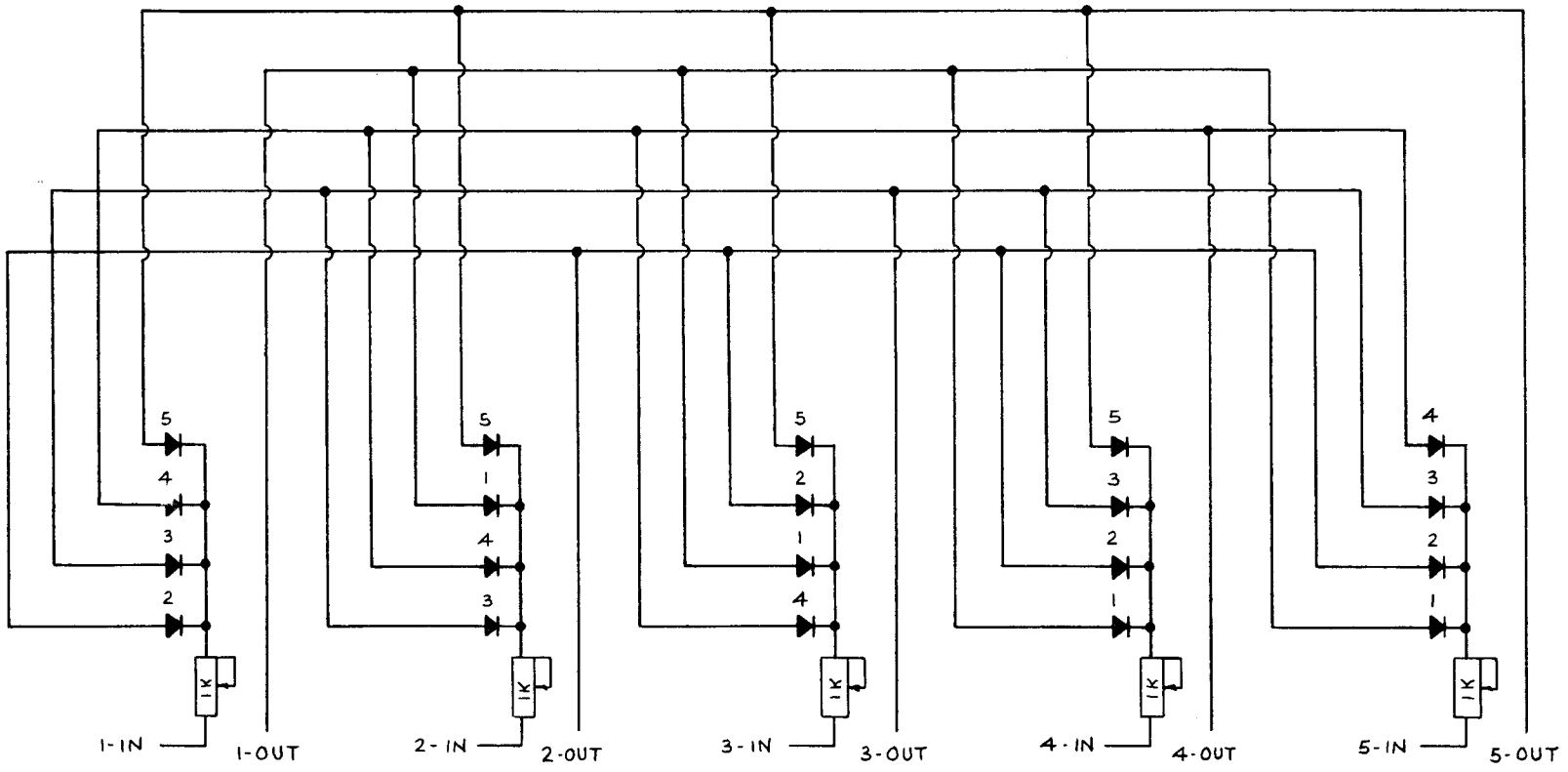
TITLE: MASTER SQUARE WAVE SOURCE BLOCK DIAGRAM

DRTN. L. BURCH

DIV. & PLANT LOCATION: GEN. CONTROL

3424D33

SUB 1



S.O. AT 83247 | 1

D.

IT.

CHANGE

TOOL REF. DWG.

ENG. REF. DWG.

WESTINGHOUSE ELECTRIC CORPORATION

02 L

TITLE VOLTAGE REGULATOR INTERCONNECTION AUCTIONEERING DIODE SCHEME

DIMENSIONS IN INCHES — SCALE

DFTM. L. BURCH 5-13-68 APPD.

APPD.

APPD.

488D948

DIV. & PLANT LOCATION GEN. CONTROL BUFFALO DIVISIONS, BUFFALO, N.Y., U.S.A.

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