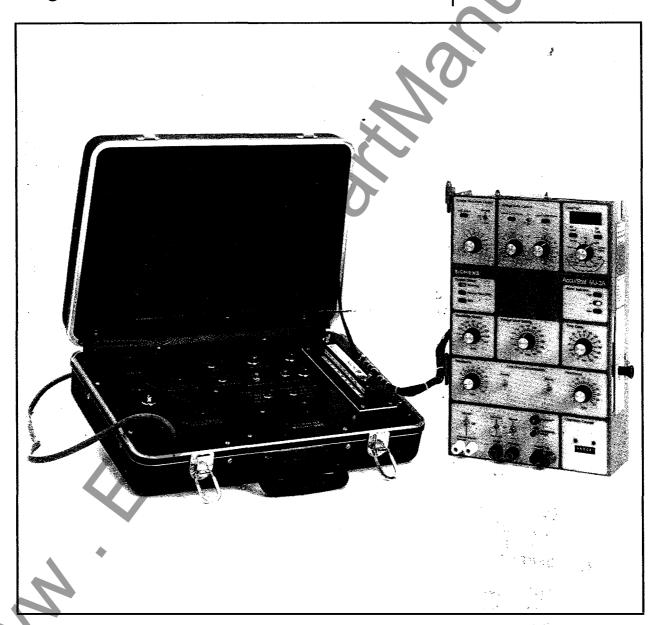
# **SIEMENS**

# **Service Manual**

ACCU/STAT™ MJ-3A Regulator Control

# Instructions

Operational Theory
Trouble Shooting
Acessories



Siemens Energy & Automation, Inc.

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Introduction

# Purpose of Manual

The intent of this manual is to enable troubleshooting and repair of the MJ-3A regulator control in the most effective manner possible. Supplemental sections provide detailed information regarding circuit operation to provide detailed information at every level. The systematic strategy used in this manual provides procedures for analyzing trouble symptoms, localizing faulty circuits, and isolating defective components. This fault- finding strategy starts with what you know - a symptom, and it takes you through a step-by-step procedure of what to do and how to do it . Using this approach, the fault can be determined methodically to enable most efficient troubleshooting.

To get the most out of this manual, you should know how to read electronic circuit diagrams and be familiar with the fundamentals of electricity, such as Ohm's law, and some of the fundamental components of electronics, such as semiconductors. You do not need mathematics, network theory, or any other skills involved in original equipment design. You should be able to read manufacturer's instructions and use standard electronic test equipment, such as the oscilloscope and the VOM. One of the early steps used in the troubleshooting procedure is to monitor operation of the circuit with various pieces of test equipment. Some recommendations and techniques are provided to help assist in troubleshooting the MJ-3A, but the operator needs to have at least a basic understanding of the equipment he will use.

This manual supplements the Accu/Stat Instruction manual (P/N 21-115527-004) by providing MJ-3A calibration and information on configuring MJ-3A controls. When an MJ-3A is repaired, it may be necessary to re-calibrate and/or re-configure the control to the same level as when it was first installed.

To achieve maximum efficiency in troubleshooting and repair of the MJ-3A control, it is extremely important to understand the operation of the circuitry. For this reason, an entire section of this manual is devoted to explaining operational theory at the circuit board level to provide an in-depth understanding of the MJ-3A control. Although the troubleshooting section provides a step by step approach where an in-depth understanding is not mandatory, maximum effectiveness at fault-finding is attained by a better understanding the details of the system.

Using this manual, you will be able to troubleshoot the MJ-3A control with much greater efficiency and a much better chance of success. Whether you are interested in intricate details of the operation, with the time to test and replace components at the board level, or one who simply wants to get the system fixed as soon as possible and desires to find faults only at the module level... this manual should help you do the job well and quickly.

# Organization of Manual

This manual is divided into four major sections followed by a series of appendices. Each section and appendix can be easily located by the large number on the outside page column referencing it. It is highly recommended that you be aware of these sections contents so the appropriate information can be found quickly when needed. The most accessed references are located in the appendices.

**Section 1** provides information on safety precautions specific to the MJ-3A, recommendations for test equipment, and a summary of troubleshooting techniques. It is highly recommended that this section is read before any troubleshooting is attempted regardless of your level of experience, because of the variety of voltage levels present on the MJ-3A control of which you must be aware.

**Section 2** provides key switch setting configurations, as well as calibration procedures. This section is used when troubleshooting to verify that the system is properly configured as well as providing information on re-calibrating after repairs have been made.

**Section 3** is a systematic and logical approach for locating specific faults in the MJ-3A control by observing the symptoms. This section ensures that before any troubleshooting is begun, a strategy is used which will enable you to pinpoint the faults most efficiently. Oscilloscope wave forms are provided to verify proper performance at key nodal points. This section is designed to provide the most efficient techniques to trap faults quickly, regardless of your level of understanding of MJ-3A circuit operation.

**Section 4** describes the entire circuit operation for maximum troubleshooting effectiveness. Each cir-

cuit is individually described in detail. Reading this section will provide a greater understanding of the data observed in section 3 and provide the trouble-shooter with a greater insight of MJ-3A operation.

Appendix Sections This section contains the most used references needed in all other sections in one convenient place. Appendix A through Appendix D are coded in such a manner that each level of the appendix corresponds with the same level as another appendix. For example, if you were interested in the transformer board, the transformer board circuit layout is in Appendix A section "A2", the block diagram is in Appendix B section "B2", the schematic in Appendix C section "C2" and the parts list in Appendix D section "D2".

**Appendix A:** Circuit Board Layouts - The MJ-3A is shown pictorially with all the available options referenced. The succeeding layouts depict each printed circuit board individually with X & Y coordinates labeled for component referencing.

**Appendix B:** Block Diagrams - This provides a top level modular look at the MJ-3A main and secondary subsystems. Referring to the block diagrams will provide a better understanding of the schematics, which follow in the next section.

**Appendix C:** Schematics - Provides detail at the component level of each of the modules shown in the block diagrams above.

Appendix D: Components part list for each module in the MJ-3A. For convenience, each component listed is identified by where it can be found on the actual circuit board layout (Appendix A).

- » QUICK & DIRECT TROUBLESHOOTING PROCEDURE
  - ".... If you ARE aware of the fault symptom, go to Appendix G (find the fault symptom listed that, you appear to be having) ... you will be guided where to proceed for fault verification & troubleshooting guidance.
  - If you ARE NOT aware of the fault symptoms, proceed to Section 3.3, where a diagnostic test will determine if and where a fault exists.

**Appendix E:** Alert Code Chart - Describes the message code if the optional Data/Pak is displaying one.

Appendix F: Troubleshooting using the Operational Simulator. -This appendix is of interest only to those who have a simulator. Throughout the troubleshooting session in section 3, various tests require excitation signals which must be directed into the MJ-3A for observing circuit behavior. If you have access to a simulator, the effort involved in each test setup is greatly simplified. This section is referenced by the troubleshooting section in section 3, and steps you through the necessary configuration of the simulator.

**Appendix G:** Fault Symptom Guidance - A comprehensive listing of fault symptoms and references in the manual to where they are addressed. This appendix provides a starting point for troubleshooting when a fault symptom is known.

**Appendix H:** A quick reference for initial isolation of problems. This appendix contains a lis of the 16 most primary test points and the pages where they are referenced. Test points will appear on units s/n MJ303S 40000 and above.

Note: All illustrations in this manual which depict circuits are labeled with location identifiers. After the name of a circuit illustration will be a reference to the appendix page where it can be found with its X-Y coordinates.

Example: {20:A10} designates page REF-20 (Appendix C), X coordinate is 'A' and Y coordinate is 10. Any circuit discussed can be quickly tied to its location using this approach.

# **Applicable Documents**

It is recommended you obtain the following documents, as references are made to them throughout this manual. Contact your local Siemens representative.

Siemens Accu/Stat MJ-3A Instruction Manual (part number 21-115527-004)

Siemens Accu/Stat MJ Series Regulator Control, Operational Performance Evaluation (part number 21-115527-003)

Modification and Repair for Printed Boards and Assemblies, (IPC-R-700B) Institute for Interconnecting and Packaging Electronic Circuits, available from:

IPC 1717 Howard Street Evanston ILL, 60202

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# **SECTION 1:** General Information



# 1.1 Safety Precautions when servicing MJ-3A

As many different voltage levels are present in the MJ-3A circuitry, you must exercise caution during troubleshooting sessions. It is also necessary to observe certain precautions during operation of the electronic test equipment used during troubleshooting. Some of the precautions are designed to prevent damage to the test equipment or to the circuit where the troubleshooting operation is being performed. Other precautions are to prevent injury to the troubleshooter. Where applicable, special safety precautions are noted throughout this manual.

- 1. When troubleshooting, be especially careful of areas where AC line voltages will be present:
  - the PDS connector
  - the transformer board
  - the lower half of the control panel board
- 2. Be careful when using more than one AC source at the test station as various outlets may be wired to different phases.
- 3. Many troubleshooting instruments are housed in metal cases. These cases are connected to the ground of the internal circuit. For proper operation, the ground terminal of the test instrument should always be connected to the ground of the equipment being serviced. If you are testing the MJ-3A with it assembled, make certain that the chassis of the MJ-3A being serviced is NOT at ground. If there is any doubt, connect the equipment being serviced to the power line through an isolation transformer.
- 4. Remember that troubleshooting equipment that operates at hazardous voltages is always dangerous. Therefore, you should familiarize yourself thoroughly with the equipment being serviced before troubleshooting it, bearing in mind that high voltage may appear at unexpected points in defective equipment. Reading the operational theory (section 4) is recommended prior to troubleshooting.

- 5. It is good practice to remove power before connecting test leads to high-voltage points. It is preferable to make all troubleshooting connections with the power removed. If this is impractical, be especially careful to avoid accidental contact with equipment and objects that are grounded. If you work with one hand away from the equipment and stand on a properly insulated floor, you will lessen the danger of electric shock.
- 6. Remember that leads with broken insulation pose the additional hazard of high voltages appearing at exposed points along the leads. Check test leads for frayed or broken insulation before working with them.
- 7. To lessen the danger of accidental shock, disconnect test leads *immediately* after the test is completed.
- 8. Remember that the risk of severe shock is only one possible hazard. Even a minor shock can place you in danger of more serious risks, such causing you to touch a source of higher voltage.
- 9. Guard continuously against injury and do not work on hazardous circuits unless another person is available to assist you in case of accident.
- 10. Even if you have had considerable experience with test equipment used in troubleshooting, always study the service literature of any instrument with which you are not thoroughly familiar.
- 11. Use only shielded leads and probes. Never allow your fingers to slip down to the metal probe tip when the probe is in contact with a hot circuit. Be sure that you do not short any terminals to ground when you make voltage measurements. If the probe should slip, for example, and short out a voltage source, you could damage one or more components.
- 12. Avoid vibration and rough treatment. Most electronic test equipment is delicate.
- 13. Study the circuit being serviced before making any test connections. Try to match the capabilities of the test instrument to the circuit being serviced. It is recom-

- mended that section 4 be read for an understanding of operational theory.
- 14. Do not remove components while the unit is plugged in.

# 1.2 Recommended Troubleshooting Test Equipment

This section discusses test equipment used in troubleshooting the MJ-3A control. It is absolutely essential that you become thoroughly familiar with your particular test instruments, which can only be gained through actual practice. It is strongly recommended that you establish a routine operating procedure or sequence for each item of troubleshooting equipment. This will save time and familiarize you with the capabilities and limitations of your particular equipment, thus eliminating false conclusions based on unknown operating conditions. This section highlights features desired in test equipment used in MJ-3A troubleshooting.

# 1.2.1 Operational Simulator

The operational simulator is available through Siemens. Section 3.2 describes the recommended MJ-3A testing procedure which is divided into four discrete phases. All of these phases, but most notably phase 1 (Determining Trouble Symptoms) is best performed with the use of an operational simulator. As the MJ-3A to be repaired is no longer in service, the use of the simulator is desirable to emulate the problem reported by the operator so you can see it first hand. The simulator contains all I/O signals required to test the MJ-3A. Without a simulator, you are forced into providing your own excitation signals to the MJ regulator control using other equipment, which takes considerably more effort, and makes fault detection considerably more complex than it would be otherwise. If you do have access to a simulator, Appendix F contains guidelines that will help simplify the troubleshooting procedures in section 3. If you do not have access to the simulator then several observations described in section 3 will not be possible as written. These will be obvious at the appropriate time.

# 1.2.2 Oscilloscope



The oscilloscope is mandatory for any level of detailed troubleshooting. It may be possible to determine trouble symptoms, and perhaps localize the problem to a functioning module without one if your only intent is to replace a defective module, but anything more detailed dictates the use of one. Beyond section 3.4, this manual assumes the availability of one.

The specifications of the oscilloscope are not critical, but for maximum effectiveness, it is recommended that the scope used have the following features:

- digital storage (with full analog capabilities)
- minimum of 100 MHz real-time bandwidth
- dual channel, time delayed sweep
- equipped with external trigger input

Use only low capacitance probes to ensure that circuitry being analyzed is not loaded by the probes such that the circuit operation is affected or the measured waveform is distorted.

As an oscilloscope provides a means of visualizing time varying voltages or signals, it is a perfect troubleshooting tool for the MJ-3A which has a basic control function based on incoming time varying signals. Because the heart of the MJ-3A is a microcomputer, the controlling waveforms can best be viewed using the digital scope. Section 3 requires the use of a scope to enable comparisons against illustrated waveforms to provide fault detection in a circuit.

It is assumed that the troubleshooter has some experience with the use of an oscilloscope, and this manual will not attempt to teach the basics of operating one.



# 1.2.3 Analog and Digital Meters

The most obvious advantage of using the scope is that it shows waveform, frequency and/or time duration, and phase simultaneously with the voltage being measured. If however, the only value required when troubleshooting is voltage (or current), use the meters because of its simplicity in readout as well as its desired form of readout (rms or average). This form of readout is desirable, for example, when wanting to find the accuracy of the voltage and current magnitude circuits on the control panel board. At times, the meter is simply more convenient to use when reading AC/DC levels or checking resistance.

You will need a high-input (1 M ohm or greater) VOM (volt-ohm-meter), DVM (digital voltmeter), or VTVM (vacuum tube voltmeter) to make resistance and voltage tests.

It is preferred that the voltmeter be a true rms reading type, however, if the meter is one which displays an average voltage with an rms correction (as for most common dial point meters) it will suffice.

Note: For convenience, a reference chart for converting rms, average, peak, and peak-to-peak voltages is provided at the end of this chapter in section 1.6.

## 1.2.4 Signal Generator

# Recommended if operational simulator is NOT available.

Note: Section 3 assumes the presence of a simulator, therefore references to simulator useage will be impossible.

Used to emulate the voltage and current amplitude and frequency signals the operational simulator would normally provide.

Two signal generators are required for optimum testing.

As the basic function of the MJ-3A is to provide control based on the incoming voltage and current signals, these signals must be simulated to verify the MJ-3A is functional.

For the testing of any power factor other than unity, separate signal generators are required for voltage, and current. In this manner, any phase condition can be simulated. At least one of the generators needs to have a trigger input, and the other a sync output to maintain the phase relationship between the two signals. The generator needs to output both sinusoidal and square waves with an amplitude of at least 5 volts, and be adjustable from 0 to 100 Hz minimum.

Make certain that the generator has some form of blocking capacitor to isolate the output circuit from the DC voltages that may appear in the circuit. If the generator does not have a built in blocking capacitor, connect a .01  $\mu$ fd capacitor between the generator's output lead and the point of injection into the circuit.

## 1.2.5 Miscellaneous Tools & Accessories

### **Soldering Iron**

- tip must be grounded and have a 1/8 inch to 3/16 inch chisel point
- preferably variable power from at least 25 to 75 watt

### Solder

- Rosin core with a 60:40 tin-lead content.
- DO NOT USE ACID CORE SOLDER

### **Hand Tools**

- Long nose pliers
- Diagonal Cutters
- Wire Strippers
- 1/8 and 1/4 inch blade screwdrivers
- 1/16 inch hex Allen wrench
- 3/8 inch nut driver

### Miscellaneous

- Vacuum desoldering tool
- Desoldering braid
- utility knife
- magnifying glass
- Assortment of test leads and clips
- DIP test clips
- rosin flux remover aerosol spray
- 4 jumpers consisting of 2.5 to 3" of 20 to 26 gauge insulated wire with each end stripped about 1/4 inch
- 2 jumpers consisting of 2 to 2.5 " of 16 to 18 gauge insulated wire with each end stripped about 1/8 inch.

# 1.3 MJ-3A Troubleshooting Guidelines

## 1.3.1 General guidelines

Follow the instructions in the troubleshooting section carefully. Read the entire step before you perform each operation.

Verify that the power is removed from the MJ-3A when making repairs. This is very important to verify because signal sources can be coming from more than one power cord (signal generators, simulators). Turn off EVERYTHING connected before making repairs. Not only can you be injured by not doing so, it is also possible to damage MJ-3A circuitry as well as the test equipment itself.

Do not under any circumstances insert or remove any component, especially an IC or transistor with the low voltage power supply energized. Doing so can cause damage to the semiconductor material due to transients. An IC is easily damaged if it intermittently looses its ground potential.

When injecting a signal into a circuit (from signal generator), make sure there is a blocking capacitor in the signal generator output to prevent circuit damage. (see section 1.2.4 under signal generators)

As troubleshooting will be conducted at the component level, defects will be located in circuits by measuring and analyzing voltages at the elements of active devices. This can be done with the circuit operating and without disconnecting any parts. Once located, the defective part can be disconnected and tested or substituted, whichever is more convenient.

Transistors can be tested using small voltage scales to detect small differences in the emitter to base junction. As it must be forward biased to get current flow, in the PNP transistor the base must be more negative than the emitter and in the NPN the base must be more positive.

When you install a diode, always match the band on the diode with the band mark on the circuit board. The circuit will not work properly if a diode

is installed backwards. If the diode has a solid body, the band is clearly defined. If the diode has a glass body, do not mistake the colored end inside the diode for the banded end. Look for a band painted on the outside of the glass.

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The printed circuit boards used in the MJ-3A are sprayed with conformal coating, and as such acts as an insulator. When probing the board for a signal, ensure that you break thru the conformal coating layer, otherwise the expected signal will not be evident.

# 1.3.2 Soldering Techniques

A good solder connection will form an electrical connection between two parts, such as a component lead and a circuit board foil. A bad solder connection could prevent an otherwise well repaired MJ-3A from operating properly. It is easy to make a good solder connection if you follow a few simple rules:

- Use the right type of soldering iron. A 25 to 75 watt pencil soldering iron with a 1/8 inch or 1/16 inch chisel tip works best. Use the lowest setting (25 watt) when working with semiconductors.
- Keep the soldering iron tip clean. Wipe it often on a wet sponge or cloth; then apply solder to the tip to give the entire tip a wet look. This process (called tinning) will protect the tip and enable you to make good connections. When solder tends to "ball" or does not stick to the tip, the tip needs to be cleaned and retinned.
- Always use rosin core, radio-type solder (60:40 tin-lead content) for all soldering.
- When soldering component leads, push the soldering tip against both the lead and the circuit board foil. Heat BOTH for two or three seconds. Apply solder to the other side of the component. Let the heated lead and the circuit board foil melt the solder. As the solder begins to melt, allow it to flow around the connection. Then remove the solder and iron and let the connection cool. Cut off excess lead lengths close to the connection.
- After repair, carefully inspect the circuit board for the following problems: unsoldered connections, poor solder connec-



tions, solder bridges between foil patterns, protruding leads which could touch together. A solder bridge may occur when you make solder connections at closely spaced foils. Therefore, after each solder step, carefully inspect the foil for solder bridges and remove any that may have formed. To remove a solder bridge, hold the circuit board foil-side down and hold the soldering iron tip between the two points that are bridged. The solder will flow down the soldering iron tip to clear the bridge.

 After any soldering repair, ensure that the area repaired is cleaned with rosin-flux remover.

### Locating and Repairing poor solder joints

The low voltages in solid state equipment make them vulnerable to poor solder joints (cold solder joints). When there is no obvious cause for a low voltage at some point in the circuit or there is an abnormally high resistance, look for cold solder or printed-circuit defects. Use a magnifying glass to locate defects in printed wiring. Minor breaks in printed wiring can sometimes be repaired by applying solder at the break, however the entire board should be replaced if there is more than one.

Cold solder joints can sometimes be found with an ohmmeter. Remove all power. Connect the ohmmeter across two wires leading out of the suspected cold solder joint, flex the circuit and note any change in resistance. Look for resistance indications that tend to drift when the ohmmeter is returned to a particular scale. If a cold solder joint is suspected, reheat the joint with the soldering iron, then recheck the resistance.

# 1.3.3 Component Replacement

Re-apply conformal coating to any area of the board which had been modified.

### Integrated Circuits - Testing, Removal, Installation

### **TESTING IC'S:**

For troubleshooting an IC, the most convenient way is to test is in-circuit because the power source is available and you do not have to unsolder the IC. As the MJ-3A uses double sided PCBs, it is difficult to unsolder an IC without an expensive solder vacuuming device. Without one, it is very easy to damage the IC and/or circuit board traces.

You must measure the DC voltages applied at the IC terminals to make sure that they are available and correct. If the voltages are absent or abnormal, this is a good place for troubleshooting.

With the power sources established, the in-circuit IC is tested by applying the appropriate input and monitoring the output. In some cases, it is not necessary to inject an input because the normal input is supplied by the circuits ahead of the IC.

One drawback to testing an IC in circuit is that the circuits before (input) and after (output) the IC may be defective. This can lead you to believe that the IC is bad. The fault finding techniques used in section 3.5 of providing key waveforms will aid you in such an instance.

### **REMOVING IC's**

As previously mentioned, without a vacuum de-soldering device, it is very difficult to remove a soldered IC without damaging plated thru holes and the circuit board traces, so use extreme caution. All the printed circuit boards in the MJ-3A control panel use double-sided PC boards, so solder must be removed from both sides. Start by clipping all the IC pins going into the IC body. Heat a pin on the foil side for about 3 seconds. While the solder at the pin is melted, use the desoldering tool to force the molten solder from the plated through hole. If you are unsuccessful, then re-solder the pin and try again. Do the same for every pin.

After the holes on the foil side look relatively clean, using the desoldering braid, remove excess solder from each of the circuit side IC pins while at the same time trying to force the IC pin towards the center of the hole. This step accomplishes two purposes. First, it removes additional solder which was not removed during the desoldering from the foil side. Second, it detaches the pin from being attached to the plated-thru hole.

Use extreme caution not to damage traces on either the top or bottom of the PC board in the process. Also, when removing IC pins from the PCB holes, be careful not to damage the plated thru hole itself.

If it is ever necessary to remove an IC from its socket, use an IC puller or a small blade screw-driver. Push the end of the IC puller or screwdriver blade between the IC and the socket and carefully lift the IC free. If any IC pins become bent, straighten them carefully. When using a screw-driver to remove an IC, be careful not to damage any PC board traces.

#### **INSTALLING IC's:**

Take special care in installing any IC as they may be damaged or destroyed if installed incorrectly.

Make sure the pins are straight. The pins on the IC's may be bent out at an angle, so they do not easily line up with the holes in the IC socket. In the event a pin gets bent out of alignment, bend it back carefully. If it appears that the bend was severe enough to possibly cause the pin to break when it is inserted, apply a very thin coating of solder to it to give it more structural stability. Do not use more than a very thin coating, however, or the IC pin will become too large to fit in the PC board hole.

When you install integrated circuits, position them so that the flat side is over the flat of the outline on the circuit board. Hold the IC in place while you turn the board over. At first, solder only two pins at diagonally opposite corners of the IC. When the solder cools, check to make sure the IC is tight against the circuit board. If not, reheat the pins while you press against the IC to reseat it. Then solder the remaining pins to the foil.

### **Replacing Resistors**

Resistors are identified in the schematics (appendix C), and parts list (appendix D). by their resistance value. They are identified by a color code of four or five color bands, where each color represents a number. These colors are given in the steps in their proper order (except the last band), which indicates a resistor's tolerance. For convenience, the color code and tolerance charts are provided in figure 1-1 below and figure 1-2 on the next page.

Occasionally, a precision or power resistor may have the value stamped on it. The letter K,or M may also be used at times to signify a decimal point...K=1000, M=1,000,000 for multiplier.

Precision resistors may also be marked with a J,G,F,D,C, or B as the last character. This indicates the tolerance, and is per the chart below.

	Band #1	Band #2	Band #3	Multiplier
Color	1st	2nd	3rd	
Black	0	0	0	1
Brown	1	1	1	10
Red	2	2	2	100
Orange	3	3	3	1000
Yellow	4	4	4	10,000
Green	5	5	5	100,000
Blue	6	6	6	1,000,000
Violet	7	7	7	10000,000
Gray	8	8	8	100000,000
White	9	9	9	-
Silver	-	-	-	.01
Gold	÷	-		.1

Figure 1-1: Resistance Color Code Chart

### **Replacing Capacitors**

When you install a polarized capacitor, always identify the markings near the leads. One lead will have a positive (+) mark or a negative (-) mark near it. Be sure to install the positive lead in the positive marked hole or the negative lead in the negative-marked hole. Be careful; as only one lead may be marked.

Capacitors will be called out by their capaci-tance value in  $\mu F$  (microfarads), nf (nano-farads), or pF (picofarads) and type: ceramic, Mylar® or any other plastic material, electro-lytic, etc. The last character coded on the ca-pacitor refers to its tolerance, and can be found in the tolerance chart shown in figure 1-3.

OLERANCE	Color or	Letter
±10%	SILVER	
±5%	GOLD	ı
±2%	RED	G
±1%	BROWN	F
±0.5%	GREEN	D
±0.25%	BLUE	c
±0.1%	VIOLET	В
± 0.05%	GRAY	

Figure 1-2: Resistor Tolerance Chart

LETTER 10 pf OR LESS OVER 10 pf
---------------------------------

±0,1pf	
±0.25pf	
±0.5pf	
±1.0pf	±1%
±2.0pf	±2%
	±3%
	±5%
	±10%
	±20%
	±0.25pf ±0.5pf ±1.0pf

Figure 1-3: Capacitor Tolerance Chart

# 1.4 Modifications and Repair for Printed Circuit Boards \*

This topic is beyond the scope of this manual, but is very important to understand when using this manual. An excellent reference for PC board repair is listed in the Introduction section under "Applicable Documents".

# 1.5 Handling of Static Sensitive Components

Static electricity is an electric charge at rest on a surface. When the charge becomes sufficiently large, an electrostatic discharge (ESD) takes place when a charged person touches a part or a charged part touches another conductive surface. People can carry 1000 to 5000 volts with-out ever feeling the sensation of a discharge. The semiconductor material used in components can be ESD sensitive within this voltage range.

To avoid potential problems, proper handling procedures of ESD sensitive components must be established. The establishment of an ESD prevention strategy should revolve around the following basic guidelines:

- 1. Treat all electronic parts and assemblies as potentially static sensitive.
  - Always handle ICs by the body, not by the leads.
  - Keep all ICs in their original containers until ready for use.
  - When handling ICs, it is highly recommended that you be grounded with a wrist or heel strap through a 1 Meg ohm resistor.
  - Do not slide ICs over any surfaces.
- 2. Handle all ESD sensitive parts and assemblies at a statically safe work station.

- If possible, do the repair on a workbench which provides both a grounded work surface and a grounded floor mat (floor mat should be grounded through a 1M ohm resistor)
- Ground all metal equipment such as test equipment, solder iron, stands and fixtures.
- Tie all grounded leads to a single common ground.
- When handling ICs you should avoid clothing coming in contact with components and their assemblies.

# 3. Package parts properly for storage and transportation.

- Use antistatic tubes or conductive foam to store or transport ICs.
- Pack ICs securely to prevent motion which can generate static.

ESD damage may be the cause of a significant fraction of costly electrical component failure. ESD protective and preventative measures are fairly simple to implement but won't succeed unless they are coupled with

continued static awareness.

1.6 Conversion Chart for Average, Rms, Peak, and Peak-to-peak Values

<b>.</b>	Multiplying Factor to Get			
GIVEN VALUE	Average	Rms	Peak	Peak-to-Peak
Average	-	1.11	1.57	3.14
Rms	0.90	-	1.414	2.828
Peak	0.637	0.707	•	2.0
Peak-to-Peak	0.32	0.354	0.5	*

Figure 1-4 Convert: Average, Rms, Peak, & Peak to Peak

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# **SECTION 2:** Configuring &Calibrating the MJ-3A

# 2 - Configuring & Calibrating the MJ-3A

## 2.1 Control Panel Board

2

# 2.1.1 Setting the 8 position DIP switch

The Accu/Stat MJ-3A control must know certain de-tails concerning desired operating mode, regulator design, and power system arrangements. This information is programmed into the MJ-3A through the 8 position DIP switch located at the lower part of the slot found on the right side of the control. The functions of each switch are as follows:

Opening **Switch 1** advances the current 90°. Set closed for all single phase regulators. Set closed on three phase regulators with single phase CT. Set open on three phase regulators with phase to phase connected CT's.

Closing **Switch 2** will prevent any tap change if current is less than 2 percent of the.C.T. Primary rateing. To enable low current tap change, Switch 2 should be open.

With Switch 4 in the closed position, the control panel senses true RMS voltage and current. In the open position, the control will sense averaged derived RMS values, the same as sensed in previous analog controls. Any difference in the values is attributable to harmonic distortion. Factory setting is closed.

**Switch 5** should be closed on regulators on wye connected systems and should be open on regulators on delta connected systems.

**Switch 6** should be closed on "lagging" regulators on delta systems and should be open on "leading" regulators on delta systems. Switch 6 has no effect when switch 5 is set for a wye system. (See appendix II of the Accu/Stat Instruction manual for description of how to determine the "leading" and "lagging" regulators on an open delta system.)

The relative polarity of the utility (tertiary) winding and the current transformer must be established for the MJ-3A. **Switch 7** shifts the current signal 180 degrees if open. The correct switch setting is established by examination of the utility winding diagram and knowledge of the regulator design.

**Switch 8** is to be closed for straight design single phase regulators and for all three-phase regulators. Set this switch open for inverted design regulators. (See appendix I of the Accu-/Stat Instruction manual for description of how to determine if a given regulator is of the "straight" or "inverted" design, based upon nameplate information.)

# 2.1.2 Setting the Basic Functions

Accu/Stat MJ-3A control panels perform the basic control functions as they are influenced by the desired voltage level, voltage bandwidth, time delay and line drop compensation settings. Settings are accomplished via incremental switch points using rotary switches on the face of the control. No locking of the knobs is required.

For detailed information on the various settings, as they pertain to the regulator they are controlling, refer to the Accu/Stat Instruction Manual.

SwitchNumber / Function		CONDITION			
		Switch Open	Switch Closed		
1	90° Current Advance	Advance In	Advance Out		
2	Low Current Inhibit	Automatic Operation at any or no load	No Auto under 2% load		
3	RPF Recognition	-Provisions under RPF	Normal RPF. recognition-		
4	Sample Mode (voltage and current)	Average Derived	True RMS		
5	WYE / Delta Regulator Configuration	Delta	WYE		
6	30° Delta Regulator Config.	Delta Connection Leading Regulator	Delta Connection Lagging Regulator		
7	Utility Winding Polarity	No phase shift			
8	Straight/ Inverted Regulator	Inverted	Straight and Three Phase		

Figure 2-1: 8 POSITION DIP SWITCH SUMMATION

## 2.2 Transformer Board

The sensing transformer provides a jumper terminal strip for compensating the regulator to which it is attached. As the MJ-3A to be troubleshot has already been configured in the field for a particular regulator, it is not possible for this manual to describe how the one you are currently using is configured. A complete description on the procedure for installing these jumpers can be found in the instruction manual. (For troubleshooting purposes, you will be instructed to configure the jum-pers for specific tests.)

The transformer board also includes provisions for three auxiliary connections. The troubleshooting instructions in section 3 will inform you when to install or remove these jumpers for testing purposes.)

- Automatic Tap-change Inhibit. The closure of an external contact across the AUTO INH terminals will prevent automatic (only) operation of the control. This represents the highest level of command in the priority of automatic operation.
- Voltage Reduction Control. The closure of an external contact across the VRC terminals will cause the regulator to to activate one of two VRC modes by the percentage which has been preset on the accessory component. (Refer to MJ-3A Instruction Manual, {21-115527-004}, for more details. The toggle switch on the component must also have been set to REMOTE.
- Current Transformer Secondary. The nominal 200 mA secondary of the regulator CT is routed through these terminals. These terminals are shorted at the factory and must remain shorted except as they are used to accommodate auxiliary apparatus, such as a current demand meter.

# 2.3 Interface Option Board

# 2.3.1 Data/Pak Current Display Settings

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Controls equipped with Data/Pak accessory require the correct CT ratio be input to the control to provide the correct current display. This is accomplished by properly setting the 5 position DIP switch (SW5) located on the interface board.

Set the 5 position DIP switch in accordance with the Figure 2-2 to provide a proper multiplier for the current display on the Data/Pak. See nameplate of the regulator for CT primary rating.

## 2.3.2 Setting Data/Pak Configuration

Setting Integration Time for Voltage, Current & Power Factor:

Accu/Stat MJ-3A controls will display voltage, current and power factor as a time integrated readout. The time intervals selected can be set independently of each other via three 4 position DIP switches (SW6-Volts, SW7-Amps, SW8-Power Factor.

Position 4 on switches 6,7, and 8 relates to present value parameters on the Data/Pak. Set closed for instantaneous response. Set open for lagged response. If 4 is set open, integration periods will then be selected by positions 1,2 and 3. (Factory set closed)

Positions 1,2 and 3 select the integrating period for drag hand parameters and the present value parameters if position 4 is set open. (refer to figure 2-3)

CT Primary	Pos.	Pos.	Pos	Pos	Pos.
Rating	1	2	3	4	- 5
50	C	C	С	С	C
75	0	.C	C	С	С
100	O C	0	С	C C	С
150	O C	O C	C C	C C	
200 °	C	С		C	C
250	0	С	0	С	С
300	C	0	0	С	С
350	0	0	О	С	С
400	C	С	C	0	С
600	0	C	C	О	υυυυ
700	С	·O	C	О	С
800	0		С	Ο	С
1000	0	0 C 0	C O	0	С
1200	С	0	0	0	С
1400	C O O C	С	0	0	С
2000	0	0	0	О	С

### O=Open

### C=Closed

Figure 2-2: Data/Pak Current Display Multiplier (SW5).

Demand Period (Min)	Pos	Pos 2	Pos
0.25	Ć	C	C
0.50	0	C	С
1.0*	$C_{\wedge}$	0	С
2.0	0	0	С
5.0	C	С	О
15,0**	O	С	0
30.0	С	0	0
60.0	0	0	0

<sup>\*</sup> Factory set, SW6,SW8.

Figure 2-3: Data/Pak Display Intigration Time Chart

# 2.4 Setting the Accessory Functions

# 2.4.1 Voltage Limit Control

Set the knobs to the maximum and minimum voltages to be held. Turning the VLC toggle switch off deactivates any minimum/maximum settings on the VLC.

# 2.4.2 Voltage Reduction Control

Set the knob to the percent voltage reduction desired when activated. Place the toggle switch in "remote" to have it activated via the VRC contacts on the transformer board.

<sup>\*</sup>This setting may be used for direct reading of CT secondary current (in millamperes).

<sup>\*\*</sup> Factory set, SW7.

SECTION 3: MJ-3A Troubleshooting Procedures

# 3.1 Bench Setup for MJ-3A Troubleshooting

It is assumed that the MJ-3A is **believed** to be defective and is removed from service. The remainder of this section assumes that the MJ-3A is at a workbench with the test equipment and tools which were recommended in section 1.

The easiest way to troubleshoot the MJ-3A is to disassemble it, removing all printed circuit boards. Lay them out on your workbench in a way that the control panel board cables attaches to the transformer board, and the option modules (if available) also connect to the control panel board. The operational simulator (if available) should then be in close enough proximity to the setup such that the PDS connector from the control panel board mates to the simulator.

In the process of disassembling the MJ-3A, it is necessary to remove the *power* and *sensing* fuses which are attached to the control panel. For trouble-shooting purposes only, solder a jumper wire from N1-N2 and M1-M2 to bypass the fuses. REMEMBER TO DISCONNECT THE JUMPERS WHEN TROUBLESHOOTING HAS BEEN COMPLETED!

Suggestion #1: .... In the event the MJ-3A unit you are troubleshooting does NOT have an interface PCB (Printed Circuit Board) with a Data/Pak option -BUT- you do have access to them, it is highly recommended that you use them for troubleshooting purposes. Using the Data/Pak (which requires the interface board to operate) makes troubleshooting much easier.

Suggestion #2:...Use the table of contents to locate specific sections which are referenced in the test procedures. This is by far easier than trying to find a section by randomly looking through the pages.

Suggestion #3:...The remainder of this section assumes the availability of an oscilloscope to monitor waveforms. If one is not available, the DVM referenced in section 1.3 can be used.

- Are you familiar with the troubleshooting strategy used in this manual?
  - YES: go to section 3.3 to begin
  - NO: go to section 3.2

# 3.2 MJ-3A Troubleshooting Strategy

# 3.2.1 Summary

The goal in troubleshooting the MJ-3A is to be most efficient in locating and correcting a particular defect. In order to do this, a logical step-by-step approach is required.

**STEP 1:** You must be able to use test equipment and proper tools to repair defective circuitry. As a minimum for electronic repair, you must be able to use the test equipment and tools mentioned in section 1.2

STEP 2: You must become familiar with the operation of the MJ-3A regulator control. This includes the functions of all MJ-3A controls and adjustments and how to manipulate them. It is difficult, if not impossible, to check out an MI-3A without knowing how to set its controls. To do a truly first-rate job of determining trouble symptoms, you must have a complete and thorough knowledge of the normal operating characteristics of the MJ-3A. In addition, you must be able to determine the symptoms in order to decide whether the equipment is performing normally or abnormally when using the control panel controls. This manual guides you along on a step-by-step approach, but does require a basic understanding of the system and its terminology. For a better understanding of both, refer to Siemens Accu/Stat Instruction Manual (P/N) 21-115527-

**STEP 3:** You should become familiar with the operation of the MJ-3A at the circuit board level. Although this section will aid in fault-finding as much as possible, it is strongly advised that you read section 4 of this manual (operational theory), and find out how each circuit works when operating

normally. In this way, you will know in detail how the system *should* work. This will enable you to better understand why a waveform you monitored in a particular circuit deviates from the desired one illustrated in this section, and thus better understand the nature of the problem.

SUGGESTION: If time does not permit you to read section 4 in its entirety, you can proceed with step 3 until you find out the malfunctioning module involved. At this point read section 4 as it relates only to that module.

**STEP 4:** A systematic, logical procedure must be instituted in order to locate the trouble. This is the purpose of section 3. By following the systematic approach, the trouble can be quickly located. Basically there are four major approaches this manual uses to troubleshoot the MJ-3A. They are:

- 1) determine trouble symptoms
- 2) localizing trouble to a functioning module
- 3) isolate the trouble to a circuit, and
- 4) locate the specific trouble, probably to a specific part.

**STEP 5:** You must be able to perform complete checkout procedures on the repaired equipment. One major reason for the checkout is that there may be more than one problem. Without the checkout, you may have assumed that you have fixed the problem, when in reality, you may have only fixed part of it. It is also possible that some initial problems were masking others not yet found.

# 3.2.2 Definition of the Systematic, Logical Procedure

The systematic approach discussed in step 4 is by far the most complex step, and this is where the emphasis is placed in this section. The four major phases of MJ-3A troubleshooting are summarized as follows:

### PHASE 1: DETERMINING TROUBLE SYMPTOMS

- This phase involves determining what the MJ-3A is supposed to do when it is operating normally and, in recognizing improper operation when that normal job is not being done. This symptom-determining phase involves noting both the normal and abnormal performance indications, manipulating the equipment's operational controls to gain further information, and correlating the symptoms. At the end of this phase, you will know that something is wrong and have a fair idea of what the trouble is, but you do not know just what area of the MJ-3A is faulty. This is established in phase 2.

It is assumed at this point, that the MJ-3A is *believed* to be defective and is removed from service. The nature of the problem is probably vaguely defined. Be aware that it is always possible for an operator to report a trouble that is actually the result of improper control settings. For this reason, it would be desirable to determine first the nature of the problem first-hand and verify the defective claims made.

PHASE 2: LOCALIZING TROUBLE TO A FUNC-TIONING MODULE OR SUBSYSTEM - The MJ-3A regulator controls can be subdivided into modules (circuit boards) that have a definite purpose or function. Block diagrams of the MJ-3A (Appendix B) show the functional relationship of all major sections in the complete assembly and are the most logical source of information to use when localizing trouble to a functional module. Initially, the schematics will be used only for referencing waveforms at key areas. Actual component references will for the most part, not be made during this phase. The MJ-3A is divided into several functioning units consisting of discrete circuit board assemblies with well defined input/output functions. These are 1) control panel PCBoard, (Printed Circuit Board), 2) transformer PCBoard, 3) interface PCBoard, 4) Data/Pak display option PCBoard, 5) VLC option PCBoard, and 6) VRC option PCBoard.

When simulating the operation of the MJ-3A, the module most believed to need attention is often found in phase 1 (determining trouble symptoms). If that is the case, then you can proceed directly to the verification of trouble relating to that module.

The completion of the determining trouble symptoms step will *not* isolate the trouble to a defective component; that comes later in the troubleshooting process.

### PHASE 3: ISOLATING TROUBLE TO A CIRCUIT -

After the trouble is localized to a single functional unit, the next phase is to isolate the trouble to a circuit in a faulty module. To do this, you consider the signal paths in the circuitry that contain the indicating instruments or other builtin aids that point to abnormal performance (i.e. band indicator LEDs,

3

alert light, watchdog, Data/Pak). By concentrating on this circuitry and ignoring the circuits that produce normal indications, you narrow down or isolate the limits of the possible trouble. The isolating step involves the use of test equipment such as meters, oscilloscopes, and signal generators for signal tracing and signal substitution in the suspected faulty area. By making the measurements and comparing them against the illustrated readings and making valid educated estimates, you can systematically and logically isolate the trouble to a single defective module. Actual repair techniques and devices are not used until after the specific trouble is located and verified. Observations are based on indications of external test equipment used for signal tracing or signal substitution, and the decisions relate to whether these indications are normal or abnormal, based on both your knowledge of how the MJ-3A works and its resemblance to the pictured waveform in the block diagram.

PHASE 4: LOCATING THE SPECIFIC TROUBLE -

Although this troubleshooting step refers only to locating the specific trouble, it includes a final analysis of the complete procedure and the use of repair techniques to remedy the trouble once it has been located. The final analysis will enable you to determine whether some other malfunction caused the component to become faulty or whether the component located is the actual cause of the trouble. An oscilloscope is used to observe waveforms and a meter is used to measure voltages and make resistance and continuity checks in order to pinpoint the defective component. After the trouble is located, a final analysis of the complete troubleshooting procedure should be made to verify the trouble. The trouble should be then be repaired, and the equipment checked out for proper operation.

When making repairs, it is suggested that you use only replacement parts obtained through Siemens in order to ensure that they meet the high quality levels initially designed into the MJ-3A.

Section 3.3 is used for phase 1, as it helps to determine trouble symptoms. If the fault symptom is obviously related to a specific circuit board, then it will reference you to section 3.5 (phase 3 & 4) directly (Isolating trouble to a circuit, and Locating the specific trouble). If however, the fault is of a broader nature, it may be necessary to first localize the problem to a circuit board (module) first. In this case, you are directed to section 3.4 (phase 2) which will determine the circuit board, then lead you to the specific circuit in section 3.5.

You will be eventually led to section 3.5 which will illustrate the circuit in question and provide a procedure to verify its operation. Go to the circuit mentioned first in the "Action" list. If it appears OK, then go down the list of each of the mentioned circuits until the fault is found.

# **START OF TROUBLE SYMPTOM ANALYSIS:**

 Set Normal/External source switch on MJ control to "normal".

# 3.3 Determining Trouble Symptoms

## 3.3.1 Initial Settings of Operator and Simulator Controls

Set the controls to the settings listed below. Doing so will ensure consistency with the routines followed in this manual. Reading the *Siemens MJ Operational Performance Evaluation*, *P/N 21-115527-003*, manual will be very helpful in understanding the organization and approach used in the troubleshooting section of this manual. This is especially true with reference to the initial setup proceedures and terminology. Also this manual contains the same settings that will be used in the troubleshooting section of this manual.



### 3.3.1.1

## MJ-3A Control Settings

(Refer to control overlay panel on MJ-3A)

- Manual auto switch "off"
- Bandwidth = 6.0V
- Voltage Level = 120V
- Time Delay = 30 seconds
- Resistance volts = 0, polarity = '+'
- Reactance volts = 0, polarity = '+'
- SW9, (the 8 position DIP switch), (starting nearest bottom of PCBoard) = 'COCCCCOC', where C=closed and O=open)
- if Data/Pak is present, set to VOLTS

### MJ-3A Jumper Connections

- On the 12 point terminal strip (TB1) on the transformer board, connect a jumper between the P and P14 points (the two bottom points). This should be the only jumper connected on that strip for the start of the test.
- 3
- To the six point terminal strip (TB2) on the transformer board.
- Connect a jumper C2 to C.
- Be certain there is <u>not</u> a jumper at "VRC" or at "AUTO-INH".
- The presence or absence of a relay at RLY
   1 position is not important at this time.
- If Interface Option Board and Data/Pak Option Board are both attached, set position 4 on switches 6,7, and 8 on the Interface Option Board CLOSED. This will ensure instantaneous response settings for voltage, current, and power factor displayed on the Data/Pak option board.
- If VRC (Voltage Reduction Control) option is attached, turn toggle switch to OFF position.
- If VLC (Voltage Limit Control) option is attached, turn toggle switch to OFF position.

## ...

### 3.3.1.2

### **Initial Simulation Setup**

- » Do you have an operational simulator?
  - YES: Review Appendix F, set up simulator, then proceed to 3.3.2
  - No: The MJ-3A should be provided with the following signals, as a minimum:
    - Line voltage potential (110 to 130 volts rms) at U2 and P2 inputs of PDS connector.
    - No input to C2 input on PDS connector. When current flow is required input must be applied.

Note: Without a simulator you may not be able to complete many observations and operations directly. However you may be able to improvise.



# 3.3.2 Fault Symptom Verification

Section 3.3.2 leads you through the necessary steps to determine not only the faulty circuit board, but in most instances what circuit sub-system is defective as well. This procedure can be used as both an initial fault verification, as well as a final inspection once the board has been fixed to ensure fault correction.

If you do not know the specific fault or are unsure that one exists, then proceed with this section. If you are aware of a specific fault, then instead of starting at the beginning of section 3.3.2, look up the fault in Appendix G, which list them alphabetically. There you will find a section number that you can go directly to in this manual.

When this section is completed, one of two things will be true:

- 1) a fault was NOT verified because an essential operating requirement was overlooked, thus no fault exists or
- 2) a fault was verified which will be isolated in later sections if the failure mode crosses more than one circuit board, or can be determined immediately if isolated to one board.

(NOTE: Steps 3.3.2.1 thru 3.3.2.50 are reserved for troubleshooting the Control Panel board, however not all steps have been utilized.

The purpose of the "Watchdog" light on the MJ-3A control panel is to determine if the panel is functioning normally. Accordingly, this indicator will be the basis of troubleshooting.



3.3.2.1

» Is the Control Panel Watchdog light flashing at about a 6 - 8 Hz Rate?

- YES: Go to 3.3.2.2
- NO:

### > VERIFY:

- Control Panel Switch SW11, (lower left coner of control panel), is in NORMAL position
- Jumpers N1-N2 and M1-M2 have been added to control panel test board as instructed.
- Cables from connectors J2 and J3 are attached to transformer board
- PDS connector is attached to excitation source
- Excitation power source to PDS connector is "on"
- LED has not broken loose

### > ACTION:

- If an item of the verification process caused the watchdog to begin flashing, then proceed to 3.3.2.2
- If watchdog indicator light is still not flashing after the verification process, then a trouble symptom has been identified. The next step is to localize the fault to a functioning module ... Proceed to section 3.4.1



### 3.3.2.2

- » Is reverse power flow light "off".
  - YES: Go to 3.3.2.3
  - NO:

### > VERIFY:

The CT magnitude was disconnected per initial setup in 3.3.1 and appendix F.

### > ACTION:

- Press control panel reset button (SW10). If light remains on, then fault has been isolated to defective control panel board. Refer to section
  - 3.5. 1.17 (Circuit Annunciation Logic )
  - 3.5.1.11 (Reset Circuit)

### 3.3.2.3

- » Is the alert light illuminated?
  - **YES:** Go to section 3.3.2.4
  - NO:

### > VERIFY:

The CT magnitude was disconnected per initial setup in 3.3.1 and appendix F

### > ACTION:

- Press control panel reset button (SW10 located on the right side of and behind the control panel.). If light remains on, then fault has been isolated to defective control panel board. Refer to section:
  - 3.5.1.17 (Circuit Annunciation Logic )
  - 3.5.1.14 (C.T. Zero Cross Detection Circuit)
  - 3.5. 1. 12 (P.T. Zero Cross Detection Circuit)
  - 3.5.1.11 (Reset Circuit)

# ...

### 3.3.2.4

- » Is voltage present at the voltmeter test terminals, on control panel?
  - YES: Go to 3.3.2.5
  - NO:

### > VERIFY:

Jumper +P - P14 loose or not installed on transformer board

### > ACTION:

A trouble symptom has been identified. The next step is to localize the fault to a functioning module.... proceed to 3.4.2.

## ...

### 3.3.2.5

- » Make necessary adjustments such that the measured voltage (voltage level read from the voltage test terminals or read from the Data/Pak) is 3-4 volts less than the setting on the voltage level switch.
- » Is the "low" light illuminated?
  - **YES**: Go to 3.3.2.6
  - NO:

### > VERIFY:

- Control panel switch settings are per instruction in section 3.3.1
- Pressing control panel reset button (SW10) should illuminate this LED while button is held in.

### > ACTION:

- Refer to section:
  - 3.5.1.17 (Circuit Annunciation Logic)
  - 3.5.1.18 (Operator Setpoint Switch Logic)
  - 3.5.1.13 (P.T. Magnitude Input Circuit)
  - 3.5.1.9 (Power Supply- low voltage A/D reference)

### 3.3.2.6

- » Press the Neutralite lamp button (on the simulator). Did the NEUTRALITE lamp glow?
  - YES: Go to 3.3.2.7
  - NO:

### > VERIFY:

PDS Connector is making good contact

### > ACTION:

- Refer to section :
  - Faulty Neutralite circuitry, see 3.5.1.3

### ...

### 3.3.2.7

- » Press the operations counter button, (on the simulator) and release it. Did the operator counter activate and increment by a count of two every time the circuit was activated?
  - YES: Go to 3.3.2.8
  - NO:

### > VERIFY:

PDS Connector is making good contact

### > ACTION:

- O Refer to section:
  - 3.5.1.5 (Operations Counter Interface)

# ...]

### 3.3.2.8

- » Press the drag hands reset button (SW14) on the lower control segment of the control panel board. Is the drag hand reset light illuminated while the button is held depressed or is 120V present at U11, (on the PDS connector), when the simulator is not present?
  - YES: Go to 3.3.2.9
  - NO:

### > VERIFY:

PDS Connector is making good contact

### > ACTION:

- O Refer to section:
  - 3.5.1.4 (DRAG HANDS reset interface)

## [...]

### 3.3.2.9

- » Slowly turn the voltage level, (on the simulator), or voltage level switch such that the measured voltage and the voltage setting are within 1.0 volt of each other
- » Is the "IN" band lamp on?
  - YES: Go to 3.3.2.10
  - NO:

### > VERIFY:

- Pressing control panel reset button should illuminate this LED while button is held in.
- Control panel switch settings are per instructed in section 3.3.1

### > ACTION:

- Refer to section :
  - 3.5.1.17 (Circuit Annunciation Logic)
  - 3.5.1.18 (Operator Setpoint Switch Logic)
  - 3.5.1.13 (P.T. Magnitude Input Circuit)
- 3.5.1.9 (Power Supply low voltage A/D reference)

## 3.3.2.10

Slowly turn the voltage level, (on the simulator), or voltage level switch such that the

measured voltage is 3-4 volts higher than the switch setting

- » Is the "HIGH" band lamp on?
  - YES: Go to 3.3.2.11
  - NO:

### > VERIFY:

- Pressing control panel reset button should illuminate this LED while button is held in.
- Control panel switch settings are per instructed in section 3.3.1

### > ACTION:

- Refer to section:
  - 3.5.1.17 (Circuit Annunciation Logic)
  - 3.5.1.18 (Operator Setpoint Switch Logic)
  - 3.5.1.13 (P.T. Magnitude Input Circuit)
  - 3.5.1.9 (Power Supply low voltage A/D reference)



### 3.3.2.11

- » Place the MANUAL/AUTO toggle switch to MANUAL. Toggle the TAP RAISE switch. Did the 'J' light, (on the simulator), illuminate, or is 120V present at 'J', (on the PDS connector), without the simulator
  - YES: Go to 3.3.2.12
  - NO:

### > VERIFY:

PDS Connector is making good contact

### > ACTION:

- O Refer to section:
  - 3.5.1.6 (Raise/Lower relay interface



- 3.3.2.12
  - » Toggle the TAP LOWER switch. Did the 'K' light, (on the simulator), illuminate, or is 120V presentat'k', (on the PDS connector), without the simulator?
    - YES: Go to 3.3.2.13
    - NO:
      - > VERIFY:
        - PDS Connector is making good contact
      - > ACTION:
        - Refer to section :
          - 3.5.1.6 (Raise/Lower relay interface
- 3.3.2.13
  - » Toggle the AUTO/MANUAL switch back to AUTO. If "K" light is not on wait about 30 seconds. After thirty seconds, is "K" light on?
    - YES: Go to 3.3.2.14
    - NO:
      - > VERIFY:
        - Switch #2 of Control Panel Configuration Switch SW9 is in open position per 3.3.1
        - Response timer is not set for more than 30 seconds
      - > ACTION:
        - Refer to section
          - 3.5.1.6 (Raise/Lower Relay interface)
          - 3.5.1.16 (Relay Driver Circuits)
          - 3.5.1.18 (Operator Setpoint Switch Logic)
- ··· 3.3.2.14
  - » Slowly turn the voltage level, or voltage level switch such that the measured voltage is within 1.5 volts of the switch setting
  - » Did the HIGH light turn off? Did the IN-BAND light turn on? Is "K" light off?
    - YES: (to all three questions) Go to 3.3.2.15
    - NO:
    - > VERIFY:

- Bandwidth setting is adjusted per 3.3.1
- Voltage differential is not greater than 1.5 volts

#### > ACTION:

- Refer to section:
  - 3.5.1.6 (Raise/Lower Relay interface)
  - 3.5.1.16 (Relay Driver Circuits)
  - 3.5.1.13 (P.T. Magnitude Input Circuit)



# 3.3.2.15

- » Slowly turn the voltage level, or voltage level switch such that the measured voltage is at least 2 volts less than the voltage level setting.
- » Wait at least 30 seconds.
- » Is "J" light on?
  - YES: Go to 3.3.2.16
  - NO: (next page)
    - > VERIFY:
      - Switch #2 of Control Panel Configuration Switch SW9 is in "open" position per 3.3.1
      - Response timer is not set for more than 30 seconds

#### > ACTION:

- Refer to section:
  - 3.5.1.6 (Raise/Lower Relay interface)
  - 3.5.1.16 (Relay Driver Circuits)
  - 3.5.1.18 (Operator Setpoint Switch Logic)

### 3.3.2.16

- » Slowly turn the voltage level, or voltage level switch such that the measured voltage is within 1.5 volts of voltage level setting. Connect the simulated current magnitude to PDS terminal C2 in phase with the P.T. magnitude by switching the power flow switch to forward creating a forward power flow.
- » Did ALERT light go out?
  - YES: Go to 3.3.2.17
  - NO:

#### VERIFY:

- There are still other alert codes set... see Appendix E.
- Current level provided to C2 must be greater than 2 mA.
- PDS Connector is making good contact

#### > ACTION:

- Refer to section:
- Refer to section that Alert Code Logic Refers you to. If due to C.T., then.....
  - If Alert code indicates a C.T problem., determine which module. Proceed to section 3.4.1.3.

### ··· 3.3.2.17

- » Transfer power flow to reverse power flow. After a 5 second delay, did the RPF light come on?
  - YES: Go to 3.3.2.18
  - NO:
    - > VERIFY:
      - Using a scope that C.T. and P.T. are out of phase
  - > ACTION:
    - Refer to section:
      - 3.5.1.12 (P.T. Zero Cross Detection Circuit)
    - 3.5.1.14 ( C.T. Zero Cross Detection Circuit)
    - 3.5. 1.17 (Circuit Annunciation Logic)
    - 3.5. 1. 15 (CT magnitude)

### 3.3.2.18

- » Temporarily remove (or lower) the PDS terminal P2 voltage by lowering the "L" (load) variac on the simulator. Did the observed voltage stay the same?
  - YES: Go to 3.3.2.19
  - NO:
    - > VERIFY:
      - RPF light is illuminated, if not.. refer to 3.3.2.17
    - > ACTION:
      - Refer to section :
        - 3.5.1.16 (Relay Driver Circuits)

## 3.3.2.19

- » Put power flow in "forward" position. Close position #2 of SW9, (the 8 position DIP switch).
- Slowly turn the voltage level, or voltage level switch such that the measured voltage is at least 4 volts lower than the voltage setting.
- Wait for "J" light to illuminate (30 seconds), then return the voltage level setting to within 1.5 volts of the measured voltage.
- » Provide a low current (less than 2 mA.) on terminal C2 by turning the current magnitude potentiometer on the simulator counter-clockwise. This will cause the ALERT light to illuminate. Ensure that the measured voltage is at least 4 volts less than the voltage setpoint.
- » Wait 30 seconds.
- » Is it true that neither the "J" light or the "K" light came on?
  - YES: Go to 3.3.2.20
  - NO:
  - > VERIFY:
    - SW9 Position #2 of the 8 position DIP switch is closed.

#### > ACTION:

- Refer to section :
  - 3.5.1.18 (Operator Setpoint Switch Logic)



- **3.3.2.20** 
  - » Re-open SW9 switch position #2 (of the 8 position DIP switch). Did the "J" light turn on?
    - YES: Go to 3.3.2.21
    - NO:
      - > VERIFY:
        - The conditions per 3.3.2.19 have been met.
      - > ACTION:
        - Refer to section:
          - 3.5.1.18 (Operator Setpoint Switch Logic)
- 3.3.2.21
  - » Turn power OFF to all of the system.
  - » Is a relay installed in RLY 1 of the transformer board?
    - YES: Go to 3.3.2.22
    - NO: Go to 3.3.2.24
- 3.3.2.22
  - » Re-configure the jumpers on the 12 point sensing transformer terminal strip:
    - +PB to 20
    - P14B to 20
    - P14A to 25
    - +PA to 20
  - » Remove the jumper which had been connected from P to P14. (This configuration tests the sensing transformer by introducing no correction for forward power flow, and a minus 5 volt correction for reverse power flow.)
  - » Re-connect transformer board, and turn on system power.
  - » Verify power flow is in FWD mode. Apply current magnitude at maximum level.
  - Wing the voltmeter, measure and compare the voltage between the test terminals and the incoming voltage on PDS connector P2 to E. Is it true that there is NO difference in voltage?
    - YES: Go to 3.3.2.23
    - NO:
    - > VERIFY:

- The correct jumper configuration has been installed
- That the RPF light is NOT on
- The switch #8 switch status is "COCCCCOC" per 3.3.1
- > ACTION:
  - Refer to section
    - 3.5.2.1 (Sensing Transformer)
- 3.3.2.23
  - » Put power flow to reverse setting. Using the voltmeter, measure and compare the voltage between the test terminals and the incoming voltage on PDS connector U2 to E.
  - » Is there a 5 volt difference between the two readings?
    - YES: Go to 3.3.2.24
    - NO:
    - VERIFY:
      - The correct jumper configuration has been installed
      - O That the RPF light is on
      - The switch #8 switch status is "COCCCCOC" per 3.3.1
    - > ACTION:
      - Refer to section :
        - 3.5.2.1 (Sensing Transformer)

### 3.3.2.24

- » Turn OFF the power switch to the system. If you modified any jumper settings in 3.3.2.22, remove themnow and replace the jumper on P to P14.
- » Put a jumper across the AUTO INH terminals on the transformer board.
- » Turn the power switch back ON.
- » Put voltage level switch to 106 volt setting. Put power flow in forward mode.
- » Wait at least 30 seconds. Are both the "J" and "K" lights off?
  - YES: Go to 3.3.2.25
  - NO:

#### > VERIFY:

- The AUTO-INH jumper is providing good continuity.
- > ACTION:
  - Refer to section :
    - 3.5.2.3 (P.T. Zero Cross Transformer)

### 3.3.2.25

- » Remove the AUTO-INH jumper. Does the "K" light illuminate?
  - YES: Go to 3.3.2.26
  - NO:
  - > VERIFY:
    - The AUTO-INH jumper is definitely removed
  - > ACTION:
    - Refer to section:
      - 3.5.2.3 (P.T. Zero Cross Transformer)

### ··· 3.3.2.26

- » Verify that current is in forward power flow mode.
- » Open switch SW9 position #8 (of the 8 position DIP switch). Does reverse power light illuminate after 5 seconds?
  - **YES:** Go to 3.3.2.51
  - NO:
    - > VERIFY:
      - C.T. is connected.
      - Alert light is not on.
    - > ACTION:
      - Refer to section:
        - 3.5.1.18 (Operator Setpoint Switch Logic)

(This concludes testing of the control panel board. NOTE: When using the Data/Pak In the following steps with the simulator, the actual power factor reading on the Data/Pak can vary slightly due to component tolerances in the simulator.)

### 3.3.2.51

- » Do you have **both** an interface module and Data/Pak option?
  - YES: Go to 3.3.2.52
  - NO: Do you have either a VLC or VRC option module?
    - YES: Go to 3.3.2.67
    - NO: Go to 3.3.2.101

### 3.3.2.52

- » Is the Interface Board Watchdog light flashing at about a 6 8 Hz Rate?
  - **YES**: go to 3.3.2.53
  - NO:
  - > VERIFY:
    - O Cable is correctly attached.
  - > ACTION:
    - O Refer to section:
      - 3.5.3.2 (Power Supply)
      - 3.5.3.1 (Oscillator)
      - 3.5.3.5 (Reset circuit/ watchdog circuit)

## 3.3.2.53

- » Is the Interface Board Transmit Light (backside of MJ) flashing about every half-second?
  - YES: Go to 3.3.2.54
  - NO:
  - > VERIFY:
    - Conditions in 3.3.2.52 have been met
  - > ACTION:
    - Shut off power and disconnect Data/Pak option board. Turn on power. If 3.3.2.53 is now satisfied, then problem exists with this module. If not, turn off power again and replace the Data/Pak. Try the same approach with the VRC and VLC modules as well. If problem is tied to option module, refer to trouble-shooting for that module:
      - Data/Pak Option Board ... section 3.5.4
      - VLC Option Board ..... section 3.5.5

- VRC Option Board ..... section 3.5.6
- Refer to section :
  - 3.5.3.10 (Control Panel Communications Interface)
  - 3.5.3.9 (Control Panel Bus Arbitration)
  - 3.5.3.10.5 (XMIT LED circuit)

### 3.3.2.54

- » Set SW9 DIP switch (located on the control panel board) to its initial starting conditions (COCCCCOC).
- » Attach the voltmeter to the test leads. Rotate the Operator calibration switch (on the side panel) until the voltage on the Data/Pak and the voltage measured at the test terminals are the same (within 1/8 [.125] volts of each other). Is the calibration LED illuminated?
  - YES: Go to 3.3.2.55
  - NO:
  - > VERIFY:
    - The Data/Pak, is at the "volts" setting.
  - > ACTION:
    - Refer to section:
      - 3.5.1.18 (Operator Setpoint Switch Logic)

### 3.3.2.55

- » Does the Data/Pak appear to be operating Correctly?
  - YES: Go to 3.3.2.56
  - NO:
    - > VERIFY:
  - > The cable from the interface board to the Data/Pak is correctly installed.
  - > ACTION:
    - Refer to section:
      - 3.5.4 (Data/Pak Option Board)

### 3.3.2.56

- » Set the following DIP switches on the interface board:
  - CT ratio switch (#5) to (CCOCC) [set for 200A CT primary rating].
  - AMP SWITCH (#7), VOLT SWITCH (#6), and PF SWITCH (#8) all are set to (COCC).
- » Set power flow for "forward". Apply full current magnitude.
- » Do COMP VOLTS and VOLTS display the same value?
  - **YES:** Go to 3.3.2.57
  - NO:
  - > VERIFY:
    - Control Panel Switches set in accordance with 3.3.1
  - > ACTION:
    - 3.5.3.7 (Interface Board Switch Decoding)
    - 3.5.4 (Data/Pak Option Board)

### 3.3.2.57

- » Does PF display a very high (slightly less than .999) power factor, and does AMPS display a reading greater than 150?
  - YES: Go to 3.3.2.58
  - NO:
    - > VERIFY:
      - Data/Pak knobs are in correct settings
      - C.T. is attached.
    - > ACTION:
      - Refer to section :
        - 3.5.3.7 (Interface Board Switch Decoding)
        - 3.5.4 (Data/Pak Option Board)

### 3.3.2.58

- Fully rotate the CT (current magnitude potentiometer on the simulator) counter-clockwise. Verify that the ALERT light illuminates.
- Turn the Data/Pak selector to the ALERT position and verify the existence of the code (should be "5000").
- » With the Data/Pak selector set to amps, rotate the current magnitude potentiometer clockwise until a reading of 1or2 appears.
- » Turn the Data/Pak selector to the ALERT position and verify the existence of the code (should be "1000").
- » Press and release the reset button (SW3) on the interface board.
- » Does the display momentarily read zero as switch is released?
  - YES: Go to 3.3.2.59
  - NO:
    - > VERIFY:
      - The reset button is SW3. The other pushbutton is the DRAG HANDS reset (SW4).
    - > ACTION:
      - Refer to section :
        - 3.5.3.5 (Interface Board Reset Circuit)

## ...

#### 3.3.2.59

- » Record the readings for the LOW VOLT, HIGH VOLT, MAX AMP, LEAD PF, and LAG PF.
- » Turn system off for 30 seconds, then turn it back on.
- » Are the values the same as those before you shut off the power? While observing each one of the readings again, press the Data/Pak Drag Hands reset button. Do at least some of the values reset to another value?
  - YES: Go to 3.3.2.60
  - NO:

#### > VERIFY:

The DRAG HAND reset button is SW4. The other pushbutton is the RESET (SW3).

#### > ACTION:

- Refer to section:
  - 3.5.3.4 (Power Monitor Circuits)
  - 3.5.3.3 (Microcomputer Memory Management)
  - 3.5.3.7 (Interface Board Switch Decoding)
  - 3.5.4 (Data/Pak Option Board)

## ...

#### 3.3.2.60

- » Disconnect current to C2 by turning the power flow switch on the simulator to OFF. Set the RESISTANCE VOLTS on the control panel to 6 volts with the polarity switch in the + position. Set the REACTANCE VOLTS on the control panel to 8 volts with the polarity switch in the + position. Turn the Data/Pak to COMP VOLTS.
- » Adjust the voltage level setting such that the setting is within 1.5 volts of the measured value. The IN-BAND indicator LED will be activated...
- » Connect C2 with maximum current and forward power flow.
- » Is LOW indicator LED on? Does COMP VOLTS read at least 1 volt less than the measured input voltage?
  - YES: Go to 3.3.2.61
  - NO:
  - > VERIFY:

° C.T. is attached.

#### > ACTION:

- Refer to section :
  - 3.5.1.1B (Operator Setpoint Switch Logic)
  - 3.5.3.7 (Interface Board Switch Decoding)

(NOTE: Test procedures 61 thru 67 test for the DIP switches on the control panel board . It is much easier to test when using the Interface & Data/Pak option modules.)



### ...

### 3.3.2.61

- » Reset line drop adjustments RESISTANCE VOLTS and REACTANCE VOLTS both back to zero.
- Set conditions for Forward Power Flow, maximum current and lagging power factor. Is the RPF LED off? Is the power factor about .700 to .800 lag?
  - **YES:** Go to 3.3.2.62
  - NO:

#### > VERIFY:

- Power factor is lagging.
- > ACTION:
  - Refer to section:
    - 3.5.1.18 (Operator Setpoint Switch Logic)

### 3.3.2.62

- » Switch to reverse power flow mode. Wait at least 5 seconds. Is RPF light now on? Does the power factor remain as in 3.3.2.61?
  - YES: Go to 3.3.2.63
  - NO:

#### > VERIFY:

 Control panel DIP switches are set in accordance with 3.3.1

#### > ACTION:

- Refer to section:
  - 3.5.1.18 (Operator Setpoint Switch Logic)

## 3.3.2.63

» Revert to Forward Power Flow. Wait 5 seconds for response. Set control panel DIP switch, position #7 to the closed position......

(COCCCCC). Is the RPF light on? Does the power factor remain as in 3.3.2.61?

- **YES:** Go to 3.3.2.64
- NO:

#### > VERIFY:

 Control panel DIP switch #8, position 7 is firmly in a closed position

#### > ACTION:

- Refer to section :
  - 3.5.1.18 (Operator Setpoint Switch Logic)

### **3.3.2.64**

- » Set DIP switch position #1 open. Is power factor now leading?
  - YES: Go to 3.3.2.65
  - NO:

#### > ACTION:

- Refer to section:
- 3.5.1.18 (Operator Setpoint Switch Logic)

### ... 3.3.2.6**5**

- » Leaving switch #1 open, open switch position #5. Is power factor now .2 to .30 leading?
  - YES: Go to 3.3.2.66
  - NO:

#### > ACTION:

- Refer to section:
  - 3.5.1.18 (Operator Setpoint Switch Logic)

## 3.3.2.66

- » Open switch position #6. Is power factor now .95 to .96 leading
  - YES: Go to 3.3.2.67
  - NO:

#### > ACTION:

- Refer to section:
  - 3.5.1.18 (Operator Setpoint Switch Logic)

(NOTE: Test procedures 67 - 69 test the VRC option, procedures 70 - 71 test the VLC option, and procedures 72 - 73 test both. If you do not have either of these option modules, then proceed to 3.3.2.101)

- 3.3.2.67
  - » Ensure that control panel board 8 position DIP switch is set to its initial condition per section 3.3.1 (COCCCCOC).
  - » Do you have a VRC option module?
    - NO: Go to 3.3.2.70
    - YES: Proceed
  - » Set the voltage switch such that it is within 1.5 volts of the measured voltage and the in-band light illuminates.
  - » Set the VRC switch to 5% setting. Turn on VRC by putting the switch in a LOCAL setting. Does the "K" light illuminate as soon as the VRC is activated without regard for time delay setting?
    - YES: Go to 3.3.2.68
    - NO:
      - > VERIFY:
        - Switch on VRC is in a detent position
      - > ACTION:
        - O Refer to section:
          - 3.5.6 (VRC option)
- 3.3.2.68
  - » Put VRC switch into REMOTE switch setting. Does the "K" light immediately go off and stay off when the transition is made?
    - YES: Go to 3.3.2.69
    - NO:
    - > ACTION:
      - Refer to section :
        - 3.5.6 (VRC option)

- 3.3.2.69
  - While the system is powered up, momentarily touch the two VRC contacts on the transformer board with a jumper wire, then remove. Does the "K" light illuminate when the jumper makes contact and immediately go off when the jumper is removed?
    - YES: Go to 3.3.2.70
    - NO:
      - > VERIFY:
        - The VRC contacts are shorting together.
      - > ACTION:
        - O Refer to section:
          - 3.5.2.3 (P.T. Zero Cross Transformer T4)
          - 3.5.6 (VRC Option)
- 3.3.2.70
  - » Do you have a VLC option module?
    - NO: Go to 3.3.2.101
    - YES: Turn toggle switch on VLC to ON position. Go to 3.3.2.71.
- **3.3.2.71** 
  - » Set the VLC UPPER volts to a setting less than the actual voltage.
  - » Do all band indicators extinguish themselves? Does the "K" light illuminate immediately?
    - YES: Go to 3.3.2.72
    - NO:
    - > ACTION:
      - Refer to section :
        - 3.5.5 (VLC option)
        - 3.5.6 (VRC Option)

- 3.3.2.72
  - » Turn both accessory toggle switches to OFF. Set rotary VRC switch to 10%. Set VLC LOWER to 115V, VLC UPPER to 125 volts. Adjust voltage until Data/Pak reads about 120 volts. Turn on both VLC and VRC to LOCAL setting. Is the "K" light on?
    - YES: Go to 3.3.2.73
    - NO:
      - > ACTION:
        - Refer to section:
          - 3.5.5 (VLC option)
          - 3.5.6 (VRC Option)
- **□** 3.3.2.73
  - » Adjust the voltage such that the it goes below 115 volts. Is the "J" light on?
    - YES: Go to 3.3.101
    - NO:
    - > ACTION:
      - O Refer to section:
        - 3.5.5 (VLC option)
        - 3.5.6 (VRC Option)

(NOTE: Test procedures 74-100 are reserved for future use )



#### 3.3.2.101

- » Phase 1 (Determining Trouble Symptoms) has been concluded.
- » Turn off power.
- » If you have not discovered a problem, it is possible that the problems may have been mis-reported due to the operator's mis-understandings of how the system should operate. If you are convinced that there is a problem, or want further verification, section 3.5 contains each circuit path and key input/ output signals.



# 3.4 Localizing Trouble to a Functioning Module or Sub-system

This section should be used only if directed specifically by another section. The fault will have been identified in the "determining trouble symptoms" of section 3.3, or a known fault would have been looked up in the cross reference section of Appendix G.

This section helps to determine when a problem is related to the:

- 1)electrical portion of the control panel board
- 2) transformer board
- 3) electronic portion of the control panel board

Due to the nature of how the transformer board is electrically "daisy-chained" into the control panel board, it is not immediately apparent where the specific fault lies. This section helps to isolate faults to not only the particular board, but also to the particular circuit on the board as well.

This section will accomplish two purposes:

- it will establish which circuit board is causing the fault
- it will provide clues of which circuits in particular appear to be causing the problem, and reference you to that appropriate circuit in section 3.5

Proceed with the suspected circuits, in the order shown, until the actual circuit has been isolated.

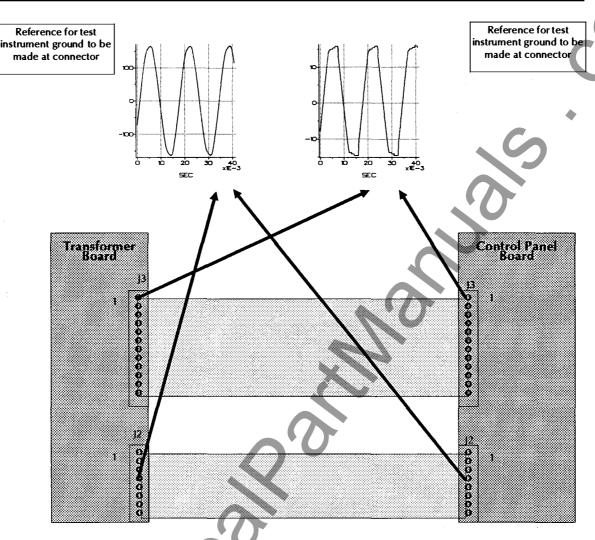


Figure 3-1: No apparent power to control panel



# 3.4.1 No apparent power to control panel.

#### » POSSIBLE CAUSES:

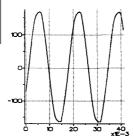
- Control panel board not receiving power from transformer board due to bad connection
- Transformer board malfunctioning

- Transformer board not receiving power from electrical portion of control panel board due to bad connection.
- Defective Electronic Section of control panel board (i.e. watchdog annunciation circuitry)
- PDS connector not receiving proper signals:

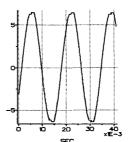
- 3.4.1.1
  - » Verify if the control panel board is receiving AC power from the transformer board
    - Connect a scope or DVM from ground to pin 1 of connector J3 as shown in Figure 3.1.
      - o If waveform is absent, go to 3.4.1.2
      - o If waveform appears, fault has been isolated to defective control panel board. Refer to section (circuit):
        - 3.5.1.8 (power supply logic reference)
        - 3.5.1.17 (circuit annunciation logic)
        - 3.5.1.10 (oscillator)
        - 3.5.1.11 (reset circuit)
- 3.4.1.2
  - » Verify that the connector from transformer board is not causing the problem
    - Connect a scope or DVM to pin 1 of connector J3 as done in 3.4.1.1, but this time at transformer board.
      - o If waveform is still absent, go to 3.4.1.3.
      - If waveform appears, fault has been isolated to defective connector, or solder connection. Repair it and continue with 3.3.2.1.
- ···· 3.4.1.3
  - » Verify if the transformer board is malfunctioning
    - Connect a scope or DVM to pin 4 of connector J2 at the transformer board as shown in Figure 3-1.
      - o If waveform is absent, go to 3.4.1.4.
      - o If waveform appears, fault has been isolated to defective transformer board. Refer to section:
        - 3.5.2.1 (transformer board)
- 3.4.1.4
  - » Verify that the connector from control panel board is not causing the problem
    - Connect a scope or DVM to pin 4 of connector J2 as done in 3.4.1.3, but this time at the control panel board.

- If waveform is still absent, go to 3.4.1.5.
- If waveform appears, fault has been isolated to defective connector, or solder connection. Repair it and continue with 3.3.2.1.
- **□** 3.4.1.5
  - » Verify that power is getting to the control panel board
    - Connect a scope or DVM to PDS connector inputs on the control panel board between U2 and E (ground) signals.
      - o If waveform is still absent, go to 3.4.1.6
      - of lf waveform appears, fault has been isolated to defective control panel board (electrical section). Refer to section:
        - 3.5.1.2 (potential & utility winding interface)
- 3.4.1.6
  - Find out why PDS connector is not getting power. It appears that either the excitation source is turned off or is malfunctioning, and this is beyond the scope of this manual.

Reference for test instrument ground to be made at connector



Reference for test instrument ground to be made at connector



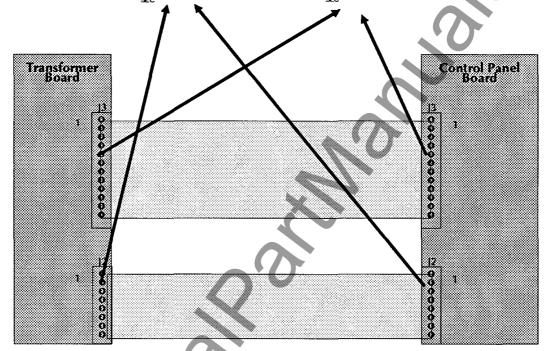


Figure 3-2: No apparent P.T. sensing

....

# 3.4.2 No apparent P.T. sensing

## » POSSIBLE CAUSES:

- Control panel board not receiving power from transformer board due to bad connection
- Transformer board malfunctioning

- Transformer board not receiving power from electrical portion of control panel board due to bad connection
- Defective Electronic Section of control panel board (i.e. P.T. magnitude circuitry)
- PDS connector not receiving proper signals.

## 3.4.2.1

- » Verify if the control panel board is receiving AC power from the transformer board
  - Connect a scope or DVM from ground to pin 5 of connector J3 as shown in Figure 3.2.
    - o If waveform is absent, go to 3.4.2.2
    - If waveform appears, fault has been isolated to defective control panel board. Refer to section (circuit):
      - 3.5.1.13 (P.T. Magnitude Input Circuit)

## **...** 3.4.2.2

- » Verify that the connector from transformer board is not causing the problem
  - Connect a scope or DVM to pin 5 of connector J3 as done in 3.4.2.1, but this time at transformer board.
    - o If waveform is still absent, go to 3.4.2.3.
    - If waveform appears, fault has been isolated to defective connector, or solder connection. Repair it and continue with 3.3.2.4.

### **....** 3.4.2.3

- » Verify if the transformer board is malfunctioning
  - Connect a scope or DVM to pin 2 of connector J2 at the transformer board as shown in Figure 3-2
    - o If waveform is absent, go to 3.4.2.4
    - If waveform appears, fault has been isolated to defective transformer board. Refer to section:
      - 3.5.2.1 (Transformer Board, Sensing Transformer)

### ···· 3.4.2.4

» Verify that the connector from control panel board is not causing the problem

- Connect a scope or DVM to pin 2 of connector J2 as done in 3.4.1.3, but this time at the control panel board
  - If waveform is still absent, go to 3.4.2.5
  - If waveform appears, fault has been isolated to defective connector, or solder connection. Repair it and continue with 3.3.2.4.

### 3.4.2.5

- » Verify that power is getting to the control panel board
  - Connect a scope or DVM to PDS connector inputs on the control panel board between P2 and E (ground) signals.
    - If waveform is still absent, go to 3.4.2.6
    - If waveform appears, fault has been isolated to defective control panel board (electrical section). Refer to section:
      - 3.5.1.2 (Potential & Utility Winding Interface)

# 3.4.2.6

» Find out why PDS connector is not getting power. It appears that either the excitation source is turned off or is malfunctioning, and this is beyond the scope of this manual.



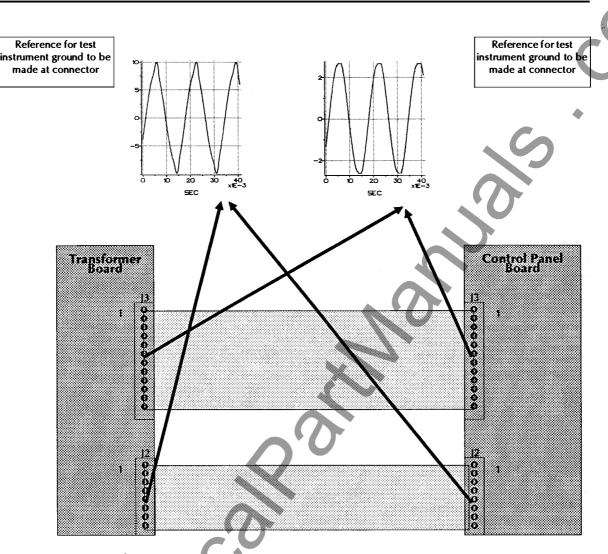


Figure 3-3: No apparent C.T. sensing



# 3.4.3 No apparent C.T. sensing

### » POSSIBLE CAUSES:

 Control panel board not receiving power from transformer board due to bad connection

- Transformer board malfunctioning (C -C2 jumper missing or defective transformer)
- Transformer board not receiving power from electrical portion of control panel board due to bad connection.
- Defective Electronic Section of control panel board (i.e. C.T. magnitude circuitry)
- PDS connector not receiving proper signals.

## ••••

#### 3.4.3.1

- » Verify if the control panel board is receiving AC power from the transformer board
  - Connect a scope or DVM from ground to pin 6 of connector J3 as shown in Figure 3.3.
    - o If waveform is absent, go to 3.4.3.2
    - o If waveform appears, fault has been isolated to defective control panel board. Refer to section (circuit):
      - 3.5.1.15 (C.T. Magnitude Input Circuit)



### 3.4.3.2

- » Verify that the connector from transformer board is not causing the problem
  - Connect a scope or DVM to pin 6 of connector J3 as done in 3.4.3.1, but this time at transformer board.
    - o If waveform is still absent, go to 3.4.3.3.
    - If waveform appears, fault has been isolated to defective connector, or solder connection. Repair it and continue with 3.3.2.17.



#### 3.4.3.3

- » Verify if the transformer board is malfunctioning
  - Connect a scope or DVM to pin 5 of connector J2 at the transformer board as shown in Figure 3-3.
    - o If waveform is absent, go to 3.4.3.4
    - o If waveform appears, fault has been isolated to defective transformer board. Refer to section:
      - 3.5.2.4(Transformer Board, AUX C.T. Transformer)



#### 3.4.3.4

» Verify that the connector from control panel board is not causing the problem

- Connect a scope or DVM to pin 5 of connector J2 as done in 3.4.1.3, but this time at the control panel board
  - o If waveform is still absent, go to 3.4.3.5
  - If waveform appears, fault has been isolated to defective connector, or solder connection. Repair it and continue with 3.3.2.17.



### 3.4.3.5

- » Verify that power is getting to the control panel board
  - Connect a scope or DVM to PDS connector inputs on the control panel board board between C2 and E1 (ground) signals.
    - o If waveform is still absent, go to 3.4.3.6
    - If waveform appears, fault has been isolated to defective control panel board (electrical section). Refer to section:
      - 3.5.1.1 (C.T. interface)



#### 3.4.3.6

Find out why PDS connector is not getting power. It appears that the excitation source is turned off or may be malfunctioning, which beyond the scope of this manual. THIS PAGE INTENTIONALLY BLANK,

# 3.5 Isolating Trouble to a Circuit

Section 3.3 helped determine if there was a fault based on operating characteristics. It has then led you to here directly orvia section 3.4 where the fault was narrowed down to a circuit board. Based on the analysis of the fault found , you are guided to the circuit most suspected of causing the fault.

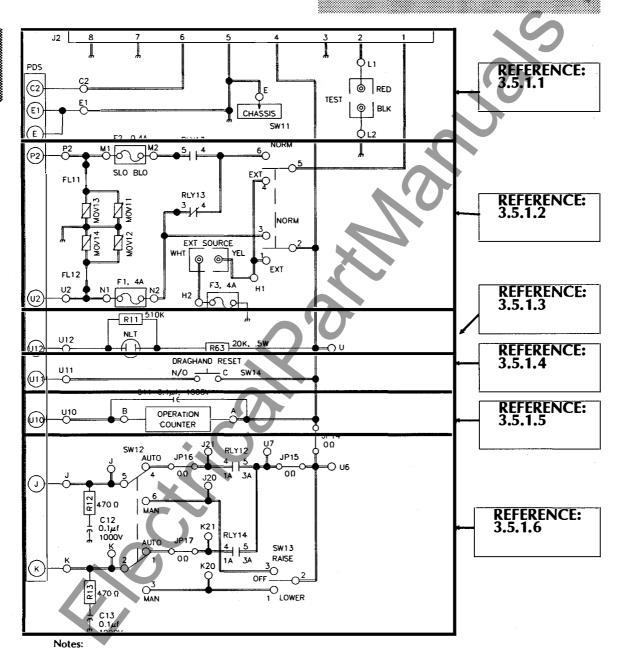
If after going through the procedure for the circuit in which you are directed, you still do not find the faulty component, go back to the area in section 3.3 and refer to the next suggested circuit. ...

3 .5.1 Control Panel Board: Fault Verified or Suspected

# Control Panel Board:

**ELECTRICAL SECTION** 

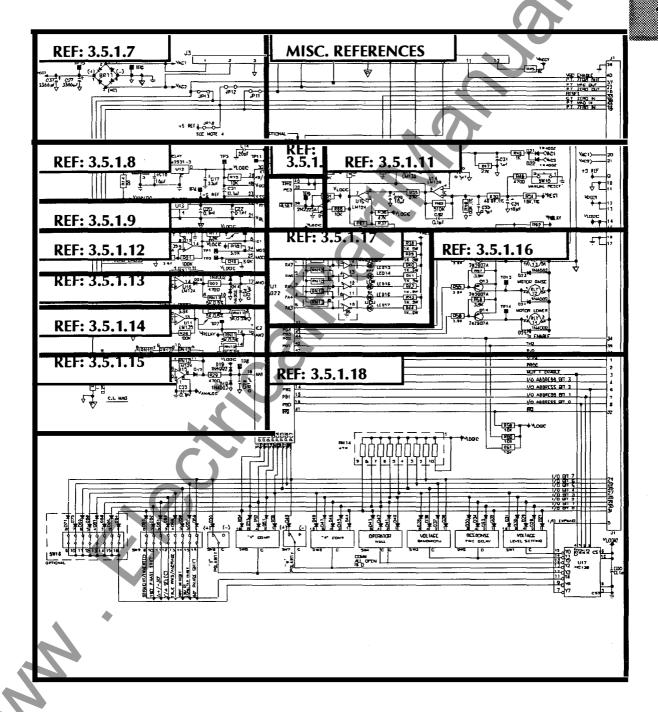
3



- 1. All resistors are .25w, 5% unless otherwise noted.
- 2. All diodes are 1n4002 unless otherwise noted.

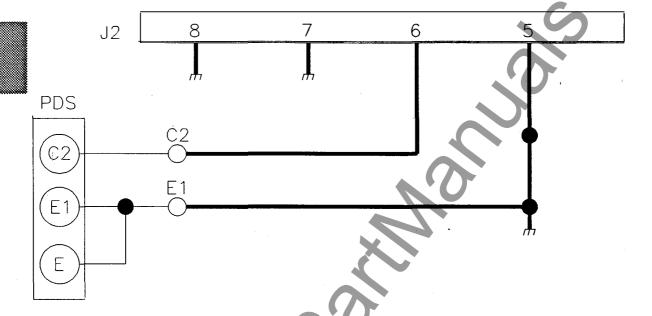
**Control Panel Board:** 

**ELECTRONIC SECTION** 



- 3.5.1.1 Current Transformer Interface
- » TEST REFERENCES:
  - 3.4.1.3

3



## ••••

### 3.5.1.1.1

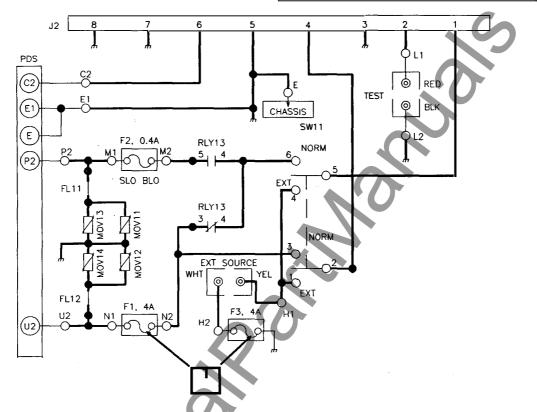
- » Actual troubleshooting of C.T. circuitry is performed at section 3.4.3.
- » If this section has led you to here, it has been determined that this isolated section of the circuitry is defective.
- » POSSIBLE CAUSES:
  - Continuity is lacking between C2 of the PDS and PIN 6 of J2 ...or...
  - Continuity is lacking between E1 of PDS and PIN 5 of J2
  - PDS not tightened or making firm contact
  - Cold solder joints on connector, or wire from PDS

...

# 3.5.1.2 Potential & Utility Winding Interface

» TEST REFERENCES:

• 3.4.1.5, 3.4.2



....

### 3.5.1.2.1

- » If you were led here due to a lack of P.T. voltage in section 3.4.2, then the fault has been isolated to this circuit.
- » Ensure test jumpers are installed for both points referenced by block #1.



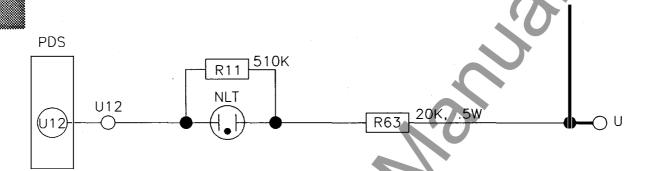
### 3.5.1.2.2

- » Verify continuity of fuse F2.
  - If FL11or FL12 is blown, observe MOV11, MOV12, MOV13, and MOV14 for damage.
- » Ensure switch is in correct position, and provides continuity between contacts.
- » Verify that RLY13 is operational. Verify contact continuity is maintained when contacts close.

3.5.1.3 Neutralite Interface

- » TEST REFERENCES:
  - 3.3.2.6

3



••••

3.5.1.3.1

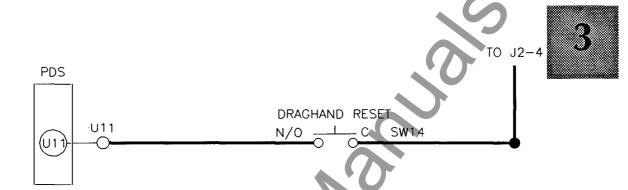
- » When the NEUTRALITE is externally activated:
  - If 120 VAC potential appears across R11, but NLT is not glowing, then replace the neon light.
  - With power off, test the resistance of R63. Replace if resistance is larger than about 21K.



# 3.5.1.4 Drag Hands Reset Interface

**»** TEST REFERENCES:

• 3.3.2.8





### 3.5.1.4.1

» When the DRAG HANDS RESET is activated:

 The closure of the button results in 120VAC potential on terminal U11. (Ground reference at E.)



### 3.5.1.4.2

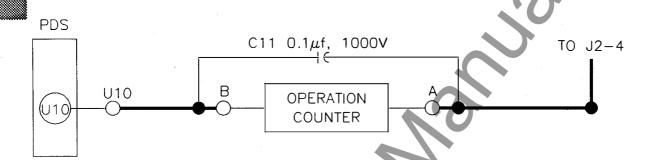
- » If DRAG HANDS reset appears defective, first verify that voltage potential is at U11 when button is pressed.
  - If potential exists, then fault lies external to PDS connector.
  - If no potential exists, place jumper across SW14 to verify switch integrity.

3.5.1.5 Operations Counter Interface

» TEST REFERENCES:

• 3.3.2.7

3



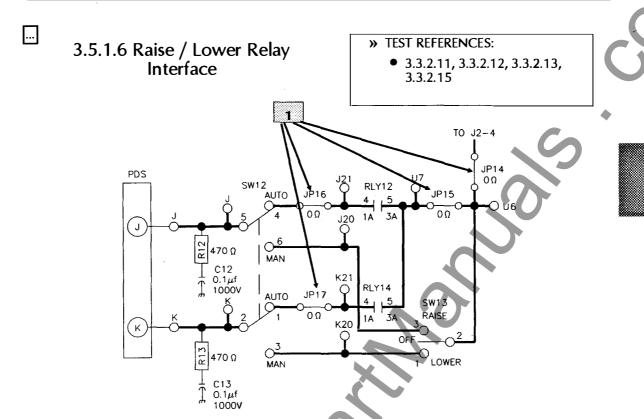
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3.5.1.5.1

3.5.1.5.2

- When an external request for operations counter update is requested...
  - The closure of the button results in 120VAC potential across points A and B. The counter moves 1/2 position on application of ground at U10, and 1/2 position at removal of ground. (Counter will advance one position [count of 2] with application and removal of ground.)
  - This can be simulated by jumpering U10 with PDS connector E.

- » If counter appears defective, first verify that voltage potential is between A & B when button is pressed.
  - If potential exists, and counter does not update... replace counter.
  - If counter needs replacing, look for any sign of damage on C11. Replace it if any sign exists.





- » If you were led here due to the lack of proper "J" or "K" response:
  - put SW12 in manual position, and test J & K response.... (120 VAC with respect to terminal E is at J or K with switch SW13 held in appropriate position)
    - o If operable, then go to 3.5.1.6.2
    - If inoperable, verify continuity of JP14,JP15, JP16, JP17 and SW13

### 3.5.1.6.2

- » If J & K responses work manually
  - verify the presence of jumpers: JP14, 15, 16, and 17. See reference block 1.
  - with power turned off... verify that no continuity exists at the following:
    - normally open contact, terminals 4 & 5 of RLY144....

### 3.5.1.6.3

- » Verify contacts 4 & 5 of RLY12 close when that relay activation is requested
  - Replace relay if defective

## 3.5.1.6.4

- » Verify contacts 4 & 5 close when RLY14 activation is requested
  - Replace relay if defective

## 3.5.1.6.5

» Test resistance of R12 and R13. Replace if not per rated value. Ensure C12 and C13 do not appear damaged... replace if necessary.

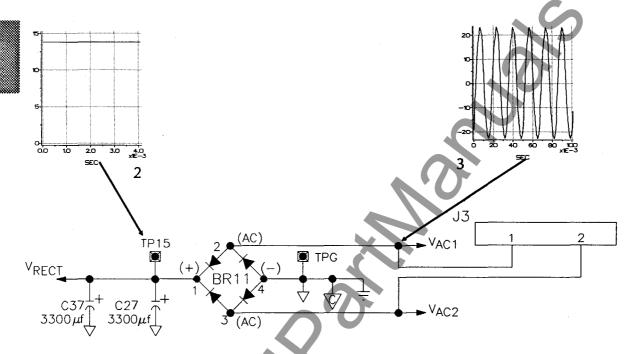
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3.5.1.7 Power Supply (Low Voltage Rectification)

**»** TEST REFERENCES:

• 3.4.1, 3.3.2.1

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3.5.1.7.1

- » Connect a scope or DVM to location pointed to by test points TP15, (VRECT). (Ground reference at TPG.)
- » Is there a rectified signal of about 13 to 18 V DC present at this point?
  - YES: If the voltage level is observed at TP15, (VRECT), then this test passes. Return to next item in current checklist.
  - NO: It was previously established that AC voltage is present at location pointed to by reference block #3 on preceeding page. Verify before proceeding to section 3.5.1.7.2
    - If AC is not present, then go back to 3.4.1.1, otherwise proceed to 3.5.1.7.2

...

3.5.1.7.2

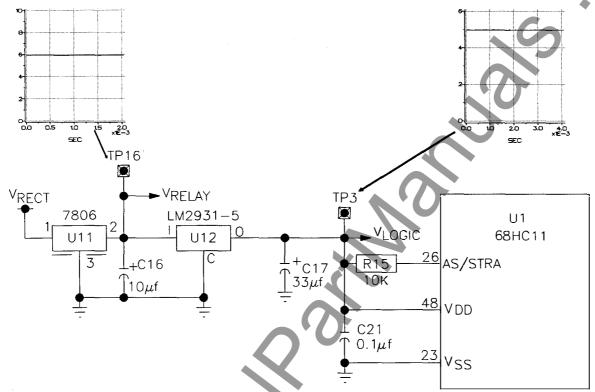
- If signal is not present at test point TP15, (VRECT), then replace bridge rectifier BR11.
- After repair, go to 3.5.1.7.1 to verify requirement is satisfied

...

# 3.5.1.8 Power Supply (Low Voltage Logic Reference)

» TEST REFERENCES:

• 3.4.1.1



<u>...</u>

#### 3.5.1.8.1

» Connect a scope or DVM from TPG to TP3 [U1, pin 48]. Is a 5 (+/- 5%) VDC logic level present?

- YES: Supply appears OK.
- NO: Go to 3.5.1.8.2

....

#### 3.5.1.8.2

- » Observe U11, pin 1 [TP15, VRECT)]. Is there a 13 to 18 VDC level present?
  - **YES:** Go to 3.5.1.8.3
  - NO: Go to section 3.5.1.7

....

#### 3.5.1.8.3

- With signs of damage to U11 or either the filter or bypass capacitors C16, C27 or C37, of VRECT, replace them.
- » After replacement, verify section 3.5.1.8.1 is satisfied.
- » Ensure correct re-installation of polarity sensitive parts C16, C27 and C37.

....

### 3.5.1.8.4

- » Connect scope or DVM from TPG to TP16. Is there a 6 (+/-5%)volt DC logic level present?
  - Yes: If the 6 volt level exists, then supply appears OK.
  - No If 6 volt level does not exist go to 3.5.1.8.5

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#### 3.5.1.8.5

- » If U12 appears defective, replace it. If there are signs of damage to bypass capacitors C17 or C21, then replace as well.
- » After replacement, verify sections 3.5.1.8.41 and 3.5.1.8.4 are satisfied.
- » Be careful to install capacitors with correct polarity.

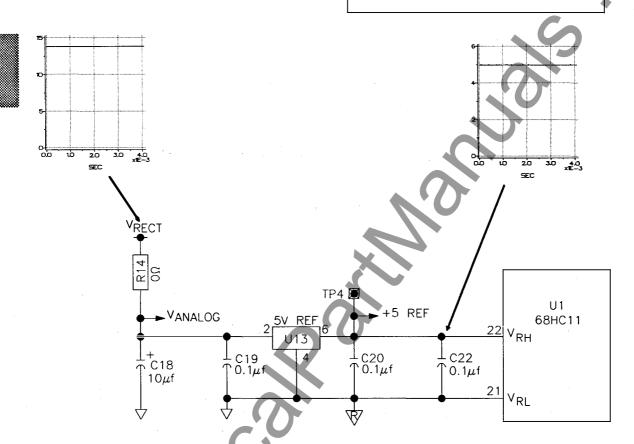
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3.5.1.9 Power Supply (Low Voltage A/D Reference)

**» TEST REFERENCES:** 

• 3.3.2.5, 3.3.1.9, 3.3.1.10

3



**3.5.1.9.1** 

- » Connect a scope or DVM from TPG) to the TP4 (U1, pin 22). Is a 5 (+/-.2%)V DC logic level present?
  - YES: If you were directed here from section 3.4, return to next item in current checklist.
  - NO: Go to 3.5.1.9.2

....

3.5.1.9.2

- » Observe the input to U13, pin 2. Is there a 13 to 18 VDC level present?
  - **YES:** Go to 3.5.1.9.3
  - NO: Go to section 3.5.1.9.4

••••

3.5.1.9.3

» If IC U13 or the bypass or filter capacitors C18,C19, C20, or C22 appear damaged then replace them. Be careful to install capacitors at the correct polarity.

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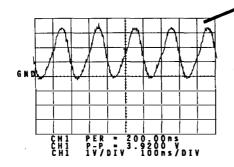
3.5.1.9.4

- » Observe test point TP15, (VRECT). Does a +13 to +18 volt DC level appear here?
  - YES: Resistor R14 is bad, replace it.
  - NO:Go to 3.5.1.8

...

# 3.5.1.10 Oscillator / Microcomputer Modes

- **»** TEST REFERENCES:
  - 3.4.1.1



OPTIONAL 4.9152 MHz X11 <u>C</u>15 20pf 20pf **TP11** R30 10M 30 R18 XTAL 3.9K MODB 24 TP1 68HC11 TP2

3

3.5.1.10.1

- » Connect a scope with a low capacitance probe from TPG to U1 pin 30 [TP11]. Does the clock frequency appear? (clock frequency is 4.9152 MHZ)
  - YES: If you were directed here from section 3.3, or 3.4, then return to next item in current checklist.
  - NO: Go to 3.5.1.10.2.

#### 3.5.1.10.2

- » An earlier step verified that the +5 volt logic level was provided to U1 pin 48. If this is not the case, go to 3.5.1.8.
- » Turn system off. With a DVM check for short across X11. If shorted locate origin. Replace R30 and C14 if necessary.
- » Verify that X11, R30, and C14 (C15 optional) are properly soldered and have continuity.
- » Re-verify 3.5.1.10.1. If no frequency yet appears, go to 3.5.1.10.3.



#### 3.5.1.10.3

Replace crystal X11. Re-verify 3.5.1.10.1.
 After replacement, verify that section 3.5.1.8.2 is satisfied. If not, replace microcomputer.

Note: If you notice frequencies other then fundamental appearing on the clock signal, replace filter C14 and optionally add C15.



### 3.5.1.10.4

- » Connect scope to TP1.
- » Does a voltage level of 5 volts +/- 5% exist?
  - YES: TP1 is functioning properly.
  - NO: Verify with DVM that resistor R18 has a resistence of 3.9K ohms, if not replace resistor R18.



### 3.5.1.10.5

- » Connect scope to TP2.
- » Does a voltage level of 5 volts +/- 5% exist?
  - YES: TP2 is functioning properly.
  - NO: Verify with DVM that resistor R19 has a resistence of 3.9K ohms, if not replace resistor R19 and go to 3.5.1.10.4.

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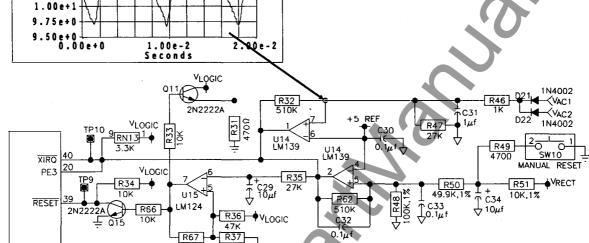
#### 3.5.1.11 Reset Circuit

1.15e+1 1.13e+1 1.10e+1 1.08e+1 1.05e+1 1.03e+1 1.00e+1 1.00e+1 1.00e+1 1.00e+1 1.00e+1 1.00e+1 1.00e+1 **>>>** 

» TEST REFERENCES:

3.4.1.1, 3.3.2.2, 3.3.2.3

3



**....** 

3.5.1.11.1

- » The 68HC11 is in a non-reset state when operating normally. Accordingly, pin 39 of the 68HC11 (TP9) should be high (5 VDC potential), . Is this true?
  - YES: If the watchdog is also flashing, (on the interface option board [if so equipped]), then the 68HC11 reset circuit, and the system reset circuits appear to be operating OK in the non-reset state.
  - NO: Go to 3.5.1.11.2

••••

3.5.1.11.2

- » Depress manual reset button (SW10) on side of control panel. Accordingly, pin 40 of 68HC11 (TP10) should go to a logic low logic state (0 VDC potential).
  - **Yes**: Go to 3.5.1.11.3
  - No: Failure of transition to a low logic state on TP10, may be the result of the IC U14, quad comparator, being defective or loss of continuity through R50, R49, or reset switch SW10. First verify with SW10 being depressed that U14, pin 5 is less than 1 VDC.
    - Yes: Replace quad comparator U14. This assumes that the analog supply voltage at U14, pin 3 and the +5 Ref voltage at U14,pins 4 and 6 are present. If not repeat sections 3.5.1.7, 3.5.1.8 and 3.1.5.9.
    - No: Check resistors R50, R49, R48, and R51 for proper continuity. Replace as necessary. With SW10 depressed, the voltage at capacitor +C34 should be at a logic low state.

### 3.5.1.11.3

- The RESET line on the 68HC11,pin 39 pointed to by TP9, should transition to a logic low state, delayed after the transition of TP10 to a logic low state. This delay is typically in the range of .25 to .5 seconds. Is this true?
  - Yes: Go to 3.5.1.11.4
  - No: Verify quad comparator output U15, pin 7 is within 3 volts of the supply voltage (typically 10 VDC). is This true?
    - Yes: Verify proper continuity of R66, and that a sufficient base bias of approximately 0.6 VDC exists at Q15. If not, replace R66 or Q15 as appropriate.
    - No: Verify proper continuity of R67,R36, R37, R35, and C29. Replace as necessary. If component continuity exists, verify voltage at U15, pin 6, (Inverting input), is lower than U15, pin 5, (non-inverting input). Is this true?
      - Yes: Replace quad comparator U15.
      - No: Verify VLOGIC level at R36 and repeat section 3.5.1.11.2.

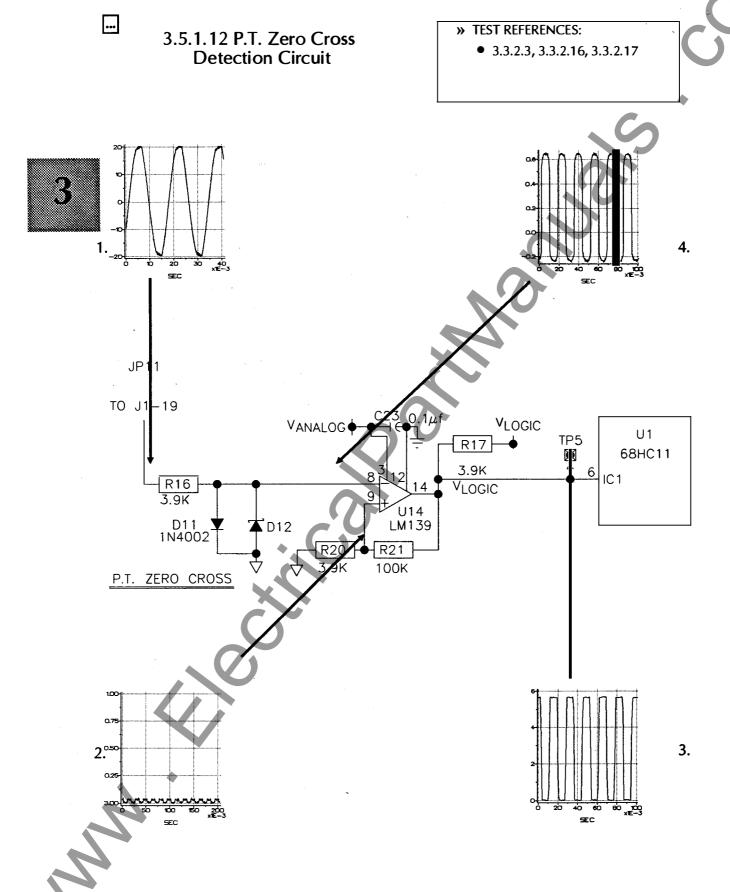
## ···· 3.5.1.11.4

- When in a reset state, the external reset signal (at J1. pin 33) should be at a logic high level (+5 VDC). Is this true?
  - **Yes**: The system active reset circuits appear to be operating properly. Proceed to 3.5.1.11.5.
  - No: Verify proper continuity of R33 and R31, and that a sufficient supply base bias of approximately (VLOGIC +0.6 VDC) exists at Q11. If not, replace R33 or Q11 as appropriate.



## 3.5.1.11,5

- » This test verifies proper operation of the loss of AC detection logic associated with the reset logic. Improper operation could result in a false reset state.
- with the control panel activated, verify that a filtered, full wave rectified signal appears at quad comparator U14, pin7 in the range of 13 to 18 VDC. Is this true?
  - Yes: This should force the output of U14, pin1 to an off state. This is not easily verified since a second U14 output at pin 2 is logically ORed with the pin 1 output. If improper operation of U14, pin 1 is suspected, replace U14.
  - No: Verify continuity of diodes D21 and D22. If shorted or open, replace. Verify continuity of R46. Replace if defective.
- » Remove AC power from control panel. Verify that pin 40 of the 68HC11 (TP10) immediately goes to a logic low(0 VDC) active reset state. Is this true?
  - Yes: Loss of AC detection logic appears to be operating properly. Reset, verification complete.
  - No: Verify voltage at U14, pin7 drops to below +5 Ref at U14, pin 6 within 2 60Hz cycles. If not, replace R.47. If true, then replace quad comparator U14 and repeat section 3.5.1.11.



### 3.5.1.12.1

- » Adjust voltage at voltage test terminals or Data/Pak (if so equipped) for 120 V rms.
- » Observe test point TP5 with a scope (with ground reference attached at TPG). Is there a 5 volt peak-to peak square wave at the output of U14?
  - YES: P.T. zero circuitry appears OK. Go to next item in checklist.
  - NO: Proper signal does not appear. Look at input voltage from JP11 to verify the presence of about a 20V p-p level as illustrated (reference block 1). Does it appear?
    - YES: Problem with P.T. zero circuitry confirmed. Proceed to 3.5.1.12.2
    - NO: Verify that jumper JP11 is installed. If this still does not correct problem, then return to 3.4.2 as voltage level at this point should have been confirmed.

### ···· 3.5.1.12.2

- » Observe U14, pin 8., (reference block 4), Does waveform appear as illustrated with a positive going level of about 600 millivolts peak, and a negative going level of about 300 millivolts peak?
  - **YES:** Proceed to 3.5.1.12.3.
  - NO: Is the positive going potential much greater than 700 millivolts peak (i.e. 1.5 volts peak), or the negative going potential much greater than 400 millivolts peak (i.e. 900 millivolts peak)?
    - o If error is on positive level replace diode D11, if error is on negative level replace diode D12.

## 3.5.1.12.3

- » Observe U14 pin 9 on scope and compare to illustration, (reference block 2). Does the waveform look similar?
  - YES: Verify R17 is properly attached and is connected to 5 VDC logic level.
     If it appears OK, then U14 is defective, replace it.
  - NO: Resistor R20 and possibly R21 appear defective. Verify continuity and replace as necessary.



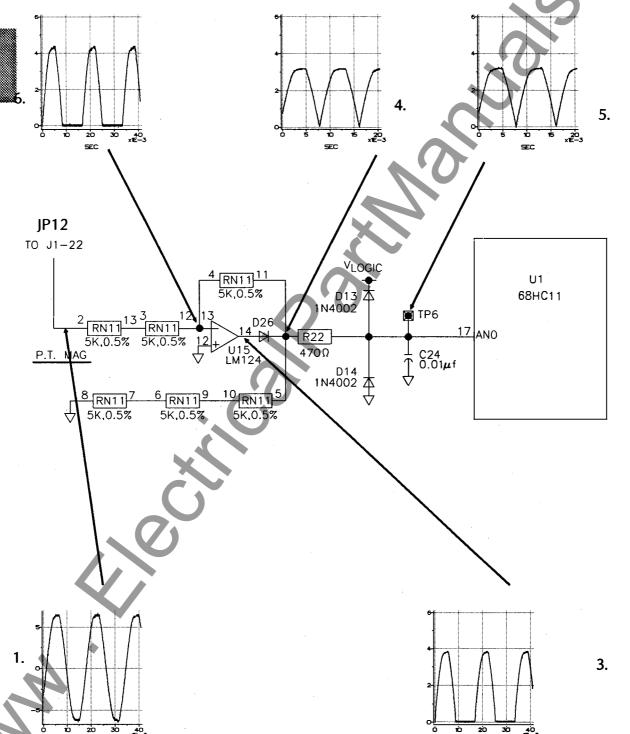


3.5.1.13 P.T. Magnitude Input Circuit

» TEST REFERENCES:

• 3.3.2.5, 3.3.2.9, 3.3.2.10, 3.3.2.14, 3.3.2.16





## 3.5.1.13.1

- » Adjust voltage at voltage test terminals or Data/Pak (if so equipped) for 120 V rms.
- » Observe test point TP6 with a scope (with ground reference attached at TPG). Is there a rectified voltage level of about 3.2 Volts peak as shown?
  - YES: P.T. magnitude circuitry appears OK, proceed to next item in checklist.
  - NO: Proper signal does not appear. Look at input voltage from JP12 to verify the presence of the ac waveform as illustrated, (reference block 1). Does it appear?
    - YES: Problem with P.T. magnitude circuitry confirmed. Proceed to 3.5.1.13.2
    - NO: Verify that jumper JP12 is installed. If this still does not correct problem, replace RN11. If this does not correct problem, then return to 3.4.2 as voltage level at this point should have been confirmed.

## 3.5.1.13.2

- » Observe U15, pin 13. Does illustrated (reference block 6) waveform appear?
  - YES: Proceed to 3.5.1.13.3
  - NO: Replace RN11.

## 3.5.1.13.3

- » Observe output U15, pin 14. Does waveform appear as illustrated (reference block 3) with a half wave rectified level of about 3.7 volts peak?
  - YES: Proceed to 3.5.1.13.4
  - NO: Possible bad diode D26 or IC U15.
     With power off, do continuity test on D26. If bad replace it. If OK, then suspect U15.

## **3.5.1.13.4**

- » Observe waveform (reference block 4) at cathode of D26. Does waveform appear?
  - YES: P.T. Magnitude circuitry confirmed.
  - NO: Go to 3.5.1.13.5

## 3.5.1.13.5

» Either resistor R22 is open or diode D13 or D14 is shorted. Determine if one is defective. If they appear OK, then look for possible cold solder joints or bad circuit traces.



## 3.5.1.13.6°

- » VOLTAGE ACCURACY:
- » A simple technique for determining the true rms voltage of the rectified waveform at ANO using a standard true rms responding 4 1/2 digit DVM is given by the following:
  - measure the dc rms component of AN0
  - measure the ac rms voltage component of ANO
  - square both values and sum, and finally
  - take the square root of the squared sums
- » This value is now directly related to the true rms voltage at the VOLTAGE TEST terminals (see equation in section 4).

» TEST REFERENCES: 3.5.1.14 C.T. Zero Cross • 3.3.2.3, 3.3.2.17 **Detection Circuit** 3. JP13 U1 TO J1-38 68HC11 C.T. ZERO CROSS 7 IC2 3.9K LM139 D15 ¥ 1N4002 R26 100K 2

# ···· 3.5.1.14.1

- » Adjust current input for 200 mA.
- » Observe TP7 with a scope (with ground reference attached at TPG). Is there a 5 volt peak-to peak square wave at the output of U14?
  - YES: C.T. zero cross circuitry appears OK.
  - NO: Proper signal does not appear. Look at input voltage from JP13 to verify the presence of about a 5.5 p-p level as illustrated, (reference block 1). Does it appear?
    - YES: Problem with C.T. zero circuitry confirmed. Proceed to 3.5.1.14.2
    - NO: Verify that jumper JP13 is installed. If this still does not correct problem, then return to 3.4.2 as level at this point should have been confirmed.

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### 3.5.1.14.2

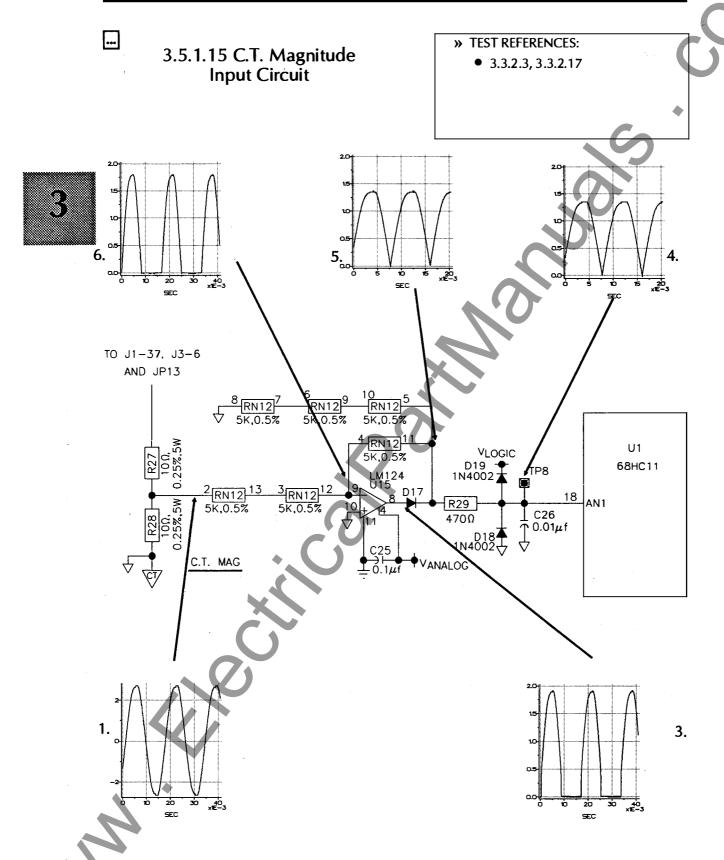
- » Observe U14, pin 10. Does waveform appear as illustrated, (reference block 4) with a positive going level of about 600 millivolts peak, and a negative going level of about 200 millivolts peak?
  - YES: Proceed to 3.5.1.14.3
  - NO: Is the positive going potential much greater than 600 millivolts peak (i.e. 1.5 volts peak), or the negative going potential much greater than 400 millivolts peak (i.e. 700 millivolts peak)?
    - o If error is on positive level replace diode D15, if error is on negative level replace diode D16.

## ••••

### 3.5.1.14.3

- » Observe U14 pin 11 on scope and compare to illustration. Does the waveform look similar?
  - YES: Verify R23 is properly attached and is connected to 5 VDC logic level. If it appears OK, then U14 is defective, replace it.
  - NO: Resistor R25, and possibly R26 appear defective. Verify continuity and replace as necessary.





## 3.5.1.15.1

- » Adjust C.T. input for 200 mA. Adjust voltage at voltage test terminals or Data/Pak (if so equipped) for 120 V rms.
- » Observe TP8 with a scope. Is there a rectified voltage level of about 1.3 Volts peak as shown?
  - YES: C.T. magnitude circuitry appears OK
  - NO: Proper signal does not appear. Look at input voltage from R28 to verify the presence of the ac waveform as illustrated, (reference block 1). Does it appear?
    - YES: Problem with C.T. magnitude circuitry confirmed. Proceed to 3.5.1.15.2
    - NO: Verify that there is 2 volts rms across resistor R28 or R27. If there is not 2V, then R28 or R27 is suspected bad, as signal to this point should have been confirmed in section 3.4.2.

## **3.5.1.15.2**

- » Observe U15, pin 9. Does illustrated, (reference block 6) waveform appear?
  - YES: Proceed to 3.5.15.3
  - NO: Replace RN12 or U15.

## 3.5.1.15.3

- Observe output U15, pin 8. Does waveform appear as illustrated, (reference block
   3) with a half wave rectified level of about
   1.8 volts peak?
  - YES: Proceed to 3.5.1.15.4
  - NO: Possible bad diode D17 or IC U15.
     With power off, do continuity test on D17 If bad replace it. If OK, then suspect U15.

## 3.5.1.15.4

- » Observe waveform at cathode of D17, (reference block 5) . Does waveform appear?
  - YES: C.T. Magnitude circuitry confirmed. Go to 3.5.1.15.5
  - NO: Either resistor R29 is open or diode D19 or D18 is shorted. Determine if either one is defective. If they appear OK, then look for possible cold solder joints or bad circuit traces.



## **3.5.1.15.5**

- » VOLTAGE ACCURACY AT AN1
- » A simple technique for determining the true rms voltage of the rectified waveform at AN1 using a standard true rms responding 4 1/2 digit DVM is given by the following:
  - measure the dc rms component of AN1
  - measure the ac rms voltage component of AN1
  - square both values and sum, and finally
  - take the square root of the squared sums
- This value is now directly related to the true rms current circulating through the C2-C terminals of the transformer board. (see equation in section 4).

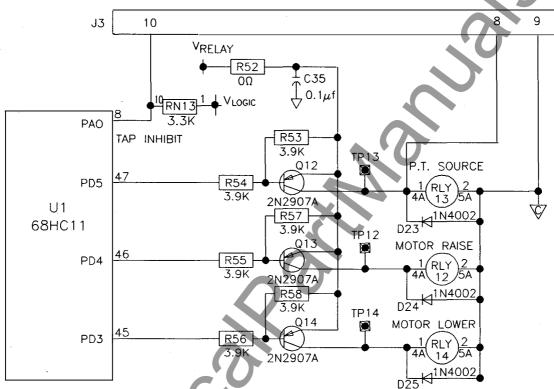
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## 3.5.1.16 Relay Driver Circuits

» TEST REFERENCES:

• 3.3.2.13, 3.3.2.14, 3.3.2.15, 3.3.2.18

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3.5.1.16.1

- » Do you wish to verify that a relay is turned OFF or ON?
  - **OFF:** Go to 3.5.1.16.2
  - ON: Go to 3.5.1.16.3

....

3.5.1.16.2

- » VERIFICATION OF RELAY IN OFF STATE
- » Each of the three relays, RLY12, RLY13 and RLY14 have a common side of the coil tied to analog ground. Thus, when a relay is de-activated (OFF), the other side of the coil should also be at 0 volts. For verification purposes, this implies that the cathodes (banded sides) of the associated flyback diodes must be at 0 volts if the relay is to be OFF.

Note: Normally open/normally closed relay contact states should be verified with relay de-energized. Contact welding may occur, resulting in improper motor control operation.

- » Is the cathode of the flyback diode for the relay in question at a ground potential (TP12, TP13, & TP14)?
  - YES: Verification of relay in OFF state confirmed. This can be further verified by ensuring that the normally open and normally closed contacts are in force.
  - NO: If the potential of the cathode was near 6 volts, then the relay is activating. If this is correct, then go to 3.5.1.16.3. If this is incorrect, then continue.
- » The relay is energized either by the 68HC11, or a fault exists, most likely, with the transistor driving it(i.e. Q12, Q13,Q14).

- » Is the respective port of the 68HC11 (PD3, PD4 or PD5) high (5 volts)?
  - YES:This is correct for an OFF state. If relay is energized, then replace respective defective transistor driver.
  - NO: This is the wrong logic for an OFF condition. Either the 68HC11 is OK, and the operation misunderstood, or the output port is defective. If the latter is the case, replace the 68HC11 microcomputer, U1.

## **└** 3.5.1.16.3

- » VERIFICATION OF RELAY IN ON STATE
- » Each of the three relays, RLY12, RL13 and RL14 have a common side of the coil tied to analog ground. Thus, when a relay is activated (ON), the other side of the coil should be at 6 volts. For verification purposes, this implies that the cathodes (banded sides) of the associated flyback diodes must be at 6 volts if the relay is to be ON
- » Is the cathode of the flyback diode for the relay in question at 6 volts DC (TP12, TP13, & TP14)
  - YES: Verification of relay in ON state is confirmed. Further verifiy by ensuring that the normally open and normally closed contacts are the inverse. If the relay is not energizing, then verify again the 6 volt potential across the coil. If so, then the relay is faulty... replace it
  - NO: If the potential of the cathode was near 0 volts, then the relay is in an off condition or no bias voltage exists. (Verify continuity of R52.) If this is true, then go to 3.5.1.16.2. If this is incorrect, then continue.
- The relay is de-energized by the 68HC11, or a fault exists, most likely with the transistor driving it (Q12, Q13, or Q14). Verify the continuity of R52.
- » Is the respective port of the 68HC11 (PD3, PD4 or PD5) low ( 0 volts)?
  - YES:This is as it should be for an ON state. If relay is de-energized, then replace respective transistor driver because it is defective.
  - NO: This is the wrong logic for an ON condition. Either the 68HC11 is OK, and the how it operates is misunderstood, or the output port is defective. If

the latter is the case, replace 68HC11 microcomputer.

## 3.5.1.16.4

- » PRELIMINARY SETUP FOR VERIFICA-TION OF AUTO INHIBIT FUNCTION.
- » Set the MJ-3A control panel Voltage Level set to 120 V, the time delay setting at 10 seconds, and the bandwidth of 4.0 V
- » On the simulator turn the voltage magnitude knob fully clockwise to create an overvoltage situation. This should cause the band indicator "high" light to come on.
- » Does the "K" light on the simulator come on after 10 seconds?
  - YES: Goto 3.5.1.16.5
  - NO: Ensure that the above settings are correct.

## 3.5.1.16.5

- » Using a DVM or scope verify that a +5 volts + or - 5% exists on either side of RN13.
- » Does this voltage exist on both sides?
  - YES: Proceed to 3.5.1.16.6
  - NO:
    - Verify continuity thru RN13 pins 1 and 10. If none replace resistor RN13
    - Go to sections 3.5.1.7 and 3.5.1.8

## 3.5.1.16.6

- » VERIFICATION OF AUTO INHIBIT FUNC-TION.
- » Place a jumper across the transformer terminal strip terminals P and P14. The tap lower light on the simulator should go out indicating that the tap change has been inhibited.
- » Does the "K" light go off when the jumper is installed?
  - YES: Tap inhibit circuit is OK.
  - NO:
    - Recheck settings listed in 3.5.1.16.4 and start over.
    - With DVM check for a voltage reading of 0 V on pin 8 of U1. (The jumper is still installed.). If 0 volts appears but "K" light is still on replace the microprocessor.

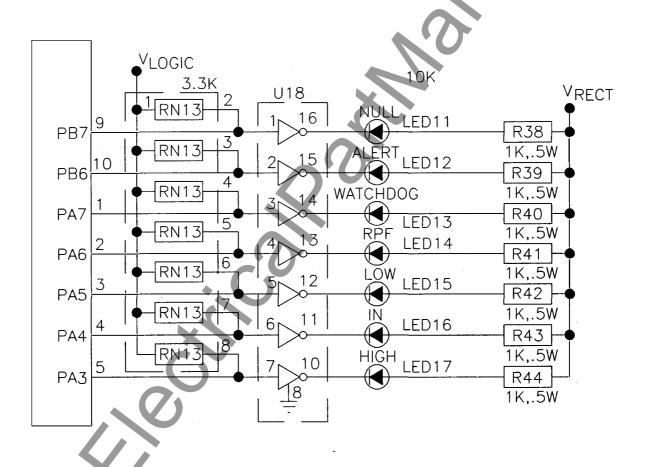
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3.5.1.17 Circuit Annunciation Logic

» TEST REFERENCES:

3.3.2.2, 3.3.2.3, 3.3.2.5, 3.3.2.9, 3.3.2.10, 3.3.2.17, 3.3.2.54

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### 3.5.1.17.1

- » Do you wish to verify that a LED is turned OFF or ON?
  - **OFF:** Go to 3.5.1.17.2
  - **ON:** Go to 3.5.1.17.3

## ••••

### 3.5.1.17.2

- » VERIFICATION OF LED IN OFF STATE
- » All of the seven LEDs , (LED11-LED17) have their anode side tied directly to the VRECT volt supply. Thus, when one of these LEDs is de-activated (OFF), the other side of the LED (cathode side) should also be at the appropriate logic high reference (VRECT). For verification purposes, this implies that the output of U18 of the associated LED driver must be at a high state if the LED is to be OFF.
- » Is the U18 driver output for the LED in question at a logic high potential?
  - YES: Verification of LED in OFF state confirmed.
  - NO: If the potential of the driver output was low (≈ 0 volts), then the LED is being directed to activate. If you believe this to be correct, then go to 3.5.1.17.3. If you believe this to be incorrect operation, then continue.
- The LED is being told to illuminate by the 68HC11, or else a fault exists, most likely with the U18 output driving it.



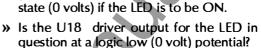
#### 3.5.1.17.2.1

- » Is the respective port of the 68HC11 (PA3, PA4,PA5, PA6, PA7, PB6 or PB7) at a logic low (0 volts)?
  - YES:This is as it should be for an OFF state. If LED is lit, then replace U18 driver because it is defective.
  - NO: This is then the wrong logic for an condition. Either the 68HC11 is OK, and the logic of how it operates is misunderstood, or the output port is defective. If the latter is the case, replace 68HC11 microcomputer, U1.

## ••••

### 3.5.1.17.3

- » VERIFICATION OF LED IN ON STATE
- » Each of the seven LEDs , (LED11-LED17), have their anode side tied directly to the VRECT volt supply. Thus, when one of these LEDs is activated (ON), the other side of the LED (cathode side) should be at 0 volts. For verification purposes, this implies that the output of U18 of the associated LED driver must be at a low state (0 volts) if the LED driver must be at a low state (0 volts) if the LED is to be ON.



- YES: Verification of LED in ON state confirmed.
- NO: If the potential of the driver output was high (≈ 16 volts), then the LED is being directed to deactivate. If you believe this to be correct, then go to 3.5.1.17.2. If you believe this to be incorrect operation, then continue. The LED is being told to illuminate due to the 68HC11 directing it to do so, or else a fault exists, most likely with the U18 output driving it or a defective LED.....

### ☐ 3.5.1.17.3.1

- » Is the respective output port of the 68HC11 (PA3, PA4,PA5, PA6, PB7, and PB8) at a logic high high (5 volts)?
  - YES:This is as it should be for an ON state. If LED is not illuminated, then verify series resistor, (R38-R44), pullup resistor network RN13, in question, or replace U18 driver because it is defective.
- » NO: This is then the wrong logic for an ON condition. Either the 68HC11 is OK, and the logic of how it operates is misunderstood, or the output port is defective. If the latter is the case, replace 68HC11 microcomputer, U1.



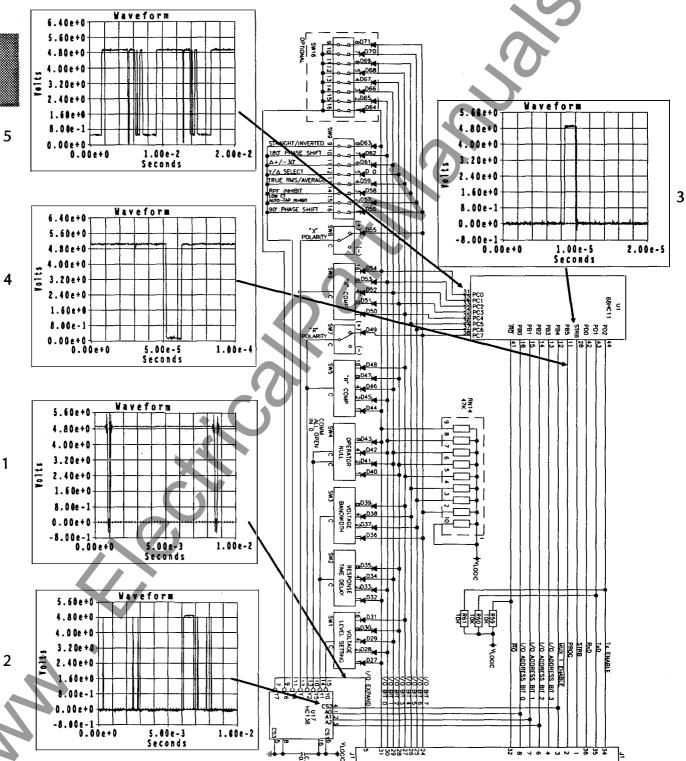
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3.5.1.18 Operator Setpoint Switch Logic

### **» TEST REFERENCES:**

• 3.3.2.5, 3.3.2.9, 3.3.2.10, 3.3.2.13, 3.3.2.15, 3.3.2.19, 3.3.2.60 thorough 3.3.2.66





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## 3.5.1.18.1

- » If you are here because of improper switch actuation, or want to test any control panel switch, continue.
- » Procedure 3.5.1.18.2 will test switche integrity. Procedure 3.5.1.18.3 will test the 68HC11, and support circuits.

## ···· 3.5.1.18.2

- » Switch testing: This test will verify the integrity of an individual switch.
- » Turn rotary switches to lowest settings, compensation polarity switches to their "(-)" settings, and dip switches to their off(Open) positions..
  - The rotary switches are binary encoded. When counter-clockwise, the switch is "OFF". In this setting, there are no activated switch contacts. Each position increases the binary count by a factor of '1'. (example: When counterclockwise and turned two positions clockwise, the binary code would be 0-0-C-0, where O=open & C=closed)
- » Turn power OFF to system.
- » Using illustration 3.5.1.18, find the 'common' for the switch in question. Put the negative (-) black lead of an ohmmeter to this common point.
- » Put the positive (+) red lead of the ohmmeter on the anode side of the diode for the binary switch position in question.
- » Close the switch to test for continuity. If none, try again on the cathode side of the diode. If not evident on the anode side but

was detected at the cathode, the diode is bad... replace it. If the continuity test fails both times, the switch appears bad. If no traces appear broken on the PC board, replace the switch.

» Repeat for each dip switch position and polarity switches, (SW8 and SW7).

## 3.5.1.18.3

- » To understand which switch is activated per a particular microcomputer address, refer to the previous chart.
- » For a detailed explanation of the ports, see the theory of operation in section 4. For testing purposes, we will only be concerned with the signals present.
- » Complete both 3.5.1.18.3.1 and 3.5.1.18.3.2. The waveforms may not be exactly like those illustrated, but they should be similar. Activity appears on these lines at least every 500 ms.....

## 3.5.1.18.3.1

- » 68HC11 port verification: Verify these signals to test the 68HC11. The 68HC11 is possibly defective if any test fails.
  - STRB port test: Connect a scope to the STRB port line, U1 pin 28, the waveform should resemble the illustration, ref. block 3.
  - PROG port test: Connect a scope to the PROG port line PB5, U1 pin 11, the waveform should resemble the illustration, ref. block 4.
  - I/O address test. Connect a scope to the switch mux. address pins PBO, PB1 or PB2. The waveforms should resemble the illustration, ref. block 5.

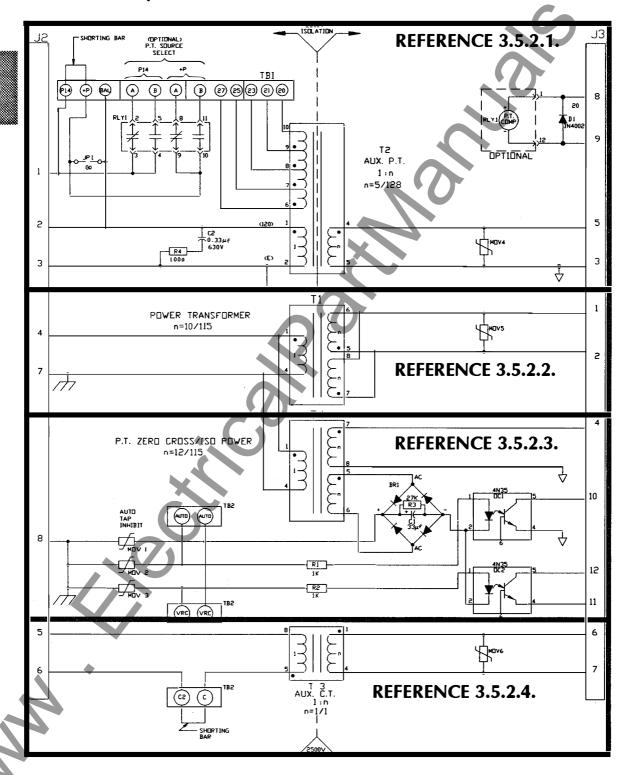
Control inputs to IC 'U17'		Output port	
CHIP SELECT	INPUT SELECTS A2, A1, A0	'U17'enabled	
0	0-0-0	0	
0	0-0-1	1	
0	0-1-0	2	
0	0-1-1	3	
0	1-0-0	4	
0	1-0-1	55	
0	1-1-0	6	
0	1-1-1	7	
1	xxx (don't care)	none	

### 3.5.1.18.3.2

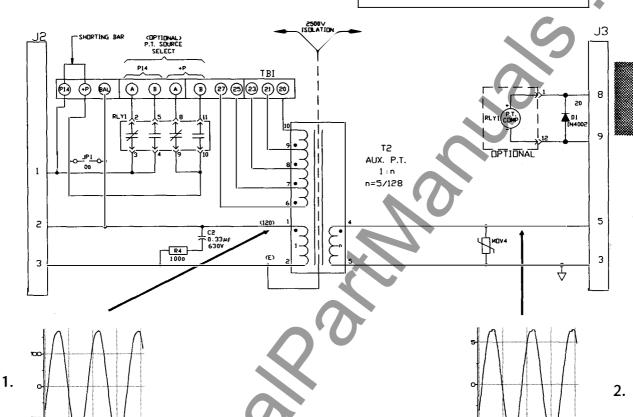
- » Support circuit test: Verify their signals to test operation of switch mux U17.
  - Switch address enable logic to multiplexer. Connect a scope to the switch mux outputs, (Y0-Y7),U17 pin 7, 9, 11, 12, 13, 10, 14, and 15. Waveforms should resemble the illustration.
  - Replace U17 if not seen, and 3.5.1.18.3.1 was successful.



3.5.2 Transformer Board Fault Verified or Suspected



TEST REFERENCES:3.4.2



....

# 3.5.2.1 Sensing Transformer

- » Ensure that voltage on Data/Pak display, or or voltage test terminals is set for 120V rms.
- » Verify on scope or DVM (with ground reference at J2-3) that the incoming AC waveform (reference block 1) appears going into transformer T2 primary on terminal J2-1.
  - YES: Verify that waveform at (reference block 2) (ground reference at J3-3) appears on secondary of transformer.

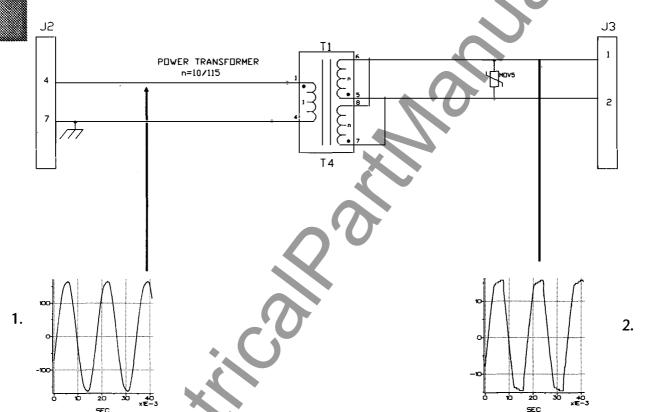
Note that secondary is 5/128 of the primary. If waveform is there, transformer is OK, if not there... replace transformer T2.

- NO: Verify that jumper from +P to P14 is installed. Verify that power is entering transformer board from control panel board.. see section 3.4.1.
- » Verify that when RLY13 on the control panel board activates, the PT compensation relay energizes. If it does not energize when 6 volts appear across the coil, replace Rly13. Verify flyback diode D1 is OK also. If 6 volts does not appear across the diode then replace D1.

» TEST REFERENCES:

• 3.4.1

3



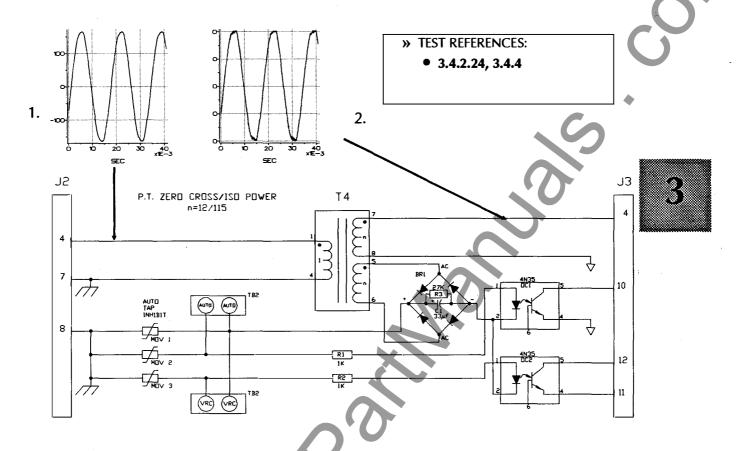
**...** 

## 3.5.2.2 Power Transformer T1

- Ensure that voltage on Data/Pak display or on voltage test terminals is set for 120V rms.
- » Verify on scope or DVM (with ground reference at J2-7) that the incoming AC voltage waveform (reference block 1) appears going into transformer T1 primary on terminal J2-4.
  - YES: Verify that waveform at (reference block 2) (ground reference at J3-2) appears on secondary of transformer.

Note that secondary is 10/115 of the primary. If waveform is there, transformer is OK.

 NO: Verify that contacts are touching on connector. Look for broken solder traces. Verify that power source exists on the control panel board.



## ....

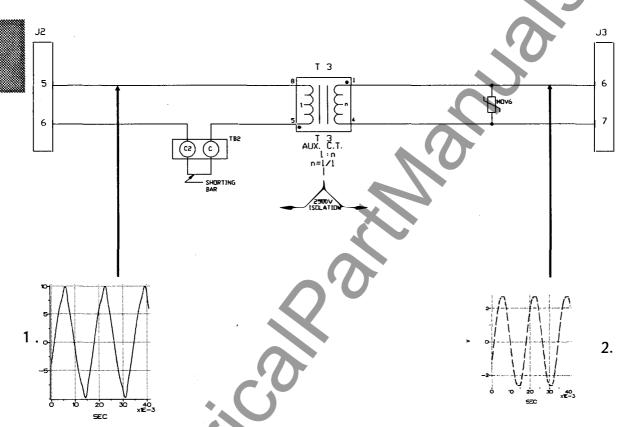
# 3.5.2.3 P.T. Zero Cross Transformer T4

- Ensure that voltage on Data/Pak display, or on voltage test terminals is set for 120V rms
- » Verify on scope or DVM (with ground reference at J2-7) that the incoming AC waveform (reference block 1) appears going into transformer T4 primary on terminal J2-4.
  - YES: Verify that (reference block 2) (ground reference at J3-3) appears on secondary of transformer. Note that secondary is 12/115 of the primary. If waveforms are there, transformer is OK, if not ... replace transformer T4.
  - NO: Verify that contacts are touching on connector. Look for broken solder traces. Verify that power source exists on the front panel board, and on transformer T1.
- Werify that the rectifier for the opto-isolators is operating correctly. If + 20 volts DC does not appear at the (+) output of BR1,

- then verify the raw AC is entering BR1. If it is, yet there is no rectified output, replace BR1... otherwise continue.
- » AUTO-INH opto-isolator verification: Verify that terminal J3, pin 10 is at +6 volt DC potential (reference ground at OC 1, (opto-isolator 1), pin 4). When the TB2 "AUTO-INH" contacts are jumpered, 0 volts should be seen at terminal 10. If it is still at +6 VDC, then replace OC 1.
- » VRC opto-isolator verification: Verify that terminal J3, pin 12 is at a +13 to +18 VDC potential (reference ground at negative end of C2 on control panel board). When the TB2 "VRC" contacts are jumpered, the +13 to +18 volt DC level can be seen at terminal 11 of J3. If not, then replace OC 2.

- **» TEST REFERENCES:** 
  - 3.4.3

3



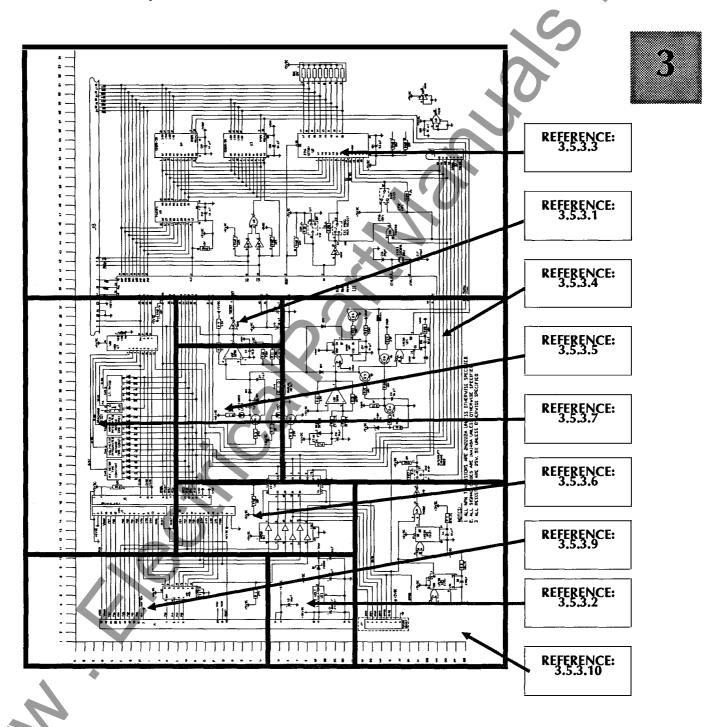
....

## 3.5.2.4 C.T. Transformer T3

- » Ensure that incoming current level is set for 200mA.
- » Verify that the incoming AC waveform (reference block 1) appears going into transformer T3 primary on terminal J2-5.
  - YES: Verify that (reference block 2) waveform appears on secondary of transformer.

Note: The secondary is the same magnitude and the same phase as the primary, (the same magnitude because the transformer ratio is 1 to 1 and the same phase because of the direction of current flow as designated by the dot convention as noted on the drawing.). The secondary voltage in waveform illustrated, (reference block 2). If waveform is there, transformer is OK, if not there... replace transformer T3.

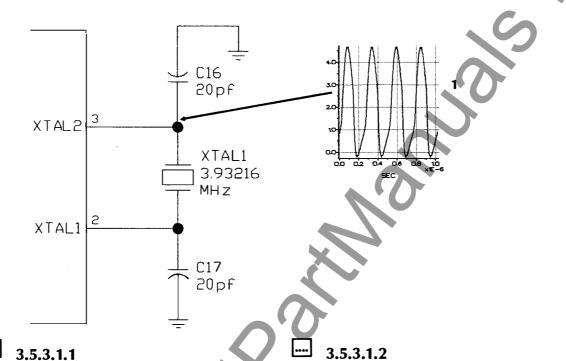
 NO: Verify that contacts are touching on connector. Look for broken solder traces. Verify that power source exists on the front panel board. 3.5.3 Interface Option Board: Fault Verified or Suspected



3.5.3.1 Oscillator

- **» TEST REFERENCES:** 
  - 3.3.2.52

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- » Connect a scope with a low capacitance probe to U1 pin 3 (reference block 1) (ground reference at negative end of capacitor C2). Does the clock frequency appear? (clock period is approximately 254 ns.)
  - YES: If the crystal frequency is displayed on the scope, then this requirement is met. If you were directed here from section 3.3, or 3.4, then return to next item in current checklist
  - NO: If clock frequency does not exist, go to 3.5.3.1.2

- » The microcomputer (U1) should have a +5 volt logic level provided on pin 40. If this is not the case, go to 3.5.3.2.
- >> Turn off the system. Put an ohmmeter across the crystal to ensure there is no short.
- » Verify that the crystal (XTAL1), C16, and C17 are properly soldered and have continuity.
- » Re-verify 3.5.3.1.1. If no frequency yet appears, go to 3.5.3.1.3.

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3.5.3.2.3

» Replace XTAL1. Re-verify 3.5.3.1.1. After replacement, verify that section 3.5.3.1 is satisfied. If not, replace microcomputer. » TEST REFERENCES: 3.5.3.2 Power Supply • 3.3.2.52 -+6VDC C3 10 μ f J1 +16 V DC +5VDC 12 5 VOLT REGULATOR 13 U13 - C4 2200μf 20μf V(MJN.) 17 2 10 SEC 2.0 ×E−6 1000 200



### 3.5.3.2.1

- » Connect a scope or DVM to reference block 4 (ground reference at negative end of C2). There should be a 5 volt reference (minus the diode D1 drop). Is logic level present?
  - YES: Verify also that voltage level exists at reference block 3 waveform. If it is not present, check that connector J1 is tight. Go to 3.5.1.8. If both reference blocks 3 and 4 exist, then verification is complete.
  - NO: If voltage does NOT exist, go to 3.5.3.2.2



### 3.5.3.2.2

- » Observe the input to U13 (pin 1) (reference block 1). Is there a 13 to 18 VDC level present?
  - YES: Go to 3.5.3.2.3
  - NO: The voltage must enter here from the control panel board. Do not continue until this is confirmed.

## ....

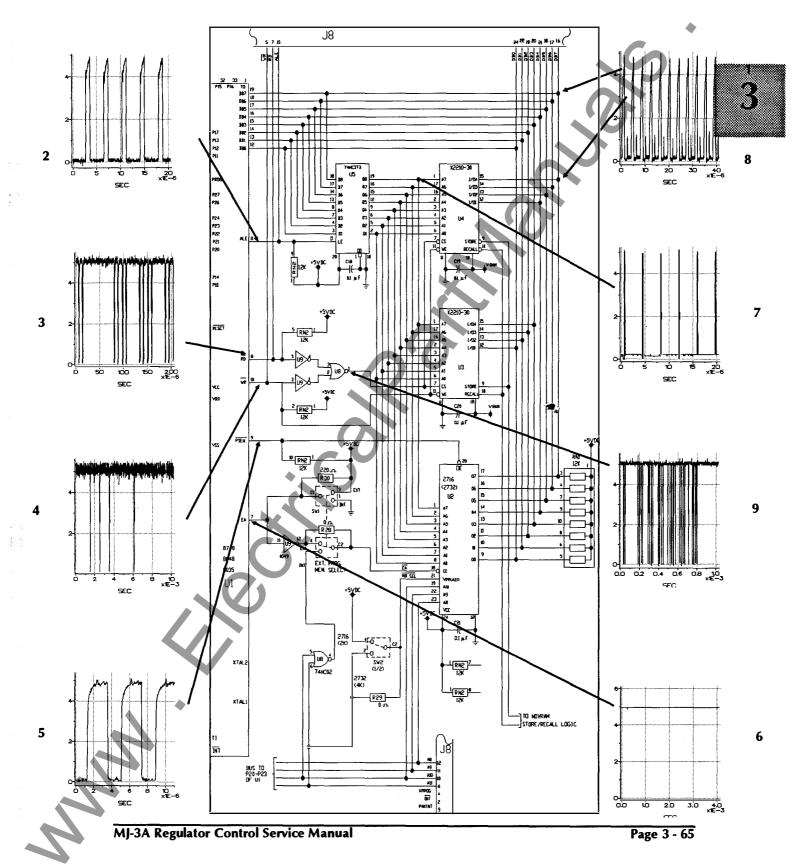
### 3.5.3.2.3

- » IC U13 appears defective, replace it. If there are any signs of damage to any filter capacitors C1, C2 or C3, then replace them as well. Ensure that C2 and C3 are inserted correctly, as they are polarity sensitive.
- » Verify that voltage waveform appears at reference block 2. If it appeared here, but not at reference block 4, then replace diode D1.





3.5.3.3 Microcomputer Memory Management



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3.5.3.3.1

» For a detailed explanation of 68HC11 ports, see section 4 Theory of operation. It is important that waveforms are similiar to those illustrated. Section 3.5.3.3.2 will test the 68HC11 ports and section 3.5.3.3.3 the associated circuitry.

3.5.3.3.2

- » Ground scope or DVM to TPG.
- » 68HC11 port test: Check signals to ensure proper 68HC11 operation. Replace 68HC11 if input voltage and clock references are good, yet fails the following tests.
  - BUS lines DB0 thru DB7 are both address and data lines, and forms a synchronous bi-directional read/write port. Waveforms should be similiar to ref. block 1.
  - ALE (address latch enable) port test: This signal occurs once each cycle. The negative edge strobes addresses into external memory. Connect scope to U1 pin 11, the wave form should resemble, ref. block 2.
  - RD port test: This output strobe is activated during a BUS read. When low, it is used as a strobe to external data memory. Connect a scope to U1 pin 8. The waveform should resemble, ref. block 3.
  - WR port test: This output strobe is activated during a BUS write. When low, it is used as a write strobe to external data memory. Connect a scope to U1pin 10. The waveform should resemble, ref. block 4.
  - PSEN port test: This active low output occurs during a fetch to external program memory. Connect scope to U1 pin 10. The waveform should resemble, ref. block 5.
  - FA port test: Forces program memory fetches to reference external memory. This active high input SHOULD ALWAYS BE HIGH. Connect scope to U1 pin 10. Verify the waveform you see to that of the illustration, ref. block 6.

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3.5.3.3.3

» 68HC11 memory support test:

NOTE: Do not proceed with these tests until section 3.5.3.3.2 is verified.

- » To test the support circuitry, it is necessary to have the correct 68HC11 output signals. This section assumes they are correct.
- » Observe U5 pins lines 01-08. These address both data and program memory. When clocked by ALE, and should resemble ref. block 7. If not, verify power supply to IC U5. ALE clock should have been verified in 3.5.3.3.2. If no signals appear here, but do appear on inputs, replace U5.
- » Monitor U4 pin 15. This outputs data from memory to the 68HC11. If the line appears "dead", verify inputs to U2, U3, and U4. Verify that the CS signal is recieved. If above conditions are met, but with no output on the data lines... replace appropriate IC. (U2, U3 or U4) Maximum input should be +5 volts. If not, verify that resistor network RN1 is properly installed. Replace if 5 volts cannot be attained.
- » The EA line was verified above to be in a continually high state. Thus, the output of U9, pin 12 should be low... and force the chip enable (CE) of U2, pin 18 low. Verify this is so.
- » The RD and WR lines are connected to a pair of inverters and a NOR gate. When the output of the NOR gate (U8, pin 1) is low a read or write occurs. Verify that the output of U8 pin 1 resembles ref. block 9. If not, then go to the inputs of U8 to verify where signal is blocked. Replace either U8 or U9 if signal is blocked.

» Test References: 3.5.3.4 Power Monitor Circuits • 3.3.2.59 +5<u>√</u>⊅C D22 D8818 R 14 27.4K.1% U12 3290 550K R19 +5<u>√</u>DC \_αίμf D53 100 -14538 U14 ERAM RECALI TO NOVRAM

MJ-3A Regulator Control Service Manual

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### 3.5.3.4.1

- » Under normal operating conditions, are the areas pointed to by reference block 4 at a logic high as shown?
  - YES: There are no apparent problems with the logic, but due to the fact that the circuit is not activated until voltage is ramped up or down, a problem could be hidden. If Data/Pak circuit "drag hands" behavior appears abnormal, then continue with procedure
  - NO: Go to 3.5.3.4.2



### 3.5.3.4.2

- » Comparator input pins monitor the 5 volt logic reference and a derived reference of roughly 8 volts (as illustrated by reference block 2). If about 8 volts is not observed, then verify components R13, R14, R15, and D22. When the supply voltage is lost, the 16 volt supply ramps downward while the 5 volt supply remains constant, at least for some milliseconds. When the input reference on U12, pin 5, is less than 5 volts, then the output pin #7 will be low. Does this happen?
  - YES: Go to 3.5.3.4.3
  - NO: If input references to U12 are there, but output pin fails to go low during above scenario, replace U12.



### 3.5.3.4.3

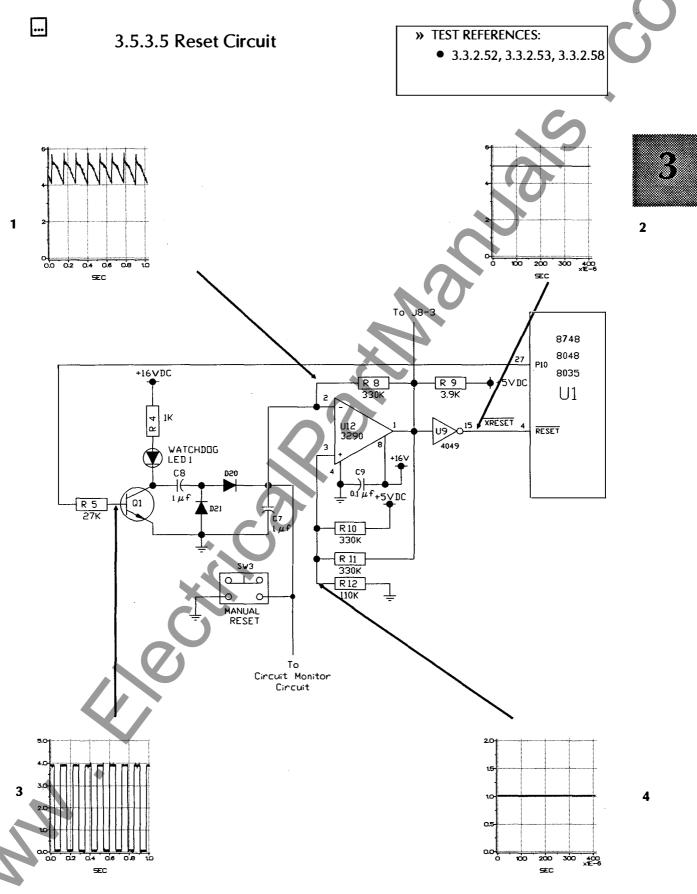
- » Does the ERAM STORE signal, U14 (pin 9), go low when output pin 7 from U12 is low?
  - YES: Go to 3.5.3.4.4
  - NO: Replace U14.



### 3.5.3.4.4

- Transistor Q4 is biased on when there is greater than .7 volts at the base. This only happens if zener diode D23 conducts, which requires 3.9 volts to do so. When power is first applied to the system, the 5 volt supply ramps to about 4.6 volts when Q4 first conducts. From that point, Q4 remains in conduction. If reference block 3 is not a logic low, then look at the base voltage of Q4. If it is greater than .7 volts, then replace Q4. If it is not greater than .7 volts, then ensure that D23 has a 3.9 volt drop across it. If it doesn't then verify resistors R26 and R16. If they are OK, replace
- » Verify that resistors R17 thru R24 are OK.
- When transistor Q4 is out of conduction (during initial power-up), transistors Q3 and Q5 are conducting, which causes the ERAM RECALL to go high, and pulse extended via U14. If either of these lines fail to go to ground upon power-up, then replace Q3 or Q5.





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### 3.5.3.5.1

- » The microcomputer (U1) is in a non-reset state when operating normally. Accordingly, pin 4 of U1 (reference block 2) should be high (5 VDC), as illustrated. Is this true?
  - YES: If the watchdog is also flashing, (on the interface option board), then the reset circuit appears to be operating OK. Otherwise go to 3.5.3.5.2.
  - NO: Go to 3.5.3.5.2



### 3.5.3.5.2

- » The input of U12, pin 3 should be about 1 volt as illustrated by reference block 4. Verify this is so.
  - YES: Go to 3.5.3.5.3
  - NO: If the voltage measured here is incorrect, verify resistors R10, R11, and R12 are correct values (color bands.)



### 3.5.3.5.3

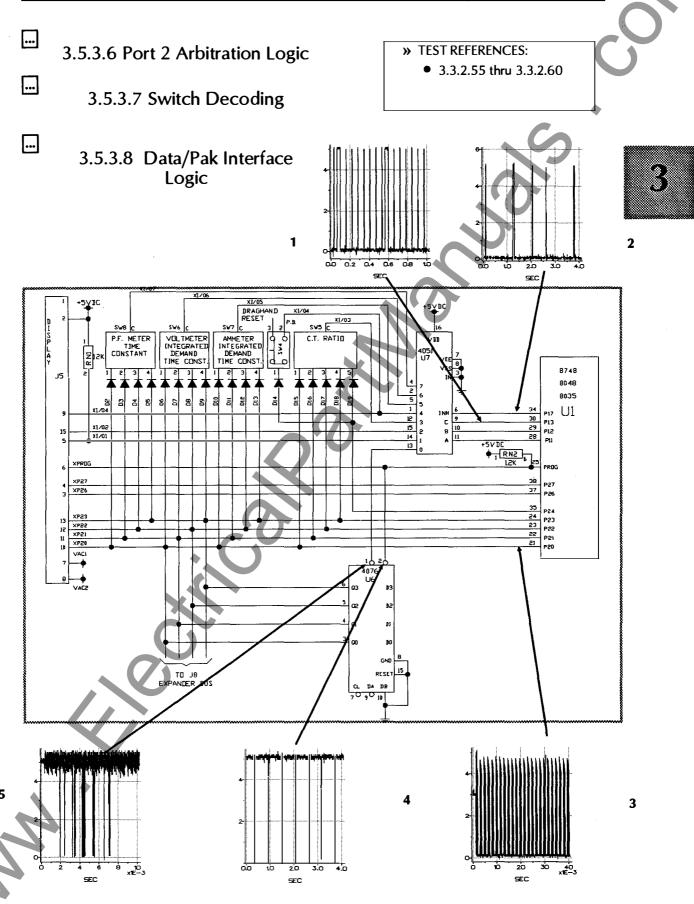
- » Verify waveform on U12 input pin 2 is per reference block 1.
  - YES: Signals into U12 are correct. If output signal (logic low) appears at U12, pin 1... then reset circuit appears OK. If no signal is observed at U12, pin 1... then replace U12. If U12, pin 1 is logic low, but the reset input to U1 is not at +5 volts (reference block 1), then replace U9.
  - NO: Verify that pressing the reset button SW3 causes this line to go low. If not do continuity check on SW3 and replace if necessary. Go to 3.5.3.5.4



### 3.5.3.5.4

- » Place jumper across LED1 (short it out). Does reference block 1appear as illustrated?
  - YES: Replace watchdog LED.
  - NO: Verify that reference block 3 appears at the base of Q1. If not, replace R5 or U1. If it does appear, check the collector of Q1. If no evident waveform is apparent, then replace Q1, if waveform is there, then verify components D20, D21, and C7.





## 3.5.3.6.1

- » The portion of circuitry contained in this section is utilized in many circuits. The specific portions of the port 2 arbitration logic which is used by a specific circuit will be tested in that specific circuit test procedure.
- » For a quick test of the logic for these circuits, verify the waveforms as illustrated.
- » For a through test of this circuitry, refer to the following circuits:
  - Switch Decoding (3.5.3.7)
  - Control Panel Bus Arbitration (3.5.3.9)
  - Control Panel Communications Interface (3.5.3.10)
  - Data/Pak Option Board (3.5.4)

## 3.5.3.7.1

### » INTERFACE BOARD SWITCH DE-CODING

- » If you were led here due to the lack of proper switch actuation, or want to verify the integrity of any control panel switch, the following procedure will help to verify it.
- » Procedure 3.5.3.7.2 will verify the integrity of the switches, whereas procedure 3.5.3.7.3 will verify the microcomputer operation, and support circuits.

## 3.5.3.7.2

- » This circuit uses the same type decoder (U7) as used on the control panel board. For a logic table of the switches it selects, refer to section 3.5.1.18.
- » Switch continuity testing: This test will verify the integrity of an individual switch.
  - Put all switches to their "open" positions.
  - Turn power OFF to system.
  - Looking at the illustration 3.5.3.7, determine the 'common' for the questionable switch. Put the negative (-) black lead of an ohumeter at this common point on the appropriate pin of U7.
  - Put the positive (+) red lead of the ohmmeter on the anode side of the diode for the binary switch position in question.
  - Close the switch to test for continuity. If it is absent, try again on the cathode side of the diode. If continuity was lacking on the anode side but seen on the cathode, then the diode is bad... replace it. If the continu-

ity test fails each of the two tests, then the switch appears bad. If no traces appear broken on the PC board, replace the switch.

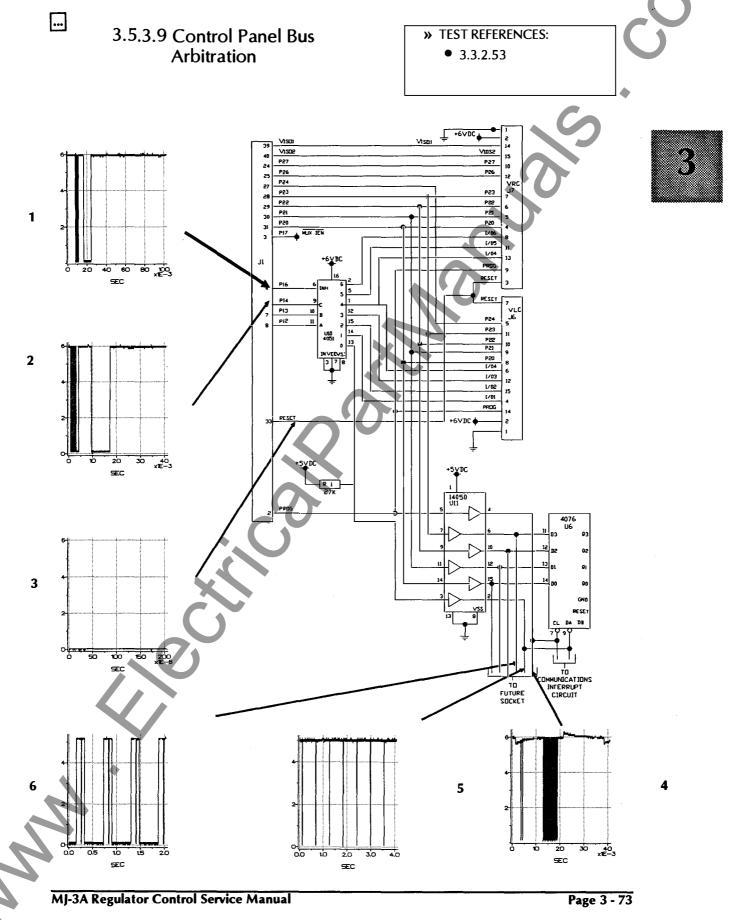
## **....** 3.5.3.7.3

- » Support circuit test:
  - (Refer to first note under 3.5.3.7.2 for reference to decoder IC)
  - Switch address enable logic to multiplexer test. Connect a scope to the mux input, (i.e. U7 pin 9). Verify the waveform you see to that of the illustration in reference block 1 waveform.
  - If no activity appears on U1 port lines, then go to sections 3.5.3.1 and 3.5.3.2.
  - Verify that U7 is enabled (reference block 1), and that the mux output is activated (any outputs of U7). Replace U7 if inputs are detected, but there are no outputs enabled.

### 3.5.3.8.1

- » A detailed test procedure for the Data/Pak is conducted in section 3.5.4. The specific areas of the interface board which are required for Data/Pak operation will be tested in that section.
- » For a detailed explanation of the Data/Pak operation, refer to section 4.



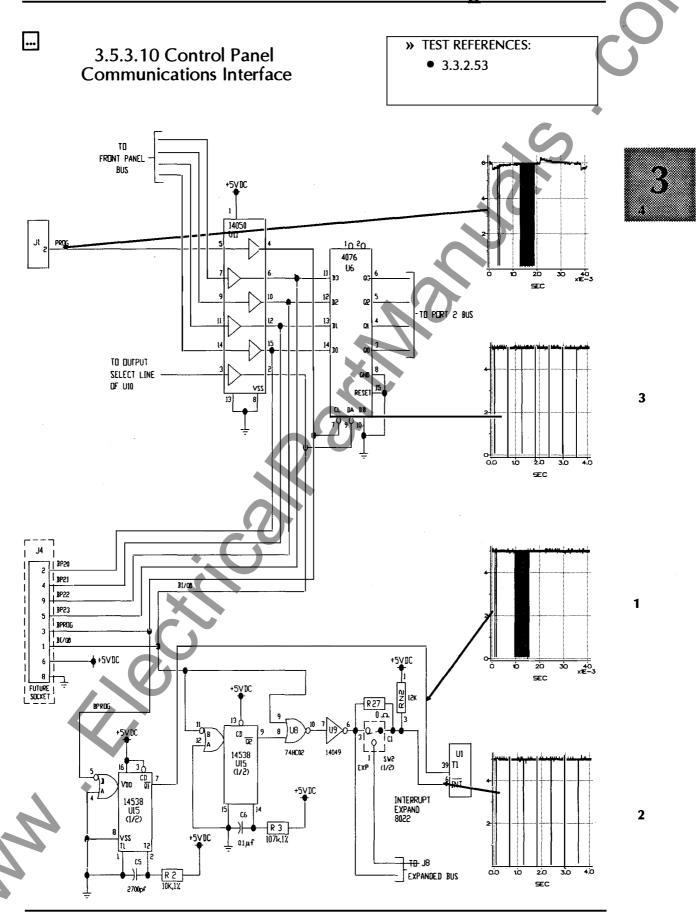




### 3.5.3.9.1

- » The portion of circuitry contained in this section is utilized in many circuits. The specific portions of the control panel arbitration logic which is used by a specific circuit will be tested in that specific circuit test procedure.
- » For a quick test of the logic for these circuits, verify the waveforms as illustrated.
- » For a through test of this circuitry, refer to the following circuits:
  - Control Panel Communications Interface (3.5.3.10)
  - VLC (Voltage Limit Control) (3.5.5)
  - VRC (Voltage Reduction Control) (3.5.6)





MJ-3A Regulator Control Service Manual



### 3.5.3.10.1

- When the control panel communicates with the interface board, it first sends a request for a data buffer transfer on U6 (pin9). This waveform is illustrated in reference block 3. Can you see its presence on flip-flop U6?
  - **YES:** Go to 3.5.3.4.2
  - NO: If you do not see it at U6, but you see it at U11, pin 3.... then replace U11. If you see it at U11, but you don't see it at U10 (pin 13) [on page 3-86], then verify that reference block 2 on same page exists on U10 inputs 9,10 and 11. Also verify waveform on U10 (pin6) (reference block 1). If seen at only U10 inputs, then replace U10. If not, then verify good connection with control panel board.



## .... 3.5.3.10.2

- » The same request line in 3.5.3.4.1 is also routed to the 8035 on T1 (pin 39). Pulse extended via U15, the conditioned waveform is per reference block 1. Is this waveform evident?
  - YES:Go to 3.5.4.3
  - NO:Replace U15. Go back to 3.5.3.10.1



#### 3.5.3.10.3

- » When actual data is sent from the control panel board, the PROG line is pulsed (J1 pin 2), per reference block 4 waveform. Is it there?
  - **YES:**Go to 3.5.3.10.4
  - NO:If seen at input pin U11, pin 5, then replace U11. Otherwise verify that connector J2 is tight and providing the signal from control panel board.



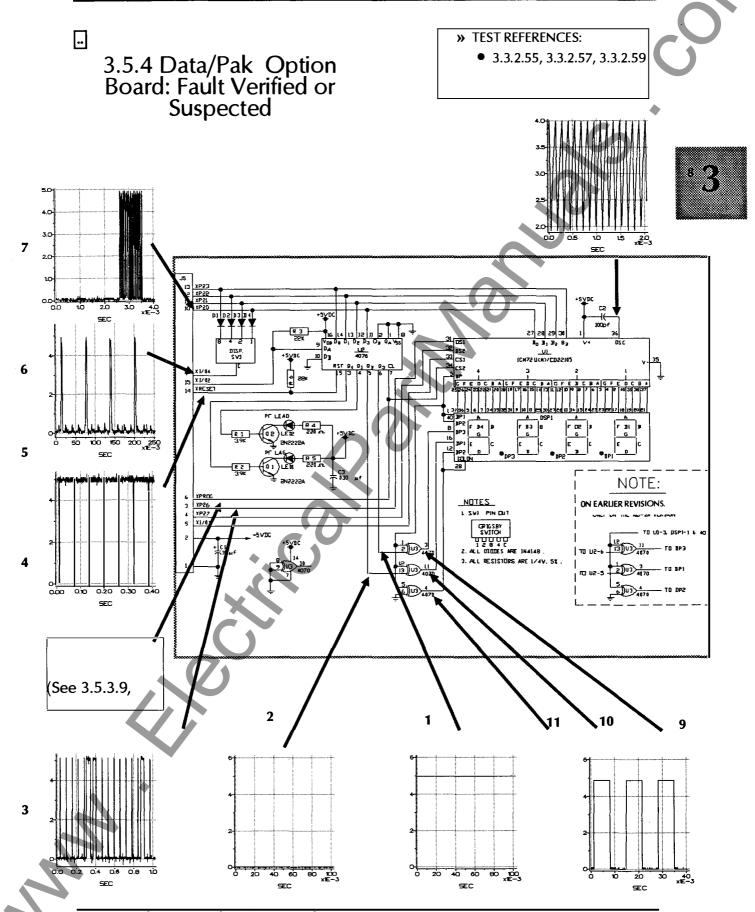
### 3.5.3.10.4

- » Look for reference block 2 waveform at the input to U1 (pin 6). This ensures that the 8035 will communicate with the control panel board for the duration of the buffer transfer. Is this waveform seen?
  - YES: Go to 3.5.3.10.5
  - NO:Check existence of waveform at nodes between U1 and the monostable multivibrator U15. Replace the component where the waveform is viewed as an input, but not an output. Replace either R27, inverter U9, or U15.



### 3.5.3.10.5

- » VERIFICATION OF COMMUNICATIONS LED"XMIT LED2". (not shown on 3.5.3.10 illustration)
- » Is the LED2 flashing at a 2 Hz rate?
  - YES: Verification of communication circuit complete.
  - NO: Monitor microcomputer U1 output (pin P14). Does a 1/2 second square wave alternating between ground and 5 volts DC exist?
    - YES: Monitor collector of transistor Q2. If it is a steady state 5 volts, then either R6 or Q2 is defective. If the square wave appears here too, then either LED2 or R7 is defective.
    - NO: If sections 3.5.10.1 thru 3.5.10.4 have been verified, yet there is no output on P14, then replace U1.



## ....

3.5.4.1

- » Verification data transmission to Data/Pak
- » Data is directed to the Data/Pak from the interface board via J5 pins 10 thru 13 (P20 thru P23). Monitor each of these four lines to verify port activity. reference block 7 provides a sample snapshot of activity. Do you verify this?
  - YES: Verify that the PROG line (reference block 4) is actively selecting the Data/Pak for data transmission. Monitor also address and chip select lines (J5 connector, pins 3,4,5) for activity similar to reference block 3. Pin 15 should have similar activity to indicate a proper data enable to U2. If so, transmission to Data/Pak appears OK, if not then see note below.
  - NO: Check these same port lines on the same pins as above, but look at the interface board instead. Verify that the connector is tight. If data transmission fails to materialize, refer to section 3.5.3.6.



3.5.4.2

#### » Verification of LED operation

- » Complete 3.5.4.1 before proceeding with this section. Test LEDs by putting the switch into the "PF" position. In this position, one of the lights will be on, the other off. (The exact sequence depends on the power flow of the unit under test.) The easiest way to test the LEDs is to verify that one LED is lit, then change to the opposite power factor and verify that the opposite LED state is now true. Does each light perform as described?
  - YES: LED test operation complete.
  - NO: Did at least one LED illuminate?
    - **YES:** Go to 3.5.4.2.1
    - NO: IC U2 may be defective if neither LED will light. If **power factor** is selected, and LCD is displaying the power factor, yet neither pin 4 or 5 of U2 is high, then replace U2. (Input to transistors Q1 and Q2 are high when respective transistor is active.) If replacement of IC does not solve problem, then proceed to 3.5.4.2.1

### ° 3.5.4.2.1

If one of the ports is high, check the collector of the appropriate transistor. If it is high, then transistor suspected bad, if low..then suspected LED or series resistor defective.

## ••••

3.5.4.3

- » Verification of rotary switch operation
- » Monitor reference block 6 waveform to verify that the switch is being selected by the interface board.
- » Monitor port 2 lines on each cathode (banded ends) of the diodes D1 thru D4). If activity similar to reference block 7 does NOT appear, diode is suspected to be defective.
- » Does the turning of the rotary switch to each position cause different LCD messages to appear?
  - YES:(to all above checks) Switch is probably OK. If you wish a more detailed test, refer to section below.
  - NO: Monitor reference block 6 to verify that the switch is being selected by the interface board. If waveform is present, switch may be defective. If incorrect readings occur, verify that diodes D1 thru D4 are OK. Also...Verify the switch in section 3.5.3.7

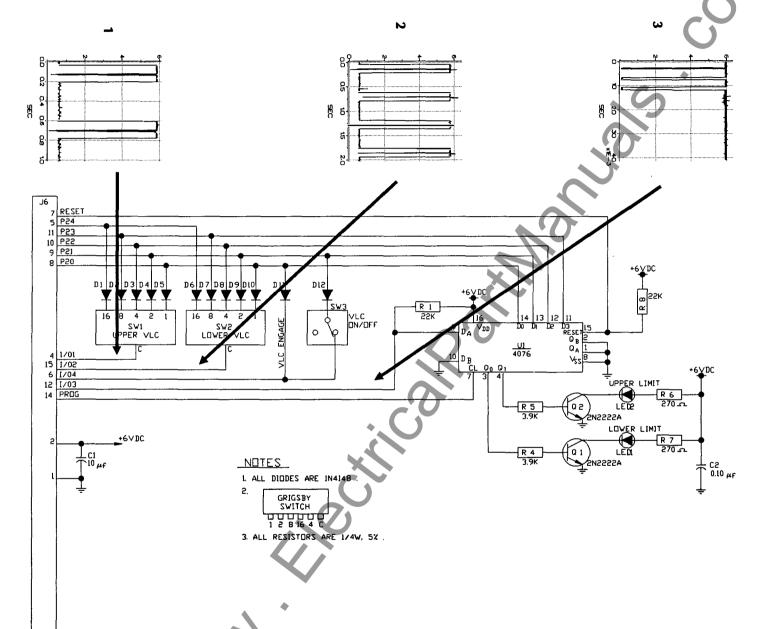


3.5.4.4

- » Verification of LCD driver and LCD operation
- » Put rotary switch into "volts" operation.
- » Verify reference block 8 waveform exists to determine that the LCD driver IC is functioning properly (verifing internal oscillator operation). Does waveform exist.
  - YES: Verify that waveforms on reference blocks 9, 10, and 11 appear at points shown and also on the A thru G segment drivers inputs of the LCD.
  - Check that the waveforms on reference blocks 3 and 4 exist to ensure that the LCD is being properly addressed. If not, go to section 3.5.3.6.
  - Verify that waveforms at reference blocks 1 and 2 are true for the DP1, DP2, and DP3 inputs in the "volts" setting. If these signals are seen but reference blocks 9, 10, and 11 are not, then replace U3. If all the drive signals are present to the LCD, but it does not light, replace the LCD.
  - NO: If it is not, first verify that the chip is receiving proper voltage to pins 1 and 35. If so, replace U1. After replacement, go back to 3.5.4.4



3.5.5 VLC (Voltage Limit Control) Option Fault Verified or Suspected





10.4

## ••••

### 3.5.5.1

### » Verification data transmission to VLC

- » Data is directed to the VLC from the interface board via J6 pin 5 and 8 thru 11 (P20 thru P24). Monitor each of these four lines to verify port activity. reference block 7 (from section 3.5.4) provides a sample snapshot of activity. Do you verify this?
  - YES: Verify that the PROG line (reference block 4) in 3.5.3.10) is actively selecting the VLC for data transmission, and that reference block 3 waveform exists, to enable the data going into U1.
  - NO: Check these same port lines on the same pins as above, but look at the interface board instead. Verify that the connector is tight. If data transmission fails to materialize, refer to section 3.5.3.6.



### 3.5.5.2

### » Verification of LED operation

- » Complete 3.5.5.1 before proceeding with this section, as it is assumed that VLC data transmission has been verified. LEDs can be tested by putting the rotary switch into a voltage level setting higher than the actual measured voltage (lower limit LED active), or lower than the actual measured voltage (upper limit LED active). Doing so will ensure that one of the lights will be on, the other off. The easiest way to test the LEDs is to verify that one LED is lit, then change to the voltage condition and verify that the opposite LED state is now true. Does each light perform as described?
  - YES: Verification of LED operation complete.
  - NO: Did at least one LED illuminate?
    - YES: Go to 3.5.5.2.1
    - NO: IC U2 may be defective if neither LED will light. (Input to transistors Q1 and Q2 are high when respective transistor is active.) If replacement of IC does not solve problem, then proceed to 3.5.5.2.1

### ° 3.5.5.2.1

If one of the ports is high, check the collector of the appropriate transistor. If it is high, then transistor suspected bad, if low..then suspected LED or series resistor defective.

- » See discussion of rotary switch binary encoding logic in section 3.5.1.18.
- » Monitor reference block 1 to verify that the Upper VLC switch is being selected by the interface board, do the same for reference block 2 to verify the Lower VLC switch.
- » Monitor port 2 lines (J5 pins 8 thru 11) as in 3.5.5.1, but this time on each cathode (banded ends) of the diodes D1 thru D10). If activity similar to waveform at reference block 7 (from section 3.5.4) does NOT appear, diode is suspected to be defective.
- » Does the turning of the rotary switch to each position cause different VLC activation points to occur?
  - YES:(to all above checks) Switch is probably OK. If you wish a more detailed test, refer to section below.
  - NO: Monitor reference block 6 on connector of interface board to verify that the switch is being selected by the interface board. If waveform is present, switch may be defective. If incorrect readings occur, verify that diodes D1 thru D4 are OK. Also...Verify the switch in section 3.5.3.7

## ....

### 3.5.5.4

#### » Verification of toggle switch operation

Follow same procedure as in 3.5.5.3.
 Verify activity on J6, pin 6 for toggle switch monitor.

## ••••

### 3.5.5.5

### » Verification of VLC being actively selected

 Ensure diode D11 is OK, otherwise the control panel board will not recognize the existence of the VLC option board being installed.



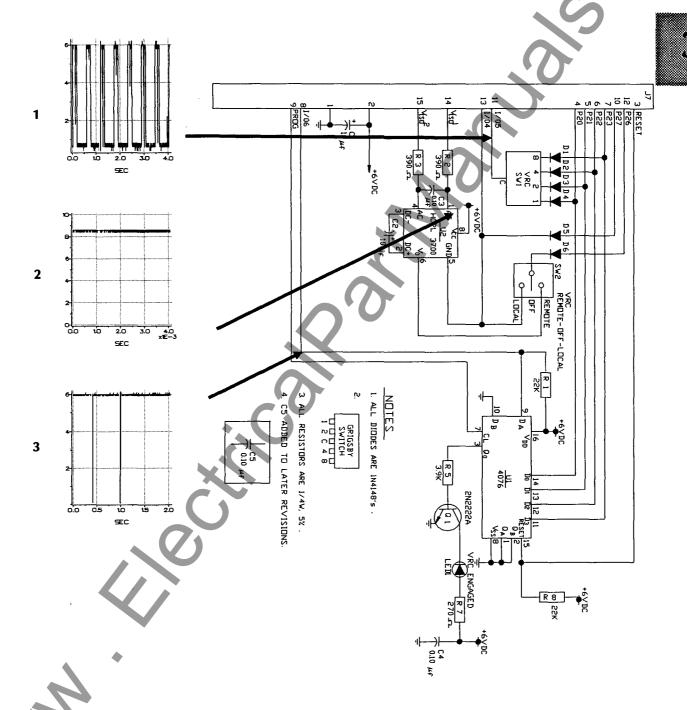
#### 3.5.5.3

» Verification of rotary switch operation

3.5.6 VRC (Voltage Reduction Control) Option Fault Verified or Suspected

» TEST REFERENCES:

• 3.3.2.71, 3.3.2.72, 3.3.2.73



## 3 - Troubleshooting Procedures

## 3.5.6.1

#### » Verification data transmission to VRC

- » Data is directed to the VRC from the interface board via J7 pins 4 thru 7 (P20 thru P23). Monitor each of these four lines to verify port activity. Reference block 7 (from section 3.5.4) provides a sample snapshot of activity. Do you verify this?
  - YES: Verify that the PROG line [J7, pin 9] (reference block 4 in 3.5.3.10) is actively selecting the VRC for data transmission, and that reference block 3 exists, to enable the data going into U1.
  - NO: Check these same port lines on the same pins as above, but look at the interface board instead. Verify that the connector is tight. If data transmission fails to materialize, refer to section 3.5.3.6.

## ....

#### 3.5.6.2

#### » Verification of LED operation

- » Complete 3.5.6.1 before proceeding with this section, as it is assumed that VRC data transmission has been verified. LED can be tested by putting the toggle switch in a "local" setting... doing so will ensure that the light will be on. Is it?
  - YES: Verification of LED operation complete.
  - NO: IC U1 may be defective if LED will not light. (Input to transistor Q1 is high when LED is active.) If replacement of IC does not solve problem, then proceed to 3.5.6.2.1
    - ° 3.5.6.2.1

If ports is high, check the collector of the transistor. If it is high, then transistor suspected bad, if low..then suspected LED or series resistor defective.

## ••••

#### 3.5.6.3

#### » Verification of rotary switch operation

- » See discussion of rotary switch binary encoding logic in section 3.5.1.18.
- » Monitor 7 pin 11, ref. block 1 to verify that the VRC switch is selected by the interface board.
- Monitor port 2 lines (J7 pins 4 thru 7) as in 3.5.6.1, but this time on each cathode (banded ends) of the diodes D1 thru D4). If activity similar to reference block 7 (from

- section 3.5.4) does NOT appear, diode is suspected to be defective.
- » Does the turning of the rotary switch to each position cause different control panel LED band conditions to occur? (When VRC is enabled with a high percentage dialed in, while the control panel has a low bandwidth setting and an in-band condition, the VRC activation will immediately upset the in-band condition.)
  - YES:(to all above checks) Switch is probably OK. For more detailed testing, refer to section below.
  - NO: Monitor J7 11 (reference block 1) on connector of interface board to verify that the switch is being selected by the interface board. If waveform is present, switch may be defective. If incorrect readings occur, verify that diodes D1 thru D4 are OK. Also...Verify the switch in section 3.5.3.7

#### 3.5.6.4

#### » Verification of toggle switch operation

 Put VRC switch in local position. Verify continuity from U2, pin 5 to the anode of D6. If switch closure does not provide continuity, check diode and toggle switch for faults. After test is made, check continuity of toggle in the remote position. (verification of output on U2, pin 6 will be made in 3.5.6.6)

## ....

#### 3.5.6.5

#### » Verification of VRC being actively selected

 Ensure diode D5 is OK, if bad the control panel board will not recognize the VRC option board.

### ....

#### 3.5.6.6

#### » Verification of VRC being actively selected remotely

 Short VRC terminals on the transformer board. If waveform at U2 pin 4, reference block 2 is present, and VRC will not activate (LED illuminates) in "remote" position, yet it did in "local" position, replace U2. If ref. block 2 is not a steady-state high when VRC contacts are shorted, then go to 3.5.2.3.



4

SECTION 4: MJ-3A: Detailed Theory of Operation

#### Theory of Operation -

Each major topic will be discussed using the same approach. It will start with a "TOPIC" OVERVIEW by first referencing the pages for circuit board layouts (Appendix A) and block diagrams (Appendix B). A review of the block diagram's logical structure will present the basics of the modules operation.

This will be followed by a more comprehensive analysis of the circuitry that comprises that particular module. For this detailed analysis, the appropriate schematic in Appendix C will be referenced. Accordingly, if you wish to learn only a functional overview, the "OVERVIEW" portion of each major heading is all you need to read, however an extensive component level coverage requires reading the "DETAILS" portion as well.

Every attempt has been made to structure this discussion in a manner that allows each section presented to "flow" directly into the next one. As a result, it was necessary to divide the discussion of the control panel PC board into "electrical" and "electronic" sections, and insert the description of the transformer board between them. The schematics in Appendix C are consistent with this approach, and in doing so provide for a clearer understanding of the system. Other than this one exception, everything else will be discussed on a board by board approach.

This "theory of operation" section is comprised of the following sections:

- MJ-3A System Top Level
- Electrical I/O (encompasses Control Panel Board [electrical section], and the transformer board)
- Control Panel PC Board (remaining electronic portion)
- Interface PC Board Option
- Data/Pak Option Module
- Voltage Limit Control (VLC) Option Module
- Voltage Reduction Control (VRC) Option Module

## 4.1 MJ-3A System - Top Leve

## 4.1.1 Top Level - Overview

#### Circuit Board Layout:

Appendix A, page REF-2

#### Block Diagram:

Appendix B, page REF-10

The MJ-3A regulator control in its minimum configuration, consists of the control panel board, transformer board, and PDS connector (See Appendix B, pages REF-10,11).

The heart of the system is the control panel board which directly or indirectly connects to everything else. It includes an A/D input section to convert analog system information from the instrument transformers into a digital code which can be processed by the microcomputer. Digital information is then used to calculate voltage, current, and power factor. Calculated values are compared to the reference values which have been selected by operator settings on the control panel. Results of the comparison form the basis for output commands of the control.

Optionally, the interface board can be added which then permits attachment of the Data/Pak Display Option, Voltage Limit Control Option (VLC), and Voltage Reduction Control Option (VRC). Any or all of the three options can be added, but as shown in the top level and interconnection block diagrams (page REF-10 and REF-11), the interface PC board must first be added.

## 4.1.2 Top Level - Detailed

(A detailed discussion of the MJ-3A regulator control at the top level will be limited to the mention of a more detailed block diagram of the entire system, this one showing the major interconnect lines [see Appendix B, page 11]. For further details, refer to the appropriate module which follows.)

**...** 

## 4.2 Electrical I/O

## 4.2.1 Electrical I/O - Overview

#### | Circuit Board Layout:

- Control Panel Board Appendix A, page REF-3
- Transformer Board Appendix A, page REF-4

#### Block Diagrams:

- Overview Appendix B, page REF-11
- Control Panel Board Appendix B, page RFF-12
- Transformer Board Appendix B, page REF-13

Because devices at different physical locations comprise this particular discussion, block diagram page REF-11 is referenced. The PDS connector serves as the MJ-3A input/output connection with the regulator that it is controlling. It is here that all interconnections to voltage and current transformers are made. It is also via the PDS that the regulator receives the actual tap raise/lower excitation from the controller, and for drag hand reset. The MJ-3A controller likewise receives excitation from the regulator via this connector for "Neutralite" indication and for updating the operations counter.

The transformer board is essentially an extension of the control panel board, and that is how it is described in the discussion. Per REF-11 and REF-12, incoming signals from the PDS connector (via the control Panel PC board) are directed to the transformer board from the voltage and current transformers at the regulator. These signals are applied to the transformer board, then re-directed to the electronic portion of the control panel board. The transformer board provides for proper scaling, selection, and isolation of the incoming voltage and current signals.

## 4.2.2 Electrical I/O - Detailed

#### Schematics:

 Control Panel Board (Electrical Portion) -Appendix C, page REF-20

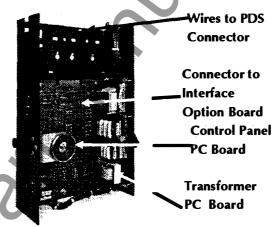


Figure 4-1: MJ-3A Control-Rear View (shown w/o options

Transformer board - App C, REF-21

The electrical I/O section consists of:

- Control Panel Board (Electrical Portion)
- Transformer Board



## 4.2.2.1 Control Panel Board (Electrical Portion)

(Reference Appendix C, page REF-20).

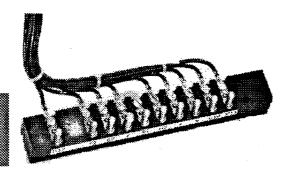


Figure 4-2: PDS Connector

#### 4.2.2.1.1 PDS Connector

The Control Panel Board interfaces with the outside world via the PDS (polarized disconnect switch) and is attached to the control panel board. The PDS attaches to a stationary female section mounted at the regulator. All electrical interfaces from the regulator to the MJ-3A are made via this connector assembly. The electrical connections are (from left to right):

**Terminal 'U12'** - Terminal from contact switch of regulator to indicate that tap changer is in neutral position. This in turn activates the NEUTRALITE on the control panel of the MJ-3A.

**Terminal 'P2'** - Output from potential (voltage) transformer winding. This voltage reference provides the source for the regulating reference signal to the MI-3A if...

- the control panel External / Internal Power switch SW11 is in the "NORMAL" position, AND
- relay RLY13 contact (pins 5 and 4) are closed.

**Terminal 'C2'** - Output from current transformer. This input provides the reference to the MJ-3A for determining the load current and its phase relationship to the voltage input within the power system.

Terminal 'E' - AC voltage common return.

**Terminal 'E1'** - Current transformer return. This point is physically tied to 'E' both by a shorting bar on the PDS connector, as well as a shorting trace on the control panel PCB.

**Terminal 'U2'** - Output from utility (tertiary) winding. This voltage input provides the control panel AC power source and the voltage phase reference for extracting system power factor and power flow information if...

 the control panel External/Internal Power switch SW11 is in the "NORMAL" position.

It will also provide the voltage reference excitation for the potential transformer to the MJ-3A under certain power flow and control panel configurations when...

> relay RLY13 contact (pins 3 and 4) are closed.

**Terminal'**// - To the RAISE motor winding. Voltage to this terminal is either by automatic control, as determined by the MJ-3A regulator, if the control panel transfer switch SW12 is in the AUTO position, or by manual control if the transfer switch SW12 is in the MANUAL position AND the momentary switch SW13 is in the RAISE position.

**Terminal 'K'** - To the LOWER motor winding. Voltage to this terminal is either by automatic control, as determined by the MJ-3A regulator, if the control panel transfer switch SW12 is in the AUTO position, or by manual control if both the transfer switch SW12 is in the MANUAL position AND the momentary switch SW13 is in the LOWER position.

**Terminal 'U10'** - Terminal from contact switch on regulator which closes every other tap change. This signal increments the operations counterlocated on the MJ-3A control panel.

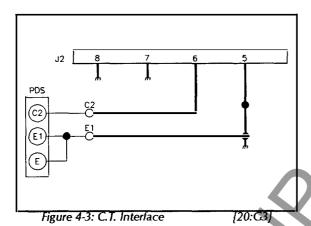
**Terminal 'U11'** - Output signal to reset the position indicator drag hands on the regulator. One drag hand moves only in the raise direction with a pointer and the other only in the lower direction with a pointer. When the MJ-3A control panel "DRAG HANDS RESET" SW14 is pressed, the momentary voltage on contact U11 forces the drag hands to their present tap position setting.

#### 4.2.2.1.2 Individual Circuits

Both the PDS connector and the transformer primaries, from the transformer board, connect directly to the control panel PCB in the high voltage electrical portion (lower section) of the board. Only the low voltage/current secondaries of the transformer board interact directly with the control panel PCB low voltage electronic section, which is electrically isolated from the high voltage electrical portion.

The input current from the current transformer is sent directly to the transformer board via connector J2 (pins 5 and 6). The current is scaled and isolated via a 1:1 isolation transformer T3 on the transformer board. The secondary of the current transformer is then routed to the low voltage portion of the MJ-3A control panel board via J3 (pins 6 and 7). Refer to C.T. Magnitude description in next section for further details.

#### Current Transformer Interface



## Potential & Utility Winding interface

(Refer to figure 4-4.) The Potential Transformer secondary and Utility Winding are interfaced to the control panel board via the PDS connector, terminals P2 and U2 respectively. Fuse F1 & F2 provides protection against P2 to U2 shorts resulting from component failure (i.e. contact welding and/or arcing). The P2 and U2 inputs are surge protected by MOV11 & MOV13 and MOV12 & MOV14 respectively. When the External/Internal power switch SW11 is in the EXT' position, the MJ-3A is powered from the externally applied source on the EXTERNAL SOURCE banana jacks on the MJ-3A control panel. When SW11 is in the NORM position however, the controller will be powered from the U2 input terminal.

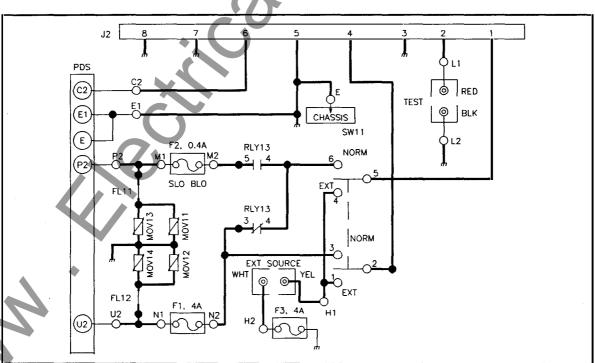


Figure 4-4: PT & Utility Winding Interface [J20:J3]

#### **NEUTRALITE** interface

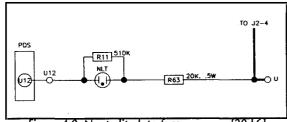


Figure 4-8: Neutralite Interface [20:L6]

This circuit provides a neon light (NLT) which glows when the contact switch of the regulator indicates that the tap changer is in the neutral position. Resistor R63 provides current limiting to the neon light. Resistor R11 ensures the neon lamp will remain off in the presence of high impedance leakage currents that may be present at the U12 terminal.

#### DRAG HANDS reset interface

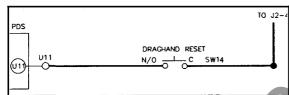


Figure 7 Draghands Reset Interface

When pushbutton SW14 (physically mounted on the control panel board) is pressed, voltage is applied to the U11 terminal, resulting in the resetting of the remote position indicator drag hands.

#### **Operations Counter interface**

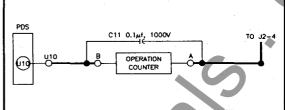


Figure 4-5: Operations Counter Interface [20:07]

Voltage appearing on terminal U10, resulting from the closure of the operations counter contact switch within the regulator, increments the operations counter located on the MJ-3A control panel every other tap change. High frequency voltage spikes are snubbed by capacitor C11 when the counter solenoid de-activates. The operations counter is hardwired to the control panel assembly at points 'A' and 'B' as shown in figure 4-7.

#### Raise / Lower Motor interface

(Refer to figure 4-8.) The transfer switches SW12 and SW13, configure the manner in which the RAISE(J)/LOWER(K) motor windings are activated. When switch SW12 is in the manual position, the RAISE(J)/LOWER(K) motor windings are activated directly by the momentary action of switch SW13 in the 'tapraise'/'taplower' positions. When switch SW12 is in the auto position, the RAISE(J)/LOWER(K) motor windings are controlled by MJ-3A relays RLY12 and RLY14, driven by the microcomputer. If

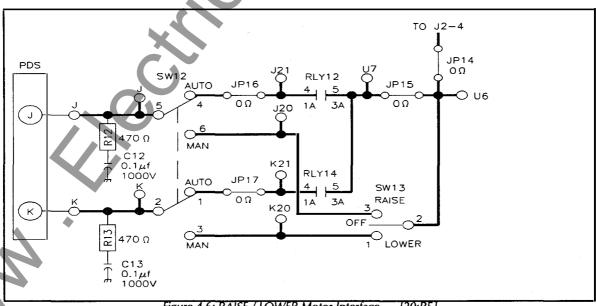


Figure 4-6: RAISE / LOWER Motor Interface [20:R5]

the microcomputer determines that the RAISE(J) motor winding should be activated, it will leave RLY14 deactivated, and only activate RLY12. When the LOWER(K) motor winding should be activated, RLY14 is activated and RLY12 is deactivated. Jumpers JP14 and JP15 must be installed to provide voltage to power the RAISE(J)/LOWER(K) motor windings. Connection points U6, U7, J20, J21, K20, K21, J and K, along with JP14 and JP15 may be used for remote control of the motor circuit. Resistor/capacitor pairs R12/C12 and R13/C13 provide an RC snubber for relay contact arc supression.

#### 4.2.2.2 Transformer Board

(Reference Appendix C, page REF-21).

The transformer board is mounted adjacent to the MI-3A control panel PCB in the MI-3A assembly, and like the PDS connector, interfaces directly with the electrical portion of the control panel board. It provides the control panel electronic section with AC voltage and current references, signal isolation. and contains configuration terminal blocks. Terminal block TB1 is used to provide compensation for regulators that do not provide a turns ratio of exactly 120 volts at rated voltage, which the MJ-3A requires. An optional relay for providing different voltage compensation under reverse power flow conditions may also be included and is also configured using this terminal strip. (Refer to Siemens MJ instruction manual, publication part number 21-115527-004, for configuration details). Terminal block TB2 provides for three different functions:

- 1) If the "AUTO INH" (automatic tap change inhibit) terminals are jumpered, tap commands to relays RLY14 and RLY12 from the control panel logic will be inhibited. The jumper will, however, have no effect when SW12 is in the MANUAL position.
  - 2) The "VRC" contacts on TB2 allow the Voltage Reduction Control module to be activated by remote control when the contacts are closed, provided the VRC option is installed, AND the control switch on the VRC option module is in the "remote" mode.
  - 3) The C2 and C connection points on TB2 allow for the series connection of auxiliary current sensing apparatus to the nominal 200 mA secondary of the regulator CT. These terminals are shorted at the factory.

Four transformers provide voltage/current references to the control panel board:

- Power Transformer T1
- Potential Transformer T2
- Current Transformer T3
- PT Zero-Cross Transformer T4

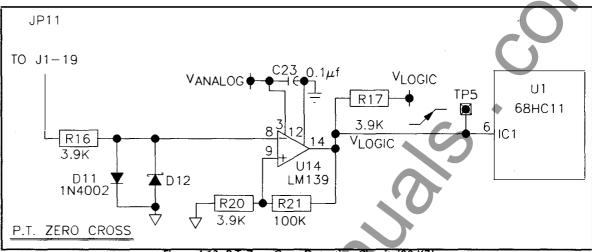
#### 4.2.2.2.1 Power Transformer T1

The power transformer provides the low voltage power supply source for the MJ-3A control panel controls. Excitation for the T1 primary (pins 1 and 4) is obtained from the PDS U2 terminal, depending on the position of the control panel External/Internal power switch SW11, as previously described. The two T1 secondaries are connected in parallel to provide maximum control panel output power (pins 6,5,8 and 7) at a turns ratio of 115:10. They are then routed directly to the output connector J3 (pins 1 and 2) where the control panel board receives a nominal 10 VAC source, at a 115 VAC input, for later rectification. T1 is a split bobbin coil design to provide maximum isolation and to minimize RFI coupling.

#### 4.2.2.2.2 Potential Transformer T2

The P.T. sensing transformer is fused by F2 and surge protected by MOV11 & 13, both located on the control panel PCB. Additional voltage surge protection is provided by snubber C2 and R4 during P.T. source select relay transitions. The Potential transformer is configured via the jumpers on TB1, mentioned previously. The primary of T2 (pins 1 and 2) is connected to the nominal 120 load side voltage of the regulator via TB1 terminals +P and P14 when the compensation relay RLY1 is not installed. The reverse power flow TB1 compensation jumpers are labeled +PA and P14A and +PB and P14B and are active when the compensation relay is installed.

Transformer T2 secondary (pins 4 and 5) provides the P.T. magnitude reference to the MJ-3A controller. The turns ratio of T2 is set at exactly 128:5. Included in the T2 transformer design are correction windings to compensate for P2 or U2 voltages not at the reference value. Any deviation is calibrated out at the factory when the MJ-3A controller is attached to a particular regulator via a set of TB1 jumpers. The resolution of the compensation windings at 120 volve is in 1 volt increments over a +/- 7 volt rms range, with the corrected P.T. voltage appearing at the Volt Test terminals located on the MJ-3A control panel. The voltages appearing at the



#### Figure 4-13: P.T. Zero Cross Detection Circuit {22:K7}

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#### P.T. Zero Cross Detection Circuit

Zero crossing information is derived via scaling transformer T4 (transformer board) for processing by the microcomputer input line IC1 (pin 6). The P.T. zero-cross signal is routed through current limiting resistor R16, bipolar diode clamps D11 and D12, and zero crossing comparator U14. The diode clamps (D11 and D12) limit the maximum input excursions applied to the U14 comparator's input to within +1 volt peak (D11) and -0.5 peak (D12) over the entire T4 output operating voltage range of 13 to 26 VAC. Diode D12 is a Schottky type to ensure that the negative voltage excursions are limited to a maximum of -0.5 volts. This is necessary to guarantee proper operation (i.e. no phase reversals) of comparator U14 in the presence of negative input voltages below its negative power rail. This clamping technique minimizes zero-cross phase error resulting from the offset threshold uncertainty of comparator U14 by clamping the T4 output signal without sacrificing its effective rate of change value as it crosses zero.

The inherent high open loop gain of the voltage comparator provides the necessary signal conditioning to convert the relatively slow changing 60/50Hz input signal into a square wave. This is required to minimize the phase uncertainty as the input signal crosses the zero voltage threshold. The square wave output of the comparator is also more suitable for the processing of phase information by the microcomputer.

The rising edge of the comparator output (pin 14) is used by the microcomputer's IC1 input (pin 6) as the phase angle time reference for both power factor and power flow derivation. Also, the time

difference between the IC1 rising edges is used to derive the power system frequency by the 68HC11 microcomputer. The rising edge was used to minimize component tolerance effects of R17, R20, and R21 on the comparator zero-cross threshold which is determined by the bias voltage on noninverting input (pin 9) of U14. With the output of the comparator at ground, the bias hyteresis voltage at the noninverting input is forced to the analog ground reference or "zero" volts. When the output of the comparator is high, resistors R20 and R21 form a voltage divider with the VLOGIC supply reference. This divider determines the resulting feedback voltage at the noninverting input. The resistor network comprised of R20 and R21 connected to the noninverting inputs provide positive feedback and the necessary input threshold hysteresis. The actual threshold voltage depends on the output state as previously described. If the sine wave monitored on the inverting input crosses the threshold in the positive direction, the actual moment of transition will be slightly delayed. There is a window of a specified time from the moment the transition was detected to when the comparator output actually transitions. This window is the amount of hysterisis in the circuit. The advantage of adding hysteresis is increased tolerance to noise voltages on the input signal. Without hysteresis, these noise voltages cause multiple switching to occur on slow input transitions. It is desirable to set the total hysteresis voltage larger than the expected magnitude of noise.

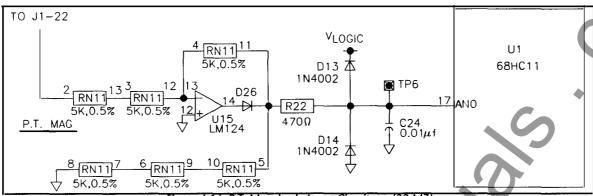


Figure 4-14: P.T. Magnitude Input Circuit [22:M7]

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#### P.T. Magnitude Input Circuit

The second P.T. analog processing path inputs the scaled secondary voltage of T2 to obtain a signal representing the magnitude of the regulator load side input voltage. The P.T. signal is routed through a precision, full-wave bridge rectifier composed of U15, RN11 and D26 via J3 (pin 5). The RN11 resistor pack has an internal relative resistance tolerance of 0.1 percent to maintain a uniform gain for positive and negative input excursions over the entire operating temperature range. The overall gain of the absolute value rectifier is 0.5. Therefore, with the given T2 turns ratio of 128:5, the peak output of the absolute value rectifier should approach but not exceed the maximum A/D input of 5 volts with a maximum P.T. input of 180 volts rms. The output of the rectifier is fed directly into the microcomputer's ANO (pin 17) analog input via a clamp network consisting of diodes D13 and D14. The 68HC11 will then calculate either an average derived or true rms value of the incoming rectified voltage signal by very rapidly sampling the waveform over a 50 msec sampling period (i.e., three cycles at 60 Hz, two and one-half cycles at 50 Hz). The decision to execute either an average derived rms algorithm or a true rms algorithm can be made via the I.D. configuration DIP switch, (SW9), position #4 (see section 2 for configuration information). During the sample interval, the digitized analog magnitude samples are either continuously integrated (summed) for the average derived algorithm or a continuous sum-ofthe-squares operation on the digitized analog samples is performed over the 50 msec period for the true rms algorithm. At the end of the sampling period, the 68HC11 will contain a digital count that is either directly proportional to the true average value of the incoming P.T. magnitude or that is directly proportional to the square of the true rms value of the incoming P.T. magnitude for the average derived or true rms algorithms respectively.

The rectified P.T. rms voltage at the 68HC11's A/D input ANO is directly related to the voltage appearing at the control panel VOLTAGE TEST banana jacks. The relationship between the two voltages is given by the turns ratio of the T2 potential transformer and the full-wave rectifier gain (i.e. VOLTAGE TEST = ANO x  $128/(5 \times 0.5)$ ). A simple technique for determining the true rms voltage of the rectified waveform at ANO using a standard true rms responding 4 1/2 digit DVM is given by the following: 1) measure the dc rms voltage component of ANO, measure the ac rms voltage component of ANO, 3) square both values and sum, and finally 4) take the square root of the squared sums. This value is now directly related to the true rms voltage at the VOLTAGE TEST terminals as described by the above relationship. Typical accuracies of 0.5% or better should be observed over a 90 to 145 volt rms P.T. input signal range.

Other components used in the P.T. magnitude signal conditioning circuit serve to protect the microcomputer from noise and transients. Bypass capacitor C24 is used as a filter for high frequency noise on the analog input ANO and decoupling of the sample/hold switching action within the 68HC11 A/D section. Resistor R22 provides current limiting to the 68HC11 analog input port and diode clamps D13 and D14. Diode clamps prevent any voltage level transients greater than 6.6 v and less than -0.6 volts from appearing at the input of the 68HC11. C.T. Signal Conditioning

The C.T. signal conditioning circuitry consists of a scaling and isolation transformer T3, zero-cross signal and conditioning circuit, and a precision full wave bridge rectifier. The C.T. scaling transformer receives excitation directly from the C.T. signal as previously described (refer to Transformer Board theory of operation). The C.T. signal conditioning circuitry is designed to operate linearly over a C.T. dynamic range of 2% to 320% of a nominal 200 mA rms 50/60 Hz input.

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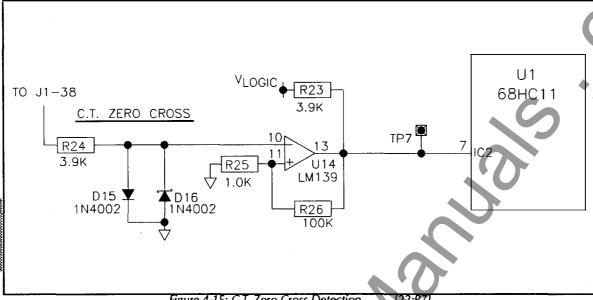


Figure 4-15: C.T. Zero Cross Detection

#### Zero Cross Detection Circuit

In the zero cross signal path the scaled secondary current from T3 is converted to a voltage via shunt resistors R27 & R28. (Reference page REF-22, top center). The C.T. zero-cross signal is routed through current limiting resistor R24, bipolar diode clamps D15 and D16, and zero crossing comparator U14. The diode clamps (D15 and D16) limit the maximum input excursions applied to the U14 comparator's inverting input to within +1 volt peak (D15) and -0.5 peak (D16) over the entire C.T. output operating current range of 4 to 640 mA ac. Diode D16 is a Schottky type to ensure that the negative voltage excursions are limited to within 0.5 volts of the ground reference. This is necessary to guarantee proper operation (i.e. no phase reversals) of comparator U14 in the presence of negative input voltages below its negative power rail. This clamping technique minimizes zero-cross phase error resulting from the offset threshold uncertainty of comparator U14 by clamping the C.T. output signal without sacrificing its effective rate of change value as it crosses zero.

The inherent high open loop gain of the voltage comparator provides the necessary signal conditioning to convert the relatively slow changing and low level 60/50Hz C.T. input signal into a square wave. This is particularly necessary at very low levels of line current in order to minimize the phase uncertainty as the input signal crosses the zero current threshold. The square wave output of the comparator is

also more suitable for the processing of phase information by the microcomputer.

The rising edge of the U14 comparator output (pin 13) is used by the microcomputer's IC2 input (pin 7) to determine the phase angle time difference from the P.T. voltage zero-cross rising edge time reference applied to IC1 via U14 (pin 14). This measured time difference is used for the basis of both power factor and forward/reverse power flow derivation. Similarly, the rising edge is used to minimize component tolerance effects of R23, R25 and R26 on the comparator zero-cross threshold which is determined by the bias voltage on noninverting input (pin 11) of U14. With the output of the comparator at ground, the bias hyteresis voltage at the noninverting input is forced to the analog ground reference or "zero" volts. When the output of the comparator is high, resistors R25 and R26 form a voltage divider with the VLOGIC supply reference. This divider determines the resulting feedback voltage at the noninverting input. The resistor network comprised of R25 and R26 connected to the noninverting inputs provide positive feedback and input hysteresis. The actual threshold voltage depends on the output state as previously described in the C.T. zero cross description. Without hysteresis, noise voltages may cause multiple switching to occur on slow and low level C.T. input transitions (i.e. less than 2% of C.T. rating). It is desirable to set the total hysteresis voltage larger than the expected magnitude of noise. Capacitor C23 provides supply decoupling at the U14 power inputs (pins 3 and 12).

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#### C.T. Magnitude Input Circuit

The second C.T. analog processing path routes the scaled secondary current of T3 into a precision shunt resistor R27 & R28 where it is converted into a voltage. The value of R28 was chosen to limit the maximum input seen by the full-wave rectifier input of U15 at an input current level of 700 mA to within 20 volts (P-P). This voltage is then fed into a precision full wave bridge rectifier, similar to the P.T. rectifier, composed of RN12, U15, and D17. The reason an active filter is used over a diode type rectifier is to reduce the size requirements of the C.T. when used with the rectifier scheme. The problem with a passive diode rectifier is that at low current levels, a significant portion of the C.T. current may be shunted through the magnetizing reactance of the C.T. due to the blocking effect of the diodes forward voltage drop in the bridge circuit.

The output of the C.T. rectifier is then fed into the 68HC11's AN1 analog input through a clamping network formed by R29 and diodes D18 and D19. The 68HC11 will then obtain an average derived or true rms value of the incoming rectified C.T. voltage signal in a fashion similar to that employed for the rectified P.T. signal. (Refer to P.T. circuit description).

The rectified C.T. rms voltage at the 68HC11's A/D input AN1 is directly related to the current circulating through the C2-C terminals (TB2) on the transformer board. The relationship between the

circulating C.T. current and the voltage appearing at the U1 (pin 18) AN1 analog input is given by the turns ratio of the T3 auxiliary C.T. transformer, the burden resistor R28, and the full-wave rectifier gain (i.e.  $C2-C = AN1/(100 \text{ hms } \times 0.5)$ ). A simple technique for determining the true rms voltage of the rectified waveform at AN1 using a standard true rms responding 4 1/2 digit DVM is given by the following: 1) measure the dc rms voltage component of AN1, 2) measure the ac rms voltage component of AN1, 3) square both values and sum, and finally 4) take the square root of the squared sums. This value is now directly related to the true rms current circulating through the C2-C terminals by the described relationship above. Typical accuracies of 0.5% or better should be observed over a 4 mA to 640 mA rms C.T. input signal range.

Other components used in the C.T. magnitude signal conditioning circuit serve to protect the microcomputer from noise and transients. Bypass capacitor C26 is used as a filter for high frequency noise on the analog input AN1 and for decoupling of the sample/hold switching action within the 68HC11 A/D section. Resistor R29 provides current limiting to the 68HC11 analog input port and diode clamps D18 and D19. Diode clamps prevent any voltage level transients greater than 6.6 v and less than - 0.6 volts from appearing at the input of the 68HC11. Capacitor C25 provides supply decoupling at the U15 power inputs (pins 4 and 11).

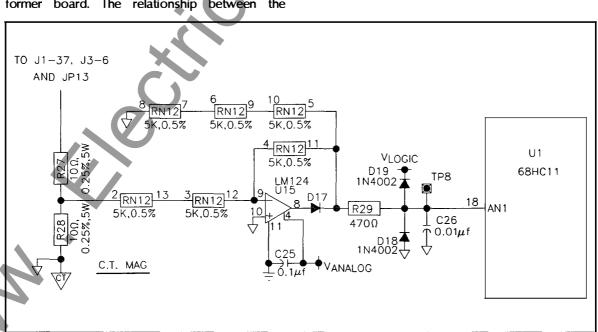


Figure 4-16: C.T. Magnitude Detection

[22:R7]

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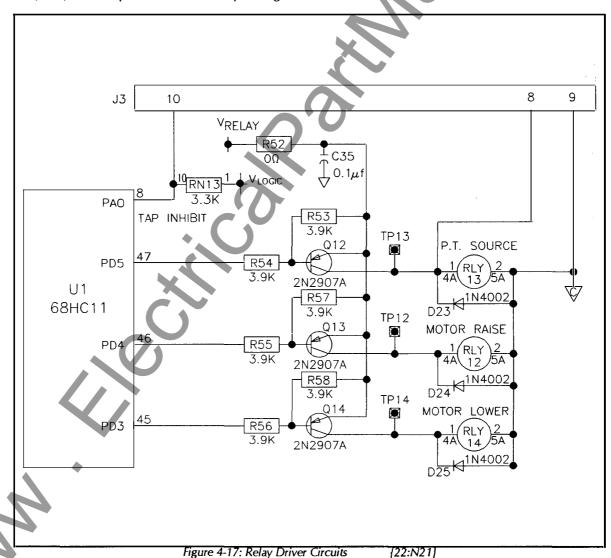
High Voltage Level Interface Circuits

#### **Relay Driver Circuits**

The "Motor Lower" (RLY14), "Motor Raise" (RLY12), and "P.T. Source" (RLY13) relays are controlled by microcomputer ports PD3 (pin 45), PD4 (pin 46) and PD5 (pin 47) respectively. Relays RLY14, RLY12, and RLY13 all incorporate 150 ohm coils and are powered via the +6VDC regulated voltage source, (VRELAY). Each relay is driven from PNP transistors Q14, Q13, and Q12, respectively, in order to supply the current necessary to energize them. Resistors R54, R55, and R56 provide the proper base biasing to the transistors to ensure relay turn on under a worst-case transistor gain. Resistors R53, R57, and R58 provide the necessary biasing to

ensure relay turn off when ports PD3, PD4, and PD5 are biased off. Diodes D25, D24, and D23 provide relay coil voltage clamping when the relays are de-energized. A separate relay coil ground return path is incorporated to shunt the potentially high circulating relay coil currents away from the more sensitive digital and analog ground returns.

The P.T. select relay RLY13 coil voltage is brought out to J3 (pins 8 & 9). These pins go to the transformer board where the P.T. compensation relay (if installed) will also activate. This will correct the sensing transformer for Forward and Reverse power flow conditions. (Refer to Siemens Instruction manual , P/N 21-115527-001, for further details).



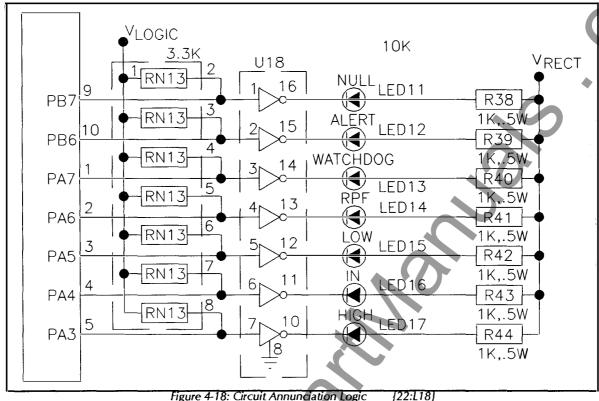


Figure 4-18: Circuit Annunciation Logic

#### User Interface Circuits

#### Circuit Annunciation Logic

A high current (500 mA) Darlington driver IC (U18) is used as an interface between the 68HC11 Ports (PA3 thru PB7) and LED11 through LED12 respectively. Pullup resistors, from resistor network RN13, connected on each of the input pins of U18 ensure that the associated Darlington driver will be biased on (turning on the LEDs) when the microcomputer port is turned off. Resistors R38 through R44 provide the necessary current limiting for their associated LEDs.

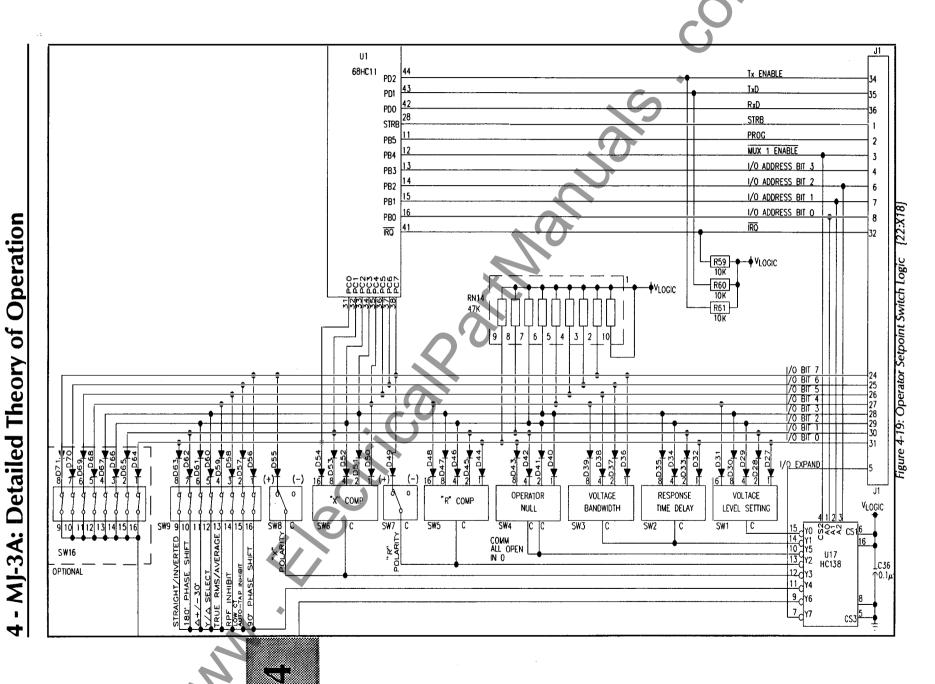
#### Operator Setpoint Switch Logic

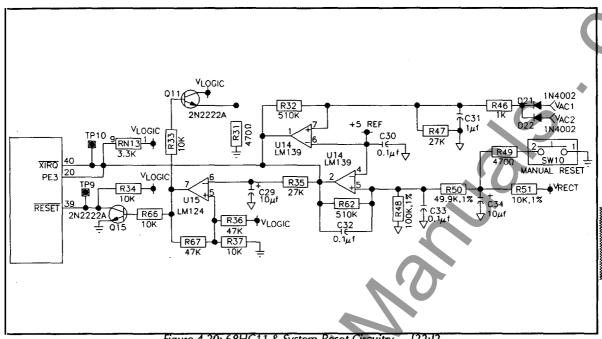
Setpoint logic, local to the MJ-3A, is made via standard control panel rotary switches, control panel toggle switches, and by setpoint switches accessed from the right side panel of the MJ-3A. These setpoint / parameter switches are encoded via nine switches SW1 through SW9 whose outputs are diode isolated and wire ORed to Port C via diodes D27 through D63(Refer to section 2 for switch definitions). These local on-board switches are individually addressed via a CMOS 3-to-8 decoder U17 and Port B through software control. Bus expansion is provided through the PCB edge connector "J1" to allow for VRC (voltage reduction control) and VLC (voltage limit control) as well as communications to the Data/Pak display option. All MJ-3A option interfaces are implemented in CMOS to minimize loading on Ports B and C and to maintain a reasonable margin of environmental noise immunity. The 47K ohm pull-up is provided for Port C input bias requirements, Additionally the use of pull-ups will be provided on the option boards due to the increased source current requirements and EMI/RFI susceptibility.

The following switches are individually scanned when PB4, pin 17, is low. This enables (mux1enable) addressing switches local to the control panel via the U17 inputs A0,A1, and A2 (pins 1,2, and 3). The required output code from ports B0, B1, and B2 necessary to select a particular switch is listed adjacent to the following switch functions using the convention (B2, B1,B0):

Standard CONTROL PANEL ACCESSED rotary and toggle switches:

- (0,0,0) Voltage Level Setting (SW1)
- (0,0,1) Time Delay (SW2)
- (0,0,1) Bandwidth Setting (SW3)





- Figure 4-20: 68HC11 & System Reset Circuitry [22:]2
- (0,1,0) "Resistance" Line Drop Compensation Switch (SW5) & Polarity switch, (SW7), "R"
- (0,1,10) "Reactance" Line Drop Compensation Switch, (SW6) and Polarity switch, (SW8),"X".

SIDE PANEL ACCESS switches:

- (1,0,0) Configuration ID switch (8 spst DIP switch (SW8)
- (1,0,1) Operator Null rotary switch (SW4).
- (1,1,0) Optional features switch (SW16)

The following switches are individually scanned when PB4 is high (which addresses remote switches on option board) via the remote 3-to-8 mux inputs A,B, and C (pins 11,10, and 9). The required output code from ports PB0, PB1, and PB2 necessary to select a particular switch is listed adjacent to the following switch functions using the convention (PB2,PB1,PB0):

REMOTELY ACCESSED option module switches:

- (1,0,1) VRC percentage switch
- (0,0,1) Upper VLC limit control switch
- (0,1,0) Lower VLC limit control switch

(1,0,0) toggle switches for VRC and VLC.

#### MI-3A Detailed Theory of Operation

#### 68HC11 RESET Function

The 68HC11 microcontroller contains on chip logic to automatically detect system RESET conditions. The RESET pin on the 68HC11 provides an active-low, bidirectional control signal to initialize the microcontroller to a known start-up state during power-up or detection of a system failure. The bidirectional RESET signal is significantly different from RESET signals used in earlier microcontrollers since it can be activated either from external RESET logic or its internal RESET system.

Under normal operating conditions the RESET input (pin 39) is held at a high 5vdc logic level by pull-up resistor R34. Transistor Q15 provides an open collector input to allow either an external logic reset or an internal self-generated 68HC11 reset. Should an internal 68HC11 reset condition occur, it will not propagate to the board SYSTEM RESET on the MJ-3A control panel at J1 (pin 33). (For detailed description of 68HC11 system RESET logic refer to Motorola M68HC11 Reference Manual M68HC11RM/AD).

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## YSTEM RESET Logic

In conjunction with the internal RESET logic function contained within the 68HC11 microcontroller, the MJ-3A control panel also incorporates external reset logic to provide a SYSTEM RESET function. The SYSTEM RESET is comprised of three separate circuit functions that contain logic for manual reset, loss of ac detection, and low operation voltage detection. The outputs of these separate reset functions are effectively ORed together to form a composite active high SYSTEM RESET output at J1 (pin 33).

Manual resetting of the control logic is accommodated via the Manual RESET switch SW10 located on the side panel access. When SW10 is depressed by the operator, the voltage level applied to the non-inverting input on comparator U14 (pin 5) is forced to a level below the inverting input (pin 4). This action will force the output of U14 (pin 2) low. The output of U14 (pin 2) is then routed to the external interrupt request input XIRQ (pin 40) on the microcontroller. This signal is then used by the 68HC11 to anticipate a SYSTEM RESET condition and initiate reset "housekeeping" functions prior to the RESET input (pin 39) going active low.

The delaying action between the external reset request XIRO and actual hardware reset is required to allow sufficient time for the 68HC11 to perform necessary "housekeeping" functions prior to a total system shutdown. Typically functions include LED indicator test and memory backup. The RESET delay time constant is determined by R35 and C29. This delay is set to approximately 0.5 seconds. The delay circuit is formed by comparator U15 (pins 5,6,& 7), R35, R36, R37, R67, and C29. It receives its input from the external interrupt request XIRQ signal. When the XIRQ signal goes active low, the inverting input to U15 (pin 6) begins to decay from the discharging action of C29 through R35. When the inverting input (pin 6) drops below the non-inverting input threshold (pin 5) on U15, the output of U15 (pin 7) goes active high. This action then biases both Q15 and Q11 on resulting in an active low RESET signal applied at the 68HC11 (pin 39) and an active high system RESET generated at J1 (pin 33). Resistors R67, R36, and R37 determined the non-inverting voltage threshold with R67 providing necessary input threshold hysteresis.

The ac power loss detection logic receives its raw ac input via rectifier diodes D21 and D22 directly from the MJ-3A power transformer secondary J3 (pins 1 & 2). This rectified input is routed through R46 to C31 and R47. These components provide

necessary filtering for proper biasing of the ac detection threshold input at U14 (pin 7) and establishes the ac loss time constant. The ac power loss logic will typically issue a reset for loss of ac greater than one cycle. The +5REF voltage applied to U14 (pin 6) determines the loss of ac threshold level. Resistor R32 provides necessary positive feedback input threshold hysteresis. During ac power loss the rectified voltage stored by C31 will discharge through R47. When this voltage level decays below the inverting input threshold on U14 (pin 6), the output of U14 (pin 1) goes active low. This signal then forms one of the three possible sources for SYSTEM RESET and similarly is routed to the external interrupt XIRQ input to the 68HC11 and reset delay circuit

The low voltage detection logic monitors the unregulated dc supply voltage VRECT on the front panel board. As previously described, this voltage is directly related to the input ac source voltage applied to the MJ-3A control panel via the PDS "U2" ac input. The unregulated supply voltage VRECT is fed directly to R51 and C34. These components form a power-up delay filter to allow stabilization of the internal dc supply voltages during power-up prior to releasing the microcontroller's RESET input. Resistors R51, R50, R49, and R62 establish the low voltage detection threshold at the non-inverting input to U14 (pin 5). This threshold is compared the +5REF voltage input threshold applied to the associated non-inverting U14 input (pin 4). Resistor R62 provides the necessary positive feedback for input threshold hysteresis. When the input supply voltage falls below the minimum threshold point (typically lower than 80 vac), the output of the low voltage detect comparator U14 (pin 2) is forced to an active low. As previously described, this output action forms the third source for SYSTEM RESET. This same logic also supports with the Manual Reset function. When the input ac voltage at the PDS "U2" input goes above the low voltage threshold point (typically greater than 85 vac), the comparator output is then forced to an active high state after the powerup delay established by R51 and C34. Note that the low voltage power detect minimum/maximum thresholds will fluctuate with the level of loading place on the VRECT power supply. Specifically, if any option modules are attached to the MJ-3A front panel, the threshold voltage window will increase slightly depending on the type and number of option modules installed. Under worst case loading the maximum power-up threshold should shift upward to no more than 90 vac (i.e. the minimum specified MI-3A operating voltage).

NOTE:
The unregulated voltage on the Interface
Board obtained from the MI-3A control pane
board is 15 volts DC, not 16 volts DC as
indicated in the Interface Board information
which follows. To be consistant with MI-1A
and MI-2A terminology, it will remain a "16
volt DC" reference by name only.

# 4.4 Interface PC Board Option

## 4.4.1 Interface PC Board - Overview

### Circuit Board Layout:

Appendix A, page REF-5

#### Block Diagram:

• Appendix B, pages REF-14

The interface board is so named because it interfaces the control panel board with the option modules:

- Data/Pak Display
- Voltage Limit Control (VLC)
- Voltage Reduction Control (VRC)

As the interface board contains the necessary support circuitry for the option modules, the interface board option is required if ANY option modules are used.

## 4.4.2 Interface PC Board Detailed

#### Schematic:

Appendix C, page REF-23

### 4.4.2.1 8035 Microcomputer

The interface board uses an Intel 8035 at the heart of its system. Provisions on the interface board have also been made to accommodate the 8748 and 8048 which are pin compatible to the 8035, but as the greatest number of interface boards produced use the 8035, the 8048/8748 will be referenced only in specific instances.

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The 8035 is configured in 40 pin Dual In-Line Package (DIP). It contains an 8 bit CPU (central processing unit), 64 bytes of RAM memory, 27 I/O lines, an internal 8 bit timer, and operates on a single 5 volt power supply. The 8035 relies on external program memory, whereas the 8048 has 1K (1024) bytes of internal ROM (read-only-memory), and the 8748 has 1K of internal EPROM (electrically programma-ble ROM).

The interface board uses the microcomputer in its expanded mode to operate with external memory. In this application, the program memory is stored in EPROM (U2). System parameters are stored in a special type of nonvolatile RAM called NOVRAM (U3 and U4). This topic will be discussed in detail under the "Microcompter Memory Management" heading.

The bus port can operate in three different modes: as a latched I/O port, as a bi-directional bus port, or as a program memory address output when external memory is used. The bus port lines are either active high, active low, or high impedance (floating).

The lower half of Port 2 can be used in three different ways: as an quasi bi-directional static port, as a port expander, and to address external program memory. In all cases, outputs are driven low by an active device and driven high momentarily by an active device and held high by a 50K resistor to 5 volts. The port may contain latched I/O data prior to its use in another mode without affecting operation of either. If lower Port 2 (P20-P23) is used to output address for an external program memory fetch, the I/O information previously latched will be automatically

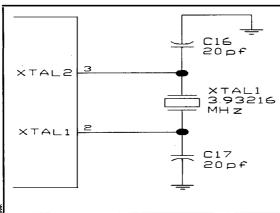


Figure 4-21: Oscillator Circuit

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removed temporarily while address is present then restored when the fetch is complete. However, if the lower Port 2 is used to communicate to another device in the expanded mode, previously latched I/O information will be removed and not restored.

#### 4.4.2.2 Oscillator Circuit

The 8035 has a built-in crystal oscillator that requires only the connection of a parallel resonant crystal for operation. Internally, the 8035 divides the crystal frequency by two to derive its basic cycle time. In this application, the chosen crystal of 3.93216 MHz yields an instruction cycle time of 3.75 microseconds.

Capacitors C16 and C17 help to prevent the internal clock oscillator from operating at any harmonics of the crystal used. To accomplish this, two 20 picofarad capacitors are connected from ground to both leads of the crystal.

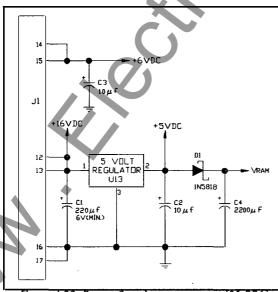


Figure 4-22: Power Supply

[23:BB6]

### 4.4.2.3 Power Supply

The unregulated +16VDC volt supply from the control panel board is available at connector 11 on pins 12 and 13. The interface board locally regulates this 16 volt level for both a +5 volt logic reference (+5VDC) and for a 5 volt NOVRAM reference (VRAM). This is accomplished via 5 volt regulator U13. Capacitors C1 and C2 provide filtering and decoupling. Schottky diode D1 acts as a barrier to isolate the 5 volt logic reference from the NOVRAM reference, ensuring that the 5 volt logic reference will not drain the NOVRAM reference voltage. The storage capacitor C4 is large enough to provide an adequate NOVRAM bias duration in the event of power failure. At the microcomputer, C12 and C13 provide added decoupling and reduced noise sensitivity (refer to REF-23 (23:U36) for placement). C3 provides decoupling of the 6 VDC supply on the interface board.

### 4.4.2.4 Microcomputer Memory Management

#### **Program Memory**

Program memory is accessed using the BUS (data bus) feature of the microcomputer. (If an 8048/8748 is used, then this feature is used to expand program memory beyond 1K.) In order to get many functions on the 8035, yet keep the package size small, some of the IC pins perform multiple functions. The eight data bits and the eight address bits are multiplexed to the same lines.

Accessing of external memory is accomplished in the following steps:

(1) The contents of the 12 bit program counter will be output to the data bus and the lower half of port 2. (2) Address latch enable (ALE) will indicate the time at which the address is valid. The trailing edge of ALE is used to latch the address externally via the U5 octal latch. (3) Program Store Enable (PSEN) indicates that an external instruction fetch is in progress and serves to enable the external memory device. (4) The data bus (BUS) reverts to input (floating) mode and the microcomputer accepts its 8 bit contents as an instruction word.

More specifically, when accessing program memory in step 1, the memory address for U2 is output on DB0 thru DB7, which are directed to the inputs

of U5 for the lower 8 bis, and P20 thru P23 for the higher 4 bits. When ALE (pin 11) goes high, the outputs of U5 (Q1 thru Q8) follow the inputs, due to latch enable, TE (pin 11), being forced high. When TE goes low in step 2, due to ALE going low, the data at the U5 inputs (D1 thru D8) will be retained at the U5 outputs until ALE goes high again.

While the address for the memory location to be accessed is available on the outputs of U5, they are also made available to inputs A0 thru A7 of U2. Both

U3 and U4 (the NOVRAMs) are disabled because the RD and WR pins are high, thus deselecting them. When the PSEN line goes low (step 3), the EPROM (U2) outputs are enabled. As SW1 is forced in the external (EXT) position by R30, the EA line will be high. All instruction fetches, including internal addresses, will be forced to be external by activating the EA pin (high level) of the 8035. Unless the microcomputer used is an 8048/8748 where SW1 may be in the internal position (INT), the EA pin will always be pulled high (+5 volts). This high level on

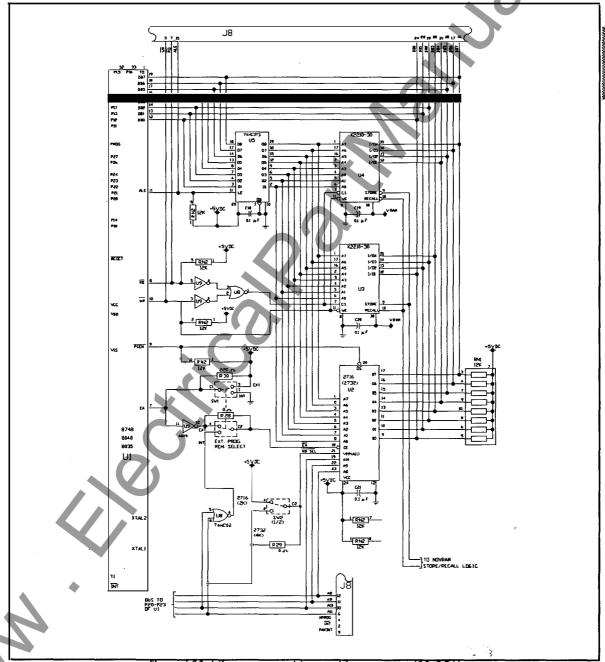


Figure 4-23: Microcomputer Memory Management {23:Q51

the input of inverter U9 forces a low output through R28, thus enabling the chip select (CS) pin of U2. Since U2 is now selected with the address on the inputs and the outputs enabled, the appropriate data is now available on outputs O0 through O7. The output lines, when tri-stated, are pulled high by resistor network RN1. They are also routed to the expander bus connector J8 and the micro data bus DB0 thru DB7. When the PSEN line goes active low, the data bus reverts to the (floating) input mode, and the output data from the EPROM U2 is treated as input data at U1.

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As mentioned earlier, the lower half of Port 2 is used as address lines A8, A9, A10 and A11. Although the Port 2 lines are used to output the most significant bits of the program address during an external program memory fetch, the I/O information is still output during certain portions of each machine cycle. I/O information is always present on Port 2's lower four bits at the rising edge of ALE and can be sampled or latched at this time.

Switch SW2 is used to select the type of EPROM installed, either a 2716 (2K) or 2732 (4K) device. If resistor R29 is installed, a 2732 (4K) EPROM must be used. The highest order address line A10 and A11 are decoded via NOR gate U8. If they were both low, indicating that an address below 1K is required, then U2 would be disabled. This feature allows program execution within the lower 1K memory bank (address 0000H to 03FFH) to occur within U1's program memory. Any program memory "fetches" beyond the 1K boundary (0400H to 0FFFH) would then be decoded via address lines A10 and A11, thus enabling the external program memory EPROM U2.

#### **Data Memory**

In a fashion similar to the program memory address decoding, the ALE signal is also used for de-multiplexing of the data memory address lines A0 through A7.

The operation of the interface board requires it to remember Data/Pak drag hand parameters. These are low voltage, high voltage, maximum Amps, leading power factor, and lagging power factor. This is accomplished with the nonvolatile static RAM (NOVRAM) comprised of ICs U3 and U4. Whenever a read or write to the NOVRAMs is required, either the RD or WR drop low (respectively). Either one will cause the output of the NOR gate U8, pin 1 to go low. This low logic enables the chip select (CS) of the NOVRAMs. The WE input of the

NOVRAM determines if either a read or write operation is about to occur when the CS line is enabled. If a read operation should occur, the logic high on the WR output of U2 will force the NOVRAMs in a "read mode". If a write operation is to be performed, a low logic level on the WR output will override the pullup of RN2, and force the NOVRAMs into a "write mode".

The purpose of the NOVRAM store/recall logic is to

- STORE: dump the contents of static RAM into the E<sup>2</sup>PROM array for safe keeping when power is removed from the system
- RECALL: dump the contents of a previously saved E<sup>2</sup>PROM array into static RAM upon applying power to the system

The STORE input, when low, will initiate the transfer of the entire contents of the RAM array to the E2PROM array internal to the NOVRAM. The WE and RECALL inputs are inhibited during the store cycle. The store operation will be completed in 10 ms or less. A store operation has priority over RAM read/write operations. If STORE is asserted during a read operation, the write will be immediately terminated and the store performed. The data at the RAM address that was being written will be unknown in both the RAM and E2PROM.

The RECALL input, when low, will initiate the transfer of the entire contents of the E2PROM array to the RAM array. The transfer of data will typically be completed in 1 microsecond or less. An array recall has priority over RAM read/write operations and will terminate both operations when RECALL is asserted. RECALL low will also inhibit the STORE input.

The actual logic which controls the store/recall logic is discussed in the POWER MONITOR CIRCUITS, which follows.



## 4.4.2.5 Power Monitor Circuits

The power monitor circuitry provides two basic functions, "power-up" RECALL and the "power-down" STORE. Each of these functions has two discrete purposes:

#### Power-Down STORE Function

#### Purpose:

- puts the reset line to the microcomputer low (in reset state) when logic voltage drops below a safe operating level
- puts the NOVRAM into a STORE state when powering down a system

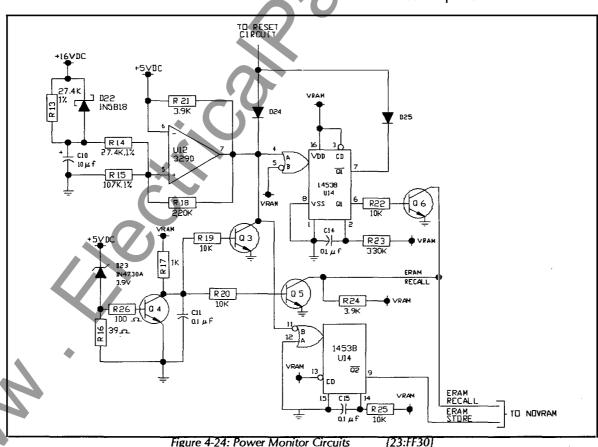
#### Power-Up RECALL Function

#### Purpose:

- forces the reset line to the microcomputer low (in reset state) until the voltage rises to a safe operating level
- puts the NOVRAM into a RECALL state when first applying power to the system.

POWER-DOWN STORE FUNCTION: The power-down STORE function is activated by a logic high-to-low falling edge transition at the B (pin 11) input of the monostable multivibrator (U14). This trigger action will only occur when either the +5VDC logic reference or +16VDC low voltage threshold detection logic senses a low system voltage condition. This forces the normally high Q2 (pin9) of the multivibrator to go low for the duration determined by C15 and R25 (1ms), thereby triggering an automatic NOVRAM store operation via the ERAM STORE output signal. The resulting pulse is at least 10 times the necessary pulse width required by the NOVRAM for a store operation.





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POWER-UP RECALL FUNCTION: The power-up RECALL function is triggered by a logic low-to-high rising edge transition at the A (pin 4) input of the monostable multivibrator (U14). This trigger action will only occur when both the +5VDC logic reference and the +16VDC low voltage detection logic sense that power supply levels are within acceptable operating limits. The actual timing for initiating a power-up recall is determined by the monostable multivibrator R23 and C14 combination (33 ms). This timing sequence is initiated on the rising edge trigger of input A (pin 4) which causes the Q1 output (pin 6) to go high for approximately 33 ms. This pulse is then inverted by Q6 and wired OR with Q5 to form the NOVRAM ERAM RECALL signal.

Note that the power-down circuitry ties in physically to the reset circuit via isolation diodes D24 and D25. When a power-down condition has been sensed or a RECALL action is active, the microcomputer is momentarily held in a reset state via diode D25 or D24.

POWER MONITOR CIRCUITS: The power monitoring function is comprised of two discrete circuits, the +5VDC logic reference detection and the +16VDC low voltage threshold detection logic. Each of these functions is implemented independently, with the outputs logically ORed at the two inputs (A and B) of the monostable multivibrator (U14). These two inputs are edge sensitive and, as a result, will only respond to logic level transitions when they occur.

The low voltage detection logic monitors the unregulated +16VDC supply voltage. This voltage is directly related to the input ac source voltage applied via the PDS "U2" input. The +16VDC low voltage threshold detection logic consists of voltage comparator U12, resistors R13, R14, R15, R18, R21, Schottky diode D22, and capacitor C10. The +16VDC is fed directly to R13, C10 and D22. These components form a power-up delay filter to allow stabilization of the internal dc supply voltages prior to releasing the microcomputer from a RESET state. Diode D22 provides a rapid discharge path around R13 to allow quick response to decaying +16VDC supply voltage. Resistors R13, R14, R15 and R18 establish the low voltage detect threshold at the non-inverting U12 input (pin 5) as compared to the +5VDC voltage input applied to U12's inverting input (pin 6). Resistor R18 provides positive feedback around the comparator and establishes the hysteresis voltage window for the low voltage detection circuit. Under normal operating system voltage levels, the output of voltage comparator U12 (pin 7) will be high. This is a result of the voltage level present on the non-inverting input (pin 5) being

greater than the voltage level signal present at the inverting input (pin 6). When the input voltage falls below the minimum threshold point (typically lower than 80 VAC at the PDS "U2" input), or power is removed from the system, the 16 volt supply ramps down, discharging C10 rapidly through D22. This results in the non-inverting input falling below the 5 volt reference of the inverting input. When this happens, the output of U12 is forced low, causing a high-to-low transition or a falling edge trigger to occur on the monostable multivibrator B (pin 11) NOVRAM STORE input. When the input voltage at the PDS "U2" input goes above the maximum threshold point (typically greater than 85 VAC), the voltage appearing at the non-inverting comparator input (pin 5) is greater than the +5VDC applied to the non-inverting input. This results in the comparator output pulled high via resistor R21. It should be noted that the low voltage detect minimum/maximum thresholds will fluctuate slightly with the level of loading placed on the +16VDC supply.

The +5VDC logic reference threshold detection logic consists of transistors Q3, Q4, and Q5, resistors R16, R17, R19, R20, R26, zener diode D23, and capacitor C11. When the system is initially powered up, zener diode D23 is not conducting because its voltage potential is less than 4.5 volts (formed by the 3.9 volt zener plus the emitter-base voltage of 0.6 volts). This biases transistor Q4 out of conduction and transistors Q3 and Q5 in conduction via R17, R19 and R20, forcing the RECALL input to the NOVRAM at ground. This action forces the NOVRAM in a recall mode, thereby inhibiting any STORE inputs during power-up. As the 5 volt supply begins ramping above 4.5 volts, zener diode D23 will begin to conduct, biasing transistor Q4 into conduction. This will turn off transistor Q5, releasing the RECALL line. Conversely, when the +5VDC logic supply falls below the 4.5 volt threshold, transistor Q4 is biased off, thus forcing Q3 into conduction. This results in a high-to-low edge trigger at the multivibrator's B input, therefore activating a NOVRAM STORE sequence as previously described. Capacitor C11 reduces the response sensitivity of the circuit to any noise that may exist on the +5VDC supply.

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#### 4.4.2.6 Reset Circuit

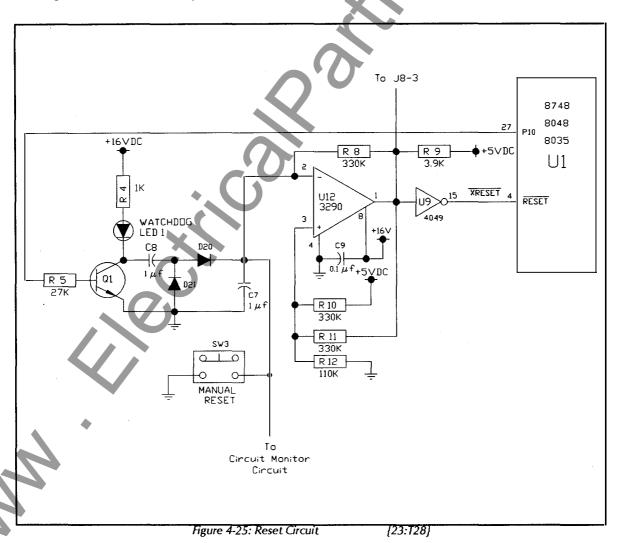
The reset circuit consists of a watchdog charge pump circuit (C7, C8, D20, D21, Q1, R4, R5, LED1), and a self-arming watchdog timer comprised of voltage level comparator circuit (U12, U9, R8, R9, R10, R11, R12, C9) which provides a simple and reliable means of automatically resetting the microcomputer should it become "lost". Under normal operating conditions, a 8 Hz square wave will appear at the output of the 8035 (U1) P10 output (pin 27). This signal is directed to the base of transistor Q1, turning it on. This periodic signal at the collector of Q1 will maintain a voltage level at the negative input of U12 (pin 2) greater than the positive input voltage threshold via the charge pumping action through C7, C8, D20 and D21. As a result, the output of U12 will be forced to a low level. Should the normal program execution flow become disrupted, the high voltage level stored on C7 will discharge thru R8 below the positive threshold,

causing the output of U12 to go high. This level is directed to the J8 bus for reset detection as well as to the input of inverter U9. The output of U9 (pin 15) is then forced to a low logic level which will reset the microcomputer. Should normal program execution fail to reoccur, C7 will then recharge via R8 and R9 to a potential higher than the positive input threshold, thus allowing the watchdog to self-arm itself and automatically re-initiate another reset pulse. This action will continue indefinitely or until normal program execution is reestablished.

The watchdog LED flashes at the 8 Hz rate tovisually indicate that the microcomputer is operating successfully. It is turned "on" when Q1 conducts and "off" when Q1 is biased off via P10.

The manual reset pushbutton forces the inverting input to ground which in turn will reset the micro-computer, as previously described.

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## 4.4.2.7 Port 2 Arbitration Logic

As mentioned in the "8035 Microcomputer" heading, the lower half of Port 2 can be used in three different ways: as an quasi bi-directional static port, as a port expander, and to address external program memory. The interface board logic utilizes all three of these modes. Addressing external memory using Port 2 was discussed previously in the "microcomputer memory management" heading. This heading deals with the other two modes which haven't as yet been discussed. The first topic deals with decoding switch settings on the interface and Data/Pak boards which use the Port 2 lines in their "quasi bi-directional" mode. The second and third topics, Data/Pak interface logic and control panel communications logic, respectively, use the "port expander mode".

Switch Decoding

DIP switches SW5, SW6, SW7 and SW8 are located on the Interface PC board and serve as configura-

tion inputs for the Data/Pak C.T. Ratio, Volts, Amps, and Power Factor display functions. The Data/Pak rotary switch informs the microcomputer of desired display function. The SW4 pushbutton performs a Data/Pak "Drag Hands" reset function, thereby clearing previously saved min/max values in NOVRAM. All these devices are selected by a CMOS decoder (U7). Port lines P11, P12, P13 and P17 determine which device has access to the Port 2 bus at the appropriate point in time. The switches are time multiplexed into Port 2 and only one switch device will be selected at a time, and no device will be selected if the inhibit INH line is high.

The outputs of the switches are diode isolated and wire ORed to Port 2 via isolation diodes D2 through D19. When the appropriate switch address is selected via U7 outputs 0 through 7, the common to the switch will be at ground potential. Any closed switch will force the appropriate Port 2 (P20 thru P27) line to which it is connected to ground potential, otherwise, the line will be biased high via the internal 50K pullups provided by the 8035. When any switch is actively being processed, all other devices are disabled, so the microcomputer "sees" only the active selected device.

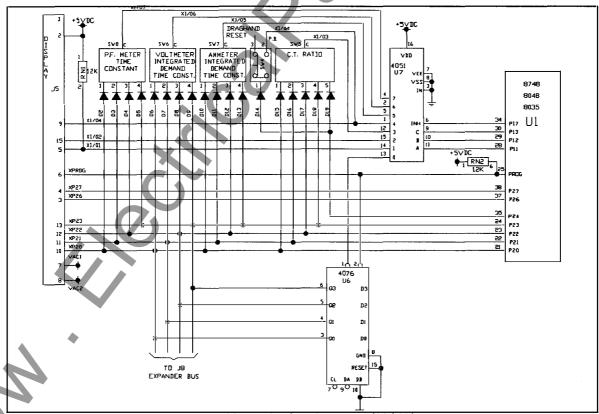


Figure 26: Port 2 Arbitration Logic. {23:h22}

#### Data/Pak Interface Logic

The rotary switch on the Data/Pak is decoded by the method just described. However, the method of both sending data to the Data/Pak and enabling it utilize the "port expander" method. The Data/Pak discussion will provide comprehensive details on this topic.

### 4.4.2.8 Control Panel Data/Pak Communications Logic

The control panel Data/Pak communications utilizes the "expanded mode" as well. Decoder U7 selects the D flip-flop U6 when Data/Pak data is to be transferred from the control panel board to the interface board. When the microcomputer wants to read the data on the Port 2 lines, a PROG pulse is generated which enables the outputs of U6. The data from U6 is then read into the 8035 via P20 thru P23.

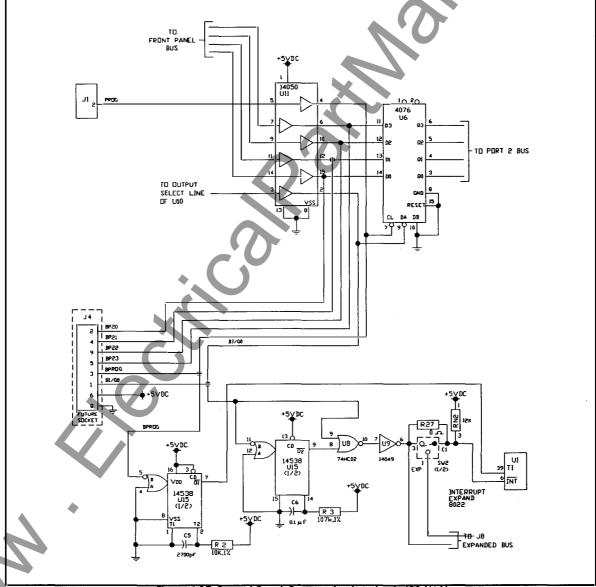


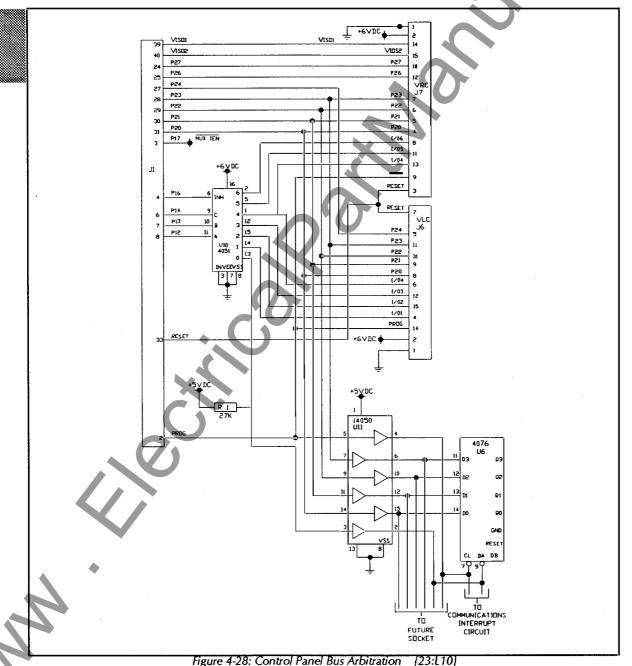
Figure 4-27:Control Panel Communications Logic [23:X16]

The 8035 is informed that data is available at U6 via interrupt circuitry. Data is then clocked into U6 via the control panel 68HC11 PROG strobe. A detailed explanation is given under the "Control Panel Communications Interface" heading.

#### 4.4.2.9 Control Panel Bus Arbitration

The control panel bus consists of P20 thru P27 on connector J1. These lines come directly from the 68HC11 microcomputer on the control panel

board and are not to be confused with the port designators for the 8035. The portion of the control panel bus which is used for arbitration are lines P20, P21, P22 and P23. These lines are directed to the VRC module, VLC module, and also to U11 which is used for data communications from the control panel to the interface board. It is the control panel board which determines which device is active by selecting the appropriate inputs on the decoder U10. A detailed explanation of the control panel communications is in the next topic of discussion. Later topics describing the VRC and VLC option modules describe their operation in detail as well.



## 4.4.2.10 Control Panel Communications Interface

The control panel address selection of (0,0,0) on inputs A,B and C selects output 0 (pin 13) on the 3-to-8 decoder U10. This occurs when a data buffer transfer is requested from the control panel board. It enables the transfer of data into the D flip-flop (U6) via the 68HC11 PROG data strobe. It also interrupts the 8035 microcomputer and alerts it to prepare for a pending control panel data transfer via the 8035 interrupt input (pin 6). The 8035 responds to this interrupt by enabling the U6 D latch outputs via its I/O select 3-to-8 decoder U7 output 0 (pin 13). The 68HC11 PROG line is used to inform the 8035 that data has been latched and is awaiting transfer via the U1 T1 input (pin 39). The pulse width of the 68HC11 PROG data strobe line is lengthened by monostable multivibrator U15 to 27 microseconds to ensure capture of the data by the 8035 at the T1 input. When actual data is sent from the control panel board, the PROG line is pulsed to a logic low (J1 pin 2). This triggers the following events: first, the data present at the D flip-flop inputs (D0 thru D3) is clocked into latch via the 68HC11 PROG strobe at U6 (pin 7). Second, the 68HC11 PROG data strobe (from the control panel) is routed to the 8035 to ensure it acts on the data immediately. Third, the latched data is then accessed via the Port 2 input lines (P10 thru P13) by enabling the D latch outputs (Q0 thru Q3) via the 8035 PROG data strobe which is controlled by the 8035 port arbitration logic. Each data transfer sequence involves 62 transfers of 4-bit data nibbles. Once the I/O channel is established by interrupting the 8035 via its INT input (pin 6), it remains active until the entire transfer sequence has been initiated. Should the data transfer become disrupted, the U14 monostable one-shot will time out, releasing the 8035 interrupt input (pin 6), thereby allowing the 8035 to resume its normal program operation.





## 4.5 Data/Pak Display Option

## 4.5.1 Data/Pak - Overview

Circuit Board Layout:

Appendix A, page REF-6

Block Diagram:

Appendix B, pages REF-15

The Data/Pak, located on the MJ-3A control panel, provides a liquid crystal display readout of:

- Present power factor with LEDs to indicate leading or lagging power factor
- Present Current Reading
- Present Voltage Reading
- Compensated Voltage Reading Reads effect of voltage with line drop compensation factored in
- Drag Hands Digital readout that indicates lowest voltage, highest voltage, maximum current, most leading power factor, and most lagging power factor, since last reset by operator
- Alert coded display that provides information to operator for limited self diagnostics

# 4.5.2 Data/Pak Display - Detailed

#### Schematic:

Appendix C, page RFF-24

The Data/Pak option provides a visual indication of key operating parameters. The heart of the Data/Pak module is the display driver IC (U1) which operates the 4 digit liquid crystal display. This driver IC is a version made for microcomputer interfacing, and provides non-multiplexed operation of LCD displays. It has 4 BCD data inputs (B0, B1, B2 and B3), two address lines (DS1, DS2), and two chip select lines (CS1, CS2).

The display driver section of U1 includes an oscillator, a 7 stage binary divider, a backplane driver, backplane slaving detector and logic, and 28 segment drivers. The RC oscillator has a nominal oscillation frequency of 19 kHz with no external components. The frequency is lowered slightly by the addition of the external capacitor (C2) between pin 36 and V+. The 19kHz (approximate) output of the on-board oscillator is divided by a 7 stage binary divider to generate the backplane frequency of 150 Hz. The backplane drive is simply an inverter whose input is the output of the last driver. The backplane output swings from ground to V+ with a 50% duty cycle. The backplane has a low (200 ohm typical) output resistance so that it can drive the capacitance of large displays. The segment drivers are CMOS inverters that swing between ground and V+ with an output resistance of about 2K ohms. The input to the inverter is switched between two signals, so that the segment driver output is the same as the backplane when LCD segment is to be turned OFF, and is BACKPLANE when the LCD segment is to be turned ON. The segment and backplane drivers are designed to have equal rise and fall times, so that the average DC component across the LCD is less than 25 millivolts.

The operation of the Data/Pak module was briefly discussed in the discussion of the interface board because it is from there that the module receives all its instructions. The port 2 arbitrator circuit discussed the scanning of switches using the decoder IC (U7). Output 4 of this decoder selects the rotary switch on the control of the Data/Pak module (SW1) to decide what function the user desires to be displayed. When selected, XI/O4 on connector J5 (pin

9) is low. This effectively places the common of the switch at ground potential as well as anylines whose switches are closed. The switch reading is then detected on the port 2 lines through isolation diodes D1,D2,D3, and D4 in the same manner as the DIP switches on the interface board are read.

The D flip flop (U2) provides logic for additional features on the Data/Pak for both updating the power factor LEDs and also for decimal point control for the LCD. The outputs are never tri-stated in this circuit because the output disable lines (pins 1 & 2) are tied to ground. The input disable is controlled by XI/O2 on the J5 connector (pin 15). Proper pull-up biasing is provided by resistor R3. This input is enabled by the port2 bus arbitrator circuit via output 2 of U7 on the interface board. Thus, only when the 8035 on the interface board places the appropriate output code, will the data lines be enabled to U2. When a clock pulse is generated by the PROG from the 8035, the data available is clocked into U2 and accordingly sets the outputs. Whether the PROG pulse strobes data into the D flip flop for LED / decimal point control, or to the actual LCD depends entirely on which one is enabled via XI/01 or XI/02 when the PROG occurs. This accordingly sets the outputs of the D latch Q0 thru Q1. Resistors R1 and R2 provide proper biasing of transistors Q2 and Q1, which in turn, satisfy the drive requirements of the status indicators LED2 and LED1. Resistors R4 and R5 provide the necessary current limiting for the LED indicators to typically 15 mA. Capacitor C3 and C1 provide decoupling for the +6VDC supply. R6 provides additional pull-up biasing for the incoming RESET line

Control of the LCD decimal points DP1, DP2, DP3 and COLON segments is accomplished via the exclusive OR function of U3. Decimal point DP2 and COLON segments are forced off by driving these segment inputs with a voltage in phase with the LCD backplane. However, the ability to both turn off or on decimal points DP1 and DP3 is provided via exclusive OR gates in conjunction with the D latch Q2 and Q3 outputs. When the Q2/Q3 outputs are at a high logic level, the outputs of the associated XOR gates will be a waveform 180 degrees out of phase with the LCD backplane (inverted). This will bias "on" the decimal point segments. Likewise, when the outputs of Q2/Q3 are latched low, the XOR gates will generate a voltage in phase with the backplane waveform, thus turning "off" the LCD segments. It is through this action that all of the active LCD segments associated with DSP1 are controlled.





# 4.6 Voltage Limit Control (VLC) Option

#### 4.6.1 VLC - Overview

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Circuit Board Layout:

Appendix A, page REF-7

Block Diagram:

Appendix B, pages REF-16

The VLC option ensures that the voltage regulated to by the MJ3A stays within a preset span. The VLC hardware resides on an external PCB and interfaces to the main control board via interface board connector J6. It includes both upper (SW1) and lower (SW2) VLC set point switches along with their associated upper (LED2) and lower (LED1) warning indicators and the VLC ON/OFF switch (SW3). The upper VLC set point range is from 120 to 135 volts rms in one volt increments. The lower VLC set point range is from 105 to 120 volts rms in one volt increments. Both switches are binary encoded type switches.

## 4.6.2 VLC - Detailed

Schematic:

• Appendix C, page REF-25

As discussed briefly in the Operator Setpoint Switch Logic section of the Control Panel PCB section, the reading of the VLC setpoint switches and control of the upper/lower limit LEDs are controlled via the Control Panel PCB microcomputer (U1) program logic. The interface board 3-to-8 decoder (U10) is used to select each switch and the D latch (U1) on the VLC module in the same manner as described for the Control Panel setpoint switches. The control

panel microcomputer, via Port 1, selects the specific I/O device at the appropriate time by applying the necessary binary code to the I/O select decoder (U10) inputs A,B, and C (pins 11,10,and 9). This action will then activate the specified output of the I/O decoder (U10) which is then routed to the proper I/O device. For the VLC module, four I/O select outputs are used for control of the VLC indicators and reading of the VLC switches.

The VLC UPPER (SW1) and LOWER (SW2) switches are enabled via the I/O1 and I/O2 lines, respectively. These lines are routed to the VLC module via connector J6 (pins 4 and 15). The specific switch information is read by the microcomputer by driving their common switch inputs (pin C) to ground potential (low) via the I/O select decoder (U10). This action will in turn force the associated Port 2 input lines (P20 - P24) low through isolation diodes (D1 thru D10) for any switch contact that is connected to the switch common (pin C). Likewise, for any switch contacts not shorted to the common pin the associated Port 2 input will not be pulled low, but will remain at a logic high. It is in this manner that the switch positions are then decoded by reading the resulting binary code via the Port 2 input lines of the control panel microcomputer.

Similarly, the presence of the VLC module and its activation via the ON/OFF switch (SW3) is sensed using the I/O4 line on J6 (pin 6). When the VLC module is attached to the J6 connector, diode D11 is used by the control panel microcomputer logic to determine if a VLC module is present. If a VLC module has been attached, this will result in the Port 2 input P20 being pulled to a logic low level through isolation diode D11 when the I/O4 line is selected. If the microcomputer logic does not sense the presence of the VLC module via this mechanism, the VLC option function will remain inactive, independent of the position of the VLC ON/OFF switch (SW3). Once the microcomputer logic has determined that the VLC module is present, it will then test the Port 2 P21 input line for the position of the VLC ON/OFF switch. If the switch is in the ON position, then P21 will be pulled to a logic low level via isolation diode D12 when the I/O4 line is activated, as previously described. Otherwise, P21 will remain pulled to a logic high when the switch is in the OFF (open) position.

The D latch (U1) allows for control of the VLC upper/lower LEDs. The two latched U1 outputs Q0 (pin 3) and Q1 (pin 4) are used to turn off/on the LOWER LIMIT and UPPER LIMIT LEDs respectively. The outputs are always in an active logic state as a result of the output enable lines QB (pin 2) and QA (pin 1) being tied to their active state. The D latch

inputs are enabled via the I/O3 line routed from 16 (pin 12) and attached to the DA (pin 9) latch enable line. As previously described, I/O3 is controlled by the control panel microcomputer Port 1 logic and is enabled only at the appropriated time. Resistor R1 provides the necessary pull-up biasing for DA when U1 has been de-selected via I/O3. Once the D latch has been selected, the desired LED on/off status presented at the D0 (pin 14) and D1 (pin 13) inputs by the microcomputer is then clocked into the D latch inputs via the clock pulse generated from the PROG line of the control panel microcomputer. The PROG pulse is routed from connector J6 (pin 14) to the D latch clock input CL (pin 7). This accordingly sets the outputs of the D latch Q0 and Q1. Resistors R3 and R4 provide proper biasing of transistors Q2 and Q1, which in turn, satisfy the drive requirements of the status indicators LED2 and LED1. Resistors R6 and R7 provide the necessary current limiting for the LED indicators to typically 15 mA. Capacitor C2 and C1 provide decoupling for the +6VDC supply. Resistor R8 provides additional pull-up biasing for the incoming RESET line.





# 4.7 Voltage Reduction Control (VRC) Option

4.7.1 VRC - Overview

4

Circuit Board Layout:

Appendix A, page REF-8

**Block Diagram:** 

Appendix B, pages REF-17

The VRC is an optional feature that can be added to the MJ-3A to allow for local or remote voltage reduction control upon demand. The VRC hardware resides on a PCB that connects to the interface board via J7. It incorporates a local/remote switch function (SW2) for enabling either externally or locally the VRC setpoints and a VRC status indicator (LED1). The VRC set point range is selectable from 0 to 10 percent in 1 percent increments and incorporate a binary encoded type switch (SW1).

#### Operating Modes.

Two operating modes are possible with the VRC on an Accu/Stat MJ-3A.

1) Activation (either by local switch or remotely) for a period of three seconds or more, will cause the regulator to lower the output voltage by the preset percentage. This reduction will be maintained for as long as VRC is activated.

NOTE: This mode of operation is identical to that of previous MJ series controls.

2) Activation with a switch closure, of less than 3 seconds duration, causes the regulator to lower its output voltage by one-third of the preset percentage. A second switch closure of less than three seconds duration causes voltage reduction to total two-thirds

of the preset percentage. Closing the switch ta third time for less than three seconds results in a voltage reduction of the full preset percentage. The forth such closure returns the control to zero reduction, i.e. deactivating the VRC.

The control can be activated locally for test or remotely, as via a relay controlled by a SCADA system connected to appropriate points on the rear of the control. When activated, the command for reduction is immediate, overriding the time delay set on the basic control. An LED is illuminated when the VRC is active.

## 4.7.2 VRC - Detailed

#### **Schematic**

Appendix C, page REF-26

As discussed briefly in the Operator Setpoint Switch Logic section of the Control Panel PCB section, the reading of the VRC setpoint switches and control of the VRC status LED is controlled via the Control Panel PCB microcomputer (U1) program logic. The interface board 3-to-8 decoder (U10) is used to select the switch and the D latch (U1) on the VRC module in the same manner as described for the Control Panel setpoint switches. The control panel microcomputer via Port 1 selects the specific I/O device at the appropriate point by applying the necessary binary code to the I/O select decoder (U10) inputs A,B, and C (pins 11,10,and 9). This action will then activate the specified output of the I/O decoder (U10) which is then routed to the proper I/O device. For the VRC module, three I/O select outputs are used for control of the VRC indicator and reading of the VRC switches.

The VRC setpoint switch (SW1) is enabled via I/O select line I/O5. This line is routed to the VRC module via connector J7 (pin 11). The specific switch information is read by the microcomputer by driving the common switch input (pin C) to ground potential (low) via the I/O select decoder (U10), on the interface board. This action will in turn force the associated Port 2 input lines (P20 - P24) low through isolation diodes (D1 thru D40) for any switch contact that is connected to the switch common (pin C). Likewise, for any switch contacts not shorted to the common pin the associated Port 2 input will not be pulled low, but will remain at a logic high. It is in this manner that the switch positions are then decoded by reading the resulting binary code via the Port 2 input lines of the control panel microcomputer.

Similarly, the presence of the VRC module and its activation via the LOCAL/OFF/REMOTE switch (SW2) is sensed using I/O select line I/O4 on J7 (pin 13). When the VRC module is attached to the J7 connector, the presence of diode D5 is used by the control panel microcomputer logic to determine if a VRC module is present. If a VRC module has been attached, this will result in the Port 2 input P27 being pulled to a logic low level through isolation diode D5 when the I/O4 line is selected. If the microcomputer logic does not sense the presence of the VRC module via this mechanism, the VRC option function will remain inactive, independent of the position of the VRC LOCAL/OFF/REMOTE switch (SW2). Once the microcomputer logic has determined that the VRC module is present, it will then test the Port 2 P26 input line for the status of the VRC LOCAL/OFF/REMOTE switch. If the switch is in the LOCAL position, then P26 will be pulled to a logic low level via isolation diode D6 when the I/O4 select line is activated, as previously described. If SW2 is in the OFF (open) position, P26 will remain pulled to a logic high when the switch status is read by the microcomputer. When SW2 is placed in the REMOTE position, OPTO-COUPLER (U2) will control the sensed status of the REMOTE VRC input located on the transformer board. (Refer to Transformer Board section 4.2.2.2 for more detailed explanation of the remote VRC input.) When the REMOTE VRC inputs are shorted on the transformer board, OPTO-COUPLER U2 is activated through current limiting resistors R2 and R3 and filter capacitor C3. Capacitor C2 provides additional ac filtering for older MJ transformer designs that did not incorporate an on-board OPTO-COUPLER. When activated, the OPTO-COUPLER's output V<sub>0</sub> (pin 6) will track its GND (pin 5) input. Therefore, if the OPTO-COUPLER has been activated via a remote VRC input and the REMOTE/OFF/LOCAL switch is in the REMOTE position, the Port 2 P26 input will be pulled to a logic low level when the I/O4 input is activated by the control panel microcomputer. This will then alert the microcomputer logic that a remote VRC signal has been sensed.

The D latch (U1) allows for control of the VRC status LED. The latched U1 output Q0 (pin 3) is used to turn off/on the VRC ENGAGED LED. The outputs are always in an active logic state as a result of the output enable lines QB (pin 2) and QA (pin 1) being tied to their active state. The D latch inputs are enabled via the I/O6 select line routed from J7 (pin 8) and attached to the DA (pin 9) latch enable line. As previously described, I/O6 is controlled by the control panel microcomputer Port 1 logic and is enabled only at the appropriate time via the I/O select decoder (U10) located on the interface board. Resistor R1 provides the necessary pull-up biasing for a logic high when U1 is de-selected.

Once the D latch has been selected, the desired LED on/off status presented at D0 (pin 14) by the microcomputer is then clocked into the D latch inputs via the clock pulse generated from the PROG line of the control panel microcomputer. The PROG pulse is routed from connector J7 (pin 9) to the D latch clock input CL (pin 7). This accordingly sets the output of the D latch Q0 (pin 3). Resistor R5 provides proper biasing of transistor Q1, which in turn, satisfies the drive requirements of the status indicator LED1. Resistor R7 provides the necessary current limiting for the LED indicator to typically 15 mA. Capacitors C1 and C4 provide decoupling for the +6VDC supply. Resistor R8 provides additional pull-up biasing for the incoming RESET line.

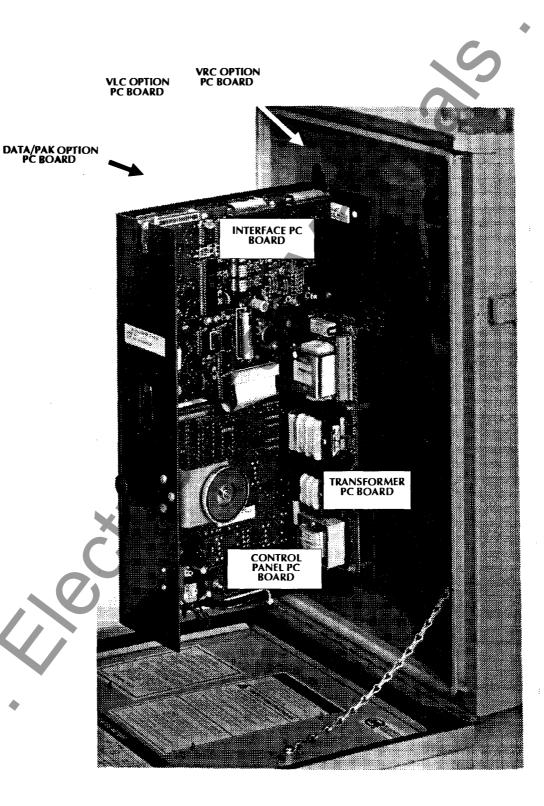


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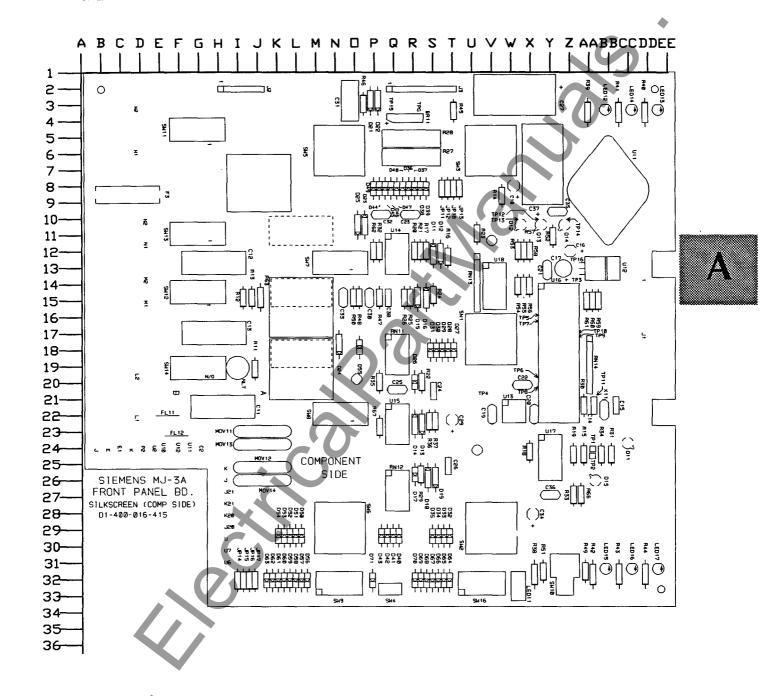
APPENDIX A: Circuit Board Layouts

### MJ3A Control Panel with Options

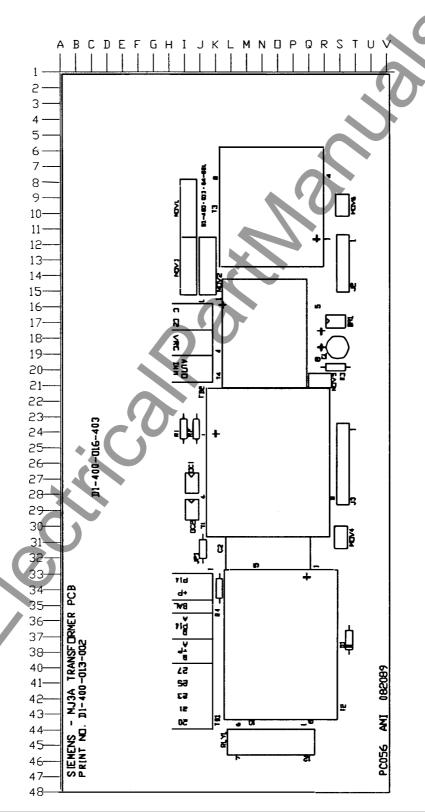




### **APPENDIX A.1: Control Panel PC Board**

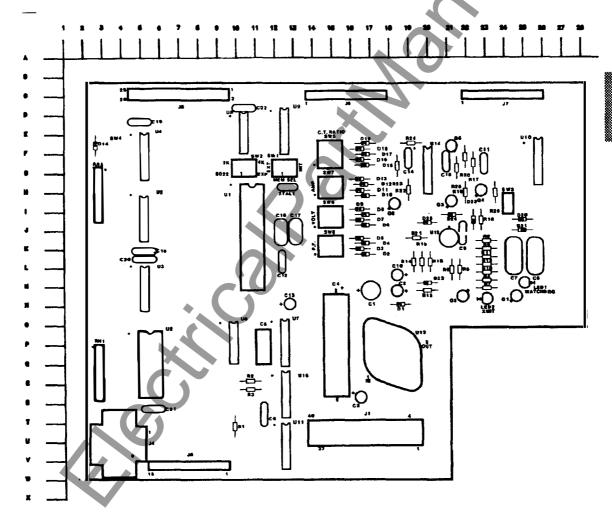


### **APPENDIX A.2: Transformer Board**





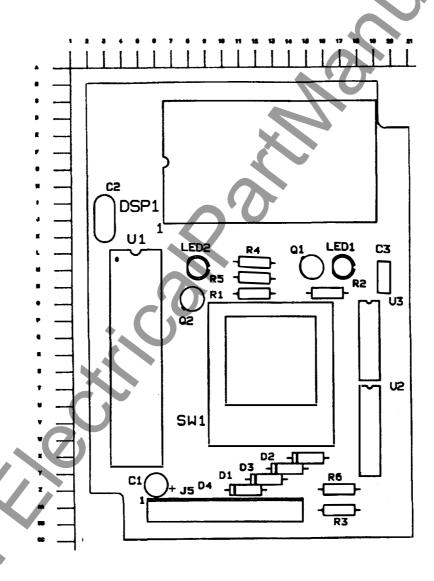
### **APPENDIX A.3: Interface PC Board**



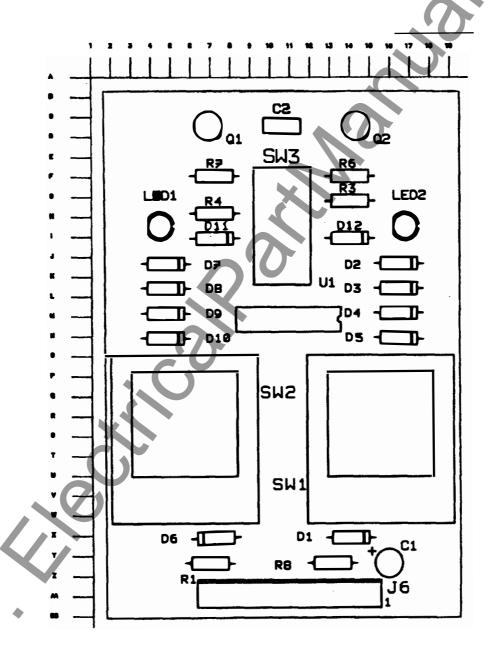


### APPENDIX A.4: Data/Pak Option



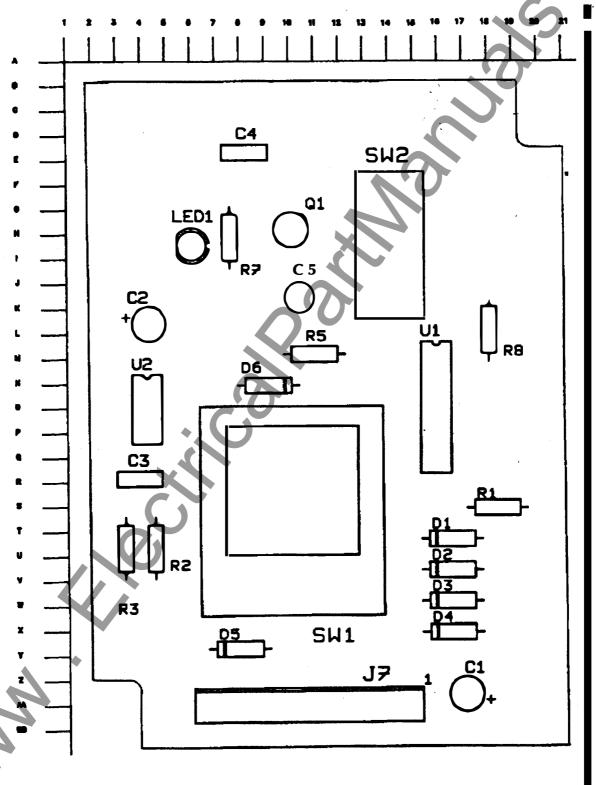


### APPENDIX A.5: VLC (Voltage Limit Control) Option





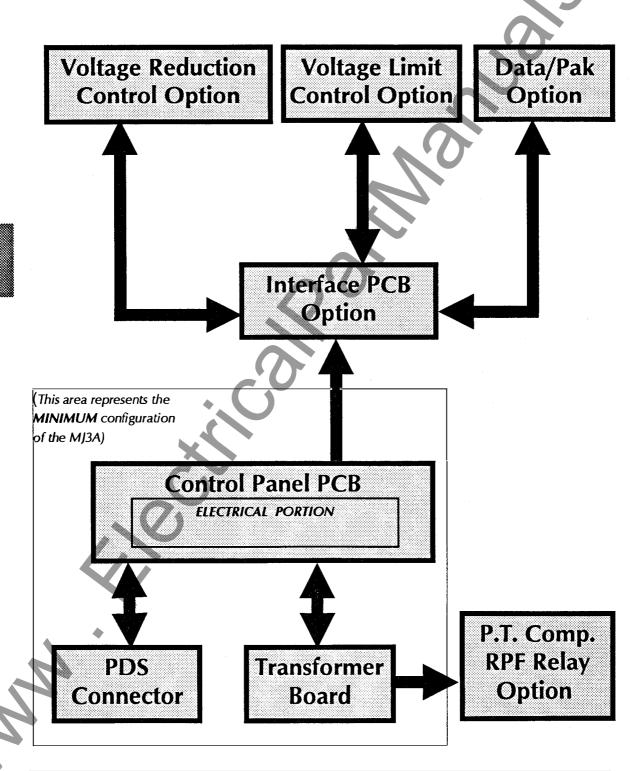
### APPENDIX A.6: VRC (Voltage Reduction Control) Option



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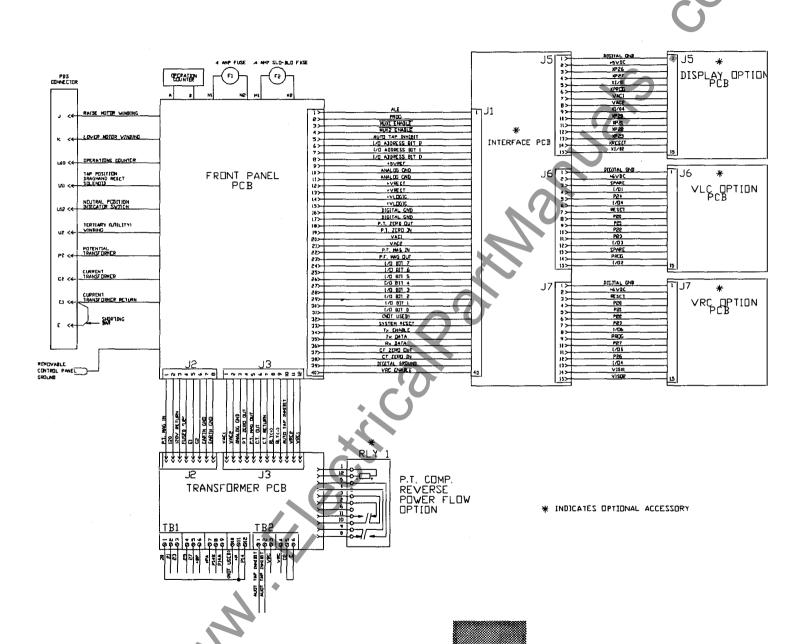
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APPENDIX B: Block Diagrams



# Appendix B: Block Diagrams

MJ3A Control Panel Interconnection Block Diagram



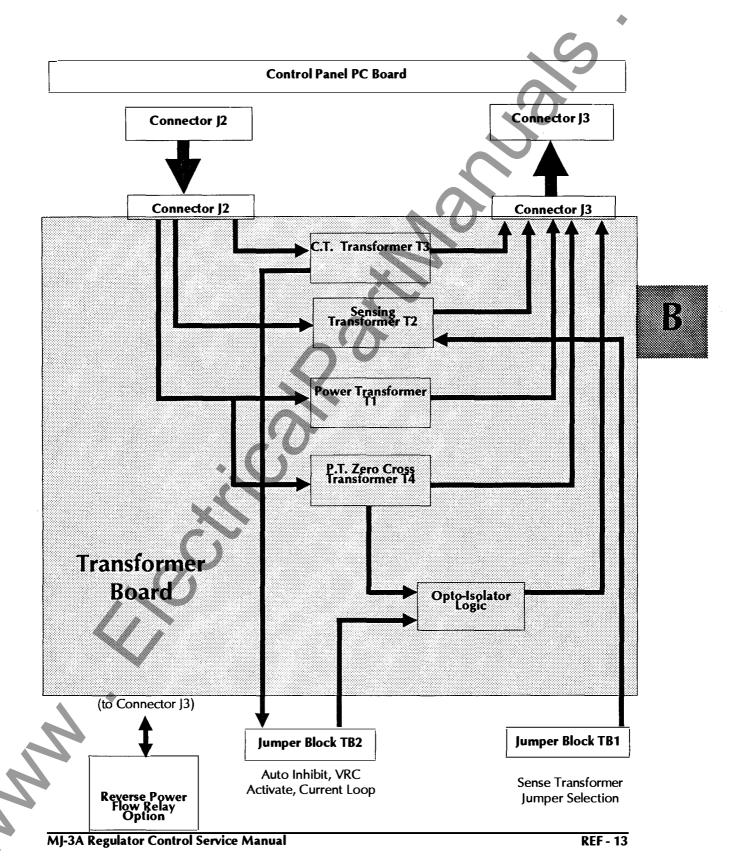
‱`∞

**Low Voltage** 

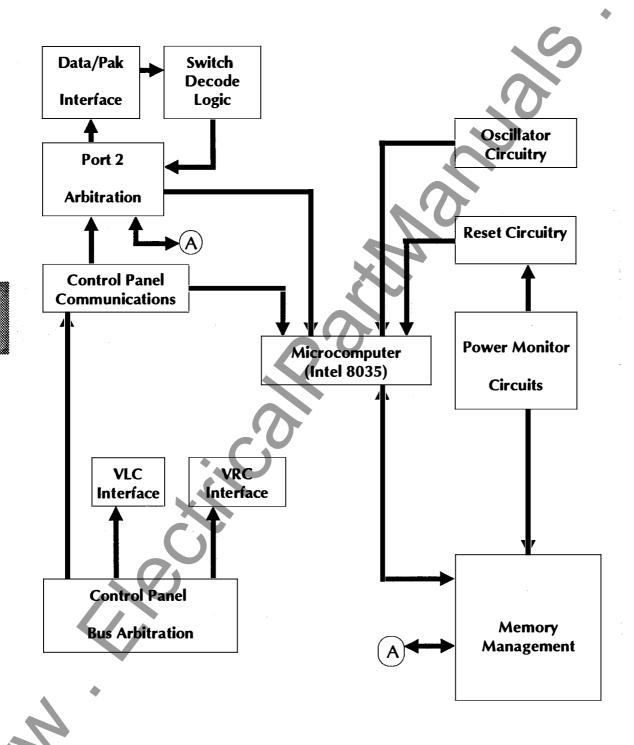
В

**Current Transformer Magnitude Reference** 

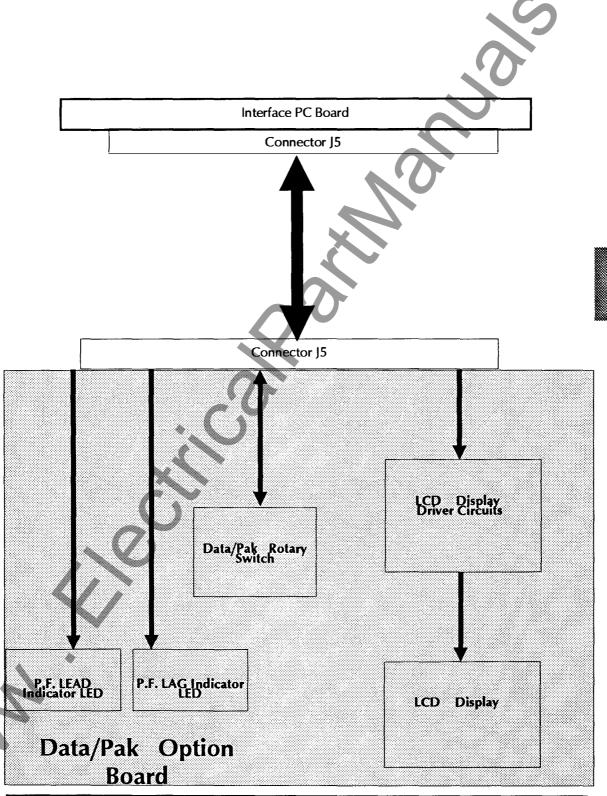
### **APPENDIX B.2: Transformer Board**

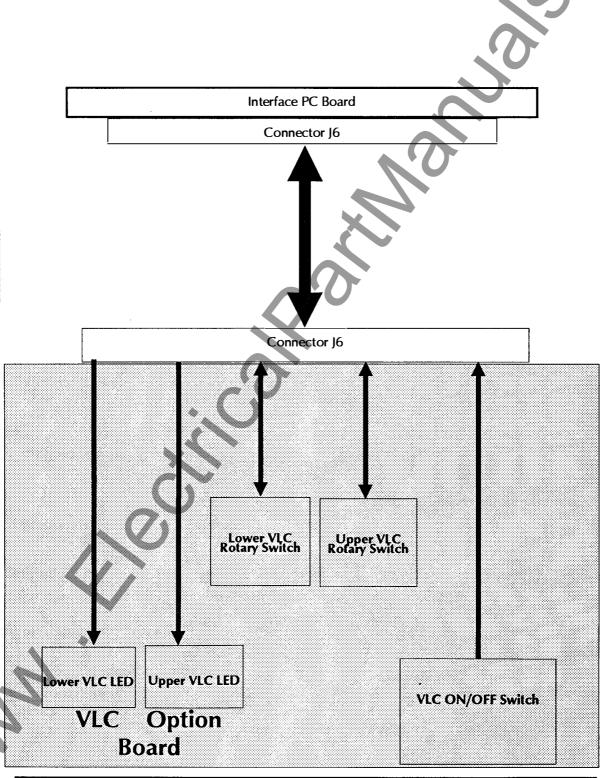






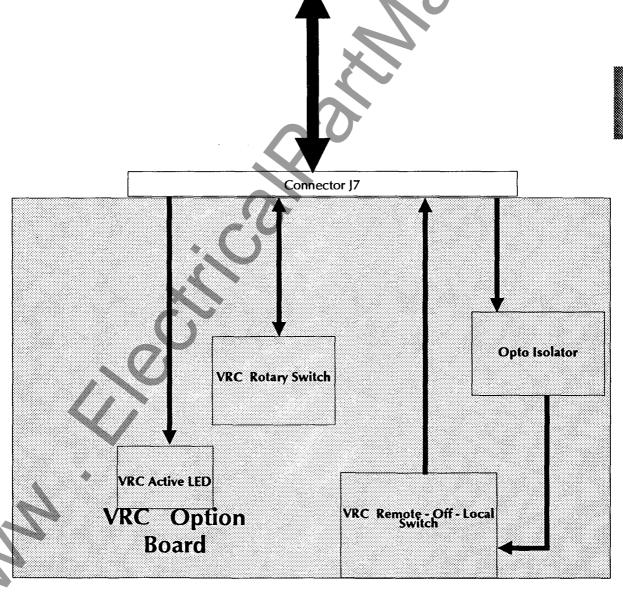
### APPENDIX B.4: Data/Pak Option





Interface PC Board

Connector J7



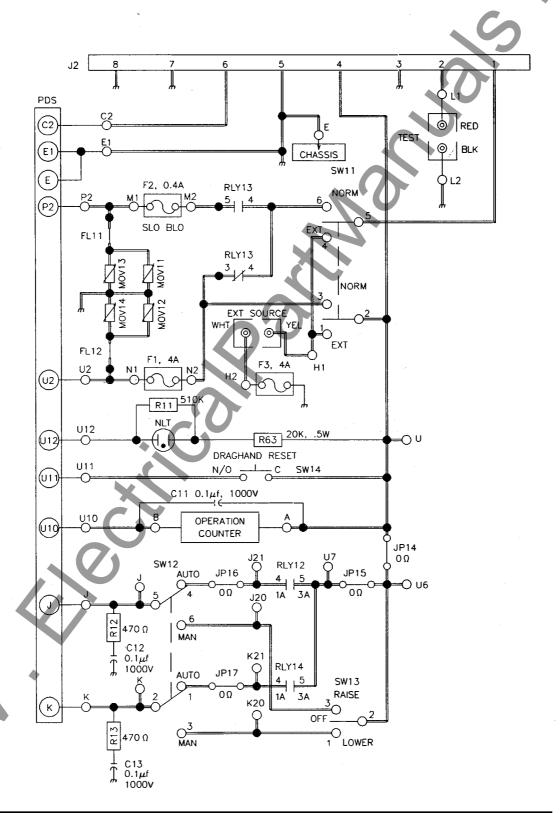
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APPENDIX C: Schematic Diagrams





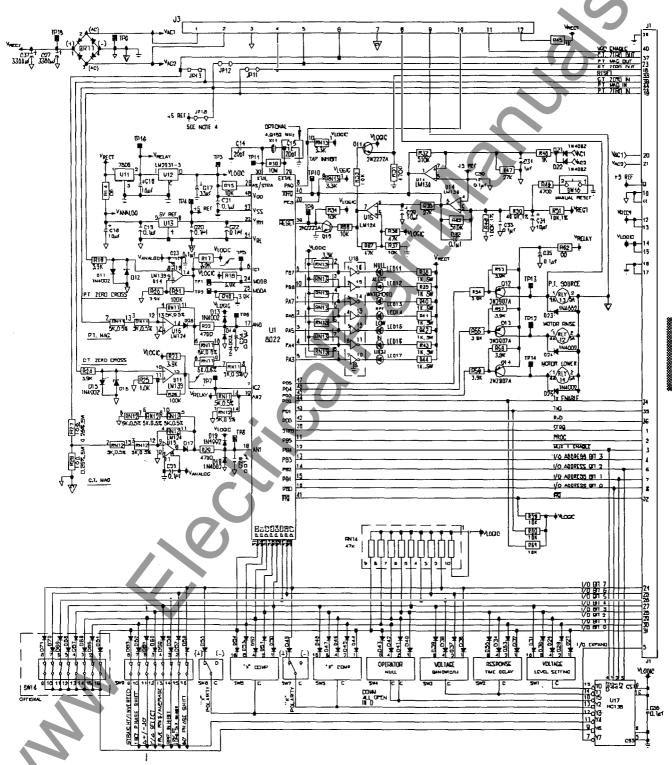
### APPENDIX C.1 (part 1): Control Panel PC Board (Electrical Portion)





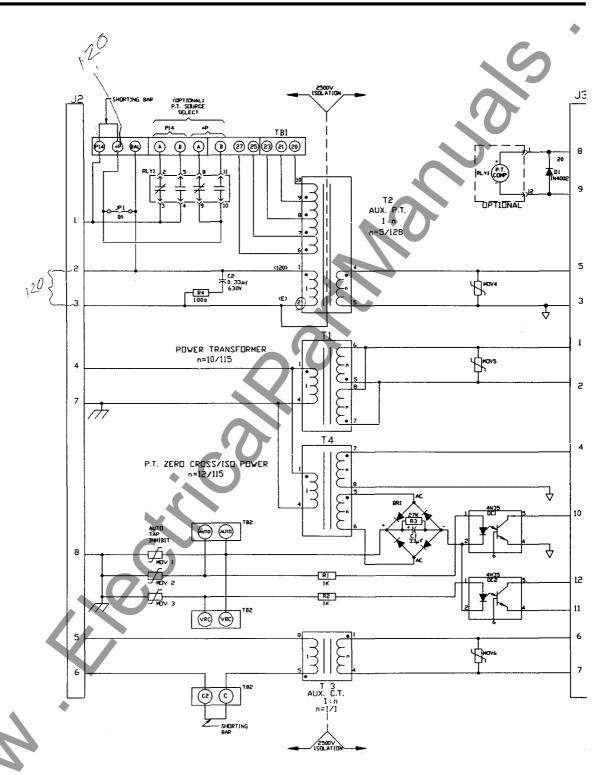
### **Appendix C: Schematics**

### APPENDIX C.1 (part 2): Control Panel PC Board (Electronic Portion)



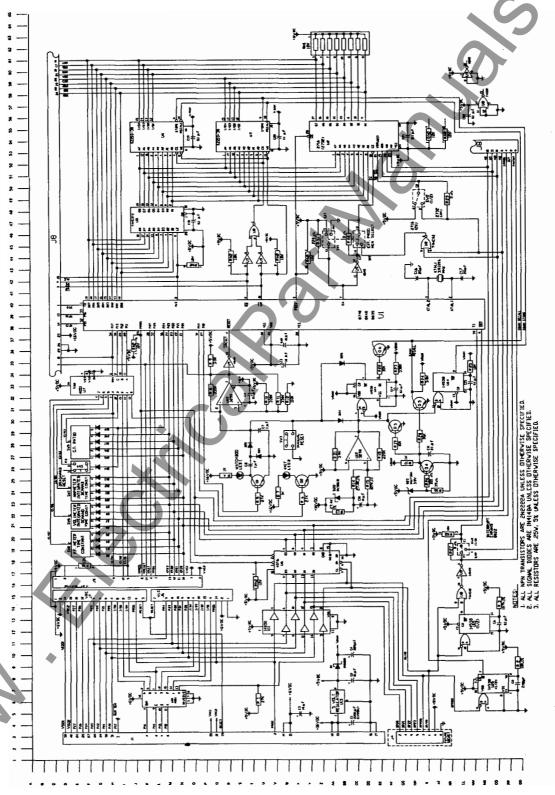


### **APPENDIX C.2: Transformer PC Board**

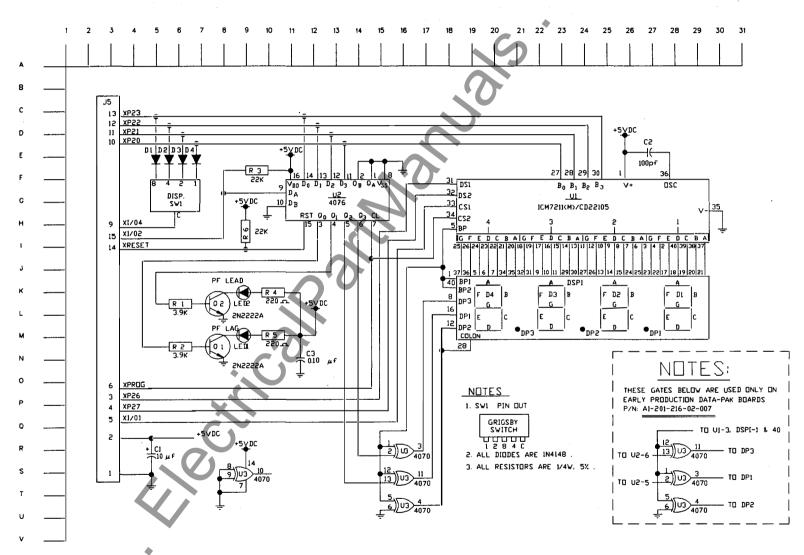


### **Appendix C: Schematics**

### **APPENDIX C.3: Interface PC Board Option**



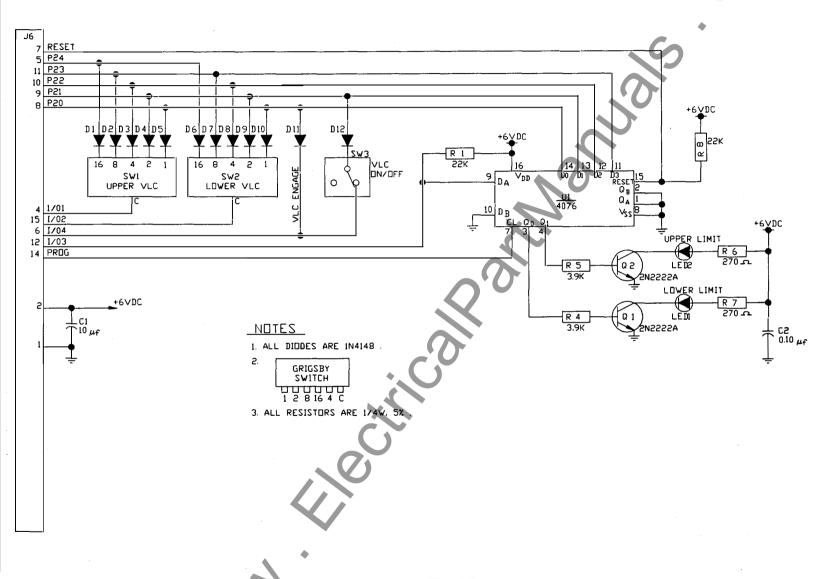
APPENDIX C.4: Data/Pak PC Board Option



## **Appendix C: Schematics**

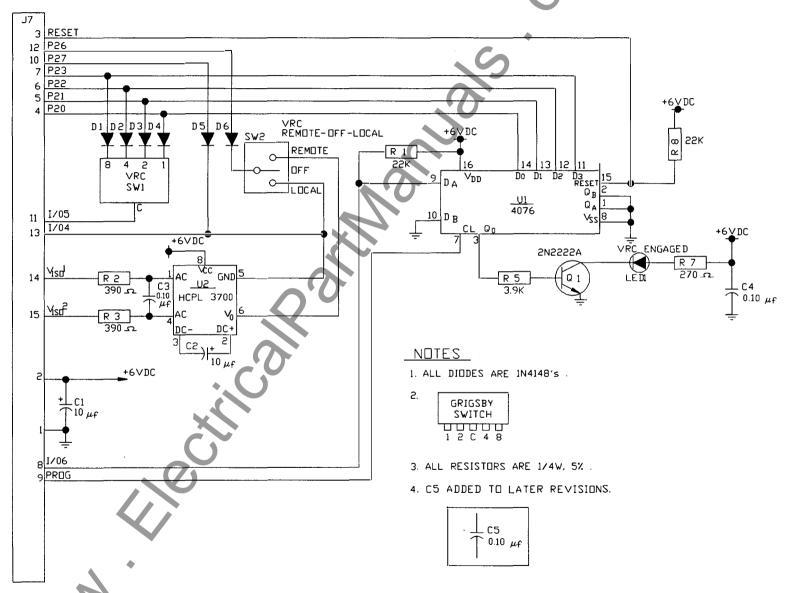
(Voltage

**Limit Control) PC Board Option** 



### Appendix C: Schematics





### APPENDIX D: Parts List

### APPENDIX D.1: Control Panel PC Board (1)

		Арреп	tix A1					
NO.	Circuit ID	Locato		COMPONENT	DESCRIPTION	DESCRIPTION 2	MISC.	PART NUMBER
		ROW	COL					
1	R11	19	]	ESISTOR	510K OHM	1/4 W, CARBON	5%	D1-RSC-ACN-138
2	R12	15	j	RESISTOR	470 OHM	1/4 W, CARBON	5%	D1-RSC-ACN-065
3	R13	15	J	RESISTOR	470 OHM	1/4 W, CARBON	5%	D1-RSC-ACN-065
4	R14	9	W	RESISTOR	ZERO OHM		-	D1-RS0-A00-001
5	R15	24	AA	RESISTOR	10K OHM	1/4 W, CARBON	5%	D1-RSC-ACN-097
6	R16	12	T	RESISTOR	3.9K OHM	1/4 W, CARBON	5%	D1-RSC-ACN-087
<i>7</i>	R17	12	S	RESISTOR	3.9K OHM	1/4 W, CARBON	5%	D1-RSC-ACN-087
8	R18	24	X	RESISTOR	3.9K OHM	1/4 W, CARBON	5%	D1-RSC-ACN-087
9	R19	24	Z	RESISTOR	3.9K OHM	1/4 W, CARBON	5%	D1-RSC-ACN-087
10	R20	12	R	RESISTOR	3.9K OHM	1/4 W, CARBON	5%	D1-RSC-ACN-087
11	R21	12	R	RESISTOR	100K OHM	1/4 W, CARBON	5%	D1-RSC-ACN-121
12	R22	20	S	RESISTOR	470 OHM	1/4 W, CARBON	5%	D1-RSC-ACN-065
13	R23	11	V	RESISTOR	3.9K OHM	1/4 W, CARBON	5%	D1-RSC-ACN-087
14	R24	15	S R	RESISTOR	3.9K OHM	1/4 W, CARBON	5%	D1-RSC-ACN-087
15 16	R25 R26	15 15	R	RESISTOR RESISTOR	1.0K OHM 100K OHM	1/4 W, CARBON 1/4 W, CARBON	5% 5%	D1-RSC-ACN-073
17	R27	6	R	RESISTOR	10.0 OHM	5W,WIRE WND	0.25%	D1-RSC-ACN-121 D1-RSH-AKF-001
18	R28	5	R	RESISTOR	10.0 OHM	5W,WIRE WND	0.25%	D1-RSH-AKF-001
19	R29	26	R	RESISTOR	470 OHM	1/4 W, CARBON	5%	D1-RSC-ACN-065
20	R30	21	ĀĀ	RESISTOR	10M OHM	1/4 W, CARBON	5%	D1-RSC-ACN-169
21	R31	24	ВВ	RESISTOR	470 OHM	1/4 W, CARBON	5%	D1-RSC-ACN-065
22	R32	12	P	RESISTOR	510K OHM	1/4 W, CARBON	5%	D1-RSC-ACN-138
23	R33	27	Z	RESISTOR	10K OHM	1/4 W, CARBON	5%	D1-RSC-ACN-097
24	R34	24	BB	RESISTOR	10K OHM	1/4 W, CARBON	5%	D1-RSC-ACN-097
25	R35	20	P	RESISTOR	27K OHM	1/4 W, CARBON	5%	D1-RSC-ACN-107
26	R36	22	S	RESISTOR	47K OHM	1/4 W, CARBON	5%	D1-RSC-ACN-113
27	R37	22	S	RESISTOR	10K OHM	1/4 W, CARBON	5%	D1-RSC-ACN-097
28	R38	32	Х	RESISTOR	1.0K OHM	1/2 W, CARBON	5%	D1-RSC-ADN-073
29	R39	3	AA	RESISTOR	1.0K OHM	1/2 W, CARBON	5%	D1-RSC-ADN-073
30	R40	3	AA	RESISTOR	1.0K OHM	1/2 W, CARBON	5%	D1-RSC-ADN-073
31	R41	3	CC	RESISTOR	1.0K OHM	1/2 W, CARBON	5%	D1-RSC-ADN-073
32	R42	31	AA	RESISTOR	1.0K OHM	1/2 W, CARBON	5%	D1-RSC-ADN-073
33	R43	31	CC	RESISTOR	1.0K OHM	1/2 W, CARBON	5%	D1-RSC-ADN-073
34	R44	31	DD	RESISTOR	1.0K OHM	1/2 W, CARBON	5%	D1-RSC-ADN-073
35	R45	3	T	RESISTOR	1.0K OHM	1/4 W, CARBON	5%	D1-RSC-ACN-073
36	R46	3	0	RESISTOR	1.0K OHM	1/4 W, CARBON	5%	D1-RSC-ACN-073
37	R47	15	Р	RESISTOR	27K OHM	1/4 W, CARBON	5%	D1-RSC-ACN-107
38	R48	15	0	RESISTOR	100K OHM	1/4 W, MET FILM	1%	D1-RSF-ACH-385
39	R49	31	AA	RESISTOR	470 OHM	1/4 W, CARBON	5%	D1-RSC-ACN-065
40	R50	15	0	RESISTOR	49.9K OHM	1/4 W, MET FILM	1%	D1-RSF-ACH-356
41	R51	32	Y	RESISTOR	10.0K OHM	1/4 W, MET FILM	1%	D1-RSF-ACH-289
42	R52	11	Y	RESISTOR	ZERO OHM	1/4 M/ CARROLL	- F0/	D1-RS0-A00-001
43	R53	12	W	RESISTOR	3.9K OHM	1/4 W, CARBON	5%	D1-RSC-ACN-087
44	R54	14	W	RESISTOR	3.9K OHM	1/4 W, CARBON	5%	D1-RSC-ACN-087
45	R55	14 14	X	RESISTOR	3.9K OHM	1/4 W, CARBON 1/4 W, CARBON	5%	D1-RSC-ACN-087
46 47	R56 R57	12	X X	RESISTOR RESISTOR	3.9K OHM 3.9K OHM		5% 5%	D1-RSC-ACN-087 D1-RSC-ACN-087
48	R58	12	X	RESISTOR	3.9K OHM	1/4 W, CARBON 1/4 W, CARBON	5%	D1-RSC-ACN-087
49	R59	15	BB	RESISTOR	10K OHM	1/4 W, CARBON	5%	D1-RSC-ACN-097
50	R60	15	AA	RESISTOR	10K OHM	1/4 W, CARBON	5%	D1-RSC-ACN-097
51	R61	15	AA	RESISTOR	10K OHM	1/4 W, CARBON	5%	D1-RSC-ACN-097
52	R62	12	P	RESISTOR	510K OHM	1/4 W, CARBON	5%	D1-RSC-ACN-138
53	R63	15	i	RESISTOR	20K OHM	1/2 W, CARBON	5%	D1-RSC-ADN-104
54	R66	27	AA	RESISTOR	10K OHM	1/4 W, CARBON	5%	D1-RSC-ACN-097
55	R67	23	P	RESISTOR	47K OHM	1/4 W, CARBON	5%	D1-RSC-ACN-113
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### APPENDIX D.1: Control panel PC Board - (2)

=									
			Appen	dix A1					
	NO.	Circuit ID	Locato		COMPONENT	DESCRIPTION	DESCRIPTION 2	MISC	PART NUMBER
			ROW	COL					
	56	JP11			RESISTOR	ZERO OHM	-	-	D1-RS0-A00-001
8	57	JP12			RESISTOR	ZERO OHM	_	-	D1-RS0-A00-001
ä	58	JP13	8	T	ESISTOR	ZERO OHM	-	-	D1-RS0-A00-001
	59	JP14	32	1	ESISTOR	ZERO OHM	-	- ( )	D1-RS0-A00-001
	60	JP15	32	1	ESISTOR	ZERO OHM	-	-	D1-RS0-A00-001
	61	JP16	32	J	ESISTOR	ZERO OHM	•		D1-RS0-A00-001
	62	JP17	32	J	ESISTOR	ZERO OHM		-	D1-RS0-A00-001
	63	JP19*			ESISTOR	ZERO OHM			D1-RS0-A00-001
	64	JP20*			ESISTOR	ZERO OHM		)	D1-RS0-A00-001
	65	RN11	8	Q	RES NETWRK	7 X 5.0K OHM	DIP	0.5%	D1-RSE-EAG-001
	66	RN12	27	Q	RES NETWRK	7 X 5.0K OHM	DIP	0.5%	D1-RSE-EAG-001
	67	RN13	14	U	RES NETWRK	9 X 3.3K OHM	SIP	2%	D1-RSF-FCJ-085
	68	RN14	19	AA	RES NETWRK	9 X 47K OHM	SIP	2%	D1-RSF-FCJ-113
	69	C11	21	Н	CAPACITOR	FILM	0.1MFD, 1000V		D1-CAF-CB0-L10
	70	C12	13	Н	CAPACITOR	FILM	0.1MFD, 1000V	-	D1-CAF-CB0-L10
- 100	71	C13	17	Н	CAPACITOR	FILM	0.1MFD, 1000V	-	D1-CAF-CB0-L10
	72	C14	22	AA	CAPACITOR	SILVER MICA	20PFD, 500V	-	D1-CRL-BTJ-R20
	73	C16	12	Z	CAPACITOR	TANTALUM	10 MFD, 25V	-	D1-CR2-CT1-J10
	74	C17	13	Z	CAPACITOR	TANTALUM	33MFD, 25V	-	D1-CR2-CT2-J33
	75	C18	8	W	CAPACITOR	TANTALUM	10 MFD, 25V		D1-CR2-CT1-J10
	76	C19	22	V	CAPACITOR	CERAMIC	0.1 MFD, 50V	-	D1-CRC-AW2-L10
	77	C20	22	X	CAPACITOR	CERAMIC	0.1 MFD, 50V	-	D1-CRC-AW2-L10
	78	C21	13	Υ	CAPACITOR	CERAMIC	0.1 MFD, 50V	-	D1-CRC-AW2-L10
٠	79	C22	20	Х	CAPACITOR	CERAMIC	0.1 MFD, 50V	-	D1-CRC-AW2-L10
	80	C23	10	R	CAPACITOR	CERAMIC	0.1 MFD, 50V	_	D1-CRC-AW2-L10
-	81	C24	20	S	CAPACITOR	FILM	0.01 MFD, 100V	-	D1-CRF-BD2-M10
	82	C25	20	Q	CAPACITOR	CERAMIC	0.1 MFD, 50V	-	D1-CRC-AW2-L10
	83	C26	25	Τ	CAPACITOR	FILM	0.01 MFD, 100V	-	D1-CRF-BD2-M10
	84	C27	2	W	CAPACITOR	ELECTROLYTIC	3300 MFD, 25V		D1-CRA-CT3-G33
5 P:	85	C29	22	T	CAPACITOR	TANTALUM	10 MFD, 25V	-	D1-CR2-CT1-J10
	86	C30	15	P	CAPACITOR	CERAMIC	0.1 MFD, 50V	-	D1-CRC-AW2-L10
8 1	87	C31	3	0	CAPACITOR	FILM	1.0 MFD, 100V	-	D1-CRF-BD6-K10
8 F:	88	C32	10	P	CAPACITOR	CERAMIC	0.1 MFD, 50V	-	D1-CRC-AW2-L10
•	89	C33	15	N	CAPACITOR	CERAMIC	0.1 MFD, 50V	-	D1-CRC-AW2-L10
	90	C34	28	X	CAPACITOR	TANTALUM	10 MFD, 25V	-	D1-CR2-CT1-J10
	91	C35	9	Υ	CAPACITOR	CERAMIC	0.1 MFD, 50V	-	D1-CRC-AW2-L10
	92	C36	27	Y	CAPACITOR	CERAMIC	0.1 MFD, 50V	-	D1-CRC-AW2-L10
- E	93	C37	5	Y	CAPACITOR	ELECTROLYTIC	3300 MFD, 25V	4) 14000	D1-CRA-CT3-G33
	94	D11	12	S	DIODE	RECTIFIER	100 PIV, 1 AMP	1N4002	D1-DDS-AB0-001
- B-	95	D12	12	T	DIODE	SCHOTIKY	30 PIV, 1 AMP	1N5818	D1-DDH-AA0-001
	96	D13	22	R	DIODE	RECTIFIER	100 PIV, 1 AMP	1N4002	D1-DDS-AB0-001
	97	D14 D15	22	R	DIODE	RECTIFIER	100 PIV, 1 AMP	1N4002	D1-DDS-AB0-001
	98		15	R		RECTIFIER	100 PIV, 1 AMP	1N4002	D1-DDS-AB0-001
	99	D16	15	S	DIODE	SCHOTTKY	30 PIV, 1 AMP	1N5818	D1-DDH-AA0-001
	100	D17	26	R S	DIODE	SMALL SIGNAL	100 PIV,0.2 AMP	1N4148	D1-DDF-AB0-001
ŀ	101 102	D18 D19	26 26	S	DIODE	RECTIFIER	100 PIV, 1 AMP	1N4002	D1-DD5-AB0-001
	103	D19	3	P	DIODE	RECTIFIER RECTIFIER	100 PIV, 1 AMP	1N4002 1N4002	D1-DDS-AB0-001 D1-DDS-AB0-001
	104	D21	3	P	DIODE	RECTIFIER	100 PIV, 1 AMP 100 PIV, 1 AMP	1N4002 1N4002	D1-DD5-AB0-001
	105	D23	10	P	DIODE	RECTIFIER	100 PIV, 1 AMP	1N4002 1N4002	D1-DD5-AB0-001
	106	D23	18	N	DIODE	RECTIFIER	100 PIV, 1 AMP	1N4002 1N4002	D1-DD5-AB0-001
	•	D25	10	0	DIODE	RECTIFIER	100 PIV, 1 AMP	1N4002 1N4002	D1-DD3-AB0-001
	108	D26	20	R	DIODE	SMALL SIGNAL	100 PIV,0.2 AMP	1N4148	
	109	D27	18	T	DIODE	SMALL SIGNAL	100 PIV,0.2 AMP	1N4148	D1-DDF-AB0-001 D1-DDF-AB0-001
	110	D28	18	T	DIODE	SMALL SIGNAL	100 PIV,0.2 AMP	1N4148	D1-DDF-AB0-001
98	111	D29	18	T	DIODE	SMALL SIGNAL	100 PIV,0.2 AMP	1N4148	D1-DDF-AB0-001



### **APPENDIX D.1: Control Panel PC Board - (3)**

		Appen	iix A1					
NO.	Circuit ID	Locato		COMPONENT	DESCRIPTION	DESCRIPTION 2	MISC.	PART NUMBER
		ROW	***************************************				4	
112	D30	18	S	DIODE	SMALL SIGNAL	100 PIV,0.2 AMP	1N4148	D1-DDF-AB0-001
113	D31	18	S	DIODE	SMALL SIGNAL	100 PIV,0.2 AMP	1N4148	D1-DDF-AB0-001
114	D32	29	T	DIODE	SMALL SIGNAL	100 PIV,0.2 AMP	1N4148	D1-DDF-AB0-001
115	D33	29	T	DIODE	SMALL SIGNAL	100 PIV,0.2 AMP	1N4148	D1-DDF-AB0-001
116	D34	29	S	DIODE	SMALL SIGNAL	100 PIV,0.2 AMP	1N4148	D1-DDF-AB0-001
117	D35	29	S	DIODE	SMALL SIGNAL	100 PIV,0.2 AMP	1N4148	D1-DDF-AB0-001
118	D36	8	R	DIODE	SMALL SIGNAL	100 PIV,0.2 AMP	1N4148	D1-DDF-AB0-001
119	D37	8	R	DIODE	SMALL SIGNAL	100 PIV,0.2 AMP	1N4148	D1-DDF-AB0-001
120	D38	8	R	DIODE	SMALL SIGNAL	100 PIV,0.2 AMP	1N4148	D1-DDF-AB0-001
121	D39	8	S	DIODE	SMALL SIGNAL	100 PIV,0.2 AMP	1N4148	D1-DDF-AB0-001
122	D40	29	Q	DIODE	SMALL SIGNAL	100 PIV,0.2 AMP	1N4148	D1-DDF-AB0-001
123	D41	29	Q	DIODE	SMALL SIGNAL	100 PIV,0.2 AMP	1N4148	D1-DDF-AB0-001
124	D42	29	Q	DIODE	SMALL SIGNAL	100 PIV,0.2 AMP	1N4148	D1-DDF-AB0-001
125	D43	29	Р	DIODE	SMALL SIGNAL	100 PIV,0.2 AMP	1N4148	D1-DDF-AB0-001
126	D44	8	Р	DIODE	SMALL SIGNAL	100 PIV,0.2 AMP	1N4148	D1-DDF-AB0-001
127	D45	8	Q	DIODE	SMALL SIGNAL	100 PIV,0.2 AMP	1N4148	D1-DDF-AB0-001
128	D46	8	Q	DIODE	SMALL SIGNAL	100 PIV,0.2 AMP	1N4148	D1-DDF-AB0-001
129	D47	8	Q	DIODE	SMALL SIGNAL	100 PIV,0.2 AMP	1N4148	D1-DDF-AB0-001
130	D48	8	Q	DIODE	SMALL SIGNAL	100 PIV,0.2 AMP	1N4148	D1-DDF-AB0-001
131	D49	8	P	DIODE	SMALL SIGNAL	100 PIV,0.2 AMP	1N4148	D1-DDF-AB0-001
132	D50	29	L	DIODE	SMALL SIGNAL	100 PIV,0.2 AMP	1N4148	D1-DDF-AB0-001
133	D51	29	L	DIODE	SMALL SIGNAL	100 PIV,0.2 AMP	1N4148	D1-DDF-AB0-001
134	D52	29	L	DIODE	SMALL SIGNAL	100 PIV,0.2 AMP	1N4148	D1-DDF-AB0-001
135	D53	29	K	DIODE	SMALL SIGNAL	100 PIV,0.2 AMP	1N4148	D1-DDF-AB0-001
136	D54	29	K	DIODE	SMALL SIGNAL	100 PIV,0.2 AMP	1N4148	D1-DDF-AB0-001
137	D55	18	Ō	DIODE	SMALL SIGNAL	100 PIV,0.2 AMP	1N4148	D1-DDF-AB0-001
138	D56	32	М	DIODE	SMALL SIGNAL	100 PIV,0.2 AMP	1N4148	D1-DDF-AB0-001
139	D57	32	L	DIODE	SMALL SIGNAL	100 PIV,0.2 AMP	1N4148	D1-DDF-AB0-001
140	D58	32	Ĺ	DIODE	SMALL SIGNAL	100 PIV,0.2 AMP	1N4148	D1-DDF-AB0-001
141	D59	32	L	DIODE	SMALL SIGNAL	100 PIV,0.2 AMP	1N4148	D1-DDF-AB0-001
142	D60	32	K	DIODE	SMALL SIGNAL	100 PIV,0.2 AMP	1N4148	D1-DDF-AB0-001
143	D61	32	K	DIODE	SMALL SIGNAL	100 PIV,0.2 AMP	1N4148	D1-DDF-AB0-001
144	D62	32	K	DIODE	SMALL SIGNAL	100 PIV,0.2 AMP	1N4148	D1-DDF-AB0-001
145	D63	32	K	DIODE	SMALL SIGNAL	100 PIV,0.2 AMP	1N4148	D1-DDF-AB0-001
146	D63	32	T	DIODE	SMALL SIGNAL	100 PIV,0.2 AMP	1N4148	D1-DDF-AB0-001
**********		32	T					
147	D65	32	S	DIODE	SMALL SIGNAL SMALL SIGNAL	100 PIV,0.2 AMP	1N4148	D1-DDF-AB0-001
148	D66		S			100 PIV,0.2 AMP	1N4148	D1-DDF-AB0-001
149 150	D67	32 32	S S	DIODE	SMALL SIGNAL SMALL SIGNAL	100 PIV,0.2 AMP	1N4148	D1-DDF-AB0-001 D1-DDF-AB0-001
151	D68	32	5			100 PIV,0.2 AMP	1N4148	
	D69 D70	32		DIODE DIODE	SMALL SIGNAL SMALL SIGNAL	100 PIV,0.2 AMP	1N4148 1N4148	D1-DDF-AB0-001 D1-DDF-AB0-001
153	D70	32	P		SMALL SIGNAL	100 PIV,0.2 AMP 100 PIV,0.2 AMP	1N4148	D1-DDF-AB0-001
154	LED11	32	W	DIODE LED	RED, RIGHT ANGLE	TOU FIV,U.Z AMP	1194140	D1-DD1-A80-001
B-++++++++++++++++++++++++++++++++++++	LED11	3	BB	LED	RED, HI INTENSITY	-	-	D1-100-024-001
155		3	DD			-		D1-100-024-001
156	LED13	3	CC	LED	YEL, HI INTENSITY RED, HI INTENSITY	-	-	D1-100-024-002
157	LED14	31		LED		-	-	
158	LED15	<del>+</del>	BB	LED	RED, HI INTENSITY	-	-	D1-100-024-001
159	LED16	31	CC	LED	RED, HI INTENSITY	-	·	D1-100-024-001
160	LED17	31	DD	LED	RED, HI INTENSITY	100 BIV 2 ALAB	-	D1-100-024-001
161	BR11	4	R	IC MOV	BRIDGE RECTIFIER	100 PIV, 2 AMP	-	D1-RES-L00-001
167	MOV11	23	J	MOV	SURGE PROTECTOR	150 VRMS 150 VRMS	-	D1-SUM-V00-005
163	MOV12	24	<del>  </del>	MOV	SURGE PROTECTOR		-	D1-SUM-V00-005
164	MOV13	25	<del>  </del>	MOV	SURGE PROTECTOR	150 VRMS	-	D1-SUM-V00-005
165	MOV14	26	1	MOV	SURGE PROTECTOR	150 VRMS	- ANI 2222 A	D1-SUM-V00-005
166	Q11	24	CC	TRANSISTOR	NPN	-	2N2222A	D1-TSS-NPA-001
167	Q12	10	Х	ANSISTOR	PNP	l	2N2907A	D1-TSS-PPB-001



### APPENDIX D.1: Control Panel PC Board - (4)

		*********						
		Appen	dix A1					
NO.	Circuit ID	Locato		COMPONENT	DESCRIPTION	DESCRIPTION 2	MISC.	PART NUMBER
		ROW						F - 2 F
168	Q13	10	Y	ANSISTOR	PNP	-	2N2907A	D1-TSS-PPB-001
169	Q14	10	Z	ANSISTOR	PNP	•	2N2907A	D1-TSS-PPB-001
170	Q15	26	AA	ANSISTOR	NPN	-	2N2222A	D1-TSS-NPA-001
171	U11	6	ВВ	IC	VOLTAGE REG	+6 VOLT	7806	D1-ICL-GV0-002
1772	U12	3	BB	IC .	VOLTAGE REG	+5 VOLT	2930	D1-ICL-GL0-001
173	U13	22	W	IC	VOLTAGE REF	+5 VOLT	REF02	D1-100-024-025
174	U14	12	Q_	IC	QUAD COMPARITOR	•	139	D1-ICL-BD0-001
175	U15	22	Q	IC	QUAD OP AMP		124	D1-ICL-AD0-001
176	U16	18	Υ	IC	MICROPROCESSOR	-	68HC11E2P	D1-100-021-517
177	U17	25	Υ	IC	DEMULTIPLEXER	-	74HC138	D1-ICD-HL0-003
178	U18	14	V	IC	TRANSISTOR ARRAY	7 NPN	DARLING.	D1-TSD-NDA-001
179	X11	22	BB	CRYSTAL	-	4.9152 MHZ	-	D1-CYS-000-001
180	SW1	19	V	SWITCH	BCD	29 POSITIONS	WHT DOT	D1-100-024-010
181	SW2	29	V	SWITCH	BCD	15 POSITIONS	RED DOT	D1-100-024-006
182	SW3	6	V	SWITCH	BCD BIGUT ANGLE	11 POSITIONS	YEL DOT	D1-100-024-007
183	SW4	33	Q	SWITCH	BCD, RIGHT ANGLE	16 POSITIONS	COLLDOT	D1-SWR-T00-004
184	SW5	6	N	SWITCH	BCD	25 POSITIONS	GRN DOT	D1-100-024-012
185	SW6 SW7	29 13	Z	SWITCH SWITCH	BCD TOGGLE	25 POSITIONS SPDT	GRN DOT	D1-100-024-012 D1-SWT-P01-001
186 187	SW8	22	N	SWITCH	TOGGLE	SPDT	-	D1-SWT-P01-001
0.0000000	SW9	32	N	SWITCH	DIP ROCKER	8 POSITIONS	PIANO STY	D1-SWD-R00-002
188	SW10	31	Z	SWITCH	PUSHBUTTON	SPDT, RT ANG	-	D1-SWP-B00-005
190	SW11	4	G	SWITCH	TOGGLE	DPDT, C.O.		D1-SWT-P02-003
191	SW12	15	G	SWITCH	TOGGLE	DPDT, C.O.		D1-SWT-P02-003
192	SW13	11	G	SWITCH	TOG MOMENTARY	SPDT, C.O.		D1-SWT-P01-003
193	SW14	19	G	SWITCH	PUSHBUTTON	SPDT	-	D1-SWP-B00-004
194	RLY12A*	19	L	RELAY	SPDT PC BD MT	6 VDC COIL	_	D1-RLM-N00-004
195	RLY13A*	8	ī	RELAY	SPDT PC BD MT	6 VDC COIL	-	D1-RLM-N00-004
196	RLY14A*	15	Ĺ	RELAY	SPDT PC BD MT	6 VDC COIL	-	D1-RLM-N00-004
197	RLY12#	18	·L	RELAY	SPDT	6 VDC COIL	-	D1-RLG-PS0-001
198	RLY13#	11	L	RELAY	SPDT	6 VDC COIL	-	D1-RLG-PS0-001
199	RLY14#	14	L	RELAY	SPDT	6 VDC COIL	-	D1-RLG-PS0-001
200	RLY12#	18	L	RETAINER	FOR RELAYS	-	-	D1-RLA-C00-001
201	RLY13#	11	L	RÉTAINER	FOR RELAYS	-	-	D1-RLA-C00-001
202	RLY14#	14	L	RETAINER	FOR RELAYS		-	D1-RLA-C00-001
203	NLT	19	I	SOCKET	FOR BI-PIN LAMPS	•	-	D1-SKL-P00-001
204	NLT	19	1	LAMP	NEON, AMBER CAP	BI-PIN	-	D1-LBN-E00-001
205	F3	8	D	FUSE	4 AMP, 125 VOLT	AGX4	-	D1-FSG-FB0-001
206	F3	9	D	FUSE CLIP	PC BD MT	1/4" DIA FUSE	(2 REQ'D)	D1-FHC-PA0-001
207	FL11	22	F	WIRE	FUSIBLE LINK	30 AWG SOLID	1.2" LONG	D1-WGP-K30-007
.00000000000	FL12	23	F	WIRE	FUSIBLE LINK	30 AWG SOLID	1.2" LONG	D1-WGP-K30-007
209	J2	2		FLAT CABLE	8 COND. + HEADER	1-		D1-100-024-003
210	J3	2	R	FLAT CABLE	12 COND. + HEADER	·	-	D1-100-024-004
211	ļ	X		HEATSINK	FOR TO-3 DEVICES	-	-	D1-HSH-P00-002
212	<del>-</del>		V-	NUT	HEX	#6-32	(2 REQ'D)	00-631-133-040
213	-	<del> </del>	ļ <u>.                                    </u>	LOKWASHER	INTERNAL TOOTH	#6	(2 REQ'D)	00-655-047-060
214	RLY12#	18	L	SOCKET	RELAY	-	-	D1-SKR-L00-002
215	RLY13#	10	L	SOCKET	RELAY		-	D1-SKR-L00-002
216	RLY14#	14	L	SOCKET	RELAY	40 DIN DID	ļ <del>-</del>	D1-SKR-L00-002
217	U16	18	Υ	SOCKET	INTEGRATED CIRCUIT	48 PIN DIP		D1-SKC-K00-002

<sup>\* =</sup> BOARD WITH RELAYS ON COMPONENT SIDE.. # = BOARD WITH RELAYS ON SOLDER SIDE. BEGAN WITH S/N mj303S - 30000.



### **APPENDIX D.2: Transformer PC Board**

		Appendi	. All			Discountries:	4	
NO.	Circuit ID	Locator ROW	COL	COMPONENT	DESCRIPTION	DESCRIPTION 2	MISC.	PART NUMBER
1	R1	24	ı	RESISTOR	1.0K OHM	1/4W, CARBON	5%	D1-RSC-ACN-073
2	R2	24	1	RESISTOR	1.0K OHM	1/4W, CARBON	5%	D1-RSC-ACN-073
3	R3	21	S	RESISTOR	27K OHM	1/4W, CARBON	5%	D1-RSC-ACN-107
4	R4	35	K	RESISTOR	100 OHM	1/4W, CARBON	5%	D1-RSC-ACN-049
ς	JP1	32	K	REISITOR	ZERO OHM	-		D1-RS0-A00-001
6	C1	20	S	CAPACITOR	TANTALUM	33 MFD, 25V		D1-CR2-CT2-J33
7	C2	32	N	CAPACITOR	FILM	0.33 MFD, 630V	-	D1-CAF-BX0-L33
8	D1	38	T	DIODE	RECTIFIER	100 PIV, 1A	1N4002	D1-DDS-AB0-001
9	MOV1	10	K	MOV	SURGE PROTECTOR	150 VRMS	-	D1-SUM-V00-005
10	MOV2	14	i	MOV	SURGE PROTECTOR	150 VRMS	-	D1-SUM-V00-005
11	MOV3	14	ĸ	MOV	SURGE PROTECTOR	150 VRMS	-	D1-SUM-V00-005
12	MOV4	31	S	MOV	SURGE PROTECTOR	25 VRMS	  -	D1-SUM-V00-003
13	MOV5	21	R	MOV	SURGE PROTECTOR	25 VRMS	_	D1-SUM-V00-003
14	MOV6	10	S	MOV	SURGE PROTECTOR	25 VRMS	_	D1-SUM-V00-003
15	BR1	17	S	IC	BRIDGE RECTIFIER	100 PIV, 1A	-	D1-RES-LD0-001
16	OC1	28	1	IC	OPTO ISOLATOR		4N35	D1-IST-R00-002
17	OC2	30	1	IC	OPTO ISOLATOR	7	4N35	D1-IST-R00-002
18	T1	26	N	TRANSFORMER	POWER	_	-	D1-100-024-016
19	T2	38	0	TRANSFORMER	P.T. AUX	_	_	D1-100-024-015
20	Т3	10	N	TRANSFORMER	C.T. AUX	-	-	D1-100-024-014
21	T4	18	N	TRANSFORMER	-P.T. ZERO, ISO POWER	-		D1-100-024-013
22	RLY1	46	N	SOCKET	FOR RELAY	_	-	D1-SKR-L00-001
23	J2	14	S	HEADER	DIPSTRIP, 8 POSITION	-	_	D1-CNM-S00-002
24	<u>J3</u>	27	S	HEADER	DIPSTRIP, 12 POSITION	_		D1-CNM-S00-003
25	TB1	40	i	TERM. STRIP	3 POSITION		(4 REQ'D)	D1-TBM-B00-006
26	TB2	20	ĺ	TERM. STRIP	3 POSITION	-	(2 REQ'D)	D1-TBM-B00-006
27	-			SHORTING BAR	-	-	FOR C-C2	D1-TBA-000-003
28	-			STANDOFF	SWAGED, 0.75 LG	-	(6 REQ'D)	D1-HSC-000-011
29	-	1		BRACKET	TRANSFORMER	-	FOR T2	D1-HMB-T00-001
30	-			SCREW	ROUND HEAD	#4-40 X 1.50	(6 REQ'D)	00-615-471-086
31	-			WASHER	FLAT	#4	(6 REQ'D)	00-651-007-042
32	-			WASHER	INSULATING	NYLON #4	(8 REQ'D)	D1-HFW-00N-008
33	-			LOCKWASHER	INTERNAL TOOTH	#4	(6 REQ'D)	00-655-047-040
34	-	1		NUT	HEX	#4-40	(6 REQ'D)	00-631-109-104
35	-			SCREW	ROUND HEAD	#6-32 X 0.50	(4 REQ'D)	00-615-471-124
36	-			WASHER	FLAT	#6	(4 REQ'D)	00-651-007-059
37	-			LOCKWASHER	INTERNAL TOOTH	#6	(4 REQ'D)	00-655-047-060
38	-			NUT	HEX	#6-32	(4 REQ'D)	00-631-109-106

### **Appendix D: Parts List**

### APPENDIX D.3: Interface PC Board Option- (1)

NO.	CIRCUIT ID		ATOR COL	COMPONENT	DESCRIPTION	DESCR. 2	MISC.	PART NUMBER
	200000000000000000000000000000000000000		2222222222			×.		
1 2	R1 R2	T Q	10 11	RESISTOR RESISTOR	27K OHM 10K OHM	1/4W, CARBON 1/4W, M.F.	5% 1%	D1-RSC-ACN-107 D1-RSF-ACH-289
3 4 5	R3 R4 R5	R L L	11 23 22	RESISTOR RESISTOR RESISTOR	107K OHM 1.0K OHM 27K OHM	1/4W, M.F. 1/4W, CARBON 1/4W, CARBON	1% 5% 5%	D1-RSF-ACH-388 D1-RSC-ACN-073 D1-RSC-ACN-107
6	R6	L	21	RESISTOR	27K OHM	1/4W, CARBON	5%	D1-RSC-ACN-107
7 8 9	R7 R8 R9	M J	23 23 23	RESISTOR RESISTOR RESISTOR	1.0K OHM 330K OHM 3.9K OHM	1/4W, CARBON 1/4W, CARBON 1/4W, CARBON	5% 5% 5%	D1-RSC-ACN-073 D1-RSC-ACN-133 D1-RSC-ACN-087
10	R10	Ĺ	23	RESISTOR	330K OHM	1/4W, CARBON	5%	D1-RSC-ACN-133
11 12 13	R11 R12 R13	K K M	23 23 20	RESISTOR RESISTOR RESISTOR	330K OHM 110K OHM 27.4K OHM	1/4W, CARBON 1/4W, CARBON 1/4W, M.F.	5% 5% 1%	D1-RSC-ACN-133 D1-RSC-ACN-122 D1-RSF-ACH-331
14 15	R14 R15	K K	19 20	RESISTOR RESISTOR	27.4K OHM 107K OHM	1/4W, M.F. 1/4W, M.F.	1% 1%	D1-RSF-ACH-331 D1-RSF-ACH-388
16 17	R16 R17	I G	23 22	RESISTOR RESISTOR	39 OHM 1.0K OHM	1/4W, CARBON 1/4W, CARBON	5% 5%	D1-RSC-ACN-039 D1-RSC-ACN-073
18 19	R18 R19	K H	20 22	RESISTOR RESISTOR	220K OHM 10K OHM	1/4W, CARBON 1/4W, CARBON	5% 5%	D1-RSC-ACN-129 D1-RSC-ACN-097
20 21	R20 R21	G	22 19	RESISTOR RESISTOR	10K OHM 3.9K OHM	1/4W, CARBON 1/4W, CARBON	5% 5%	D1-RSC-ACN-097 D1-RSC-ACN-087
22 23	R22 R23	H	19 18	RESISTOR RESISTOR	10K OHM 330K OHM	1/4W, CARBON 1/4W, CARBON	5% 5%	D1-RSC-ACN-097 D1-RSC-ACN-133
24 25	R24 R25	H	19 22	RESISTOR RESISTOR	3.9K OHM 10K OHM	1/4W, CARBON 1/4W, CARBON	5% 5%	D1-RSC-ACN-087 D1-RSC-ACN-097
26 27	R26 R27	l G	24 10	RESISTOR RESISTOR	100 OHM ZERO OHM	1/4W, CARBON -	5% -	D1-RSC-ACN-049 D1-RS0-A00-001
28 29 30	R28 R29 R30	G G	12 10 12	RESISTOR RESISTOR RESISTOR	ZERO OHM ZERO OHM 220 OHM	- 1/4W, CARBON	- 5%	D1-RS0-A00-001 D1-RS0-A00-001 D1-RSC-ACN-057
31	RN1	P G	2	RES NETWORK RES NETWORK	9 x 12.0K OHM	SIP	2% 2%	D1-RSF-FCJ-099 D1-RSF-FCJ-099
32 33 34	RN2 C1 C2	N M	2 17 18	CAPACITOR CAPACITOR	9 x 12:0K OHM ELECTROLYTIC TANTALUM	SIP 220 MFD, 25V 10 MFD, 25V	270 -	D1-CRA-CT2-H22 D1-CR2-CT1-J10
35	C3 C4	S	16 15	CAPACITOR CAPACITOR	TANTALUM	10 MFD, 25V	-	D1-CR2-CT1-J10 D1-CAA-CT0-G22
36 37 38	C5 C6	M Q T	11 11	CAPACITOR CAPACITOR	ELECTROLYTIC SILVER MICA CERAMIC	2200 MFD, 25V 2700 PFD, 500V 0.1 MFD, 50V	5% 10%	D1-CRL-BTJ-N27 D1-CRC-AW2-L10
39 40	C7 C8	M M	24 26	CAPACITOR CAPACITOR	FILM FILM	1.0 MFD, 100V 1.0 MFD, 100V		D1-CRF-BD6-K10 D1-CRF-BD6-K10
41 42	C9 C10	K L	22 18	CAPACITOR CAPACITOR	CERAMIC TANTALUM	0.1 MFD, 25VDC 10 MFD, 25V	20%	A1-CRC-LHW-M01 D1-CR2-CT1-J10
43 44 45	C11 C12 C13	F M N	23 12 13	CAPACITOR CAPACITOR CAPACITOR	CERAMIC CERAMIC TANTALUM	0.1 MFD, 25VDC 0.1 MFD, 25VDC 10 MFD, 25V	20% 20%	A1-CDC-LHW-M01 A1-CDC-LHW-M01 D1-CR2-CT1-J10
46	C14	G	19	CAPACITOR	CERAMIC	0.1 MFD, 50V	10%	D1-CRC-AW2-L10
47 48 49	C15 C16 C17	G I I	21 12 13	CAPACITOR CAPACITOR CAPACITOR	CERAMIC SILVER MICA SILVER MICA	0.1 MFD, 50V 20 PFD, 500V 20 PFD, 500V	10%	D1-CRC-AW2-L10 D1-CDF-XEG-H02 D1-CDF-XEG-H02
50	C18	ĸ	5	CAPACITOR	CERAMIC	0.1 MFD, 25VDC	20%	A1-CDC-LHW-M01
	000000000000000000000000000000000000000					**		

### APPENDIX D.3: Interface PC Board Option- (2)

NO	. CIRCUIT		IDIX A	COMPONENT	DESCRIPTION	DESCR. 2	MISC.	PART NUMBER
	ID			COMPONENT	DESCRIPTION	HR.L.	MISC.	FAAT NUMBER
		ROW	COL					
	-00400000000000000000000000000000000000		5000000000000000					
51	C19	D	5	CAPACITOR	CERAMIC	0.1 MED 25 MDC	200	A1-CDC-LHW-M01
52	C20	Ĺ	5	CAPACITOR	CERAMIC	0.1 MFD, 25VDC 0.1 MFD, 25VDC	20% 20%	A1-CDC-LHW-M01
53	C21	С	6	CAPACITOR	CERAMIC	0.1 MFD, 25VDC	20%	A1-CDC-LHW-M01
54	C22	D	11	CAPACITOR	CERAMIC	0.1 MFD, 25VDC	20%	A1-CDC-LHW-M01
55	D1	N	19	DIODE	SCHOTTKY	30 PIV, 1 AMP	1N5818	D1-DDH-AA0-001
56	D2	K	17	DIODE	SMALL SIGNAL	100 PIV, 0.2 AMP	1N4148	D1-DDF-AB0-001
57	D3	K	16	DIODE	SMALL SIGNAL	100 PIV, 0.2 AMP	1N4148	D1-DDF-AB0-001
58	D4	K	17	DIODE	SMALL SIGNAL	100 PIV, 0.2 AMP	1N4148	D1-DDF-AB0-001
59 60	D5 <b>D6</b>	J I	16 17	DIODE DIODE	SMALL SIGNAL SMALL SIGNAL	100 PIV, 0.2 AMP	1N4148 1N4148	D1-DDF-AB0-001 D1-DDF-AB0-001
00		,		DIODE	SIVINEL SICINAL	100 PIV, 0.2 AMP	1114140	ו יייייייייייייייייייייייייייייייייייי
61	D7	1	16	DIODE	SMALL SIGNAL	100 PIV, 0.2 AMP	1N4148	D1-DDF-AB0-001
62	D8	!	17	DIODE	SMALL SIGNAL	100 PIV, 0.2 AMP	1N4148	D1-DDF-AB0-001
63 64	D9 D10	l H	16 17	DIODE DIODE	SMALL SIGNAL	100 PIV, 0.2 AMP	1N4148	D1-DDF-AB0-001
65	D11	H	16	DIODE	SMALL SIGNAL SMALL SIGNAL	100 PIV, 0.2 AMP 100 PIV, 0.2 AMP	1N4148 1N4148	D1-DDF-AB0-001 D1-DDF-AB0-001
					J. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1.	1001117, 0.2711711		B. BB. 7.B0 001
66		G	17	DIODE	SMALL SIGNAL	100 PIV, 0.2 AMP	1N4148	D1-DDF-AB0-001
67 68	D13 D14	G F	16 2	DIODE DIODE	SMALL SIGNAL	100 PIV, 0.2 AMP	1N4148	D1-DDF-AB0-001
69	D14 D15	F	17	DIODE	SMALL SIGNAL SMALL SIGNAL	100 PIV, 0.2 AMP 100 PIV, 0.2 AMP	1N4148 1N4148	D1-DDF-AB0-001 D1-DDF-AB0-001
70	D16	F	16	DIODE	SMALL SIGNAL	100 PIV, 0.2 AMP	1N4148	D1-DDF-AB0-001
		_		DIODE		,		
71 72	D17 D18	E E	1 <i>7</i> 16	DIODE DIODE	SMALE SIGNAL	100 PIV, 0.2 AMP	1N4148	D1-DDF-AB0-001
73	D19	E	1 <i>7</i>	DIODE	SMALL SIGNAL SMALL SIGNAL	100 PIV, 0.2 AMP 100 PIV, 0.2 AMP	1N4148 1N4148	D1-DDF-AB0-001 D1-DDF-AB0-001
74		ī	25	DIODE	SMALL SIGNAL	100 PIV, 0.2 AMP	1N4148	D1-DDF-AB0-001
<sub>*</sub> 75	D21	J	25	DIODE	SMALL SIGNAL	100 PIV, 0.2 AMP	1N4148	D1-DDF-AB0-001
76	D22	М	20	DIODE	CHOTTKY	20 DIV 1 4 4 4 D	*******	D1 DDU 440.001
77	D22	H	20 22	DIODE	SCHOTTKY ZENER	30 PIV, 1 AMP 3.9V, 5%	1N5818 1N4730A	D1-DDH-AA0-001 D1-DDZ-AA0-004
78	and the second second second second	ı	21	DIODE	SMALL SIGNAL	100 PIV, 0.2 AMP	1N4148	D1-DDF-AB0-001
79	D25	1	20	DIODE	SMALL SIGNAL	100 PIV, 0.2 AMP	1N4148	D1-DDF-AB0-001
§ 80	LED1	М	25	LED	RED, HI INTENSITY	-	-	A1-100-024-001
81	LED2	N	23	LED	RED, HI INTENSITY	_		A1-100-024-001
82	Q1	М	24	TRANSISTOR	NPN	-	2N2222A	D1-TSS-NPA-001
83	Q2	М	22	TRANSISTOR	NPN	-	2N2222A	D1-TSS-NPA-001
84 85		l H	21 23	TRANSISTOR TRANSISTOR	NPN	-	2N2222A	D1-TSS-NPA-001
03	ν,,	" /		INANSISTOR	NPN	-	2N2222A	D1-TSS-NPA-001
86		E	22	TRANSISTOR	NPN	<u>.</u>	2N2222A	D1-TSS-NPA-001
87			18	TRANSISTOR	NPN	-	2N2222A	D1-TSS-NPA-001
88 89		H	10 5	IC IC	MICROPROCESSOR EPROM 4K		80 <del>33</del>	D1-100-024-031 D1-100-021-512
90	343404040404040404040404040404040404040	L	• 5	IC	EE PROM	PROGRAMMED 64 x 4	MPAK04.01	D1-100-021-312 D1-1CM-GC0-002
		K				0424	2210	2 · · · · · · · · · · · · · · · · · · ·
91		E	5	IC IC	EE PROM	64 x 4		D1-ICM-GC0-002
92 93	300000000000000000000000000000000000000	H	5 10	IC IC	OCTAL LATCH QUAD D REGISTER	•	2210 74HC373	D1-ICD-FC0-001 D1-ICD-MC0-001
94	**************************************	ŏ	12	iC	MULTIPLEXER	•	4076B	D1-ICL-FC0-001
95	U8 **	D	10	IC	QUAD 2 INPUT NOR	-	4051B	D1-ICD-DC0-002
-00	۸.,	_	44	ıc	CIPALA DIFFER		74HC02	D1 ICD FC2 221
96 97		D E	12 25	IC IC	HEX INVERTER 8 CHANNEL MUX	-	4049UB	D1-ICD-EC0-001 D1-ICM-FC0-001
98		Ť	12	iC	HEX BUFFER	•	40490B 4051B	D1-ICD-EC0-002
99	U12	Ţ	20	IC	DUAL COMPARATOR	-	4050B	D1-ICL-BW0-001
100	) U13	Р	19	IC	VOLT REGULATOR	5 VOLT	CA3290	D1-ICL-GX0-003
							323	
	2 200 0 000 00 00 00 00 00 00 00					•		

### **Appendix D: Parts List**

### APPENDIX D.3: Interface PC Board Option- (3)

NO.	CIRCUIT	roc	ATOR	COMPONENT	DESCRIPTION	DESCR. 2	MISC.	PART NUMBER
******		8.1.244.8	COL					
				_				
101	U14	F	20	IC	MULTIVIBRATOR	MONOSTABLE	4538B	D1-ICD-JC0-001
102	U15	R	13	IC CDVCTAL	MULTIVIBRATOR	MONOSTABLE	45388	D1-ICD-JC0-001
103	XTAL1	Н	13	CRYSTAL	OUGLI DUTTOU	3.93216 MHZ	-	D1-CYS-000-003
104	SW3	H	24	SWITCH	PUSH BUTTON	SPDT	7	D1-SWP-B00-003
105	SW4	E	3	SWITCH	PUSH BUTTON	SPDT, RTANG		D1-SWP-B00-005
106	SW5	E	15	SWITCH	DIP ROCKER	5 POSITION		D1-SWD-R00-003
107	SW6	Ī	15	SWITCH	DIP ROCKER	4 POSITION		D1-SWD-R00-003
107	SW7	Ġ	15	SWITCH	DIP ROCKER	4 POSITION	7	D1-SWD-R00-004
109	SW8	S	15	SWITCH	DIP ROCKER	4 POSITION	7	D1-SWD-R00-004
110	3770  1	J T	17	CABLE ASSY	40 CONDUCTOR	410311014	<b>3</b>	D1-100-021-511
110	11	'	1.5	CABLE A331	40 CONDUCTOR		•	D1-100-021-311
111	15	V	8	HEADER	15 POSITION		(3 REO'D)	D1-CNM-S00-004
112	J6	c	16	HEADER	15 POSITION		(3 REQ'D)	
113	<b>j</b> 7	Ċ	24	HEADER	15 POSITION		(3 REQ'D)	
114				SOCKET	24 PIN DIP		(FOR U2)	
115	· · · · · · · · · · · · · · · · · · ·	-		HEATSINK	FOR T0-3 DEVICES	<b>.</b> .	`````	D1-HSH-P00-002
116		_	•	NUT	HEX	#6-32	(2 REO'D)	00-631-133-040
117		-		LOCKWASHER	INTERNAL TOOTH	#6	(2 REQ'D)	00-655-017-018
- 3						×		



### **Appendix D: Parts List**

### APPENDIX D.4: Data/Pak PC Board Option

		A Section of the Contract of t	ATOR		DECEMBEROS.		l	
NO.	CIRCUIT			COMPONENT	DESCRIPTION	DESCR. 2	MISC.	PART NUMBER
	•••	ROW	COL				4	
********								
3		ś		ŝ		1	400	
1	R1	0	12	RESISTOR	3.9K OHM	1/4 W, CARBON	5%	D1-RSC-ACN-087
2	R2	0	16	RESISTOR	3.9K OHM	1/4 W, CARBON	5%	D1-RSC-ACN-087
3	R3	BB	16	RESISTOR	22K OHM	1/4 W, CARBON	5%	D1-RSC-ACN-105
4	R4	L	12	RESISTOR	220 OHM	1/4 W, CARBON	5%	D1-RSC-ACN-057
5	R5	N	12	RESISTOR	220 OHM	1/4 W, CARBON	5%	D1-RSC-ACN-057
6	R6	Ζ	16	RESISTOR	22K OHM	1/4 W, CARBON	5%	D1-RSC-ACN-105
7	C1	С	6	CAPACITOR	TANTALUM	10 MFD, 25V	i i	D1-CR2-CT1-J10
8	C2	1	3	CAPACITOR	SILVER MICA	100 PFD, 500V	•	D1-CRL-BTJ-P10
9	C3	L	20	CAPACITOR	FILM	0.1 MFD, 63V		D1-CRF-BD2-L10
10	D1	Υ	12	DIODE	SMALL SIGNAL	100 PIV, 0.2 AMP	1N4148	D1-DDF-AB0-001
				DIODE	51 61 <del>0</del> 1.11	100 000		D4 DDF 4 D0 004
11	D2 D3	X	14	DIODE	SMALL SIGNAL	100 PIV, 0.2 AMP	1N4148 1N4148	D1-DDF-AB0-001
12	D3 D4	Y Z	13 11	DIODE	SMALL SIGNAL A	100 PIV, 0.2 AMP 100 PIV, 0.2 AMP	1N4148	D1-DDF-AB0-001 D1-DDF-AB0-001
13 14	LED1	Z I	1 <i>7</i>	LED	RED. WITH SPACER	100 PIV, 0.2 AMP	1194140	D1-100-024-001
15	LED1	L	8 8	LED	RED, WITH SPACER		7	D1-100-024-001
13	LLU2			LLD	KED, WITT 31 ACEK			D1-100-02-001
16	DSP1	1	7	DISPLAY	LCD, 4 DIGIT	•	4	D1-DSL-C00-001
17	Q1	i		TRANSISTOR	NPN		2N2222A	D1-TSS-NPA-001
18	Ŏ2	P	100000000000000000000000000000000000000	TRANSISTOR	NPN		2N2222A	D1-TSS-NPA-001
19	Ū1	L	4		DECODER/LCD DRIVER	4 DIGIT LCD	•	D1-ICD-CI0-001
20	U2	U	19	IC	QUAD D REGISTER	-	4076B	D1-ICD-MC0-001
					77 //			
21	U3	Р	19	IC	QUAD EXCLUSIVE NOR	-	4070B	D1-ICD-DC0-001
22	SW1	V	10	SWITCH	10 POSITION	BCD	ORN DOT	D1-100-024-005
23	J5	Ζ	9	HEADER	15 POSITION	-	•	D1-CNM-S00-004



# **Appendix D: Parts List**

### APPENDIX D.5: VLC (Voltage Limit Control) PC Board Option

NO.	CIRCUIT ID	APPEN LOCA	TOR	COMPONENT	DESCRIPTION	DESCR. 2	MISC	PART NUMBER
*******		Bullinder	8					
1	R1	Z	6	RESISTOR	22K OHM	1/4 W, CARBON	5%	D1-RSC-ACN-105
2	R3	G	14	RESISTOR	3.9K OHM	1/4 W, CARBON	5%	D1-RSC-ACN-087
3	R4	H F	フ 14	RESISTOR RESISTOR	3.9K OHM 270 OHM	1/4 W, CARBON	5%	D1-RSC-ACN-087
4 5	R6 R7	F	7	RESISTOR	270 OFM 270 OHM	1/4 W, CARBON 1/4 W, CARBON	5%	D1-RSC-ACN-059 D1-RSC-ACN-059
3	<b>N/</b>	Г		KESISTOK	270 OHM	1/4 W, CARBON	5%	DI-KSC-ACN-039
6	R8	Z	12	RESISTOR	22K OHM	1/4 W, CARBON	5%	D1-RSC-ACN-105
7	C1	Ϋ́	16	CAPACITOR	TANTALUM	10 MFD, 25V	270	D1-CR2-CT1-I10
8	Č2	c	10	CAPACITOR	FILM	0.1 MFD, 63V		D1-CRF-BA2-L10
9	D1	X	14	DIODE	SMALL SIGNAL	100 PIV, 0.2 AMP	1N4148	D1-DDF-AB0-001
10	D2	J	16	DIODE	SMALL SIGNAL	100 PIV, 0.2 AMP	1N4148	D1-DDF-AB0-001
11	D3	K	16	DIODE	SMALL SIGNAL	100 PIV, 0.2 AMP	1N4148	D1-DDF-AB0-001
12	D4	М	16	DIODE	SMALL SIGNAL	100 PIV, 0.2 AMP	1N4148	D1-DDF-AB0-001
13	D5	N	16	DIODE	SMALL SIGNAL	100 PIV, 0.2 AMP	1N4148	D1-DDF-AB0-001
14	D6	X	7	DIODE	SMALL SIGNAL	100 PIV, 0.2 AMP	1N4148	D1-DDF-AB0-001
15	D7	J	4	DIODE	SMALL SIGNAL	100 PIV, 0.2 AMP	1N4148	D1-DDF-AB0-001
16			4	DIODE	SMALL SIGNAL	100 PIV, 0.2 AMP		D1 DDF 400 001
17	D8 D9	L M	4 4	DIODE	SMALL SIGNAL	100 PIV, 0.2 AMP	1N4148	D1-DDF-AB0-001 D1-DDF-AB0-001
18	D10	N	4	DIODE	SMALL SIGNAL	100 PIV, 0.2 AMP	1N4148 1N4148	D1-DDF-AB0-001
19	D11	ï	7	DIODE	SMALL SIGNAL	100 PIV, 0.2 AMP	1N4148	D1-DDF-AB0-001
20	D12	i	14	DIODE	SMALL SIGNAL	100 PIV, 0.2 AMP	1N4148	D1-DDF-AB0-001
		•		5.652	J, J LEE D. C. V. LE	100 111, 0.271111		BIBBIADOOT
21	LED1	G	4	LED	RED, WITH SPACER	-		D1-100-024-001
22	LED2	G	17	LED	RED, WITH SPACER	-		D1-100-024-001
23	Q1	D	7	TRANSISTOR	NPN	-	2N2222A	D1-TSS-NPA-001
24	Q2	D	14	TRANSISTOR	NPN	-	251222224	D1-TSS-NPA-001
25	U1	K	12	IC /	QUAD D REGISTER	-	2N2222A	D1-ICD-MC0-001
							4076B	
26	SW1	V	11	SWITCH	17 POSITION	BCD		D1-100-024-009
27	SW2	ð	11	SWITCH	17 POSITION	BCD	₿₩	D1-100-024-009
28 29	SW3	F AA	11	SWITCH	TOGGLE	SPST	₿Ŭŧ	D1-SWT-P01-001
29	J6	AA	16	HEADER	15 POSITION	-	DOL	D1-CNM-S00-004
8							**************************************	



# **Appendix D: Parts List**

### APPENDIX D.6: VRC (Voltage Reduction Control) PC Board Option

NO.	CIRCUIT ID	LOC	DIXA ATOR	COMPONENT	DESCRIPTION	DESCR. 2	MISC.	PART NUMBER
1 2 3 4 5	R1 R2 R3 R5 R7	S U U L H	18 4 3 11 7	RESISTOR RESISTOR RESISTOR RESISTOR RESISTOR	22K OHM 390 OHM 390 OHM 39K OHM 270 OHM	1/4 W, CARBON 1/4 W, CARBON 1/4 W, CARBON 1/4 W, CARBON 1/4 W, CARBON	5% 5% 5% 5%	D1-RSC-ACN-105 D1-RSC-ACN-063 D1-RSC-ACN-063 D1-RSC-ACN-087 D1-RSC-ACN-059
6 7 8 9 10	R8 C1 C2 C3 C4	M Z K R D	18 17 4 4 8	RESISTOR CAPACITOR CAPACITOR CAPACITOR CAPACITOR	22K OHM TANTALUM TANTALUM FILM FILM	1/4 W, CARBON 10 MFD, 25V 10 MFD, 25V 0.1 MFD, 63V 0.1 MFD, 63V	5% - - - -	D1-RSC-ACN-105 D1-CR2-CT1-J10 D1-CR2-CT1-J10 D1-CRF-BD2-L01 D1-CRF-BD2-L01
11 12 13 14 15	D1 D2 D3 D4 D5	T U V X X	16 16 16 16 8	DIODE DIODE DIODE DIODE DIODE	SMALL SIGNAL SMALL SIGNAL SMALL SIGNAL SMALL SIGNAL SMALL SIGNAL	100 PIV, 0.2 AMP 100 PIV, 0.2 AMP 100 PIV, 0.2 AMP 100 PIV, 0.2 AMP 100 PIV, 0.2 AMP	1N4148 1N4148 1N4148 1N4148 1N4148	D1-DDF-AB0-001 D1-DDF-AB0-001 D1-DDF-AB0-001 D1-DDF-AB0-001 D1-DDF-AB0-001
16 17 18 19 20	D6 LED1 Q1 U1 U2	Z H G M Z	9 6 10 16 4	DIODE LED TRANSISTOR IC IC	SMALE SIGNAL RED, WITH SPACER NPN QUAD D REGISTER OPTOCOUPLER	100 PIV, 0.2 AMP - - - -	1N4148 2N2222A 4076B HCPL-3700	D1-DDF-AB0-001 D1-100-024-001 D1-TSS-NPA-001 D1-ICD-MC0-001 D1-IST-R00-001
21 22 23 24	SW1 SW2 J7 C5	X F AA J	12 14 11 10	SWITCH SWITCH HEADER CAPACITOR	11 POSITION TOGGLE 15 POSITION CERAMIC	BCD SPDT, CO - 0.01 MFD 50V	YEL DOT - -	D1-100-024-007 D1-SWT-P01-002 D1-CNM-S00-004 D1-CRC-AW2-M10



APPENDIX E:
Data/Pak Option
.... Alert Codes

E

## Appendix E: Data/Pak Option .... Alert Codes

# **Alert Code Definitions** Look for the specific fault below. Appendix G will guide you where to troubleshoot. BINARY B3 B2 B1 B0 B3 B2 B1 BO B3 B2 B1 BO B3 B2 B2 B1 FAULTY VOLTAGE LEVEL SWITCH FAULTY TIME DELAY SWITCH **FAULTY BANDWIDTH SWITCH** FAULTY "R" COMPENSATION SWITCH FAULTY "X" COMPENSATION SWITCH FAULTY VRC SELECTOR SWITCH FAULTY LOWER LIMIT SWITCH ON VLC **FAULTY UPPER LIMIT SWITCH ON VLC** (NOT USED) FAULTY MICROPROCESSOR PORT #1 FAULTY MICROPROCESSOR PORT #2 LINE CURRENT > 350% OF PRIMARY CT LINE CURRENT < 2% OF CT RATING INPUT VOLTAGE < 64 VOLTS NO C.T. OR P.T. PHASE INPUT (NOT USED)

APPENDIX F:
Troubleshooting with the
Operational Simulator



## **Appendix F: Troubleshooting with the Simulator**

#### .Operational Simulator - Initial Setup

If you are using a simulator for testing, set the adjustments on it as follows:

- Power Switch "off"
- S and L variacs at about 80% point
- Power flow "off"
- High power factor
- Straight regulator
- SSPT "off"
- Current magnitude potentiometer fully clockwise

#### **Operational Simulator - Notes**

For the duration of troubleshooting:

- the SSPT switch will ALWAYS be "off"
- the Straight/Inverted switch will ALWAYS be in a "straight" position

During the testing process, you will often be asked to provide a voltage differential between the measured voltage and the voltage level setting. As the simulator provides both source and load variacs, the differential can be satisfied via these adjustments. This would be the preferred method. (If the neither simulator or variac were available, it would be necessary to provide a differential by raising / lowering the voltage setpoint itself.) Although this would work, adjusting the actual voltage is much preferred, as it better simulates actual operating conditions.



APPENDIX G: Fault Symptoms Guidance



# **Appendix G: Fault Symptoms Guidance**

#### **Fault Symptoms Lookup Chart**

This appendix lists fault symptoms in alphabetical order for quick identification. Locate the fault symptom experienced and proceed to the section and page shown.

#### **SECTION:PAGE**

Alert code message on Data/Pak:

0	Faulty switch (voltage level, time delay, bandwidth, compensation)	3-55
0	Faulty switch (VRC) Faulty switch (VLC upper, VLC lower)	3-79,3-82
0	Faulty microprocessor port	3-45
0	Line current problems	3-49
0	Sensed voltage problems	3-42
0	No C.T. or P.T. phase input	3-46
Autor	matic control does not operate, manual control only	3-05
Circu	its, control panel board fault suspected	
0		
0	Annunciation logic	3-52
	C.T. Magnitude input circuit	3-48
0	C.1. Zero Cross detection circuit	3-46
0	Current transformer interface	3-30
0	DRAG HANDS reset interface	3-33
0	NEUTRALITE interface	3-32
0	Operator setpoint switch logic	3-55
0	Operations Counter interface	3-34
•	Oscillator	3-39
0	Potential & Utility winding interface	3-31
0	Power Supply (low voltage rectification)	3-36
0		3-37
•	Power Supply (low voltage A/D reference)	3-38
0	P.T. Magnitude input circuit	3-45
•	P.T. Zero Cross detection circuit	3-42
0	Relay Driver Circuits	3-50
0	Reset circuit	3-40
0	Raise/Lower relay interface	3-35

# **Appendix G: Fault Symptoms Guidance**

Circuits, interface board fault suspected

Oata/Pak interface logic	3-70
Control Panel Bus Arbitration	3-72
Control Panel Communications Interface	3-74
Memory Management	3-64
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Port 2 Arbitration Logic	3-70
Power Monitor Circuits	3-66
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Switch Decoding	3-70
Circuits, transformer board fault detected	
C.T. transformer T3	3-60
Power transformer T1	3-58
P.T. transformer T4	3-59
Sensing Transformer T2	3-57
Current does not appear to be sensed	3-24
Current is sensed incorrectly	3-49
Communications, option boards appear defective	3-74
Data/Pak not properly operating	3-76
DRAG HANDS reset function does not operate	3-33
NEUTRALITE does not operate	3-32
Operations counter does not operate.	3-34
Switches, control panel, do not operate correctly	3-55
Switches, interface board, do not operate correctly	3-70
Switches, (VLC, VRC, Data/Pak) do not operate correctly	3-79, 3-80
Voltage not present at TEST TERMINALS	3-22
Voltage is not correctly sensed	3-45
(VLC) Voltage Limit Control Option not operating properly	3-79
(VRC) Voltage Reduction Control Option not operating properly	3-82
Watchdog lite, control panel doesn't flash	3-20
Watchdog lite, interface board panel doesn't flash	3-68



3-68

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APPENDIX H: Diagnostic Quick Reference



# **Appendix H: Diagnostic Quick Reference**

#### Test Point Quick Reference Table

The following table is appended for the convience of quickly determining the primary test points and quickly locating the pages where these test points are mentioned.

TP#	DESCRIPTION	LOCATION	PAGE#
TP1	MODB	U1 (PIN 24)	3-
TP2	MODA	U1 (PIN 25)	3-
TP3	VLOGIC	U17 (PIN 6, OR 16)	3-37
TP4	VRH	J1 (PINS 14 & 15)	3-38 - 3-39
TP5	IC1	U1 (PIN 22)	3-42 - 3-43
TP6	ANO	U1 (PIN 17)	3-44 - 3-45
TP7	IC2,	U1 (PIN 7)	3-46 - 3-47
TP8	<u>AN1</u>	U1 (PIN 18)	3-48 - 3-49
TP9	RESET	U1 (PIN 39)	3-40 - 3-41
TP10	XIRQ	U1 (PIN 40)	3-40 - 3-41
TP11	XTAL	U1 (PIN 30)	3-39
TP12	MOTOR RAISE RELAY (PIN 1)	(PIN 1)	3-50 - 3-51
TP13	PT SOURCE RELAY (PIN 1)	(PIN 1)	3-50 - 3-51
TP14	MOTOR LOWER RELAY (PIN 1)	(PIN 1)	3-50 - 3-51
TP15	VRECT	U11 (PIN 1), J1 (PIN 12)	3-36
TP16	VRELAY	U11 (PIN 2)	3-37

MAN CIPCTICAL PARTITION COSTS.

# **SIEMENS**

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If drawings or other supplementary instructions for specific applications are forwarded with the manual or separately, they take precedence over any conflicting or incomplete information in this manual.