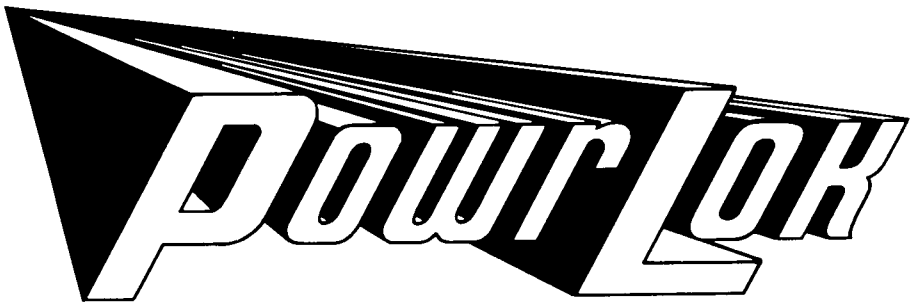
INSTRUCTION BOOK

GEK-31042



THREE PHASE
UNINTERRUPTIBLE
POWER SUPPLIES

CUSTOM POWER EQUIPMENT DEPARTMENT

GENERAL ELECTRIC

PHILADELPHIA, PA.

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SECTION I: OVERALL SYSTEM

INTRODUCTION

The advent of computer technology and its widespread application to commercial and industrial enterprises has created a need for a power source which is entirely free from voltage dips and interruptions, even of the order of a few cycles. Computers are not alone in this respect. Other critical loads include vital communication links, power distribution telemetry, and the like.

Commercial power distribution systems cannot satisfactorily supply service to these critical loads because of the nature of distribution practices. Lightning strokes, tree contact, and rodent damage are examples of events which can cause interruption of electrical power. These interruptions can be frequent, and can adversely affect critical loads even if their duration is a matter of seconds or even cycles.

Various types of apparatus have been devised to isolate the critical load from disturbances on the distribution system. These include M-G sets with flywheels, clutches, diesels, etc. in various configurations. None of these performs as well as General Electric's Uninterruptible Power Supply system. This system with its solid state components features fast response (order of microseconds), quiet operation, stable output frequency regardless of loading, no special foundations or shaft alignment, and long life with minimum maintenance. The rectifier and inverter technology on which these systems are based is not new and has been treated in other publications. However, the combined application of these equipments complete with control and storage battery calls for instructional information which embraces the entire system. It is the purpose of this book to present a detailed description of the Uninterruptible Power Supply, the various types, function of major components, and operation of subassemblies and circuits. It is intended as an aid to the user in getting optimum performance from his equipment. It is also intended that the elementary diagram supplied with the equipment be used as a companion to this manual, since the elementary diagram contains a schematic of all the circuits described.

RECEIVING & INSTALLATION

Installation consists of unpacking, setting up the apparatus and making connections between the various assemblies. A few suggestions are given here, however, the actual methods used are dependent upon the local conditions existing at the time of installation.

This equipment is assembled, tested, and packed with care to enable the purchaser to install and place it in operation with a minimum of time and labor. Immediately upon receiving the equipment, it should be carefully checked against the memorandum of shipment. If any parts are found damaged, or missing, the purchaser should immediately present a claim to the Transportation Company and notify the nearest sales office of the General Electric Company.

It is good practice to place the equipment as near as possible to its permanent location before unpacking. The standard type of unpacking tools should be used. A nail puller can be especially useful. Careless unpacking methods will invariably result in parts being damaged or marred. Some parts such as bolts and screws are packed in special containers to keep them together; however, they may become separated. Therefore, packing material should not be discarded until it is certain that all parts have been removed. Equipment should be thoroughly cleaned to remove particles of packing materials or foreign substances which may have become lodged in or between any of the parts. Apparatus not immediately installed should be labeled and set aside in a clean dry place of moderate temperature and protected from injury.

When equipments are installed, ample space should be provided around the various parts to permit easy inspection, adjustment, and repair. Whenever possible all control devices are mounted at the factory; interconnections are made and leads are brought out to numbered terminals, making it necessary only to install the component pieces and connect the numbered terminals to the various pieces of apparatus. The remote interconnection diagrams supplied should be used as a guide for making the connections.

When the equipment has been set up, it should be thoroughly inspected and checked to be sure that all connections are complete and tight, that the relays and instruments are in good mechanical condition, that they have been thoroughly cleaned, and that all of the movable parts work freely. All devices should make good contact and have clean contact surfaces.

SYSTEM DESCRIPTION

NON-REDUNDANT UPS

The simplest form of uninterruptible power supply (UPS) utilizes a regulated rectifier, an electrical storage battery, and a static inverter. A single line diagram of this kind of system is shown in Figure 1.

During normal operation the battery charger converts the incoming AC to a regulated DC bus voltage. The DC bus then supplies the power to the static inverter which converts it to AC power with the characteristics described below. Since the AC output is produced from DC power by the static inverter, the control system of the static inverter alone governs the characteristics of the AC output.

Any fluctuations in voltage or frequency which occur on the power distribution system are completely isolated from the critical load.

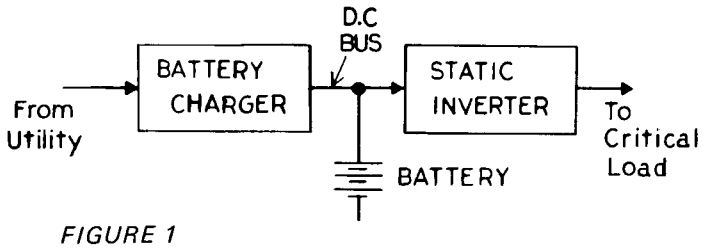


FIGURE 1
SINGLE LINE DIAGRAM OF NON-REDUNDANT UPS

In the event of either a momentary or prolonged failure of the owner's normal source of commercial power, the electrical storage battery will furnish the DC power needed to operate the static inverter. The battery is continually connected to the DC bus so that it is always available to supply electrical energy whenever it is required. This arrangement is defined as a "Floated Battery" system, because the battery is constantly available without the need of any switching operation. (Since a battery charger can transmit electrical power in one direction only, the battery cannot feed power back into the commercial power system. Thus, there is no danger of discharging the battery into a dead commercial power system.)

Once the normal power to the UPS has been restored, the regulated rectifier will resume supplying the inverter, and at the same time the regulated rectifier will recharge the battery.

REDUNDANT UPS

The simplest UPS described above suffers from one very serious flaw. A failure of the static inverter interrupts power to the critical load. Thus, the reliability of the UPS cannot be made any greater than the reliability of the inverter itself. While solid state inverters are a very reliable class of equipment, they are not perfect; so that an eventual inverter failure must be expected. However, by using a "Redundant" System it is possible to overcome this limitation and to provide a UPS which has an overall system reliability that is actually greater than the reliability of any individual component of the UPS.

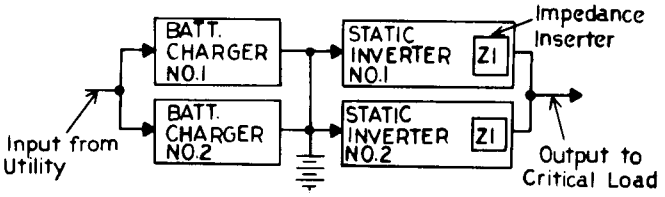


FIGURE 2 - SINGLE LINE DIAGRAM OF REDUNDANT UPS

The obvious way to avoid the complete dependence on a simple static inverter is to provide two such inverters connected in parallel. Unless special precautions are taken, however, a failure in either of the two inverters will cause the voltage of the critical bus to collapse. Thus a failure in either inverter will fail the entire UPS. Clearly the overall reliability of this arrangement is no better than before. In fact, it is worse, since there is almost twice the chance for a failure to occur in either of the two inverters as there is for a failure to happen in only one inverter. Thus, if redundant inverters are going to be used, a means must be devised to prevent a failure in any one inverter from affecting the overall system performance. This means that any inverter which fails must be removed from the system immediately, well before the effects of failure are felt at the critical bus. A solid state "Impedance Inserter" has been provided between each inverter and the critical bus to accomplish this function. Whenever a fault is sensed within one of the redundant inverters, the appropriate impedance inserter immediately isolates the offending inverter from the system. (See Section 6 for detailed ZI functions.) Tests have shown this isolation is accomplished before the system output is disturbed. A simplified diagram of a redundant UPS with impedance inserter is shown in Figure 2. Also note that two battery chargers have also been provided in case one charger should fail.

Except for either a failure within the UPS or a fault within the critical load; the operation of the redundant UPS is the same as the operation of the simple non-redundant UPS. The only differences are as follows:

1. Whenever an internal failure develops within one of the redundant inverters, this failure is sensed by the impedance inserter and the offending inverter is immediately disconnected from the system.
2. If the system becomes overloaded or if a short circuit develops in the critical load, the UPS is called upon to deliver greater current than it is capable. Under these circumstances this impedance inserter will limit the load current by introducing a high impedance into the feeders leading to the critical bus. If this excessive current is not reduced to normal within three seconds, the ZI takes the inverter off the line by tripping the inverter output breaker.

UPS WITH BYPASS SWITCHGEAR

A complement of circuit breakers, complete with the necessary transformer and synchronizing equipment, can be added to the UPS. A single line diagram of a simple by-pass system is shown in Figure 3. This by-pass switchgear is used to feed the critical load from the utility source while the UPS is off the line for maintenance or inspection. The synchronizing equipment enables an operator to place the

inverter output in phase with the commercial power source, allowing Breaker (b) to be closed, which sets up a momentary paralleling situation. Breaker (a) can then be opened, fully transferring the load to the utility. Power flow to the critical load is not interrupted during this transfer.

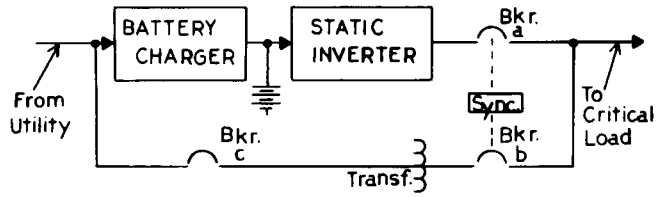


FIGURE 3 - SINGLE LINE DIAGRAM OF UPS WITH BY-PASS SWITCHGEAR

An automatic transfer to the by-pass switchgear can also be achieved. In this type arrangement, the inverter output is kept in phase-lock with the utility source through a special phase discriminator circuit. Transfer to by-pass can, of course, be accomplished manually. If, however, the inverter should fail or load conditions are such that failure is imminent, a transfer to by-pass will be automatically initiated. Except for the very rare case where the inverter has a total internal failure, the transfer to by-pass is a make-before-break transition so there is no interruption of power to the load.

An additional refinement in the form of a static bypass can also be incorporated into a UPS. It is essentially an "instantaneous close" circuit breaker applied in parallel with the conventional by-pass circuit breaker. In this arrangement, the inverter output is again kept in phase-lock with the utility source. Even in the case of a total internal failure in the inverter, the static by-pass (instantaneous close circuit breaker) is electronically switched on at the same time as the impedance inserter in the inverter. Thus power flow to the load is never interrupted. A few cycles after the static switch is closed, the conventional by-pass circuit breaker closes it's contacts, shorts out the static breaker, and carries current to the load.

UPS MAJOR COMPONENTS

This section describes the equipments which make up the UPS system, i.e. Battery Charger, Inverter, Master Control, and Station Battery. It also describes the major circuits associated with each equipment and the function performed.

BATTERY CHARGER

Input power comes from a three pole, manually-operated circuit breaker to the primary of the three-phase transformer. The purpose of the transformer is to change the a-c primary voltage to the level required to obtain the desired output of 405 Volts d-c at maximum conduction angle. A three-phase control-power disconnect is provided to isolate the control circuits in the unit.

The rectification of the a-c voltage is accomplished by the SCR (thyristor) power modules. The basic power module consists of a three phase bridge circuit, with each leg of the bridge containing SCR cells and a series current limiting fuse. An SCR is a phase controlled rectifying device which is controlled by applying a signal to the gate lead during the positive half cycle of the a-c voltage wave (anode of SCR positive with respect to cathode), causing the SCR to conduct as an ordinary rectifier. When the applied a-c voltage reverses in polarity, the SCR will turn off until the next gate signal is applied. A neon light is shunted across each SCR to indicate failure of SCR or fuse. Gate signals to fire the SCR's are produced by a gate pulse generator which is, in turn, controlled by the regulating amplifier module. Details of the gate pulse generator are contained in a separate instruction book, GEI-90837. Details of the regulating amplifier are contained in GEK-13522.

A filter is placed in the output to limit ripple voltage. The silcomatic rectifier is protected against normal voltage transients, such as produced by switching and other line disturbances, by surge suppressors connected to both the a-c and d-c buses.

The output voltage of the battery charger is regulated by continuous adjustment of the time in the power cycle at which the SCR's are gated. The regulating circuit is of an internal closed-loop type. A feedback signal proportional to the d-c output voltage is compared to a reference signal and the resultant error is fed to the control circuit. This signal will cause a shift in the gating pulse of the thyristors; resulting in their firing at different times in the power cycle.

A current walk-in feature is provided to prevent excessive current when the input circuit breaker is closed and the silcomatic rectifier is connected to a load, such as a battery or filter capacitors on the d-c bus.

To protect against battery overcharge after an outage, current-limit is integrated into the regulating circuit. The current-limit utilizes an inverse voltage-current relationship to control the battery charger output. Should the current exceed this relationship at a given d-c voltage, the regulator circuit will cause the SCR's to fire at a later time on the power cycle and reduce the output voltage. The voltage will drop until the inverse current-voltage relationship is met. If the d-c voltage exceeds the maximum rated, the overvoltage relay will open the incoming a-c breaker and shut down the regulated rectifier.

A thermotector is embedded in the input transformer to protect the transformer from overheating. When the transformer temperature reaches the thermal design limit, the input breaker is tripped.

Fan failure on any of the rectifier cubicles trips the input breaker.

See Section 2 - Battery Charger for more detailed information.

INVERTER

The static inverter is used to convert d-c voltage to stepped sine-wave voltage. It utilizes phase-controlled SCR's in a bridge-type circuit to chop the d-c voltage into pulses, which are combined and filtered to approximate a sine-wave voltage. The inverter input operating range is 320 to 405 VDC.

A starting circuit is used to initially charge the d-c filter capacitors, which will, when charged, pick up the d-c voltage relay. This voltage relay initiates a sequence of events which removes the starting circuit from the power circuit. The a-c output breaker can not be closed until this sequence is completed.

The d-c power is fed in the output transformer through the inverter SCR cells. Each primary winding of the output transformer is connected between the positive and negative d-c buses but is electrically isolated from each bus by a set of forward and reverse SCR cells. Firing the forward set of cells allows a positive rectangular pulse of d-c voltage to be applied to the winding. The voltage magnitude of this pulse is equal to the value of the d-c bus voltage. The duration is controlled by the overlap in the conducting period of the positive d-c bus thyristor with respect to the negative d-c bus SCR. No voltage appears across the transformer primary winding until both the cells are gated on. The turn-on of the negative bus cell can be delayed with respect to the turn-on of the positive bus cell, hence, the width of the voltage square-wave (or average voltage) impressed on the primary winding can be controlled. The inverter employs six such pairs of thyristors and three transformer primary windings.

Proper gating of the cells results in a stepped voltage wave being impressed on the primary of the transformer. The secondary windings are connected in a zig-zag configuration to decrease output harmonic content. This output is then filtered to attenuate remaining harmonics.

Output frequency is controlled by the frequency at which the SCR power cells are gated. The gating circuit is triggered by a solid-state fixed frequency (adjustable + 1 CPS), oscillator and generates a voltage pulse which is amplified to gate the inverter thyristors. Since the oscillator is electrically independent of the power circuit, the output frequency is unaffected by system loading. Voltage control changes only the phase relationship of the gating signals without affecting their frequency.

The voltage regulation system is of the closed loop type. A feedback signal, proportional to the average of the output phase voltages, is compared to a reference signal and the resultant error is fed to the control circuit. This causes an advance or delay in the gating pulses of certain cells which will result in a relative shift in the firing time of the negative bus SCR with respect to the positive-bus cell. This shift in the gating time will change the duration of voltage pulse across the output voltage. The level of the output voltage is changed by adjusting the reference signal potentiometer.

In a redundant system, a static interrupter is placed in series with the output breaker of each inverter to prevent excessive critical a-c bus transients in the event of an internal fault in an inverter. It consists of a set of back-to-back SCR's, shunted by an impedance, in each of the three phases. During normal operation, the SCR's are continuously energized so that they pass alternating current with only the forward drop of the cell in series with the output voltage.

In the event of a critical bus fault, a pre-charged capacitor back biases the cells which were conducting and causes them to block, thus inserting impedance into the circuit to limit current from the inverter system. The inverter system will operate in the current limit mode for a preset interval (approximately 3 seconds) after which the system output breaker will trip. Downstream protective devices should be selected to clear within the 3 second interval to assure load-fault protection. Current available in the current limit mode is the sum of full load currents from each inverter in the system. If an internal inverter fault occurs, the static interrupter disconnects the faulted inverter from the critical bus. This is done quickly enough to prevent the other inverters from seeing the fault. See Section 3 & 4 - Inverter and Section 6 - Impedance Inserter for more detailed information.

MASTER CONTROL

The Master Control compartment(s) is part of every UPS. It houses the electronic control for the system and also some instrumentation. Electronic power supplies to provide excitation for the control circuits are also included in the master control. Voltage relays and synchronizing devices (when required) are also mounted here. These synchronizing devices are associated with transfer to the by-pass switchgear when it is present and are located on a front door for accessibility. The electronic control for the system utilizes solid state components mounted on printed circuit boards to perform various functions, including:

1) Oscillators to establish and control the UPS output frequency by generating the basic pulses ultimately used to gate the inverter SCR's.
2) The monostable circuit to combine the output of the oscillators and form a single train of pulses*.
3) The master flip-flop circuits which take the train of pulses from the monostable circuit and act in conjunction with a steering signal to produce gate pulses

for the SCR's in the master inverter carts. The steering circuits assure that the flip-flops operate as required to obtain the correct positive and negative a-c half cycles and also the correct phase sequence at the inverter output.

4) Slave flip-flop circuits which are actuated by the master flip flops and produce gate pulses for the SCR's in the slave inverter carts. The output of the slave flip-flop can be delayed by the action of the phase control boards. This, in turn, determines how wide the voltage pulse will be across the output transformer primary winding. This, then, controls the magnitude of the inverter output voltage.
5) The voltage regulator circuit takes a sample of the inverter output voltage and works in conjunction with the phase control circuit to determine how much the slave flip-flop output should be delayed or advanced. This variation allows the inverter output voltage to increase or decrease slightly as required to stay constant at a pre-determined level.

There are two electronic power supplies in the Master Control equipment. The 17 Volt "Chopper" supply energizes the master and slave flip-flop printed circuit boards, the phase control boards, pulse amplifier boards and fuse monitor. Note that a 48 Volt takeoff from the "Chopper" is used to energize the oscillator and the voltage regulator boards. The other power supply, with a 48 Volt output, feeds the printed circuit boards on the impedance inserter and the Static Switch (when used). These two power supplies are mounted on separate panels and each forms a complete subassembly. See Master Control - Section 5 for more detailed information.

*Used on Redundant Systems Only.

BATTERY

The battery normally furnished with the UPS is the lead calcium type, consisting of 184 cells in series, per battery. This is a lead-acid battery that uses a new, improved lead calcium plate alloy. It does not require an equalizing charge and is non-gassing. The battery remains connected to the DC bus at all times to immediately assume load if the commercial power source fails. It will furnish power to maintain rated UPS output for the time required and will be recharged by the rectifier battery charger upon return of the commercial power source. The battery protection consists of a circuit breaker sized to handle the continuous current required by the inverter and also the short circuit amperes from the battery. As in common station battery practice, the cells are situated in a rack which can be two or three tiers. These racks can be arranged back-to-back or end-to-end.

TURN-ON PROCEDURE BATTERY CHARGERS

With commercial power available and properly connected to the UPS, begin the turn-on procedure with the Battery Charger(s) and proceed as follows:

1) Close the control power switches to start the cooling fans, energize logic and protective circuits and the gate pulse generator and regulator circuits.
2) Turn Mode Selector switch to the "Automatic" position.
3) Turn current limit potentiometer R79 on the instrument door completely CCW.
4) Close the AC breaker.
5) Turn the current limit potentiometer (R79) CW until the DC Voltmeter reads 405 Volts.
6) Perform Steps 1 through 5 for the redundant Battery Charger (If any).
7) Close the Battery breaker.
8) Turn the current limit potentiometer R79 completely

The battery charger(s) are now paralleled with the station battery on the DC bus input to the inverter(s). Continue turn-on procedure with the Master Control and Inverter(s) as follows, starting with the inverter which supplies 208 Volts AC input to the 48 Volt DC supply in the Master Control:

1) Close the single pole knife switch in the Master Control section to energize excitation circuits for the pulse generator and regulator circuits. This also provides power for the inverter indicating lamp and alarm circuits.
2) Close the double pole knife switch in the DC input unit of the Inverter.
3) Close the DC input breaker. After a short time delay, the DC contactor closes and seals in. This action is automatic. The Inverter output voltage will build up to rated value.
4) Check for rated AC voltage on all three phases.
5) Close the AC output breaker connecting the inverter to the critical bus.
6) Close the Impedance Inserter (ZI).
7) Perform Steps 2 through 6 for the redundant inverter, if any. Note: The voltage may have to be adjusted after closing onto the critical bus.

TURN-OFF PROCEDURE

Begin with the Inverter and Master Control and proceed as follows:

1) Open the AC output breaker.
2) Open the DC input breaker.
3) Wait 5 seconds and open the control power knife switch in the DC input unit of the inverter.
4) Repeat Steps 1 through 3 for the redundant Inverter(s), if any.
5) Open the knife switch in the Master Control section.

Normally the Battery Charger is left connected to the battery in order to maintain required charging current to it.

However, if this also is to be shut down for maintenance or cleaning:

1) Open the battery breaker.
2) Turn the current limit potentiometer (R79) on the door completely CCW.
3) Open the AC breaker.
4) Repeat Steps 1 through 3 for the redundant Battery Charger(s), if any.
5) Open the control power switches.

MONITORING OF VOLTAGES

This important function is performed by various voltage relays which detect abnormal conditions at critical locations throughout the equipment. The more common are listed here although additional devices may be added for any one particular equipment.

a) On the 17 Volt Power Supply (Chopper): These instantaneous type relays (Type PJV) monitor the output of this critical supply. They are de-energized if the 17 Volt output is lost, and prevent start-up of the inverters until the condition is corrected.
b) On the 48 Volt Power Supply: These instantaneous type relays monitor the output of this supply which feeds the impedance inserter control. They initiate transfer to the bypass switchgear (when present) if the 48 Volt output is lost.
c) On the DC bus: Instantaneous undervoltage relays (Type NGV) shut down the system by tripping the AC and DC circuit breakers whenever this bus voltage drops below the 320 Volt level. These relays also prevent start-up of the inverter if this DC voltage is not at least at that level.
d) On the DC bus: Instantaneous overvoltage relays (Type NGV) trip the AC input breaker on the battery charger if an overvoltage occurs at this location.
e) On the inverter AC output: Induction disk relays (Type IAV) (if supplied) are of the overvoltage-undervoltage type. They operate to initiate a transfer to by-pass switchgear on incipient failure of inverter output voltage.

MAINTENANCE

A periodic routine of cleaning and inspection should be established. Such cleaning is necessary to prevent faulty operation of a device due to accumulation of dust or corrosion. Inspections should be more frequent if the demands on the equipment are exacting. Under normal conditions, the protective devices do not operate; therefore these devices need careful inspection. Remove dust from all modules & components with a vacuum cleaner or blow out with compressed air.

The listing below is intended as a general guide when visually checking electrical equipment. Frequently such a check will detect a faulty component before its failure causes an outage:

COMPONENT	LOOK FOR
Resistors	Broken, blackened, loose connections
Capacitors	Bulged, leaking, loose connections
Diodes, Transistors	Broken, loose connections
Printed Ckt. Boards	Black spots around components, loose connections, gaps in solder runs.
Pushbuttons &Switches	Binds in shaft, broken or burned contacts
Relays	Charring around coil, dirty contacts
Instruments	Broken case or cover, bent needle
Terminal Blocks	Cracks, loose connections
Wire & Cable	Cracks in insulation, exposed conductor, loose terminations
Contactors	Charring around coil, dirty contacts
Fan Motors	Binds in bearings, loose connections
Circuit Breakers	Broken arc chutes, dirty contacts
Transformers	Charred insulation, loose connections
Bus Joints	Should be tight. Use contact grease if remaking joint.

SECTION 2: BATTERY CHARGER

GENERAL INFORMATION

The battery charger is used with the UPS system to charge the electrical storage battery and to furnish DC current to the inverter. The battery charger utilizes a rectifying circuit to convert electrical energy at power frequency to a nominal 405 Volts DC to charge the storage battery. The rectifying elements of the battery charger are silicon controlled rectifiers which are arranged in a three phase full wave bridge circuit. The battery charger equipment is a specifically modified version of the General Electric Silcomatic regulated rectifier.

REFERENCES: GEK-17540 - General Instruction, Inspection and Test Procedures for Silcomatic I.
GEK-13595 - General Instruction, Inspection and Test Procedures for Silcomatic II.

DESCRIPTION OF COMPONENTS

Each battery charger contains the following components:

1) A rectifier transformer used for isolation purposes and to step down the incoming line voltage to the level needed for proper operation.

2) SCR rectifier circuit to convert the incoming AC power to DC power.
3) A DC filter section to smooth out the DC voltage to the load.
4) A DC potential transformer module (DCPT) to obtain a voltage feedback signal.
5) A DC current transformer (DCCT) to obtain a current feedback signal.
6) Regulator-Amplifier Tray Board used to amplify error signal and to produce a DC control signal to control the gate pulse generator.
7) Gate pulse generator tray board to generate pulses for the gating of the thyristors.
8) DC Circuit Breaker, AK-2-50X, manual operation.
9) Instrumentation
   a) DC Voltmeter 0-500 VDC scale.
   b) DC Ammeter suitable scale.
10) Controls
   a) Green light to indicate breaker open.
      Red light to indicate breaker closed.
   b) Alarm Switch: An alarm circuit is provided from the battery charger input breaker to the master control section of the UPS. This alarm is activated whenever the input AC breaker in the battery charger is tripped. The alarm switch, disables this circuit. The AC breaker will be tripped under any of the following conditions:

      1) DC overvoltage
      2) Fan failure
      3) Transformer overtemperature
      4) Loss of 46 V DC supply

   c) Indicating Lights
      1) YIL-1 - "Control Volts OK"
      2) WIL-1 - "Loss of Cooling Air"
      3) WIL-2 - "Transformer Overtemperature"
      4) CIL-3 - "Capacitor Fuse"
      5) WIL-3 - "DC Overvoltage"
   d) Current limit adjustment, on the door of each charger.
   e) "Manual - Auto" switch, places battery charger in one of the two modes of operation.
   f) "Manual Voltage Adjust" Rheostat - Adjust battery charger's output volts when charger is in manual operation.
   g) RHF rheostat on the DCPT tray - Adjust unit output volts when battery charger is in automatic operation.
   h) Reset switch for DC overvoltage circuit.

OPERATION

The incoming power from the Utility Company or from the auxiliary power (Diesel Generators) is fed to the AC bus. The battery charger is connected to AC incoming bus through the input circuit breaker, which is a manually operated device. With the closing of this circuit breaker, the transformer T1 decreases the voltage from 480 VAC to 356 VAC. Transformer T1 is delta-wye connected and feeds into the SCR (Silicon Controlled Rectifiers) modules for rectification.

An SCR is a phase controlled rectifying device which is controlled by applying a signal to the gate lead during the positive half cycle. This causes the SCR to conduct as an ordinary rectifier. When the applied AC voltage reverses in the polarity (anode to cathode of the SCR), the SCR will turn off until the next gate signal is applied.

A filter circuit is placed in the output to limit ripple voltage. The power supply is protected against normal voltage transients, such as produced by switching and other line disturbances, by surge suppressors connected to both the AC and DC buses. A manual operated DC circuit breaker (AK-2-50X) is used for the output disconnect.

Refer to GEK-17540 or GEK-13595 for completely detailed information on Silcomatic operation.

TURN-ON PROCEDURE

The start-up procedure given below is for starting the battery chargers only. For the procedure to start the entire UPS, see Section I.

1. Check Transfer Switch.*
2. Turn Alarm Switch to "ON" Position.
3. Turn Current Limit Potentiometer (On the instrument door) all the way CCW.
4. Close AC Breaker in the switchgear (Breaker can only be closed manually).
5. Turn Current Limit Potentiometer CW until the DC voltmeter reads 405 VDC.
6. Close the DC Breaker (AK-2-50X) in the battery charger.
7. Close the Battery Breaker in the switchgear.
   Note: Do not reverse the order of 6 & 7.
8. Turn Current Limit Potentiometer all the way CW.

* If Transfer Switch is in the "Auto" position, the battery charger will be voltage regulated at a voltage determined by the setting of the RHF rheostat in the front of the DCPT tray, and with a current limit determined by the setting of R79 on the door of the battery charger. If the Transfer Switch is in "Manual" position, the battery charger will operate at an output voltage determined by the "Manual Voltage Adjust" rheostat. CAUTION must be exercised, though, as there is no indication of unit voltage until it is higher than battery voltage and as the regulator is by-passed, there is no current limit on the unit. The battery chargers must be operated in the "Auto" position when connected to the inverters.

OVERVOLTAGE ADJUSTMENT

The overvoltage alarm was factory set for 420 Volts DC.

If the overvoltage relay is to be reset, remove its cover and adjust the Rheostat located within the relay case above the relay. Of course, this must be done with the appropriate voltage at the Rectifier sensing leads since this is where the overvoltage relay is connected.

COOLING SYSTEM

This equipment is forced air cooled by fans. Screens are supplied at the bottom front of the Charger for air intake. The safety devices are so designed such that this unit will not operate without the fans running. These safety features MUST NOT be disabled. Electrical component failure will result if the unit is operated without the fans operating. A white light and bell alarm will indicate cooling air failure. A white light will indicate what the temperature of the transformer is over the normal operating temperature. There is a ON/OFF switch to silence the alarm bell when conditions cause the alarm to be energized, but the light will remain on to indicate there is still a fault in the cooling system.

SECTION 3: INVERTER

GENERAL INFORMATION

An electrical device which converts DC power into AC power is termed an "Inverter". Conceptually, such a device can be thought of as a group of switches which connects the load to a DC bus, and then alternates the polarity of the connection in a regular cycle. Such an arrangement of switches is shown in Figure 4.

In large inverters, such as those used in this UPS, Silicon Controlled Rectifiers (SCR) are used as the switching components. These devices require very little energy to be switched on, have no known wear out mechanism, and are extremely reliable. Thus, they make ideal switching devices. However, the SCR suffers from one serious limitation. Once the SCR has been turned on, and is made to conduct, there is no way to turn it off except to cause the current through the SCR to be reduced to essentially zero. Circuits have been devised to effect this current reversal and they are discussed later under the heading of "Commutation". First however, it is desired to explain the operation of the inverter circuit as a whole. To introduce the commutation circuits into the discussion at this time would only complicate the explanation. Thus the inverter circuits described below will be presented using simple switches. Later it will be shown that each switch can be replaced by a SCR together with its associated turnoff circuit.

Refer to Figure 4A. Assume that switches 1 and 1' are closed and switches 4 and 4' are open. Then the DC voltage will appear at the load with the polarity indicated. After some interval, switches 1 and 1' are opened and switches 4 and 4' are closed. Again, the load is connected to the DC bus, but now the polarity has been reversed (Figure 4B). Next, the switches return to the configuration of Figure 1A. Clearly, if the switches are continually operated in this cycle shown, an alternating voltage will appear at the output terminals of the inverter with the wave form shown in Figure 1C. This is the simplest form of inverter circuit.

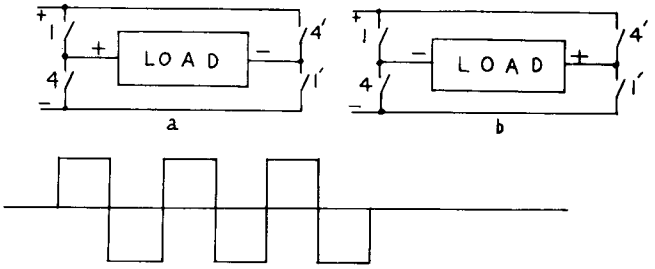


FIGURE 4: SIMPLE INVERTER CIRCUIT WITH OUTPUT VOLTAGE

The simple circuit presented above forms the basis of the inverters used in this uninterruptible power system. However, as it stands, the circuit is not adequate for use in the UPS. The refinements which must be added to the circuit are described below.

1. Isolation: The circuit of Figure 4 shows the load connected directly to the DC bus through the inverter. In actual practice, the load must be isolated from the DC bus. This isolation is accomplished with an output transformer. Also, it will be explained later that if an output transformer is used to couple multiple inverter circuits together to feed a common load, the distortion of the output wave form can be reduced.
2. SCR Switching Devices: As indicated earlier, the switching device used in this equipment are silicon controlled rectifiers (SCR). The circuit of Figure 4 is repeated in Figure 5 below showing SCRs in place of the switches. Also, an output transformer has been shown to couple the load to the inverter. Figure 2A shows SCR No. 1 and No. 1' conducting and SCR No. 4 and No. 4' not conducting. The current path is indicated. The operation of this circuit is identical with that shown in Figure 4.

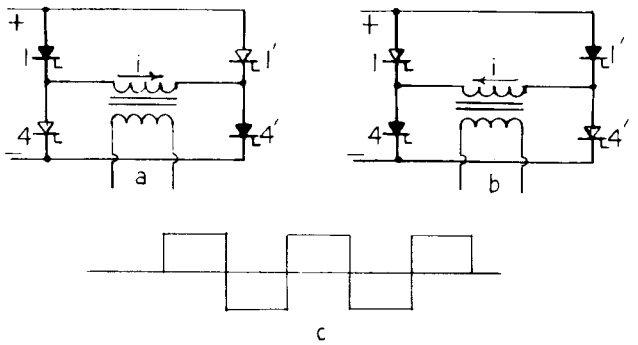


FIGURE 5: SINGLE PHASE INVERTER USING SILICON CONTROLLED RECTIFIERS

3. Three Phase Output
   Most large electrical loads, including the load being served by this UPS, require three phase power. The simple circuit shown in Figure 4 or 5 gives a single phase output. Consequently it must be combined with two other such circuits to form an inverter which yields a three phase output. The circuit configuration which gives a polphase output is discussed in greater detail under "Polyphase Inverters".
4. Reduced Distortion
   The critical load which is being supplied by a UPS requires an input voltage which is sinusoidal. However, the inverter output waveform shown in Figure 4C is a square wave. The difference between the two waveforms is known as distortion. Although the mathematics are beyond the scope of these instruction; it can be shown that the difference between the sine wave and the square wave consists of an infinite number of sine waves. These sine waves are at frequencies which are odd multiples of the basic frequencies of the waveform. (If this fundamental frequency is 60 CPS, the distortion will be at 180 CPS, 300 CPS, 420 CPS, etc.). Before the output of the inverter can be applied to serve the critical load, means must be found to filter out these higher harmonics so that only fundamental sine wave remains. Part of this filtering is accomplished with "line filters" and part is accomplished by the interconnecting of the output transformers.
5. Voltage Control
   The output voltage of Figure 4C is directly proportional to the DC bus voltage. If the DC bus voltage drops by 10 percent, as it will when an electrical storage battery is discharging, the output of the inverter also drops by 10 percent as well. Such a drop is not acceptable for an uninterruptible power system. It will be shown later that by Gating SCR No. 1' and No. 4; later than SCR No. 1 and No. 4, the output voltage can be varied. Alternately, the inverter output voltage can be held to a nearly constant value despite changes in the D-C input voltage. This function is discussed in greater detail under "Voltage Control".

COMMUTATION

As stated above, each switch that is shown in the inverter circuit actually consists of a SCR together with its associated turn-off or commutation circuit. An SCR is shown symbolically in Figure 6. The terminals labeled cathode and anode carry the rated current of the device (the conduction current). The gate terminal is for the small electrical signal (the gate) which turns the SCR on. Without going into detail, the operation of an SCR is as follows:

1. Initially, the SCR is non-conducting. That is, it will not conduct current in either direction.
2. The small gate signal is applied. The SCR then becomes capable of conducting current in the positive direction only. (Anode to Cathode). Once in the conducting state, the SCR continues to carry current until the current either stops or reverses direction.
3. A mechanism in the circuit, external to the SCR, causes the current to stop. The SCR then reverts to the non-conduction state after an appropriate "turn-off time".

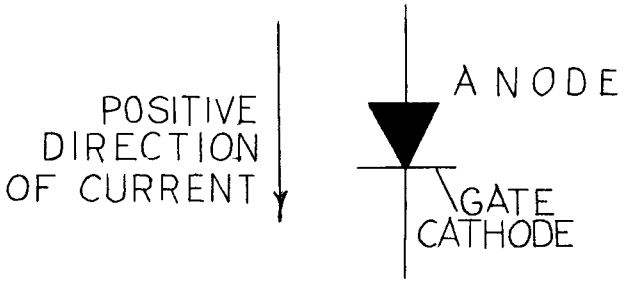


FIGURE 6: SYMBOLIC DIAGRAM OF SILICON CONTROLLED RECTIFIER (SCR)

If further details regarding the SCR are desired, the General Electric Silicon Controlled Rectifier Manual (Fourth edition) should be consulted.

The proper operation of the inverter depends upon the two SCR's that are in series, such as No. 1 and No. 4, not being in a conducting state at the same time. Should such a pair of rectifiers be in a conducting or gated state at the same time they present a direct short circuit to the DC bus. This short circuit is known as a "conduction through" and it causes the protective fuses to rupture and interrupt the current. Thus it is necessary to commutate to zero any current in one SCR at the time its opposite is gated. This action is explained by referring to Figure 7.

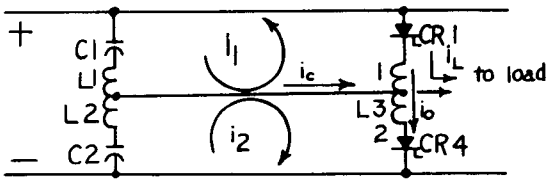


FIGURE 7: SIMPLIFIED INVERTER HALF BRIDGE

When SCR CR1 is conducting, capacitor C2 is charged to the DC bus voltage and a constant DC load current I_L flows through CR1 to the load. (It is assumed that there is no change in the load current during the commutating interval).

When SCR CR4 is gated, and allowed to conduct, a DC fault current I_O will begin to build up through CR1, L3, and CR4. The rate of rise of this fault current will be limited by the series reactance of spanning reactor L3. See Figure 8.

At the same time capacitor C2 will begin to discharge (i_2) through L2, 1/2 of L3, and CR4. The transformer coupling between the two halves of the spanning reactor L3 requires equal currents to flow in both halves of the spanning reactor and therefore a current (i_1) equal to the above capacitor discharge current (i_2) must flow through 1/2 of L3, CR1, C1, and L1. This latter current through CR1 is opposite to the load current I_L and the DC fault current I_O. When the commutating current (i_1) flowing in CR1 reaches a value equal to I_L plus I_O, forward conduction through CR1 will cease and this SCR will be able to hold off forward voltage until it is again gated. When CR1 ceases to conduct, capacitor C1 charges to the DC bus voltage and is available to commutate the forward current in CR4 at the proper time.

It should be noted that it has been maintained in a non-conducting state for a specific length of time.

The excess of commutating current over and above $I_L + I_O$ cannot flow backwards through CR1 and therefore flows through the by-pass diode (D1) establishing a negative bias on the controlled rectifier as shown below:

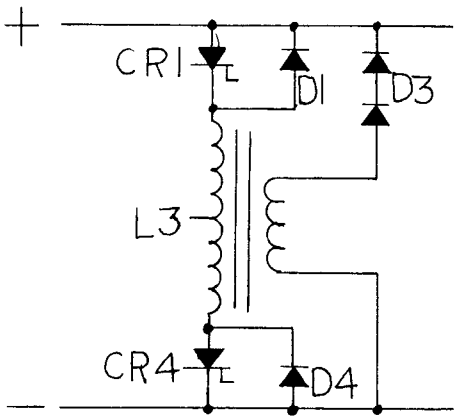


FIGURE 8: INVERTER HALF BRIDGE WITH SPANNING REACTOR

During proper operation, SCR's CR1 and CR4 are alternatively gated every 180 degrees. Thus CR1 and CR4 become conductive and non-conductive every 180 degrees to produce the square wave pulses previously discussed.

Since the commutating currents (i_1 and i_2) flowing in each half of the spanning reactor L3 are equal, these commutating currents build up and decay as sinusoidal currents at rates determined by the natural frequency of C_1, L_1, and C_2, L_2, and independent of the reactance L_3.

As the commutating current i_1 in the upper half of the spanning reactor reduces the net load current, the corresponding commutating current i_2 in the lower half adds to the net load current. Thus the ampere turns in the spanning reactor are maintained at a constant value during commutation. (It is assumed that the load current is constant during the short commutating period).

Referring to Figure 9, prior to time T_O, CR1 is gated on and carrying load current I_L. At time t_O CR4 is gated on and a DC current I_O begins to build up; commutating current at t_1 has built up to a value equal to I_L plus I_O hence forward conduction through CR1 ceases. At this time the excess of the commutating current begins to flow through D1 producing a back bias voltage across CR1. This back bias is maintained across CR1 as long as the commutating current exceeds $I_L + I_O$ or until time t_2.

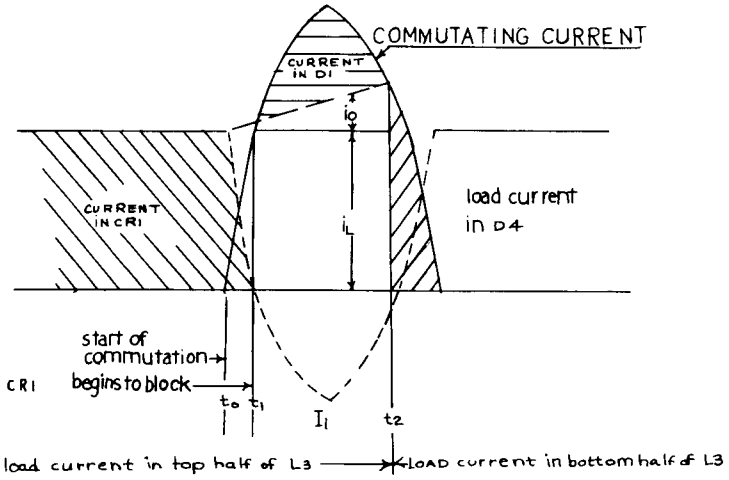


FIGURE 9: INVERTER COMMUTATION CURRENTS

After time t_2, the commutating current is no longer larger than the load current plus the DC current and therefore load current ceases to flow through the top half of the spanning reactor. Part of the load current is supplied from the remaining commutating current and the excess load current flows through diode D4 until such time as the load current reverses.

Just prior to time t_2, the flux in the spanning reactor L3 has been at a level determined by I_1 and I_O. After time T_2 when CR1 and D1 are both blocking this flux must be momentarily changed by the transfer of current to the bottom half of the reactor or to its secondary winding.

The bottom half will assume a current equal to the load current I_L which will now flow through D4. Refer to Figure 8.

The flux level previously maintained by I_O will rapidly decay to zero causing a voltage to appear across the spanning reactor. This voltage adds to the voltage that SCR CR1 must block and is limited by the difference in this voltage reflected into the secondary and the DC bus voltage since the secondary voltage cannot exceed the DC bus voltage when diodes D3 are conducting.

REFERENCE: GEK-492-Impulse Commutated Inverters.

VOLTAGE CONTROL

The inverter circuit described above is capable of providing an adjustable output voltage. This adjustable voltage is necessary so that the voltage regulator of the inverter can

hold the output voltage to nearly a constant value, despite changes in the DC bus voltage or changes in the loading on the inverter.

1) Inverter Half-Bridges

As explained above, the silicon controlled rectifiers always operate in pairs. Whenever one SCR is gated on, this SCR also causes the commutation circuit to "back-bias" and turn off the SCR which is in series with it. Similarly, when the second SCR is gated, the first SCR is turned off. Thus each series pair of SCR's (i.e. SCR No. 1 & SCR No. 4 of Figure No. 5) can be thought of as a single switching unit. This unit is called a "Half-Bridge". Clearly then, each half-bridge always has one of its SCR's conducting and the other SCR is blocking.

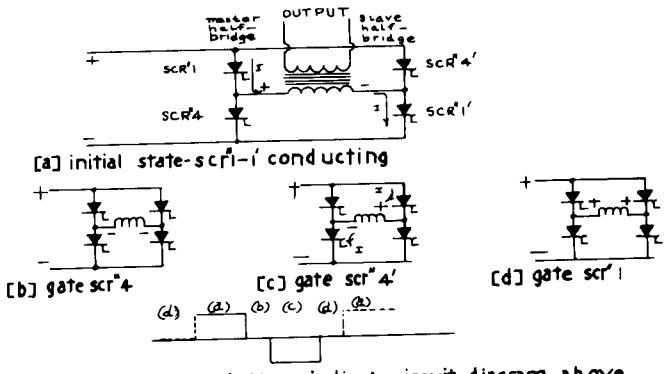


FIGURE 10:
DELAYED GATING OF "SLAVE" HALF-BRIDGE

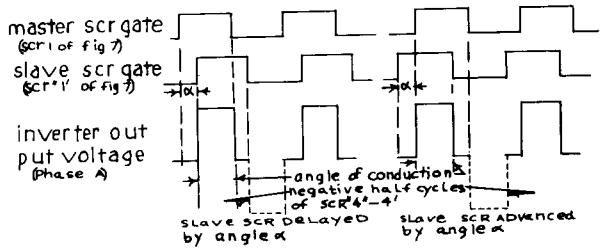


FIGURE 11:
INVERTER OUTPUT VOLTAGE AS CONTROLLED BY DELAYING OR ADVANCING THE SLAVE GATE SIGNAL.

2) Delayed Gating

The single phase inverter shown in Figure 5 consists of two half-bridges, No. 1 - No. 4 and No. 1' - No. 4'. As the operation of this circuit was explained previously, SCR No. 1 was gated at the same time that SCR No. 1' was gated; and SCR No. 4 was gated whenever SCR No. 4' was gated. Thus the two bridges operated in unison, and the output wave form was that shown in Figure 5C. However, the two half bridges need not be gated at the same time. Initially, suppose that SCR No. 1 and SCR No. 1' in Figure 10a are conducting. Next SCR No. 4 is gated, but SCR No. 4' is not immediately gated. During this interval, SCR No. 4 and SCR No. 1' are conducting and SCR No. 1 and SCR No. 4' are blocking (Figure 10b). The output transformer will be connected to the negative bus only, so that there can be no voltage at the inverter output. The operation of half bridge 1' - 4' has been delayed with respect to half bridge 1 - 4. The complete sequence of operation together with the output voltage is shown in Figure 10.

3) Synchronization

It is obvious that both Half-Bridges, 1-4 and 1' -4', must operate at exactly the same frequency and with a preset time delay between them, in other words, the operation of one-half bridge must be synchronized with the other. This is accomplished by using one master gate pulse generator for both Half-Bridges. The Master Gate Pulses Trigger the SCR's of half-Bridge 1-4 directly. The same Master Gate Pulses are also used to generate a second set of Gate Pulses, which are exactly alike except that they are retarded by some controlled time delay. The gate pulses of this second set are termed "Slaves" since they follow and are entirely dependent on the first or Master Gate Pulses. It is an obvious extension of this terminology that half-bridge 1-4 is called the Master half-bridge and the half-bridge 1' - 4' is termed the slave half-bridge.

4) Phase Shift Control

It is obvious from Figure 10 that increasing the delay between the operation of half-bridge 1-4, the master, and half-bridge 1' - 4', the slave, will reduce the width of the voltage pulse in the inverter output. If the maximum amount of delay is employed (180 electrical degrees), there will be no pulse at all so that the output voltage will be zero. The "Effective Value" of the inverter output voltage (the RMS Value) is dependent on the width of this voltage pulse. The same control of the output voltage can also be accomplished by gating the slave SCR before the master SCR is gated. This is shown in Figure 11 as can be seen by comparing Part (a) and (b) of Figure 11, it makes no difference in the output wave form whether the slave SCR is advanced by an amount alpha or is delayed by alpha. In either case, the overlap angle is the same so that the inverter output voltage is the same. Thus varying the delay or advance between the gating of the master and slave half-bridges will control the effective or RMS value of the output voltage.

POLYPHASE INVERTERS

Most large inverters are used to supply three phase loads. An inverter circuit which will deliver a three phase output consists of three of the circuits described above. The switches are operated in the proper sequence to produce

three single phase outputs, each displaced 120 electrical degrees from the others. The circuit is shown in Figure 12. Even though the output of this circuit is three phase, the correct name for the circuit is a "Six Phase Inverter" because it consists of six pairs of switches or six "Half-Bridges".

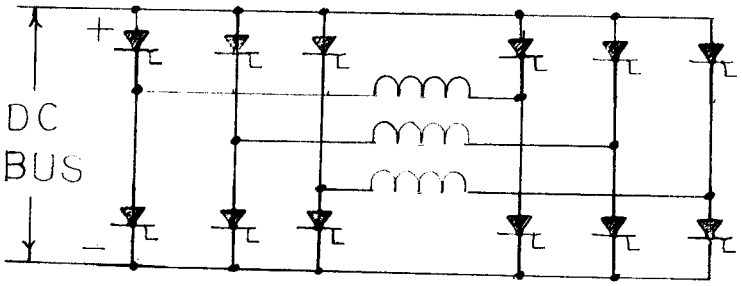


FIGURE 12: SIX PHASE INVERTER

Notice that the inverter again is coupled to the load with an output transformer. The output transformer serves two purposes. First it provides electrical isolation between the load and the DC Bus. Second, the output transformer is used to reduce the distortion of the output wave form so that the output voltage approaches more nearly the desired sine wave. The reduced distortion is brought about because the transformer connection nearly eliminates the "Third Harmonic" and all multiples of the third harmonic from the output voltage. The actual mechanism of the removal of the third harmonic from the output of a three phase transformer is beyond the scope of these instructions, but a full description can be found in a text on three phase circuits. The output waveforms for a six phase inverter are shown on Page 3 of GEK-492.

Further improvement in output wave form can be obtained if the circuit in Figure 13 is employed. This circuit is known as a "Twelve Phase" Inverter.

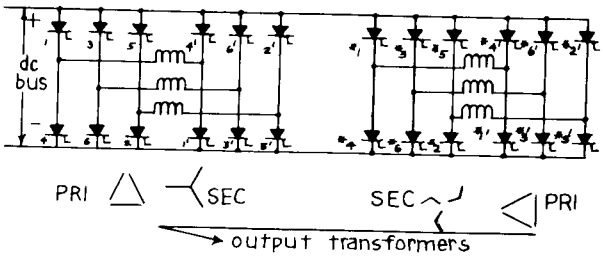


FIGURE 13: TWELVE PHASE INVERTER

As can be seen, it consists of two six phase inverters which are coupled together through the output transformer. (The transformer connections are shown in Figure 18). The twelve phase configuration removes the third, fifth, and seventh harmonics; as well as all of the multiples of the frequencies from the output voltage. A complete set of wave forms for various time delay or retard angles are shown on Page 4 of GEK-492.

Because twelve phase inverters produce output voltages which have minimal distortion, most large UPS systems employ this type of inverter circuit.

POLYPHASE INVERTER CONTROL

In the paragraph above, the inverter POWER circuits have been described in terms of the operation or gating of SCR pairs. It should be obvious from those discussions that unless each SCR in the circuit receives its gating signal at precisely the right moment, the inverter will not operate properly. Accordingly, considerable attention must be devoted to the control circuits which generate and distribute the SCR gating signals. Although the inverter used in this UPS is a 12 phase unit, it will be much easier to understand the control circuits if they are explained for a six phase inverter first.

1) Control for a Six Phase Inverter

A schematic diagram for the control of a six phase inverter is shown in Figure 14. The three master half-bridges are labeled A, B, and C; and the corresponding slave half bridges are labeled A', B', and C'.

a) Master Gate Pulses:

Since the inverter must produce a three phase output, it is clear that the three master half bridges must be operated 120 electrical degrees apart (i.e. at 0°, 120°, and 240°). But each half bridge must be gated twice each cycle; once for the upper SCR and 180° later for the lower SCR. Consequently, six master gate pulses are required. As shown in Figure 15, the six gate signals are equally spaced during the cycle (60° apart).

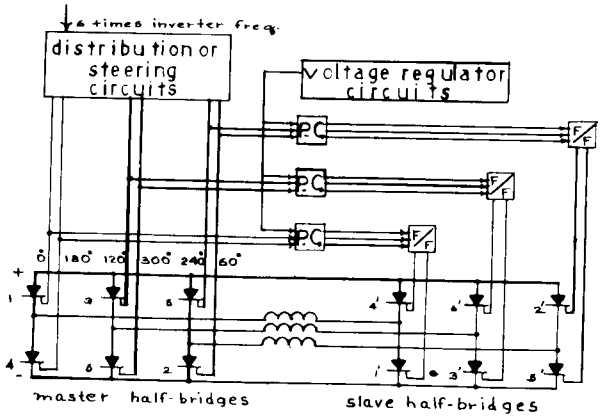


FIGURE 14: CONTROL FOR SIX PHASE INVERTER

Since the six master pulses required each cycle are equally spaced, these pulses are obtained by operating the master oscillator at six times the desired inverted frequency. This train of pulses, shown in Figure 16a, is then sent to a steering circuit which divides the pulses into six separate channels, one channel for each of the six SCR's in the

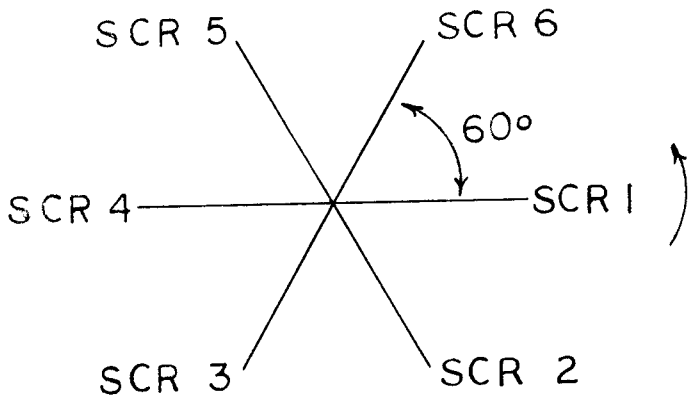


FIGURE 15: PHASOR RELATIONSHIP OF GATE PULSE SIGNALS FOR SIX PHASE INVERTER

master half-bridges. As each pulse is received by the steering circuit, the pulse is directed to the next SCR in the gating sequence. (1-2-3-4-5-6-1-2.....) In this sense, the action of this circuit is very similar to the operation of a distributor on an automobile engine. The original pulse train along with the six gate pulses for the master SCR's are shown in Figure 16.

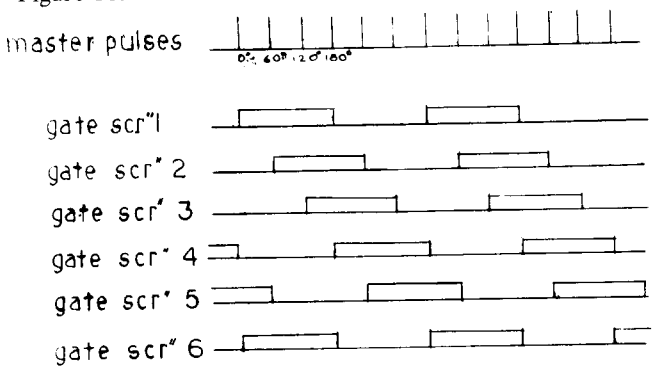


FIGURE 16:
SCR GATE SIGNALS FOR SIX PHASE INVERTER

b) Slave Gate Signals:

Six slave gate pulses are also required, each of which must be synchronized to its corresponding master SCR gate signal. As explained previously, the voltage of the inverter is determined by the length of time during which the master SCR and its corresponding slave SCR are both conducting. This overlap angle can be controlled by either gating the slave SCR before the master SCR or after the master SCR. In this equipment, the slave SCR is advanced ahead of the corresponding master SCR.

The actual circuits achieve this advance in the following way.

The gate for each slave SCR is not triggered by the corresponding master SCR gate signal. Instead, the slave SCR is synchronized with the series mate of the master SCR. (i.e. SCR No. 1' is synchronized with SCR No. 4). If there were no other time delay in the slave gating circuit, SCR No. 1 - 4' would conduct together and SCR No. 4 - 1' would conduct at the same time. This means that the slave half-bridge would be conducting 180 electrical degrees out of phase with the master half-bridge. This would cause the inverter output voltage to be zero.

If additional delay is introduced into the slave gating circuits, the slave SCR's will conduct still later. This means that the slave half-bridge is gated between 180° and 360° after its corresponding master half-bridge. This is equivalent to having the slave half-bridge conduct between 0° and 180° before the master half-bridge. (i.e. if the slave half-bridge conducts 350° after the master half-bridge, it is also conducting 10° before the next pulse of the master half-bridge).

c) Voltage Control:

From Figure 17, it can be seen that the overlap conduction period between the master and slave SCR is equal to the delay in firing the slave SCR. Thus to increase the output voltage of the inverter, the delay in the slave gate must be increased also. The voltage regulating circuits, indicated in block diagram form in Figure 14, compare the inverter output voltage with a reference signal. The result of this comparison is then fed to the phase control boards where it is used to set the desired delay in the slave gating signal.

2) Control for a Twelve Phase Inverter

A twelve phase inverter consists of two six phase inverters operated in unison and which are connected together at the secondaries of the output transformer.

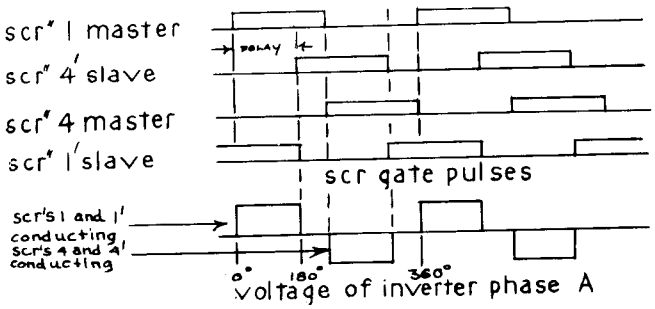


FIGURE 17:
GATING SEQUENCE FOR PHASE "A" OF SIX PHASE INVERTER

A diagram of the power circuits for a twelve phase inverter is shown in Figure 13. It is found that the distortion of the output voltage can be minimized if the secondaries of the two output transformers are connected as shown in Figure 18, and if the two inverters are operated 30 electrical degrees apart.

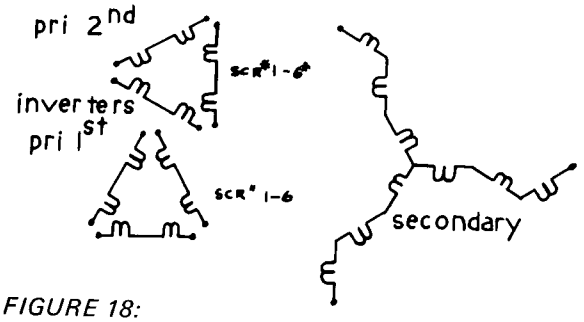


FIGURE 18:
OUTPUT TRANSFORMER CONNECTION FOR TWELVE PHASE INVERTER

a) Master Gate Signals

The 30° displacement between the two inverters is achieved by displacing the master gate signals by this amount. This is shown schematically in Figure 19. Phasors 1-2-3-4-5-6 represent the master gate signals for the first six phase inverter and phasors *1-*2-*3-*4-*5-*6 represent the master gate signals for the second six phase inverter. From the diagram it is seen that twelve equally spaced signals are needed. These pulses are obtained by operating the master oscillator at twelve time rated frequency. The steering circuit then divides the pulses into twelve separate channels, one channel for each master SCR in both six phase inverters.

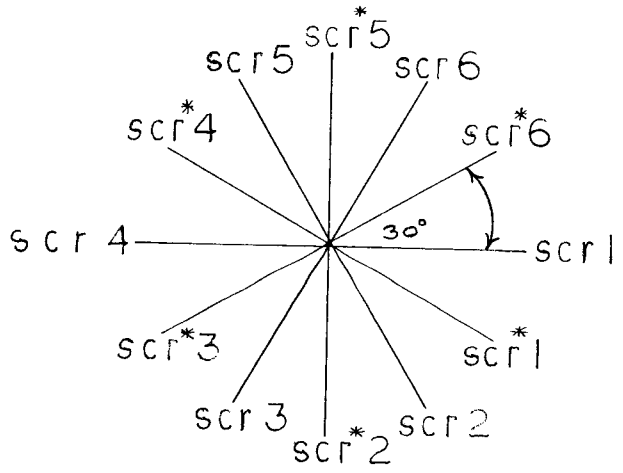


FIGURE 19:
PHASOR DIAGRAM OF MASTER GATE PULSES FOR TWELVE PHASE INVERTER

b) Slave Gate Signals

The gate signal for each slave SCR is obtained in an identical fashion as for a six phase inverter.

SECTION 4: INVERTER AUX. CIRCUITS

GENERAL INFORMATION

The operation of the inverter which was described in section 3 assumes that the equipment is already in operation.

It is the purpose of this section to explain the operation of the auxiliary starting circuit which is required to bring the inverter up to the steady state made of operation. The inverter SCR's must be receiving gate signals before D.C. power is applied to the inverter power circuits. Thus the master control section must be in operation as outlined under turn-on procedure in section 1 before any attempt is made to activate the auxiliary starting circuit.

DETAILED INVERTER STARTING SEQUENCE

The following is a description of the events, some manually initiated, some automatic, which must take place to successfully put the inverter into operation.

1. Manual closing of the double pole knife switch in the D.C. input unit causes the D.C. circuit breaker undervoltage device to pick up through the lockout relays, blower alarm relay, and undervoltage relay contacts, all of which must be in the closed position, indicating normal operating conditions. The yellow indicating lamp comes on, showing presence of control power in this circuit.

2. Manual closing of the D.C. circuit breaker causes pick-up of the blower time delay relay thru an auxiliary contact on the D.C. circuit breaker. The discharge resistor contact also picks up, removing the discharge resistor from the D.C. bus. In addition, the time delay relay for the main contactor picks up. Its contact opens immediately since this time delay is on drop out. Note that the blower time delay relay contacts do not pick up for about 10 seconds to give the inverter time to bring the blowers up to speed.

3. D.C. voltage is applied to the inverter power circuits thru the 3.5 ohm charging resistor. Since the input capacitors in each inverter cart are initially uncharged, the D.C. ammeter will jump to about 100 amps. As these capacitors charge up, the input current should reduce to about 30 amps. (If the ammeter stays at 100 amps, the inverter has had a conduction through. The operator must immediately open the D.C. input circuit breaker to disconnect the inverter. He should then wait a few seconds and try again).

4. As the capacitors begin to charge up, the D.C. voltage at the inverter cart increases. When this voltage reaches about 300 volts the charging resistor contactor picks up. Its main set of contacts short out a portion of the charging resistor, leaving only 0.5 ohm in series with the inverter carts. The input current again jumps to about 100 amps and then starts to fall off as the inverter capacitors accumulate more charge. An auxiliary contact of the charging resistor contactor opens and de-energizes the time delay relay for the main contactor. After about 1 second, the normally

closed contacts of this relay revert to the closed position, energizing the main contactor which now closes in.

5. When the main contactor closes, it shorts out all of the starting resistor and applies the D.C. bus voltage directly to the inverter power circuits. In addition, auxiliary contacts "seal in" the main contactor coil and pick up the undervoltage device on the A.C. output breaker. This permits the A.C. output breaker to be closed when desired.
6. As D.C. voltage is applied to the power circuits, the inverter will begin to commutate and develop an A.C. output voltage. This will start the equipment blowers. As the blowers come up to speed, the centrifugal switch in each motor will close to provide a closed circuit for the fan alarm relays.

The inverter is now operating as described in section 3 and is ready to have load applied.

SECTION 5: MASTER CONTROL

GENERAL INFORMATION

This section describes the electronic control circuits which generate, shape and channel the pulses required to control firing of the inverter SCR's. It also covers the circuits which regulate the inverter output voltage. In addition, it explains the operation of the electronic power supplies which furnish excitation voltage for the pulse generation, shaping, control and regulating circuits.

The master control circuits are so constructed that the components are mounted on printed circuit boards, and there is, generally speaking, a separate board for each major function. Hence the expression "oscillator board", or "phase control board", or "master flip-flop board". Note that this construction allows entire circuits to be replaced or interchanged.

In a redundant type UPS, the redundancy is achieved in certain critical circuits by the use of 2 identical printed circuit boards operating simultaneously to perform one function. Obviously, the failure of one such circuit in a redundant supply will not cause interruption of service since the other is available for continued performance. As the term implies, a non-redundant system has only one such circuit board.

MASTER OSCILLATOR

The redundant type UPS is provided with 2 identical master oscillators. Normally these oscillators operate in union, but if one oscillator fails, the control circuits are so arranged that the UPS will continue to function on the remaining oscillator alone. In addition, a sensing circuit is provided to detect the failure of either oscillator and to trigger an alarm on the master control annunciator panel. Furthermore, each is interlocked with the other to insure that both units operate in synchronism. The basic oscillator circuit, interlocking circuit, and failure sensing circuit is constructed on a single printed circuit board. Both boards are mounted in the master control tray of the master control unit. The board assembly is numbered 0207A1424. A non-redundant type UPS has a single master oscillator. The same oscillator board 0207A1424 is furnished, but the sensing and interlocking features are not utilized. The following description is oriented toward a redundant type UPS with its 2 oscillator boards. However, it applies also to the non-redundant control if the alarm sensing and interlocking features are disregarded.

OPERATION

The generation of a train of pulses by the master oscillators is the first step in a chain of events which ends with gate signals of the proper characteristics being distributed to each SCR in the inverter power circuits. Thus, the rate at which the oscillator produces output pulses, sets the frequency of the UPS output voltage. Refer to Figure 20.

The unijunction oscillator is designed to produce voltage pulses to trigger the master pulse circuit. The oscillator produces 8 volts pulses at six times the desired inverter output frequency. The power for the oscillator comes from the 48VDC zener supply in the chopper assembly. This 48V is stepped down to 15VDC by the combination of resistor R1 and zeners Z1 and Z2. When power is applied to the oscillator, capacitor C2 starts charging at a rate determined by its capacitance and by the resistance of R5 and RH1. As C2 charges, it lowers the voltage at the emitter of unijunction transistor Q1. When the emitter of Q1 reaches what is called its "peak point", the base B1 to emitter E resistance (RB1) drops to a very low value (from several thousand ohms to less than 50 ohms). C2 then discharges through R4, R2, and RB1. This discharge current increases the voltage drop across R2 very rapidly. This is coupled to transistor Q2 through capacitor C6, increasing Q2's emitter to base voltage until it turns on. The output pulses are produced then across RH2. The magnitude of the pulses can be varied adjusting RH2. This is factory set and should not be tampered with. To adjust frequency, a frequency adjust potentiometer is located on front of the control tray.

When two separate oscillator circuits are furnished, as in a redundant UPS, a means must be provided to insure that the oscillators operate in synchronism. This is accomplished by connecting pin 35, which is the oscillator output, to pin 27 on the other circuit board. There it is coupled through capacitor C7 to B2 of the unijunction. Thus when one

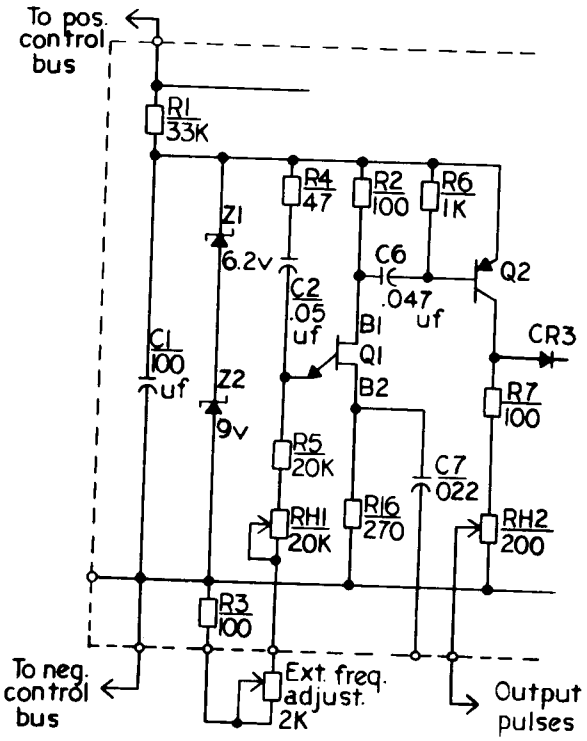


FIGURE 20: PART OF OSCILLATOR CIRCUIT

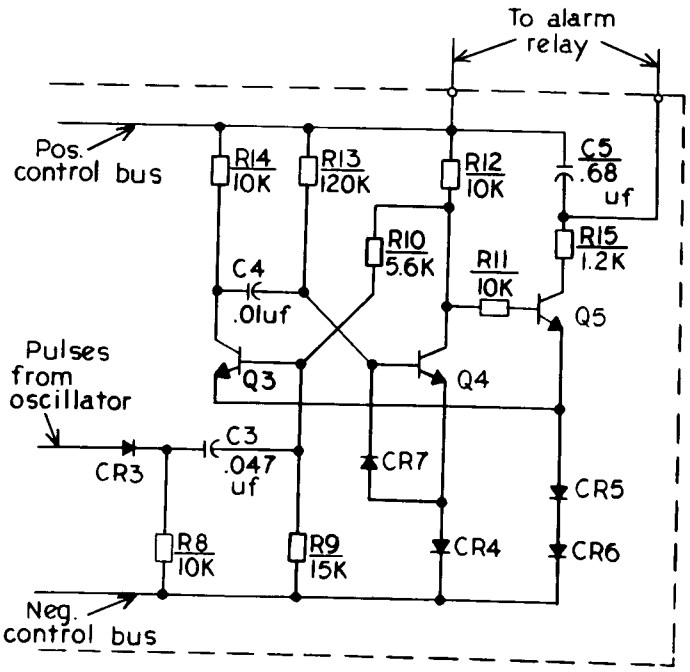


FIGURE 21 OSCILLATOR FAILURE ALARM SENSOR

oscillator produces an output pulse, it raises the interbase voltage and forward biases B1-e on the second oscillator, causing it to generate its pulse at the same time.

Some means must be provided to detect the failure of either one of the 2 redundant oscillators. Otherwise the UPS would continue to operate on only one oscillator and the redundancy feature would be lost. Thus, a failure sensing circuit is provided which energizes a relay whenever the oscillator is delivering a train of pulses. If the oscillator fails, the relay drops out and operates an alarm. This failure sensing circuit, frequently termed a "monostable", has one stable or unexcited state. When a pulse is received from the oscillator, it is excited into an unstable state which energizes a relay. As long as pulses continue to be received, the circuit remains excited which holds up the alarm relay. If the pulses stop, the circuit reverts to its unexcited state which triggers the alarm. The circuit is shown in Figure 21 and it operates as follows. The stable or unexcited state of the circuit is with transistors Q3 and Q5 off and transistor Q4 on. Since Q4 is on, its base voltage is nearly zero. Thus capacitor C4 is initially charged to approximately 50 volts (positive on left). Capacitor C3 is initially uncharged.

The waveforms are shown in Figure 22.

1. A pulse is received from the oscillator through diode CR3. Since the voltage across capacitor C3 cannot change instantaneously, this voltage pulse is transmitted to the base of transistor Q3 and this transistor is turned on. The collector of transistor Q3 then drops to nearly zero voltage.
2. Neither the charge on capacitor C4 nor the voltage across the capacitor can change instantaneously. Thus, when transistor Q3 turns on and the position terminal of capacitor C4 is reduced to nearly zero voltage, the negative terminal of this capacitor must go to approximately 50 volts negative with respect to the negative control bus. The wave form is shown in Figure 22c.
3. This also makes the base of transistor Q4 negative and the transistor turns off. Q4 turning off causes its collector voltage to rise abruptly, which supplies signals to the bases of both Q3 and Q5 and which keeps these transistors on; even though the original pulse has disappeared. When transistor Q5 is on, it energizes the alarm relay.
4. Meanwhile, the charge on capacitor C4 has begun to dissipate through resistors R14 and R13. As capacitor C4 discharges, the voltage on the base of Q4 returns to about .6 volt position, as shown in Figure 22c.
   a. Base of Transistor Q3
   b. Collector of Transistor Q3
   c. Base of Transistor Q4
   d. Collector of Transistor Q4
   e. Voltage Across Relay (Pin "1"5)
5. When the base voltage of transistor Q4 becomes positive again, the transistor turns on, its collector voltage drops to nearly zero voltage, and the base voltage of

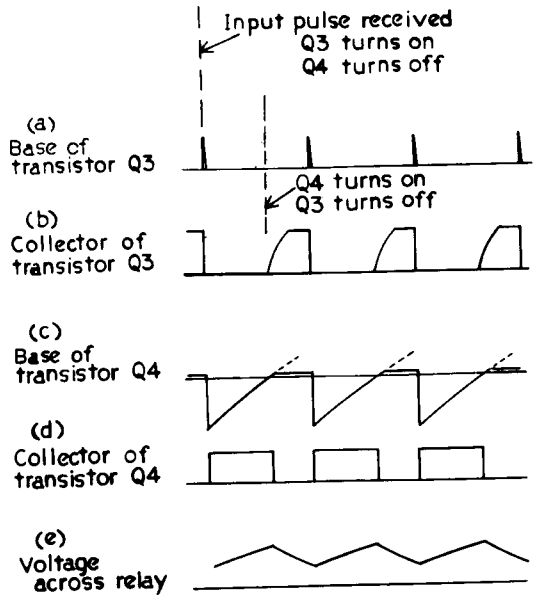


FIGURE 22

transistor Q3 becomes nearly zero. Transistor Q3 then turns off.

6. Transistor Q3 is now off and transistor Q4 is on as in the initial state. Thus, capacitor C4 begins to charge through resistor R14 to approximately 50V.

As long as the oscillator continues to deliver pulses, the circuit will remain energized. If the pulses stop, the circuit reverts to its stable state which triggers the "Oscillator Failure" alarm. The capacitor C5 filters the voltage to the alarm relay, and prevents this relay from "chattering" between oscillator pulses.

FIELD ADJUSTMENTS

The output of each oscillator is tapped off and brought directly out to test jacks on the front of the control tray.

1. Output Wave Form: The oscillator output, as observed with an oscilloscope, is shown in Figure 23. It is recommended that these connections be made only when the inverters are not in operation.
2. Frequency Adjustment: The frequency of each oscillator can be adjusted in two ways.

   a. During normal operation, the UPS frequency can be corrected for minor drift with the adjusting rheostat located on the front of the control tray. This adjustment is actually two rheostats mounted on a single shaft, one rheostat for each oscillator. This rheostat is shown as the 2000 ohm pot. in the oscillator circuit diagram, Figure 20.

   b. The internal trimming potentiometer is located on the printed circuit board. This potentiometer is normally set once at the initial START-UP of the UPS and then not changed unless the oscillator assembly is either repaired or replaced. The potentiometer can be adjusted with a small screw driver while the oscillator board is mounted in the control tray, but should be done during the procedure described in paragraph 3 below.

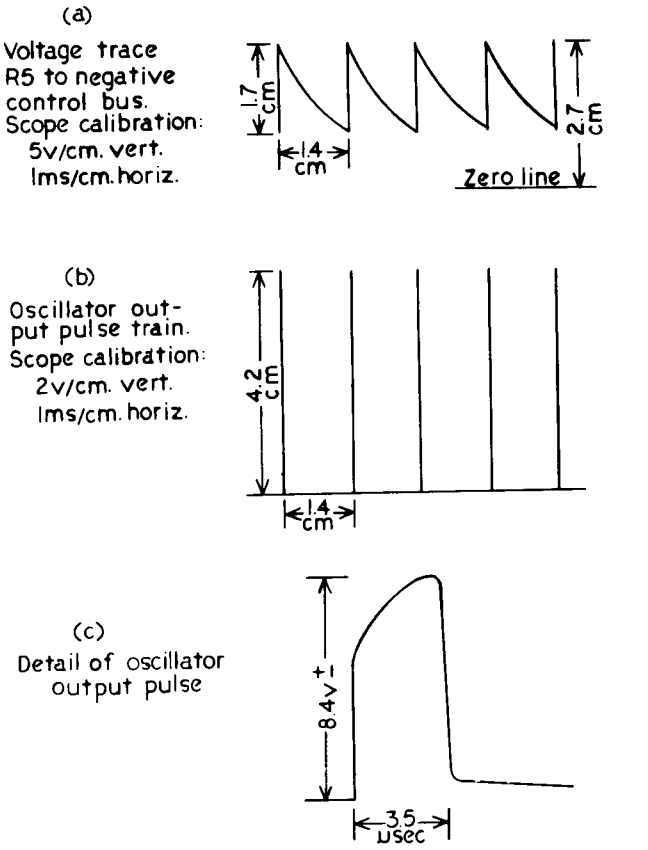


FIGURE 23: OSCILLATOR OUTPUT WAVEFORMS

3. Frequency Setting: During the installation and initial START-UP of the UPS, the trimming potentiometer of each oscillator board should be set such that oscillator delivers twelve times rated frequency (720 Hz) when the external frequency adjustment is set at the approximate center of its range of adjustment. The procedure is as follows:

   a. Insert one oscillator assembly into its assigned slot in the control tray. The other oscillator must be removed from the control tray.
   b. Set the external frequency adjusting rheostat to mid range (approximately 50.0).
   c. Connect the oscilloscope as described in Paragraph 1 above to the output of this oscillator. Set the oscilloscope to "Internal Synch". Adjust the trimming potentiometer until the period between pulses is 1389 micro-seconds. (2 milli-second/division, scale with 6.9 divisions between pulses).

d. Switch the oscilloscope to "Line Synch". The output pulses from the oscillator should appear on the scope, but they will tend to move across the screen. Adjust the trim pot on the oscillator until the pulses stand still on the oscilloscope.

The oscillator has now been synchronized with the 60 CPS utility line. The oscillator should be removed from the control tray and the procedure repeated for the other master oscillator. When both oscillator assemblies have been individually adjusted, they are both installed for normal operation. Note: Before removing either oscillator, disconnect control power first.

4. Alternate Procedure for Setting the UPS Frequency: The procedure described in sub-paragraph 3 above has one inherent danger. The final adjustment of each oscillator depends on synchronizing the 720 Hz oscillator output with the 60 Hz utility line. However, then the oscillator can be synchronized with any multiple of 60 Hz, not just 720 Hz. If this procedure is not carefully followed, the oscillator might be accidently set at either 660 Hz or 780 Hz. This would result in a UPS output frequency of 55 Hz or 65 Hz. It is possible to avoid this problem by using the following procedure instead:
   a. With only one oscillator in place, connect the oscilloscope probe to the output of one of the "flip-flops" in the master steering circuit.
   b. This wave form will be a square wave of approximately 60 Hz. With the oscilloscope in "Line Synch", adjust the oscillator trimming potentiometer until the "flip-flop" wave form stands still on the oscilloscope.
   c. Repeat this procedure with the second oscillator.
5. Setting the Voltage on the 17 Volt Power Supply: This adjustment must be made in the event that component board 0133C6745 must be replaced. Set the voltage level to 17 volts by adjusting trim pot P1 to the 17 volt level between point 3 and point 5 on the terminal board of the chopper. Current limit is adjusted by RH1 trim pot.

MONOSTABLE ASSEMBLY

This discussion of the monostable assembly applies to a redundant type UPS since it is not present on a non-redundant type. In a redundant type UPS, the outputs from the two master oscillators must be combined into a single pulse train to drive the gate pulse steering circuits.

Moreover, the UPS must continue to operate despite the complete loss of either master oscillator. Thus the circuit, which combines the two oscillator outputs, must also produce an output pulse train, if only one of the master oscillators is functioning. In addition, the circuit must deliver output pulses of the proper shape to be used with the master pulse steering circuits which follow. The circuit used for this function is termed the monostable assembly. It consists of a monostable multivibrator and a differentiating circuit and is constructed on printed circuit board 0207A1405. The board is mounted in the master control tray in the master control unit.

MULTIVIBRATOR

The monostable multivibrator produces an output pulse when it is triggered by an input pulse from either master oscillator. The circuit is shown in Figure 24. The pulses from the master oscillators are fed into the monostable circuit through diodes CR4 and CR5. These diodes prevent the output from one oscillator from affecting the other oscillator. The circuit takes its input power from either of two regulated power supplies through diodes CR9 and CR10. These diodes prevent a short circuit in one power supply from affecting the output voltage of the other supply. The monostable assembly can operate from either power supply. The multivibrator has only one stable state: transistor Q2 off and transistor Q3 on. Since Q3 is on, its base voltage is nearly zero. Thus, capacitor C2 is initially charged to approximately 50 volts (positive on left). Capacitor C3 is initially uncharged.

1. A pulse is received from either master oscillator through Diode CR3 or Diode CR4. Since the voltage across Capacitor C3 cannot change instantaneously, this voltage pulse is transmitted to the base of transistor Q2 and this transistor is turned on. The collector of transistor Q2 then drops to nearly zero voltage.

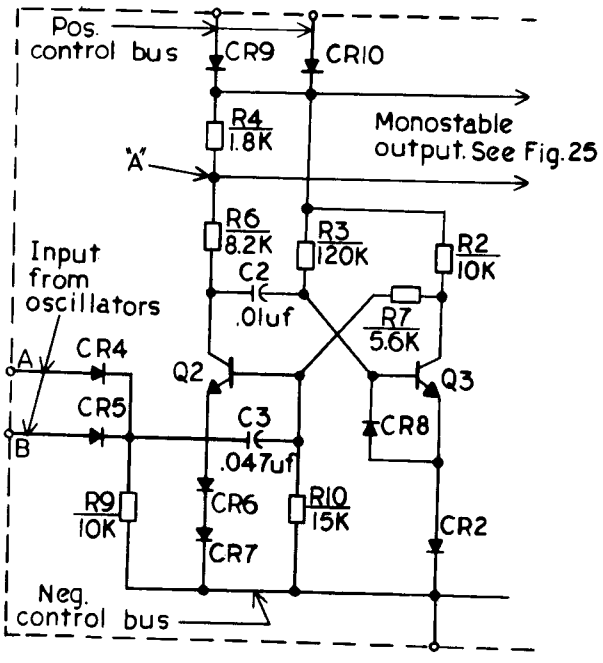


FIGURE 24: MONOSTABLE MULTIVIBRATOR

2. Neither the charge on Capacitor C2 nor the voltage across the capacitor can change instantaneously. Thus, when transistor Q2 turns on and the positive terminal of capacitor C2 is reduced to nearly zero voltage, the negative terminal of this capacitor must go to approximately 50 volts negative with respect to the negative control bus.
3. This also makes the base of transistor Q3 negative and transistor turns off. Transistor Q3 turning off causes its collector voltage to rise abruptly, which supplies signals to the base of Q2 which keeps this transistor on even though the original pulse has disappeared.
4. Meanwhile, the charge on capacitor C2 has begun to dissipate through resistors R3, R4, and R6. As capacitor C2 discharges, the voltage on the base of Q3 returns to about .6 volt positive.
5. When the base voltage of transistor Q3 becomes positive again; the transistor turns on, its collector voltage drops to nearly zero voltage, and the base voltage of transistor Q2 becomes nearly zero. Transistor Q2 then turns off.
6. Transistor Q2 is now off and transistor Q3 is on as in the initial state. Thus, capacitor C4 begins to charge through resistor R14 to approximately 50V. The circuit has now reverted to its stable state.

During the period when Q2 was conducting, current was drawn through resistor R4. Thus, a voltage pulse was produced across R4.

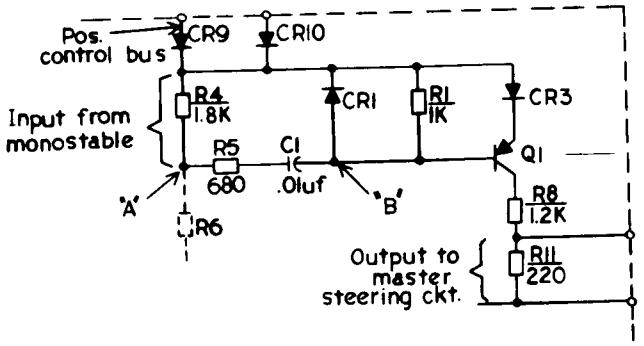


FIGURE 25: DIFFERENTIATING NETWORK

DIFFERENTIATOR

The output of the monostable multivibrator is approximately a square wave. However, the input to the master pulse steering circuit must be a series of pulses, each of relatively short duration. The conversion of the monostable circuit output to a pulse train for the steering circuits is accomplished with a differentiating circuit as shown in Figure 25. Initially resistor R1 and diode CR3 insure that the emitter junction of transistor Q1 is back biased. Thus, transistor Q1 is non-conductive and no voltage appears across resistor R11, the output.

1. When transistor Q2, shown in the mono-stable circuit of Figure 24, begins to conduct, the voltage at point "A" of Figure 24 & 25 abruptly drops from about 50 VDC to about 40 VDC. Since capacitor C1 cannot absorb this abrupt voltage change, point "B" in Figure 25 also drops to about 40 VDC. This forward biases the emitter junction of transistor Q1, and the transistor turns on. The resulting current through resistor R11 produces an output pulse.
2. Meanwhile, capacitor C1 has begun to charge through resistors R1 and R5. As the voltage across C1 increases, point "B" again returns to 50 VDC which turns off transistor Q1 and terminates the output pulse. Thus, the duration of the output pulse is established by the time constant of R1, R5 and C1.
3. Later, when transistor Q2 of the mono-stable circuit turns off, point "A" reverts to 50 VDC and C1 discharges through diode CR1 and resistors R4 and R5.

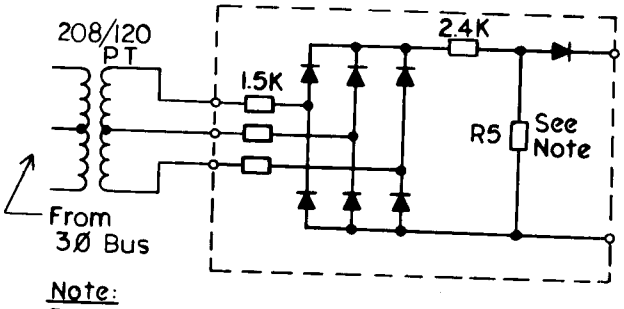
VOLTAGE REGULATOR

The UPS incorporates a closed loop voltage regulation system, which will keep the output voltage at a desired level. The central regulator circuit (0207A1307) in the master control tray, controls the phasing for all inverters and thus controls the output voltage level of the UPS. Each inverter has an auxiliary feedback circuit (0207A1305) which feeds a common bus connected to the input of the master regulator. An auxiliary feedback circuit (0207A1306) is connected to the main load bus, but feeds the central regulator a voltage slightly higher than the auxiliary feedback circuits of the inverters. Thus, the central regulator will normally operate from the voltage signal that is from the main bus.

1. Auxiliary Feedback Circuit
   a. Function: The auxiliary feedback circuits are used to sense the output voltages at each inverter and at the main output bus of the UPS. The circuit then converts the three phase output voltages to DC voltages to provide an input signal for the central voltage regulator. The assemblies, excluding the potential transformers, are built on printed circuit boards.
   b. Operation: The nominal 208 VAC is fed into the potential transformers and reduced to 120 VAC, which is then fed into the auxiliary feedback circuit. The 120 VAC then enters a bridge rectifier and is converted to DC. The output of the rectifier appears across a voltage divider. The desired voltage appears across resistor R5 and is then fed to the central regulator. The diode is to isolate each circuit from the central regulator input bus. The circuit is shown in Figure 26.

NOTE:

1. Resistor is 160 ohms when circuit is used on main bus (0207A1306).
2. Resistor is 150 ohms paralleled with 820 ohms when circuit is used with an individual inverter.



Note:
Resistor is 160Ω when circuit is used on main bus. Resistor is 150Ω paralleled with 820Ω when circuit is used with an individual inverter.

FIGURE 26: AUXILIARY VOLTAGE REGULATOR

2. Central Voltage Regulator

The Central Voltage Regulator Controls the output voltage of the UPS, and this regulator continually adjusts the UPS output voltage to the desired level. The central regulator accepts DC voltage signals from auxiliary regulator circuits on each inverter and on the main bus and then compares these input signals with a pre-set reference signal. If the output voltage of the UPS should deviate from the desired level, an error signal is generated which will adjust the phasing of the slave SCR's to return the output voltage to the correct value. The regulator consists of a differential amplifier, which includes a reference signal, and an amplifier to increase the gain of the resulting error signal.

a. Differential Amplifier with Reference: See Figure 27. The Differential Amplifier consists of a dual transistor which compares the feedback signal at b2 to a reference voltage produced by the zener diode (ZD2). Zener (ZD2) supplies 6 volts across R20 and the volt. Adjust rheostat. By adjusting the latter, the reference level is lowered or raised to achieve the desired inverter output voltage level.

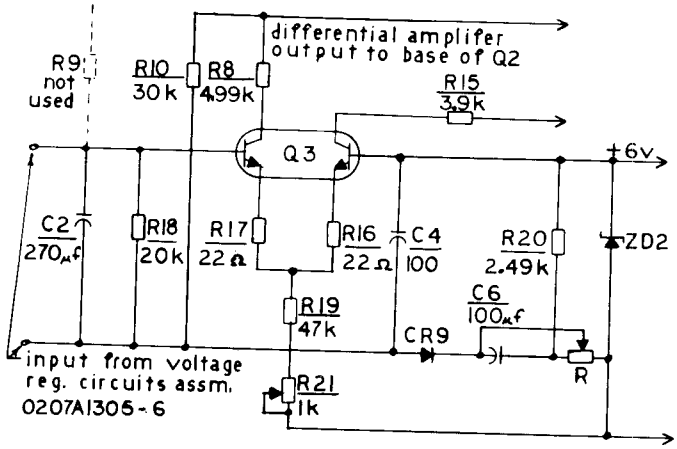


FIGURE 27:
DIFFERENTIAL AMPLIFIER WITH REFERENCE

The reference voltage is then added to the feedback voltage at b2. When combined voltage reaches some critical point, the transistor with base b2 will begin to turn on, and b1 transistor will begin to turn off.

b. Regulator Amplifier: See Figure 28. Turning Q2 off will begin to turn Q4 on thus, reducing the voltage output at point 15. When the feedback voltage is high, the output of the regulator is low. When the feedback is low, output is high. This output is then fed into the phase control boards. Potentiometer R6 is adjusted to set the maximum level of output.

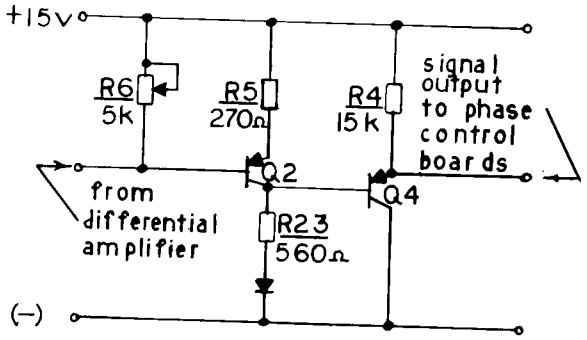


FIGURE 28: REGULATOR AMPLIFIER

PHASE CONTROL CIRCUIT

The Phase Control Circuit consists of three separate parts as indicated in Figure 29. They are the ramp charge circuit, discharge circuit and the level comparator.

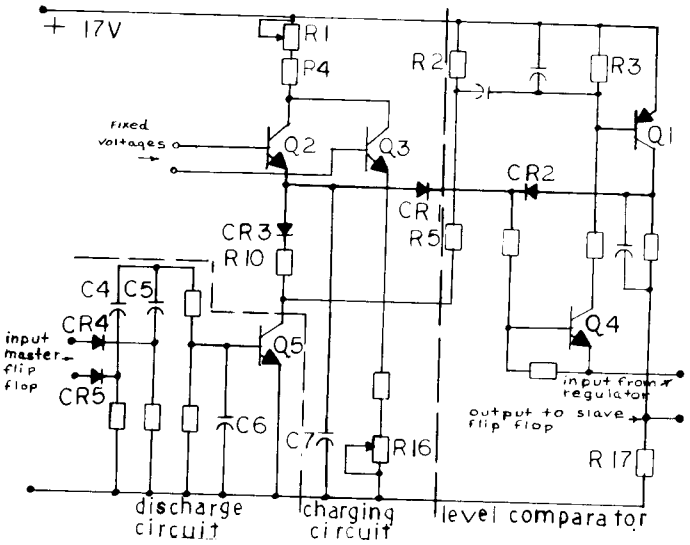


FIGURE 29: PHASE CONTROL CIRCUIT

1. Charging Circuit

The charging circuit is a ramp generator. The linear ramp voltage is generated by a constant charging

current across C7. The bases of Q2 and Q3 are kept at fixed reference voltages. This ramp is most critical. All six phase control boards must be identical as any mismatch will cause unbalance in phase sequence of the slave flip-flop. R1 or R16 provide alignment adjustments.

2. Discharging Circuit
   The discharge circuit function is to discharge the ramp capacitor C7 at the end of each half cycle of the master flip-flop. For pulses see Figure 30 (a and b). The pulses from the master flip-flop enter a differentiating circuit, which produces sharp pulses that turn transistor Q5 on, thus discharging C7, see Figure 30 (c).
3. Level Comparator
   At the beginning of a half cycle, both transistors Q1 and Q4 are off. The emitter of Q4 is held at a reference voltage level established by the voltage regulator and proportioned to the phase shift desired. When the ramp voltage across the capacitor C6 exceeds this reference level, diode CR1 conducts into the base of Q4, which starts to turn it on. Transistor Q4 conducting in turn, draws base current through Q1 thus turning Q1 on. As the collector voltage of Q1 rises above the reference level, diode CR2 conducts more current into base of Q4, thus resulting in positive feedback rapidly driving Q1 and Q4 into saturation. Diode CR1 blocks again and the ramp continues on to the peak point. The positive going signal across resistor R17 is coupled to the slave flip-flops and initiates its switching states. See Figure 30 (e).

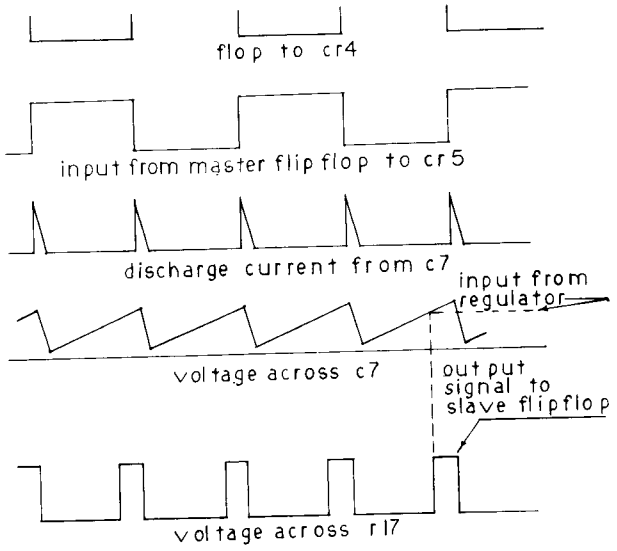


FIGURE 30:
WAVEFORMS FOR PHASE CONTROL CIRCUITS

MASTER FLIP-FLOP

The silicon-controlled rectifiers (SCR) in the inverter are "turned on" (gated) by 180 square wave "gate" pulses. These pulses are generated by transistorized flip-flop circuits that deliver about 100ma into the bases of the amplifier transistor, which feeds the pulses to the SCR's. These flip-flops are bistable multi-vibrators, that are triggered by a combination of pulses from two sources. The pulses that originate in the oscillator are capacitively coupled to the base of each transistor in the flip-flop circuit. Steering pulses are added to either side of the flip-flop through a steering resistor (RS). See Figure 31. Thus, a combination of the oscillator pulses and the steering pulses will turn off the transistor on that particular side that the steering pulses were applied. The steering network time constant is determined by C_S R_S. An auxiliary steering resistor RT is used to insure that the flip-flops start in the proper mode. This is needed on one of the three flip-flops.

Diodes CR1 and CR2 isolate the cross-coupling circuits from the load so that the base current of the flip-flop transistors do not flow through the base of the amplifier transistors that are off. The steering resistors are also decoupled from the amplifier by the same diodes so that the steering transient currents do not affect the amplifier.

When transistor Q2 switches "OFF", its collector voltage drops drawing current through RA, RC and RD, thus turning Q1 "ON". When Q1 turns "ON" a current of about 105ma is taken off the collector and fed into amplifier circuits. The emitter to base current of Q1 establishes a positive emitter to base voltage on Q1 which locks Q1 on.

A similar action takes place in each of the three associated flip-flop circuits which make up the master pulse circuits.

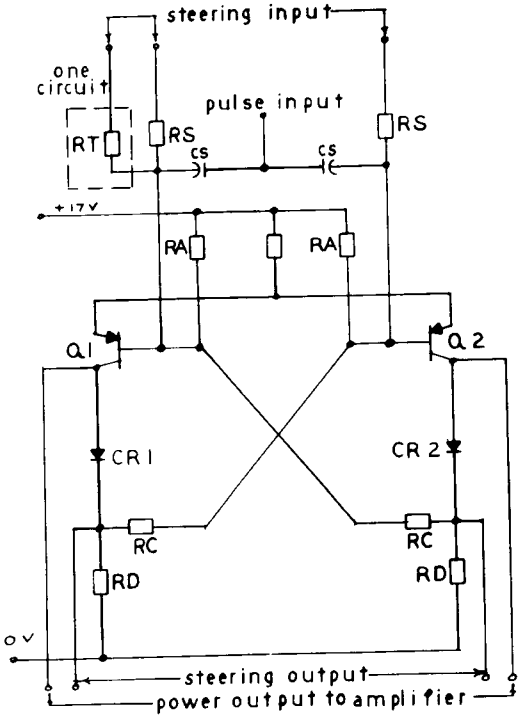


FIGURE 31: MASTER FLIP-FLOP

SLAVE FLIP-FLOP

The slave pulse circuit produces square wave pulses similar to those generated in the master pulse circuit except that the slave pulses are delayed from the master pulses for a controlled period of time. The circuit for the slave is identical to the master, except for the value of the steering resistors; thereby changing its time constant C_S R_S. The slaves are sequenced by the masters, where as, the masters are steered internally.

The switching pulses come from the phase control circuit, and is delayed from the master flip-flop by a variable time. The amount of time that the phase control circuit delays the slaves, will control the phase of the firing of the power SCR's and thus the voltage output of the inverter.

SCR PULSE AMPLIFIER

The gate driver amplifier for the master control circuitry consists of two transistors and is shown in Figure 32. These two NPN transistors are alternately turned on by the positive going signals of their respective flip-flop circuits. The amplifiers feed into a center-tapped transformer operating from a 17 volt dc supply. The inverter amplifier puts out a square wave across the secondary of the pulse transformers, and then feed to the gates of the power SCR's.

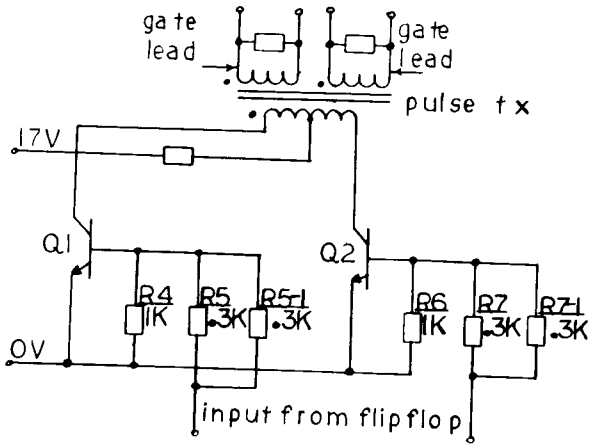


FIGURE 32: SCR GATE PULSE AMPLIFIER

17 VOLT CHOPPER POWER SUPPLY

Refer to Figures 33 & 34.

The 17V control power is derived from the 405V DC bus supplying the inverter power. It is essentially a DC step down circuit which achieves the lower voltage from the higher by time ratio control.

The 17V supply provides power to the pulse delay and gate drive circuits in the control tray. This is a critical voltage and is regulated to very fine tolerance with large swings in input voltage. The step down action is achieved by SCR, saturating autotransformer L1, commutating capacitor C4 and free wheeling diode D4. Reactor L2 and capacitor C6 provide filtering for the 17 volts output. It can be seen that before SCR1 is gated into conduction, C4 will charge up to 405V DC through L1, L2, and the load resistance. When SCR1 is gated into conduction, load current flows through L1, L2, and some charge is delivered to C6. C4 impresses a voltage across part of L1 which in time saturates. C4 then rapidly discharges through SCR1 and part of L1. The energy from C4 is stored in the inductance of L1, so a reversal of polarity takes place charging C4 up in the opposite direction. Eventually L1 saturates in the opposite direction and C4 discharges backwards through SCR1. This action causes SCR1 to turn off. Since a current has built up in L2, it circulates through C6, D4, and L1. The above described action repeats at a rate such that the voltage across C6 is maintained at 17V DC. It can now be seen that the voltage across C6 is proportional to the ratio between the time SCR1 is in the conducting state and the time it is non-conducting, hence, the term time ratio control. The conducting time is controlled by the time taken for L1 to go into positive and negative saturation. The non-conducting time is determined by the frequency of gating SCR1. The voltage across C6 can then be changed or regulated by controlling the frequency of the gate pulse appearing at SCR1.

The gating circuit derives its power supply from zener diode Z3 and resistor R14. A portion of the voltage across C6 appears at the wiper of P1. This voltage is compared through the base emitter junction of Q3 to the reference voltage provided by a zener diode built into reference amplifier Q2. If the voltage at the wiper of P1 is increasing higher than the combined base emitter voltages of Q3, Q2, and the reference voltage, then an increasing current flows from R2 and D1.

This increasing current flows from R2 through D1. This increasing current diverts current from charging capacitor through C2. The resistor R2, capacitor C2, and unijunction transistor Q1 form a relaxation oscillator whose repetition

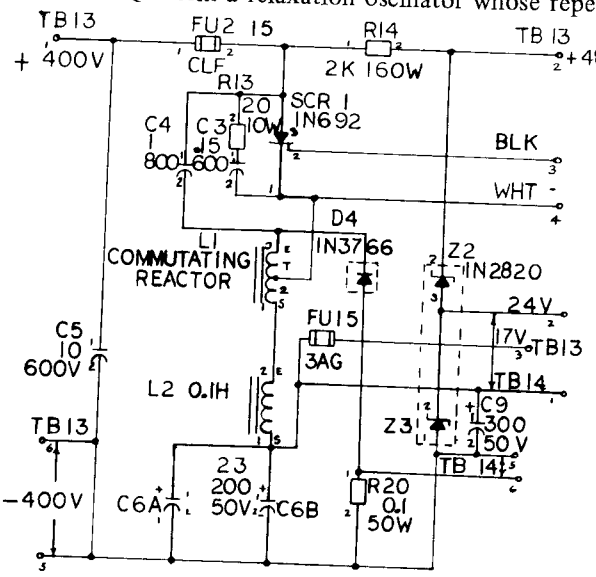


FIGURE 33: 17V D.C. POWER SUPPLY

rate can be varied by varying the charging current to C2. It is obvious then that the current being diverted through D1 and reference amplifier Q2 causes the frequency of the oscillator to slow down. If the voltage of P1 decreases, then the current is reduced (by amplifier action) through D1, and D2 can charge faster increasing the pulse rate to SCR1. Transformer T1 couples the pulses in the oscillator to SCR1 gate. The series connected zener diode Z2 and Z3 supply 48 volts to the oscillator. The 0.1 ohm resistor (R20) provides a feedback proportional to current and provides a current limit feature for the 17 volt supply to protect it from overloading and possible damage. This level is preset at the factory. Do not change it.

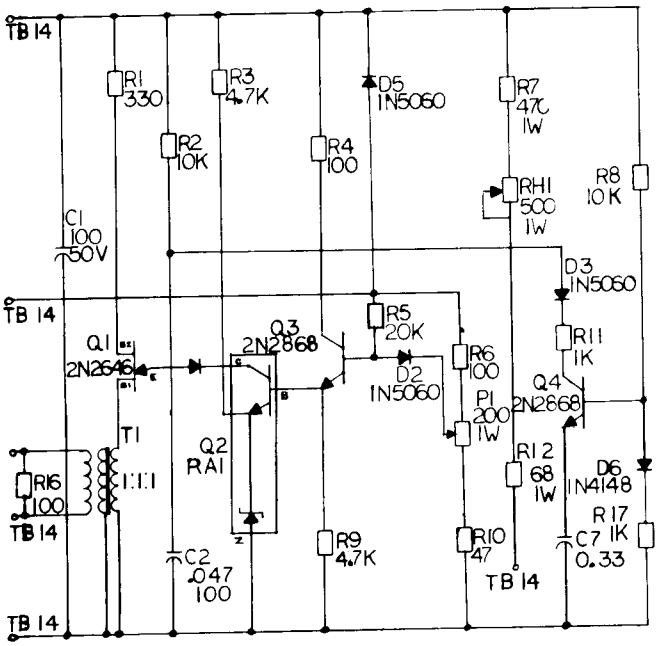


FIGURE 34:
GATING CIRCUIT FOR 17V POWER SUPPLY

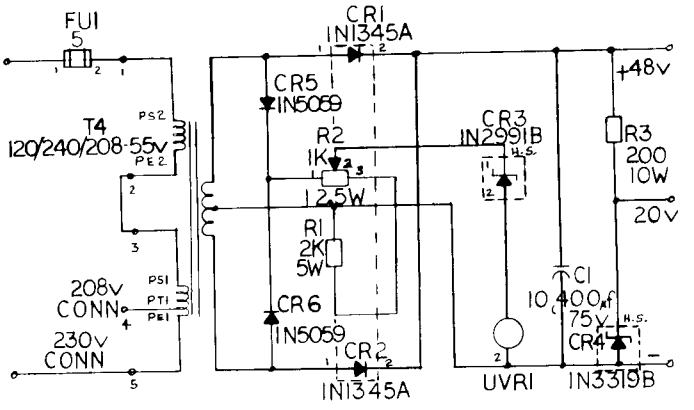


FIGURE 35: 48 V D.C. POWER SUPPLY

48 VOLT POWER SUPPLY

This single phase center tap rectifier takes the A.C. output of the inverter and converts it to filtered 48 volts D.C. See Figure 35. This 48 volts is used to supply the control circuits of the impedance inserter (ZI) when present.

SECTION 6: IMPEDANCE INSERTER

GENERAL INFORMATION

The impedance inserter is a special type three phase static circuit breaker. It protects equipment against damage caused by fault currents by stopping the flow of fault current at a magnitude slightly above its trip level. After the fault current is interrupted an impedance is inserted which limits the current conducted to the point of fault until a secondary protective device operates and isolates the fault. If the fault is cleared within 3 seconds, it automatically switches its main power SCRs to "ON" and the normal power flow is restored.

The impedance inserted power circuit is divided into a main three phase power circuit and an impedance limited three phase power circuit. Its control circuit consists of solid state components assembled on printed circuit boards. See Figure 36 for a block arrangement of the power circuit and the control circuit.

During normal operation power flows through the main three phase power circuit. As previously mentioned, at the time a fault occurs the main three phase power circuit is turned "OFF" in micro-seconds, the impedance limited power circuit is turned "ON" and reduced power flows to the fault. The control circuit provides a timing period that allows the limited fault current to flow for a maximum of 3 seconds. If the fault is cleared within the 3 second period so that the current in the power circuit has reduced to the control circuit reset level the main power circuit SCRs are turned "ON" and the impedance limited power circuit SCRs are turned "OFF". This causes the flow of power to be transferred back to the main three phase power circuit. If the fault is not cleared within the 3 second period, then both the main power circuit SCRs and the impedance limited power circuit SCRs are turned "OFF" and the flow of power stopped.

In order to turn "OFF" the main power circuit SCRs in micro-seconds when a fault occurs, a commutating capacitor circuit is connected to each SCR. A commutating capacitor circuit consists of a power capacitor, a reactor and a power SCR connected in series. The three components are then connected in parallel with each main power circuit SCR. At the time a fault develops the main power circuit SCRs are turned "OFF" in micro-seconds as follows: the gate signals to the main power circuit SCRs are stopped; the gate signals to the commutating circuit SCRs are started; the

commutating circuit SCRs turn "ON" and the energy stored in the commutating capacitors discharges through the associated main power circuit SCRs in the reverse direction to its normal current flow and commutates the main power circuit SCRs to "OFF".

Actually the reverse current flow causes the current in each main power circuit SCR to reduce to zero and then to go negative momentarily as the carriers are swept out of the junction of the SCR. Then the current through the SCR instantly declines to zero and then the SCR turns "OFF". The commutating SCRs are turned "OFF" as follows: after the commutating capacitors are discharged currents flow into the capacitors from the power source and through the commutating SCRs to bring the capacitors voltages to the instantaneous source voltage; because of the circuit inductance the capacitor voltage will overshoot; this causes reverse current to flow through the commutating SCRs and they turn "OFF".

The impedance inserter is built in a 700 ampere frame size. It is installed in an enclosure that has a draw out mechanism. Two exhaust fans located in the top of the cubicle provide cooling air for the power circuit SCRs.

The impedance inserter's green, red and amber lights show through an opening in the enclosure door. The green light is located in the pushbutton section of the "Power Off" switch. The red light is located in the pushbutton section of the "Power On" switch. The amber light is used to indicate that the dc control power is turned "ON".

The rating of the impedance inserter is:

Nominal Operating Voltage . . .	208 Volts
Nominal Operating Current . . .	700 Amperes
Phase	3
Frequency	60 Cycles
Current Trip Level Adjustment . .	Min. 700 Amp. RMS Max. 900 Amps. RMS
Height	28 inches
Width	26 inches
Depth	22 inches
Weight	300 Pounds

The impedance inserter consists of a three phase power circuit and a control circuit. The three phase power circuit is made up to three identical single phase power circuits. Each single phase power circuit consists of: a main power circuit; an impedance limited power circuit; two commutating capacitor circuits and six snubber circuits. The main power circuit has two power SCRs that are connected back to back and two reactors. A reactor is connected in series with each SCR. The purpose of the reactor is to limit the rate of rise of current through the SCR, limit the maximum short circuit current and magnetically decouple the main power circuit from the commutating circuit. A snubber circuit consisting of a resistor and a capacitor connected in series is connected in parallel with each main power circuit SCR. The snubber circuit limits the rate of voltage rise across the SCR when the SCR is turned "OFF". The impedance limited circuit consists of two power SCRs connected bact to back, a stainless steel resistor connected in series with the power SCRs and a snubber circuit connected in parallel with each of the power SCRs. The impedance value of the stainless steel resistor has been selected to limit the fault current to 700-amperes on a 208 volt three phase power system. The impedance limited circuit is referred to as a by-pass circuit in the instructions.

A temperature detector protects the stainless steel resistors against excessive temperature rise that can occur if the impedance inserter is manually reclosed many times when a fault exists. If the stainless steel resistor temperature exceeds 220°C the temperature detectors normally closed contacts open and a back up circuit breaker trips. The temperature detector contacts close when the resistor temperature drops to 192°C + 8°C.

Each commutating capacitor circuit consists of a power capacitor, a reactor and a power SCR connected in series. A commutating circuit is connected in parallel with each main power circuit SCR. The rating of the commutating capacitor is 1000 micro-farads, 450 volts dc. Actually two capacitors are connected in parallel to obtain the 1000 micro-farads rating. A snubber circuit connects across each SCR.

A charging circuit is provided for continually charging the commutating capacitors. The capacitors charge from 0 to 300 volts dc in less than 500 milliseconds.

The charging circuit consists of a transformer with seven isolated output windings. Six of the output windings connect to six full wave rectifier circuits and the rectifier outputs connect to the commutating capacitors. The output of the seventh winding provides a signal to the control circuit ac undervoltage circuit. If the ac power voltage drops below 100 volts, the impedance inserter will turn "OFF".

The control circuit consists of: Four printed circuit boards, three pulse type transformers, three current transformers and two lighted pushbuttons. The seven printed circuit boards are identified as follows: PCB-02075311, card E; PCB-02075312, card F; PCB-02075313, card G and PCB-02075314, card D. Two of the pulse type transformers are identified as transformers, T1 and T2; these are part of the oscillator No. 1 and oscillator No. 2 circuits respectively. The third pulse type transformer is identified as transformer T3. Its part of the circuit that develops the gate signals for the commutating SCRs. The three current transformers are identified CT-4, CT-5 and CT-6. These current transformers supply the intelligence for the control circuit over-current trip circuit. The two lighted pushbutton are identified "Power Off" and "Power On". A green light is for "Power

Off" and a red light is for "Power On". In addition to the green and red lights an amber light is used to indicate the dc control power is "ON"

PRINTED CIRCUIT BOARD DESCRIPTION

The following is a detailed description of the circuits on each printed circuit board:

PCB-0207A5311 (card E)

The control circuits of card E contain an overcurrent trip circuit and a circuit that trips a back up circuit breaker if a fault exists for 3 seconds. This circuit picks up a reed type relay after 3 seconds and its contacts open the undervoltage relay circuit of the back up circuit breaker.

The power circuit currents are monitored by the current transformers CT-4, CT-5 and CT-6. Voltage signals proportional to current and in phase are sent from current transformers CT-4, CT-5 and CT-6 to card E, pins 35-37, pins 41-43 and pins 47-49 respectively. These signals are rectified and the outputs of the full wave rectifiers are paralleled and fed to a potentiometer R1.

During normal operation when the impedance inserter is turned "ON" the transistors Q2, Q4 and Q7 are turned "ON". When a fault occurs, the signal that appears across R1 increases and the transistor Q1 turns "ON". Next, the schmidt trigger circuit switches to "ON", the transistor Q2 turns "OFF" and the transistor Q3 turns "ON". When the transistor Q3 turns "ON" the voltage across the zener diode Z1 drops below its spillover voltage, the base voltage of transistor Q4 goes to zero and the transistor Q4 turns "OFF". The collector voltage of the transistor Q4 increases to near the 20 volts bus. Simultaneously, four signals are sent out when the transistor Q4 turns "OFF".

1. A pulse goes through the capacitor, C2, and R13 to the base of the transistor Q8. The transistor Q8 turns "ON" for 20 micro-seconds and at this time the transformer, T3, develops gate pulses to turn "ON" the commutating capacitor circuits SCRs.
2. A signal goes from pin 29 to turn "OFF" the oscillator No. 1 and the pulse circuits of cards A, B and C. This stops the gate pulses to the main power circuit SCRs and they turn "OFF".
3. A signal goes from pin 31 to turn "ON" the oscillator No. 2. This starts the gate pulse for the impedance limited circuit SCRs and they turn "ON".
4. A signal initiates the starting of the timing circuit consisting of R11, CR16, R14 and C3. If a fault remains for three seconds the unijunction transistor Q5 turns "ON".

When the unijunction transistor Q5 turns "ON" the transistor Q6 turns "ON" and the transistor Q7 turns "OFF". The transistors Q6 and Q7 and the associated components make up a monostable vibrator circuit. After a 20 micro-seconds timing period the monostable vibrator switches to its "OFF" state, the transistor Q7 switches "ON" and the transistor Q6 switches "OFF". In addition, when the unijunction transistor Q5 fires, a signal is sent out of pin 25 that turns "ON" the control circuit trip lock-out circuit located on card F.

When the current in the power circuit reduces below 600 amperes the schmidt trigger circuit switches to its reset mode and the control circuits return to the normal operating pattern.

PCB-0207A5312, (card F)

The control circuits of card F consists of the following circuits:

1. A circuit that locks-out the control circuit because of the following conditions occurring:
   when the "Power Off" pushbutton is pressed; when an overcurrent fault exist for 3 seconds; when a dc control voltage undervoltage condition occurs and when fault signal is sent from the power inverter fuse monitoring circuit.
2. A circuit that turns "OFF" the lock-out circuit and allows the controls to turn "ON" the impedance inserter.
3. A circuit that provides a 0.6 second time delay period at the time the impedance inserter turns "OFF" due to a fault and this circuit prevents turning "ON" the impedance inserter until after the time delay period has elapsed. The purpose of this time delay period is to provide the necessary time required for recharging the commutating capacitors after a fault condition.
4. An ac undervoltage control circuit that turns "OFF" the impedance inserter if the ac power circuit voltage drops below 100 volts. If the ac power circuit voltage increases above 100 volts during the time the impedance inserter is turned "OFF" due to a low ac control voltage condition it will automatically turn "ON".
5. A circuit that receives the faults signal from the power inverter fuse monitoring circuit.

The above control circuits operate as follows:

1. The circuit that locks out the controls consists of the SCR1, its gate circuits and associated components. To turn on the SCR1 a signal may be fed to its gate circuit from pin 19 through the diodes CR4 and CR5, R7 and R13 or a signal may be fed to its gate circuit from pins 21 and 27. When the SCR1 is turned "ON" the control circuit is locked out and the impedance inserter is "OFF". To turn "ON" the impedance inserter the power on pushbutton must be pressed.
2. The circuit that turns "OFF" the lock-out circuit and

allows the impedance inserter to turn "ON" consists of transistor Q3, capacitor C3 and the resistors R9, R11 and R12. When transistor Q3 is turned "ON" by a signal from card G to pin 31 the charge on the commutating capacitor, C3, discharges and causes current to flow in the reverse direction through SCR1, forces the SCR1 to current zero and slightly reverse and then it turns "OFF".

3. The 0.6 second timing circuit consist of transistors Q1, Q2, Q4 and Q5, SCR2 and the associated circuit components. During normal operation when the impedance inserter is turned "ON" the transistor Q4 and SCR2 are turned on and the charge on capacitor C1 is kept close to zero. Also the transistor Q2 and Q5 are turned "ON", and transistor Q1 is turned "OFF".

   When a fault occurs and the card D transistors Q4 turns "ON" and Q5 turns "OFF", the card F transistor Q4 turns off, SCR 2 turns "OFF" and the capacitor C1 start to charge. This turns "ON" transistor Q1 and in turn transistors Q2 and Q5 turn "OFF". When transistor Q1 is turned "ON" a signal is sent from pin 47, to card D, pin 5 to keep the main SCRs turned "OFF", a signal is sent from pin 37 to card G, pin 27 to keep the by-pass SCRs turned "ON", and a signal is sent from pin 17 to card E, pin 27, to continue timing the 3 second timing circuit of the control trip circuit. After the approximately 0.6 second, the transistor Q1 turns off and allows transistors Q2 and Q5 to turn "ON". The associated control circuits will switch and turn "ON" the main SCRs and turn "OFF" the by-pass SCRs.
4. The ac undervoltage circuit consists of the zener diode Z1, resistors R4, resistor R5, and capacitor C2. When the ac control voltage is normal the zener diode Z1 will spill over and provide a signal to the base of the transistor Q2. Transistors Q2 and Q5 are turned "ON". At this time there will be no signal on pins 17, 37 and 47. A signal is on pin 51 and is sent to card G, pin 23. When the ac control voltage drops below 100 volts the zener diode Z1 stops conducting and this turns off transistors Q2 and Q5.
5. A fault signal from the fuse monitor circuit is received on pin 1. The signal goes from pin 1, R23, CR7, CR6, pin 3 to pin 27 and turns on the lock-out circuit SCR1. At the same time a signal from pin 1, R23, CR7, CR8, C4, pin 7 goes to the card E, pin 21, and develops gate signal pulses for the commutating SCRs. In micro-seconds the main SCRs are turned off.

PCB-0207A5313, (card G)

The circuits on card G consist of the following:

1. The oscillator No. 2 transistor circuits. The transformer, T2, that is part of the oscillator No. 2 is located on a separate control board. The oscillator No. 2 develops six isolated ac voltages from the 42 volts dc control voltage. The six isolated ac voltage are rectified and each rectifier output is 10 volts dc. These six dc voltage supply the gate signals for the by-pass SCRs.
2. A circuit that provides a 200 milli-second time delay after pressing the "Power On" pushbutton before the main SCRs turn "ON". During the 200 milli-second period the by-pass SCRs are turned on. The purpose of turning "ON" the by-pass SCRs first and then the main SCRs is to allow the initial excitation currents to the power inverter ZIG-ZAG transformer to be limited below the trip level of the impedance inserter.
3. Circuits that clamp the oscillator No. 2.
4. Circuits that unclamp the oscillator No. 2. The above circuits operate as follows:
   a. The 200 milli-second time delay circuit is initiated when the "Power On" pushbutton is pressed and transistor Q7 turns on. The capacitor, C1, is charged through transistor Q7, and R17. The unijunction transistor Q8 turns "ON" after 200 milliseconds. When the transistor Q8 turns "ON" it causes several other transistors to switch and the final result is the main SCRs turn "ON". The above timing circuit stops when transistor Q5 turns "ON" and turns "OFF" transistor Q7. The transistor Q5 is turned "ON" when the control lockout circuit turns "OFF", and a signal is sent from card F, pin 35 to card G, pin 5. Also a signal from the collector of Q5 is card D provides a second signal to assure that transistor Q5 turns "ON".
   b. The oscillator No. 2 is clamped when either transistor Q3 is turned "ON" or transistor Q9 is turned "ON". The transistor Q3 is turned "ON" when the transistor Q4 is turned "OFF" and transistor Q10 or Q11 is turned "OFF".
   c. The oscillator No. 2 is unclamped when the transistor Q3 is turned "OFF" and the transistor Q9 is turned "OFF".

PCB-0207A5314, (card D)

The following circuits are located on card D:

1. A 48 volts dc source from the inverter connects to pin 33 (positive) and pin 17 (negative). The power source is used for the control circuit 42 volts control bus. Power for the 20 volts dc control bus is developed from the 42 volts by the zener diode Z1 and its associated circuit R5 and C2.
2. A control circuit connects to the transformer, T1, located on a separate board. The combination form the oscillator No. 1. The oscillator No. 1 develops six isolated ac voltages and each ac voltage is rectified and equal 10 volts dc.

3. A dc undervoltage circuit is developed by the zener diode Z2 and its associated components. When the 42 volts dc control voltage drops below 33 volts the zener diode stops conducting, this causes the transistor Q3 to turn "OFF". A signal close to 48 volts at pin 13 turns "ON" card F-SCR1 and, in turn, the control circuit locks-out and turns "OFF" the impedance inserter.
4. The control circuit "Power Off" transistor clamp circuit. When the transistor Q4 is turned "ON" it clamps the oscillator No. 1 and pick up the reed relay that lites the "Power Off" lite and closes the alarm circuit.
5. The control circuit "Power On" transistor circuit. When the transistor Q5 turns "ON" it lites the red indicating lamp, and simultaneously a signal is sent from pin 11 to card G to assure that the bypass SCRs are turned off.

DETAILS OF OPERATION

The impedance inserter power and control circuits are shown on the elementary diagrams 0669D0879 Sh. 2 and 0669D0880.

Prior to turning "ON" the impedance inserter the 48 volts dc control power and the 208 volts ac control power must be "ON". This turns "ON" the dc undervoltage control circuit and the ac undervoltage control circuit. These circuits must be "ON" before the impedance inserter can be turned "ON".

An amber lite, when "ON" indicates that the DC control power is "ON". When the impedance inserter is "OFF" a green "Power Off" lite is lit. To turn the impedance inserter "ON" press the "Power On" pushbutton. The red "Power On" lite should turn "On".

The impedance inserter power circuit turns "ON" as follows: First, the by-pass SCRs turn "ON" and insert impedance into each power line. This impedance limits the maximum load current to 700 amperes per line. Second, after a time delay period of 200 milli-seconds the main SCRs are switched "ON" and at this time the bypass SCRs are switched "OFF". Load currents up to the selected trip level can flow. The trip level is adjustable between 700 to 900 amperes RMS (980-1275 amperes peak).

The impedance inserter can be turned "OFF" by pressing the Power Off pushbutton. It will turn "OFF" automatically if any of the following conditions should occur:

1. If the currents in the power circuits reach the selected trip level.
2. If the 48 volts dc control voltage decreases below 33 volts, the dc undervoltage circuit will cut-off and turn "OFF" the impedance inserter.
3. If the 208 volts ac control voltage decreases below 100 volts, the ac undervoltage circuit will cut off and turn "OFF" the impedance inserter.
4. If a signal is received from the fuse monitor circuit indicating trouble in the power inverter.

The impedance inserter operates as follows for each of the above conditions:

1. If the trip level is exceeded the power circuits switch in micro-seconds from the main SCRs to the bypass SCRs thus inserting impedance into each power line. At the time the trip signal occurs a 0.6 second timing period is initiated and provides time to recharge the commutating capacitors. After this timing period has elapsed and providing that the load current has reduced below the trip circuit reset level (600 amperes) the impedance inserter will automatically switch from the bypass SCRs to the main SCRs.
2. If the fault has been cleared the main SCRs will remain "ON". If the fault reoccurs the above trip cycle will be repeated. It is possible under certain operating conditions that as many as five trip and reclosure cycles may repeat before the 3 seconds time delay circuit turns "ON" the control circuit lockout circuit SCR. After the lockout circuit is turned "ON" the impedance inserter will turn "OFF". The power on pushbutton must be pressed to turn "ON" the impedance inserter.
3. If a signal is received from the fuse monitoring circuit that indicates trouble in the power inverter the control circuit lock out circuit will turn "ON" and the impedance inserter will turn "OFF" in micro-seconds. To turn "ON" the impedance inserter the "Power On" pushbutton must be pressed.

SWITCHING POWER ON

The following is a description of the operation of the control circuit starting with turning "ON" the impedance inserter. Each component is identified by the letter and number appearing on the drawing and, in addition, a letter indicating the card on which the component is located. As an example "D-Q1" indicates that the component is transistor Q1 and is located on card D. Under normal operating conditions, when the "Power On" pushbutton is pressed the transistors G-Q6 and G-Q7 turn "ON". When transistor G-Q7 turns "ON" the following occurs:

1. It provides a seal-in circuit for G-Q6.
2. It starts the timing circuit that turns "ON" the uni-junction transistor G-Q8 after a time delay period of 200 milli-seconds.
3. It turns "ON" the transistor G-Q4.

The transistor G-Q4 turns "OFF" the transistor G-Q3. This unclamps the oscillator No. 2 and it turns "ON". When the oscillator No. 2 turns "ON" it sends gate signals to the by-pass SCRs. The bypass SCRs turn "ON" and allow excitation currents limited to 700-amperes to flow to the power inverter ZIG-ZAG transformer. The ZIG-ZAG trans-

former excitation currents are directed through the impedance inserting circuits to avoid these currents reaching the trip level of the impedance inserter and turning it "OFF".

When the unijunction transistor G-Q8 fires, a signal is sent from card G, pin 1 to card F, pin 31, to turn "OFF" the control SCR, F-SCR1, of the lock out circuit. When F-SCR1 turns "OFF" the following occurs:

1. Transistor D-Q4 turns off and transistor D-Q5 turns on. When D-Q4 turns off the oscillator No. 1 is unclamped. Gate signals are sent to the main SCRs and they turn "ON".
2. A signal is sent from card F, pin 35 to card G, pin 5 and this signal turns "ON" transistor G-Q5. When G-Q5 turns "ON" it turns off transistor G-Q7. This breaks the seal-in circuit around transistor G-Q6 and G-Q6 turns "OFF". Circuit redundancy provides a second signal that develops when transistor D-Q5 turns "ON" and this signal is sent from card D, pin 11 to card G, pin 3, to be assured that the seal-in circuit is broken and transistor G-Q6 turns "OFF". After transistor G-Q6 and G-Q7 turn "OFF" the 200 milli-seconds timing circuit is stopped, transistor G-Q4 turns off and transistor G-Q3 turns on. When transistor G-Q3 turns "ON" it clamps the oscillator No. 2 to the "OFF" mode. This turns "OFF" the gate signals to the bypass SCRs and they turn "OFF" at the next current zeroes. The impedance inserter is now turned "ON" and it will remain "ON" until it is either manually or automatically tripped.

OVERCURRENT TRIP

The following is a description of the control circuit operation due to an overcurrent fault:

The current transformers CT4, CT5 and CT6 are located on the input power studs and are used to monitor the line currents of phases No. 1, No. 2 and No. 3 respectively. The outputs of the three current transformers are fed to three full wave rectifiers located on the card E. If a fault occurs and the line currents increase to or above the trip level the main SCRs will switch "OFF" and the bypass SCRs will switch "ON" in micro-seconds.

During normal operation card E transistors E-Q2, E-Q4 and E-Q7 are turned "ON" and transistors E-Q1, E-Q3, E-Q5, E-Q6 and E-Q8 are turned "OFF". When a trip occurs the transistors E-Q1 and E-Q3 switch to "ON" and the transistors E-Q2, E-Q4 and E-Q7 switch to "OFF". When the transistor E-Q4 switches to "OFF", simultaneously signals are sent to the following circuits:

1. A signal is sent from card E, pin 29 to card D, pin 25. This signal turns on transistors D-Q6 and D-Q4 and turns "OFF" transistor D-Q5. When D-Q4 switches "ON" oscillator No. 1 is clamped. The gate signals to the main SCRs are stopped.
2. A signal is sent to turn "ON" transistor E-Q8. Transistor E-Q8 and its associated circuit develops six isolated gate pulse signals for the commutating SCRs. The commutating SCRs turn "ON" and commutate the main SCRs "OFF" in micro-seconds.
3. A signal is sent from card E, pin 31 to card G, pin 31 to unclamp the oscillator No. 2 by turning "ON" transistor G-Q4 and turning "OFF" transistor G-Q3. Gate signals are sent to the bypass SCRs and they turn "ON".
4. A signal initiates the 3 second time delay circuit E-R11, E-CR16, E-R14 and E-C3. If the fault remains for 3 seconds the unijunction transistor E-Q5 fires and a signal is sent to turn "ON" transistor E-Q6 and F-SCR1. When E-Q6 turns "ON" the reed relay picks up and trips a back-up circuit breaker. When F-SCR1 turns "ON" it locks out the control circuit.

During normal operation and prior to transistor D-Q4 switching "ON" and transistor D-Q5 switching "OFF" the 0.6 second time delay circuit located on card F is set up as follows:

Transistor F-Q4 and SCR F-SCR2 normally remain in the "ON" mode. Capacitor F-C1 is discharged. The card F, pin 49 that the collector of F-Q4 and anode of F-SCR2 connect to is approximately 0.5 volts from common. The transistor F-Q1 is turned off.

At the time transistor D-Q4 switches "ON" and transistor D-Q5 switches to "OFF" the capacitor F-C1 starts to charge and immediately turns "ON" transistor F-Q1. After a 0.6 second timing period the transistor F-Q1 turns off. When transistor F-Q1 is turned "ON" the transistors F-Q2 and F-Q5 are turned "OFF". At this time a signal from card F, pin 47 to card D, pin 5 keeps transistor D-Q4 turned "ON". This assures that the oscillator No. 1 and the cards A, B and C pulse circuits remain clamped. Thus, no gate signals can be developed for the main SCRs.

Following an overcurrent trip the bypass SCRs are turned "ON" by signals from oscillator No. 2 which are actuated by a signal from card E, pin 31. This signal exists until the card E trip circuit resets. The trip circuit resets when the load current drops below 600 amperes. To assure that sufficient time is available for re-charging the commutating capacitors, a second signal associated with the 0.6 second timing circuit is sent from card F, pin 37 to card G, pin 27. This signal turns "ON" transistor G-Q10. The transistor G-Q11 will be "ON" providing the ac control voltage is normal. The transistor G-Q3 is turned "OFF" and the oscillator No. 2 is unclamped, thus allowing it to supply gate pulses to the bypass SCRs.

The bypass SCRs will remain "ON" until after the elapse of the 0.6 seconds timing period and until the trip circuit has reset. The trip circuit resets when the fault current drops below 600 amperes. If both of the above conditions are met within a 3 second period, the power circuit will

switch from the bypass SCRs to the main SCRs. If the conditions are not met within the 3 second period the control circuit will lockout at the elapse of the 0.6 second timing period following turning "ON" of the control SCR, FSCR1. The control SCR, FSCR1 turns on when the unijunction transistor of E-Q5 fires.

TRIP SIGNAL FROM INVERTER FUSE MONITOR CIRCUIT

The following is a description of the control circuit operation when a trip occurs due to a fault signal from the power inverter fuse detector circuit. When a fault signal is sent from the power inverter to card F, pin 1, the following occur simultaneously:

1. The control SCR, FSCR1 is turned on. This causes the control circuit to lockout as previously explained and the gate signals to the main SCRs stop.
2. A signal is sent from card F, pin 7, to card E, pin 21 turning "ON" transistor E-Q8. This causes a pulse to go through the primary of transformer T3. The outputs of transformer T3 send a gate pulse to each of the commutating SCRs. The commutating SCRs turn "ON" and drive the main SCRs "OFF" in microseconds.
3. A signal is sent from card F, pin 9, to card G, pin 15. The transistor G-Q9 turns on and clamps the oscillator No. 2 "OFF".

   The signal which indicates a fault condition in the inverter must be removed from card F, pin 1, before the impedance inserter can be turned "ON" by the "Power On" pushbutton.

TRIP DUE TO DC UNDERVOLTAGE

If the 48 volts dc control voltage drops below 33 volts, the impedance inserter will turn "OFF". First the zener diode, D-Z2 stops conducting, next D-Q3 turns "OFF", then a signal from card D, pin 13, to card F, pin 21, turns "ON" F-SCR1. When FSCR1 turns "ON" the control circuit is locked out. The main SCRs turn "OFF" at the next power circuit current zero.

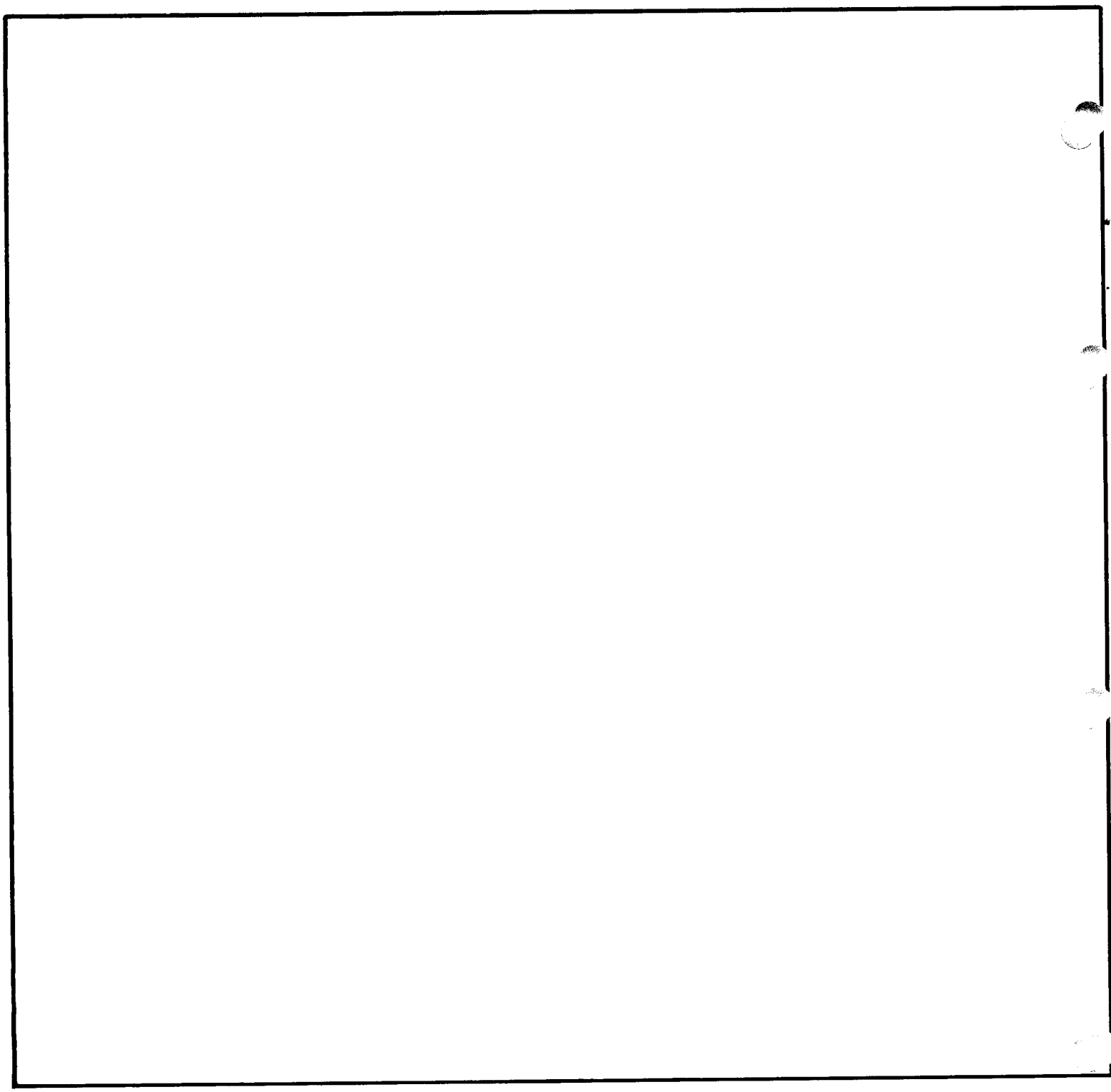
TRIP DUE TO AN AC UNDERVOLTAGE

If the 208 volts ac control voltage drops below 100 volts the impedance inserter will turn "OFF". If the ac control voltage remains below 100 volts for more than 3 seconds, the control circuit will lockout and it will be necessary to press the "Power On" pushbutton to turn "ON" the impedance inserter. If the ac control voltage rises above 100 volts within a 3 second period the impedance inserter will turn "ON". When the ac control voltage drops below 100 volts the zener diode F-Z1 stops conducting. Next, transistors F-Q2 and F-Q5 turn "OFF". A signal is sent from card F, pin 47, to card D, pin 5, thus turning "ON" transistor D-Q4. When transistor D-Q4 turns "ON" the oscillator No. 1 is clamped and the gate signals to the main SCRs are stopped.

In addition, a signal from pin 17 is sent to card E, pin 27, this signal initiates the 3 second timing period that a fault is allowed to remain before the control circuit is locked out. The operation of the 3 second timing period in the trip circuit has been explained under the sub-heading Overcurrent Trip.

MANUAL TURN OFF

Pressing the "Power Off" pushbutton causes a signal to be sent to card F, pin 27, through FR6, F-CR5, FR7 and FR-13 to turn "ON" FSCR1. When F-SCR1 turns on it locks out the control circuit. The main SCRs turn off at the next power circuit current zeroes.



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