Technical reference manual
Phasor measurement terminal
RES 521*1.0

ABB

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Phasor measurement terminal
RES 521*1.0

About this manual:

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Manufacturer:

ABB Automation Technologies AB
Substation Automation
SE-721 59 Västerås
Sweden
Telephone: +46 (0) 21 34 20 00
Facsimile: +46 (0) 21 14 69 18
Internet: www.abb.com/substationautomation

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Chapter 1 Introduction

1 About this manual

This manual contains the complete documentation for RES 521*1.0. It can be used for all purposes from installation to acquiring detailed knowledge about operation and design.

2 Intended audience

The manual can be used by installers, commissioners, operators and system engineers.

2.1 Responsibilities

The reader should have basic engineering knowledge and specific knowledge in system automation depending on purpose.

3 Organization of chapters

The manual is organized into chapters according to the intended audience so that each chapter corresponds to the needs of the reader:

- The application and operation chapters should be read by system engineers and operators.
- The installation, commissioning and requirements chapters should be read by installers and commissioners.
- The functional description and design chapters should be read by anyone interested in the product’s functionality and design.
- The diagrams section should be used by installers, commissioners and system engineers in order to create connection tables and cabling drawings.

Chapter 2 Application

This chapter describes the application of RES 521*1.0.

4 Introduction

RES 521*1.0 is a Phasor Measurement Terminal, that provides power system AC voltages and currents as phasors, i.e. as real and imaginary parts or as magnitude and phase angle. The reference for the phase angle is the NavStar Global Positioning System, GPS, that also supplies highly accurate time and date. The accurate time tagging of measurements taken at different geographical locations makes it possible to derive the phasor quantities. Based on phasors a number of power system applications becomes available.

5 WAMS applications

Phasor Measurement Units (PMUs) have so far mainly been used for recording and on-line supervision, Wide Area Measurement System (WAMS) applications. In a typical setup 10-20 PMUs, at different locations in a synchronized power network, stream phasor data, together with power flow data, frequency, etc., to a data concentrator. The data concentrator usually is a mass storage with capacity for about one week of data in a FIFO buffer. In case of any disturbance it should be very easy to access the data recorded to support the disturbance analysis process. The phasor data is normally sent from the PMU to the data concentrator at a speed of 25/30 or 50/60 samples per channel and second. The number of sampled channels is typically 10-20. Phasor data is normally understood as the magnitude and phase angle of the positive sequence voltage or current. The common reference for the angle measurement is the GPS system, which provide a very precise time reference. Since every measurement sent to the data concentrator is time tagged, any angle difference between power system AC quantities can be derived.

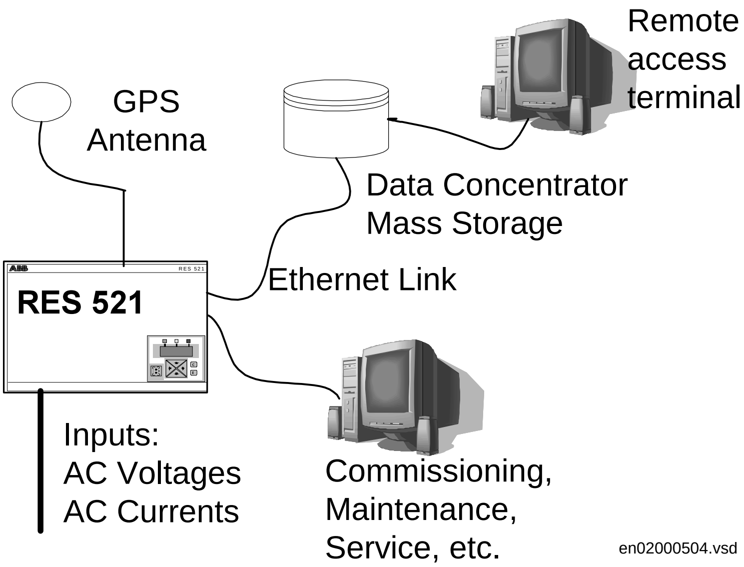


Figure 1: Typical PMU application in a WAMS environment.

6 State estimation

If PMUs are installed in a larger number of busbars in a power system, their output phasor data can be used for improved state estimation - to improve the SCADA system state estimator or, if the amount of PMUs is enough, to replace the state estimator.

7 HUB based protection system

If the data concentrator in a WAMS application is extended to also include protection and control algorithms and a possibility to send action signals, a wide area protection system is designed. Such a system can be supplied by a few PMUs up to tens of PMUs, depending on the size of the power system and the complexibility of the protection functions.

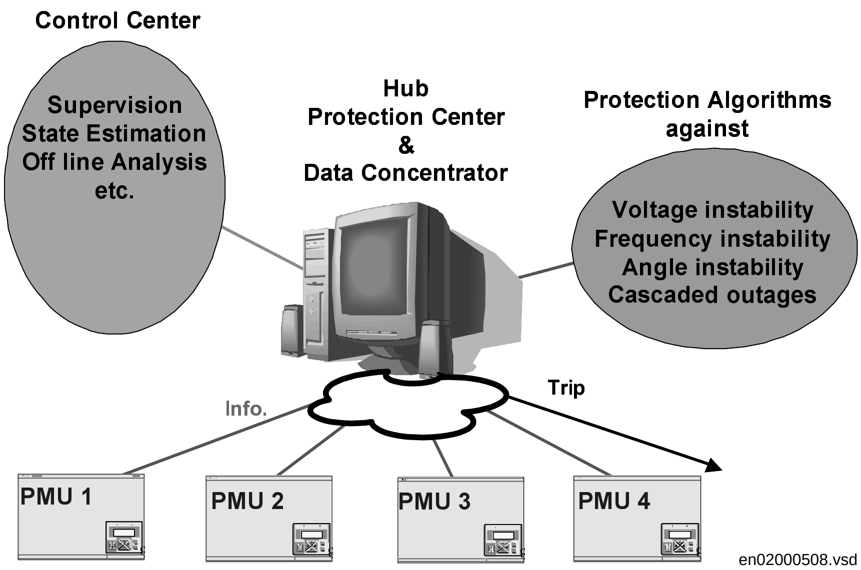


Figure 2: HUB based wide-area protection system.

8 PMU stand alone applications

A limited number of PMUs can exchange data to derive power system phase angles. Based on these angle quantities, alarms can be given to the operator, but actions can also be ordered directly in the power system, in order to avoid out-of-step conditions or to improve damping in case of power oscillations, see figure 4. Control orders can for damping purposes be executed by SVCs, AVRs on generators, turbine governors on generators or by switched braking resistors.

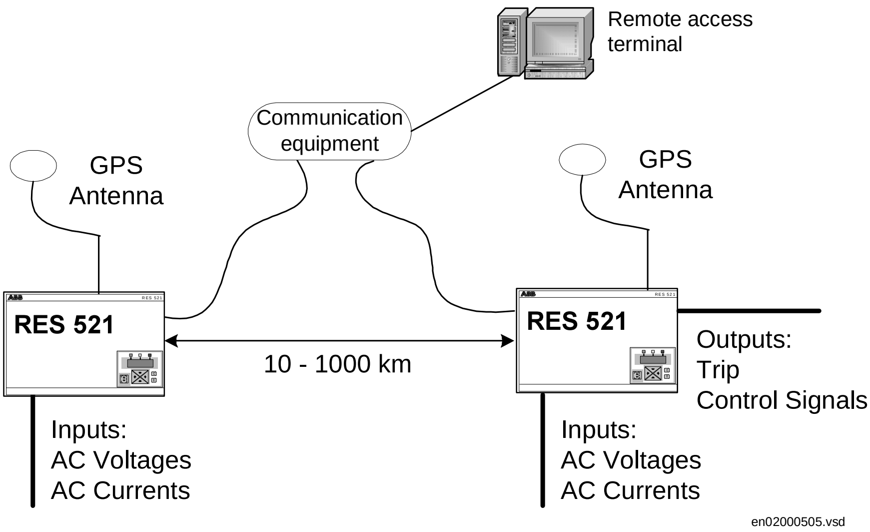


Figure 3: Example of a 2-PMU stand alone control system for power oscillation damping.

9 General wide-area protection design

All control and protection systems have the basic functions: indicators, algorithms and actions. Below some examples for wide-area protection systems are shown.

Table 1: Wide-area protection basic functions

Indicators	Algorithms	Actions
• Angle voltage/current • Angle difference • Rate of change of angle • Power flow	• Less Than/Greater Than • 2 out of 3, etc. voting systems • Robust binary logic • 1st swing algorithms • Damping algorithms	• Load shedding/switching • Governor boosting • HVDC support • Breaking resistors • AVR boosting • Shunt device switching

10 Mobile PMUs for line parameter calculation

Portable PMUs can be used to calculate line parameter values, such as resistance, inductance, and capacitance. If different loading conditions, voltage levels, etc., are used, also corona effects and zero sequence parameters can be calculated.

Chapter 3 Requirements

This chapter describes the requirements of surrounding equipment, environmental requirements, etc.

11 General

This chapter specifies the requirements of inputs and outputs, DC-supply and environmental conditions.

12 Galvanic Ethernet

A galvanic Ethernet communication port (RJ-45), is located at the back of the terminal.

13 Fiber optic Ethernet: 100 Base-FX

Fiber optic Ethernet can be chosen as an option. It is, however, not possible to use both galvanic and optic Ethernet. Use glass fibers according to the following table.

Table 2: Fiber optic requirements

	Glass fiber
Cable connector	ST style connector
Fiber diameter	62.5/125 µm
Max. cable length	2000 m

14 DC-supply

The auxiliary DC-supply level must be within 24-60V or 90-250V depending on ordered module. The DC-supply shall be connected to X141:4 (+) and X141:5 (-).

15 Binary inputs and binary outputs

The voltage level of the binary inputs/outputs has to be ordered: 24/30 V, 48/60 V, 110/125 V or 220/250 V. The voltage level shall then be within 19,2-36 V, 38,4-72 V, 88–150 V, and 176-300 V, respectively, since the binary input/output module can accept input voltages within +/- 20% of the nominal value. The binary inputs should be connected to X91:1-16. The binary outputs should be connected to X92:1-18. The details of the connection diagrams are shown in the terminal diagram drawings at the end of this manual, see Chapter 10 "Terminal diagrams".

16 Analog input voltage

Rated AC phase-phase voltage for the analog input module is 100/110/115/120 V. The analog voltage inputs from the VTs should be connected to X11:22-30, and X51:22-30, according to the terminal diagrams, see Chapter 10 "Terminal diagrams".

17 Analog input current

Rated AC current input for the analog input module is 1 or 5 A. The choice is made by selecting the appropriate screw connection, on the analog input module. Each input channel corresponds to 3 screw connections – one common, one for rated current equal to 1A, and one for rated current equal to 5A. The appropriate rated current has also to be made as a setting of the parameter CTRatedInt_x in the function block calib3I. The analog current inputs from the CTs should be connected to X11:1-18, and X51:1-18, according to the terminal diagrams, see Chapter 10 "Terminal diagrams".

18 Synchrophasor output data format - IEEE Std 1344-1995 and IEEE PC37.118

RES 521 is equipped with two versions of synchrophasor streaming data protocol for data output, and they can be used simultaneously. Both protocols are implemented on TCP/IP Sockets. For details concerning the IEEE Std 1344-1995 see, Standard for Synchrophasors for Power Systems, IEEE Std 1344-1995, December 1995.

19 Environmental requirements

The water and dust protection level is: IP40 for the front, IP30 for the sides and IP20 for the back. For flush mounting, sealing strips to achieve IP54, can be ordered. The storage temperature for the terminal should be within –40ºC to +70ºC.

Chapter 4 Installation

This chapter contains instructions for installation of RES 521*1.0.

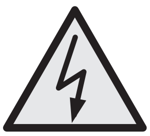
20 Introduction

The mechanical and electrical environmental conditions at the installation site must be within permissible range according to the technical data of the terminal. Dusty, damp places, places liable to rapid temperature variations, powerful vibrations and shocks, surge voltages of high amplitude and fast rise time, strong induced magnetic fields or similar extreme conditions should be avoided.

Sufficient space must be available in front of and at rear of the terminal to allow access for maintenance and future modifications. Flush mounted units should be mounted so that unit modules can be added and replaced without excessive demounting. The ring-lug option does not fully comply with EN 50178

Warning!

Do not touch circuitry during operation.
Hazardous voltages and currents are present.



Warning!

Do not disconnect a secondary connection of current transformer circuit without short-circuiting the transformer's secondary winding.

21 Preparations

21.1 Receiving, unpacking and checking

1. **Remove the transport casing.**
2. **Visually inspect the terminal.**

   Check that all items are included in accordance with the delivery documents. Check for transport damages.

In case of transport damage appropriate action must be taken against the latest carrier and the nearest ABB office or representative should be informed. ABB should be notified immediately if there are any discrepancies in relation to the delivery documents.

21.2 Storage

Store the terminal in the original transport casing in a dry and dust free place. Observe the environmental requirements stated in the technical data.

22 Mechanical installation

Suitable mounting kits for 19" rack mounting, flush mounting, and wall mounting can be ordered. The mounting kits contain all parts needed for the mounting, including screws and assembly instructions.

22.1 19" rack installation

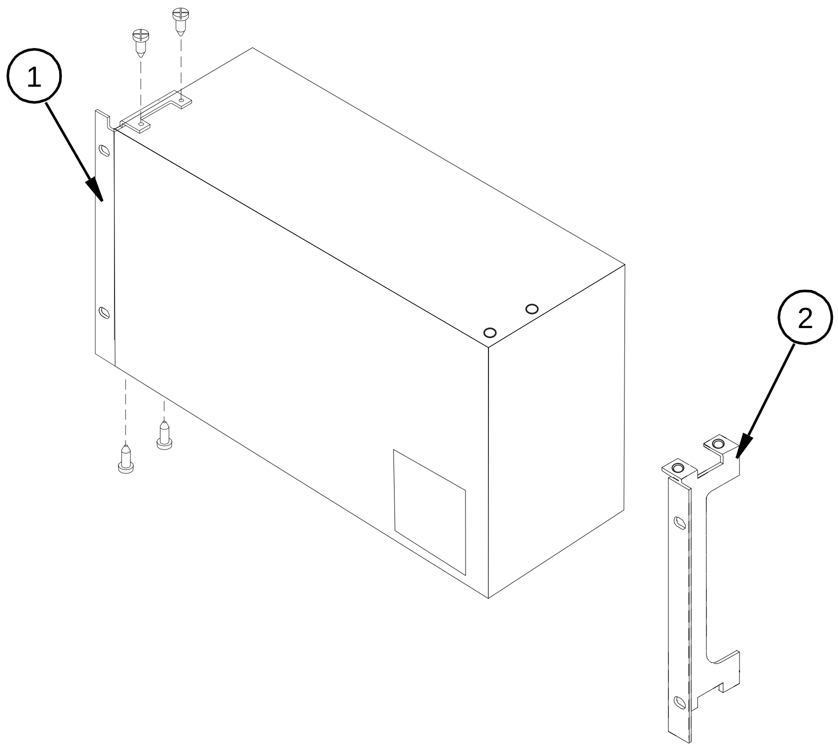


Figure 4: Terminal mounted in 19" rack.

The mounting kit consists of:

- Two mounting angles for 6U, 19" rack, with screws (TORX T20), pos (1) and (2).
- Assembly instructions.

22.2 Flush mounting

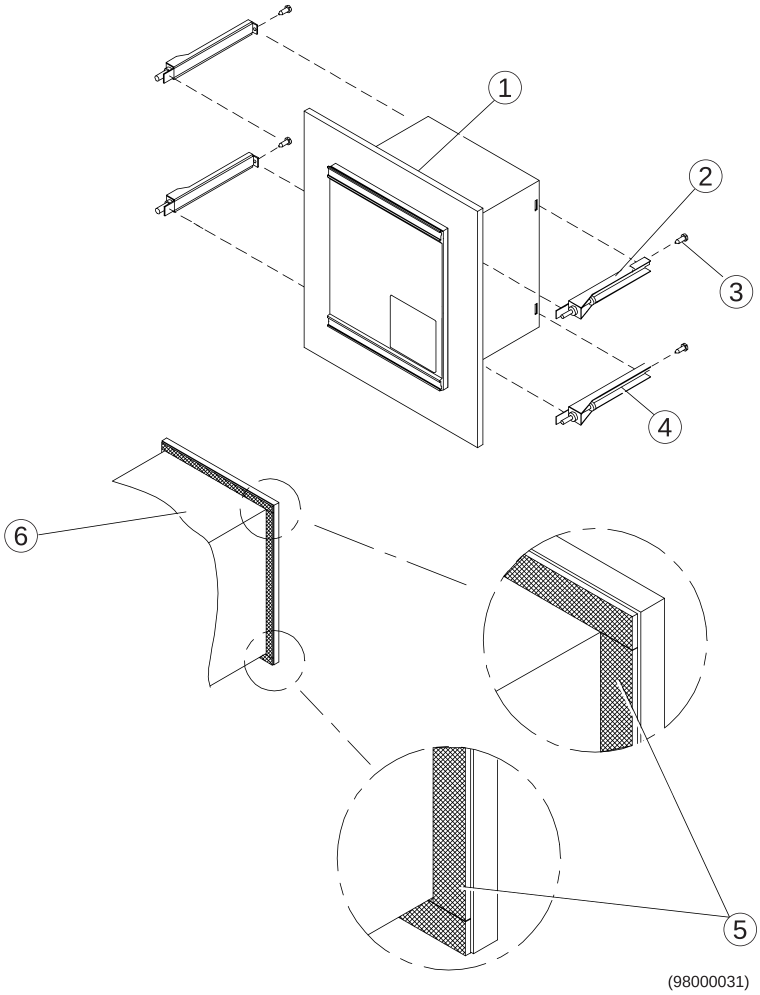


Figure 5: Flush mounting.

Mounting kit for flush mounting of all sizes of case 6U consists of:

- Four side holders and a sealing strip, pos (4) and (5).
- Four small (TORX T10), pos (3), and four big screws (TORX T25), not shown.
- Assembly instructions.

Also see “Case and cut-out dimensions” in Table 3 and Table 4.

22.2.1 Mounting procedure

1 Cut and affix the sealing strip if IP 54 is required.

2 Put the terminal in the cut-out.

3 Fasten the side holders to the back of the terminal with the small screws.

4 Fix the terminal with the big screws.

22.3 Wall mounting

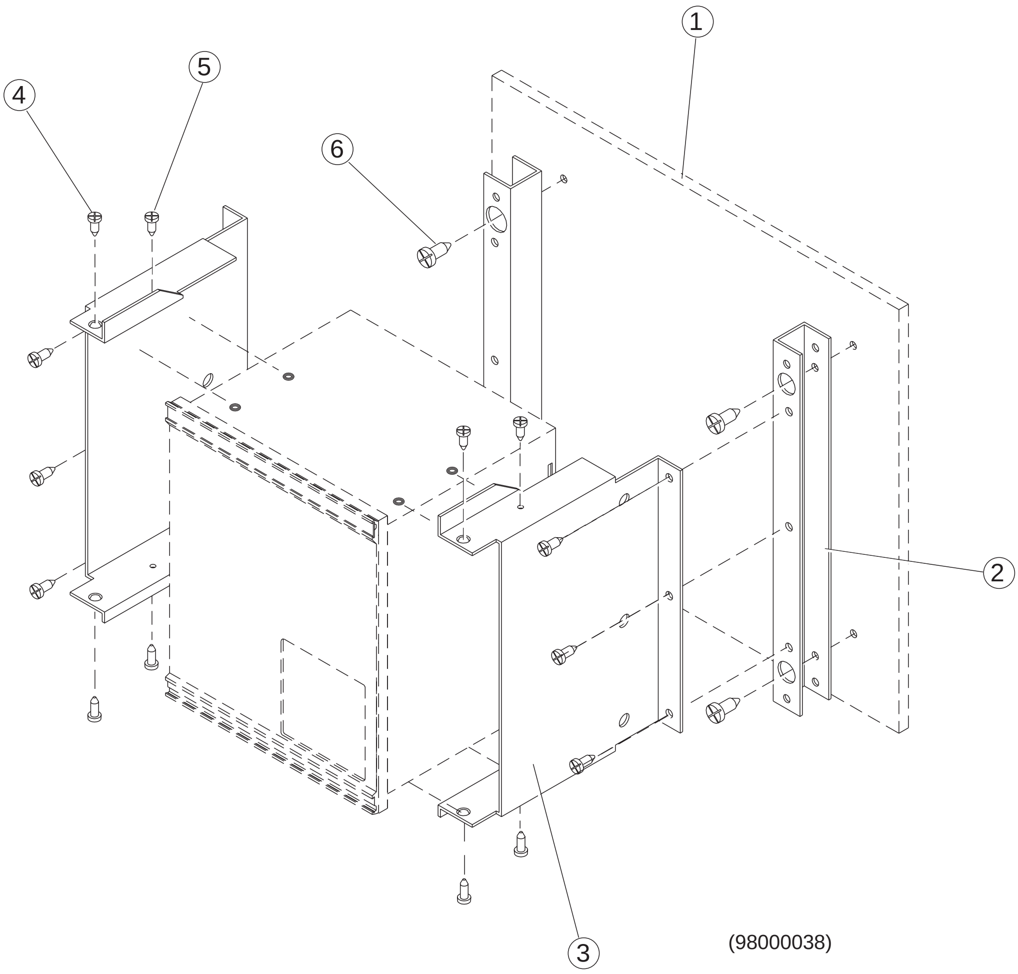


Figure 6: Wall mounting.

Mounting kit for wall mounting of all sizes of case 6U consists of:

- Two mounting angles (side plates), pos (3).
- Screws (grip size TORX T20, T25 and T30), pos (4), (5) and (6).
- Two mounting bars to be mounted on the wall, pos (2).
- Assembly instructions.

22.4 Case and cut-out dimensions

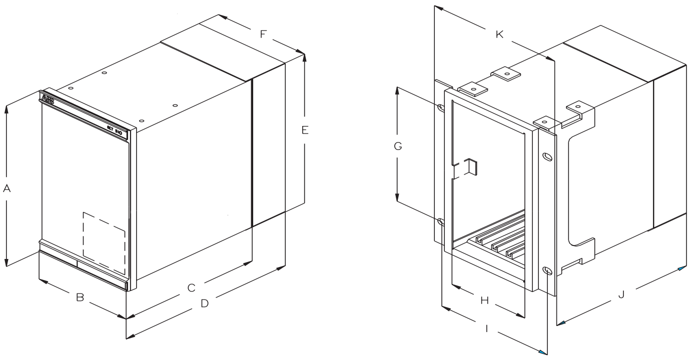


Table 3: Case dimensions (mm)

A	B	C	D	E	F	G	H	I	J	K
265.9	448.3	204.1	245.1	255.8	430.3	190.5	428.3	465.1	227.6	482.6

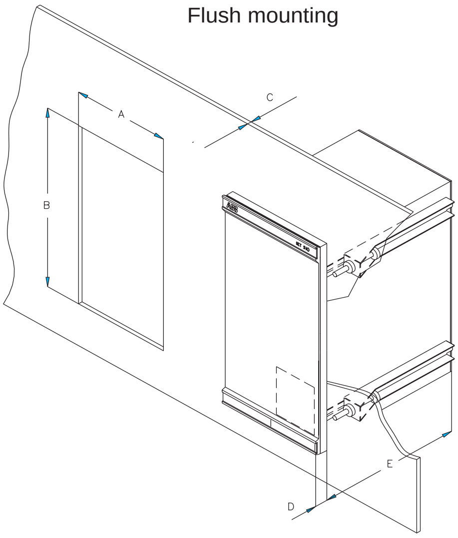


Table 4: Flush mounting cut-out dimensions (mm)

A	B	C	D	E	F	G
434.7	259.3	4-10	16.5	187.6/228.6[a]	106.5	97.6/138.6[a]

a) With protective cover

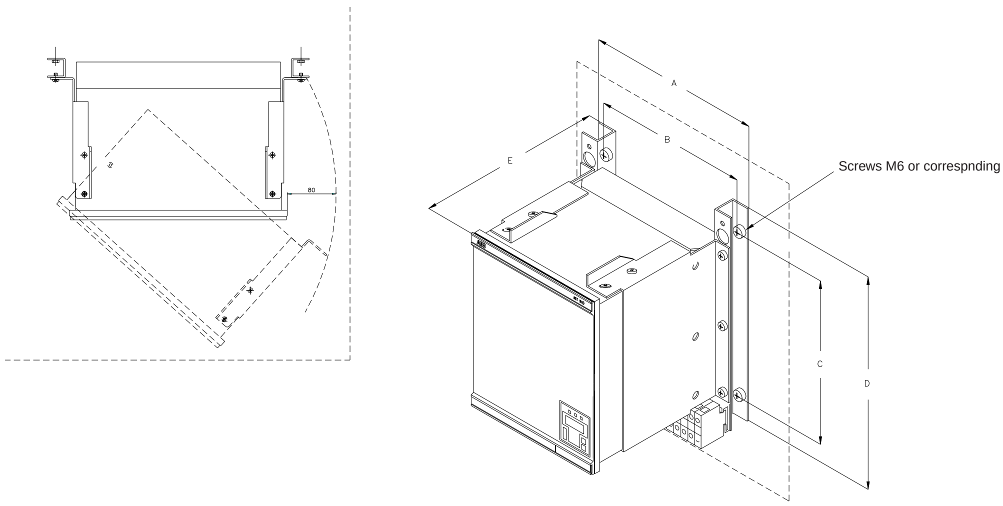


Table 5: Wall mounting (mm)

A	B	C	D	E
516	491.1	272.8	390	247

23 Electrical installation

Always make sure established guidelines for the type of terminal is followed during installation. When necessary use screened twisted-pair cables to minimize susceptibility. Otherwise use any kind of regular nonscreened tinned RK cable or equivalent.

When using screened cabling always use 360° full screen cable bushings to ensure screen coupling. Ensure that all signals of a single circuit are in the same single cable. Avoid mixing current and voltage measuring signals in the same cable.

23.1 Power and signal connectors

Power and signals are connected using COMBICON (Phoenix technology) plug-in screw connectors.

Connect signals to the COMBICON plug. Then plug the connector into the corresponding back-side mounted receptable. Lock the plug to the receptable by fastening the lock screws.

Use a solid or stranded conductor with a cross section area between 0.2-2.5 mm^2 (AWG24-12). Use a ferrule with plastic collar to connect two conductors, cross section area between 0.5-1.5 mm^2 (AWG20-18).

For the ring-lug option the outer diameter of the connector should not exceed 8 mm and the centre hole diameter should be 4 mm. For direct wire connection the wire size should be: # 12-22 AWG cU (corresponding to 0.33-3.3 mm^2).

23.1.1 DC-power supply connection

The auxiliary DC-supply level must be within 24-60V or 90-250V depending on ordered module. The DC-supply shall be connected to X141:4 (+) and X141:5 (-).

23.1.2 Analog input voltage connection

The analog three-phase voltage for phasor number 1 should be connected as listed below. If both metering and protection cores are available on the voltage transformer secondaries, it is recommended to use the protection core to cover a larger voltage variations during disturbances.

X11:22: UL1-phase

X11:24: UL1-earth

X11:25: UL2-phase

X11:27: UL2-earth

X11:28: UL3-phase

X11:30: UL3-earth

The analog three-phase voltage for phasor number 2 should be connected as listed below. If both metering and protection cores are available on the current transformer secondaries, it is recommended to use the protection core to cover a larger current variations during disturbances.

X51:22: UL1-phase

X51:24: UL1-earth

X51:25: UL2-phase

X51:27: UL2-earth

X51:28: UL3-phase

X51:30: UL3-earth

23.1.3 Analog input current connection

The analog three-phase currents for phasor number 3 should be connected as follows:

X11:1: IL1-1A, or X11:2: IL1-5A

X11:3: IL1-CT-neutral

X11:4: IL2-1A, or X11:5: IL2-5A

X11:6: IL2-CT-neutral

X11:7: IL3-1A, or X11:8: IL3-5A

X11:9: IL3-CT-neutral

The analog three-phase currents for phasor number 4 should be connected as follows:

X11:10: IL1-1A, or X11:11: IL1-5A

X11:12: IL1-CT-neutral

X11:13: IL2-1A, or X11:14: IL2-5A

X11:15: IL2-CT-neutral

X11:16: IL3-1A, or X11:17: IL3-5A

X11:18: IL3-CT-neutral

The analog three-phase currents for phasor number 5 should be connected as follows:

X51:1: IL1-1A, or X51:2: IL1-5A

X51:3: IL1-CT-neutral

X51:4: IL2-1A, or X51:5: IL2-5A

X51:6: IL2-CT-neutral

X51:7: IL3-1A, or X51:8: IL3-5A

X51:9: IL3-CT-neutral

The analog three-phase currents for phasor number 6 should be connected as follows:

X51:10: IL1-1A, or X51:11: IL1-5A

X51:12: IL1-CT-neutral

X51:13: IL2-1A, or X51:14: IL2-5A

X51:15: IL2-CT-neutral

X51:16: IL3-1A, or X51:17: IL3-5A

X51:18: IL3-CT-neutral

23.1.4 Binary input connection

The rated voltage level for the binary inputs has been chosen in the ordering phase to either 24/30 Vdc, 48/60 Vdc, 110/125 Vdc or 220/250 Vdc. The binary inputs should be connected according to the following:

X91:1,2: Binary Input Channel 1

X91:3,4: Binary Input Channel 2

X91:5,6: Binary Input Channel 3

X91:7,8: Binary Input Channel 4

X91:9,10: Binary Input Channel 5

X91:11,12: Binary Input Channel 6

X91:13,14: Binary Input Channel 7

X91:15,16: Binary Input Channel 8

23.1.5 Binary output connection

The binary outputs provide information according to the following:

X92:1,2:	Binary Output Channel 1: GPS synch lost
X92:1,3:	Binary Output Channel 2: Data out
X92:1,4:	Binary Output Channel 3: freqHigh
X92:1,5:	Binary Output Channel 4: freqLow
X92:1,6:	Binary Output Channel 5: dFreqHigh
X92:7,8,9:	Binary Output Channel 6: dLowHigh
X92:10,11:	Binary Output Channel 7: underVolt1
X92:10,12:	Binary Output Channel 8: underVolt2
X92:10,13:	Binary Output Channel 9: overCurr1
X92:10,14:	Binary Output Channel 10: overCurr2
X92:15,16:	Binary Output Channel 11: overCurr3
X92:17,18:	Binary Output Channel 12: overCurr4

23.2 Protective grounding

Connect the unit to the ground bar of the cubicle with a short green/yellow conductor, cross section at least 1.5 mm^2 (AWG18), connected to the ground connector at the back of the unit.

23.3 Screen connection

When using screened cables always make sure screens are grounded and connected according to applicable engineering methods. This may include checking for appropriate grounding points near the terminal, for instance, in the cubicle and/or near the source of measuring. Ensure that ground connections are done with short (max. 10 cm) conductors of an adequate cross section, at least 1.5 mm^2 (AWG18) for single screen connections.

23.4 Galvanic Ethernet connection

The galvanic Ethernet should be connected to the RJ-45 connector on the back of the terminal.

24 Optical installation

Fiber optical cables are sensitive to handling. Do not bend too sharply. The minimum curvature radius is 15 cm for plastic fibers and 25 cm for glass fibers. If cable straps are used, apply with loose fit.

When the optic Ethernet module is used, the protection plate for the galvanic connection must not be removed.

Always hold the connector, ***never*** *the cable, when connecting or disconnecting. Do not twist, pull or bend the optical fiber.*

25 Antenna installation

In order to receive GPS signals from the satellites orbiting the earth a GPS antenna must be used.

25.1 Mechanical installation

The antenna is mounted on a console for mounting on a horizontal or vertical flat surface or on an antenna mast.

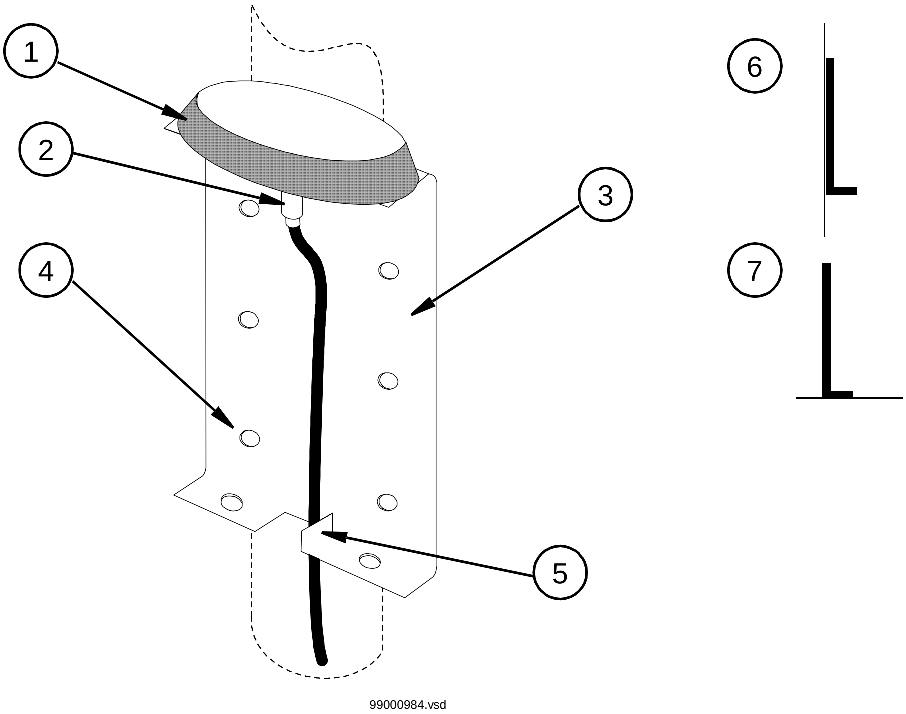


Figure 7: Antenna console mounted on mast.

Table 6: Antenna console

1	GPS antenna
2	TNC connector
3	Console, 78x150 mm
4	Mounting holes 5.5 mm
5	Tab for securing of antenna cable
6	Vertical mounting position
7	Horizontal mounting position

Mount the antenna and console clear of flat surfaces such as buildings walls, roofs and windows to avoid signal reflections. If necessary, protect the antenna from animals and birds which can affect signal strength. Also protect the antenna against lightning.

Always position the antenna and its console so that a continuous clear line-of-sight visibility to all directions is obtained, preferably more than 75%. A minimum of 50% clear line-of-sight visibility is required for un-interrupted operation.

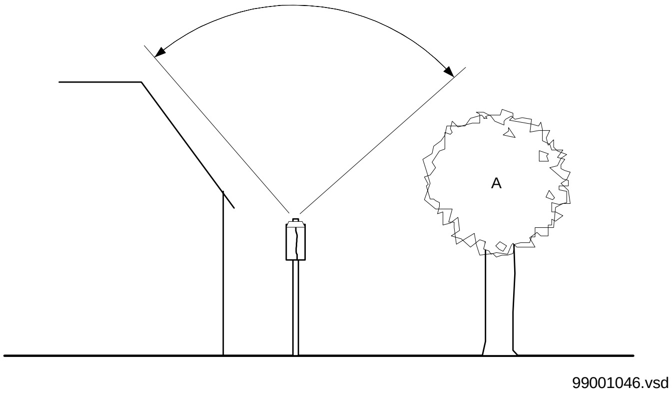


Figure 8: Antenna line-of-sight.

25.2 Electrical installation

Use a 50 ohm coaxial cable with a male TNC connector in the antenna end and a male SMA connector in the receiver end to connect the antenna to RES 521. Choose cable type and length so that the total attenuation is max. 26 dB at 1.6 GHz. A suitable antenna cable is supplied with the antenna.

The antenna has a female TNC connector to the antenna cable.

Make sure that the antenna cable is not changed when connected to the antenna or to the receiver. Short-circuit the end of the antenna cable with some metal device, when first connected to the antenna. When the antenna is connected to the cable, connect the cable to the receiver. RES 521 must be switched off when the antenna cable is connected.

26 Terminal connectors

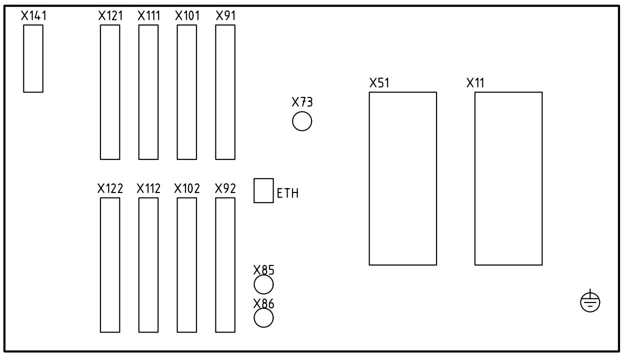


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Figure 9: Terminal connectors.

Table 7: Terminal connectors

Connector	Usage
X73	Antenna connection
X85, X86	Optical Ethernet connection
ETH	Galvanic Ethernet connection
X141	Power supply connector
X11, X51	Analog input module
X91	Binary input connector
X92	Binary output connector
X101 - X122	Not used

Table 8: Power supply connection

Connection	Usage
X141:1	Internal fail / loss of auxiliary voltage (normally open)
X141:2	Auxiliary alarm voltage supply (+)
X141:3	Internal fail / loss of auxiliary voltage (normally closed)
X141:4	Auxiliary DC voltage supply (+)
X141:5	Auxiliary DC voltage supply (-)

Table 9: Analog Input Module connections

Connector		Usage
AIM 1	**AIM 2**	
X11:1,2,3	X51:1,2,3	CT, phase L1, for Phasor no. 3/5
X11:4,5,6	X51:4,5,6	CT, phase L2, for Phasor no. 3/5
X11:7,8,9	X51:7,8,9	CT, phase L3, for Phasor no. 3/5
X11:10,11,12	X51:10,11,12	CT, phase L1, for Phasor no. 4/6
X11:13,14,15	X51:13,14,15	CT, phase L2, for Phasor no. 4/6
X11:16,17,18	X51:16,17,18	CT, phase L3, for Phasor no. 4/6
X11:19,20,21	X51:19,20,21	Not used
X11:22,24	X51:22,24	VT, phase L1, for Phasor no. 1/2
X11:25,27	X51:25,27	VT, phase L2, for Phasor no. 1/2
X11:28,30	X51:28,30	VT, phase L3, for Phasor no. 1/2

Table 10: Binary Input connector

Connector	Usage
X91:1,2	Binary input no. 1
X91:3,4	Binary input no. 2
X91:5,6	Binary input no. 3
X91:7,8	Binary input no. 4
X91:9,10	Binary input no. 5
X91:11,12	Binary input no. 6
X91:13,14	Binary input no. 7
X91:15,16	Binary input no. 8

Table 11: Binary Output connector

Connector	Usage	Comment
X92:1,2	Binary output no. 1	GPS synch lost
X92:1,3	Binary output no. 2	Data invalid
X92:1,4	Binary output no. 3	freqHigh
X92:1,5	Binary output no. 4	freqLow
X92:1,6	Binary output no. 5	dFreqHigh
X92:7,8,9	Binary output no. 6	dFreqLow
X92:10,11	Binary output no. 7	underVolt1
X92:10,12	Binary output no. 8	underVolt2
X92:10,13	Binary output no. 9	overCurr1
X92:10,14	Binary output no. 10	overCurr2
X92:15,16	Binary output no. 11 (reed contacts)	overCurr3
X92:17,18	Binary output no. 12 (reed contacts)	overCurr4

Binary output no. 1, GPS, is activated if the GPS synchronization fails, and the time accuracy of 1 microsecond is lost. The most probable reason to get this alarm is that the antenna has been shaded, and the number of observed satellites has been to few. This is the same binary signal as sent in the IEEE synchrophasor format, called "synchronization status".

Binary output no. 2, Data Out, is activated if at least one communication connection is established and active. The communication connection can be either of IEEE1344 or PC37.118 type.

Binary output no. 3, freqHigh, is activated if the frequency exceeds the setting of parameter TRIGGFREQ_1/limitOver (see section 36 and 43.7) for a time longer than the setting of parameter TRIGGFREQ_1/tDelayOver.

Binary output no. 4, freqLow, is activated if the frequency is below the setting of parameter TRIGGFREQ_1/limitUnder (see section 36 and 43.7) for a time longer than the setting of parameter TRIGGFREQ_1/tDelayUnder.

Binary output no. 5, dFreqHigh, is activated if the rate of change of frequency exceeds the setting of parameter TRIGGFREQ_2/limitOver (see section 36 and 43.7) for a time longer than the setting of parameter TRIGGFREQ_2/tDelayOver.

Binary output no. 6, dFreqLow, is activated if the frequency is below the setting of parameter TRIGGFREQ_2/limitUnder (see section 36 and 43.7) for a time longer than the setting of parameter TRIGGFREQ_2/tDelayUnder.

Binary output no. 7, underVolt1, is activated if the voltage magnitude of phasor 1 is below the setting of parameter TRIGGUV2CH_1/limitCh1 for a longer time than the setting of parameter TRIGGUV2CH_1/tDelayCh1.

Binary output no. 8, underVolt2, is activated if the voltage magnitude of phasor 2 is below the setting of parameter TRIGGUV2CH_1/limitCh2 for a longer time than the setting of parameter TRIGGUV2CH_1/tDelayCh2.

Binary output no. 9, overCurr1, is activated if the current magnitude of phasor 3 exceeds the setting of parameter TRIGGOC4CH_1/limitCh1 for a longer time than the setting of parameter TRIGGOC4CH_1/tDelayCh1.

Binary output no. 10, overCurr2, is activated if the current magnitude of phasor 4 exceeds the setting of parameter TRIGGOC4CH_1/limitCh2 for a longer time than the setting of parameter TRIGGOC4CH_1/tDelayCh2.

Binary output no. 11, overCurr3, is activated if the current magnitude of phasor 5 exceeds the setting of parameter TRIGGOC4CH_1/limitCh3 for a longer time than the setting of parameter TRIGGOC4CH_1/tDelayCh3.

Binary output no. 12, overCurr4, is activated if the current magnitude of phasor 6 exceeds the setting of parameter TRIGGOC4CH_1/limitCh4 for a longer time than the setting of parameter TRIGGOC4CH_1/tDelayCh4.

Chapter 5 Commissioning

This chapter contains instructions for performing commissioning.

27 General

Since commissioning in some cases cannot be performed on a single terminal due to the introduction of remote I/O, commissioning has to be planned and methods must be applied specifically for each single project with a system level approach. In this manual only the goals of a single terminal commissioning is stated, speaking less of the methods for performing a system wide commissioning.

Warning!
Do not touch circuitry during operation.
Hazardous voltages and currents are present.

Warning!
Do not disconnect a secondary connection of current transformer circuit without short-circuiting the transformer's secondary winding.

28 Decommissioning

28.1 Transporting and storing

Store and transport the product in the original transport casing in a dry and dust free place. Observe the environmental requirements for storage stated in the technical data.

28.2 Disposal

Dispose the product according to the current environmental regulations regarding recycling and disposal of electronic materials.

29 Product specific commissioning

29.1 Overview

Perform the commissioning tests to:

- Verify that all functions are operating as expected.
- Verify the installation.

Always document the commissioning for future reference.

29.2 Preparations

Check that all necessary test equipment, documentation and software are available. This includes:

- Valid wiring diagrams.
- Setting lists.

29.3 Checking the external connections

29.3.1 Power supply check

Check that the supplied voltage is in accordance with the RES 521 technical data and that the voltage has the correct polarity.

29.3.2 Connection check

Check that the wiring is in strict accordance with the supplied wiring diagram. Do not continue further until any errors are corrected. Check:

- that the antenna has been properly connected.

29.4 Energizing tests

Follow the following instructions:

1. **Energize the terminal**

   Wait at least 30 minutes before proceeding.
   When using the terminal for the first time, or if the terminal has not been used for several months, acquiring satellite data will take several minutes. Moving the antenna to a new position could also affect the start-up time.

2. **Check the LED indications**

   The green LED should be steady lit, no other indications should be present.

30 Quick start

This section gives the RES 521 user the very minimum of instructions and settings, necessary to start and check the terminal.

30.1 Installation

Connect the GPS antenna to connector X73 and the auxiliary DC power to X141 (+ to pin 4 and 0V to pin 5). See figure 9 on page 27 and “Terminal diagrams” on page 123. Make sure that the antenna is protected from lightning.

30.2 Start-up

Switch on the power.

Watch the HMI displaying first nothing then “TERMINAL STARTUP” and after a while the entrance to the whole HMI. Push E to enter. Using the arrows, ‘E’ to enter a menu, and ‘C’ to “back-up” one level. Find your way to STATUS->GPS status->satellites to see how many satellites the GPS antenna have contact with. If the number of satellites is low or zero the time is not accurate and you have to re-arrange your GPS-antenna position. Make sure that the new antenna position is protected from lightning.

Use ‘C’ to get back to the top level. Then find your way to Settings->Time->TIME_UTC to see the accurate time according to the GPS. For details concerning the HMI, see Chapter 6.

30.3 Configuration and settings

RES 521*1.0 is delivered with a fix configuration. Most settings are pre-set to default values. A few settings must be changed before use, e.g. the communication settings, such as the IP-address. See Table 12 for the most important settings.

Table 12: Important settings

Scope	Path from Settings menu in HMI	Default	Description
System	Communication->IP_Addr	10.1.150.3	RES 521 IP-address
System	Communication->IP_Mask	255.255.255.0	Subnet mask
System	Communication->GateWay_IP	10.1.150.1	Gateway IP-address
System	Communication->IEEE1344_Port	4711	IEEE1344 Socket port
System	Communication->PC37.118_Port	4712	PC37.118 Socket port
System	Communication->PMU_Id1	0	Hi 32bit part of PMU ID

Table 12: Important settings

System	Communication->PMU_Id2	0	Lo 32bit part of PMU ID
System	Communication->1344_TransfRate	1 every cycle	Data transfer rate
System	PMUapp->PmuOut_1->Angle_Ref	Time	Phasor readings ref
System	PMUapp->TIMEREF_1->freqRated	50	Nominal frequency
Phasor1	PMUapp->PHASOR3U_1->VTRatioExt	1	VT scaling U1, X11:22-30
Phasor2	PMUapp->PHASOR3U_2->VTRatioExt	1	VT scaling U2, X51:22-30
Phasor3	PMUapp->PHASOR3I_1->CTRatioExt	1	CT scaling I1, X11:1-9
Phasor3	PMUapp->PHASOR3I_1->CTRatedInt	1	CT input I1, X11:1-9
Phasor4	PMUapp->PHASOR3I_2->CTRatioExt	1	CT scaling I2, X11:10-18
Phasor4	PMUapp->PHASOR3I_2->CTRatedInt	1	CT input I2, X11:10-18
Phasor5	PMUapp->PHASOR3I_3->CTRatioExt	1	CT scaling I3, X51:1-9
Phasor5	PMUapp->PHASOR3I_3->CTRatedInt	1	CT input I3, X51:1-9
Phasor6	PMUapp->PHASOR3I_4->CTRatioExt	1	CT scaling I4, X51:10-18
Phasor6	PMUapp->PHASOR3I_4->CTRatedInt	1	CT input I4, X51:10-18

Setting examples in the CALIB3-menu

- Ex: VTRatioExt, 132000/110 = 1200
- Ex: CTRatioExt, 3000/5 = 600
- Ex: CTRatio Int, 5A input -> 5

30.3.1 Communication settings

Go to Settings->Communication->IP_Addr, IP_Mask, GateWay_IP and make sure that they all correspond to your communication network properties.

If you change any value, you will see a different dialogue on the HMI while going back to the top level, this dialogue asks you if you want to save the new value. Answer “Yes”, “No” or “Cancel”. Note: This setting will not take effect until next reboot.

30.3.2 CT/VT rating

Example: Set VT-Ratio for phase U_L1, U_L2 and U_L3 in Phasor1:

Go to Settings->PMUapp->PHASOR3U_1->VTRatioExt, press ”E” for edit mode and use the arrows to alter the VT-ratio. Press “E” again to leave the edit mode. After altering the settings, press “C” twice to back out of this setting branch and answer “yes” in the save dialogue.

RES 521 must be restarted for this setting to take effect. There is a restart entry in the settings menu, Settings->Restart, set reboot Terminal to “Yes” and save the setting.

The currents can be connected either to the 1A input or to the 5A input. The setting CTRatedInt must be set to reflect the input choice, so that 1A => 1.00000 and 5A=> 5.00000. Note that the Setting CTRatedExt should be set to the ratio of the CT, e.g. if the CT is of type 3000A to 5A, the CTRatedExt should be set to 600.

30.4 Functional tests with applied signals

30.4.1 Connect secondary voltages and currents

Time to hook up your terminal with some incoming currents and voltages. Use a three-phase signal generator, e.g. a relay test system. Connect incoming currents and voltages according to table 13, “Connections of X11” on page 36 and table 14, “Connections of X51” on page 37

Table 13: Connections of X11

Plint number	Analog input connector
X11:1	Phasor3 I_L1, 1A-input
X11:2	Phasor3 I_L1, 5A-input
X11:3	Phasor3 I_L1, neutral (return)
X11:4	Phasor3 I_L2, 1A-input
X11:5	Phasor3 I_L2, 5A-input
X11:6	Phasor3 I_L2, neutral (return)
X11:7	Phasor3 I_L3, 1A-input
X11:8	Phasor3 I_L3, 5A-input
X11:9	Phasor3 I_L3, neutral (return)
X11:10	Phasor4 I_L1, 1A-input
X11:11	Phasor4 I_L1, 5A-input
X11:12	Phasor4 I_L1, neutral (return)
X11:13	Phasor4 I_L2, 1A-input
X11:14	Phasor4 I_L2, 5A-input
X11:15	Phasor4 I_L2, neutral (return)
X11:16	Phasor4 I_L3, 1A-input
X11:17	Phasor4 I_L3, 5A-input

Table 13: Connections of X11

X11:18	Phasor4 I_L3, neutral (return)
X11:19	Not connected
X11:20	Not connected
X11:21	Not connected
X11:22	Phasor1 U_L1
X11:23	Not connected
X11:24	Phasor1 U_L1, neutral
X11:25	Phasor1 U_L2
X11:26	Not connected
X11:27	Phasor1 U_L2, neutral
X11:28	Phasor1 U_L3
X11:29	Not connected
X11:30	Phasor1 U_L3, neutral

Table 14: Connections of X51

Plint number	Analog input connector
X51:1	Phasor5 I_L1, 1A-input
X51:2	Phasor5 I_L1, 5A-input
X51:3	Phasor5 I_L1, neutral (return)
X51:4	Phasor5 I_L2, 1A-input
X51:5	Phasor5 I_L2, 5A-input
X51:6	Phasor5 I_L2, neutral (return)
X51:7	Phasor5 I_L3, 1A-input
X51:8	Phasor5 I_L3, 5A-input
X51:9	Phasor5 I_L3, neutral (return)
X51:10	Phasor6 I_L1, 1A-input
X51:11	Phasor6 I_L1, 5A-input
X51:12	Phasor6 I_L1, neutral (return)
X51:13	Phasor6 I_L2, 1A-input

Table 14: Connections of X51

X51:14	Phasor6 I_L2, 5A-input
X51:15	Phasor6 I_L2, neutral (return)
X51:16	Phasor6 I_L3, 1A-input
X51:17	Phasor6 I_L3, 5A-input
X51:18	Phasor6 I_L3, neutral (return)
X51:19	Not connected
X51:20	Not connected
X51:21	Not connected
X51:22	Phasor2 U_L1
X51:23	Not connected
X51:24	Phasor2 U_L1, neutral
X51:25	Phasor2 U_L2
X51:26	Not connected
X51:27	Phasor2 U_L2, neutral
X51:28	Phasor2 U_L3
X51:29	Not connected
X51:30	Phasor2 U_L3, neutral

30.4.2 Verify results using the HMI

Use the HMI to check if the currents and voltages seem to be reasonable. Push ‘E’ to make the HMI come alive. Navigate to ServiceReport->PMUapp->PmuOut_1->amplitude03 and make sure that it reads the same thing as the current put into the terminal on connection X11:1-X11:9. Also look at the other readings and make sure that they are correct. Observe that the value shown on the HMI is the phase-neutral voltage, not the phase-phase voltage. See table 15 on page 39 to know which amplitude channel reads which incoming connection.

Table 15: HMI ServiceReport

Scope	Path from ServiceReport menu in HMI	Connections
Phasor1	PMUapp->PmuOut_1->Amplitude01 PMUapp->PmuOut_1->PhaseAngle01	X11:22 – X11:30
Phasor2	PMUapp->PmuOut_1->Amplitude02 PMUapp->PmuOut_1-> PhaseAngle 02	X51:22 – X51:30
Phasor3	PMUapp->PmuOut_1->amplitude03 PMUapp->PmuOut_1-> PhaseAngle 03	X11:1 – X11:9
Phasor4	PMUapp->PmuOut_1->Amplitude04 PMUapp->PmuOut_1-> PhaseAngle 04	X11:10 – X11:18
Phasor5	PMUapp->PmuOut_1->Amplitude05 PMUapp->PmuOut_1-> PhaseAngle 05	X51:1 – X51:9
Phasor6	PMUapp->PmuOut_1->Amplitude06 PMUapp->PmuOut_1-> PhaseAngle 06	X51:10 – X51:18

30.4.3 Testing the trigger functions

Each phasor has its own overcurrent or undervoltage trigger (overcurrent for the four current phasors, and undervoltage for the two voltage phasors). To find the triggers, navigate to Settings->PMUapp-> and you will find triggers named “TRIGGFREQ_1, TRIGGDFREQ_1, TRIGGOC4CH_1, TRIGGUV2CH_1”. To see which trigger that operates on each phase use Table 16. The logical configuration of the triggers is shown in chapter 11, “RES 521 standard configuration” on page 128 and page 129.

For example, when dropping the incoming voltage on X11:22 – X11:30 below a specified value, one should hear a clear click when BO:7 goes high. This is also noticeable when looking at the HMI in ServiceReport->PMUapp->PmuBO_1->ch07. The incoming voltage could be low for different reasons, one is that the actual voltage of each phase is too low, others might be wrong order of phases or the angle between phases is disturbed. Correct the cause of the low incoming voltage and hear a clear click from the BO:07 when it resets. You specify at which voltage level you want the undervoltage to trip in the HMI at Settings->PMUapp->TRIGGUV2CH_1->limitCh1. The undervoltage resets at the specified level+hystAbs or specified level+hystRel all found under Settings->PMUapp->TRIGGUV2CH_1.

Much using the same method as for the undervoltage, overcurrent could be tested. Changing the incoming currents, reading the new value on the HMI under ServiceReport->PMUapp->PmuOut_1->amplitude03, hear a clear click and see the value of the overcurrent pin at ServiceReport->PMUapp->PmuBO_1->overCurr1 when incoming current exceeds the limit specified at settings->PMUapp->TRIGGOC4CH.

Table 16: Trigger settings

Trigger	Phasor	Path from Settings menu in HMI	ServiceReport	Relay output X92:1 = common
Freq (over)	Phasor1	PMUapp->TRIGGFREQ_1	PMUapp-PmuBO->freqHigh	X92:1, X92:4
Freq (under)	Phasor1	PMUapp->TRIGGFREQ_1	PMUapp-PmuBO->freqLow	X92:1, X92:5
df/dt (High)	Phasor1	PMUapp->TRIGGDFREQ_1	PMUapp-PmuBO->dFreqHigh	X92:1, X92:6
df/dt (Low)	Phasor1	PMUapp->TRIGGDFREQ_1	PMUapp-PmuBO->dFreqLow	X92:7, X92:9
OverCurrent	Phasor3	PMUapp->TRIGGOC4CH_1	PMUapp-PmuBO->overCurr1	X92:10, X92:13
OverCurrent	Phasor4	PMUapp->TRIGGOC4CH_1	PMUapp-PmuBO->overCurr2	X92:10, X92:14
OverCurrent	Phasor5	PMUapp->TRIGGOC4CH_1	PMUapp-PmuBO->overCurr3	X92:15, X92:16
OverCurrent	Phasor6	PMUapp->TRIGGOC4CH_1	PMUapp-PmuBO->overCurr4	X92:17, X92:18
UnderVoltage	Phasor1	PMUapp->TRIGGUV2CH_1	PMUapp-PmuBO->underVolt1	X92:10, X92:11
UnderVoltage	Phasor2	PMUapp->TRIGGUV2CH_1	PMUapp-PmuBO->underVolt2	X92:10, X92:12

Chapter 6 Human machine interface

31 Introduction

The built-in human machine interface (HMI) provides local communication between the user and the terminal.

The HMI module consists of three light emitting diodes (LEDs), a liquid crystal display (LCD), six membrane pushbuttons, and one optical connector, for local PC communication (not used).

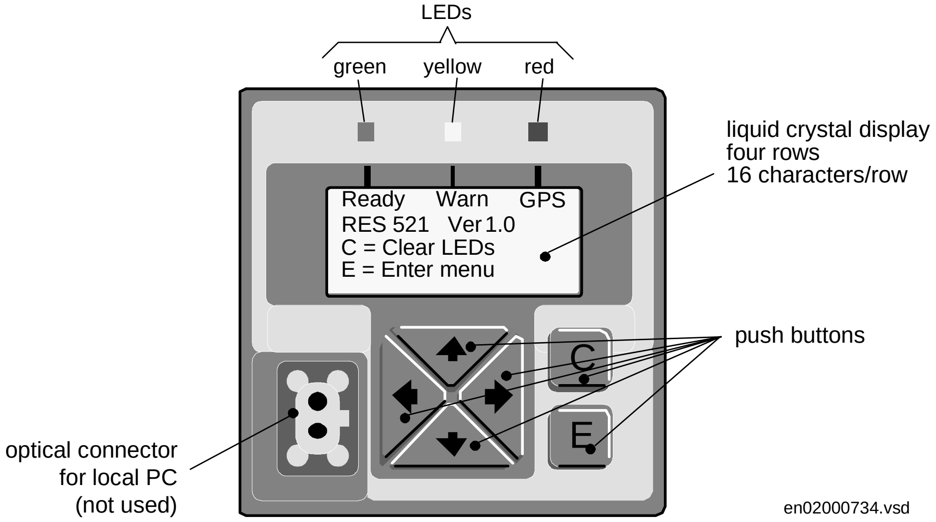


Figure 10: Built-in human-machine interface module.

31.1 LEDs

Three LEDs provide primary information on the status of the terminal. Each LED has a specific function, which also depends on whether it is off, steady on, or flashing.

Table 17: LED indications

LED	**Operation**		
	Off	**Lit**	**Flashing**
Green	Power off	Normal operation	Internal failure
Yellow	Normal operation	Not used	Recoverable error e.g. time sync error, terminal restoring services
Red	Normal operation	No GPS data received	GPS signal below acceptable quality

31.2 LCD display

The liquid crystal display (LCD) provides detailed information on the terminal. Normally, it is off. Select any button to turn on the LCD display. The first row on the LCD display shows the current status of all LEDs and the second row displays the type of terminal with its version.

The display shuts down after you exit the menu tree or if no button is selected for more than about 5 minutes (setting, default 5 minutes).

31.3 Pushbuttons

The number of buttons used on the HMI module is reduced to the minimum acceptable amount to make the communication as simple as possible for the user. The buttons normally have more than one function, depending on where they are used in the dialog.

All buttons have one function in common: when the display is in idle (dark, non active) mode, selecting any of them results in activation of the display.

The C button has two main functions, it:

- Cancels the operation, when used together with the dialog windows.
- Provides an Exit operation in a menu tree. This means that each selection of the C button within the menu tree results in stopping the current function or leaving the menu branch and moving one step higher in the menu tree.

The E button mainly provides an Enter function. It activates, for example, the selected menu tree branch, confirm settings, and different actions.

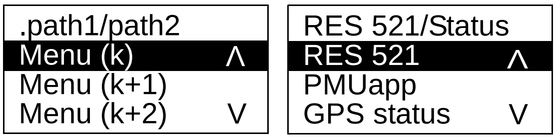
The left and right arrow buttons have two functions, to:

- Position the cursor in a horizontal direction, for instance, to move between the digits in a number during the setting procedures for real values.
- Move between the data windows within the same menu branch.

The up and down arrow buttons have three functions, to:

- Move among different menus within the menu and the dialog windows.
- Scroll the menu tree when it contains more branches than shown on the display.
- Change the parameter values in the data windows during the setting procedure.

32 Menu window



a) b)

Figure 11: Menu window, general configuration (a) and typical example (b).

For row one:

- A dot always appears at the beginning of the row when the selected menu window does not represent the main menu.
- path1 displays the name of the superior menu.
- path2 displays the name of the active menu window.

For rows two, three, and four:

- Menus k, k + 1 and k + 2 appear in the three bottom rows.
- When the cursor highlights one of the rows, it indicates the path that you can activate by selecting the E button.

The up arrow appears in row 2 when more menus are available before the k menu. The down arrow appears in the bottom row when more menus are available after the k+2 menu. To change the active path within the menu tree (scrolling the menu) select the up or down arrow button.

To change the menu window into a new menu window or into a data window select the E button. In same case the paths in the first row change in such a way that the old path2 now becomes a path1 and the previous menu line with the cursor then changes into path2.

32.1 Starting the dialogue

Figure 12: "Start dialogue window." on page 45 shows the dialog window to start communication with the terminal. Select the:

- C button to clear the display, or
- E button to enter the menu tree

The text (Ready, Warn, GPS) in row one of the window in Figure 12: "Start dialogue window." on page 45 describes the function of the LEDs that are at the top of the display when it is active.

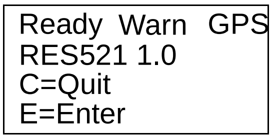


Figure 12: Start dialogue window.

33 Data window

33.1 View status and readings

Use the menu window and the pushbuttons to move to the desired menu branch. To move between the data windows with readings or data values within the same menu branch use the left and right arrows.

33.2 Change and save settings

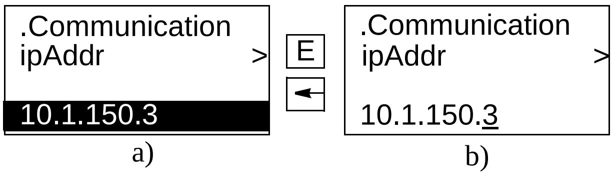


Figure 13: Change a setting.

After you have selected the E button, the data window changes from figure 13a to figure 13b. Select the left/right arrow to move to the digits you want to change. Select the up/down arrow to increase/decrease the actual digit. Use the up or down arrows in the same way if you are supposed to choose between different alternatives (on or off) as in figure 14.

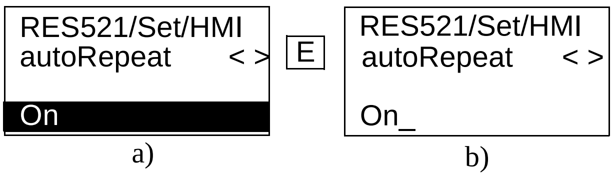


Figure 14: Change a setting.

Select the E button when the setting is changed. To save the changes select the C button and the window changes according to figure 15.

Use the right or left arrow to move to YES, NO or CANCEL. Then select E to confirm your selection. Select Yes to confirm that you want to save the changes. If you select CANCEL you return to the window that was shown on the display before the dialog window appeared. To make the changes active the terminal must be rebooted.

```
Save settings?
Group: 1
_______________
|Yes||No||Cancel||
```

Figure 15: Save settings.

34 HMI structure

This section describes the structure of the human machine interface (HMI).

The following conventions are used:

1 The table header displays the actual path of the information shown in the cells. The information in the header is displayed in a cell with a greyscale-fill.

Example:

RES521	RES521/Settings	.Set/PMUapp	.PMUapp/AI32_1

Is equal to:

RES 521
  Settings
    PMUapp
      AI32_1

2 The path to the end-nodes appear in **bold**.

3 Data nodes (parameters) appear in *italic*.

Example:

.TIMEREF_1
adaptiveOper
freqRated
freqLowLimit
freqHighLimit

4 Dialogues and references to other documents are located in thicker frames.

35 Display for Status menu

RES521	**RES 521/Status**	**.Sts/RES521**
Status	**RES521**	*Health*
Settings	**PMUapp**	*State*
ServiceReport	**GPS status**	*Load*
	Terminal info	

.Sts/PMUapp
Health
State
minExecTime
meanExecTime
maxExecTime

.Sts/GPS status
satellites
quality
utcOffset

.Terminal Info
serialNo
orderNo
prodDate

35.1 GPS status

- “satellites” is the number of GPS-satellites in range.
- “quality“ is the maximum time error in microseconds.
- “utcOffset“is the offset in seconds between UTC-time and GPS-time. UTC-time continously adds leap seconds, but GPS-time does not, so the difference is a few seconds.

36 Display for Settings menu

RES521	RES521/Settings	.Set/PMUapp
Status	**PMUapp**	AI32_1 (*)
Settings	**Communication**	PMUOut_1 (*)
Service Report	**Time**	TIMEREF_1 (*)
	Restart	PHASOR3I_1- _4 (*)
	HMI	PHASOR3U_1- _2 (*)
		AMPPHASE_1 - _6 (*)
		TRIGGFREQ_1 (*)
		TRIGGDFREQ_1 (*)
		TRIGGOC4CH_1 (*)
		TRIGGUV2CH_1 (*)
		ABSREF_1 - _4

.Set/Communication
IP_Addr
IP_Mask
GateWay_IP
Ethernet_media
IEEE1344_Port
PC37.118_Port
PMU_Id1
PMU_Id2
1344_TransfRate
numberOfPhasor
numberOfDigital
stationName
phasor1Name
phasor2Name
phasor3Name
phasor4Name
phasor5Name
phasor6Name

(*) Setting data described in Chapter 7 “Functional description”

RES521	RES521/Settings	.Set/Communication
		digital1Name
		digital2Name
		digital3Name
		digital4Name
		digital5Name
		digital6Name
		digital7Name
		digital8Name
		ActiveSetGrp
		SetGrp1Name

RES521/Set/Time
Time_UTC

.Set/Restart
rebootTerminal

RES521/Set/HMI
langId
timePerKeyPoll
timeoutTime
autoRepeat
maxSetGroup

36.1 PMUapp

Data for PMUapp settings is described in Chapter 7 “Functional description” .
When changing and saving settings in PMUapp the application is automatically restarted.
When changing the rated frequency, TIMEREF_1/freqRated, the terminal has to be rebooted.

At the end of the PMUapp menu SetGroup can be found. This parameter is not used in RES 521*1.0 and should not be changed.

36.1.1 Absolute reference

ABSREF_1 ABSREF_8 are absolute references, i.e. constant values, given in the configuration according to chapter 11. **These constants should normally not be changed.**

36.2 Communication

When changing communication settings the terminal has to be rebooted.

- “IEEE1344_Port“ is the socket port for the IEEE1344 protocol.
- “PC37.118_Port“ is the socket port for the PC37.118 protocol.
- “PMU_Id1” and “PMU_Id2” is 2x32bit decimal numbers for identification of the terminal.

At the end of the menu Communication, ActiveSetGrp and SetGrp1Name can be found. These parameters are not used in RES 521*1.0 and they should not be changed.

36.3 Time

Here the UTC time and date can be checked.

36.4 Restart

To reboot the terminal change “rebootTerminal“ from No to Yes and then save the setting.

At the end of the menu Restart, ActiveSetGrp and SetGrp1Name can be found. These parameters are not used in RES 521*1.0 and they should not be changed.

36.5 HMI

This part of the menu controls the HMI.

- "langId" is the language parameter - only English is available.
- "timePerKeyPoll" controls how often the key pad is checked.
- "timeoutTime", the HMI is switched off after this time if no button is pushed.
- "autoRepeat" makes it possible to scroll fast in a menu by pressing a push button for a long time.
- "maxSetGroup" controls the maximum number of setting groups.

At the end of the menu HMI, ActiveSetGrp and SetGrp1Name can be found. These parameters are not used in RES 521*1.0 and they should not be changed.

37 Display for readings menu

RES521	**RES521/Sr**	**.RES521/Sr/PMUapp**	***Sr/PMUapp/AI32-1***
Status	**PMUapp**	**AI32_1**	*ch01 - ch32*
Settings		**BI8_1**	*Timestamp*
ServiceReport		**PmuOut_1**	
		PmuBO_1	

Sr/Pmuapp/BI8_1
ch01-ch08

.Pmuapp/PmuOut_1
frequency
deltaFrequency
amplitude01
phaseAngle01
:
amplitude06
phaseAngle06
out01 - out08
freqTrg
dFreqTrg
angleTrg
overCurrTrg
underVoltTrg
rateTrg
userTrg
timestamp

.Pmuapp/PmuBO_1
GPS
Data
freqHigh
freqLow
dFreqHigh
dFreqLow
underVolt 1
underVolt 2
overCurr 1
overCurr 2
overCurr 3

RES521	RES521/Sr	.RES521/Sr/PMUapp	.Pmuapp/PmuBO_1
			overCurr 4
			out 1
			out 2
			out 3
			out 4

The service report data shows actual readings in the input and output functional blocks of the application.

Chapter 7 Functional description

38 Introduction

The terminal provides highly accurate UTC date and time and data acquisition time base which makes simultaneous and highly accurate sampling of data possible even when the phasor measurement terminals are separated by large geographic distances.

39 Start-up delay

When using the terminal for the first time or if the terminal has not been used for several months acquiring satellite data will take several minutes. Moving the antenna to a new position could also affect the start-up time.

40 Date and time

The global positioning system provides time accuracy better than +/-0.5 µs, provided that the receiver position is known and not moving and that signals from at least four satellites are received.

The date and time obtained follows the *Coordinated Universal Time* standard, UTC. This standard covers handling of dates including leap years and time including leap seconds.

Leap seconds are introduced as necessary, primarily in the last minute of the months of December or June and in second hand in the last minute of March or September. Leap seconds are normally positive, but can be negative.

41 Self supervision

Check the LED indicators of the HMI to monitor the terminal’s current status.

Table 18: LED indications

LED	Operation		
	Off	**Lit**	**Flashing**
Green	Power off	Normal operation	Internal failure
Yellow	Normal operation	Not used	Recoverable error e.g. time sync error, terminal restoring services
Red	Normal operation	No GPS data received	GPS signal below acceptable quality

42 Calibration

RES 521 is equipped with three separate kinds of calibration to compensate amplitude and phase angle of the measured phasor, i.e. voltages or currents. The three separate calibrations are:

- Internal calibration due to inaccuracy of terminal measurement transformers.
- External calibration due to inaccuracy of substation instrument transformers.
- System calibration due to different phase angle in two parts of a power system, e.g. caused by Y/D-transformers (voltage calibration only).

The internal calibration parameters are not customer settable because the internal transformers are calibrated automatically before delivery. The external calibration parameters are settable by HMI interface. If the user does not change the parameters, the default values of parameters are automatically chosen.

The main purpose of the calibration function is to improve the accuracy of the measurement capability of the terminal, i.e. compensate for the inaccuracy of the input transformers inside the terminal - this calibration is made at the factory. An external calibration makes it possible for the (advanced) user to include a calibration curve for the external CTs and VTs. But it is not necessary to perform the external calibration since the instrument transformers are already good enough, for most applications.

The calibration is based on the following formula:

$$S_{calib} = Amp_{filter} * e^{jAng_{filter}} * Amp_{\mathrm{int}} * \mathrm{e}^{\mathrm{jAng_{int}}} * Amp_{ext} * \mathrm{e}^{\mathrm{jAng_{ext}}} * \mathrm{e}^{\mathrm{jAng_{sys}}}$$

Where:

S_{calib} = Calibrated signal, voltage or current.

Amp_{filter} = Amplitude of filtered signal.

Ang_{filter} = Angle of filtered signal.

Amp_{int} = Internal amplitude adjustment factor.

Ang_{int}= Internal angle adjustment value.

Amp_{ext}= External amplitude adjustment factor.

Ang_{ext}= External angle adjustment value.

Ang_{sys}= System angle adjustment (for voltage phasor only).

This means that the amplitude calibration is a factor, and the angle calibration is additive.

As mentioned above the external calibration points, i.e. the values for amplitude adjustment factor and phase angle adjustment for instrument transformers are settable. Further, these parameters are settable for current and voltage separately.

Seven settable points, amp_n, in percent of rated current or voltage forms eight class intervals in order to calibrate the physical input signals, see figure 16 and figure 17. Where these calibration points are from 5% to 300% of nominal current or voltage. Linear interpolation is used in all class intervals. Each interval may have different inclination depending on setting values, extAmpCalibm_n and extAngCalibm_n. Where:

m [1,2,3] is an indication of which phase will be calibrated and

n [1,2,3,4,5,6,7] is an indication of the chosen points on the nominal current or voltage.

Notice that the interval between zero and first point is constant, i.e. amp_1 is valid from zero to the first point of nominal current or voltage. The same thing is valid for the interval over the last point, i.e. amp_7 is valid from 300 percent of nominal current or voltage and upward.

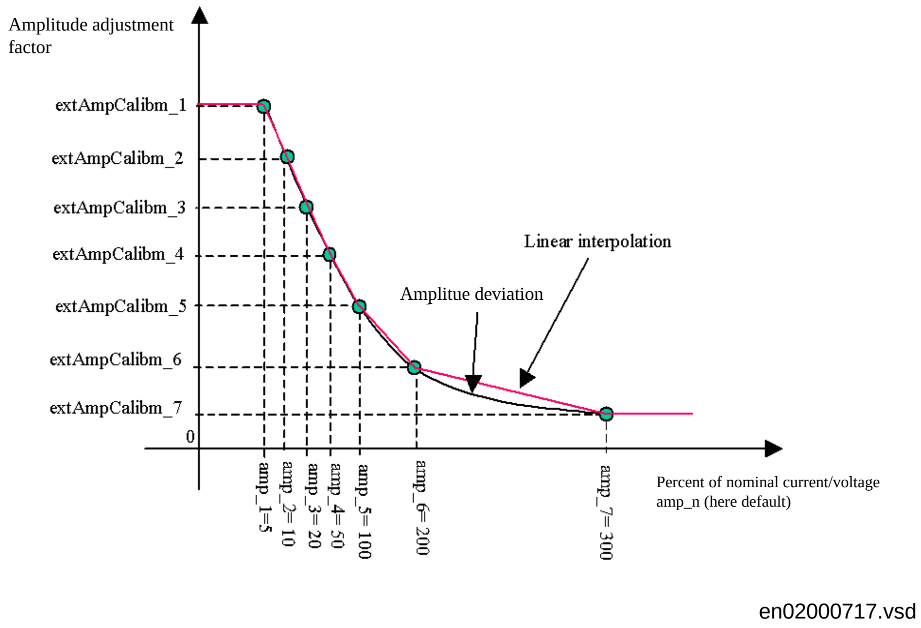


Figure 16: Amplitude adjustment.

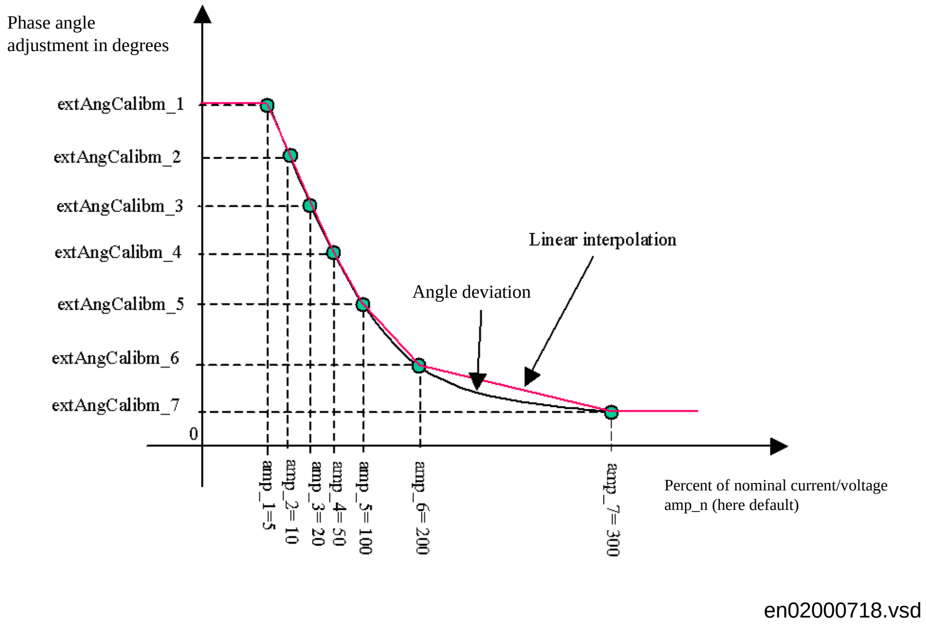


Figure 17: Phase angle adjustment.

43 Function block design and interface

This section describes the general design and interface of the different function blocks used in RES 521*1.0 standard configuration. The inputs and outputs are shown on each function block while the setting parameters are not shown in the function blocks. A square on the input side indicates that the input operates in the initialization phase and not in the execution phase. RES 521*1.0 configuration contains the following function blocks:

- AI32
- timeRef
- phasor3I
- phasor3U
- ampPhase
- triggFreq
- triggDFreq
- triggOC4ch
- triggUV2ch
- transfPh

- transfSc
- BO8
- PMUOut

43.1 Function block AI32

This function block is designed to connect the analogue inputs i.e.voltage and current quantities from RES 521 Analogue Input Module (AIM) via A/D-convertor to RES 521 application configuration. Time stamp from GPS time synchronization is also imported via AI32 function block.

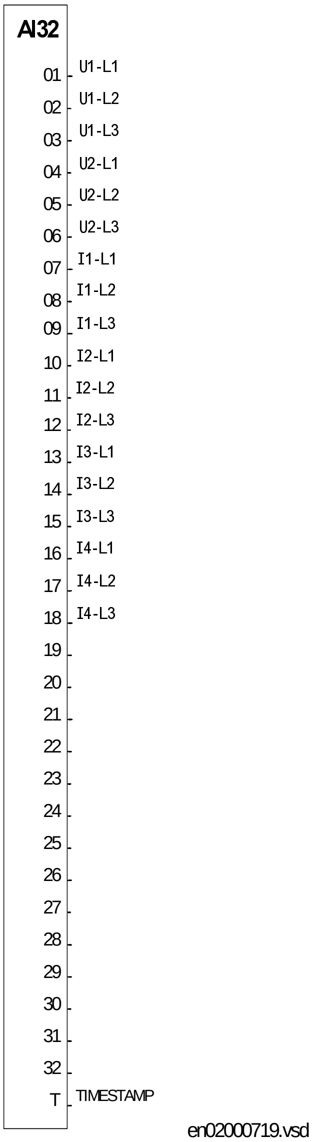


Figure 18: Function block AI32.

43.1.1 Output signal description

Table 19: Output signals

Signal	Description
U1-L1	Voltage phase L1, phasor 1
U1-L2	Voltage phase L2, phasor 1
U1-L3	Voltage phase L3, phasor 1
U2-L1	Voltage phase L1, phasor 2
U2-L2	Voltage phase L2, phasor 2
U2-L3	Voltage phase L3, phasor 2
I1-L1	Current phase L1, phasor 3
I1-L2	Current phase L2, phasor 3
I1-L3	Current phase L3, phasor 3
I2-L1	Current phase L1, phasor 4
I2-L2	Current phase L2, phasor 4
I2-L3	Current phase L3, phasor 4
I3-L1	Current phase L1, phasor 5
I3-L2	Current phase L2, phasor 5
I3-L3	Current phase L3, phasor 5
I4-L1	Current phase L1, phasor 6
I4-L2	Current phase L2, phasor 6
I4-L3	Current phase L3, phasor 6
TIME STAMP	GPS based time stamp.

Table 20: Settings

Parameter	Default	Description
Buffer_Size	1	AI32 buffer size

The Buffer_Size parameter controls the size of the analog input buffer in the AI32 function block, for alignments of incoming data.

43.2 Function block timeRef

The main purpose of function block timeRef is to compute a reference signal, a real part and an imaginary part, based on GPS time signal. It means that each phasor will be related and synchronized to the same reference, i.e. the GPS based time signal. Power system frequency, cycle time (filter window) and rate of change of frequency are also derived and measured in the timeRef function block.

Cycle time is the sampling window for the fourier filter used in RES 521. The fourier filter can operate with adaptive filter window or fixed filter window. This feature is settable by setting parameter “adaptiveOper”. A range of adaptive filter operation around rated frequency can also be set by setting parameters “freqLowLimit” and “freqHighLimit”.

The setting parameter “adaptiveOper”, TRUE, means that the filter window will vary with power system frequency. The parameter “adaptiveOper”, FALSE, means that the filter window will be fixed, no matter how the system frequency differ from rated frequency. The adaptive operation can be limited in a settable frequency range by setting parameters “freqLowLimit” and “freqHighLimit”.

TimeRef also includes a delay function called delay T3. This delay function is used to compensate for the group delay in the report filters. Delay T3 is actually a FIFO queue with settable depth. Time-stamp and reference angle (delta-phi) are queued together, the depth of the queue is calculated by multiplying group-delay (of selected report filter) and a delay factor. The delay factor can be 0, 1 or 2, representing last-, middle- or first- sample in window respectively. This facility gives the user the freedom to choose time stamping method.

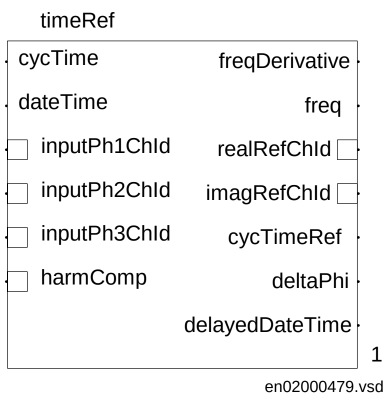


Figure 19: Function block timeRef.

43.2.1 Input, output and setting description

Table 21: Input signals

Signal	Default	Description
cycTime	1	Fundamental cycle time which is filter window (per unit value, as input always fixed)
dateTime		GPS time reference for all phasors
inputPh1ChId		Analogue (physical) channel used for reference signal and frequency measurement, phase L1
inputPh2ChId		Analogue channel used for reference signal and frequency measurement, phase L2
inputPh3ChId		Analogue channel used for reference signal and frequency measurement, phase L3
harmComp	1	Selected harmonic component

Table 22: Output signals

Signal	Description
freqDerivative	Measured rate of change of frequency, df/dt
freq	Measured system frequency
realRefChId	Real part of reference signal
imagRefChId	Imaginary part of reference signal
cycTimeRef	Measured fundamental cycle time, the reference for the filter window, adaptive/fixed depending on setting “adaptiveOper”
deltaPhi	Phase angle representing the absolute angular position of the physical input channels at each moment. DeltaPhi is derived from GPS time-stamp and delayed in T3
delayedDateTime	This time stamp is delayed in T3 to be used for time tagging of phasors in the communication protocols

Table 23: Settings

Parameter	Default	Description
freqLowLimit	40	Low frequency limit for adaptive operation
freqHighLimit	80	High frequency limit for adaptive operation
adaptiveOper	TRUE	Enables adaptive filter operation, i.e. varying filter window
freqRated	50	Rated frequency in Hz
timeTagging	Last	Time tagging princip first, center or last of calculation window

For the adaptive operation the frequency characteristic is symmetrical around a center frequency defined as (freqLowLimit + freqHighLimit) /2. Within this frequency interval the gain is very close to 1 and outside the interval the gain goes very rapidly to 0, see figure 20 and figure 21. If non-adaptivity is chosen, the filter is just centered to 50/60 Hz.

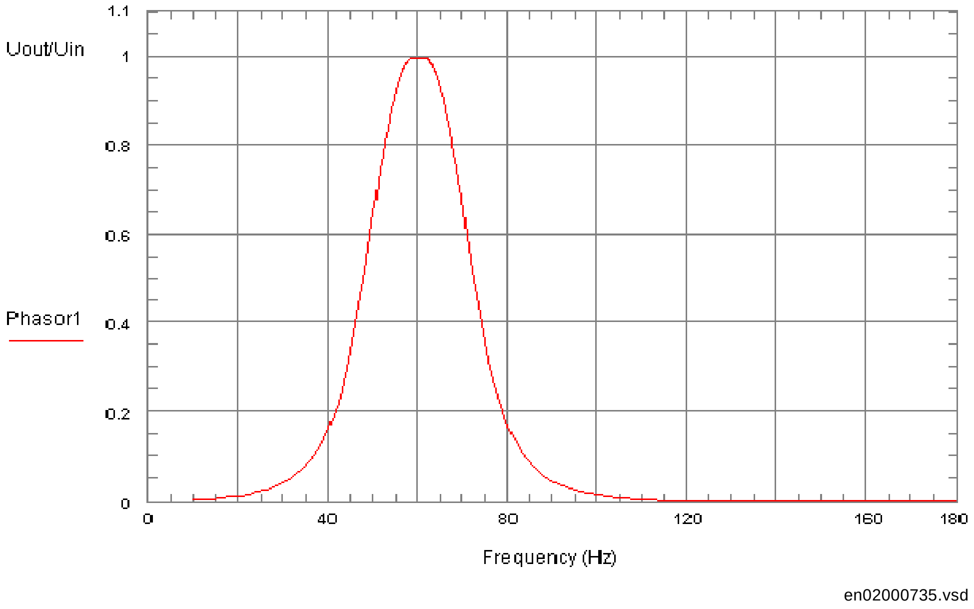


Figure 20: Frequency filter for adaptive operation 59-61 Hz.

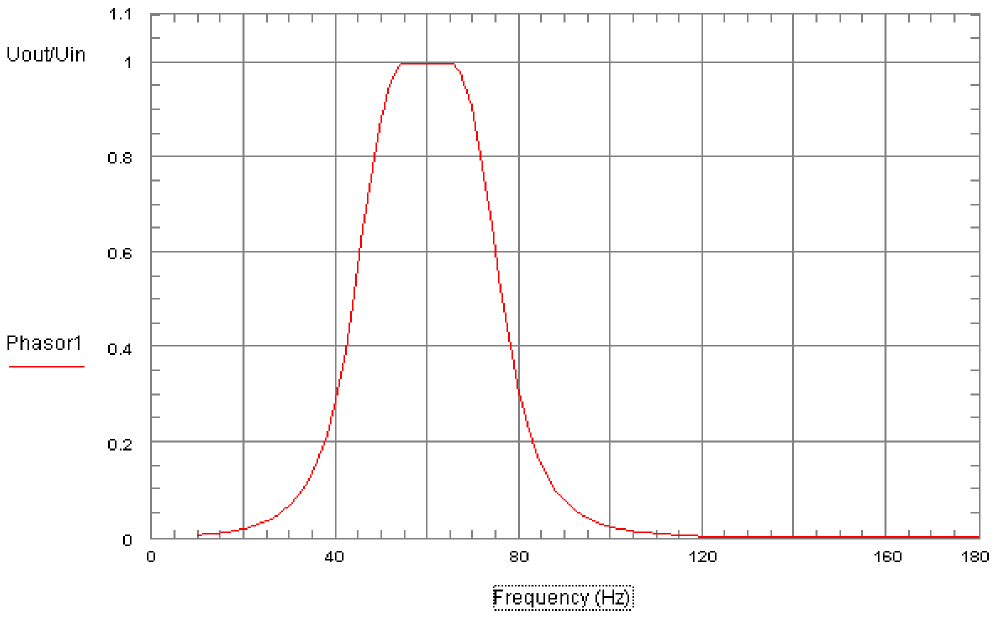


Figure 21: Frequency filter for adaptive operation 55-65 Hz.

43.3 Function block phasor3I

This function block carries out a 3-phase current phasor measurement and calibration. The physical input, in this case the currents, are calculated through adaptive Fourier filters and bandpass filters, then the current phasors are calibrated for both internal transformers and external transformers. Internal transformers are the terminal transformers, by external transformers we mean instrument transformers.

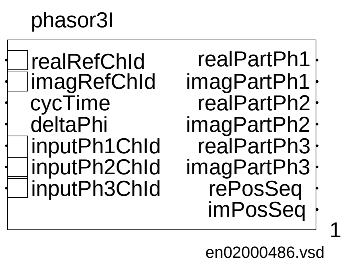


Figure 22: Function block phasor3I.

43.3.1 Input, output and setting description

Some input signals and settings are common for all three phases and some of them are specified for each phase. In the tables below x corresponds to phase L1, L2 or L3.

Table 24: Input signals

Signal	Description
realRefChId	Real part of reference signal
imagRefChId	Imaginary part of reference signal
cycTime	Measured fundamental cycle time, the reference for the Fourier filter window, adaptive/fixed depending on setting adaptiveOper in timeRef
deltaPhi	Phase angle representing the absolute angular position of the physical input channels at each moment
inputPhxChId	Analogue (physical) input channel , phase Lx

Table 25: Output signals

Signal	Description
realPartPhx	Calibrated real part of physical input
imagPartPhx	Calibrated imaginary part of physical input
rePosSeq	Calibrated real part of physical input, positive sequence
imPosSeq	Calibrated imaginary part of physical input, positive sequence

Table 26: Settings

Parameter	Default	Description
CTRatioExt	1	Current ratio, instrument transformer (Iprim/Isec), common to all three phases
CTRatedInt	1	Rated current terminal transformer (1 or 5 [A]), common to all three phases
nomI	1	Nominal current of transmission line, same for all three phases
amp1	5	Amplitude in % of nominal current (nomI), step 1
amp2	10	Amplitude in % of nominal current (nomI), step 2

Table 26: Settings

amp3	20	Amplitude in% of nominal current (nomI), step 3
amp4	50	Amplitude in% of nominal current (nomI), step 4
amp5	100	Amplitude in% of nominal current (nomI), step 5
amp6	200	Amplitude in% of nominal current (nomI), step 6
amp7	300	Amplitude in% of nominal current (nomI), step 7
extAmpCalx_1	1	Amplitude adjustment factor for external current, step 1
extAmpCalx_2	1	Amplitude adjustment factor for external current, step 2
extAmpCalx_3	1	Amplitude adjustment factor for external current, step 3
extAmpCalx_4	1	Amplitude adjustment factor for external current, step 4
extAmpCalx_5	1	Amplitude adjustment factor for external current, step 5
extAmpCalx_6	1	Amplitude adjustment factor for external current, step 6
extAmpCalx_7	1	Amplitude adjustment factor for external current, step 7
extAngCalx_1	0	Angle adjustment in degrees for external current, step 1
extAngCalx_2	0	Angle adjustment in degrees for external current, step 2
extAngCalx_3	0	Angle adjustment in degrees for external current, step 3
extAngCalx_4	0	Angle adjustment in degrees for external current, step 4
extAngCalx_5	0	Angle adjustment in degrees for external current, step 5
extAngCalx_6	0	Angle adjustment in degrees for external current, step 6
extAngCalx_7	0	Angle adjustment in degrees for external current, step 7

43.4 Function block phasor3U

This function block carries out a 3-phase voltage phasor measurement and calibration. The physical input, in this case the voltages, are calculated through adaptive Fourier filters and bandpass filters, then the voltage phasors are calibrated for both internal transformers and external transformers. Internal transformers are the terminal transformers, by external transformers we mean instrument transformers.

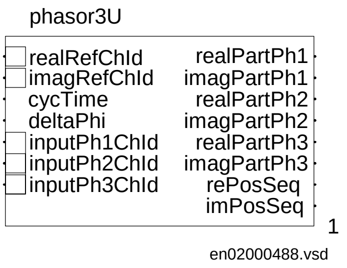


Figure 23: Function block phasor3U.

43.4.1 Input, output and setting description

Some input signals and setting parameters are common for all three phases and some of them are specified for each phase, see figure 24. In the tables below x corresponds to phase L1, L2 or L3.

Table 27: Input signals

Signal	Description
realRefChId	Real part of reference signal
imagRefChId	Imaginary part of reference signal
cycTime	Measured fundamental cycle time, the reference for the Fourier filter window, adaptive/fixed depending on setting adaptiveOper in timeRef
deltaPhi	Phase angle representing the absolute angular position of the physical input channels at each moment
inputPhxChId	Analogue (physical) input channel , phase Lx

Table 28: Output signals

Signal	Description
realPartPhx	Calibrated real part of physical input
imagPartPhx	Calibrated imaginary part of physical input
rePosSeq	Calibrated real part of physical input, positive sequence
imPosSeq	Calibrated imaginary part of physical input, positive sequence

Table 29: Settings

Parameter	**Default**	**Description**
VTRatioExt	1	Voltage ratio, instrument transformer (e.g. 132000/110 [V]), common to all phases
nomU	1	Nominal voltage (phase to earth) (e.g. 132000 / sqrt(3))
angSysCal	0	Calibration parameter for system angle in degrees
amp1	5	Amplitude in % of nominal voltage (nomU), step 1
amp2	10	Amplitude in % of nominal voltage (nomU), step 2
amp3	20	Amplitude in % of nominal voltage (nomU), step 3
amp4	50	Amplitude in % of nominal voltage (nomU), step 4
amp5	100	Amplitude in % of nominal voltage (nomU), step 5
amp6	200	Amplitude in % of nominal voltage (nomU), step 6
amp7	300	Amplitude in % of nominal voltage (nomU), step 7
extAmpCalx_1	1	Amplitude adjustment factor for external voltage, step 1
extAmpCalx_2	1	Amplitude adjustment factor for external voltage, step 2
extAmpCalx_3	1	Amplitude adjustment factor for external voltage, step 3
extAmpCalx_4	1	Amplitude adjustment factor for external voltage, step 4
extAmpCalx_5	1	Amplitude adjustment factor for external voltage, step 5
extAmpCalx_6	1	Amplitude adjustment factor for external voltage, step 6
extAmpCalx_7	1	Amplitude adjustment factor for external voltage, step 7
extAngCalx_1	0	Angle adjustment in degrees for external voltage, step 1
extAngCalx_2	0	Angle adjustment in degrees for external voltage, step 2
extAngCalx_3	0	Angle adjustment in degrees for external voltage, step 3

Table 29: Settings

extAngCalx_4	0	Angle adjustment in degrees for external voltage, step 4
extAngCalx_5	0	Angle adjustment in degrees for external voltage, step 5
extAngCalx_6	0	Angle adjustment in degrees for external voltage, step 6
extAngCalx_7	0	Angle adjustment in degrees for external voltage, step 7

43.5 Function block ampPhase

The main purpose of function block “ampPhase” is to convert the real and imaginary parts of a phasor to amplitude and phase angle. Angle compensation around positive real axis is the other feature of ampPhase. For example if the setting “deltaTheta” is set to 1 degree, then all angle values from 359 degrees to 1 degree will be shown as 0 degrees on the HMI. By choosing the deltaTheta to zero one may see on HMI when the angle changes between 0.0 and 359.9 degrees.

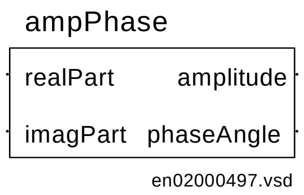


Figure 24: Function block ampPhase.

43.5.1 Input, output and setting description

Table 30: Input signals

Signal	Description
realPart	Real part of the phasor
imagPart	Imaginary part of the phasor

Table 31: Output signals

Signal	Description
amplitude	Amplitude of the phasor
phaseAngle	Phase angle of the phasor

Table 32: Settings

Parameter	Default	Description
deltaTheta	0	Angle compensating around 0 degrees

43.6 Sub function block comparator

This function block, used in the so-called trigg-blocks, is assigned to detect when the input signal “in” crosses the limit set by input “startValue”.

If input “invert” is set to FALSE, then the output “out” will be TRUE if the input signal “in” will become higher than “startValue”. The active hysteresis is the one giving the largest hysteresis of “hysteresisRelative” and “hysteresisAbsolute”, see figure 25..

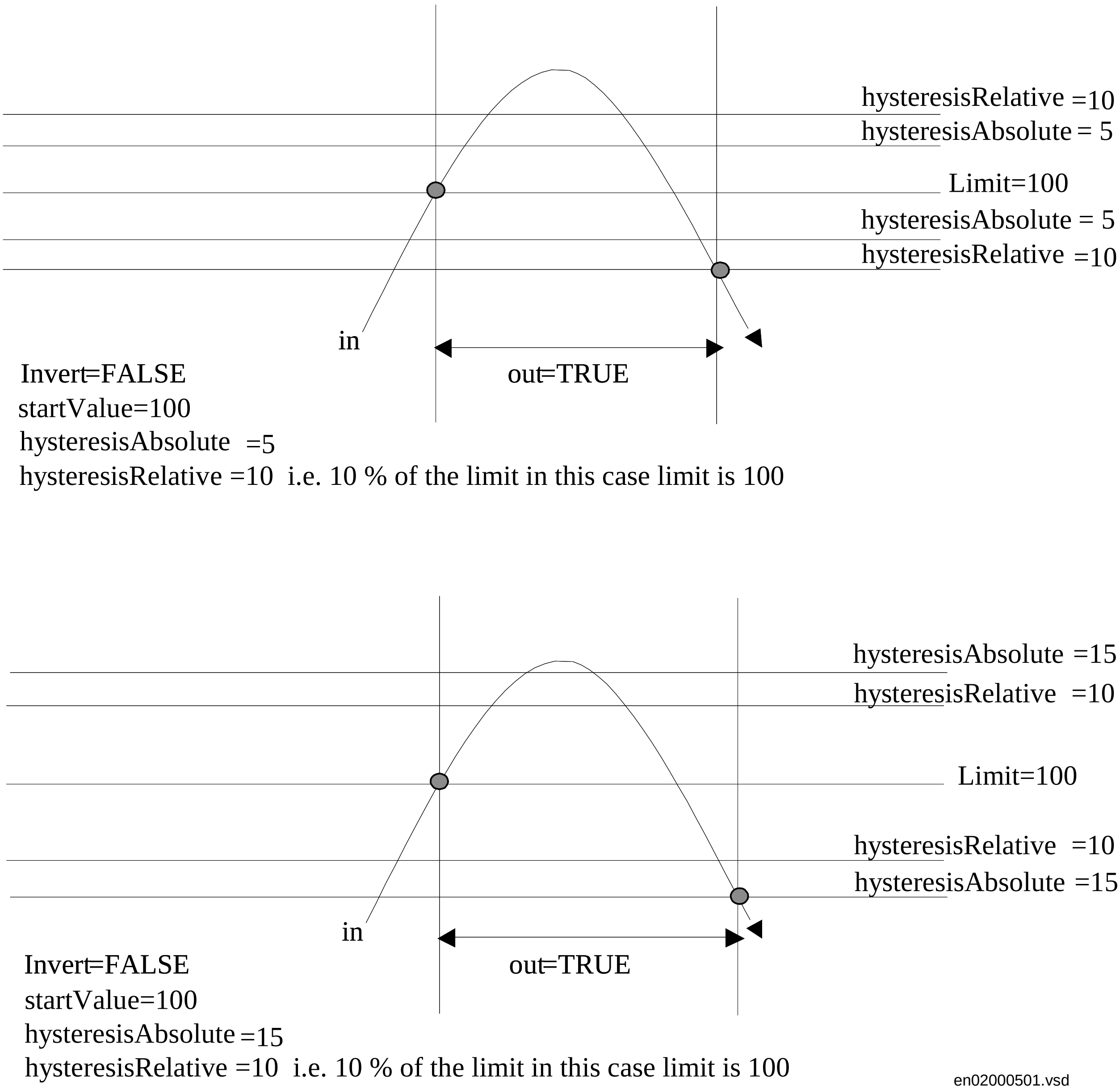


Figure 25: Example when the invert is set to FALSE.

If “invert” is set to TRUE, then the output “out” will be TRUE if the input signal “in” will become lower than “startValue”. The active hysteresis is the one giving the largest hysteresis of “hysteresisRelative” and “hysteresisAbsolute”, see figure 26.

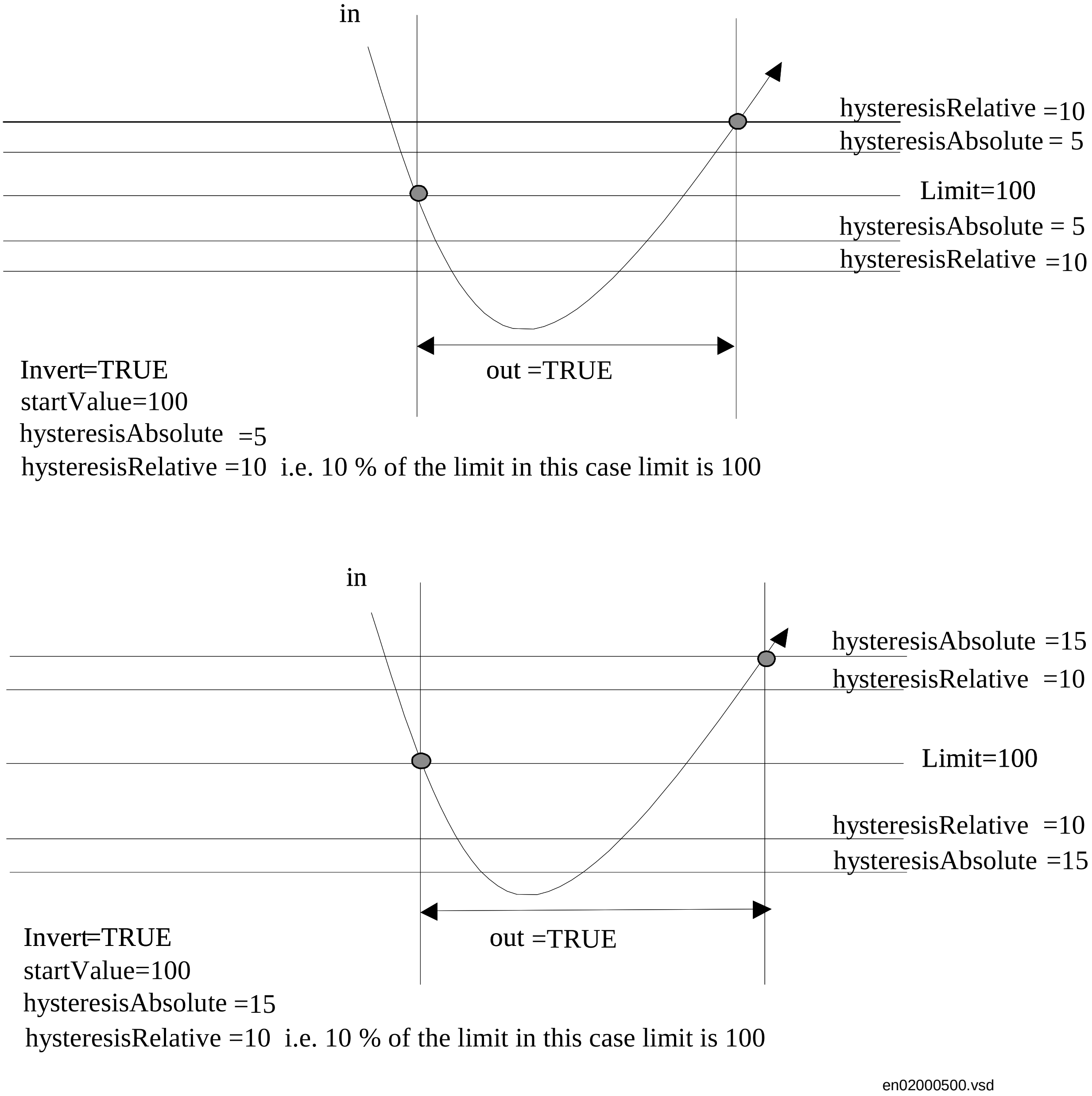


Figure 26: Example when the invert is set to TRUE.

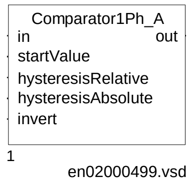


Figure 27: Function block comparator.

43.6.1 Input, output and setting description

Table 33: Input signals

Signal	Default	Description
in		input signal
startValue		Operate limit
hysteresisRelative		Relative hysteresis for operate limit
hysteresisAbsolute		Absolute hysteresis for operate limit
invert	FALSE	TRUE=>the output will be true if input signal is lower than the limit FALSE=> the output will be true if input signal is higher than the limit

Table 34: Output signals

Signal	Description
out	Indicating crossing of operate limit

43.7 Function block triggFreq

The triggFreq function block is a simple under- and over-frequency function. It has two independent comparators similar to the one described in section 43.6 ; one for the under-frequency part and one for the over-frequency part.
It is possible to delay the trigg and start output through time-on-delay (TON) timers. In addition, other timers (TOF) guarantee that a trigg and start pulse is not shorter than 15 ms. See outline in figure 29.

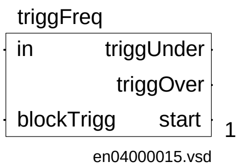


Figure 28: Function block triggFreq

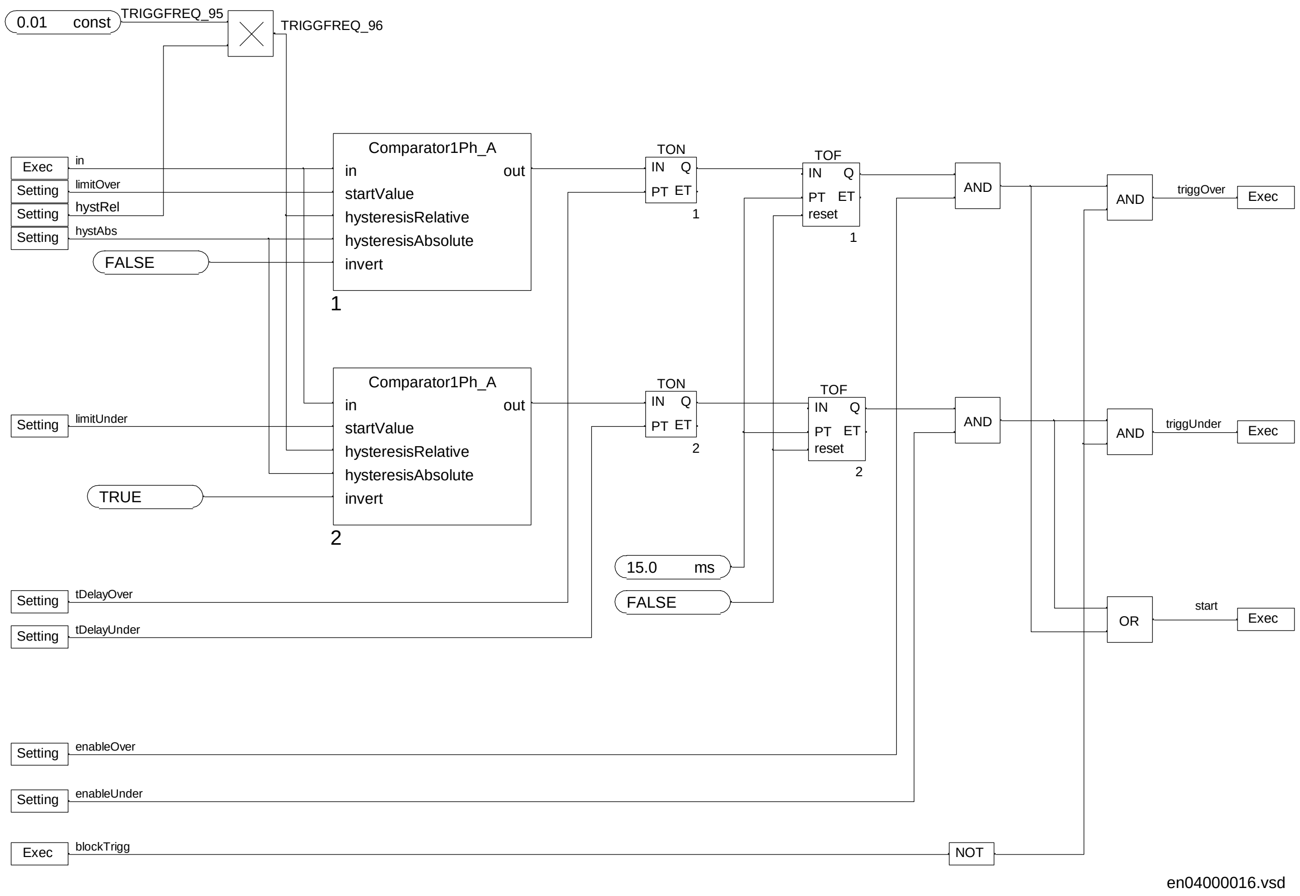


Figure 29: Outline of function block triggFreq

43.7.1 Input, output and setting description

Table 35: Input signals

Signal	Default	Description
in		The frequency input signal
blockTrigg		Disables trigg output (start is still enabled)

Table 36: Output signals

Signal	Description
triggUnder	Indicates that the frequency is below the lower limit “limitUnder”
triggOver	Indicates that the frequency is above the upper limit “limitOver”
start	Indicates that a limit has been surpassed

Table 37: Settings

Quantity	Parameter	Range and step	Default
Enable under-frequency trigger.	enableUnder	0,1 with step 1	1
Enable over-frequency trigger.	enableOver	0,1 with step 1	1
Limit under-frequency trigger, in Hz.	limitUnder	30.000-75.000 with step 0.001	55.000
Limit over-frequency trigger, in Hz.	limitOver	30.000-75.000 with step 0.001	55.000
Pick-up time delay under-frequency trigger, in ms.	tDelayUnder	100-999999 with step 1	100
Pick-up time delay over-frequency trigger, in ms.	tDelayOver	100-999999 with step 1	100
Relative value for hysteresis, in % of the limit.[a]	hystRel	0.0-100.0 with step 0.1	0.0
Absolute value for hysteresis, in Hz.[b]	hystAbs	0.000-100.000 with step 0.001	0.500

a) Hysteresis set as % of the limit, e.g. setting 10 means 10% of the limit.
b) Hysteresis set as an addition value to the limit. See figure 25 and figure 26.

43.8 Function block triggDFreq

The triggDFreq function block is a simple under- and over-rate of change of frequency function. It has two independent comparators similar to the one described in section 43.6 ; one for the under-rate of change of frequency part and one for the over-rate of change of frequency part.
It is possible to delay the trigg and start output through time-on-delay (TON) timers. In addition, other timers (TOF) guarantee that a trigg and start pulse is not shorter than 15 ms. See outline in figure 31.

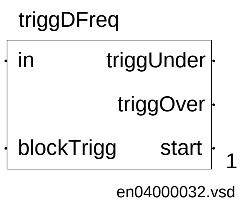


Figure 30: Function block triggDFreq

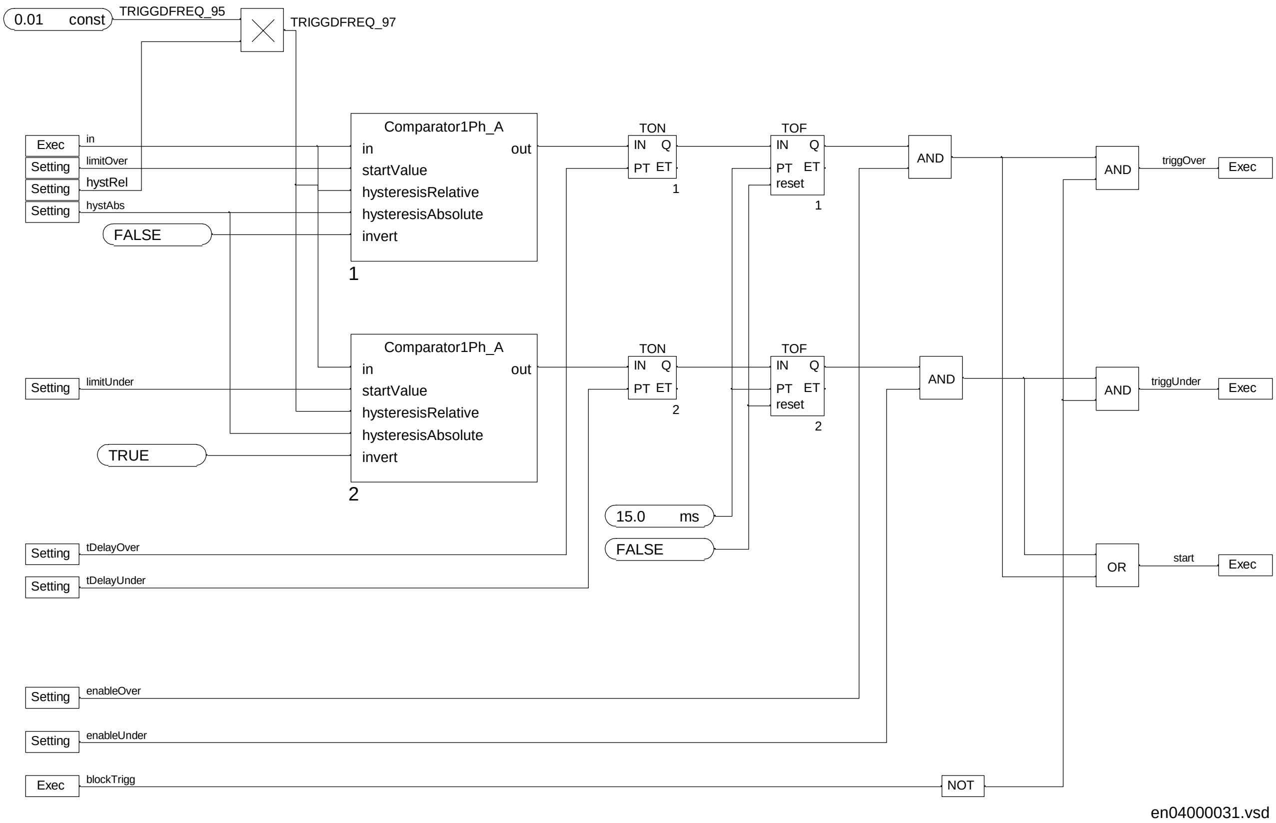


Figure 31: Outline of function block triggDFreq

43.8.1 Input, output and setting restriction

Table 38: Input signals

Signal	Default	Description
in		The rate of change of frequency input signal
blockTrigg		Disables trigg output (start is still enabled)

Table 39: Output signals

Signal	Description
triggUnder	Indicates that rate of change of frequency is below the lower limit “limitUnder”
triggOver	Indicates that rate of change of frequency is above the upper limit “limitOver”
start	Indicates that a limit has been surpassed

Table 40: Settings

Quantity	Parameter	Range and step	Default
Enable rate of change of under-frequency trigger.	enableUnder	0,1 with step 1	1
Enable rate of change of over-frequency trigger.	enableOver	0,1 with step 1	1
Limit rate of change of under-frequency trigger, in Hz/s	limitUnder	-100.000-0.000 with step 0.001	-10.000
Limit rate of change of over-frequency trigger, in Hz/s	limitOver	0.000-100.000 with step 0.001	10.000
Pick-up time delay rate of change of under-frequency trigger, in ms.	tDelayUnder	100-999999 with step 1	100
Pick-up time delay rate of change of over-frequency trigger, in ms.	tDelayOver	100-999999 with step 1	100
Relative value for hysteresis, in % of the limit.[a]	hystRel	0.0-100.0 with step 0.1	0.0
Absolute value for hysteresis, in Hz/s.[b]	hystAbs	0.000-100.000 with step 0.001	0.500

a) Hysteresis set as % of the limit, e.g. setting 10 means 10% of the limit.
b) Hysteresis set as an addition value to the limit. See figure 25 and figure 26.

43.9 Function block triggUV2ch

The triggUV2ch function block is a simple two-channel under-voltage function. It has two independent comparators similar to the one described in section 43.6 .
It is possible to delay the trigg and start output through time-on-delay (TON) timers. In addition, other timers (TOF) guarantee that a trigg and start pulse is not shorter than 15 ms. See outline in figure 33.

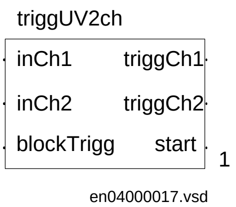


Figure 32: Function block triggUV2ch

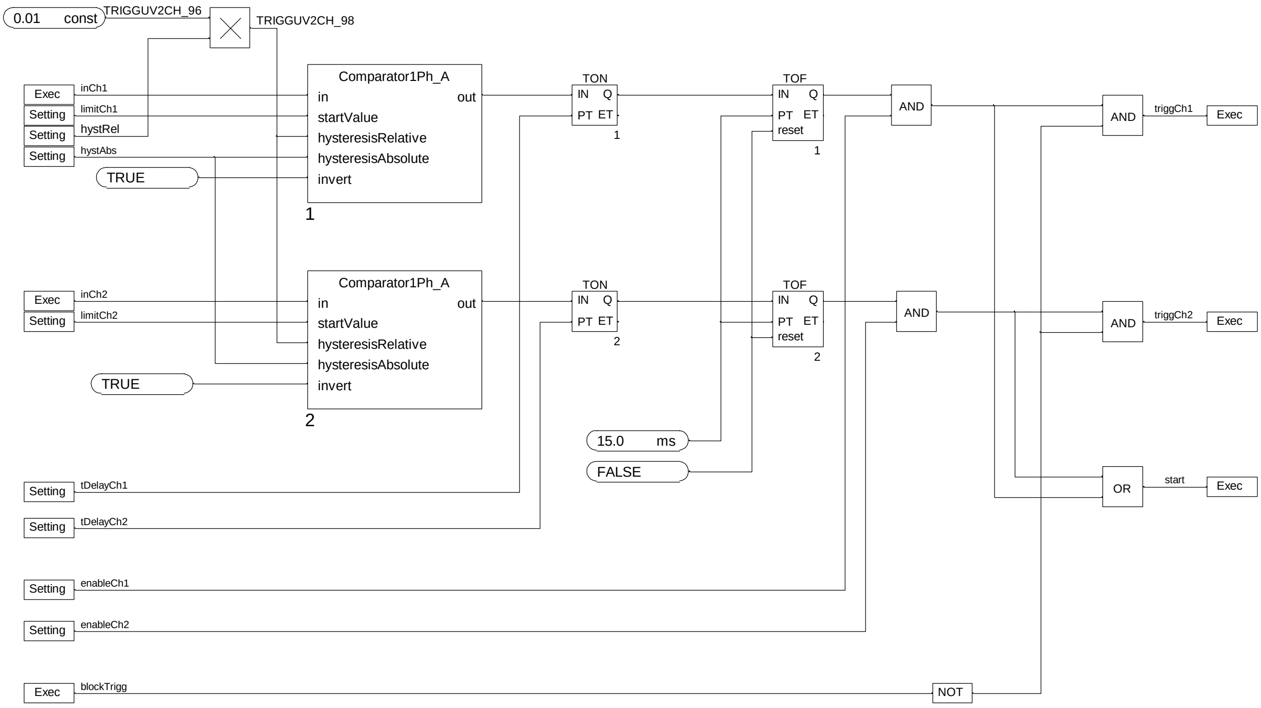


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Figure 33: Outline of function block triggUV2ch

43.9.1 Input, output and setting description

Table 41: Input signals

Signal	Default	Description
inCh1		Input signal for the first channel
inCh2		Input signal for the second channel
blockTrigg		Disables trigg output (start is still enabled)

Table 42: Output signals

Signal	Description
triggCh1	Indicates that the voltage is below the limit (“limitCh1”) for the first channel
triggCh2	Indicates that the voltage is below the limit (“limitCh2”) for the first channel
start	Indicates that at least one limit has been surpassed

Table 43: Settings

Quantity under voltage	Parameter	Range and step	Default
Enable under-voltage trigger phasor 1.	enableCh	0,1 with step 1	1
Enable under-voltage trigger phasor 2.	enableCh2	0,1 with step 1	1
Limit under-voltage trigger, in V phasor 1.	limitCh1	0-1000000 with step 1	230000
Limit under-voltage trigger, in V phasor 2.	limitCh2	0-1000000 with step 1	230000
Pick-up time delay under-voltage trigger, in ms phasor 1.	tDelayCh1	100-999999 with step 1	100
Pick-up time delay under-voltage trigger, in ms phasor 2.	tDelayCh2	100-999999 with step 1	100
Relative value for hysteresis, in % of the limit.[a]	hystRel	0.0-100.0 with step 0.1	10
Absolute value for hysteresis, in V.[b]	hystAbs	0-1000000 with step 1	0

a) Hysteresis set as % of the limit, e.g. setting 10 means 10% of the limit.
b) Hysteresis set as an addition value to the limit. See figure 25 and figure 26.

43.10 Function block triggOC4ch

The triggOC4ch function block is a simple four-channel over-current function. It has four independent comparators similar to the one described in section 43.6 .
It is possible to delay the trigg and start output through time-on-delay (TON) timers. In addition, other timers (TOF) guarantee that a trigg and start pulse is not shorter than 15 ms. See outline in figure 35.

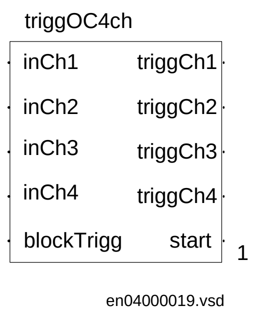

Figure 34: Function block triggOC4ch

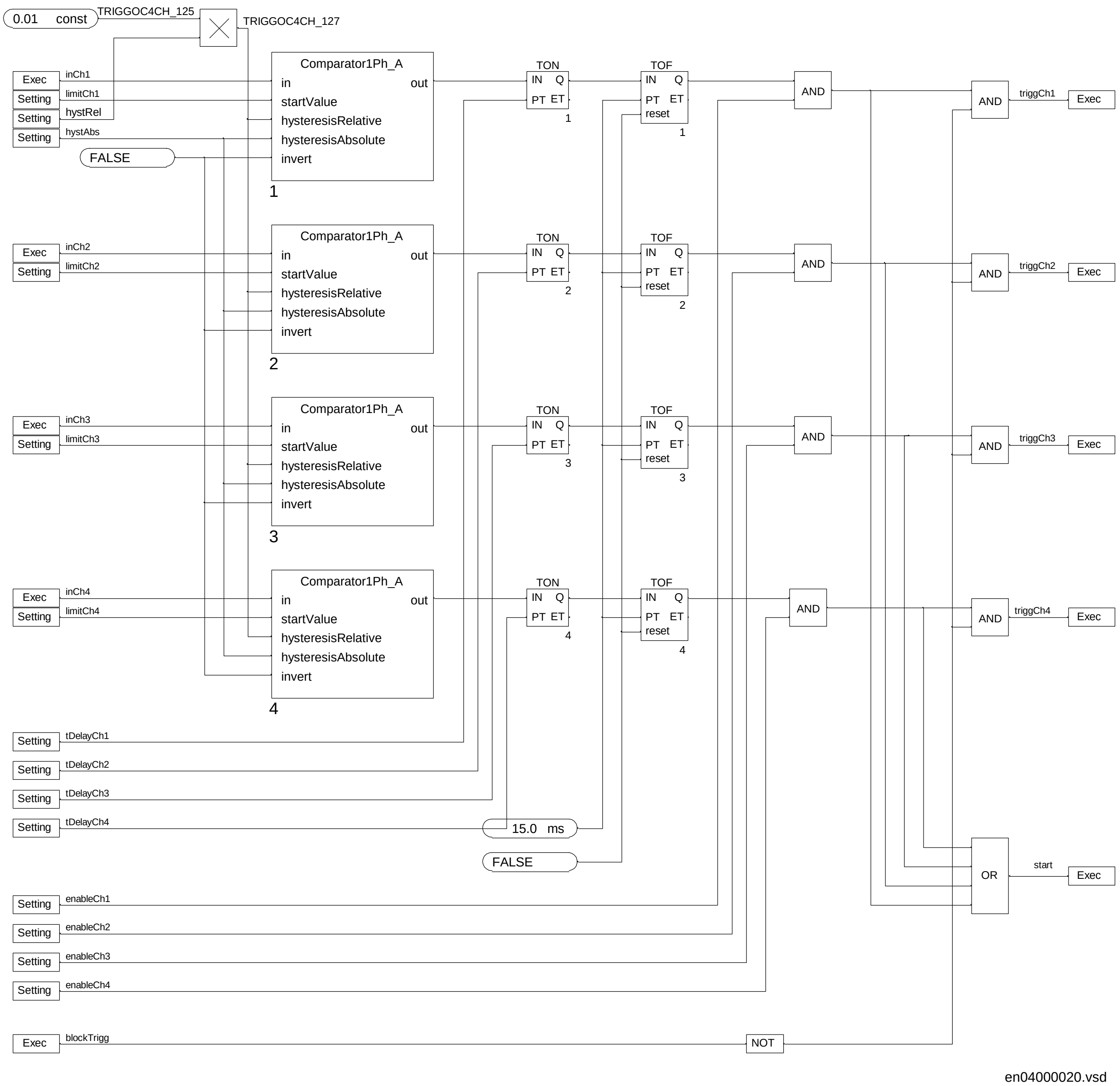

Figure 35: Outline of function block triggOC4ch

43.10.1 Input, output and setting description

Table 44: Input signals

Signal	Default	Description
inCh1		Input signal for the first channel
inCh2		Input signal for the second channel
inCh3		Input signal for the third channel
inCh4		Input signal for the fourth channel
blockTrigg		Disables trigg output (start is still active)

Table 45: Output signals

Signal	Description
triggCh1	Indicates that the current is above the limit (“limitCh1”) for the first channel
triggCh2	Indicates that the current is above the limit (“limitCh2”) for the second channel
triggCh3	Indicates that the current is above the limit (“limitCh3”) for the third channel
triggCh4	Indicates that the current is above the limit (“limitCh4”) for the fourth channel
start	Indicates that at least one limit has been surpassed

Table 46: Settings

Quantity	Parameter	Range and step	Default
Enable over-current trigger phasor 1.	enableCh1	0,1 with step 1	1
Enable over-current trigger phasor 2.	enableCh2	0,1 with step 1	1
Enable over-current trigger phasor 3.	enableCh3	0,1 with step 1	1
Enable over-current trigger phasor 4.	enableCh4	0,1 with step 1	1
Limit over-current trigger, in A phasor 1.	limitCh1	0-50000 with step 1	5000
Limit over-current trigger, in A phasor 2.	limitCh2	0-50000 with step 1	5000
Limit over-current trigger, in A phasor 3.	limitCh3	0-50000 with step 1	5000
Limit over-current trigger, in A phasor 4.	limitCh4	0-50000 with step 1	5000
Pick-up time delay over-current trigger, in ms phasor 1.	tDelayCh1	100-999999 with step 1	100
Pick-up time delay over-current trigger, in ms phasor 2.	tDelayCh2	100-999999 with step 1	100
Pick-up time delay over-current trigger, in ms phasor 3.	tDelayCh3	100-999999 with step 1	100
Pick-up time delay over-current trigger, in ms phasor 4.	tDelayCh4	100-999999 with step 1	100
Relative value for hysteresis, in % of the limit.[a]	hystRel	0.0-100.0 with step 0.1	10
Absolute value for hysteresis, in A.[b]	hystAbs	0-50000 with step 1	0

a) Hysteresis set as % of the limit, e.g. setting 10 means 10% of the limit.
b) Hysteresis set as an addition value to the limit. See figure 25 and figure 26.

43.11 Function blocks transfPh

This function block prepares a phasor signal to be transfered to the IEEE 1344 Synchrophasor streaming data. The phasor is filtered in order to suppress anti-aliasing effects (see section 43.14.2.1). The type of filter characteristic is selected under Communication settings.

Some of the filter characteristics result in quite long group delays, so in order not to have this affect the trigger performance this function block is made into a separate element, placed after the trigger function blocks in the signal flow.

After filtering, the phasor is synchronized to the GPS based reference signal through input “deltaPhi”.

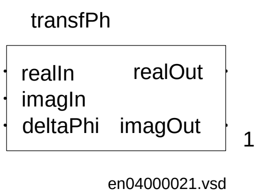

Figure 36: Function block transfPh.

43.11.1 Input and output description

Table 47: Input signals

Signal	Description
realIn	Real part of input phasor
imagIn	Imaginary part of input phasor
deltaPhi	Phase angle representing the absolute angular position of the physical input channels at each moment

Table 48: Output signals

Signal	Description
realOut	Real part of filtered and synchronized output phasor
imagOut	Imaginary part of filtered and synchronized output phasor

43.12 Function blocks transfSc

This function block prepares a scalar signal to be transfered to the IEEE 1344 Synchrophasor streaming data. The signal is filtered in order to suppress anti-aliasing effects (see section 43.14.2.1). The type of filter characteristic is selected under Communication settings.

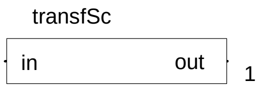

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Figure 37: Function block transfSc.

43.12.1 Input and output description

Table 49: Input signals

Signal	Description
in	Input scalar signal

Table 50: Output signals

Signal	Description
out	Filtered output scalar signal

43.13 Function block PmuBO

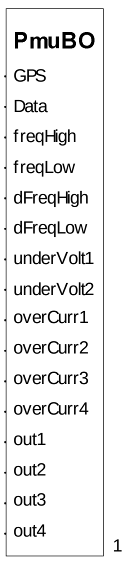

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Figure 38: Function block Binary Out, PmuBO.

43.13.1 Output description

Table 51: Output signals

Signals	Default	Description
GPS	0	GPS synch lost
Data	0	Data out
freqHigh	0	High frequency
freqLow	0	Low frequency
dFreqHigh	0	High rate of change of frequency
dFreqLow	0	Low rate of change of requency
underVolt1	0	Undervoltage phasor 1
underVolt2	0	Undervoltage phasor 2
overCurr1	0	Overcurrent phasor 3
overCurr2	0	Overcurrent phasor 4
overCurr3	0	Overcurrent phasor 5
overCurr4	0	Overcurrent phasor 6

The signal GPS is activated if the GPS synchronization fails, and the time accuracy of 1 microsecond is lost. The most probable reason to get this alarm is that the antenna has been shaded, and the number of observed satellites has been to few. This is the same binary signal as sent in the IEEE synchrophasor format, called "synchronization status".

The signal Data Out, is activated if at least one communication connection is established and active. The communication connection can be either of IEEE1344 or PC37.118 type.

The signal freqHigh is activated if the frequency exceeds the setting of parameter TRIGGFREQ_1/limitOver (see section 36 and 43.7) for a time longer than the setting of parameter TRIGGFREQ_1/tDelayOver.

The signal freqLow is activated if the frequency is below the setting of parameter TRIGGFREQ_1/limitUnder (see section 36 and 43.7) for a time longer than the setting of parameter TRIGGFREQ_1/tDelayUnder.

The signal dFreqHigh is activated if the rate of change of frequency exceeds the setting of parameter TRIGGDFREQ_1/limitOver (see section 36 and 43.7) for a time longer than the setting of parameter TRIGGDFREQ_1/tDelayOver.

The signal dFreqLow is activated if the frequency is below the setting of parameter TRIGGDFREQ_1/limitUnder (see section 36 and 43.7) for a time longer than the setting of parameter TRIGGDFREQ_1/tDelayUnder.

The signal underVolt1 is activated if the voltage magnitude of phasor 1 is below the setting of parameter TRIGGUV2CH_1/limitCh1 for a longer time than the setting of parameter TRIGGUV2CH_1/tDelayCh1.

The signal underVolt2 is activated if the voltage magnitude of phasor 2 is below the setting of parameter TRIGGUV2CH_1/limitCh2 for a longer time than the setting of parameter TRIGGUV2CH_1/tDelayCh2.

The signal overCurr1 is activated if the current magnitude of phasor 3 exceeds the setting of parameter TRIGGOC4CH_1/limitCh1 for a longer time than the setting of parameter TRIGGOC4CH_1/tDelayCh1.

The signal overCurr2 is activated if the current magnitude of phasor 4 exceeds the setting of parameter TRIGGOC4CH_1/limitCh2 for a longer time than the setting of parameter TRIGGOC4CH_1/tDelayCh2.

The signal overCurr3 is activated if the current magnitude of phasor 5 exceeds the setting of parameter TRIGGOC4CH_1/limitCh3 for a longer time than the setting of parameter TRIGGOC4CH_1/tDelayCh3.

The signal overCurr4 is activated if the current magnitude of phasor 6 exceeds the setting of parameter TRIGGOC4CH_1/limitCh4 for a longer time than the setting of parameter TRIGGOC4CH_1/tDelayCh4.

43.14 Function block PMUOut

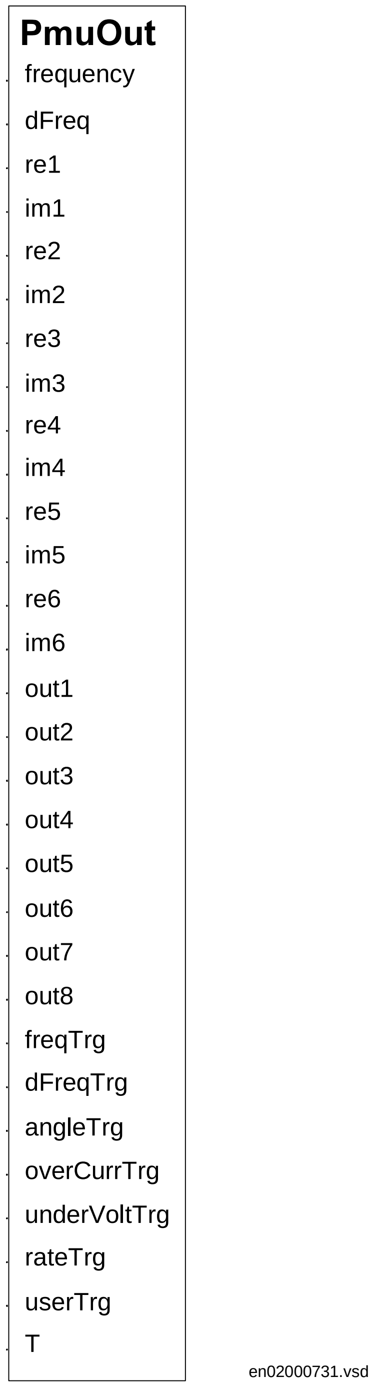


Figure 39: Function block PMUOut.

43.14.1 Output description

Table 52: Output signals

Signals	Description
frequency	Measured system frequency
dFreq	Rate of change of frequency
re1	Real part of phasor 1, positive sequence in RMS
im1	Imaginary part of phasor 1, positive sequence in RMS
re2	Real part of phasor 2, positive sequence in RMS
im2	Imaginary part of phasor 2, positive sequence in RMS
re3	Real part of phasor 3, positive sequence in RMS
im3	Imaginary part of phasor 3, positive sequence in RMS
re4	Real part of phasor 4, positive sequence in RMS
im4	Imaginary part of phasor 4, positive sequence in RMS
re5	Real part of phasor 5, positive sequence in RMS
im5	Imaginary part of phasor 5, positive sequence in RMS
re6	Real part of phasor 6, positive sequence in RMS
im6	Imaginary part of phasor 6, positive sequence in RMS
out1	Binary input 1, blockTrigg
out2	Binary input 2
out3	Binary input 3
out4	Binary input 4
out5	Binary input 5
out6	Binary input 6
out7	Binary input 7
out8	Binary input 8
freqTrg	Abnormal frequency
dFreqTrg	Abnormal rate of change of frequency
angleTrg	Not used
overCurrTrg	Overcurrent
underVoltTrg	Undervoltage
rateTrg	Not used
UserTrg	Not used
T	Time stamp

Table 53: Settings

Parameter	Default	Description
Angle_Ref	Time	Angle reference for HMI readings only, Time or any phasor

When reading the phasors (amplitude and phase angle) on the HMI, via the commands: Readings/PMUapp/PMUOut_1, the parameter Angle_Ref makes it possible to choose any phasor or time as reference for these readings, “Display for readings menu” on page 52. It usually makes more sense to select a voltage phasor as the reference for HMI readings, than to use the default value, i.e. time. The Angle_Ref parameter only affects the HMI readings. The data sent on the ethernet output always has time as reference.

43.14.2 Synchrophasor streaming data

RES 521 is equipped with two versions of synchrophasor streaming data protocol and they can be used simultaneously.

Both protocols are implemented on TCP/IP Sockets:

1. IEEE1344 according to the IEEE1344-1995 standard.
2. PC37118 according to the draft 2.51 of the PC37.118 IEEE standard.
   Some exceptions are made from the standard, the data part of the config frames are according to the IEEE1344. The SYNC word in the command frame (sent by the client) is not implemented.
   So the command frame should be according to IEEE1344 for both protocols. See the table below.

Table 54: Streaming data frame types

FrameType	Header	DataPart
DataFrame	PC37.118	PC37.118
ConfigFrame1,2	PC37.118	IEEE1344
HeaderFrame	PC37.118	PC37.118 (same as IEEE1344)
CmdFrame	IEEE1344	IEEE1344

43.14.2.1 Filtering

Channels that are to be included in the IEEE 1344 Synchrophasor streaming data (phasors and frequency) are filtered in order to suppress antialiasing effects, as the rate of the IEEE 1344 data is much slower than the data rate for internal processing.

There are six different filter characteristics to chose from.
As these filter characteristics are designed for -40dB at a specific frequency (half the 1344 transfer frequency for the last three characteristics) it is convenient to denote them using this frequency, expressed as a fraction of the rated power system frequency f0 (i.e. x/y times f0).

Table 55: IEEE 1344 transfer filter selection

#	Description	Total Group delay at f0 = 60 Hz	Total Group delay at f0 = 50 Hz	Comment
0	No filter for IEEE1344 transfer	10.4 ms	12.5 ms	Only the limited filtering in the “phasor3I/U” blocks. Not good for aliasing suppression.
1	-40dB at 7/8 of f0	25.5 ms	30.5 ms	Alternative with larger bandwidth
2	-40dB at 6/8 of f0	34.4 ms	41.2 ms	Alternative with larger bandwidth
3	-40dB at 1/2 of f0	61.4 ms	73.7 ms	Intended for transfer rate every cycle
4	-40dB at 1/4 of f0	129.4 ms	155.2 ms	Intended for transfer rate every other cycle
5	-40dB at 1/8 of f0	254.2 ms	305.0 ms	Intended for transfer rate every fourth cycle

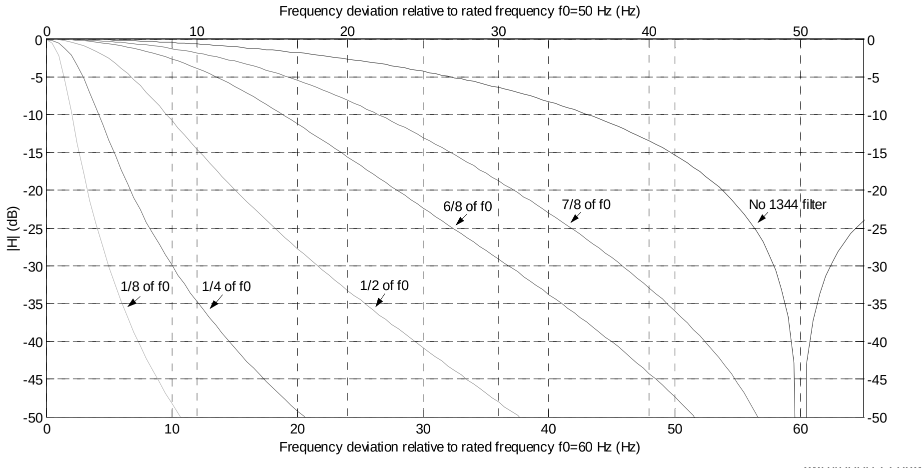


Figure 40: Attenuation of filters.

43.14.2.2 Configuration

Both protocols use the same configuration except for the socket port number.

Table 56: HMI:Settings/Communication

Parameter	Default	Description
IP_Addr	10.1.150.3	IP-Address
IP_Mask	255.255.255.0	Subnet mask
GateWay_IP	10.1.150.1	Gateway
Ethernet_media	Galvanic	Ethernet Connection
IEEE1344_Port	4711	IEEE 1344 Socket Port
PC37.118_Port	4712	PC37118SocketPort
PMU_Id1	0	PMU ID Hi 32 bit (Decimal). The 64 bit PMU Id is split into two 32 bit integers
PMU_Id2	0	PMU ID Low 32 bit (Decimal)
1344_TransfRate	1 every cycle	Data Transfer Rate
reportFiltSel	0	Selection of 1344 transfer filter selection
1344_sendUDP	off	Data output on UDP on/off
UDP_format	IEEE1344	Format of UDP data IEEE1344 or PC 37.118
UDP_Broadcast	234.5.6.7	UDP destination IP address
numberOfPhasor	6	Number of Phasors
numberOfBinary	8	Number of Digitals

Table 56: HMI:Settings/Communication

stationName	Station Name$	Number of Station
phasor1Name	phasor1$	Name of Phasor 1
phasor2Name	phasor2$	Name of Phasor 2
phasor3Name	phasor3$	Name of Phasor 3
phasor4Name	phasor4$	Name of Phasor 4
phasor5Name	phasor5$	Name of Phasor 5
phasor6Name	phasor6$	Name of Phasor 6
digital1Name	blockTriggers$	Blockof binary output triggers
digital2Name	digital2$	Name of Digital 2
digital3Name	digital3$	Name of Digital 3
digital4Name	digital4$	Name of Digital 4
digital5Name	digital5$	Name of Digital 5
digital6Name	digital6$	Name of Digital 6
digital7Name	digital7$	Name of Digital 7
digital8Name	digital8$	Name of Digital 8
ActiveSetGrp	Grp1	Active Setting Group
SetGrp1Name	Grp1$	Name of Setting Group1

43.14.2.3 How to alter settings and configuration:

HMI: Means that the setting is found in the local HMI tree.

The Terminal needs to be restarted to get the new communication settings active.

The IEEE1344 header frame needs to be downloaded to the RES 521 terminal via ftp, with the target location:/flash/IEEE1344HEADER.TXT.

- Use the command line ftp client in windows NT/2000 or 95/98.
- No password is required even though it is asked for.
- Use binary transfer mode.

Example:

ftp 192.168.1.10 (Start the ftp client from the location where you have the config files)

> u (return is ok as user)
> p (return is ok as password)
> binary
> cd /flash
> put IEEE1344HEADER.TXT
> dir (optional)
> bye

Most FTP clients with GUI will not work, however WS_FTP pro (www.ipswitch.com) is a GUI based ftp client that do work if the host type is set to vxWorks.

The IEEE1344HEADER.TXT file is a plain text file that can be edited in a text editor.

RES 521 is delivered with default configuration files.

44 Short guidance for the use of UDP

The UDP implementation in RES 521 is actually a UDP multicast server. To get data from RES 521, just subscribe to the multicast server and data will come. The multicast server sends only data frames. Header frames and configuration frames have to be achieved in another way, for example by the use of TCP.

It is possible to set the multicast address from the HMI, its located at Settings->Communication->UDP_Broadcast. There is no check that the multicast address is correct or even valid. There is no way to change the port that the multicast server sends to, its fixed to 8910.

If no one is listening to the multicast data communication, it is possible to turn it of, either using the HMI at Settings->Communication->1344_sendUDP; change the "ON" to "OFF", or by sending a IEEE1344 command frame containing RTDOFF or RTDON to the terminal on port 4713 with TCP.

If the RTDON/RTDOFF is changed from a remote place, the settings will not be saved, so the next time a save or reboot command is issued, the previous value is used.

Data can be sent either as IEEE1344 frames or as PC37.118 frames. The selection is made under Settings->Communication->UDP_format.

Chapter 8 Design

This chapter gives an overview of the product design and its hardware modules.

45 Introduction

RES 521 phasor measurement terminal is designed for *power system protection*. So far protection terminals have been focused on *equipment protection*, such as line protection, transformer protection, etc. The aim of the protection devices have been to identify and isolate faulted or overloaded equipment, in order to save the equipment from damage, save people and property, and re-establish the power supply to the healthy parts of the system. The purpose of *power system protection* is to take necessary actions, to save the system and minimise the negative impact, when the power system is in transition towards an instability, even though no equipment is faulty or operated outside its limits.

RES 521 terminal is the first version of the general system protection terminal. The PMU provides power system angles by direct measurements, using the GPS time system as a common reference. By direct measurement of power system angles, algorithms to counteract power oscillations and out-of-step conditions can be designed and state estimation can be improved compared with traditional methods.

46 Basics

RES 521 is based on the same hardware platform as RET 521 and RED 521. Application specific software modules are then added to create a specific terminal type or family. Modules are described in detail in the following sections.

47 Casing

RES 521 is delivered using a full-sized (1/1 x 6U) assembly suitable for 19" rack, flush or wall mounting. Suitable mounting kits are available for ordering. See technical overview brochure “Mechanical design and mounting accessories” for series RE 500 products for details.

48 Common modules

48.1 General

This section gives an overview of the common modules the terminal is or might be equipped with and their purpose. For in-depth information concerning design details, please contact ABB Automation Technology Products AB.

48.2 Combined backplane module (CBM)

The dual bus combination backplane module supports both CompactPCI and CAN based modules. There are 8 CompactPCI and 4 CAN slots available. Each module can be electronically identified by its factory programmed serial number, article number, hardware version and final test date. Every signal is impedance matched to 65Ω ±10%, calculated for a bare circuit-board.

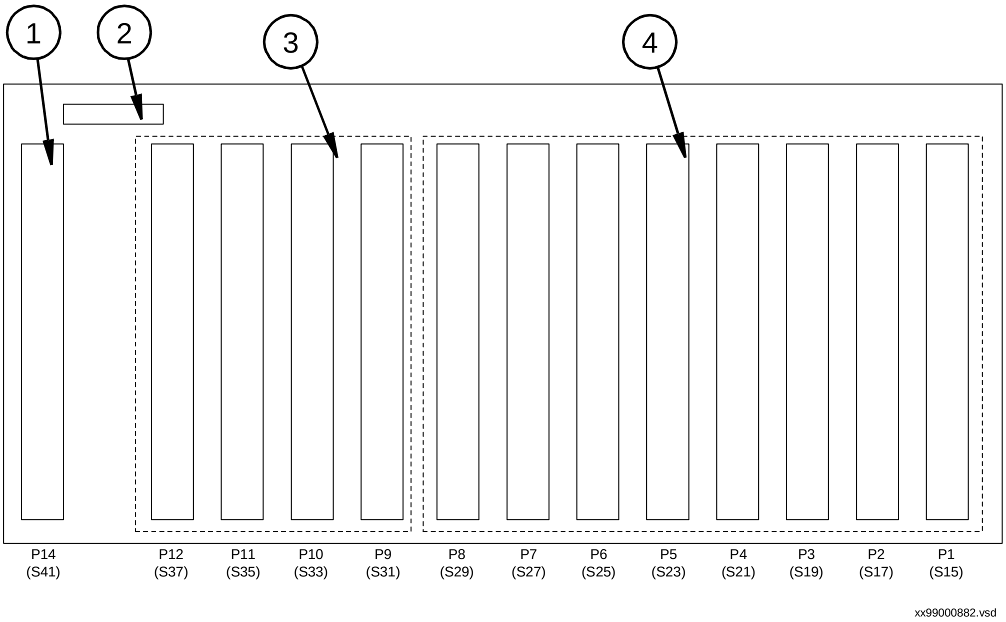


Figure 41: CBM connectors.

Table 57: Backplane connectors

	Connector
1	Power connector
2	HMI connector
3	CAN connectors
4	CompactPCI connectors

48.3 Power supply module (PSM)

The power supply module is a fully isolated, self-regulated and supervised DC/DC converter with input voltage 24-60 VDC and 90-250 VDC, having a ±20% input voltage tolerance.

48.4 Numerical module (NUM)

The CompactPCI numerical module is mainly used for processing and time tagging.

Each NUM can be electronically identified by its factory programmed serial number, article number, hardware version and final test date. Base and application software is stored in flash memory and is easily updated.

The module is equipped with IEEE P1386.1 (PCI Mezzanine Card) compliant sub-modules. Use the 100 Base-FX card, where optical Ethernet communication is required.

48.5 Communication interface module (CIM)

The CompactPCI communication interface module is used as:

- time synchronization master.
- carrier of the GPS receiver (GCM) module.

For time synchronization purposes, connect GCM to the CIM.

49 Application specific modules

49.1 General

This section gives an overview of the application specific modules available for RES 521. For in-depth information concerning design details, please contact ABB Automation Technology Products AB.

49.2 GPS clock module (GCM)

The built in GPS clock module decodes time information received from the global positioning system. The module is mounted on the communication interface module. Time information is further processed by NUM.

50 Hardware design

RES 521 follows the 6U Eurocard industry mechanical standard with a passive back-plane and a number of slots. The backplane supports two kinds of modules, standard CompactPCI modules and specific ABB Automation Technology Products AB modules based on the CAN bus.

All modules are designed for low power dissipation (no fans), EMC safety (both immunity and emission) and good environmental resistance. That gives high reliability and safe system also under disturbed and rugged conditions.

50.1 Hardware architecture

RES 521 consists of a number of different modules. These modules communicate through the internal PCI bus or the internal CAN bus. The PCI bus is used for modules which need extra high data transfer rate. Modules with low and medium data rate use the CAN bus.

The local HMI unit communicates directly with the NUM module through two serial channels. Remote HMI are connected via the Ethernet port.

50.2 Hardware modules

The basic configuration of RES 521 consist of the following modules:

- CBM, Combined Backplane Module. The backplane has 8 slots for CompactPCI modules and 4 slots for specific ABB Automation Products AB modules. One slot is designed for the power supply module.
- CEM, Combination Extension Backplane Module. The CEM is an addition to the CBM and is mounted on the CBM module. All communication with the RCAN based ABB printed circuit boards are handled inside this module.
- AIM, Analog Input Module. This is a CompactPCI module with 10 high performance analog input channels. The module consists of transformers, analog to digital converters and a signal processor. Main functions in the software are:
  - time tagging of all values
  - filtering and calibration adjustments of analog inputs
  - self supervision
- IOM, Input and Output Module. This module has serial communication to the main CPU through a CAN bus. It is a module with 8 optical isolated binary inputs and 12 relay outputs. Main functions in the software are:
  - time tagging of all events
  - filtering of binary inputs
  - self supervision

- NUM, Numerical Module. This is the main CPU module based on a high performance micro processor. It fits into the specific system slot in the backplane. The module may carry a mezzanine card, according to the PMC (PCI Mezzanine Card) standard, see the OEM module. The software system is running on a real time operating system. The main functions in the software are:
  - administration of the internal CompactPCI bus
  - administration of the internal CAN bus
  - supervision of all modules included in the rack
  - control error handling
  - control the I/O system
  - handle local HMI
  - handle remote HMI
  - RES 521 function execution
  - Galvanic Ethernet communication
- PSM, power supply module. DC/DC converter that support the electronics with +/-12V, +5V and +3,3V. The module can provide up to 50W. Supervision of all voltages are implemented. The module includes one relay output for the “Internal Fail“ signal.
- HMI, human machine interface. Local HMI panel located at the front of the RES 521 terminal.

50.2.1 Optional modules

- A mezzanine card for the NUM module, follows the PMC standard. Communication module with optical Ethernet type OEM. If the optical Ethernet option is chosen, the galvanic Ethernet can not be used.

51 Numerical module (NUM)

51.1 Hardware design

The NUM, NUmerical Module is a high performance, standard off-the-shelf compact-PCI CPU module. It uses the 6U-format on the board and takes one slot in width.

For communication with high speed modules, e.g. analog input modules and high speed serial interfaces, the NUM is equipped with a Compact PCI bus. The NUM is the compact PCI system card, i.e. it controls bus mastering, clock distribution and receives interrupts.

The NUM has an Ethernet 10 Base T/100 Base Tx port with RJ-45 contact.

NUM is equipped with a PMC slot (32-bit IEEE P1386.1 compliant) in which as an option, a daughter card may be mounted, e.g. 100 Base-FX optical Ethernet.

To reduce bus loading of the compactPCI bus in the backplane the NUM has one internal PCI bus for internal recourses and the PMC slot and external PCI accesses through the backplane are buffered in a PCI/PCI bridge. If this division of the bus was not done there could not be eight slots on the bus since the CompactPCI standard only allows eight loads.

The application code and configuration data is stored in flash memory using a flash file system. During power up the application code is moved to and then executed from the DRAM. The code is stored in the flash memory because its nonvolatile and executed in DRAM because of the DRAMs higher performance.

The NUM is equipped with a real time clock. It uses a battery for power backup of the real time clock and this battery has to be changed on regular bases, e.g. 5 years. This is only necessary when no time synchronization is used.

All the communication not possible with a standard CPU-module is, added on the CEM.

No fans are needed on this standard module since the power dissipation is low.

51.2 Technical specifications

The NUM conforms to the CompactPCI Specification revision 2.0.

Take care when using PMC modules as to how much current they require, especially from the +5V supply.

51.3 Block diagram

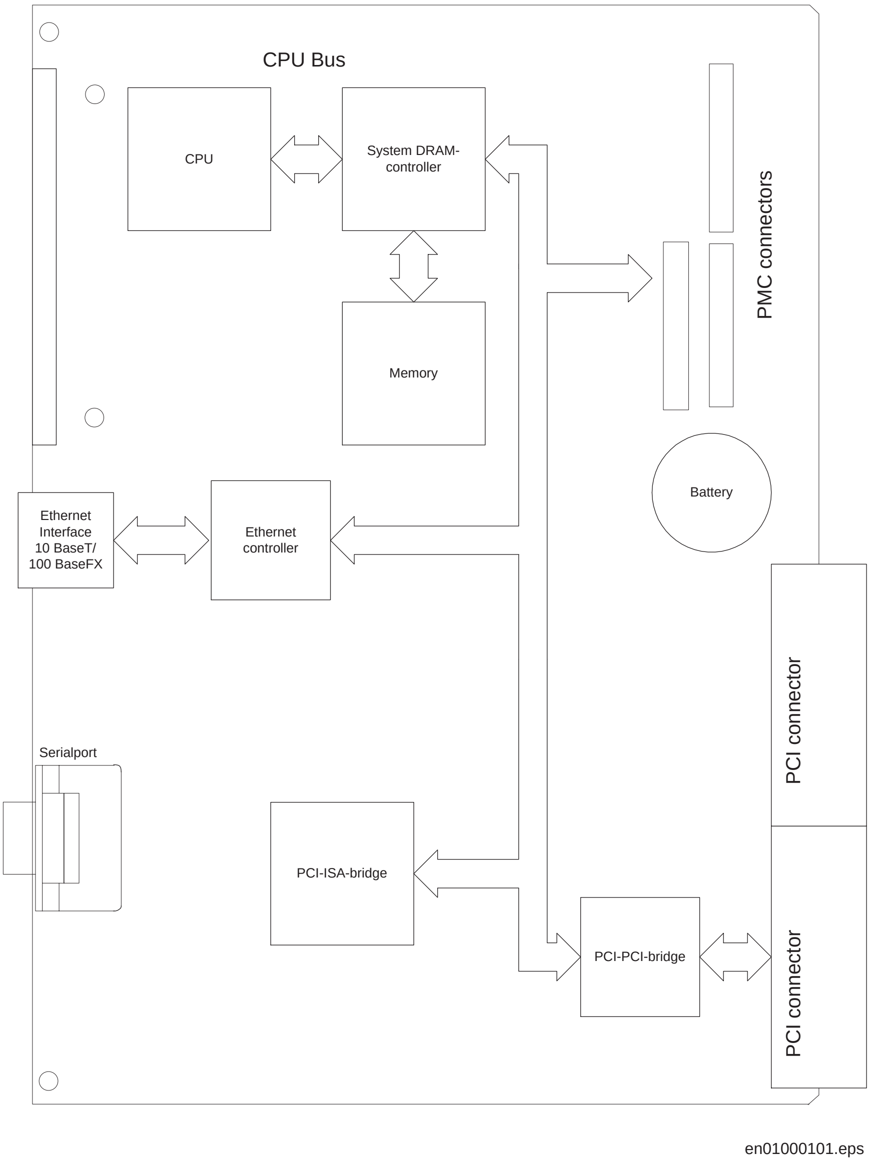


Figure 42: Numerical Module block diagram (actual placement of components differ).

52 Optical Ethernet module (OEM)

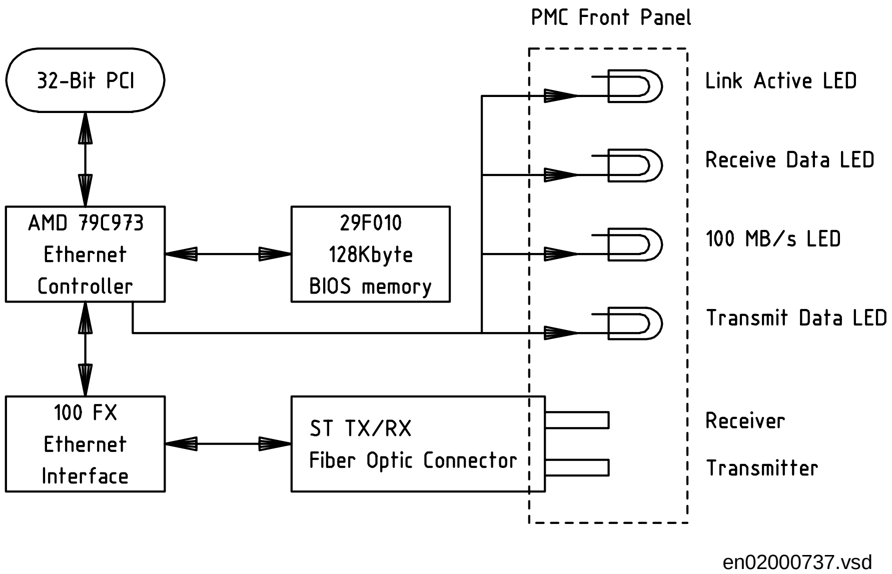


Figure 43: Optical Ethernet module block diagram (actual placement of components differ).

The Optical Ethernet Module (OEM) provides a single port 100BASE-FX Ethernet connection using Fiber Optic media.

The Fiber Optic connectors used on the board are of "ST RT/TX" style. To interconnect with 100BASE-FX equipment with other style of connectors, use adaptor fiber cables, e.g. ST to SC.

Four green activity and status LEDs are visible from the PMC front panel. They indicate Link active, receive data, 100 MB/s and transmit data.

The optical wavelength supported in this design is between 1270 and 1380 nm and is compatible with standard multi-mode fiber as used in FX applications (62.5/125µm). The max fiber length is 2 km.

As the RES 521 is running TCP/IP it is possible to use standard networking equipment for long distance connections, E.g. LAN-WAN gateways or bridges.

The choice of network equipment depends on available networking infrastructure and other circumstances as geography. As 100BASE-FX is easy to convert to 100BASE-TX with a media converter or a switch, it is easy to find equipment on the open market.

Example:

You want to use a serial link between the substation and the operators central.

You have a multiplexed fiber available with G.703 interface. In the substation you need a Router with one Ethernet port and one serial port. The serial port interface must match the serial link, here G.703. The Ethernet port could be of the following types 100BASE-FX, 100BASE-TX or 10BASE-T. If the Ethernet port is of other type than 100BASE-FX a media converter or switch is needed. If you also want a local IEEE 1344 client in the substation you need a switch anyway. If there are more than one RES 521 in the substation they can share one WAN connection, by using an Ethernet switch.

In the operators central you also need a Router between Ethernet and G.703, to convert the serial link back to Ethernet to interface the data concentrator.

Example of equipment:

Switch:

OnTime Networks FSU208 (www.ontimenet.com)

Media converter:

D-Link DMC-300SC (www.dlink.co.uk)

Router:

Cisco 1721 with WIC-1T (WAN Interface Card) (www.cisco.com)

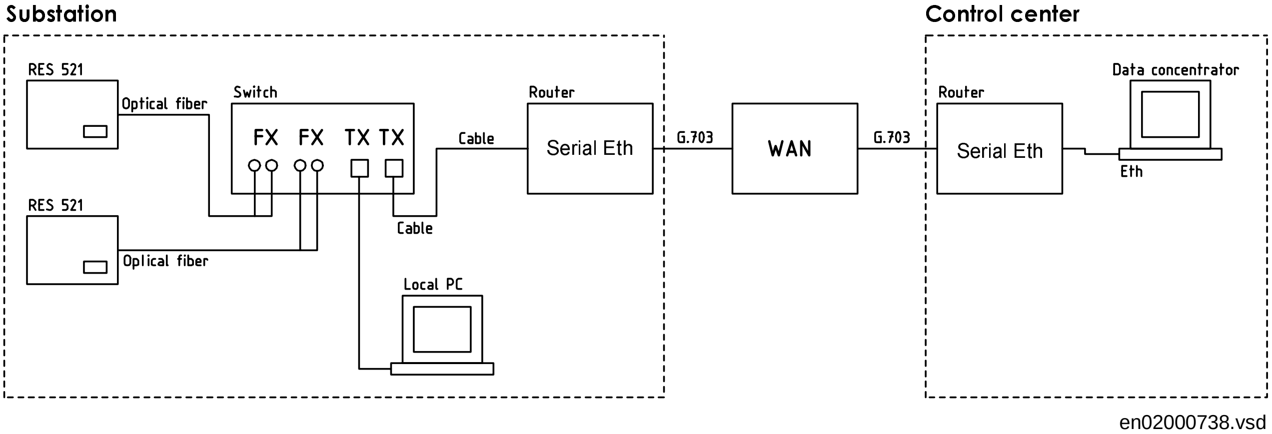


Figure 44: Example configuration of long-distance connection between RES 521 and the control center.

53 Compact backplane module (CBM)

53.1 Hardware design

CBM is a backplane that has 8 CompactPCI connectors and 4 connectors for RCAN based ABB boards. One of the CompactPCI connectors has a special use since it hosts the CEM and is therefore mounted on the opposite side of the backplane. For the compact PCI slots a 220pin 2mm Hard Metric connector is used. The RCAN based ABB boards uses a 3 row, 96 pin standard Euro-connector. There is a need for some signals to be present in both connector types. For this purpose some of the User defined parts of the CompactPCI connector are used.

The CompactPCI specification gives the possibility for a 3.3V OR 5V signaling in the backplane. The CBM backplane and connected modules must be 5V PCI-compatible.

Some pins on the CompactPCI connector are connected to the RCAN bus, to be able to communicate with RCAN based modules.

For identification in production and field upgrades the CBM is equipped with two IDchips with the contents of a factory programmed unique serial number and during production it is programmed with article number, hardware version and final test date. One ID contains backplane data and the other contains product data.

For the power supply there is a 3 row, 96 pin, Euro-connector.

For power degradation early warning there is a signal, ACFail.

If a modules selftest discovers an error it informs other modules through the Internal Fail signal.

53.2 Technical specifications

Table 58: Mounted connectors

Function	Connector identifier
Compact PCI	X1-8 (where X2 is mounted on the opposite side for CEM)
RCAN based	X9-12
Power supply	X14
HMI connector	X30

Table 59: The buses in the backplane are connected to the following connectors

Bus	Connectors
Compact PCI	X1-8 (X8 according to v2.1 where no user pins are used, rest is according to v1.0 of the CompactCPI-standard)
RCAN	X1-7,9-12,14
HMI display and keyboard interface	X1-7,9-12
HMI optical communication interface	X1-7,9-12

Table 60: Special signals

Signal	Description	Connector
PRST	System reset	X1-7,9-12,14
AC_FAIL_N	Power supply degradation early warning	X1-7,9-12,14
INTERNAL_FAIL_N	Module failure broadcast signal	X1-7,9-12,14
PPS, MPPS, CMPPS	Timesyncronisation	X1-7,9-12,14
SYS_ID	Electronic ID	X1-7,9-12,14

Impedance matching: Every signal is impedance matched to 65 Ohm +/-10%, calculated for a bare PCB.

53.3 Block diagram

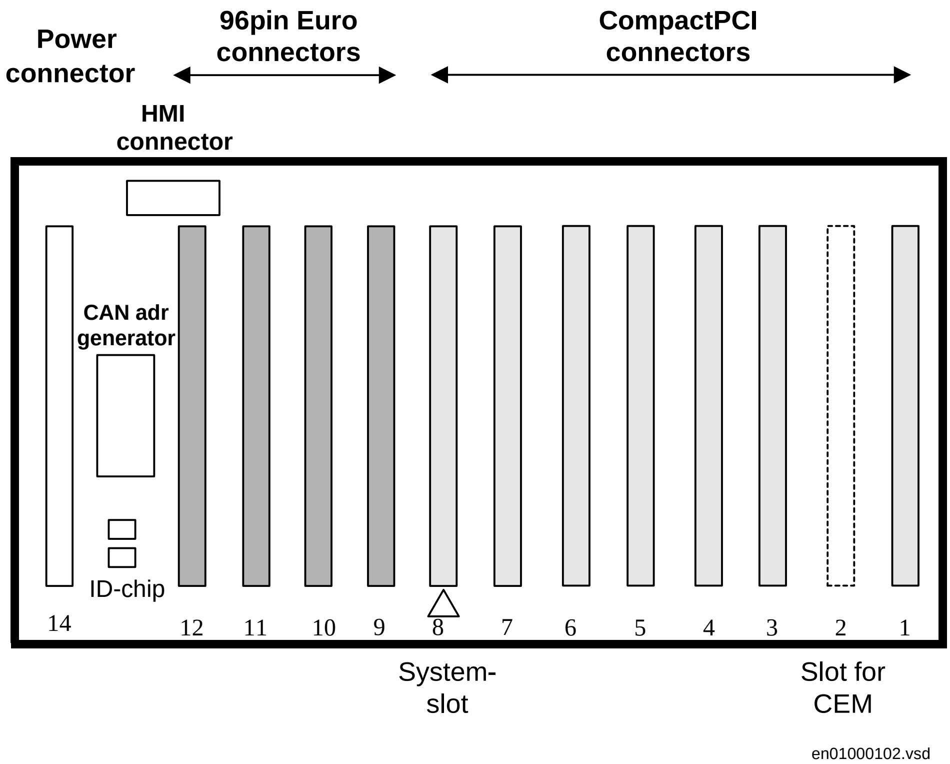


Figure 45: Connectors on the backplane as seen from the connector side.

54 Combination extension backplane module (CEM)

54.1 Hardware design

CEM is an addition to the CBM and it is mounted on the CompactPCI-connector X2 placed on the opposite side of the CBM. For the compact PCI slot a 220pin 2mm Hard Metric connector is used. All communication between the RCAN based ABB boards are handled inside the CEM.

There are also two asynchronous serial ports. One for the HMI-display and keyboard and one for the HMI optical interface.

For identification in production and field upgrades the CEM is equipped with two IDchips with the contents of a factory programmed unique serial number and during production it is programmed with article number, hardware version and final test date. One ID contains CEM data and the other contains the data about the standard CPU-module, NUM. It also handles the common ID-signal SYS_ID in the same way.

The CEM also handles the power degradation early warning signal, ACFail, and present this as an interrupt to the CPU-module.

If a modules selftest discovers an error it informs other modules through the Internal Fail signal. Since there is no direct connection to the CPU-module the CEM also handles this signal.

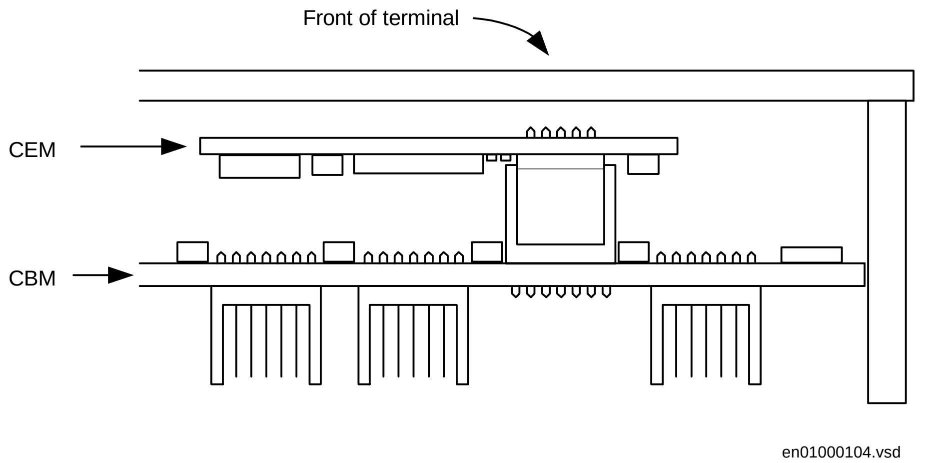


Figure 46: CBM and CEM seen from the top of the terminal.

54.2 Technical specifications

CEM uses the CompactPCI specification revision 1.0 where user pins are available.

Table 61: Resources

Function	Description
Serial I/O	HMI display and keyboard interface
Serial I/O	HMI optical communication interface
RCAN interface	Communication with all RCAN based modules on the backplane, CBM.
ID chips	Handling of the three ID-signals.

Table 62: Special signals

Signal	Description
PRST	System reset
AC_FAIL_N	Power supply degradation early warning
INTERNAL_FAIL_N	Module failure broadcast signal

Table 62: Special signals

Signal	Description
SYS_ID	Electronic ID
RCAN_ID	Rack information ID. Slot numbers

54.3 Block diagram

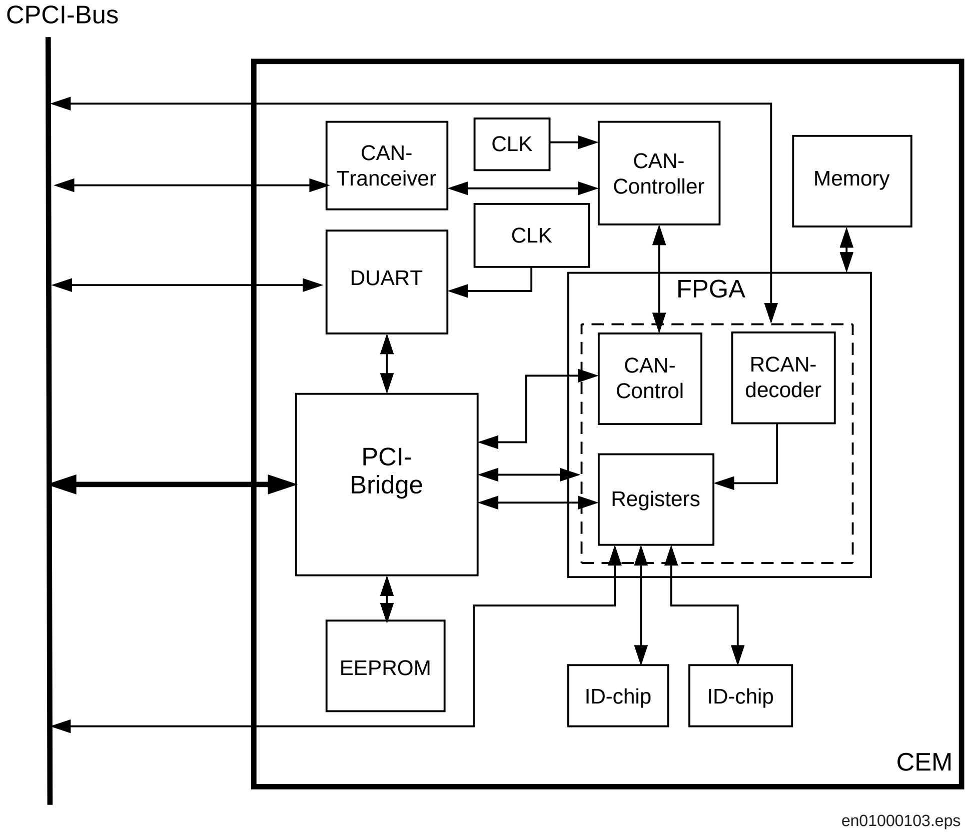


Figure 47: CEM block diagram.

55 Power supply module (PSM)

55.1 Hardware design

The power supply module contains a built-in, self-regulated DC/DC converter that provides full insulation between the terminal and the external battery system.

The PSM, converts a DC input voltage range either from 24 to 60 V or from 110 to 250 V, including a ±20% tolerance on the EL voltage.

The output voltages are +3.3, +5, +12 and -12 Volt and the module can provide 50W.

55.2 Block diagram

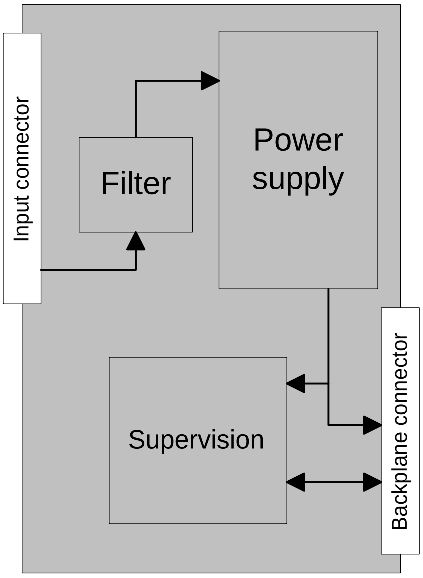


Figure 48: Block diagram for the PSM.

56 Analog input module (AIM)

56.1 Hardware design

The analog input module (AIM) consists of two connectors for the external connections and two printed board assemblies; transformer board and A/D board.

Current and voltage input transformers are mounted on the transformer board. The transformers form an insulating barrier between the external wiring and the A/D-conversion board, and adapt the values of the measuring quantities to the input circuits of the A/D-conversion board. Maximum ten transformers can be mounted on the transformer board. The design is made for mounting of either a current transformer or a voltage transformer in each of the transformer locations.

The other printed board assembly is the A/D-conversion board. The signals from the transformer board are transmitted to input channels of the A/D board over a contact socket strip on the transformer board inside the AIM to a contact pin strip on the A/D board. The A/D conversion board is mainly filtering and converting analog to digital signals. The transmission of data between the A/D board and the numerical module is done via the backplane board with the CompactPCI bus. The A/D board has ten measuring channels. The channels are equipped for current measuring alternatively voltage measuring.

The printed circuit board assemblies and the external connectors are attached with screws to a common mounting plate. The primary windings of the transformers are connected to the external connectors with cables.

The analog input module is provided with components for time-synchronization. The time-synchronization components are located on the A/D board. An external synchronization pulse from a synchronization device will be used to get the same time everywhere in the system.

56.2 Technical specifications

56.2.1 Transformer board

Toroidal type of transformers are used as current input transformers and EI 38 type of transformers are used as voltage input transformers. The current transformers have primary windings for both 1A and 5A rated current. The voltage transformers are covering a rated range from 57.7V to 120V. The process interface of the external connector has screw terminals for maximum one conductor with the area $4mm^2$ alternatively two conductors with the area 2.5 mm^2, or optionally, ring lug connections area 3.3 mm^2.

56.2.2 A/D-conversion board

The signals from the transformer board are amplified and filtered with a bandwidth of 10kHz on two ranges for each channel and converted with a resolution of 12 bits. The results, from the conversion on the two ranges, are combined into a single 24bit word and filtered in two cascaded decimation filters programmed into a digital signal processor (DSP).

The numerical filters are of finite impulse response type, giving a linear phase response and appropriate anti aliasing with a cut-off at 2300/2760Hz and 500/600Hz respectively, at 50/60 Hz rated frequency.

High accuracy is obtained by a factory made calibration process. Internal supervision of all vital functions is implemented.

56.3 Block diagram for the A/D-conversion board

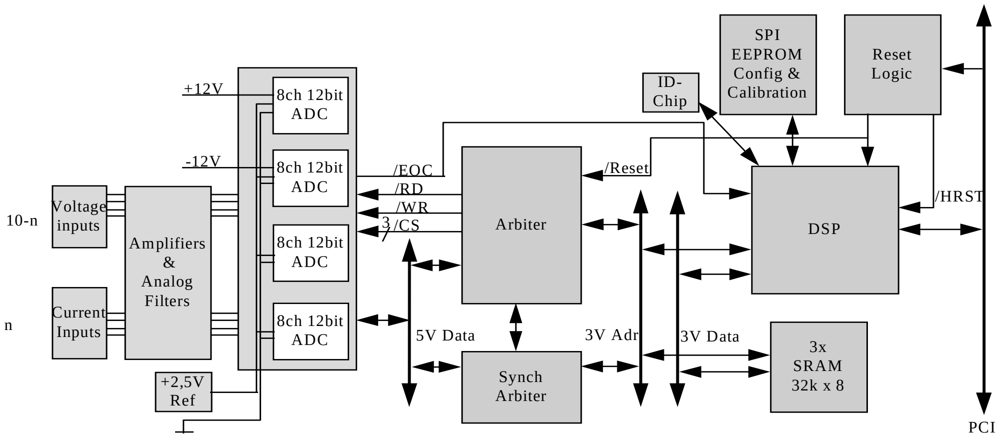


Figure 49: Block diagram of the Analog Input Module (AIM).

57 Binary in/out module (IOM)

57.1 Hardware design

The Binary in/out module contains eight optical isolated binary inputs and twelve binary output contacts. Ten of the output relays have contacts with a high-switching capacity (Trip and signal relays). The remaining two relays are of reed type and for signalling purpose only. The relays are grouped together as can be seen in the terminal diagram.

In RES 521*1.0, only port 01, 02, 04 and 05 are used.

57.2 Block diagram

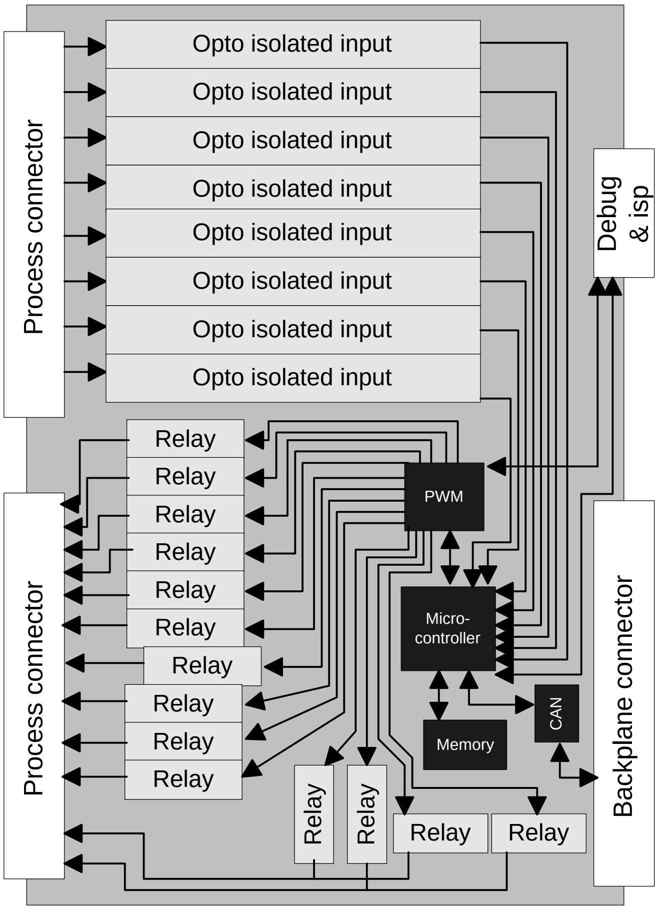


Figure 50: Block diagram for the binary input/output module.

Chapter 9 Technical data

This chapter lists the technical specifications of RES 521*1.0.

58 General technical data

This section lists technical data valid in all terminal configurations and variants

Table 63: Energizing quantities, rated values and limits

Quantity	Rated value	Nominal range	Operative range
Current Burden	I_r = 1 A or 5 A < 0,25 VA at I_r	(0.2-30) x I_r (0.2-4) x I_r continuously	(0.03 - 100 x I_r) 100 x I_r for 1 s*
AC voltage Ph-Ph** Burden	U_r = 100/110/115/120 V < 0.2 VA at U_r	80-120% of U_r	1.5 x U_r continuously 2.5 x U_r for 1 s
Frequency	f_r = 50/60 Hz	±2.5 Hz/±3.0 Hz	±5 Hz/± 6 Hz
Auxiliary DC voltage EL Power consumption (Terminal equipped with all IO-modules) Auxiliary DC power in-rush Binary input (8) /output (12) module	EL = 24-60 V EL = 90-250 V < 35 W 220 VDC, <30 A, 0.1 ms 110 VDC, <15 A, 0.1 ms 48 VDC, < 15 A, 0.1 ms 24 VDC, < 10 A, 0.1 ms	±20% ±20%	±20% ±20%
DC voltage RL power consumption each I/O board each output relay RL24 = 24/30 V RL48 = 48/60 V RL110 = 110/125 V RL220 = 220/250 V	RL24 = 24/30 V RL48 = 48/60 V RL110 = 110/125 V RL220 = 220/250 V ≤ 1 W ≤ 0.15 W max. 0.05 W/input max. 0.1 W/input max. 0.2 W/input max. 0.4 W/input	±20% ±20% ±20% ±20%	±20% ±20% ±20% ±20%

Table 63: Energizing quantities, rated values and limits

Quantity	Rated value	Nominal range	Operative range
Ambient temperature	20°C	-5°C to +55°C	-10°C to +55°C
Ripple in dc auxiliary voltage	max. 2%	max. 12%	Full wave rectified
Relative humidity	10-90%	10-90%	0-95%

* Max 350 A for 1 s when COMBIFLEX test switch is used

** Ph-ph voltage may also be directly connected across the analog voltage inputs

Table 64: Influencing factors, permissible influence

Dependence on	Within nominal range	Influence
Ambient temperature	-10 °C to +55°C	0.01%/ °C
Auxiliary DC voltage	(110-250) Vdc ±20%	0.01% / %
Ripple in auxiliary DC voltage	12% of EL	0.01% / %
Interruption in auxiliary DC voltage without resetting no unwanted function	(110-250) Vdc ±20%	 < 50 ms 0 - ∞

Table 65: Electromagnetic compatibility (EMC), immunity tests[1]

Test	Type test values	Reference standards
1 MHz burst disturbance	2.5 kV	IEC 60255-22-1, Class III
Electrostatic discharge Direct application Indirect application	 15 kV, air discharge 8 kV, contact discharge 6 kV, contact discharge	 IEC 60255-22-2, Class IV IEC 61000-4-2, Class III
Fast transient disturbance	4 kV	IEC 60255-22-4, Class IV
Surge immunity test	1-2 kV, 1.2/50 µs, high energy	IEC 61255-22-5
Power frequency immunity test	150-300 V, 50 Hz	IEC 60255-22-7, Class A
Power frequency magnetic field test	1000 A/m, 3 sec	IEC 61000-4-8, Class V
Radiated electromagnetic field disturbance	10 V/m (25-1000) MHz	IEC 61000-4-3 IEEE/ANSI C37.90.2
Radiated electromagnetic field disturbance GSM	10 V/m, 1.4-2.0 GHz, 900 MHz, 1890 MHz	EN 61000-4-3
Conducted electromagnetic field disturbance	10 V/m (0.15-80) MHz	IEC 61000-4-6, level 3

1) The galvanic ethernet communication port (RJ-45) follows the IEEE Standard 802.3™-2002 physical specification in part 3.

Table 66: Electromagnetic compatibility (EMC), emission tests[1]

Test	Type test values	Reference standards
Electromagnetic emission, radiated	30-1000 MHz, class A	EN 55011
Electromagnetic emission, conducted	0,15-30 MHz, class A	EN 50081-2 (Informative annex)

Table 67: Insulation[1]

Test	Type test values	Reference standards
Dielectric test	2.0 kV ac 1 min	IEC 60255-5
Impulse voltage test	5 kV, 1.2/50 μs, 0.5 J	IEC 60255-5
Insulation resistance	> 100 Mohm at 500 V dc	IEC 60255-5

Table 68: CE-mark

Test	According to
Immunity	EN 50082-2
Emissivity	EN 50081-2
Low voltage directive[a]	EN 50178

a) Ring-lug option does not fully comply with EN 50178

Table 69: Mechanical tests

Test	According to	Reference standards
Vibration	Class I	IEC 60255-21-1
Shock and bump	Class I	IEC 60255-21-2
Seismic	Class I	IEC 60255-21-3

1) The galvanic ethernet communication port (RJ-45) follows the IEEE Standard 802.3TM-2002 physical specification in part 3

Table 70: Contact data (reference standard: IEC 60255)

Function or quantity	Trip- and signal relays	Fast signal relays (parallel reed relay)
Max. system voltage	250 V ac, dc	250 V ac, dc
Test voltage across open contact, 1 min	1,0 kV rms	800 V, dc
Current carrying capacity continuous 1 s	 8 A 10 A	 8 A 10 A
Making capacity at inductive load with L/R > 10 ms 0,2 s 1,0 s	 30 A 10 A	 0,4 A 0,4 A
Breaking capacity for ac, cosφ > 0,4	250 V/8,0 A	250 V/8,0 A
Breaking capacity for dc with L/R < 40 ms	48 V/1 A 110 V/0,4 A 220 V/0,2 A 250 V/0,15 A	48 V/1 A 110 V/0,4 A 220 V/0,2 A 250 V/0,15 A
Maximum capacitive load		10 nF

Table 71: Connection system

Connector type	Rated voltage	Maximum wire cross section area	Maximum load continuous	Maximum load 1 s
Binary input/ output module voltage compression type of screen connection	250 V AC	2,5 mm^2 2 x 1 mm^2	10 A	30 A
Analog input module voltage/ current compression type of screen connection	250 V AC	4 mm^2	20 A	500 A
Voltage Ring Lugs	250 V AC	5.3 mm^2	10 A	30 A
Current Ring Lugs	250 V AC	5.3 mm^2	20 A	500 A
Fiber connectors	Glass: Bayonet ST Plastic: Snap in Simplex Latching			

Table 72: Additional general data

Weight approximate	**<18 kg**
Dimensions	
Width	448 mm
Height	267 mm
Depth	245 mm
Water and dust protection level	Front IP 40 (IP 54 with sealing strip)
	Sides IP 30
	Back IP 20
Storage temperature	-40°C to +70°C

59 RES 521*1.0 specific technical data

This section lists technical data valid for this specific product in all configurations and variants.

Table 73: GPS Antenna and cablel

Function	Value
Max antenna cable attenuation	26 dB @ 1.6 GHz
Antenna cable impedance	50 ohm
Lightning protection	Must be provided externally
Antenna cable connector	SMA

Table 74: Accuracy

Specification	Value
Receiver accuracy	±1 µs relative UTC

Table 75: Service values for input quantities

Function	Nominal range	Accuracy
Frequency	(0.7 -1.2) x fr	± 5 mHz at three phase connection
Rate of change of frequency	5 Hz/s	
Current	(0.1 - 4.0) x Ir	± 0.1%
Voltage	(0.1 - 1.5) x Ur	± 0.1%
Angles	0.0° - 359.9°	± 0.1°

Table 76: triggFreq

Quantity	Parameter	Range and step
Enable under-frequency trigger.	enableUnder	0,1 with step 1
Enable over-frequency trigger.	enableOver	0,1 with step 1
Limit under-frequency trigger, in Hz.	limitUnder	30.000-75.000 with step 0.001
Limit over-frequency trigger, in Hz.	limitOver	30.000-75.000 with step 0.001
Pick-up time delay under-frequency trigger, in ms.	tDelayUnder	100-999999 with step 1
Pick-up time delay over-frequency trigger, in ms.	tDelayOver	100-999999 with step 1
Relative value for hysteresis, in % of the limit.[a]	hystRel	0.0-100.0 with step 0.1
Absolute value for hysteresis, in Hz.[b]	hystAbs	0.000-100.000 with step 0.001

a) Hysteresis set as % of the limit, e.g. setting 10 means 10% of the limit.
b) Hysteresis set as an addition value to the limit.

Table 77: triggDFreq

Quantity	Parameter	Range and step
Enable rate of change of under-frequency trigger.	enableUnder	0,1 with step 1
Enable rate of change of over-frequency trigger.	enableOver	0,1 with step 1
Limit rate of change of under-frequency trigger, in Hz/s	limitUnder	-100.000-0.000 with step 0.001
Limit rate of change of over-frequency trigger, in Hz/s	limitOver	0.000-100.000 with step 0.001
Pick-up time rate of change of delay under-frequency trigger, in ms.	tDelayUnder	100-999999 with step 1
Pick-up time delay rate of change of over-frequency trigger, in ms.	tDelayOver	100-999999 with step 1
Relative value for hysteresis, in % of the limit.[a]	hystRel	0.0-100.0 with step 0.1
Absolute value for hysteresis, in Hz/s.[b]	hystAbs	0.000-100.000 with step 0.001

a) Hysteresis set as % of the limit, e.g. setting 10 means 10% of the limit.
b) Hysteresis set as an addition value to the limit.

Table 78: triggOC4ch

Quantity	Parameter	Range and step
Enable over-current trigger phasor 1.	enableCh1	0,1 with step 1
Enable over-current trigger phasor 2.	enableCh2	0,1 with step 1
Enable over-current trigger phasor 3.	enableCh3	0,1 with step 1
Enable over-current trigger phasor 4.	enableCh4	0,1 with step 1
Limit over-current trigger, in A phasor 1.	limitCh1	0-50000 with step 1
Limit over-current trigger, in A phasor 2.	limitCh2	0-50000 with step 1
Limit over-current trigger, in A phasor 3.	limitCh3	0-50000 with step 1
Limit over-current trigger, in A phasor 4.	limitCh4	0-50000 with step 1
Pick-up time delay over-current trigger, in ms phasor 1.	tDelayCh1	100-999999 with step 1
Pick-up time delay over-current trigger, in ms phasor 2.	tDelayCh2	100-999999 with step 1
Pick-up time delay over-current trigger, in ms phasor 3.	tDelayCh3	100-999999 with step 1
Pick-up time delay over-current trigger, in ms phasor 4.	tDelayCh4	100-999999 with step 1
Relative value for hysteresis, in % of the limit.[a]	hystRel	0.0-100.0 with step 0.1
Absolute value for hysteresis, in A.[b]	hystAbs	0-50000 with step 1

a) Hysteresis set as % of the limit, e.g. setting 10 means 10% of the limit.
b) Hysteresis set as an addition value to the limit.

Table 79: triggUV2ch

Quantity under voltage	Parameter	Range and step
Enable under-voltage trigger phasor 1.	enableCh	0,1 with step 1
Enable under-voltage trigger phasor 2.	enableCh2	0,1 with step 1
Limit under-voltage trigger, in V phasor 1.	limitCh1	0-1000000 with step 1
Limit under-voltage trigger, in V phasor 2.	limitCh2	0-1000000 with step 1
Pick-up time delay under-voltage trigger, in ms phasor 1.	tDelayCh1	100-999999 with step 1
Pick-up time delay under-voltage trigger, in ms phasor 2.	tDelayCh2	100-999999 with step 1
Relative value for hysteresis,in % of the limit.[a]	hystRel	0.0-100.0 with step 0.1
Absolute value for hysteresis, in V.[b]	hystAbs	0-1000000 with step 1

a) Hysteresis set as % of the limit, e.g. setting 10 means 10% of the limit.
b) Hysteresis set as an addition value to the limit.

Table 80: Synchronizing signals (GPS)

Function	Accuracy
GPS	± 0.5 µs

Table 81: Sampling/storing/sending rate for phasor and system quantities

Function	Setting
Transfer rate, based on 50 or 60 Hz power system frequency	once per cycle, once per 2 cycles, once per 4 cycles

Table 82: Startup performance

Condition	Value
Time to reliable time reference with antenna in new position or after power loss longer than 1 month	less than 30 minutes
Time to reliable time reference after a power loss longer than 48 hours	less than 15 minutes
Time to reliable time reference after a power loss shorter than 48 hours	less than 5 minutes

59.1 Communication

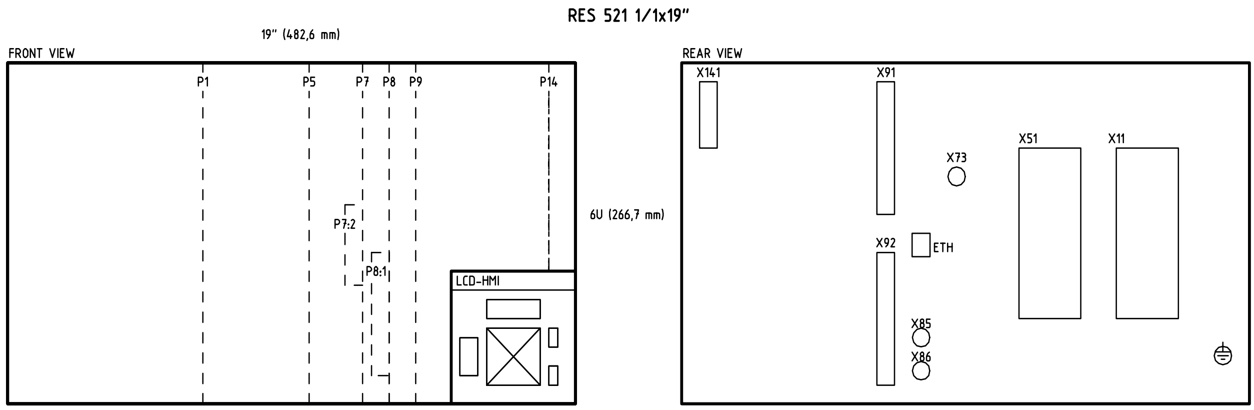
Table 83: Optical Ethernet

Function	Value
Applicable standard	IEEE 802.3u 100BASE-FX
Communication speed	100/200 Mbps for half/full-duplex
Connectors	ST RX/TX Style connectors
Cable	62.5/125 µm multi-mode fiber optic cable up to 2 km (glass)
Optical wavelength	1270-1380 µm
LED Indicators	Link Active, Receive Data, 100 MB/s, Transmit Data

Table 84: Galvanic Ethernet

Function	Value
Applicable standards	IEEE802.3 10BASE-T IEEE802.3u 100BASE-TX
Communication speed	10/20 Mbps for half/full-duplex 100/200 Mbps for half/full-duplex
Connector	RJ-45
Cable	10BASE-T 2-Pair UTP Cat. 3, 4, 5 up to 100m 100BASE-TX 2-Pair UTP Cat 5 up to 100m

Chapter 10 Terminal diagrams



LOCATION	QTY OF CURRENTS/VOLTAGES			RATED FREQUENCY,fr	RATED VOLTAGE,Ur	RATED CURRENT,Ir
	ANALOGUE INPUT MODULE					
	7I+3U	8I+2U	9I+1U			
P1	X	–	–	50Hz / 60Hz	100,100/√3,110,110/√3 115,115/√3,120,120/√3	1A / 5A RECONNECTABLE
P5		–	–			

LOCATION	BINARY IN/OUT MODULE AUXILIARY VOLTAGE (DC)			
	RL24	RL48	RL110	RL220
	24/30V	48/60V	110/125V	220/250V
P9				

DESIGNATION CORRESPONDING TO CASING		
MODULE	FRONT	REAR
AIM	P1	X11
AIM	P5	X51
CIM	P7	-
GCM	P7:2	X73
NUM	P8	ETH
OEM	P8:1	X85-86
IOM	P9	X91,92
PSM	P14	X141

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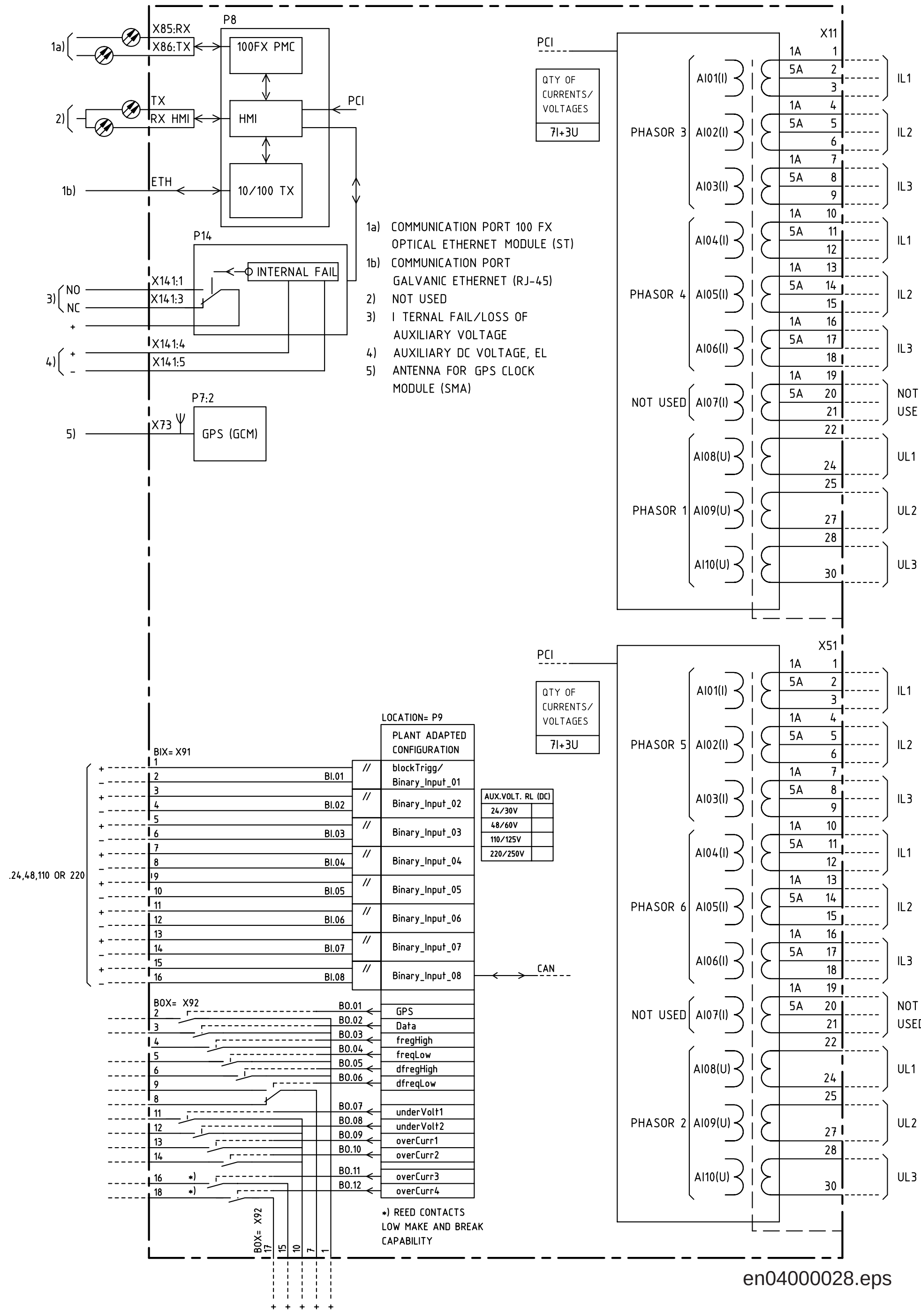

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Chapter 11 Configuration

60 RES 521 standard configuration

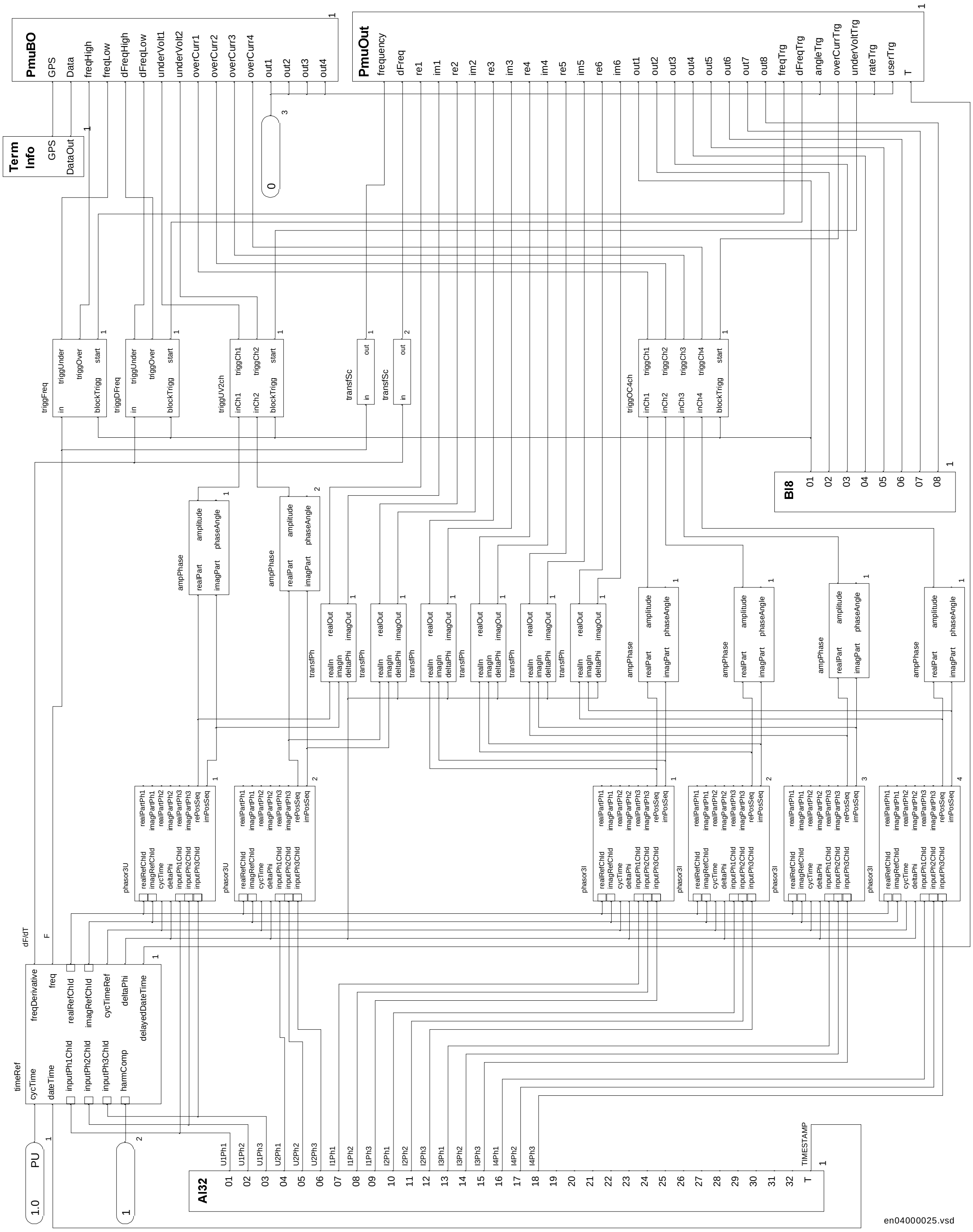

Figure 51: RES 521 configuration, 2 analog input modules

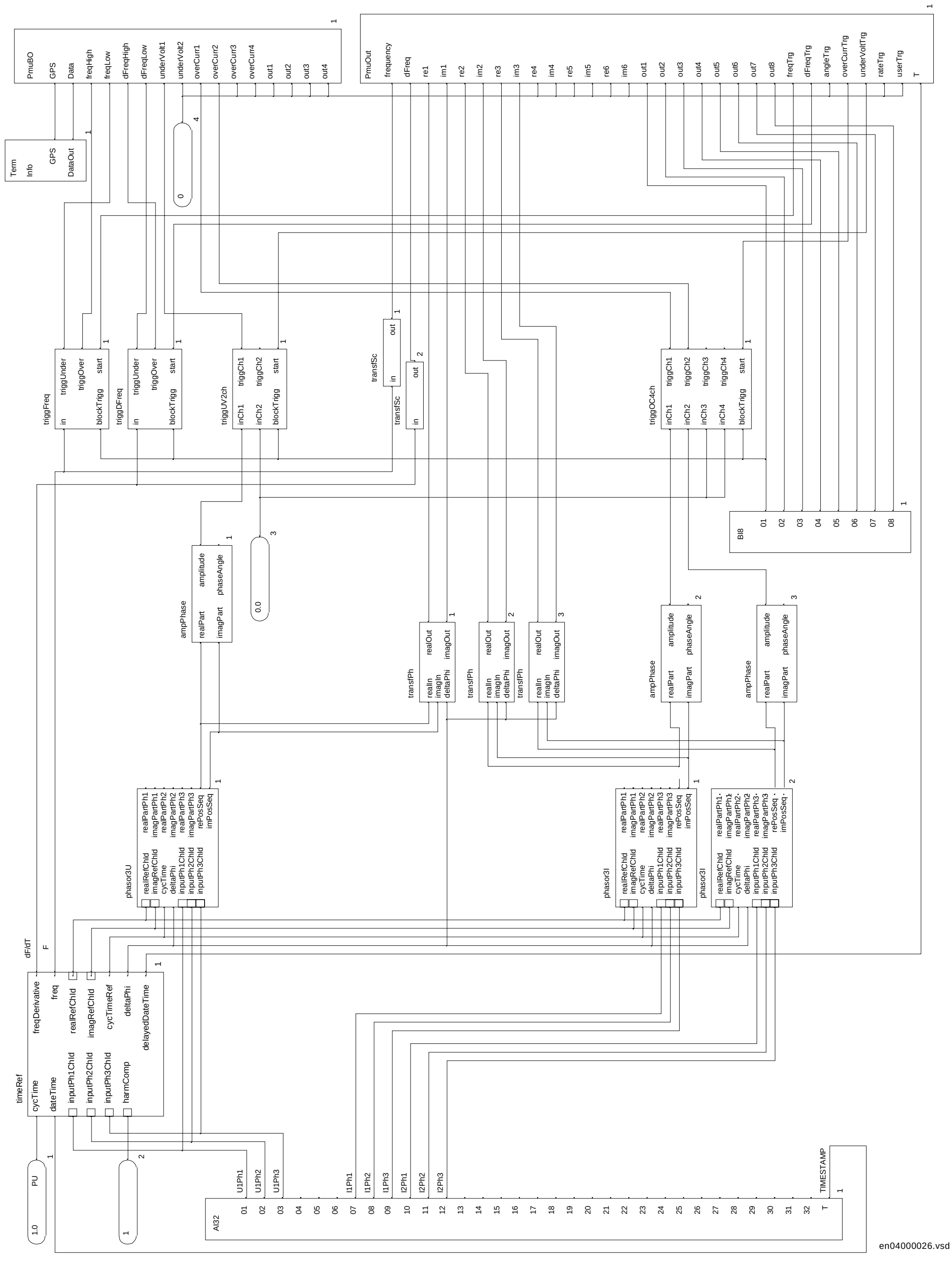

Figure 52: R*ES 521 configuration, 1 analog input module*

These are the standard PMU configurations. Depending on ordered numbers of analog input modules (1 AIM or 2 AIM), one of these configurations is downloaded into the terminal in the factory.

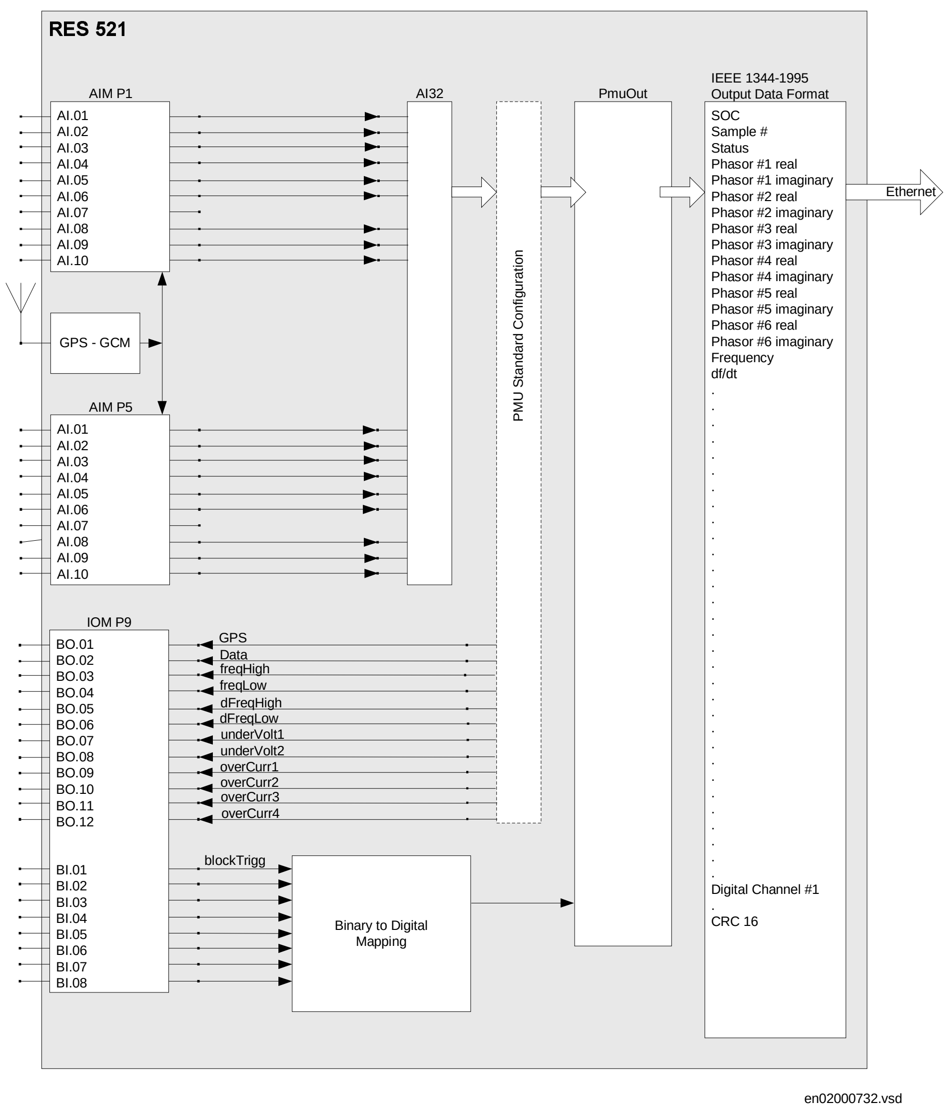

Figure 53: RES 521 inputs and output, and how they are related to the configuration.

In figure 53 it is shown how the physical analog inputs and binary inputs are related to the configuration, the IEEE 1344-1995 synchrophasor data format and the output on the Ethernet connection. The binary inputs are mapped to the synchrophasor format digital channel data #1 (the 8 binary inputs are mapped to one byte), and the trigger levels are connected to the binary outputs. The function block AI32 is the interface between the analog inputs, phase quantities and GPS signal, and the configuration. The function block PmuOut is the interface between the configuration and the synchrophasor format.

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ABB Automation Technologies AB
Substation Automation
SA Support Line
SE-721 59 Västerås
Sweden

By facsimile:

Send to + 46 21 14 69 18

ABB Automation Technology Products AB
Control and Force Measurement
Substation Automation
SE-721 59 Västerås
Sweden
Telephone: +46 (0) 21 34 20 00
Facsimile: +46 (0) 21 14 69 18
Internet: www.abb.com/substationautomation

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