A140 CURRENT SENSOR

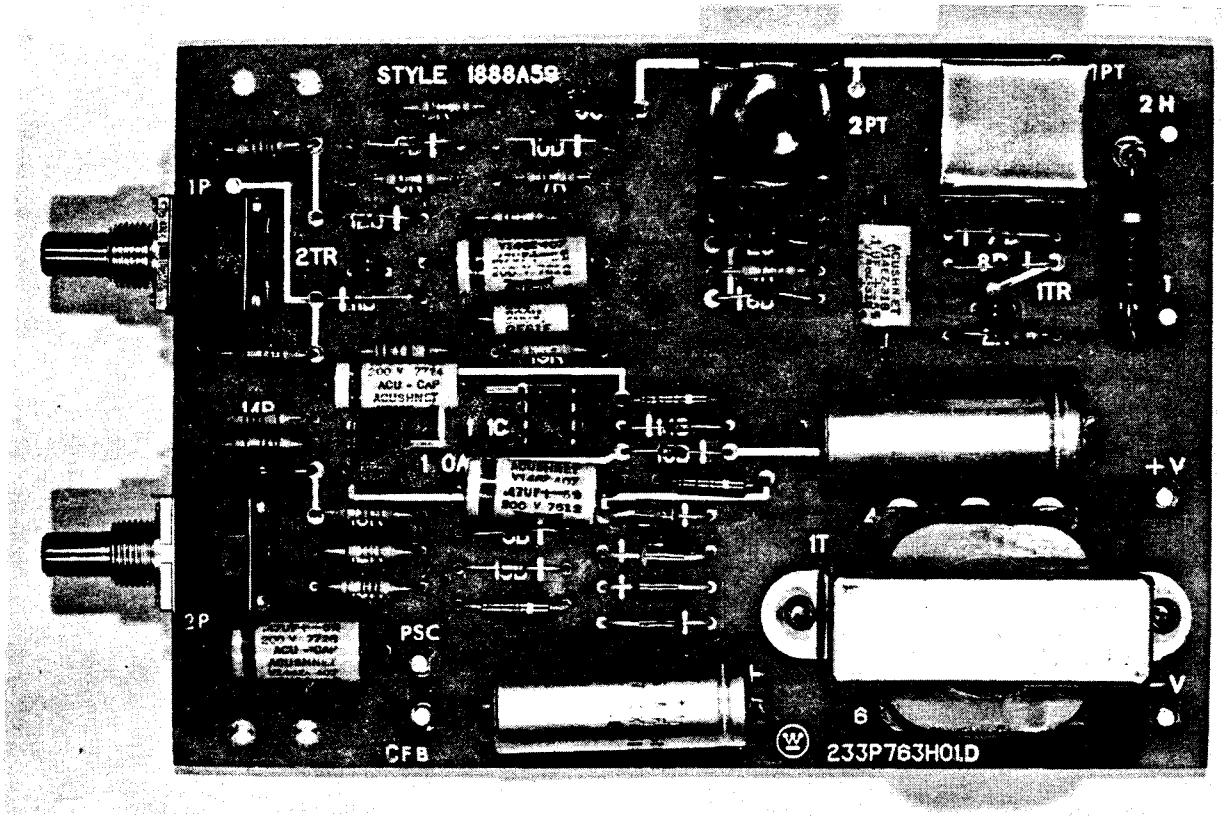
I. INTRODUCTION

The A140 Current Sensor S#1888A75 is designed to isolate and amplify the millivolt signal of a current shunt. The module contains printed circuit board S#1888A59. External connections to the unit are made via two terminal blocks located on the module faceplate. Millivolt inputs are connected to terminals 1 and 2H for the upper gain range or 1 and 2L for the lower gain range. Output is available between terminals CFB and PSC. Gain and offset balance adjustments may be made using the appropriately labeled pots secured to the faceplate.

Three sensor group options are available. Selection is dependent on drift and power supply requirements. G01 employs a standard 741 operational amplifier and receives 115 VAC power via terminals +V and -V. G02 features a special low-drift op amp and 115 VAC power. G03 employs a 741 op amp and receives ±24 VDC power via terminals +V and -V.

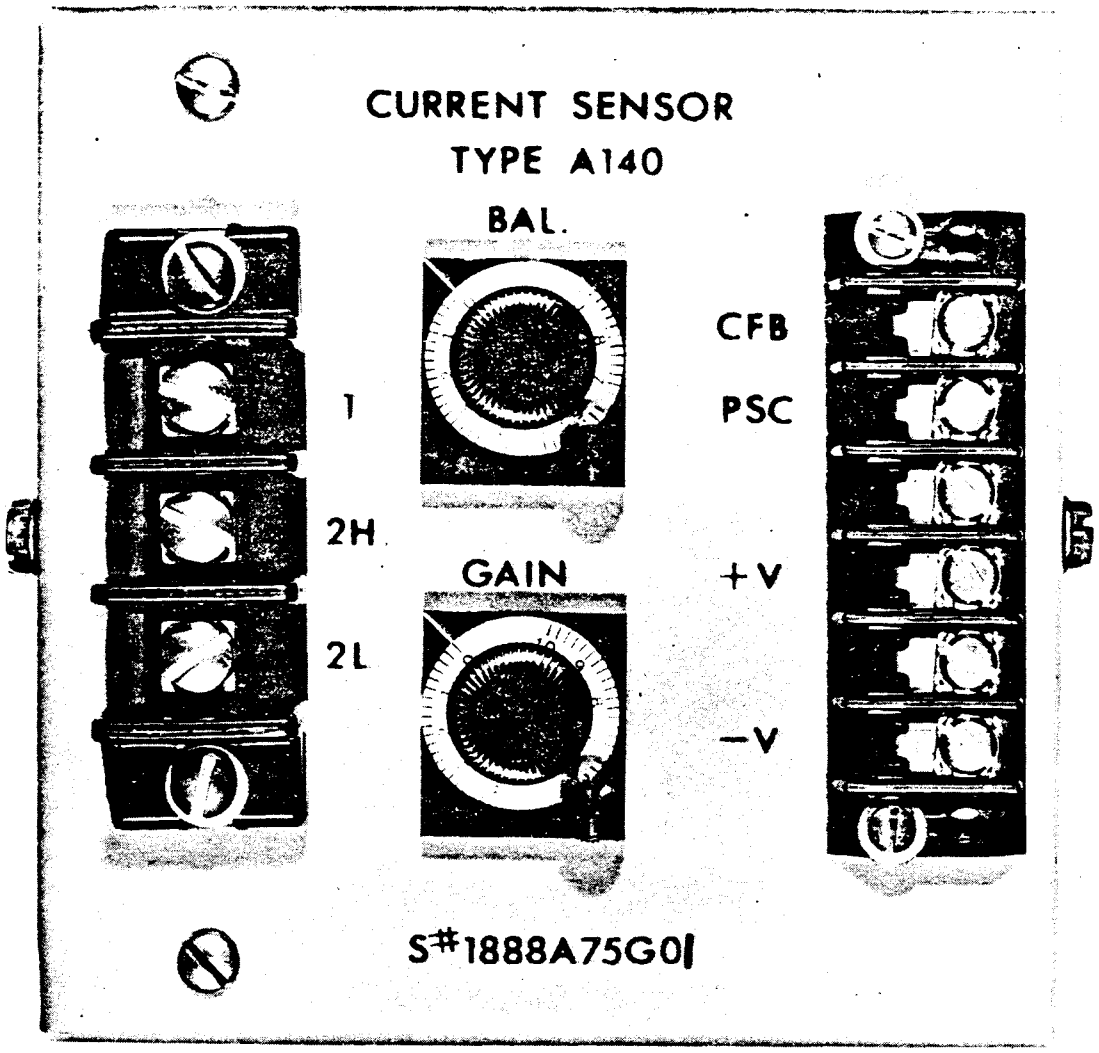
Figure 2 is a photograph of the A140 Current Sensor Module. Figure 1 shows the printed circuit board internal to the unit. A front view locating all components by schematic identification is shown on the last page of the instruction leaflet.

NOTE: Drawing 1888A59 is a multi-group assembly and some components will be missing from some style number pc cards.

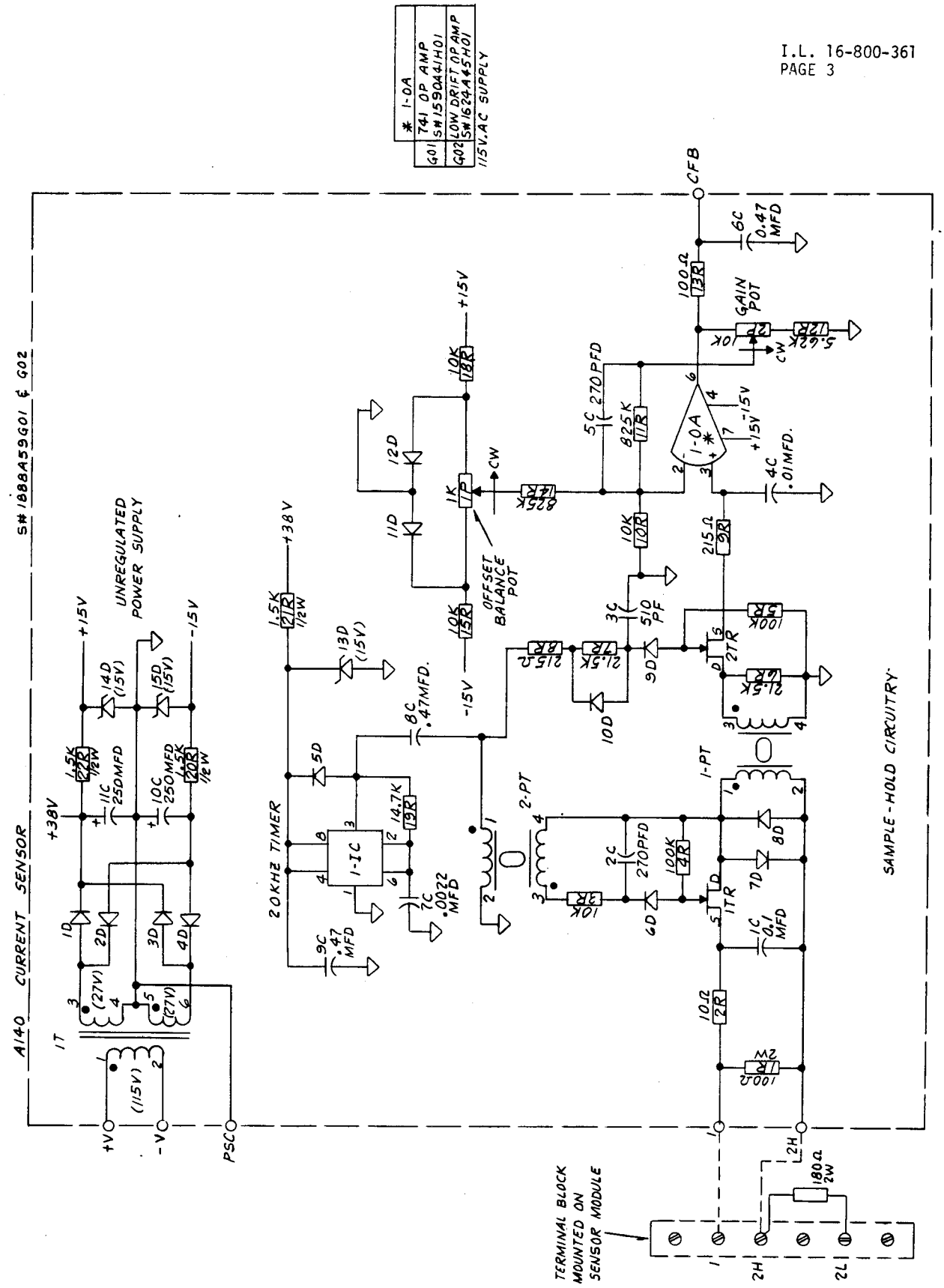


A140 PRINTED - CIRCUIT BOARD

FIGURE 1



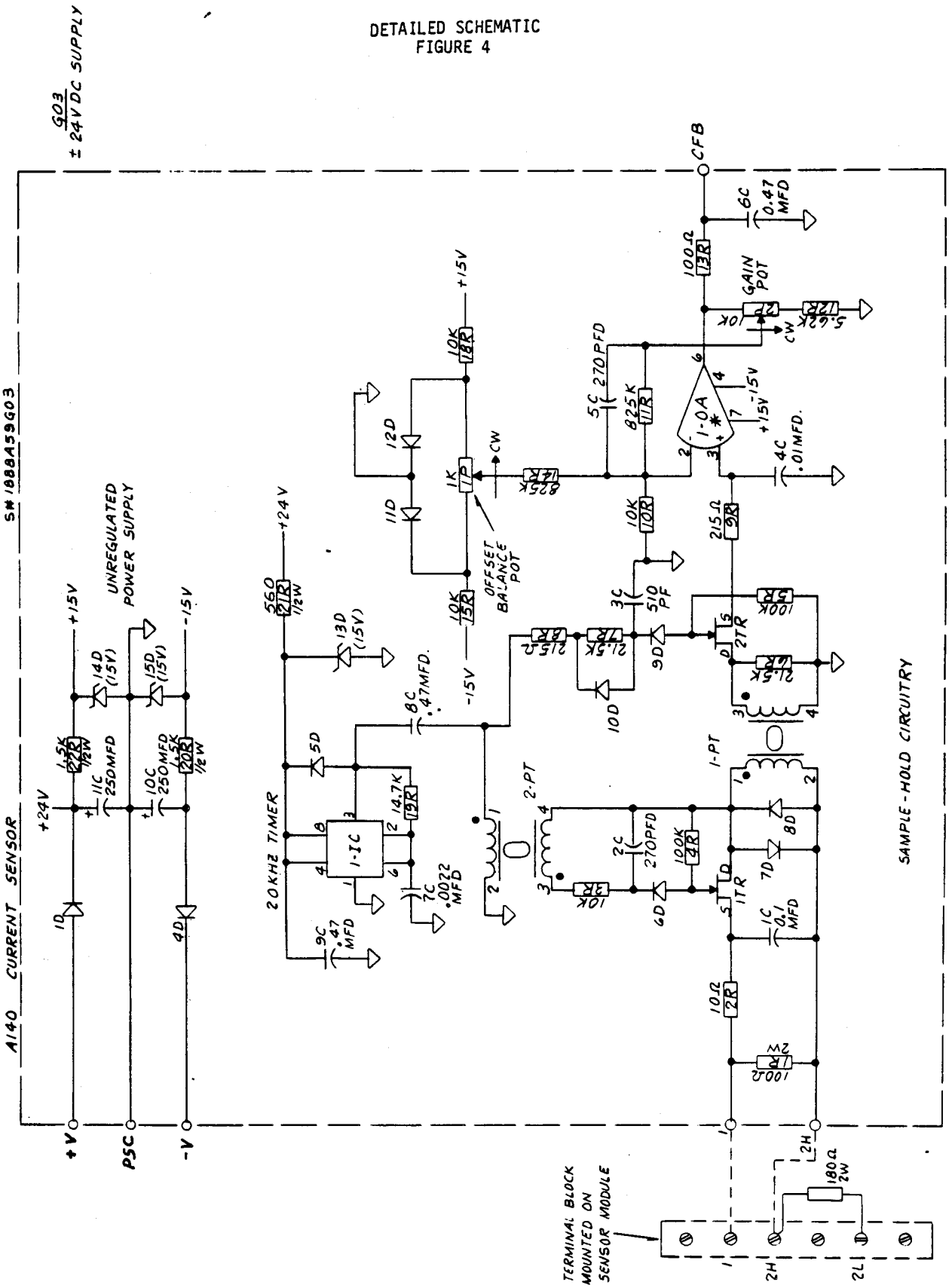
A140 CURRENT SENSOR MODULE
FIGURE 2

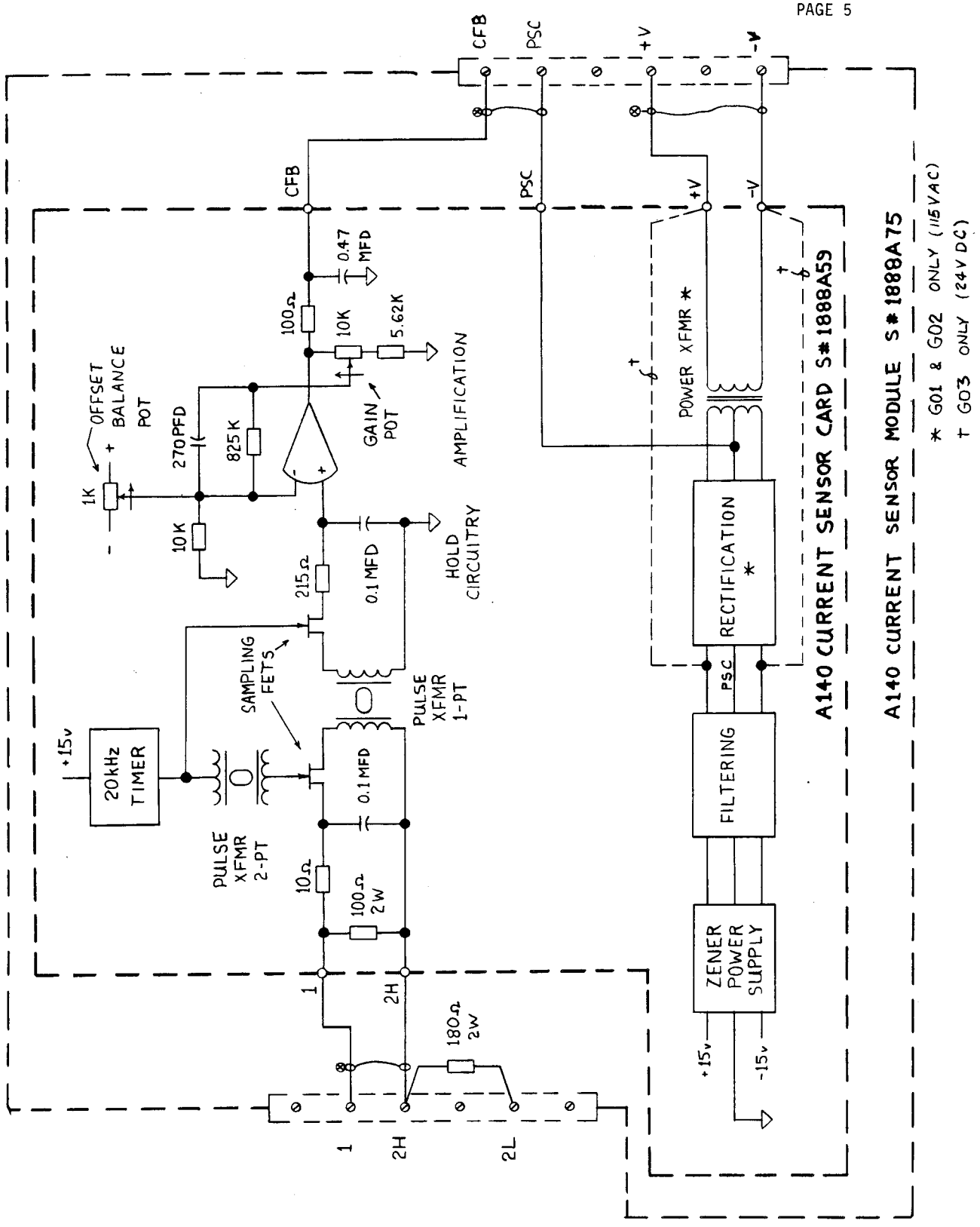


DETAILED SCHEMATIC

FIGURE 3

DETAILED SCHEMATIC
FIGURE 4





SIMPLIFIED SCHEMATIC

FIGURE 5

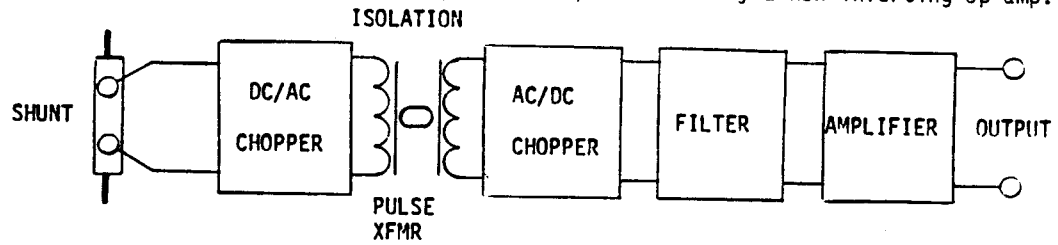
II. DESCRIPTION OF OPERATION

A. Introduction

The A140 Current Sensor is essentially a DC chopper circuit designed for use as a shunt isolator. The card features high-isolation pulse transformers and FET switch sampling controlled by a 20 KHZ timer. Signal amplification is accomplished using an operational amplifier in the non-inverting mode. Two ranges of gain are available: 30 to 80 and 80 to 230. The board contains an offset balance pot in addition to the gain pot.

B. Circuit Operation

Refer to the block diagram of Figure 6. The DC millivolt signal from a current shunt serves as the input to the A140. Chopper circuitry converts this signal into a series of pulses for application across the primary of a pulse transformer. Chopping and filtering in the transformer secondary provide a DC signal for amplification by a non-inverting op amp.



A140 BLOCK DIAGRAM

FIGURE 6

For the following discussion, refer to the simplified scheme of Figure 5 or the detailed schematics of Figures 3 or 4. The A140 printed circuit card contains a 555 timer 1-IC set up for astable operation at approximately 20 KHZ. To obtain free-running operation, the timer is self-triggered by delayed feedback from the output at pin 3 to the trigger and threshold inputs at pins 2 and 6, respectively. Assume that the output is high. Capacitor 7C charges to the 10-volt threshold level, at which point the output switches low. Capacitor 7C then discharges to the 5-volt trigger level, at which point the output switches high and the cycle is repeated. The frequency and duty cycle of the output pulses are thus controlled by the time constant of the feedback. External components 7C and 19R allow precise control of these parameters.

The purpose of the timer is to fix the sampling rate of the sensor. Pulses from the 555 are conditioned and used to drive the gates of FET switches 1TR and 2TR. Capacitor 8C removes the DC component from the timer pulses. Since 1TR is in the sensor input network, which may be floating at several hundred volts to common, a pulse transformer 2-PT is used to isolate the timer and input networks. Resistor 3R and capacitor 2C serve to shape the ±7.5-volt square-wave appearing across the secondary of 2-PT. Diode 6D insures a negative voltage at the gate of 1TR. Gating waveforms to 2TR are similarly shaped. A pulse transformer is not required in this case since 2TR is located in the isolated, low-voltage secondary of 1-PT. Note that 2TR is designed to conduct following 1TR and block prior to 1TR, thus preventing 1TR switching noise from being fed into the hold-amplification circuitry associated with op amp 1-OA.

The millivolt signal from the shunt or bus bar enters the sensor via 1 and 2H and charges capacitor 1C. This signal is sampled 20 times per millisecond by 1TR and applied across the primary of pulse transformer 1-PT. The isolated secondary voltage is then sampled by 2TR, charging 4C through 9R with a 21.5μ sec time constant. Capacitor 4C will hold its charge following the turn-off of 2TR. Resistors 10R and 11R provide an op amp gain of +82.5. Pot 2P can be used to vary this gain between +82.5 and +230, limited by the presence of 12R. Feedback capacitor 5C in conjunction with 11R introduces a 0.22 msec delay. Capacitor 6C is added for protection against external noise being introduced at CFB. Resistor 13R is added for op amp protection against any voltages mistakenly applied at CFB. For 1 positive with respect to 2H (or 2L) the output at CFB will be positive.

A second gain range is available. This change in gain is accomplished by connecting a 180 ohm resistor between points 2H and 2L of the external input terminal block. A voltage divider is created by the combination of this resistor and the 100 ohm input resistor 1R, effectively decreasing the sampled signal and the overall gain by the 0.36 divider ratio.

Thus, using 1 and 2L for input connections reduces the gain range to approximately 30 to 80.

Note that some 20 KHZ offset appears at the op amp non-inverting terminal. Balance circuitry involving pot 1P is provided to null the DC average of this offset and any offset contributed by the operational amplifier. Offset should be nulled with either 1 and 2H or 1 and 2L jumpered, depending on the gain range used, since offset is sensitive to input resistance.

Input leads brought to 1 and 2H or 1 and 2L should be twisted in order to limit noise pick-up. For best results, two-conductor shielded wire can be used, with the shield tied to the can. Also, the purpose of the metallic can is to shield the sensor from external interference; it should be tied to the system common if practical.

For G01 and G02, 115 VAC power is supplied via +V and -V. Transformer 1T takes this 115 VAC signal and provides a 54 VAC centertapped secondary voltage. A diode bridge and capacitors rectify and filter this signal to provide a ±38-volt DC supply which is then zenered down to ±15-volts, as required. Magnetic coupling between the power supply transformer 1T and pulse transformer 1-PT generates 60 HZ noise at CFB. High-permeability shielding of 1-PT reduces the peak-to-peak noise level from an observed maximum of 110mV to approximately 15mV with gain pot 2P full clockwise. With 2P full counterclockwise, peak-to-peak noise is reduced to approximately 5mV.

For G03, the transformer and diodes 2D and 3D are removed, jumpers are added between transformer pads 1-3 and 2-6, and ±24 VDC power is supplied via +V and -V. Resistors 20R, 21R, and 22R are sized to provide the same amount of current through the zener diodes as in G01 and G02.

III. CHARACTERISTICS & RATINGS

A. Power Supply:

GROUP	POWER SOURCE	CONNECTIONS	LOADING
G01 - G02	115 VAC 50/60 HZ	+V and -V	5.0 VA
G03	±24 VDC	+V and -V	+V 36mA -V 18mA

B. CFB Polarity:

If 1 is positive with respect to 2H or 2L, CFB is positive with respect to PSC.

C. CFB Output Range:

±10 volts for $R_{LOAD} \geq$ 2K
±12 volts for $R_{LOAD} \geq$ 10K

D. Gain Range:

Range 1:	80 to 230	Inputs to 1 and 2H
Range 2:	30 to 80	Inputs to 1 and 2L

E. Bias Pot Range:

For an op amp gain of 100, CFB may be varied approximately ±700mV with 1 & 2H jumpered.

F. Risetime & Time Constant:

For an op amp gain of 100 and a 100mV step input, risetime is measured at approximately 0.6 msec with a 0.35 msec time contant.

G. Bandwidth:

Bandwidth is measured at approximately 550 Hz. An effect of the sampling technique is that spikes in the frequency response occur at multiples of the sampling frequency. The output frequency differs from input frequency near these points.

H. Maximum Common Mode Voltage: 1000 VRMS

I. Output Drift:

Over a -10°C to +60°C ambient temperature range, offset is within the range shown below with 1 and 2H jumpered

G01, G03	<	100mV DC
G02	<	5mV DC

J. Input Signal:

The A140 is designed for use with standard 50mV and 100mV current shunts. Note that the overall gain of shunt and sensor should be such that instantaneous voltage peaks at CFB do not exceed the CFB output limits as specified in section C.

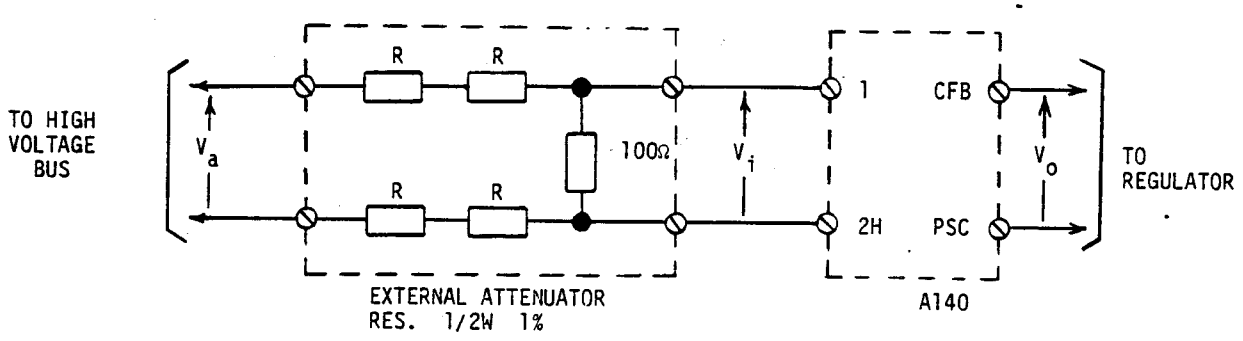
IV. VOLTAGE SENSOR

A. Introduction

The A140 may be applied as a voltage sensor if appropriate external attenuation is used. The peak input to the A140 must be brought down to the 50mV to 100mV range. Overall circuit gain must be low enough such that peak bus voltage does not drive the sensor into saturation (see section III C). Otherwise, A140 operation remains the same as discussed previously.

B. Application

For high-voltage isolation and sensing the general scheme shown in Figure 7 should be used.



A140 VOLTAGE SENSOR SCHEME

FIGURE 7

As an example, assume that a maximum signal of roughly 50mV is desired at V_i. The following chart shows possible external attenuation resistors (R) that may be used in this application for various bus voltages (V_a). The A140 gain adjustment range is also given.

CHART 1

RATED V_a	R		RATED V_i	RATED V_o RANGE	
	THEORETICAL	ACTUAL		GAIN = 80	GAIN = 230
120 V	30.0K	31.6K	47.4 mV	3.80V	10.9V
240	60.0K	68.1K	44.0	3.52	10.1
500	125K	121K	51.6	4.13	11.9
600	150K	147K	51.0	4.08	11.7
700	175K	178K	49.2	3.93	11.3
1000	250K	261K	47.9	3.83	11.0

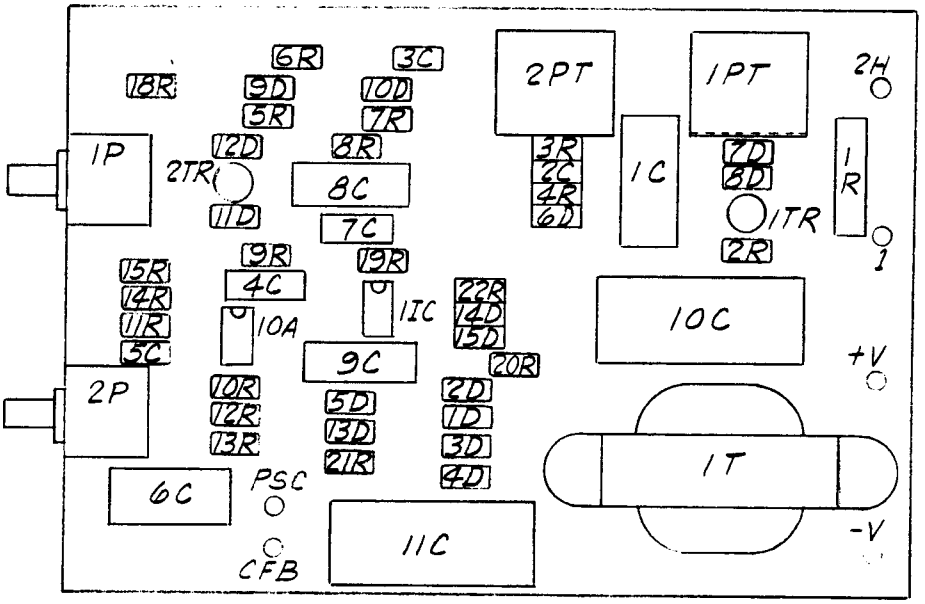
To find R for a given bus voltage V_a and peak sensor input V_i:

$$V_i = V_a \frac{50}{50 + 4R}$$

$$R = 12.5 \left(\frac{V_a}{V_i} - 1 \right)$$

where 50 is the parallel combination of the 100-ohm attenuator resistor and the 100-ohm A140 input resistance. R is chosen close to the theoretical value. A140 gain may then be adjusted between 80 and 230 to obtain the desired control voltage V_o.

Note that in this application, control voltage (V_o) offset balancing should be done with the attenuator connected to the A140 as shown in Figure 7 and V_a = 0.



TOP VIEW OF PC BOARD
FIGURE 8